User's Manual

ISL8024DEMO2Z

A Power Module for Xilinx RFSoC Applications Demonstration Board

Industrial Analog and Power

Rev.1.00 Mar 2019

1. Overview

The ISL8024DEMO2Z is a low-noise power module to power the high-speed data converters on Xilinx RFSoCs. It is used as a power module that plugs into an application board.

1.1 Key Features

- Three input voltage sources: 5.0V, 3.3V, and 1.8V
- Five output voltages: ADC_AVCC, ADC_AVCCAUX, DAC_AVCC, DAC_AVTT, and DAC_AVCCAUX
- PMBus interface that can digitally control the voltage set-point and margining of the DAC_AVTT rail
- All rails have differential point-of-load voltage sensing
- Additional low-pass filter to reduce output voltage ripple related to the switching regulator while maintaining high efficiency

1.2 Specifications

Table 1. Specifications

Rail	Typical Voltage (V)	Voltage Set-Point Accuracy (%)	Adjustment Range (V)	Maximum Current (A)
ADC_AVCC	0.925	±1	0.70 to 1.16	2.0
ADC_AVCCAUX	1.8	±1	1.35 to 2.25	2.0
DAC_AVCC	0.925	±1	0.70 to 1.16	3.5
DAC_AVCCAUX	1.8	±1	1.35 to 2.25	2.0
DAC_AVTT	2.5 and 3.0	±1	1.88 to 3.75	2.0

1.3 Ordering Information

Part Number	Description
ISL8024DEMO2Z	ISL8024 demonstration board

1.4 Related Literature

For a full list of related documents, visit our website:

- ISL8024, ISL28191 device pages

2. Functional Description

Overall system power blocks are shown in Figure 1. The 1.8V and 2.5V output voltage is derived from 5V, and the 0.925V rails are derived from 3.3V. Each rail is followed by an additional LC filter to reduce output voltage ripple.

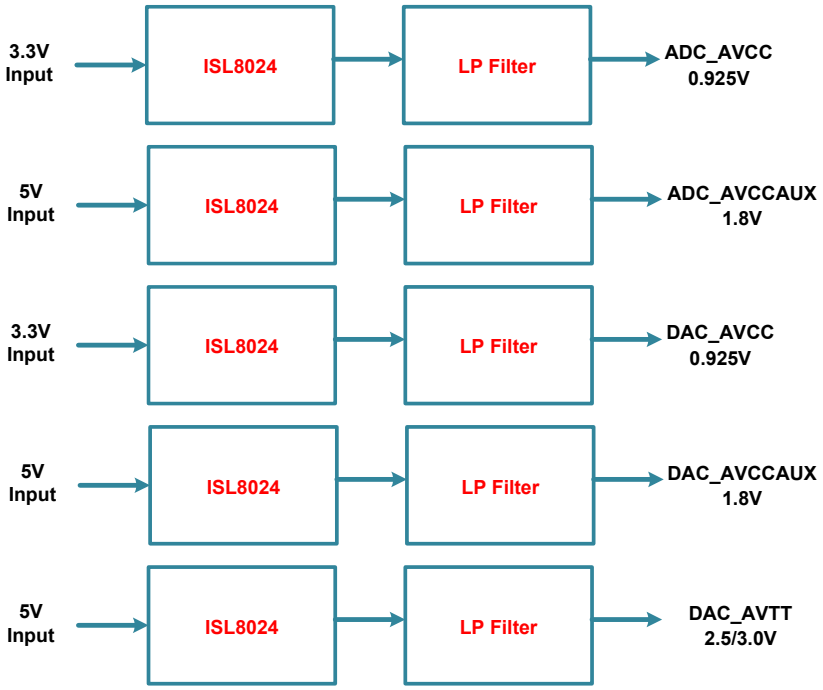

Figure 1. Simplified Block Diagram of the ISL8024DEMO2Z Power Module Board

Based on the specification, the ISL8024 is used as the DC/DC converter solution and as the main component. The ISL8024 has ±0.8% VFB tolerance across the temperature range of -40°C to +85°C. It has a programmable switching frequency up to 2MHz to reduce the size of the LC filters. To further reduce the output voltage ripple, a 2nd stage LC filter is used after the LC filter for the buck regulators. To reduce the conductor trace voltage drop related to the board connectors and to achieve the best load point voltage regulation, a remote sense scheme is used with the ISL28191 as a differential amplifier. Reduce the EMI to the upstream converters, a dedicated LC filter is also used as the input filter for each rail. An example power block and its related schematics is shown in Figure 2, demonstrating the device components.

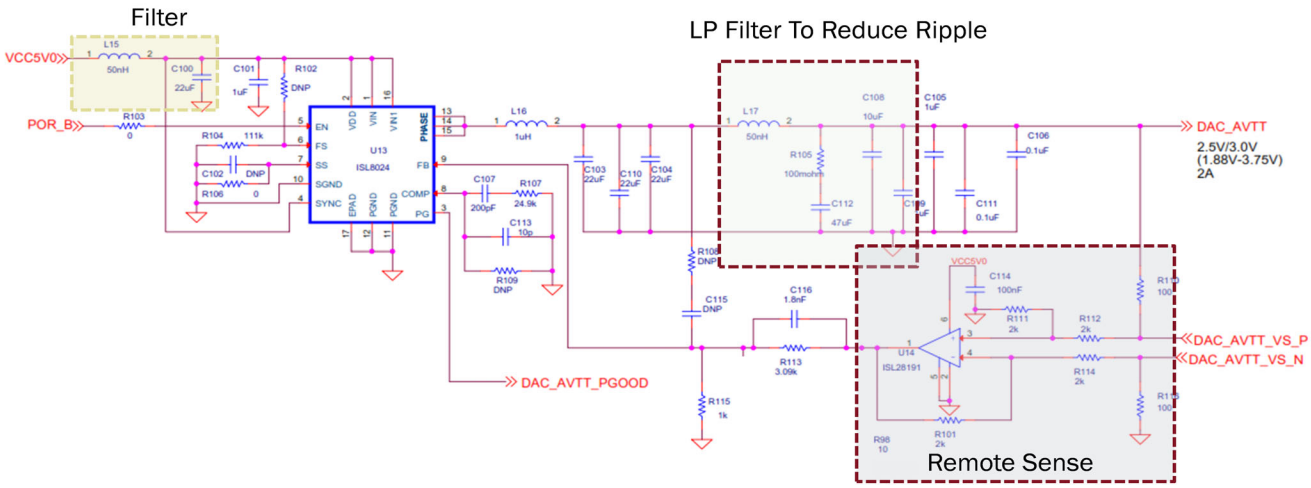

Figure 2. Single Rail Power Block

Low-pass filter design requires a balance between phase loss and V_{OUT} ripple attenuation. The LC filter used in Figure 2 has about 40dB noise attenuation at 2MHz and a phase drop of 20° at 100kHz as shown in Figure 3. The compensation design of the ISL8024 regulator has been tuned to accommodate this phase loss.

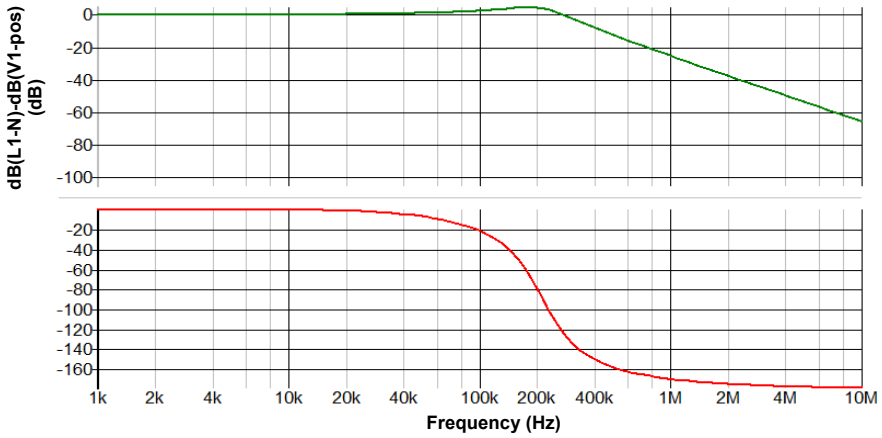

Figure 3. 2nd Stage LC Filter Characteristics

2.1 Quick Start Guide

The ISL8024DEMO2Z board can be powered on or off with external connectors, or plugged into Xilinx application boards.

3. PCB Layout Guidelines

3.1 ISL8024DEMO2Z Demonstration Board

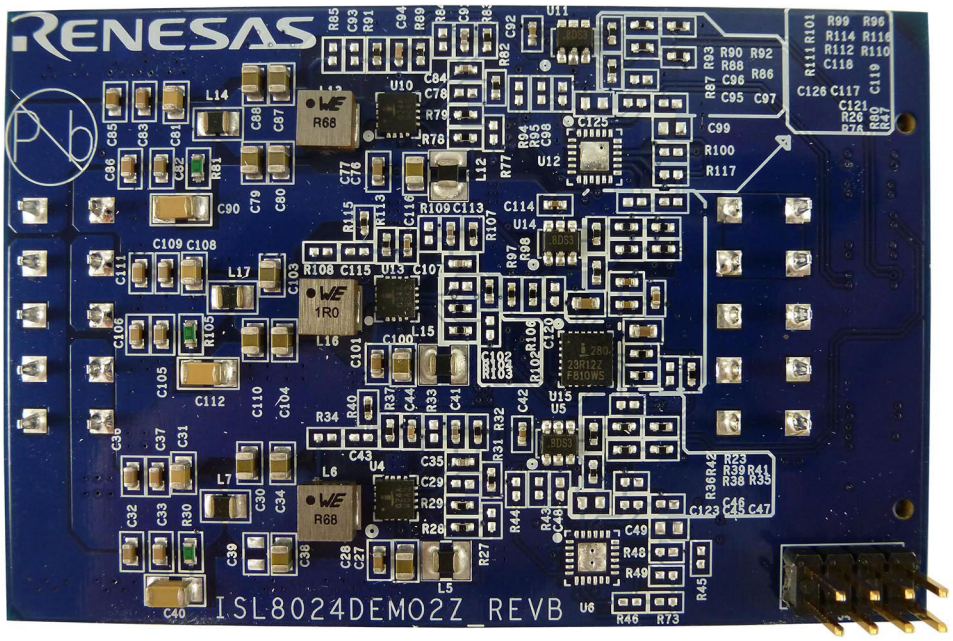

Figure 4. ISL8024DEMO2Z Demonstration Board (Bottom)

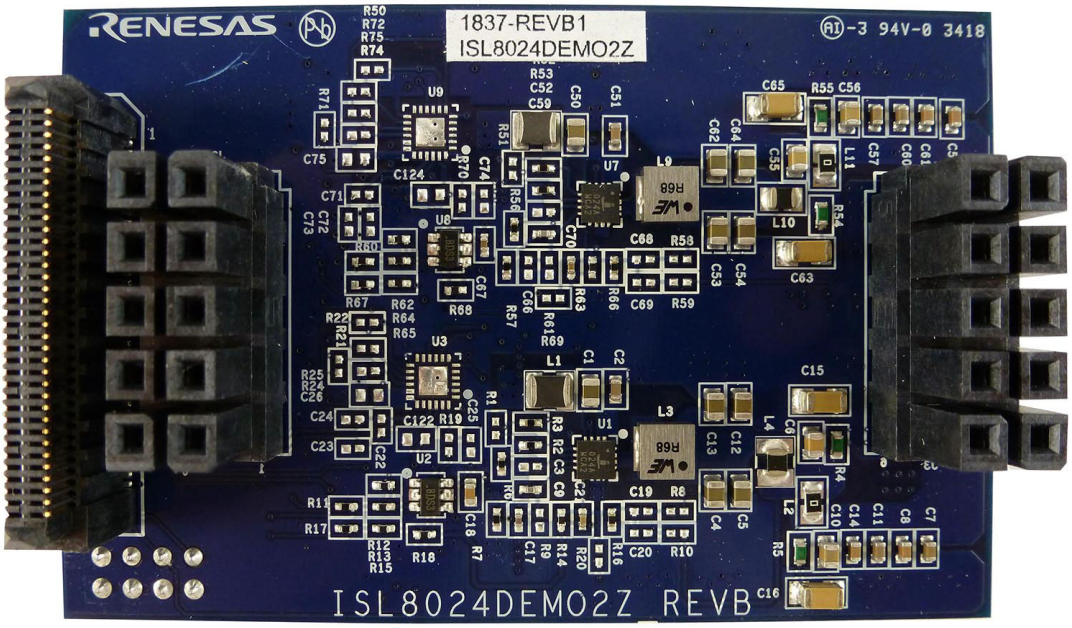

Figure 5. ISL8024DEMO2Z Demonstration Board (Top)

3.2 ISL8024DEMO2Z Circuit Schematic

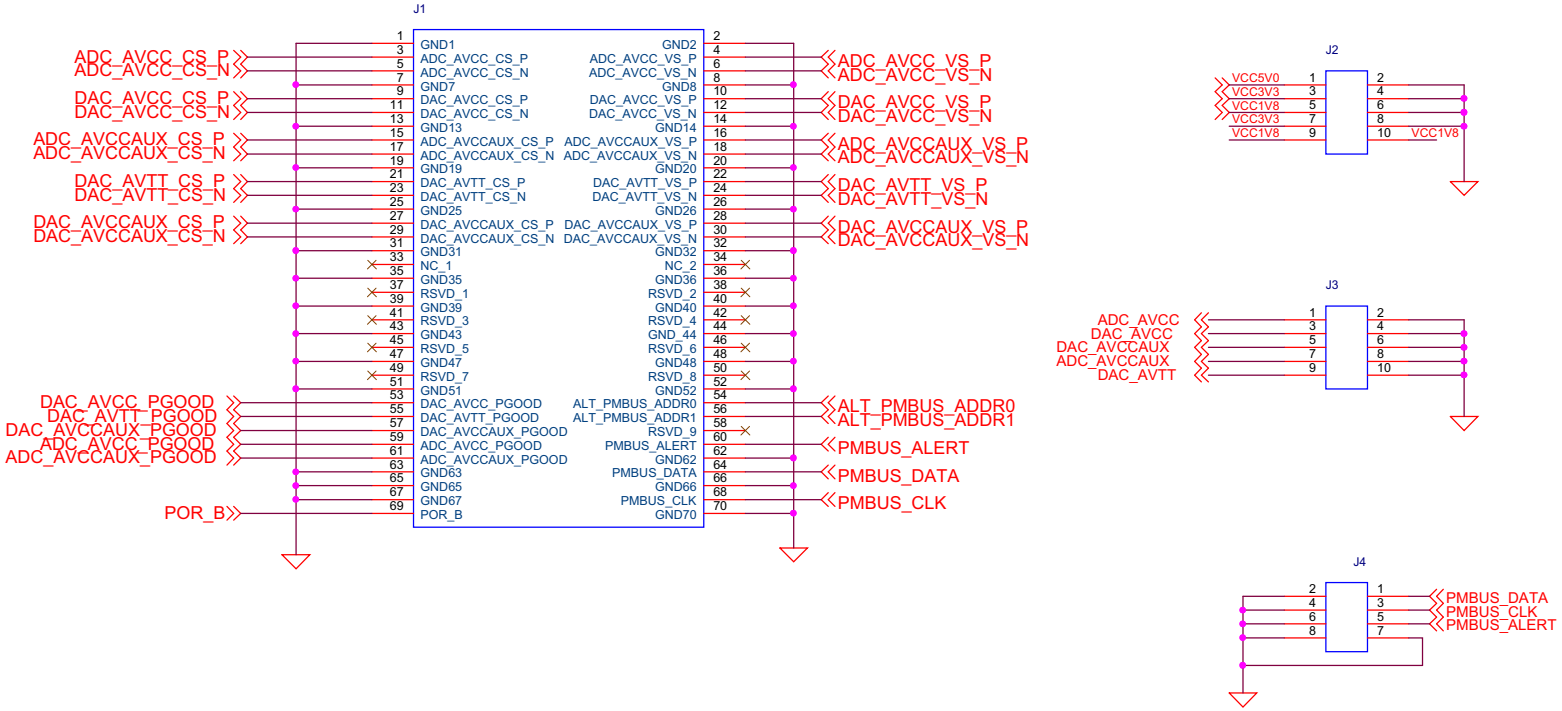

Figure 6. ISL8024DEMO2Z Schematics, Page 1

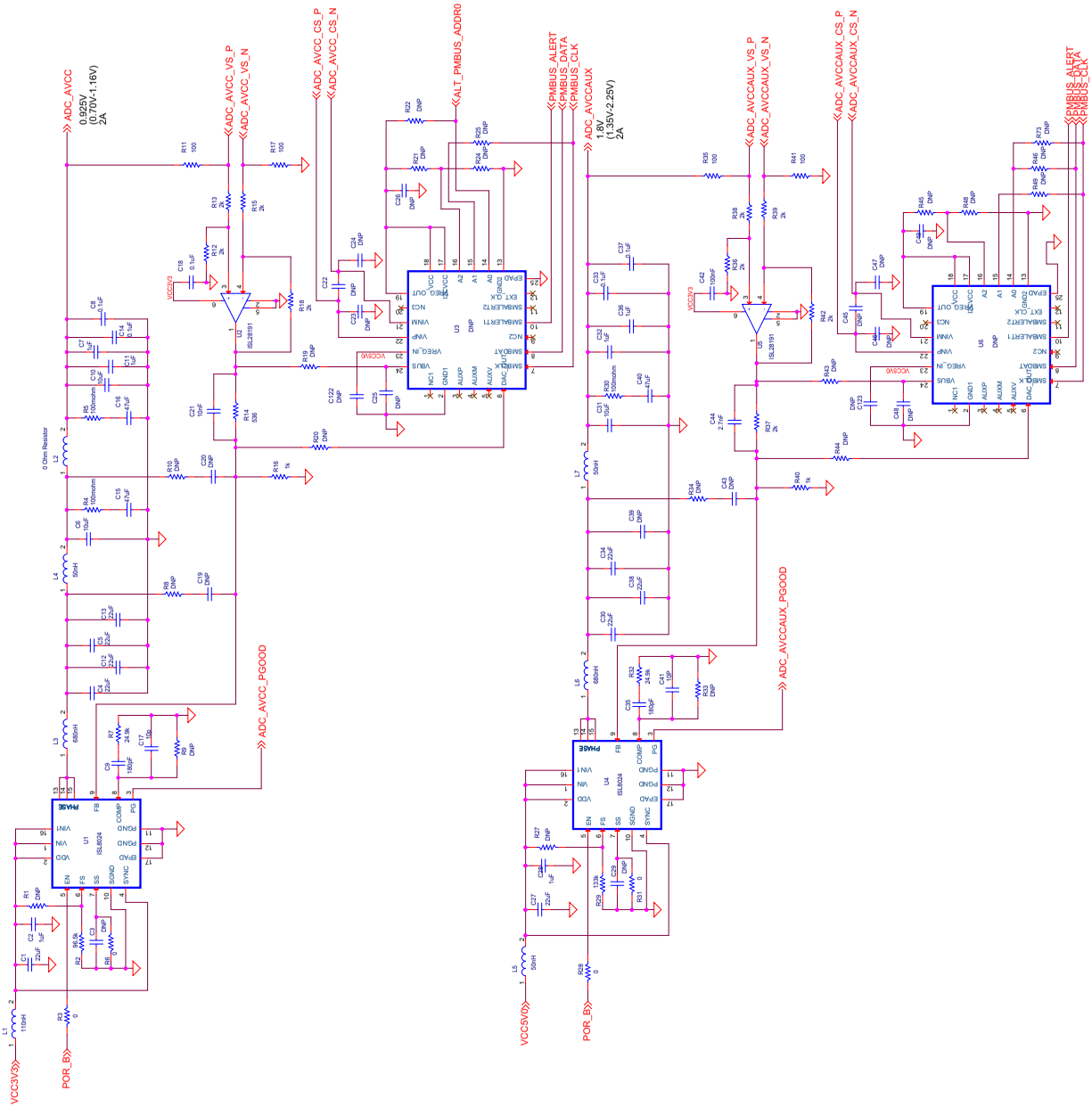

Figure 7. ISL8024DEMO2Z Schematics, Page 2

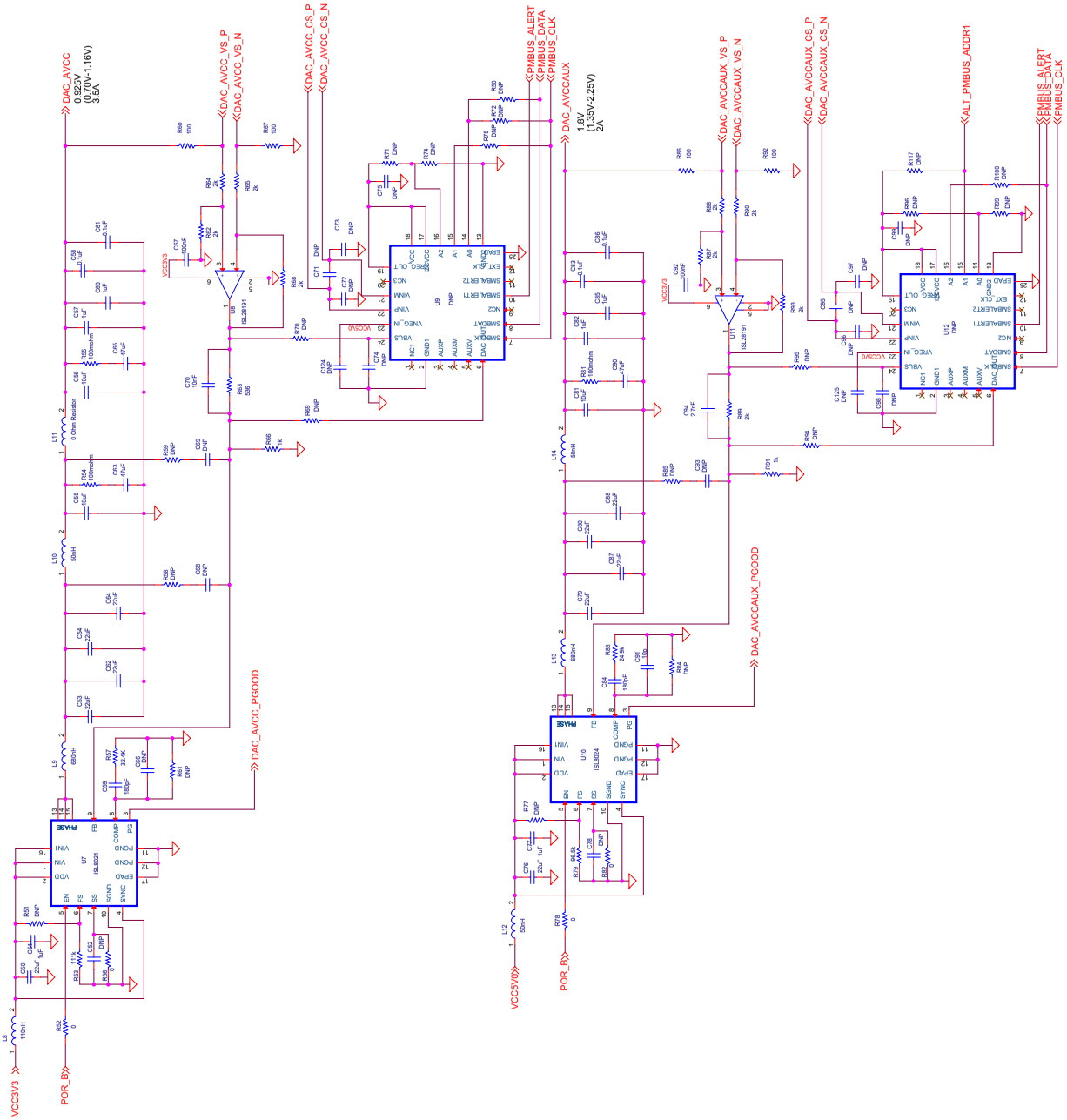

Figure 8. ISL8024DEMO2Z Schematics, Page 3

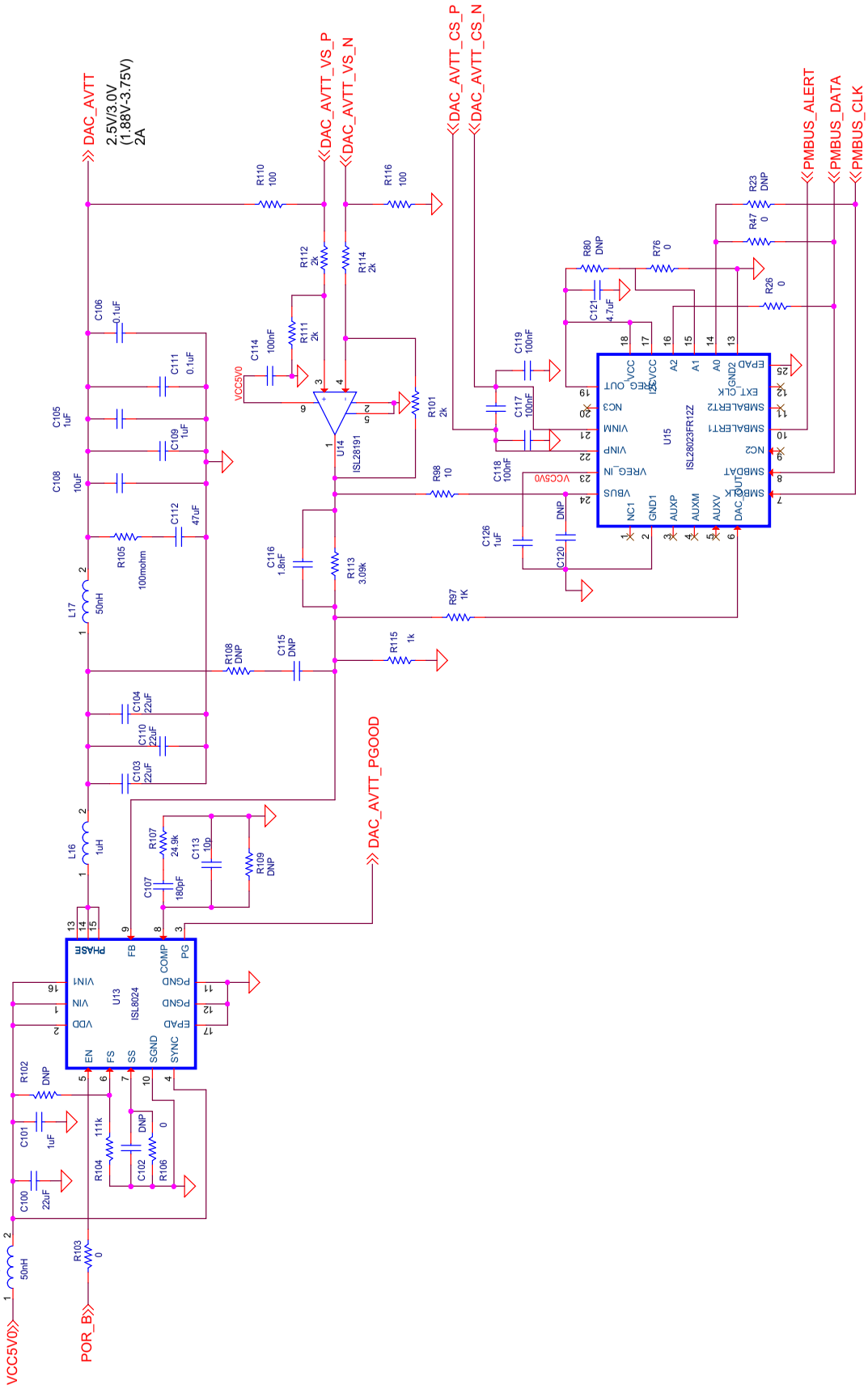

Figure 9. ISL8024DEMO2Z Schematics, Page 4

3.3 Bill of Materials

Qty	Reference Designator	Description	PCB Footprint	Part Number
23	C1, C4, C5, C12, C13, C27, C30, C34, C38, C50, C53, C54, C62, C64, C76, C79, C80, C87, C88, C100, C103, C104, C110	22µF	SMC0805, X5R, 10V	
16	C2, C7, C11, C28, C32, C36, C51, C57, C60, C77, C82, C85, C101, C105, C109, C126	1µF	SMC0603, X5R, 10V	
17	C3, C19, C20, C25, C29, C43, C48, C52, C68, C69, C74, C78, C93, C98, C102, C115, C120, C122, C123, C124, C125, C26, C49, C75, C99,	DNP		
7	C6, C10, C31, C55, C56, C81, C108	10µF	SMC0805, X5R, 10V	
11	C8, C14, C18, C33, C37, C58, C61, C83, C86, C106, C111	0.1µF	SMC0603, X7R, 10V	
5	C9, C35, C59, C84, C107	180pF	SMC0402, COG, 10V	
7	C15, C16, C40, C63, C65, C90, C112	47µF	SMC1206, X5R, 10V	
4	C17, C41, C113, C91	10PF	SMC0402, COG, 10V	
2	C21, C70	10nF	SMC0402, X7R, 10V	
7	C42, C67, C92, C114, C117, C118, C119	100nF	SMC0402, X5R, 10V	
13	C22, C23, C24, C45, C46, C47, C71, C72, C73, C95, C96, C97, C66	DNP		
1	C121	4.7µF	SMC0603, X5R, 10V	
2	C44, C94	2.7nF	SMC0402, X7R, 10V	
1	C116	1.8nF	SMC0402, X7R, 10V	
1	C39	DNP	SMC0805	
24	R3, R6, R26, R28, R31, R47, R52, R56, R76, R78, R82, R103, R106	0	SMR0402	
1	J1	CON70A	ERM8_035_08_LDV_K_TR	ERM8_035_08_LDV_K_TR
2	J2, J3	CON10A	IPBS-105-01-T-D	IPBS-105-01-T-D
1	J4	CON8A	Jumper8	5-146256-4
10	L4, L5, L12, L15, L7, L10, L14, L17	50nH	L805	74479978105
2	L2, L11	0Ω	SMR0805	
4	L3, L6, L9, L13	680nH	IND_WE7443835XXX	744383560068
2	L1, L8	110nH	WE7447997XXX	74479899111
1	L16	1µH	IND_WE7443835XXX	74438356010
24	R1, R8, R9, R10, R23, R24, R27, R33, R34, R48, R50, R51, R58, R59, R61, R73, R74, R77, R80, R84, R85, R96, R102, R108, R109, R71, R75, R72, R99, R100	DNP	SMR0402	
2	R2, R79	97.6k	SMR0402, 1%	
7	R4, R5, R30, R54, R55, R81, R105	100mΩ	SMR0603, 1%	RL0816S-R10-F
4	R7, R32, R83, R107	24.9k	SMR0402, 1%	
10	R11, R17, R35, R41, R60, R67, R86, R92, R110, R116	100	SMR0402, 1%	
22	R12, R13, R15, R18, R36, R37, R38, R39, R42, R62, R64, R65, R68, R87, R88, R89, R90, R93, R101, R111, R112, R114	2k	SMR0402, 1%	
2	R14, R63	536	SMR0402, 1%	

Qty	Reference Designator	Description	PCB Footprint	Part Number
1	R57	32.4k		
6	R16, R40, R66, R97, R115, R91	1k	SMR0402, 1%	
1	R98	10	SMR0402, 1%	
1	R29	133k	SMR0402, 1%	
	R20, R44, R69, R70, R95, R19, R43, R21, R25, R45, R46, R49, R94	DNP		
2	R22, R117	DNP	SMR0402, 1%	
2	R53, R104	110k	SMR0402, 1%	
1	R113	3.09k	SMR0402, 1%	
5	U1, U4, U7, U10, U13		QFN16_118X118_197_EPD	ISL8024IRTAJZ
5	U2, U5, U8, U11, U14		SOT23-6	ISL28191FHZ
1	U15		QFN24_157X157_197_EP	ISL28023FR12Z
3	U3, U6, U9, U12	DNP		

3.4 Board Layout

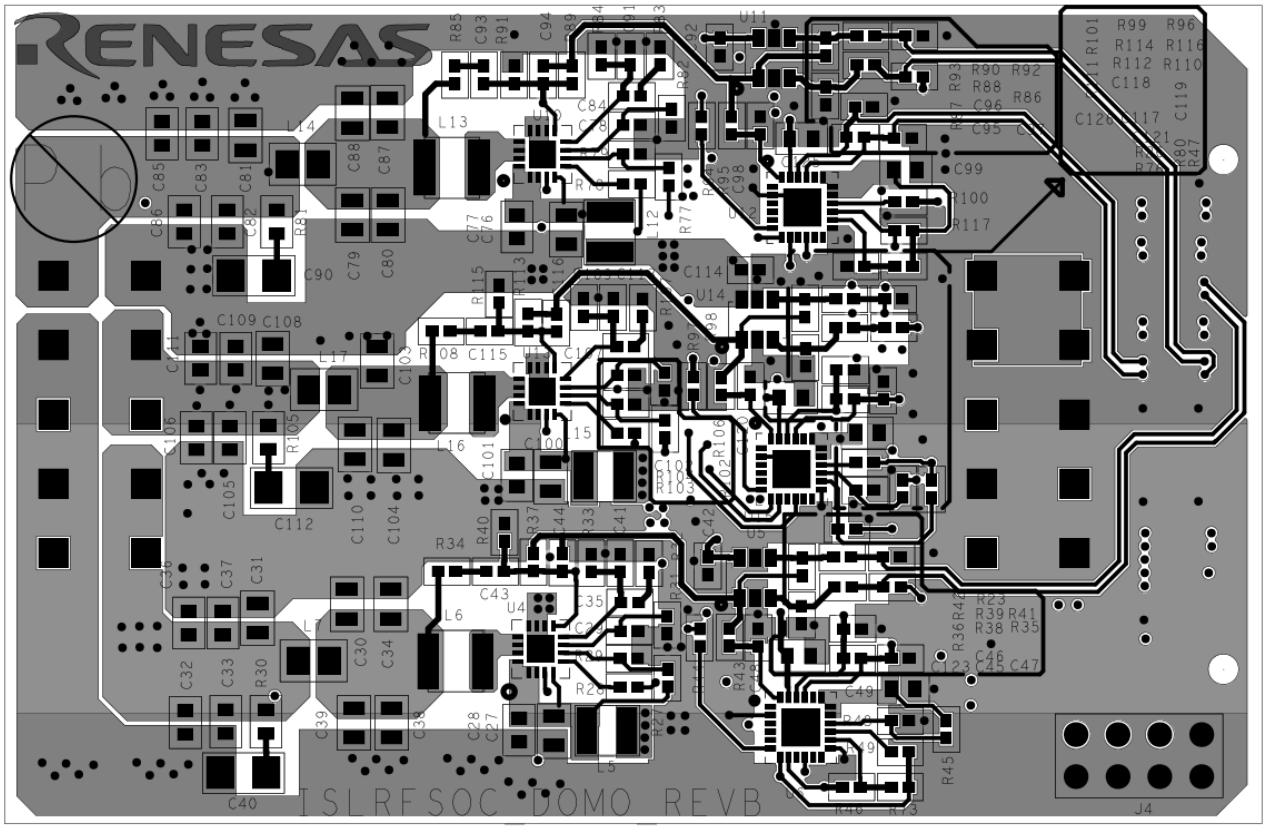

Figure 10. Top Layer

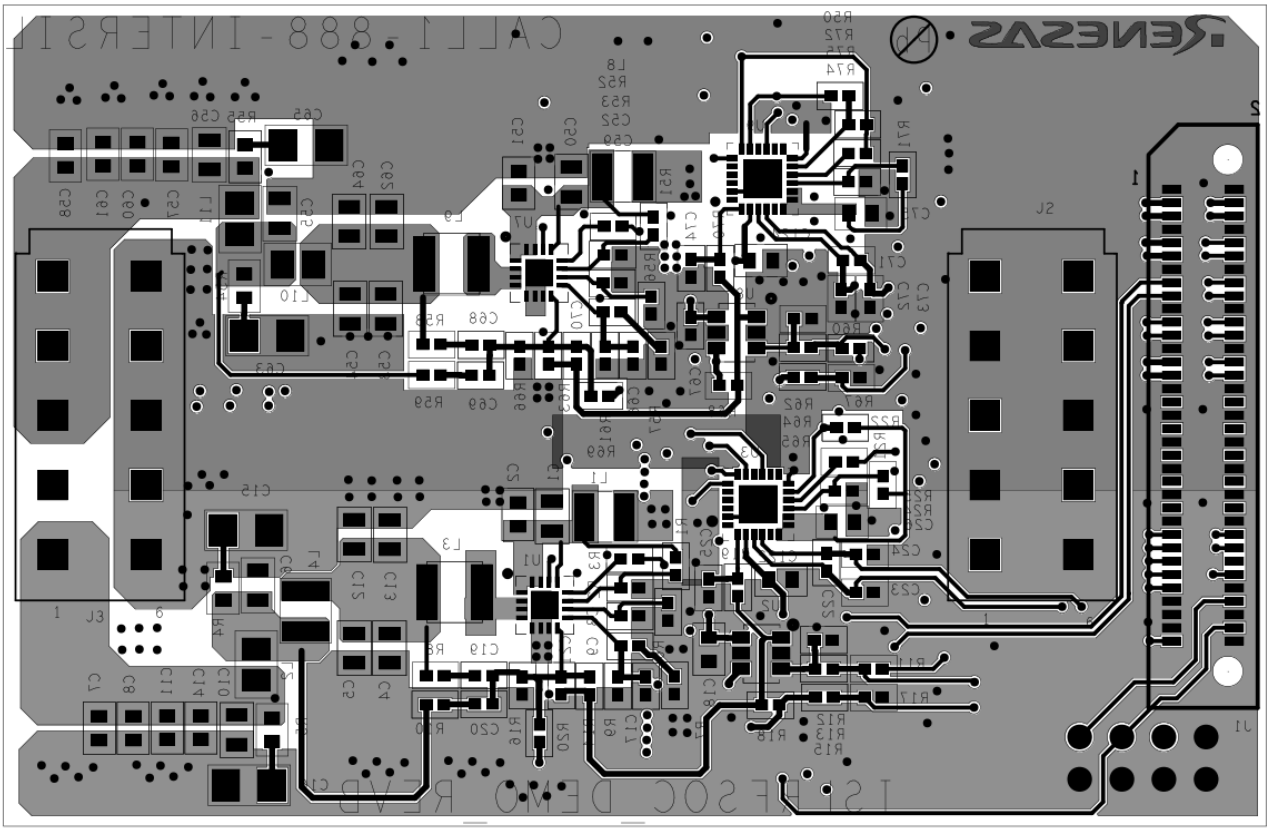

Figure 11. Bottom Layer

4. Typical Performance Curves

Efficiency was tested on these boards.

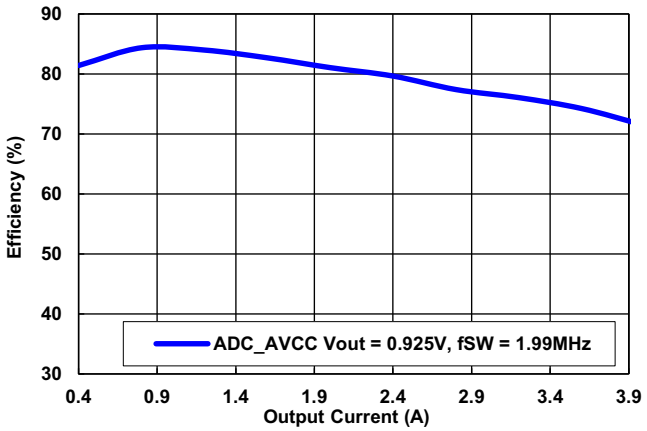

Figure 12. ADC_AVCC Rail, Peak Efficiency = 84%

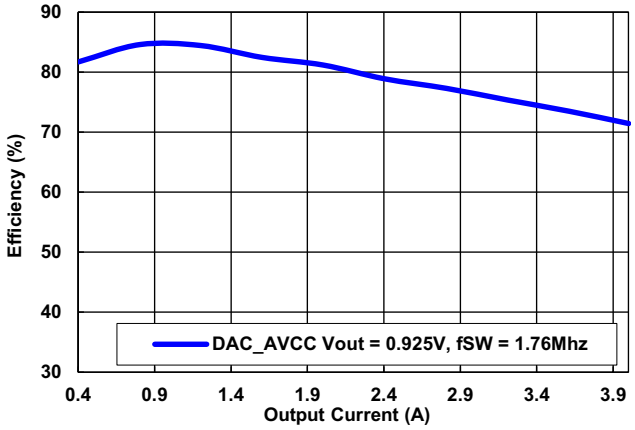

Figure 13. DAC_AVCC Rail, Peak Efficiency = 85%

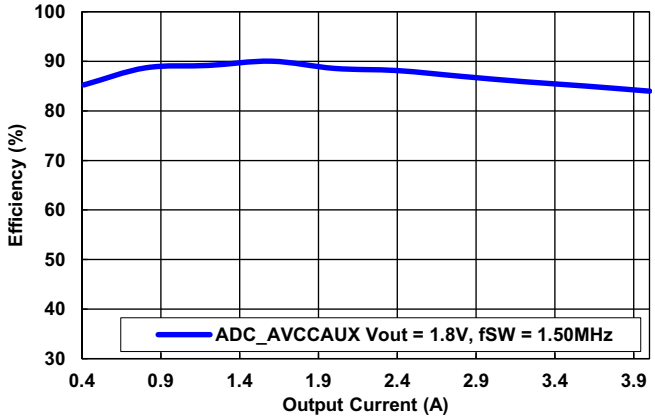

Figure 14. ADC_ACCAUX Rail, Peak Efficiency = 90%

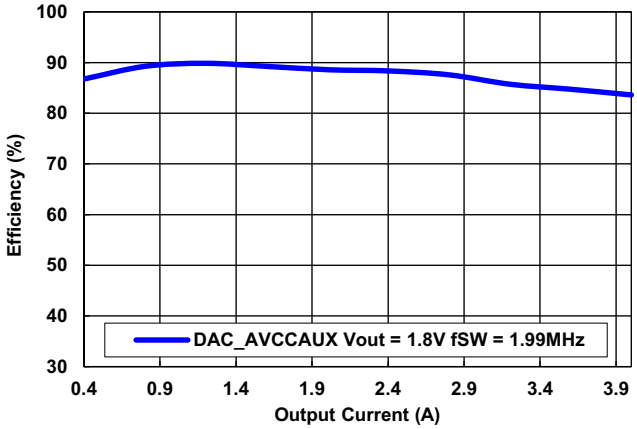

Figure 15. DAC_AVCCAUX Rail, Peak Efficiency = 90%

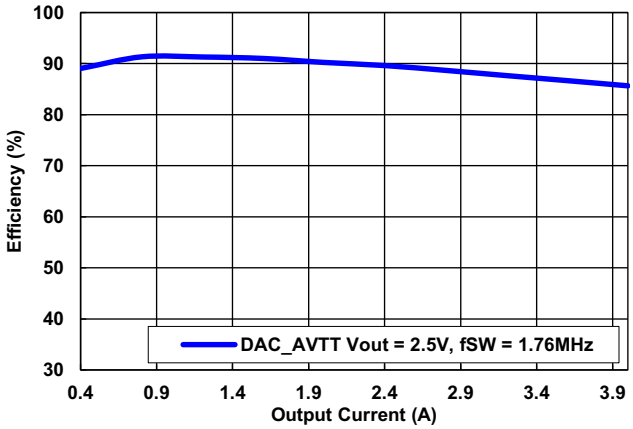

Figure 16. 5.DAC_AVTT Rail, Peak Efficiency = 92%

5. Summary

The ISL8024DEMO2Z demonstration board integrates five output voltage rails into a high-density plug-in power module. It offers a very low output voltage ripple with dual LC filters. It has very tight load-point voltage regulation with remote voltage sense to compensate for board copper loss and interconnection voltage drop. Digital programmability is also available as an option. LC filters at each input rail alleviate the EMI interactions between different rails.

6. Revision History

Rev.	Date	Description
1.00	Mar 5, 2019	The Typical Performance Curves heading was modified: “output voltage ripple” was deleted. Typical Performance Curves 13, 15, 17, 19, and 21 were deleted, and the remaining figures were renumbered.
0.00	Oct 10, 2018	Initial release

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(Rev.4.0-1 November 2017)

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