RENESAS

ISL8104EVAL1Z

Using the ISL8104 PWM Controller Evaluation Board

The ISL8104 is a simple single-phase PWM controller for a synchronous buck converter with integrated MOSFET driver that operates from +8V to +14.4V bias supply voltage. The ISL8104 employs voltage-mode control with dual-edge modulation to achieve fast transient response. The controller features the ability to safely start-up into prebiased output loads and provides protection against overcurrent fault events. Overcurrent protection is implemented using topside MOSFET r_{DS(ON)} sensing, eliminating the need for a current sensing resistor.

The ISL8104 evaluation board highlights the operations of the controller in a DC/DC application.

ISL8104 Reference Design

The evaluation board is designed to optimize for the output voltage and current specifications shown in Table [1.](#page-0-0)

TABLE 1. ISL8104 EVALUATION BOARD DESIGN PARAMETERS

Design Procedure

The following sections illustrate simple design steps and component selections for a converter using the ISL8104.

Output Inductor Selection

The output inductor is chosen by the desired inductor ripple current, which is typically set to be approximately 40% of the rated output current. The desired output inductor can be calculated using Equation [1:](#page-0-1)

$$
L = \frac{V_{IN} - V_{OUT}}{\Delta I} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{F_{SW}}
$$

= $\frac{14.4 - 1.8}{0.4 \cdot 20} \times \frac{1.8}{14.4} \times \frac{1}{300 \times 10^3}$ (EQ. 1)
= 0.66_µH

In the evaluation board, a 0.68 μ H inductor with 1.6m Ω DCR (Vishay's IHLP5050FD-R68) is employed. This yields approximately 0.64W conduction loss in the inductor.

Output Capacitor Selection

The output capacitors are generally selected by the output voltage ripple and load transient response requirements. ESR and capacitor charge are major contributions to the output voltage ripple. Assuming that the total output capacitance is

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sufficient, then the output voltage ripple is dominated by the ESR, which can be calculated using Equation [2](#page-0-2).

$$
V_{RIPPLE} = \Delta I_L \cdot ESR
$$
 (EQ. 2)

To meet the $30mV_{P-P}$ output voltage ripple requirement, the effective ESR should be less than $4m\Omega$.

The output voltage response to a transient load is contributed from ESL, ESR and the amount of output capacitance. With V_{IN} >> V_{OUT} , the amplitude of the voltage excursions can be approximated using Equation [3:](#page-0-3)

$$
\Delta V = \frac{L \cdot I_{tran}^2}{C_{OUT} \cdot V_{OUT}}
$$
 (EQ. 3)

With 0.68µH inductor and 0A to 20A step load, the total output capacitance of 1900µF is required for 80mV output voltage transient. In the evaluation board, four of Fujitsu's FP-4R0RE561M-L8 are employed.

Input Capacitor Selection

The input bulk capacitors selection criteria are based on the capacitance and RMS current capability. The RMS current rating requirement for the input capacitor is approximated in Equation [4:](#page-0-5)

$$
I_{IN(RMS)} = \sqrt{I_0^2(D - D^2) + \frac{\Delta I^2}{12}D} \qquad D = \frac{V_O}{VIN}
$$
 (EQ. 4)

In this application, the RMS current for the input capacitor is 7.2A; therefore, three of Sanyo's 35ME330AX are used.

Small ceramic capacitors for high frequency decoupling are also required to control the voltage overshoot across the MOSFETs.

MOSFET Selection

The ISL8104 requires two N-Channel power MOSFETs as the main and the synchronous switches. These should be selected based in $r_{DS(ON)}$, gate supply requirements and thermal management requirements.

The total power loss on MOSFET consists of conduction loss and switching loss, as shown in Equation [5:](#page-0-4)

$$
P_{MOSFET(TOT)} = P_{cond} + P_{sw}
$$
 (EQ. 5)

In this relatively small duty cycle design, the low-side MOSFET conducts current most of the time. To optimize the converter efficiency, select the high-side MOSFET with low gate charge for fast switching transition and low-side MOSFET with low r_{DS(ON)}.

The budget power losses in each high-side and low-side MOSFETs is 1W.

LOW-SIDE MOSFET SELECTION

The low-side MOSFET's RMS current is approximated in Equation [6:](#page-1-1)

$$
I_{L(RMS)} = I_{OUT} \cdot \sqrt{1 - D} \cdot \sqrt{1 + \frac{1}{12} \cdot \left(\frac{\Delta I_L}{I_{OUT}}\right)^2} \approx 18.6 \text{A}
$$
 (EQ. 6)

Assuming a target conduction loss of 0.5W in the low-side MOSFET, the ON-resistance of the low-side MOSFET must be less than 1.5m Ω . Two of Infineon's BSC030N03LS are employed in the evaluation board. The conduction loss in the low-side MOSFETs is calculated using Equation [7:](#page-1-2)

$$
P_{\text{LFET}(\text{cond})} = I_{\text{L}(\text{RMS})}^{2} \cdot r_{\text{DS}(\text{ON})}\Big|_{\text{LFET}} = 0.52W
$$
 (EQ. 7)

The switching loss in the low-side MOSFETs is dominated by the loss in body diode, which can be calculated using Equation [8:](#page-1-3)

$$
P_{\text{diode}} = I_0 \cdot t_D \cdot V_F \cdot F_{SW} = 0.4W \tag{EQ.8}
$$

Where t_D is the total dead time in each switching period (\sim 60ns) and V_F is the forward voltage drop of MOSFET's body diode.

The total power dissipation in the low-side MOSFETs is calculated using Equation [9:](#page-1-4)

$$
P_{\text{LFET(TOT)}} = 0.92W \tag{EQ.9}
$$

HIGH-SIDE MOSFET SELECTION

For the high-side MOSFET selection, first we assume that the conduction loss and the switching loss contribute evenly to the total power dissipation.

The high-side MOSFET's RMS current is approximated using Equation [10:](#page-1-5)

$$
I_{H(RMS)} = I_{OUT} \cdot \sqrt{D} \cdot \sqrt{1 + \frac{1}{12} \cdot \left(\frac{\Delta I_L}{I_{OUT}}\right)^2} \approx 7.8 \text{A}
$$
 (EQ. 10)

Hence, the required ON-resistance of the high-side MOSFET is $8.2 \text{m}\Omega$. Infineon's BSC080N03LS is selected. The conduction loss in the high-side MOSFET is calculated using Equation [11](#page-1-6):

$$
P_{HFET(cond)} = I_{H(RMS)}^{2} \cdot r_{DS(ON)} \Big|_{HFET} = 0.49W
$$
 (EQ. 11)

The switching loss in the high-side MOSFET can be approximated using Equation [12:](#page-1-0)

$$
P_{HFET(SW)} = \frac{1}{2} \cdot I_0 \cdot V_{IN} \cdot t_{tr} \cdot F_{SW} + \frac{1}{2} \cdot C_{OSS} \cdot V_{IN}^2 \cdot F_{SW}
$$

= 0.21W (EQ. 12)

where t_{tr} is the combined ON and OFF MOSFET transition times.

The total power dissipation in high-side MOSFET is shown in Equation [13:](#page-1-7)

$$
P_{HFET(TOT)} = 0.7W
$$
 (EQ. 13)

Overcurrent Protection Setting

The OCP function is enabled with the drivers at start-up. OCP is implemented via a resistor (R_{TSOC}) and a capacitor (C_{TSOC}) connecting the TSOC pin and the drain of the topside MOSFET. An internal 200µA current source develops a voltage across R_{TSOC} , which is then compared with the voltage developed across the top-side MOSFET at turn on, as measured at the LX pin. When the voltage drop across the MOSFET exceeds the voltage drop across the resistor, a sourcing OCP event occurs. C_{TSOC} is placed in parallel with R_{TSOC} to smooth the voltage across R_{TSOC} in the presence of switching noise on the input bus.

A 120ns blanking period is used to reduce the current sampling error due to leading-edge switching noise. An additional simultaneous 120ns low pass filter is used to further reduce measurement error due to noise.

The OCP trip point varies mainly due to MOSFET $r_{DS(ON)}$ variations and layout noise concerns. To avoid overcurrent tripping in the normal operating load range, find the R_{OCSFT} resistor from Equation [14](#page-1-8) with:

- 1. The maximum $r_{DS(ON)}$ at the highest junction temperature
- 2. The minimum I_{TSOC} from the specification table in datasheet

Determine the overcurrent trip point greater than the maximum output continuous current at maximum inductor ripple current.

Simple OCP Equation

$$
R_{TSOC} = \frac{I_{OC_SOURCE} \cdot r_{DS(ON)}}{200 \mu A}
$$

Detailed OCP Equation

$$
R_{TSOC} = \frac{\left(I_{OC_SOURCE} + \frac{\Delta I}{2}\right) \bullet r_{DS(ON)}}{I_{TSOC} \bullet N_{T}}
$$
 (EQ. 14)

 N_T = NUMBER OF TOP-SIDE MOSFETs

$$
\Delta I = \frac{V_{IN} - V_{OUT}}{F_{SW} \cdot L_{OUT}} \cdot \frac{V_{OUT}}{V_{IN}}
$$

With Infineon's BSC080N03LS as the top-side MOSFET and R_{TSOC} of 1.15k Ω , the overcurrent trip point on the evaluation board has been approximately set to 25A.

FIGURE 1. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN

Feedback Compensator

Type-III network is recommended for compensating the feedback loop. Figure [1](#page-2-0) shows Type-III compensation configuration for the ISL8104.

With the inductor and output capacitor selected as described in the previous sections, the poles and zero of the power stage can be summarized in Equation [15:](#page-2-2)

$$
F_0 = \frac{1}{2 \times \pi \times \sqrt{L \times C}} = 4.1 \text{kHz}
$$

\n
$$
F_{ESR} = \frac{1}{2 \times \pi \times C \times ESR} = 47.3 \text{kHz}
$$
 (EQ. 15)

1. With a value of 23.2k Ω for R₁, select R₄ for the target output voltage of 1.8V using Equation [16](#page-2-3):

$$
R_4 = R_1 \times \frac{V_{REF}}{V_{OUT} - V_{REF}}
$$

= 11.5k Ω (EQ. 16)

2. With the desired feedback loop bandwidth at approximately 50kHz, R_2 can be calculated using Equation [17:](#page-2-4)

$$
R_2 = \frac{V_{\text{OSC}} \cdot R_1 \cdot F_{BW}}{d_{\text{max}} \cdot V_{\text{IN}} \cdot F_0}
$$
 (EQ. 17)
= 44.2 kΩ

3. Select C_1 such that F_{Z1} is located at 1.5kHz:

$$
C_1 = \frac{1}{2\pi \cdot R_2 \cdot 1.5 \times 10^3}
$$
 (EQ. 18)

$$
\approx 2.2nF
$$

4. Select C_2 such that F_{P1} is located at F_{ESR} :

$$
C_2 = \frac{C_1}{2\pi \cdot R_2 \cdot C_1 \cdot F_{ESR} - 1}
$$
 (EQ. 19)
\n
$$
\approx 82pF
$$

5. Select R_3 such that F_{Z2} is located at F_{LC} and F_{P2} is located at 150kHz:

$$
R_3 = \frac{R_1}{\frac{150 \times 10^3}{F_0} - 1} \approx 655 \Omega
$$

$$
C_3 = \frac{1}{2\pi \cdot R_3 \cdot 150 \times 10^3} \approx 1.5 \text{nF}
$$
 (EQ. 20)

A more detailed explanation of designing compensation networks for buck converters with voltage mode control can [be found in TB417 entitled "Designing Stable Compensation](http://www.intersil.com/data/tb/tb417.pdf) Networks for Single Phase Voltage Mode Buck Regulators".

Evaluation Board Performance

Figures [2](#page-2-1) and [3](#page-3-0) show photographs of the ISL8104EVAL1Z and ISL8104EVAL2Z boards, respectively.

FIGURE 2. ISL8104EVAL1Z

FIGURE 3. ISL8104EVAL2Z FIGURE 4. SOFT-START

Power and Load Connections

Terminals J1 and J2 are connected to the input of the power stage. For single rail supply, the IC bias supply can be tied to the converter input supply through pin 1 and 2 of the Jumper J5. When using separate supplies, provide the IC bias voltage to terminal J6 with pin 2 and pin 3 of J5 connected together. The load can be connected to terminal J4 and J5. TP6 and TP3 can be used for DMM to measure output voltage. The toggle switch, SW1, can be used to disable the controller.

Start-up

When the voltages at V_{CC} and P_{VCC} of ISL8104 exceed their rising POR thresholds, a 30µA current source driving the SS pin is enabled. Upon the SS pin exceeding 1V, the ISL8104 begins ramping the non-inverting input of the error amplifier from GND to the System Reference. During initialization, the MOSFET drivers pull TGATE to LX and BGATE to PGND.

If the ISL8104 is utilizing the internal reference, then as the SS pin's voltage ramps from 1V to 3V, the soft-start function scales the reference input (positive terminal of error amp) from GND to VREF (0.597V nominal). Figure [4](#page-3-1) shows the start-up profile of the ISL8104 in relation to the start-up of the 12V input supply and the bias supply.

Soft-Start with Pre-Biased Output

If the output is pre-biased to a voltage less than the expected value, the ISL8104 will detect that condition. Drivers are held in tri-state (TGATE pulled to LX, BGATE pulled to PGND) at the beginning of a soft-start cycle until two PWM pulses are detected. The bottom-side MOSFET is turned on first to provide for charging of the bootstrap capacitor. This method of driver activation provides support for start-up into prebiased loads by not activating the drivers until the control loop has entered its linear region, thereby substantially reducing output transients that would otherwise occur had the drivers been activated at the beginning of the soft-start cycle.

FIGURE 5. SOFT-START WITH PRE-BIASED OUTPUT

Output Ripple

Figure [6](#page-4-0) shows the ripple voltage on the output of the regulator.

FIGURE 6. OUTPUT RIPPLE (20MHz BW)

Transient Performance

Figures [7](#page-4-2), [8](#page-4-3) and [9](#page-4-4) show the response of the output voltage when subjected to transient loading from 0A to 15A at 1A/µs.

FIGURE 7. TRANSIENT RESPONSE

FIGURE 8. TRANSIENT RESPONSE

FIGURE 9. TRANSIENT RESPONSE

Efficiency

ISL8104 based regulators enable the design of highly efficient systems. The efficiency of the evaluation board using a 12V input supply is shown in Figure [10](#page-4-1).

FIGURE 10. EVALUATION BOARD EFFICIENCY (V_{OUT} = 1.8V)

References

[For Intersil documents available on the web, go to](http://www.intersil.com/) [http://www.intersil.com/.](http://www.intersil.com/)

- 1. ISL8104 Data Sheet "8V to 14V, Single-Phase [Synchronous Buck Pulse-Width Modulation \(PWM\)](http://www.intersil.com/cda/deviceinfo/0,1477,ISL8104,0.html) Controller With Integrated Gate Drivers", Intersil Corporation
- 2. Tech Brief TB417 , "Designing Stable Compensation [Networks for Single Phase Voltage Mode Buck Regulators",](http://www.intersil.com/data/tb/tb417.pdf) Intersil Corporation

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ISL8104EVAL1Z Bill of Materials

ISL8104EVAL1Z Bill of Materials **(Continued)**

ISL8104EVAL1Z Printed Circuit Board Layers

FIGURE 11. ISL8104EVAL1Z - TOP LAYER (SILKSCREEN) FIGURE 12. ISL8104EVAL1Z - TOP LAYER (COMPONENT SIDE)

FIGURE 13. ISL8104EVAL1Z - LAYER 2 FIGURE 14. ISL8104EVAL1Z - LAYER 3

FIGURE 15. ISL8104EVAL1Z - BOTTOM LAYER FIGURE 16. ISL8104EVAL1Z - BOTTOM LAYER (SOLDER SIDE)

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ISL8104EVAL2Z Bill of Materials

ISL8104EVAL2Z Bill of Materials **(Continued)**

ISL8104EVAL2Z Printed Circuit Board Layers

FIGURE 17. ISL8104EVAL2Z - TOP LAYER (SILKSCREEN) FIGURE 18. ISL8104EVAL2Z - TOP LAYER (COMPONENT SIDE)

FIGURE 19. ISL8104EVAL2Z - LAYER 2 FIGURE 20. ISL8104EVAL2Z - LAYER 3

FIGURE 21. ISL8104EVAL2Z - BOTTOM LAYER FIGURE 22. ISL8104EVAL1Z - BOTTOM LAYER (SOLDER SIDE)

