ISL8118EVAL1Z

Using the ISL8118 PWM Controller Evaluation Board

AN1489
Rev 0.00
June 20, 2009

Introduction

The ISL8118 is a single-phase PWM controller for a synchronous buck converter with an integrated MOSFET driver that operates from +3.3V to +20V bias supply voltage. Utilizing voltage-mode operation with input voltage feed-forward compensation, the ISL8118 maintains a constant loop gain, providing optimal transient response for applications with a wide input operating voltage range.

The controller features the ability to safely start-up into prebiased output loads and provides protection against overcurrent fault events. Overcurrent protection is implemented using both topside and bottomside MOSFET $r_{DS(ON)}$ sensing, eliminating the need for a current sensing resistor. Dual sensing allows the ISL8118 to detect overcurrent faults at the very low and very high duty cycles that can result from the ISL8118's wide input range.

The ISL8118 evaluation board highlights the operations of the controller in a DC/DC application.

ISL8118 Reference Design

The evaluation board is designed to optimize for the output voltage and current specifications shown in Table 1.

TABLE 1. ISL8118 EVALUATION BOARD DESIGN PARAMETERS

PARAMETER	MIN	TYP	MAX
Operating Input Voltage (V_{IN})	4.5V	12V	20V
Optimal Input Voltage (V_{IN})	9.6V	12V	14.4V
Output Voltage (V_{OUT})		1.8V	
Output Voltage Ripple		30mV	
Continuous Load Current			25A
Switching Frequency		300kHz	

Design Procedure

The following sections illustrate simple design steps and component selections for a converter using the ISL8118.

Output Inductor Selection

The output inductor is chosen by the desired inductor ripple current, which is typically set to be approximately 35% of the rated output current. The desired output inductor can be calculated using Equation 1:

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{F_{SW}} = \frac{14.4 - 1.8}{0.35 \cdot 25} \times \frac{1.8}{14.4} \times \frac{1}{300 \times 10^3} = 0.6\mu H \quad \text{(EQ. 1)}$$

In the evaluation board, a 0.68µH inductor with a 1.6mΩ DCR (Vishay's IHLP5050FD-R68) is employed. This yields approximately 1W conduction loss in the inductor.

Output Capacitor Selection

The output capacitors are generally selected by the output voltage ripple and load transient response requirements. ESR and capacitor charge are major contributions to the output voltage ripple. Assuming that the total output capacitance is sufficient, then the output voltage ripple is dominated by the ESR, which can be calculated using Equation 2.

$$V_{RIPPLE} = \Delta I_L \cdot ESR \quad \text{(EQ. 2)}$$

To meet the $30mV_{P-P}$ output voltage ripple requirement, the effective ESR should be less than 3.5mΩ.

The output voltage response to a transient load is contributed from ESL, ESR and the amount of output capacitance. With $V_{IN} >> V_{OUT}$, the amplitude of the voltage excursions can be approximated using Equation 3:

$$\Delta V = \frac{L \cdot I_{tran}^2}{C_{OUT} \cdot V_{OUT}} \quad \text{(EQ. 3)}$$

With 0.68µH inductor and 0A to 25A step load, the total output capacitance of 1600µF is required for 150mV output voltage transient. In the evaluation board, five of Sanyo's 6TPF330M9L are employed.

Input Capacitor Selection

The input bulk capacitors selection criteria are based on the capacitance and RMS current capability. The RMS current rating requirement for the input capacitor is approximated in Equation 4:

$$I_{IN(RMS)} = \sqrt{I_O^2(D - D^2) + \frac{\Delta I^2}{12}D} \qquad D = \frac{V_O}{VIN} \quad \text{(EQ. 4)}$$

In this application, the RMS current for the input capacitor is 8.98A; therefore, two of Nippon Chemi-con's EKZE350ELL561MJ25S are used.

Small ceramic capacitors for high frequency decoupling are also required to control the voltage overshoot across the MOSFETs.

MOSFET Selection

The ISL8118 requires two N-Channel power MOSFETs as the main and the synchronous switches. These should be selected based on $r_{DS(ON)}$, gate supply requirements and thermal management requirements.

The total power loss on MOSFET consists of conduction loss and switching loss, as shown in Equation 5:

$$P_{MOSFET(TOT)} = P_{cond} + P_{sw} \quad \text{(EQ. 5)}$$

In this relatively small duty cycle design, the low-side MOSFET conducts current most of the time. To optimize the converter efficiency, select the high-side MOSFET with low gate charge for fast switching transition and low-side MOSFET with low $r_{DS(ON)}$.

The budget power losses in each high-side and low-side MOSFETs are 1W.

LOW-SIDE MOSFET SELECTION

The low-side MOSFET's RMS current is approximated in Equation 6:

$$I_{L(RMS)} = I_{OUT} \cdot \sqrt{1-D} \cdot \sqrt{1 + \frac{1}{12} \cdot \left(\frac{\Delta I_L}{I_{OUT}}\right)^2} \approx 23.1A \quad \text{(EQ. 6)}$$

Assuming a target conduction loss of 0.7W in the low-side MOSFET, the total ON-resistance of the low-side MOSFETs must be approximately less than 1.3mΩ. Two of Infineon's BSC018N04LS are employed in the evaluation board. The conduction loss in the low-side MOSFETs can be calculated using Equation 7:i

$$P_{BFET(cond)} = I^2_{L(RMS)} \cdot r_{DS(ON)}\big|_{BFET} = 0.67W \quad \text{(EQ. 7)}$$

The switching loss in the low-side MOSFETs is dominated by the loss in body diode, which can be calculated using Equation 8:

$$P_{diode} = I_O \cdot t_D \cdot V_F \cdot F_{SW} = 0.54W \quad \text{(EQ. 8)}$$

Where t_D is the total dead time in each switching period (~60ns) and V_F is the forward voltage drop of MOSFET's body diode.

The total power dissipation in the low-side MOSFETs is calculated using Equation 9:

$$P_{BFET(TOT)} = 1.21W \quad \text{(EQ. 9)}$$

HIGH-SIDE MOSFET SELECTION

For the high-side MOSFET selection, first we assume that the conduction loss and the switching loss contribute evenly to the total power dissipation.

The high-side MOSFET's RMS current is approximated using Equation 10:

$$I_{T(RMS)} = I_{OUT} \cdot \sqrt{D} \cdot \sqrt{1 + \frac{1}{12} \cdot \left(\frac{\Delta I_L}{I_{OUT}}\right)^2} \approx 10A \quad \text{(EQ. 10)}$$

Hence, the required ON-resistance of the high-side MOSFET is 5mΩ. Two of Infineon's BSC059N04LS are selected. The conduction loss in the high-side MOSFET is calculated using Equation 11:

$$P_{TFET(cond)} = I^2_{T(RMS)} \cdot r_{DS(ON)}\big|_{TFET} = 0.425W \quad \text{(EQ. 11)}$$

The switching loss in the high-side MOSFET can be approximated using Equation 12:

$$P_{TFET(SW)} = \frac{1}{2} \cdot I_O \cdot V_{IN} \cdot t_{tr} \cdot F_{SW} + \frac{1}{2} \cdot 2 \cdot C_{OSS} \cdot V^2_{IN} \cdot F_{SW} = 0.34W \quad \text{(EQ. 12)}$$

where t_{tr} is the combined ON and OFF MOSFET transition times.

The total power dissipation in high-side MOSFET is shown in Equation 13:

$$P_{TFET(TOT)} = 0.765W \quad \text{(EQ. 13)}$$

Overcurrent Protection Setting

The ISL8118 monitors both the top side MOSFET and bottom side MOSFET for overcurrent events. Dual sensing allows the ISL8118 to detect overcurrent faults at the very low and very high duty cycles that can result from the ISL8118's wide input range. The OCP function is enabled with the drivers at start-up.

BOTTOM SIDE OCP

A resistor(R_{BSOC}) and a capacitor(C_{BSOC}) between the BSOC pin and the source of the bottom side MOSFETs set the bottom side source and sinking current limits. A 100µA current source develops a voltage across the resistor which is then compared with the voltage developed across the bottom side MOSFET during the conduction period. A capacitor (C_{BSOC}) of 1000pF or greater should be used in parallel with R_{BSOC}.

The OCP trip point varies mainly due to MOSFET $r_{DS(ON)}$ variations and layout noise concerns. To avoid overcurrent tripping in the normal operating load range, find the R_{BSOC} resistor from Equation 14 with:

1. The maximum $r_{DS(ON)}$ at the highest junction temperature
2. The minimum I_{BSOC} from the specifications table in the datasheet

Determine the overcurrent trip point greater than the maximum output continuous current at maximum inductor ripple current.

Simple Bottom side OCP Equation

$$R_{BSOC} = \frac{I_{OC\_SOURCE} \bullet r_{DS(ON)}\big|_{BFET}}{100\mu A}$$

Detailed OCP Equation

$$R_{BSOC} = \frac{\left(I_{OC\_SOURCE} + \frac{\Delta I}{2}\right) \bullet r_{DS(ON)}\big|_{BFET}}{I_{BSOC} \bullet N_B} \quad \text{(EQ. 14)}$$

N_B = NUMBER OF BOTTOM-SIDE MOSFETs

$$\Delta I = \frac{V_{IN} - V_{OUT}}{F_{SW} \bullet L_{OUT}} \bullet \frac{V_{OUT}}{V_{IN}}$$

With two of Infineon's BSC018N04LS as the bottom-side MOSFETs and R_{BSOC} of 511Ω, the bottom-side overcurrent trip point on the evaluation board has been approximately set to 35A.

TOP SIDE OCP

A resistor (R_{TSOC}) and a capacitor (C_{TSOC}) between the TSOC pin and the drain of the top side MOSFETs set the top side sourcing current limits. A 100µA current source develops a voltage across the resistor R_{TSOC} which is then compared with the voltage developed across the top side MOSFET while on. A capacitor (C_{TSOC}) of 1000pF or greater should be used in parallel with R_{TSOC}.

Simple Bottom Side OCP Equation

$$R_{TSOC} = \frac{I_{OC\_SOURCE} \bullet r_{DS(ON)}|_{TFET}}{100\mu A}$$

Detailed OCP Equation

$$R_{TSOC} = \frac{\left(I_{OC\_SOURCE} + \frac{\Delta I}{2}\right) \bullet r_{DS(ON)}|_{TFET}}{I_{TSOC} \bullet N_T} \quad \text{(EQ. 15)}$$

N_T = NUMBER OF TOP-SIDE MOSFETs

$$\Delta I = \frac{V_{IN} - V_{OUT}}{F_{SW} \bullet L_{OUT}} \bullet \frac{V_{OUT}}{V_{IN}}$$

With two of Infineon's BSC059N04LS as the top-side MOSFETs and R_{TSOC} of 1.59kΩ, the top-side overcurrent trip point on the evaluation board has been approximately set to 35A.

Voltage Margining

When MARGIN is pulled high or low, the positive or negative margining functionality is respectively enabled. When MARGIN is left floating, the function is disabled. Upon positive margining, an internal buffer drives the OFSN pin from VCC to maintain OFSP at 0.591V. The resistor divider, R_{MARG} and R_{OFSP}, causes the voltage at OFSN to be increased. Similarly, upon negative margining, an internal buffer drives the OFSP pin from VCC to maintain OFSN at 0.591V. The resistor divider, R_{MARG} and R_{OFSN}, causes the voltage at OFSP to be increased. In both modes, the voltage difference between OFSP and OFSN is then sensed with an instrumentation amplifier and is converted to the desired margining voltage by a 5:1 ratio.

A desired percentage change in the output voltage when using the internal 0.591V reference can be calculated from Equation 16:

$$V_{M-POS} = 20 \times \frac{R_{MARG}}{R_{OFS}} = 16.95$$
$$V_{M-NEG} = 20 \times \frac{R_{MARG}}{R_{OFS}} = 16.95 \quad \text{(EQ. 16)}$$

Setting Input UVLO

The input voltage can be monitored through the enable pin. Programmable enable's hysteresis can be achieved with the internal 10µA sink current and an external resistor divider. Setting the ISL8118 to be enabled at an input voltage of 4.2V with 0.5V hysteresis, resistor divider network is expressed in Equation 17:

$$R_{up} = \frac{V_{EN\_HYS}}{I_{EN\_HYS}} = 49.9k\Omega$$
$$R_{down} = \frac{R_{UP} \bullet V_{EN\_REF}}{V_{EN\_RTH} - V_{EN\_HYS} - V_{EN\_REF}} = 7.15k\Omega \quad \text{(EQ. 17)}$$

Feedback Compensator

A Type-III network is recommended for compensating the feedback loop. Figure 1 shows Type-III compensation configuration for the ISL8118.

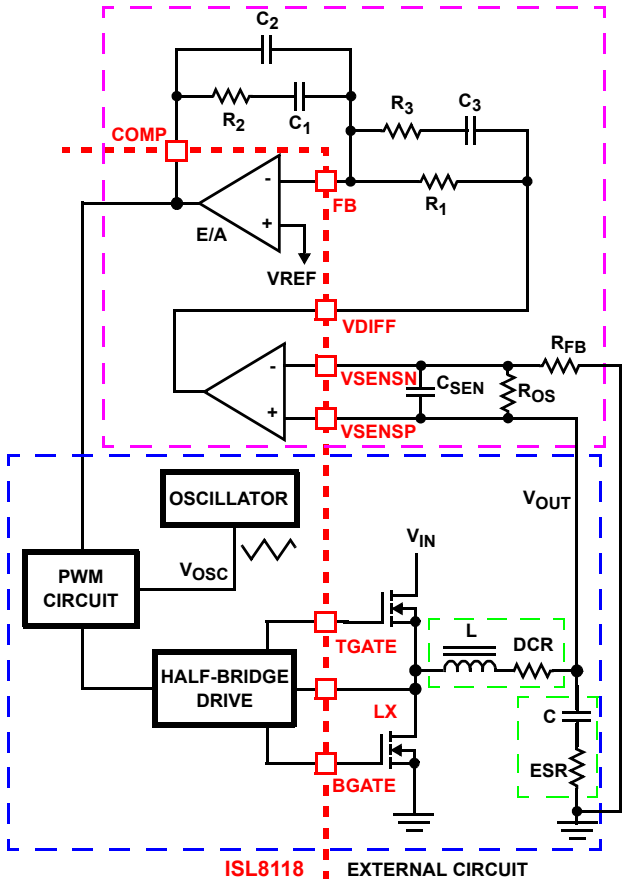


FIGURE 1. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN

With the inductor and output capacitor selected as described in the previous sections, the poles and zero of the power stage can be summarized in Equation 18:

$$F_0 = \frac{1}{2 \times \pi \times \sqrt{L \times C}} = 4.75kHz$$
$$F_{ESR} = \frac{1}{2 \times \pi \times C \times ESR} = 53.6kHz \quad \text{(EQ. 18)}$$

1. With a value of 1.07kΩ for R_{FB}, select R_{OS} for the target output voltage of 1.8V using Equation 19:

$$R_{OS} = R_{FB} \times \frac{V_{REF}}{V_{OUT} - V_{REF}} \quad \text{(EQ. 19)}$$
$$= 523\Omega$$

2. With the desired feedback loop bandwidth at approximately 50kHz, R_2 can be calculated using Equation 20, setting R_1 to 2kΩ:

$$R_2 = \frac{V_{OSC} \cdot R_1 \cdot F_{BW}}{d_{max} \cdot V_{IN} \cdot F_0} \bullet \frac{(R_{OS} + R_{FB})}{R_{OS}} = 10k\Omega \quad \text{(EQ. 20)}$$

3. Select C_1 such that F_{Z1} is located at 3.5kHz:

$$C_1 = \frac{1}{2\pi \cdot R_2 \cdot 3.5 \times 10^3} \approx 4.7nF \quad \text{(EQ. 21)}$$

4. Select C_2 such that F_{P1} is located at F_{ESR}:

$$C_2 = \frac{C_1}{2\pi \cdot R_2 \cdot C_1 \cdot F_{ESR} - 1} \approx 270pF \quad \text{(EQ. 22)}$$

5. Select R_3 such that F_{Z2} is located at F_{LC} and F_{P2} is located at 150kHz:

$$R_3 = \frac{R_1}{\frac{150 \times 10^3}{F_0} - 1} \approx 64.9\Omega$$

$$C_3 = \frac{1}{2\pi \cdot R_3 \cdot 150 \times 10^3} \approx 15nF \quad \text{(EQ. 23)}$$

A more detailed explanation of designing compensation networks for buck converters with voltage mode control can be found in TB417 entitled “Designing Stable Compensation Networks for Single Phase Voltage Mode Buck Regulators”.

Evaluation Board Performance

Figure 2 shows a photograph of the ISL8118EVAL1Z.

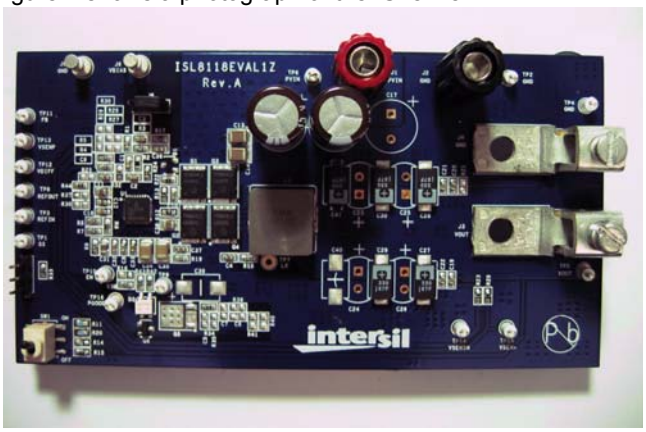


FIGURE 2. ISL8118EVAL1Z

Power and Load Connections

Terminals J1 and J2 are connected to the input of the power stage. For single rail supply, the IC bias supply can be tied to the converter input supply through pin 1 and 2 of the Jumper J8. When using separate supplies, provide the IC bias voltage to terminal J6 with pins 2 and pin 3 of J8 connected together. The load can be connected to terminal J3 and J4. TP4 and TP5 can be used for DMM to measure output voltage. The toggle switch, SW1, can be used to enable/disable the controller.

Start-up

When the voltages at V_{CC}, P_{VCC}, V_{FF} and EN of ISL8118 exceed their rising POR thresholds, a 38A current source driving the SS pin is enabled. Figure 3 shows the start-up profile of the ISL8118 in relation to the start-up of the 12V input supply and the bias supply..

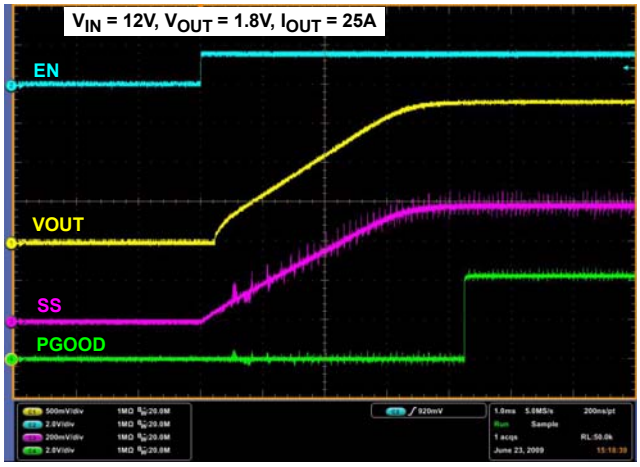


FIGURE 3. SOFT-START

Soft-Start with Pre-Biased Output

If the output is pre-biased to a voltage less than the expected value, the ISL8118 will detect that condition. Drivers are held in tri-state (TGATE pulled to LX, BGATE pulled to PGND) at the beginning of a soft-start cycle until the COMP signal exceeds the bottom of the oscillator ramp. The bottom-side MOSFET is turned on first for 200ns to charge the bootstrap capacitor. This method of driver activation provides support for start-up into prebiased loads by not activating the drivers until the control loop has entered its linear region, thereby substantially reducing output transients that would otherwise occur had the drivers been activated at the beginning of the soft-start cycle.

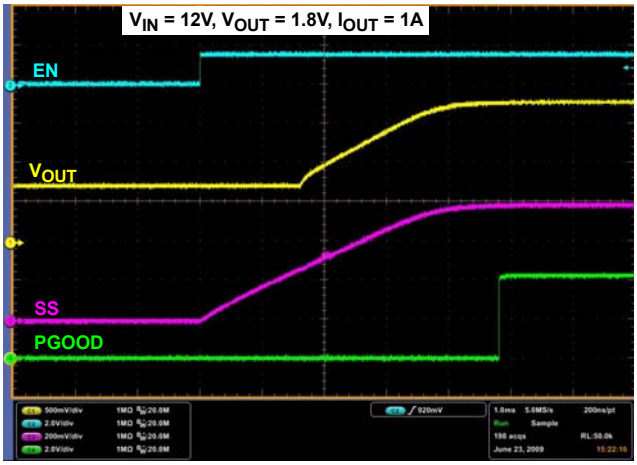


FIGURE 4. SOFT-START WITH PRE-BIASED OUTPUT

Output Ripple

Figure 5 shows the ripple voltage on the output of the regulator.

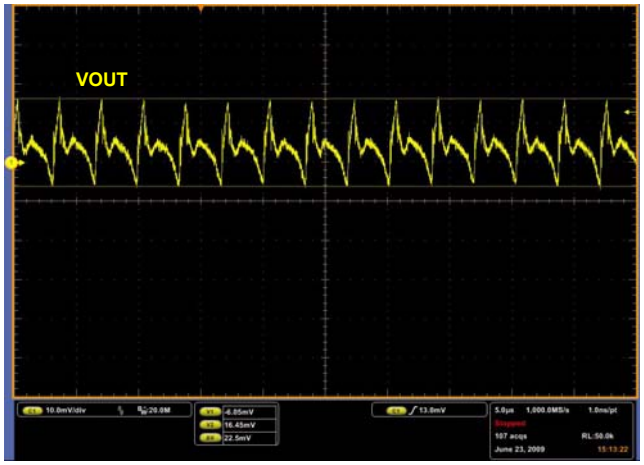


FIGURE 5. OUTPUT RIPPLE (20MHz BW)

Transient Performance

Figures 6, 7 and 8 show the response of the output voltage when subjected to transient loading from 0A to 25A at 1A/µs.

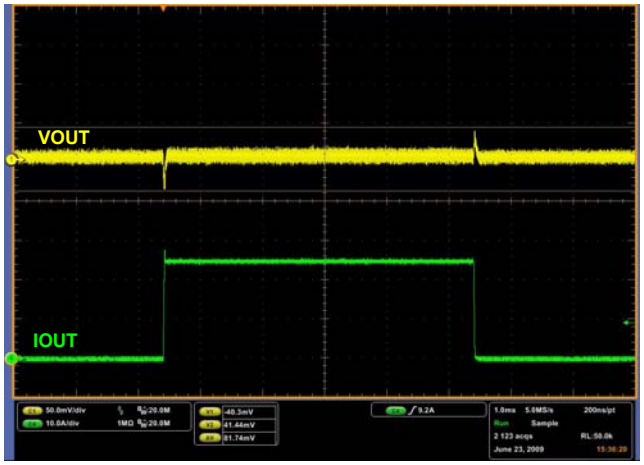


FIGURE 6. TRANSIENT RESPONSE

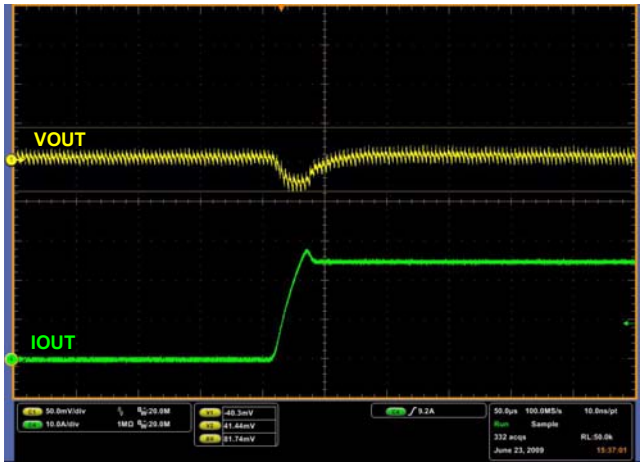


FIGURE 7. TRANSIENT RESPONSE

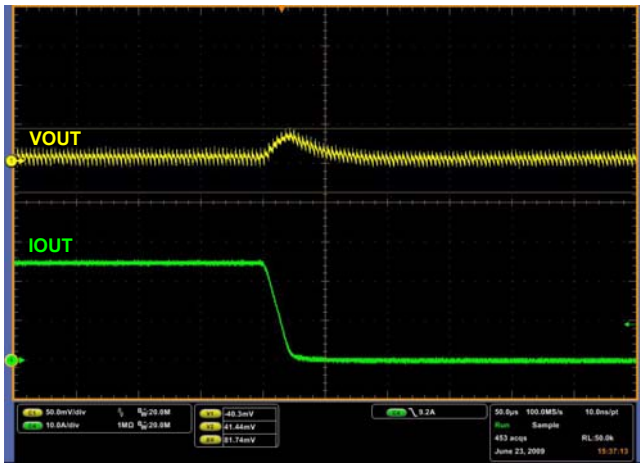


FIGURE 8. TRANSIENT RESPONSE

Efficiency

ISL8118 based regulators enable the design of highly efficient systems. The efficiency of the evaluation board using a 12V input supply is shown in Figure 9.

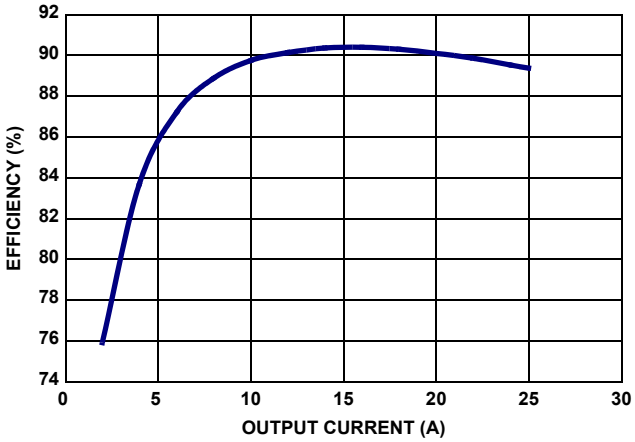


FIGURE 9. EVALUATION BOARD EFFICIENCY (V_{OUT} = 1.8V)

Voltage Margining

By pulling MARGIN high or low, the positive or negative margining funtionality is respectively enabled. Waveforms are included in Figures 10 and 11.

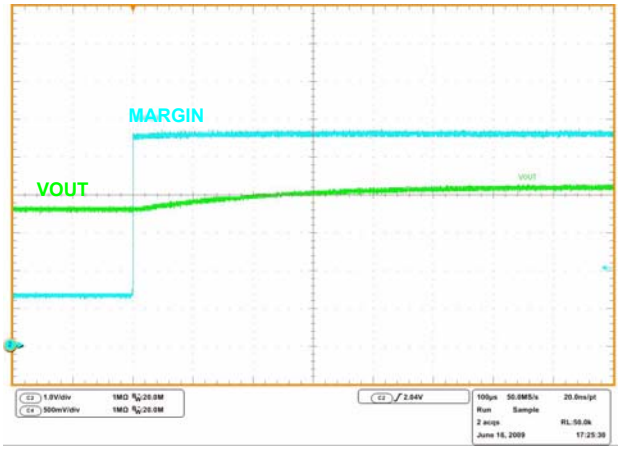


FIGURE 10. MARGINING UP

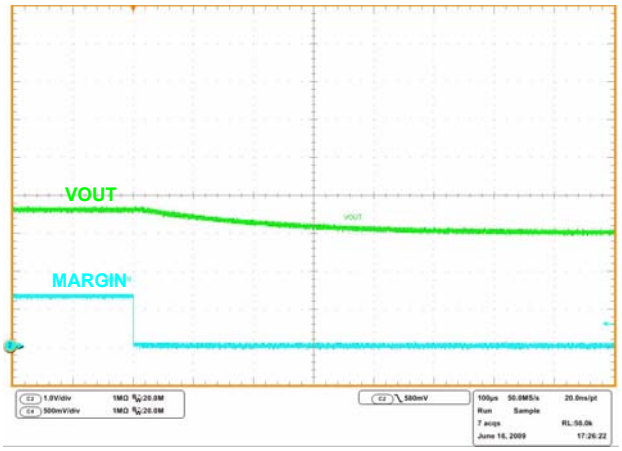


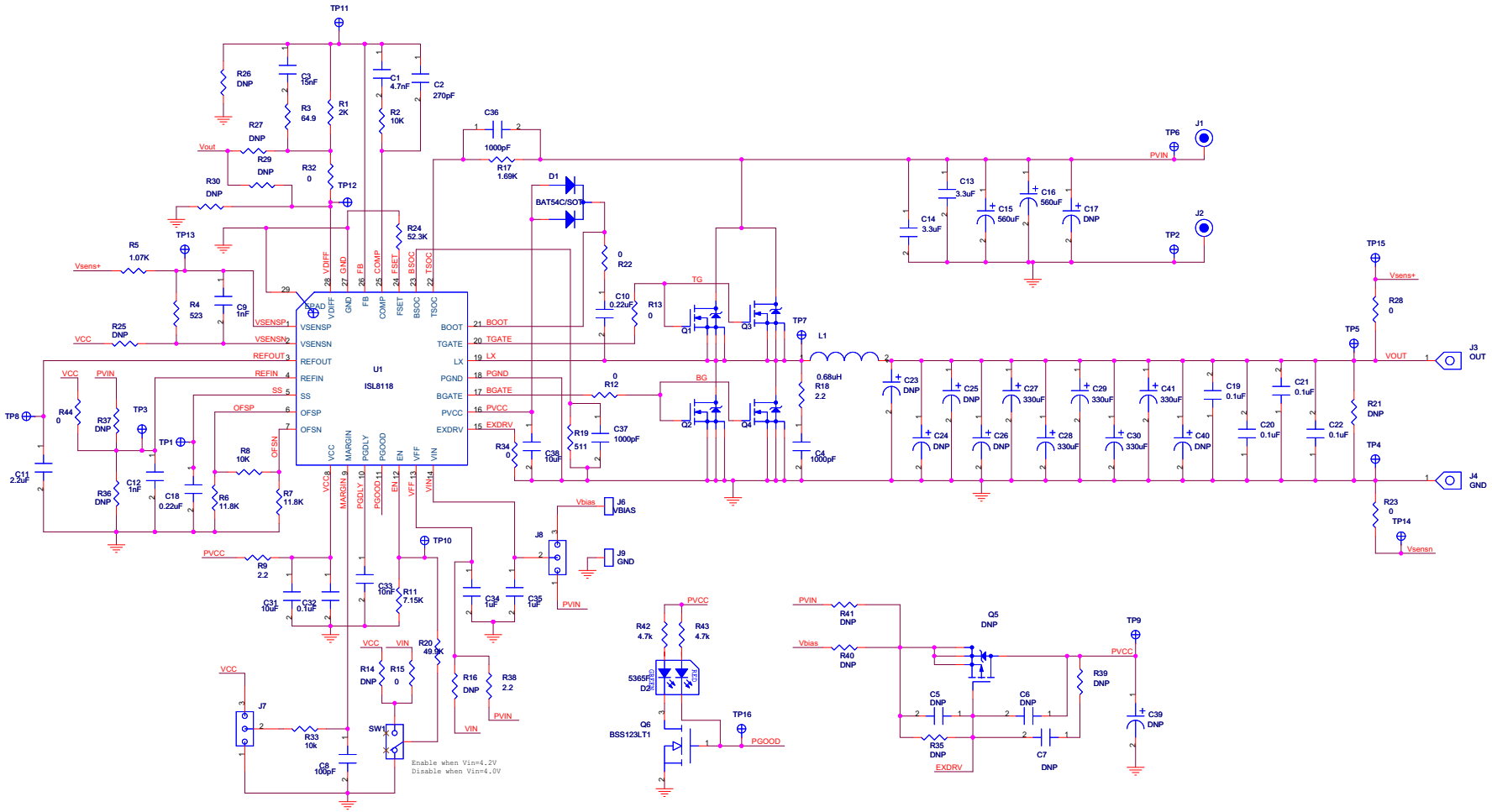
FIGURE 11. MARGINING DOWN

References

For Intersil documents available on the web, go to http://www.intersil.com/.

1. ISL8118 Data Sheet “3.3V to 20V, Single-Phase PWM Controller with Integrated 2A/4A MOSFET Drivers”, Intersil Corporation
2. Tech Brief TB417 , “Designing Stable Compensation Networks for Single Phase Voltage Mode Buck Regulators”, Intersil Corporation

ISL8118EVAL1Z Schematic



ISL8118EVAL1Z Bill of Materials

ID	REFERENCE	QTY	PART NUMBER	PART TYPE	DESCRIPTION	PACKAGE	VENDOR
1	U1	1	ISL8118IRZ	IC, Linear	IC, Single PWM Controller	28 Ld 5x5 MLFP	Intersil
2	Q1, Q3	2	BSC059N04LS G	MOSFET	40V N-Channel MOSFET	TDSON-08	Infineon
3	Q2, Q4	2	BSC018N04LS G	MOSFET	40V N-Channel MOSFET	TDSON-08	Infineon
4	D1	1	BAT54C	Schottky Diode	30V, 200mA Schottky diode	SOT23	Onsemi
5	L1	1	IHLP5050FD-R68	Inductor	0.68µH, high current inductor	SMD	Vishay
6	SW1	1	GT11MSCKE	Toggle Switch	Switch toggle, SMD, Ultramini, 1P, SPST Mini		C&K
7	D2	1	SSL-LXA3025IGCF	LED	Dual LED RED/GREEN	SMD 3x2.5mm	LUMEX
8	Q6	1	BSS123LT1G	MOSFET	100V 0.17A N-Channel MOSFET	SOT23	On Semi
9	Q5	DNP					
CAPACITORS							
10	C1	1		Capacitor, Ceramic, X7R	4.7nF, 50V, 10%, ROHS	SM_0603	Generic
11	C2	1		Capacitor, Ceramic, X7R	270pF, 50V, 10%, ROHS	SM_0603	Generic
12	C3	1		Capacitor, Ceramic, X7R	15nF, 50V, 10%, ROHS	SM_0603	Generic
13	C4, C9, C12, C36, C37	5		Capacitor, Ceramic, X5R	1000pF, 50V, 10%, ROHS	SM_0603	Generic
14	C8	1		Capacitor, Ceramic, COG	100pF, 50V, 10%, ROHS	SM_0603	Generic
15	C10	1		Capacitor, Ceramic, X7R	0.22µF, 25V, 10%, ROHS	SM_0603	Generic
16	C11			Capacitor, Ceramic, X5R	2.2µF, 16V, 10%, ROHS	SM_0805	Generic
17	C13, C14	1	C3225X7R1H335K	Capacitor, Ceramic, X7R	3.3µF, 50V, 10%, ROHS	SM_12105	TDK
18	C15, C16	2	EKZE350ELL561MJ25S	Aluminum Capacitor	560µF, 35V	RAD 10x25	United CHEMI-CON
19	C18	1		Capacitor, Ceramic, X7R	0.22µF, 50V, 10%, ROHS	SM_0603	Generic
20	C19-C22, C32	5	C1608X7R1H104K	Capacitor, Ceramic, X7R	0.1µF, 50V, 10%, ROHS	SM_0603	Generic
21	C27-C30, C41	5	6TPF330M9L	POSCAP	330µF, 6.3V, 20%, ROHS	SMD D3L	Sanyo
22	C31, C38	2		Capacitor, Ceramic, X5R	10µF, 16V, 10%, ROHS	SM_0805	Generic
23	C33			Capacitor, Ceramic, X7R	0.01µF, 50V, 10%, ROHS	SM_0603	Generic
24	C34, C35	2		Capacitor, Ceramic, X7R	1.0µF, 50V, 10%, ROHS	SM_12105	Generic
25	C5, C6, C7, C17, C23, C24, C25, C26, C39, C40	DNP					
RESISTORS							
26	R1	1		Resistor, Film	2kΩ, 1%, 1/10W	SM_0603	Generic
27	R2	1		Resistor, Film	10kΩ, 1%, 1/10W	SM_0603	Generic
28	R3	1		Resistor, Film	64.9Ω, 1%, 1/10W	SM_0603	Generic
29	R4	1		Resistor, Film	523Ω, 1%, 1/10W	SM_0603	Generic
30	R5	1		Resistor, Film	1.07kΩ, 1%, 1/10W	SM_0603	Generic
31	R6, R7	2		Resistor, Film	11.8kΩ, 1%, 1/10W	SM_0603	Generic
32	R8, R33	2		Resistor, Film	10kΩ, 1%, 1/10W	SM_0603	Generic
33	R9, R18, R38	3		Resistor, Film	2.2Ω, 1%, 1/10W	SM_0603	Generic
34	R11	1		Resistor, Film	7.15kΩ, 1%, 1/10W	SM_0603	Generic

ISL8118EVAL1Z Bill of Materials (Continued)

ID	REFERENCE	QTY	PART NUMBER	PART TYPE	DESCRIPTION	PACKAGE	VENDOR
35	R12, R13, R15, R22, R23, R28, R32, R34, R44	9		Resistor, Film	0Ω, 1/10W	SM_0603	Generic
36	R17	1		Resistor, Film	1.69kΩ, 1%, 1/10W	SM_0603	Generic
37	R19	1		Resistor, Film	511Ω, 1%, 1/10W	SM_0603	Generic
38	R20	1		Resistor, Film	49.9kΩ, 1%, 1/10W	SM_0603	Generic
39	R24	1		Resistor, Film	52.3kΩ, 1%, 1/10W	SM_0603	Generic
40	R42, R43	2		Resistor, Film	4.7kΩ, 1%, 1/10W	SM_0603	Generic
41	R14, R16, R21, R25, R26, R27, R29, R30, R35, R36, R37, R39, R40, R41	DNP				SM_0603	
OTHERS							
42	J1	1	111-0702-001	Blinding Post	Conn-Gen, Bind. Post, RED, Thmbnut-Gnd		Johnson Components
43	J2,	1	111-0703-001	Blinding Post	Conn-Gen, Bind. Post, Black, Thmbnut-Gnd		Johnson Components
44	J3, J4	2	KPA8CTP	Cable Terminal	14AWG Cable Terminal		BERG/FCI
45	J6, J9	2	1514-2	Turrett Post	Conn-Turret, Terminal Post, TH, ROHS		Keystone
46	J7, J8	2	68000-236HLF		3-pin Jumper		BERG/FCI
47	J5	1	68000-236-1x3		3-pin Jumper		Berg/FCI
48	TP1-TP6, TP8-TP16	15	5002	Test Point	Conn-Mini Test Point, Vertical, White, ROHS		Keystone
49	TP7	DNP					

ISL8118EVAL1Z Printed Circuit Board Layers

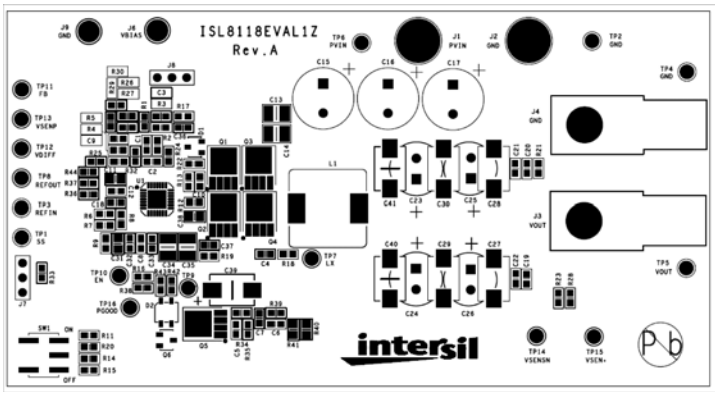


FIGURE 12. TOP SILK SCREEN

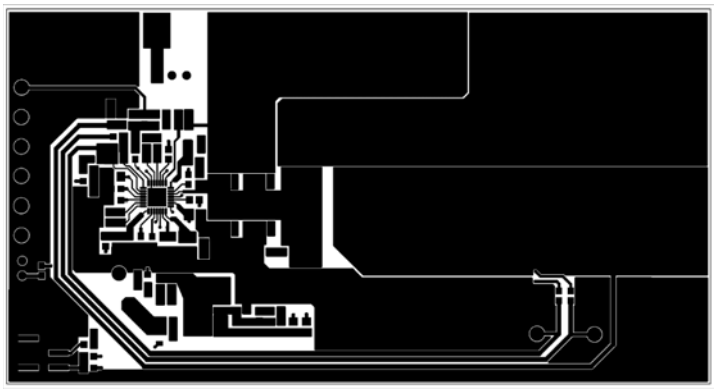


FIGURE 13. TOP LAYER

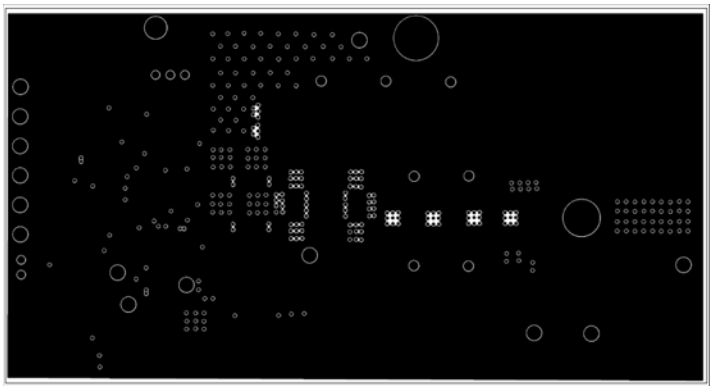


FIGURE 14. LAYER 2

ISL8118EVAL1Z Printed Circuit Board Layers (Continued)

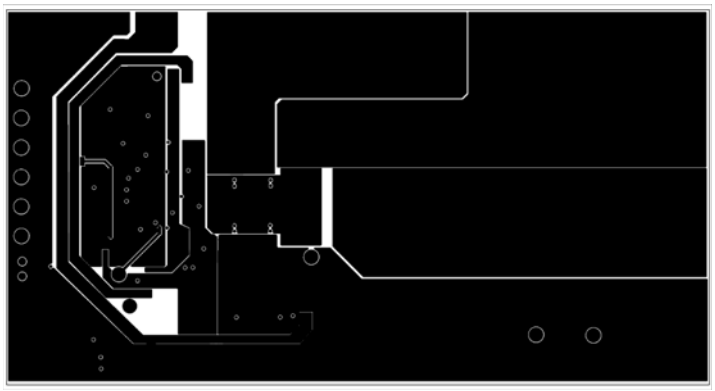


FIGURE 15. LAYER 3

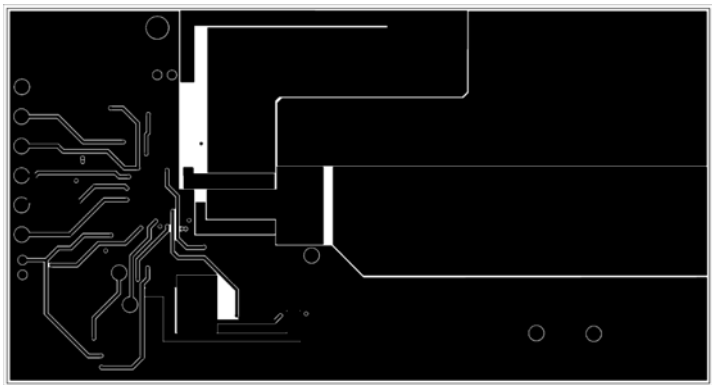


FIGURE 16. BOTTOM LAYER

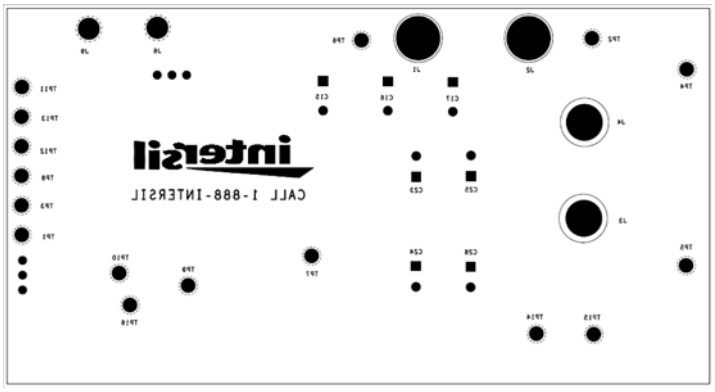


FIGURE 17. BOTTOM SILKSCREEN