

ISL8120EVAL3Z

Evaluation Board Setup Procedure

AN1528
Rev.2.00
July 1, 2016

Description

The [ISL8120](#) integrates two voltage mode synchronous buck PWM controllers. It can be used either for dual independent outputs or a 2-phase single output regulator.

The ISL8120EVAL3Z evaluation board is for performance demo of the dual independent outputs and DDR applications.

The ISL8120EVAL4Z evaluation board is used for performance demo of 2/n-phase single-output applications. Refer to application note [AN1607](#) "ISL8120EVAL4Z Evaluation Board Setup Procedure" for details of the ISL8120EVAL4Z board.

Preset Specifications

| VIN (V) | FREQUENCY (kHz) | VOUT1 | VOUT2 |
|---------|-----------------|----------|----------|
| 12 | 500 | 1.2V/25A | 1.2V/25A |

Recommended Equipment

- 0V to 22V power supply with at least 20A source current capability, battery, or notebook AC adapter.
- Two electronic loads capable of sinking current up to 30A
- Digital Multimeters (DMMs).
- 100MHz quad-trace oscilloscope.

References

- [ISL8120](#) Datasheet
- [AN1607](#), "ISL8120EVAL4Z Evaluation Board Setup Procedure"

Ordering Information

| PART NUMBER | DESCRIPTION |
|---------------|---|
| ISL8120EVAL3Z | ISL8120 evaluation board for performance evaluation |

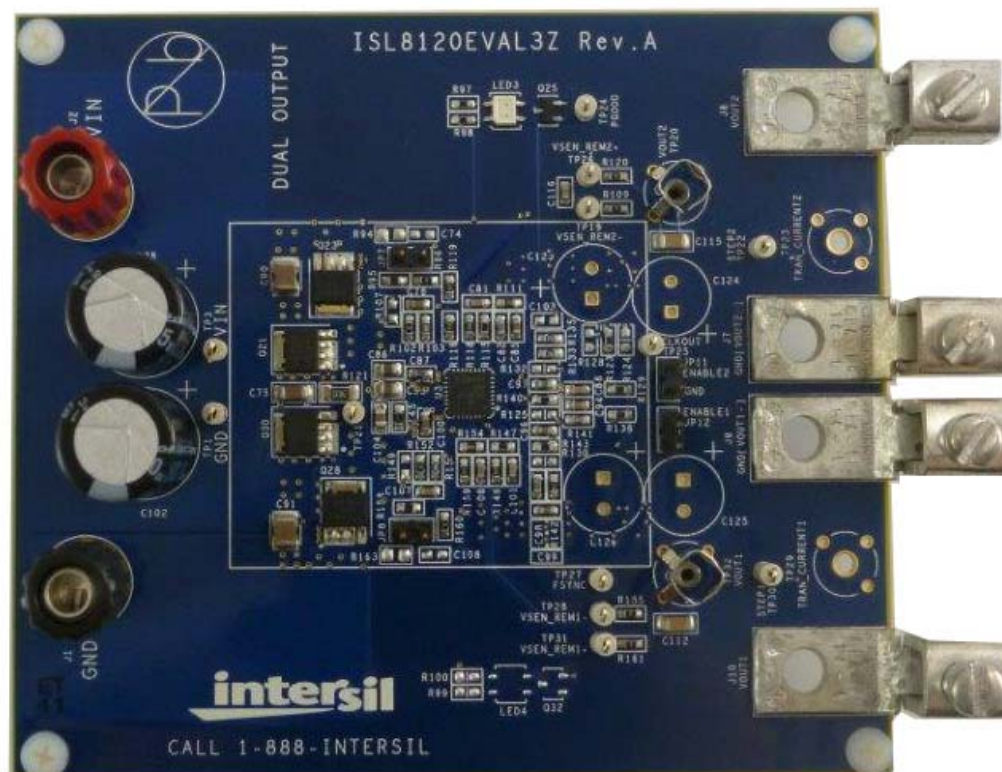


FIGURE 1. ISL8120EVAL3Z EVALUATION BOARD

Circuits Description

J1 and J2 are the input power terminals.

Two input electrolytic capacitors are used to handle the input current ripples.

Two upper and two lower Renesas “speed” series LFPK MOSFETs are used for each channel. Q₁ and Q₂ are footprint options for low current applications where a SO8 package integrating dual MOSFET can be used.

320nH PULSE surface mount inductors are used for each channel. Under the 500kHz setup, the inductor current peak-to-peak ripple is 7.5A at 12V input.

Two SANYO POSCAP 2R5TPF470M7L (7mΩ) are used as output E-caps for each channel. Also, through-hole electrolytic capacitor footprints C₁₂₃ ~ C₁₂₆ are available for the user to evaluate different output capacitors.

J7, J8, J9 and J10 are output lugs for load connections.

TP19, TP26, TP28 and TP31 are remote sense posts. These pins can be used to monitor and evaluate the system voltage regulations. If the user wants to use these test posts for remote sense, the R₁₀₉, R₁₂₀, R₁₅₅ and R₁₆₁ need to be changed to higher values, such as 10Ω. Also, the related voltage sense divider needs to be increased to a higher resistance, such as 1k.

Q₂₆, Q₂₇, R₁₂₆, R₁₅₆, R₁₂₂, R₁₃₁, R₁₅₁ and R₁₅₃ are circuit footprint options to add an on-board transient load to the regulator. Use a signal generator to apply a clock signal at TP22 (TP30) to generate step-up and step-down transient load. Make sure that the duty cycle of the clock is small enough to avoid burning load resistors R₁₂₆ and R₁₅₆.

JP11 or JP12 are the jumpers used to disable the channels independently.

TP27 is a post that can be used to inject a clock signal for the controller to be synchronized with.

JP7 and JP8 are jumpers for r_{DS(ON)} sensing configuring. Also, these jumpers can be used to monitor the DCR sensing capacitor voltage.

R₉₄, C₇₄, R₁₆₃ and C₁₀₈ are optional footprints for snubbers, which are used to filter the ringing at phase nodes.

R₉₉, R₁₀₀, R₁₂₅, R₁₃₀, R₁₃₂, LED4 and Q₃₂ are useless footprints.

R₁₂₁ and C₈₆ are small added filters for the VIN pin. R₁₄₅ is used to isolate the noise at PVCC caused by driving. In 3.3V applications, R₁₂₁ and R₁₄₅ are recommended to short to 0 to prevent VCC from going below POR under low input voltage. Also, it is recommended to add a 2k resistor from LGATE to GND to discharge the low gate at the state of LGATE OFF.

Quick Start

1. Ensure that the circuit is correctly connected to the supply and loads prior to applying any power.
2. Adjust the input supply to be 12V. Turn on the input power supply.

3. Verify that the two output voltages are correct. If the PGOOD is set high, the LED3 will be green. If the PGOOD is set low, the LED3 will be red. TP24 is the test post to monitor PGOOD.

Evaluating the Other Output Voltage

The ISL8120EVAL3Z kit outputs are preset to 1.2V/25A, V_{OUT1} can also be adjusted between 0.6V to 3V by changing the value of R₁₁₉ and R₁₁₆ for V_{OUT1} as given by [Equation 1](#). The same rule applies for V_{OUT2}.

$$R_{116} = \frac{R_{119}}{(V_{OUT1}/V_{REF}) - 1} \quad \text{Where } V_{REF} = 0.6V \quad (\text{EQ. 1})$$

r_{DS(ON)} Sense Configuration

If the desired output voltage is higher than 3V, the current sense has to be configured as r_{DS(ON)} sensing because of the common-mode voltage limitation of the current sense differential amplifier. The default setup of ISL8120EVAL3Z is DCR sensing. The following steps show how to change to r_{DS(ON)} sensing for Channel 2:

1. Remove R₁₀₂ and R₉₆ to be open.
2. Change R₁₀₇ and R₉₅ to be 0Ω.
3. Short jumper JP7.

Programming the Input Voltage UVLO and its Hysteresis

By programming the voltage divider at the EN/FF pin connected to the input rail, the input UVLO and its hysteresis can be programmed. The ISL8120EVAL3Z has R₁₂₉ (R₁₃₆) 13.7k and R₁₃₅ (R₁₄₁) 4.42k; the IC will be disabled when input voltage drops below 3.38V and will restart until V_{IN} recovers to be above 4.42V.

For 12V applications, it is suggested to have R₁₂₉ (R₁₃₆) 33k and R₁₃₅ (R₁₄₁) 5.1k, of which the IC is disabled when the input voltage drops below 6V and will restart until V_{IN} recovers to be above 7V.

Refer to the [ISL8120](#) datasheet to program the UVLO falling threshold and hysteresis. The equations are restated in [Equations 2](#) and [3](#), where R_{UP} and R_{DOWN} are the upper and lower resistors of the voltage divider at EN/FF pin. V_{HYS} is the desired UVLO hysteresis and V_{FTH} is the desired UVLO falling threshold.

$$R_{UP} = \frac{V_{HYS}}{I_{HYS}} \quad \text{Where } I_{HYS} = 30\mu A \quad (\text{EQ. 2})$$

$$R_{DOWN} = \frac{R_{UP} \cdot V_{EN_REF}}{V_{FTH} - V_{EN_REF}} \quad \text{Where } V_{EN_REF} = 0.8V \quad (\text{EQ. 3})$$

Note that the ISL8120 EN/FF pin is a triple function pin and the voltages applied to the EN/FF pins are also fed to adjust the amplitude of each channel's individual sawtooth.

DDR Application

The ISL8120 can be used as a DDR controller. The Typical Application II schematic in the [ISL8120](#) datasheet shows its configuration. Channel 1 is used for VDDQ. VDDQ output is fed to the REFIN pin of Channel 2, thus Channel 2 can track VDDQ at start-up and supplies as VTT.

Please note the configuration of EN/FF pins for start-up timing. The VDDQ channel (Channel 1) start-up should be delayed to VTT (Channel 2) by adding more filtering at EN/FF1 than EN/FF2. This is to start up the internal SS ramp of Channel 2 and make it invalid because EN/FF2 is still 0 coming from VDDQ (Channel 1).

[Figure 2](#) shows the reference configurations and parameters of the EN/FF pins. RA is a resistor externally added as a filter resistor for EN/FF1.

With the configuration of [Figure 2](#), VDDQ is 1.8V and VTT is 0.9V. The gain of the resistor divider from VDDQ (Channel 1) to REFIN pin should have the same value with the resistor divider of VTT (Channel 2). RB is an externally added resistor for the upper resistor of the divider from VDDQ output to REFIN.

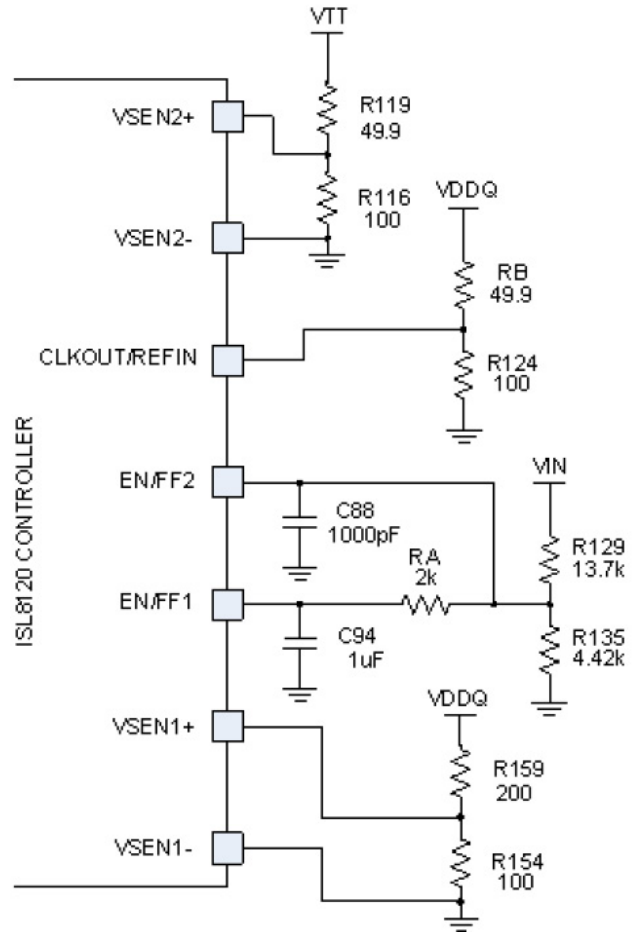


FIGURE 2. DDR CONFIGURATION

ISL8120EVAL3Z Schematic

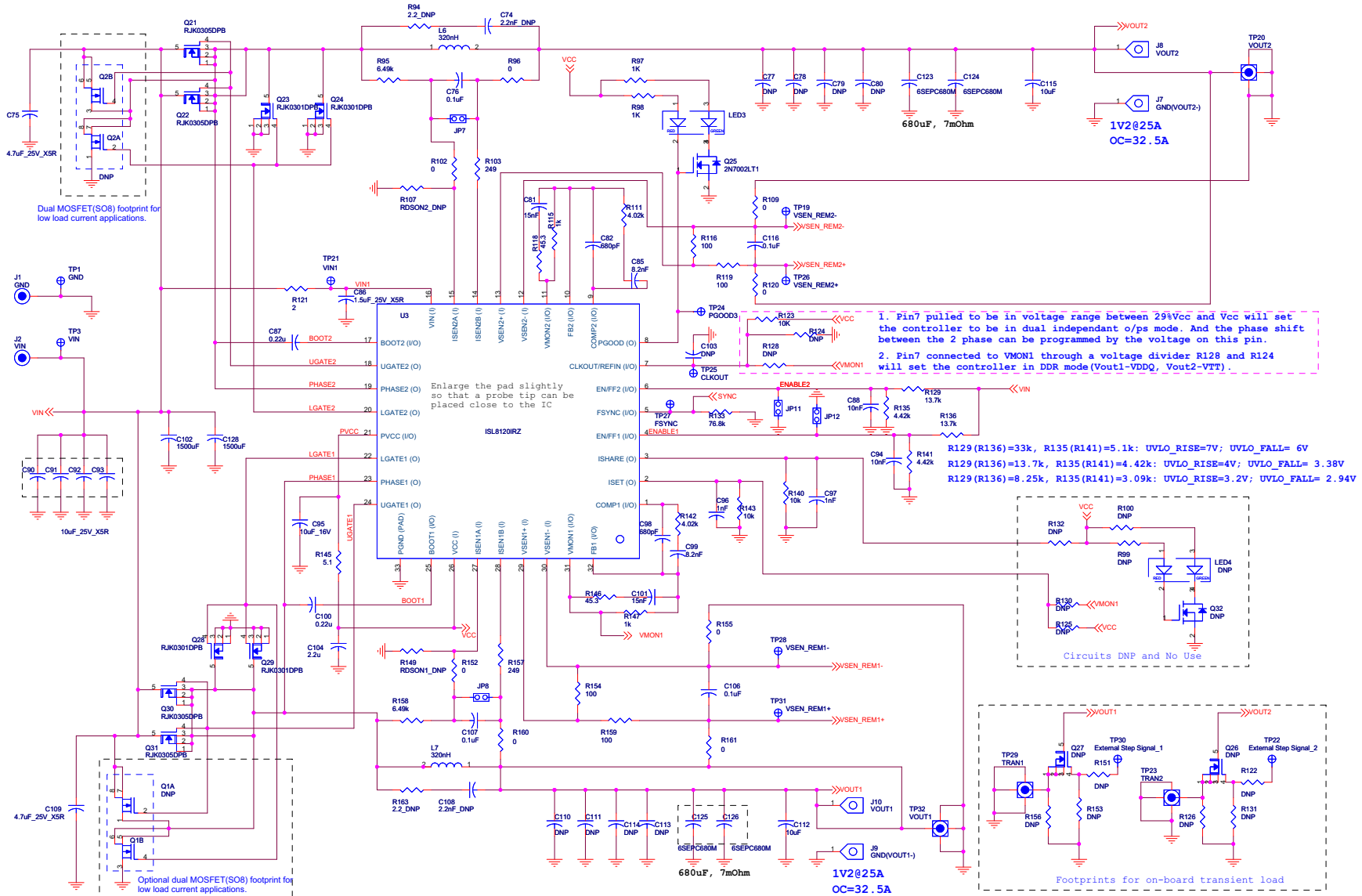


FIGURE 3. ISL8120EVAL3Z SCHEMATIC

ISL8120EVAL3Z Bill of Materials

| REFERENCE DESCRIPTION | PART NUMBER | QTY | MANUFACTURER | DESCRIPTION |
|--|--------------------|-----|--------------------|---|
| C123-C126 | DNP | 0 | | |
| C96, C97 | GRM188R71H102KA | 2 | MURATA | CAP, SMD, 0603, 1000pF, 50V, 10%, X7R, ROHS |
| C88, C94 | 06032R103K8B20 | 2 | PHILLIPS | CAP, SMD, 0603, 0.01μF, 25V, 10%, X7R, ROHS |
| C76, C106, C107, C116 | GRM39X7R104K025AD | 4 | MURATA | CAP, SMD, 0603, 0.1μF, 25V, 10%, X7R, ROHS |
| C81, C101 | ECJ-1VB1H153K | 2 | PANASONIC | CAP, SMD, 0603, 0.015μF, 50V, 10%, X7R, ROHS |
| C87, C100 | C1608X7R1E224K | 2 | TDK | CAP, SMD, 0603, 0.22μF, 25V, 10%, X7R, ROHS |
| C82, C98 | GMC10CG681J50NT | 2 | CAL-CHIP | CAP, SMD, 0603, 680pF, 50V, 5%, NPO, ROHS |
| C85, C99 | ECJ-1VB1H822K | 2 | PANASONIC | CAP, SMD, 0603, 8200pF, 50V, 10%, X7R, ROHS |
| C74, C103, C108 | DNP | 0 | | CAP, SMD, 0603, DNP-PLACE HOLDER, ROHS |
| C95 | C0805X5R160-106KNE | 1 | VENKEL | CAP, SMD, 0805, 10μF, 16V, 10%, X5R, ROHS |
| C86 | GRM21BF51E155ZA01L | 1 | MURATA | CAP, SMD, 0805, 1.5μF, 25V,+80-20,Y5V, ROHS |
| C104 | ECJ-2FB1E225K | 1 | PANASONIC | CAP, SMD, 0805, 2.2μF, 25V, 10%, X5R, ROHS |
| C112, C115 | C1206X5R250-106KNE | 2 | VENKEL | CAP, SMD, 1206, 10μF, 25V, 10%, X5R, ROHS |
| C75, C109 | C1206C475K3PACTU | 2 | KEMET | CAP, SMD, 1206, 4.7μF, 25V, 10%, X5R, ROHS |
| C79, C80, C113, C114 | DNP | 0 | | CAP, SMD, 1206, DNP-PLACE HOLDER, ROHS |
| C90, C91, C92, C93 | ECJ-4YB1E106M | 4 | PANASONIC | CAP, SMD, 1210, 10μF, 25V, 20%, X5R, ROHS |
| C102, C128 | 25ZL1500M12.5X25 | 2 | RUBYCON | CAP, RADIAL, 12.5X25, 1500μF, 25V, 20%, ALUM.ELEC., ROHS |
| C77, C78, C110, C111 | 2R5TPF470M7L | 4 | SANYO | CAP, POSCAP, SMD, 7.3X4.3, 470μF, 2.5V, 20%, 7mΩ, ROHS |
| L6, L7 | PA1513.321NLT | 2 | PULSE | COIL-PWR INDUCTOR, SMD, 13mm, 320nH, 20%, 45A, Pb-free |
| J2 | 111-0702-001 | 1 | JOHNSON COMPONENTS | CONN-GEN, BIND.POST, INSUL-RED, THMBNUT-GND |
| J1 | 111-0703-001 | 1 | JOHNSON COMPONENTS | CONN-GEN,BIND.POST, INSUL-BLK, THMBNUT-GND |
| TP20, TP32 | 131-4353-00 | 2 | TEKTRONIX | CONN-SCOPE PROBE TEST PT, COMPACT, PCB MNT, ROHS |
| TP1, TP3, TP19, TP21, TP22, TP24, TP25, TP26, TP27, TP28, TP30, TP31 | 5002 | 12 | KEYSTONE | CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS |
| JP7, JP8, JP11, JP12 | 69190-202 | 4 | BERG/FCI | CONN-HEADER, 1x2, RETENTIVE, 2.54mm, ST, ROHS |
| LED4 | DNP | 0 | | |
| LED3 | SSL-LXA3025IGC-TR | 1 | LUMEX | LED, SMD, 3mmx2.5mm, 4P, RED/GREEN, 12/20MCD, 2V |
| U3 | ISL8120IRZ | 1 | INTERSIL | IC-DUAL PHASE PWM CONTROLLER, 32P, QFN, 5x5, ROHS |
| Q25 | 2N7002-7-F | 1 | DIODES, INC. | TRANSISTOR, N-CHANNEL, 3LD, SOT-23, 60V, 115mA, ROHS |
| Q1, Q2 | DNP | 0 | | DNP-PLACE HOLDER, TRANSIST-DUAL MOS, N-CHAN, 8P, SOIC, 30V, 6A, ROHS |
| Q26, Q27 | DNP | 0 | | DNP-PLACE HOLDER, TRANSIST-MOSFET, N-CHAN, 5P, LFFPAK, 30V, 9.4mΩ, ROHS |
| Q32 | DNP | 0 | | DNP-PLACE HOLDER |

ISL8120EVAL3Z Bill of Materials (Continued)

| REFERENCE DESCRIPTION | PART NUMBER | QTY | MANUFACTURER | DESCRIPTION |
|---|-------------------|-----|--------------------|---|
| Q23, Q24, Q28, Q29 | RJK0301DPB | 4 | RENESAS TECHNOLOGY | TRANSISTOR, N-CHANNEL, 5P, LFPAK, 30V, 60A, ROHS |
| Q21, Q22, Q30, Q31 | RJK0305DPB | 4 | RENESAS TECHNOLOGY | TRANSISTOR, N-CHANNEL, 5P, LFPAK, 30V, 30A, ROHS |
| R145 | CRCW06035R10FNEA | 1 | VISHAY/DALE | RES, SMD, 0603, 5.1Ω, 1/10W, 1%, TF, ROHS |
| R96, R102, R109, R120, R152, R155, R160, R161 | | 8 | Various | RESISTOR, SMD, 0603, 0Ω, 1/10W, TF, ROHS |
| R116, R119, R154, R159 | RK73H1JT1000F | 4 | KOA | RES, SMD, 0603, 100Ω, 1/10W, 1%, TF, ROHS |
| R97, R98, R115, R147 | RK73H1JTTD1001F | 4 | KOA | RES, SMD, 0603, 1k, 1/10W, 1%, TF, ROHS |
| R123, R140, R143 | RK73H1JT1002F | 3 | KOA | RES, SMD, 0603, 10k, 1/10W, 1%, TF, ROHS |
| R129, R136 | RC0603FR-0713K7L | 2 | YAGEO | RESISTOR, SMD, 0603, 13.7k, 1/10W, 1%, TF, ROHS |
| R103, R157 | CR0603-10W-2490FT | 2 | VENKEL | RES, SMD, 0603, 249Ω, 1/10W, 1%, TF, ROHS |
| R111, R142 | ERJ-3EKF4021V | 2 | PANASONIC | RES, SMD, 0603, 4.02kΩ, 1/10W, 1%, TF, ROHS |
| R135, R141 | RC0603FR-074K42L | 2 | YAGEO | RES, SMD, 0603, 4.42k, 1/10W, 1%, TF, ROHS |
| R118, R146 | CR0603-10W-45R3FT | 2 | VENKEL | RES, SMD, 0603, 45.3Ω, 1/10W, 1%, TF, ROHS |
| R95, R158 | ERJ-3EKF6491V | 2 | PANASONIC | RES, SMD, 0603, 6.49k, 1/10W, 1%, TF, ROHS |
| R133 | CR0603-10W-7682FT | 1 | VENKEL | RES, SMD, 0603, 76.8k, 1/10W, 1%, TF, ROHS |
| R99, R100, R107, R122, R124, R125, R128, R130 to R132, R149, R151, R153 | DNP | 0 | | RES, SMD, 0603, DNP-PLACE HOLDER, ROHS |
| R94, R163 | DNP | 0 | | RES, SMD, 0805, DNP-PLACE HOLDER, ROHS |
| R121 | CR1206-4W-02R0 | 1 | VENKEL | RES, SMD, 1206, 2Ω, 1/4W, 1%, TF, ROHS |
| R126, R156 | DNP | 0 | | RES, SMD, 2512, PLACE HOLDER, TF, ROHS |
| J7, J8, J9, J10 | KPA8CTP | 4 | BERG/FCI | HDWARE, MTG, CABLE TERMINAL, 6-14AWG, LUG&SCREW, ROHS |
| TP23, TP29 | DNP | 0 | | DNP-PLACE HOLDER |

ISL8120EVAL3Z Board Layout

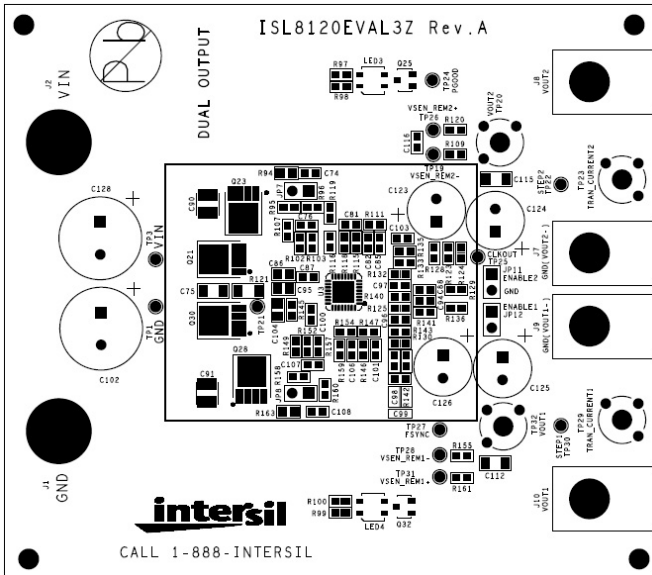


FIGURE 4. TOP SILKSCREEN

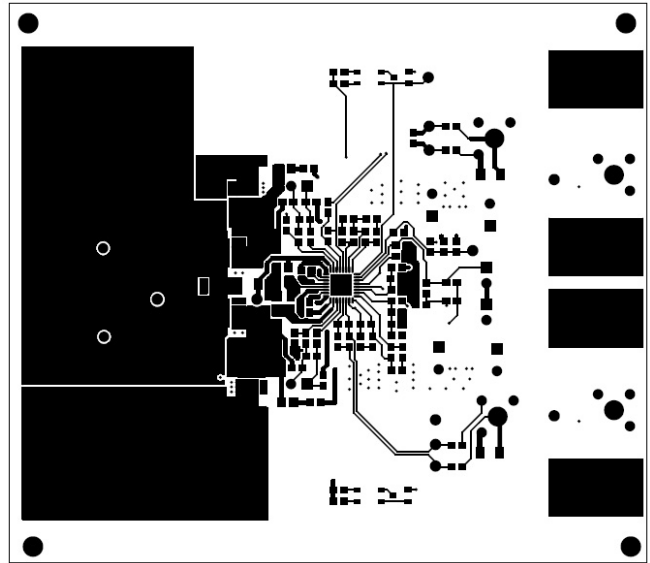


FIGURE 5. TOP LAYER

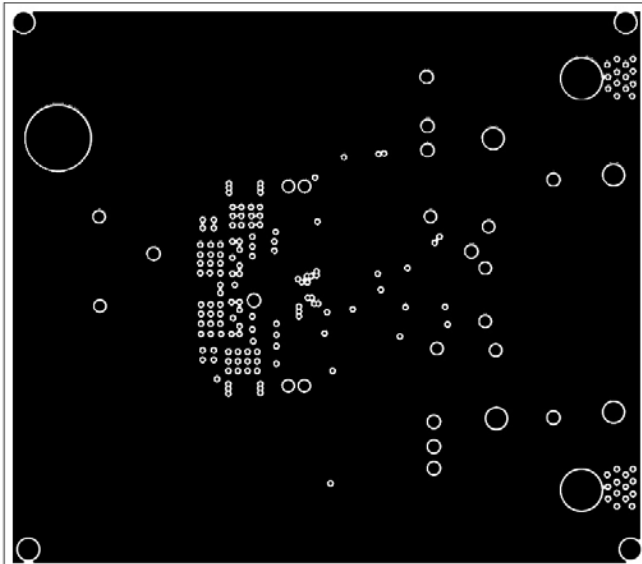


FIGURE 6. SECOND LAYER

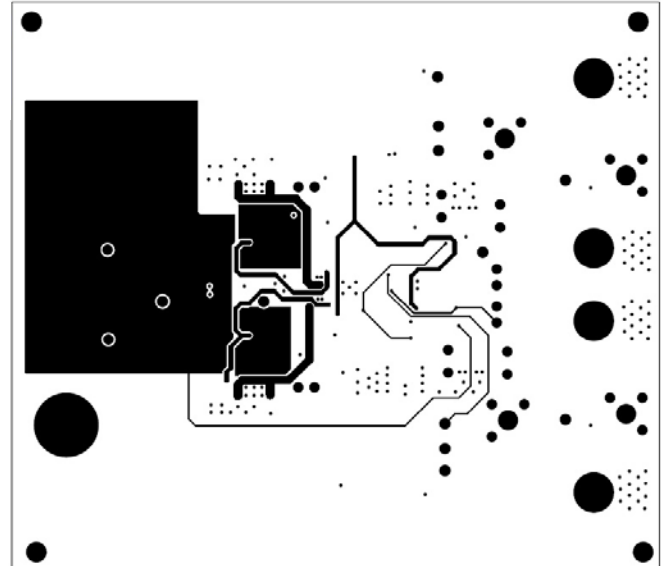


FIGURE 7. THIRD LAYER

ISL8120EVAL3Z Board Layout (Continued)

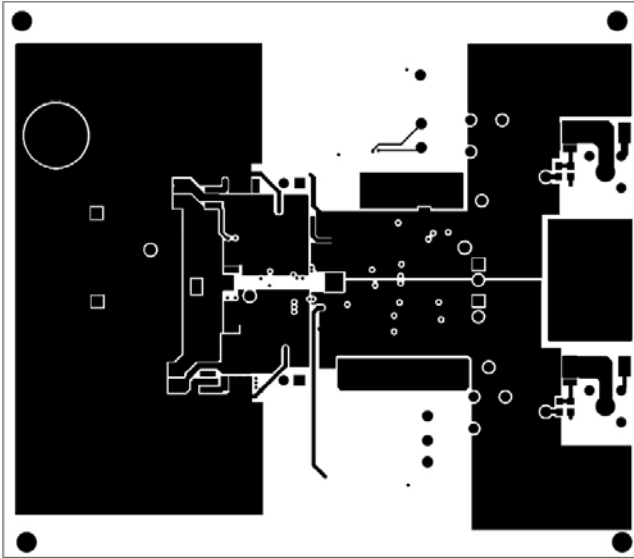


FIGURE 8. BOTTOM LAYER

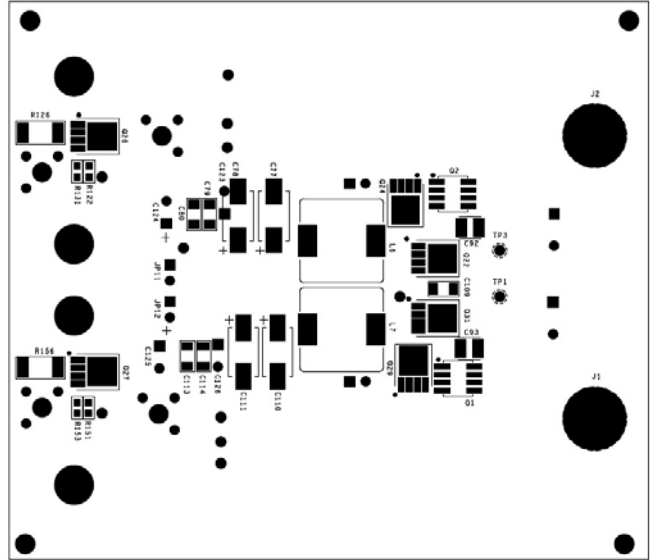


FIGURE 9. BOTTOM SILKSCREEN (MIRRORED)

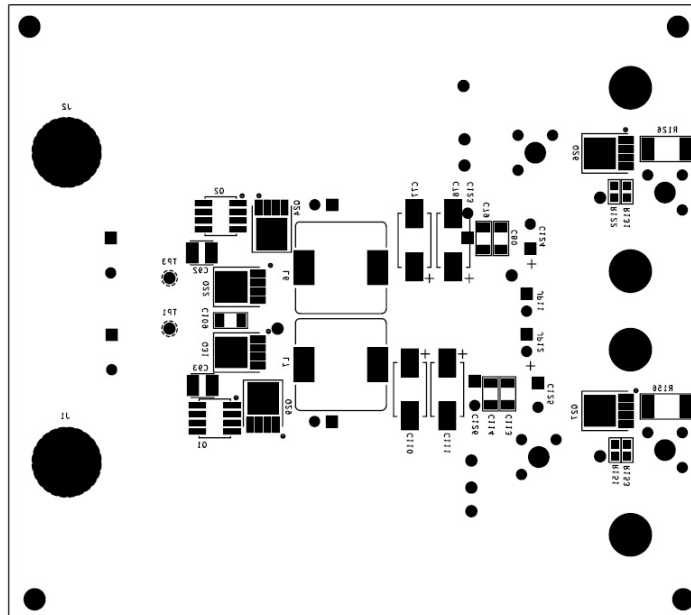


FIGURE 10. BOTTOM SILKSCREEN

Test Data for ISL8120EVAL3Z

Efficiency

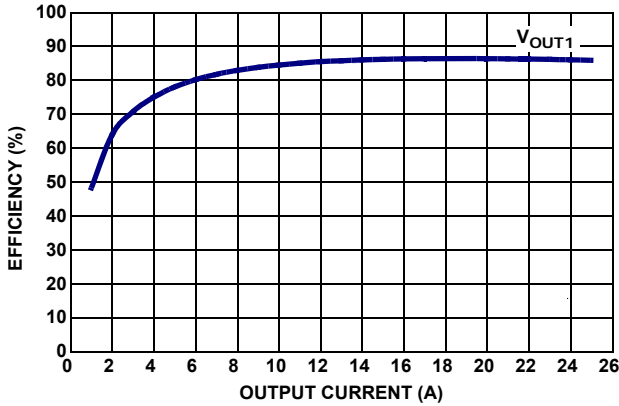


FIGURE 11. CHANNEL 1 EFFICIENCY (12V V_{IN} AND 1.2V V_{OUT})

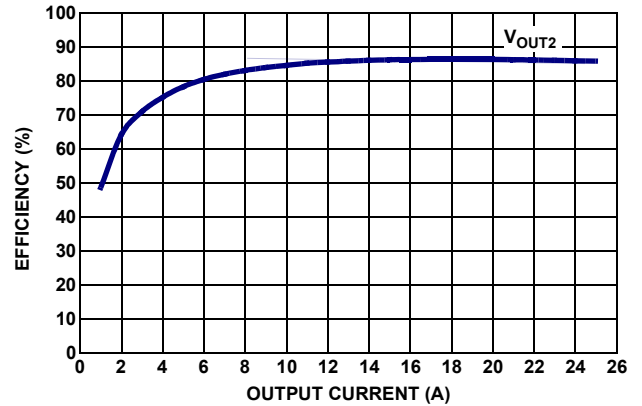


FIGURE 12. CHANNEL 2 EFFICIENCY (12V V_{IN} AND 1.2V V_{OUT})

Line Regulation

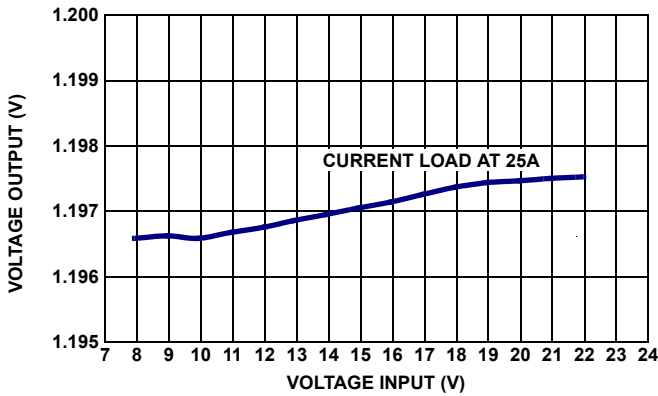


FIGURE 13. CHANNEL 1 LINE REGULATION

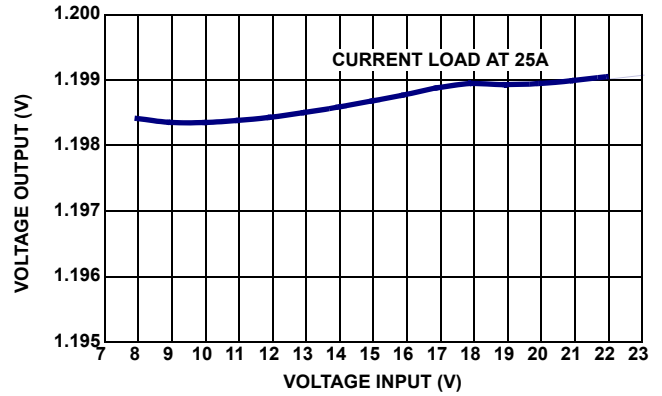


FIGURE 14. CHANNEL 1 LINE REGULATION

Start-Up

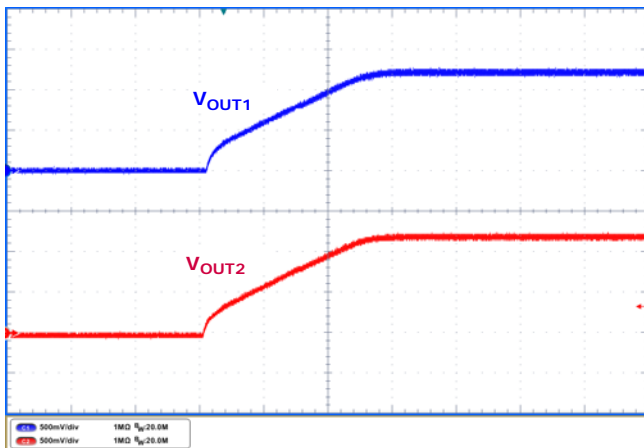


FIGURE 15. POWER-UP UNDER FULL LOAD (25A FOR EACH CHANNEL)

Load Transient

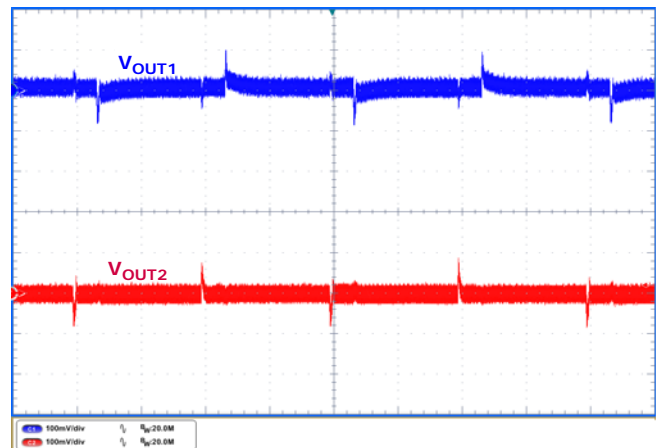


FIGURE 16. LOAD TRANSIENT (0A TO 25A STEP, SLEW_RATE = 1.6A/MS)

Test Data for ISL8120EVAL3Z (Continued)

Output Ripple

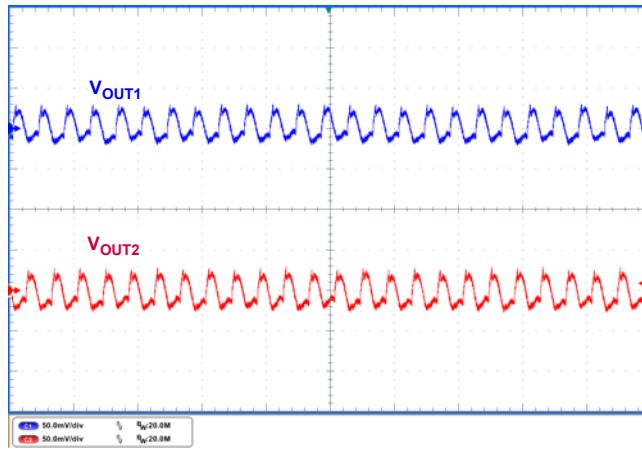


FIGURE 17. OUTPUT RIPPLES UNDER 25A LOAD FOR EACH CHANNEL

DDR Application Waveforms

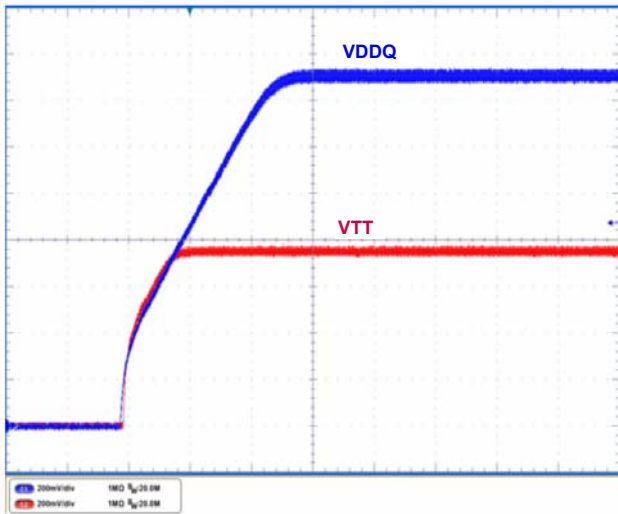


FIGURE 18. VDDQ AND VTT START-UP TRACKING (DDR3)

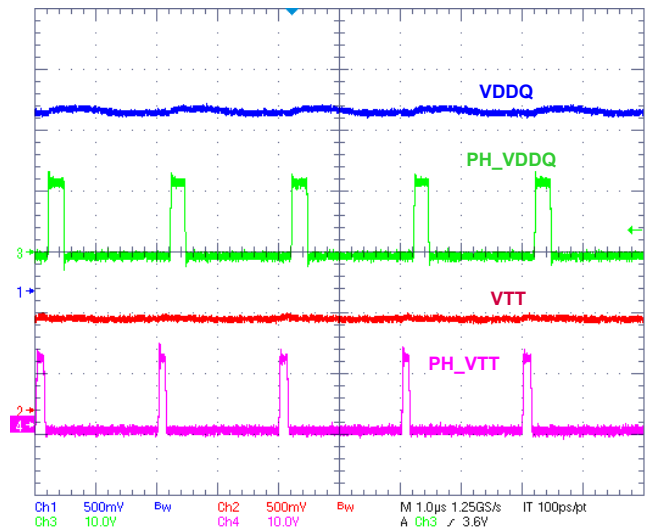


FIGURE 19. PHASE AND VOUTS (DDR3)