ISL8130EVAL2Z

Evaluation Board

AN1909
Rev 0.00
December 20, 2013

Introduction

The ISL8130 is a wide input range, synchronous buck controller. It is designed to drive N-Channel MOSFETs in a synchronous rectified buck topology for up to 25A load current. The ISL8130 integrates control, output adjustment, monitoring and protection functions into a single package. All the necessary components are with a 2.125 inch by 1.25 inch PCB area.

The ISL8130EVAL2Z provides simple, voltage mode control with fast transient response. The 0.6V internal reference as well as external reference can be selected via the REFIN pin.

The ISL8130 is offered in a space saving 4x4 QFN and easy-to-use 20 Ld QSOP packages.

Evaluation Board Specifications

TABLE 1. EVALUATION BOARD ELECTRICAL SPECIFICATIONS

SPEC	DESCRIPTION	MIN	TYP	MAX	UNIT
VIN	Input Voltage	5.6	12	16	V
VOUT	Output Voltage	4.75	5.0	5.25	V
IOUT	Output Current		25		A
Fsw	Switching Frequency		280		kHz
η	Efficiency, V_{IN} = 12V, I_{OUT} = 25A		94		%

FIGURE 1. PHOTOGRAPH OF THE ISL8130EVAL2Z EVALUATION BOARD

TABLE 2. RECOMMENDED COMPONENT SELECTION FOR QUICK EVALUATION

V_{OUT} (V)	I_{OUT} (A)	UPPER MOSFET	LOWER MOSFET	INDUCTOR	FSW/RT (kHz/kΩ)
5	25	2 X BSC057N03 LS	2 X BSC057N03 LS	SER2010-901ML	280/52.3
5	15	1 X BSC057N03 LS	1 X BSC030N03 LS	SER2009-901ML	500/31.6
3.3	25	2 X BSC057N03 LS	2 X BSC030N03 LS	SER2010-901ML	280/52.3
3.3	15	1 X BSC057N03 LS	1 X BSC030N03 LS	SER2009-901ML	500/31.6

Please contact Intersil Sales for assistance.

Recommended Equipment

The following equipment are recommended for evaluation:

- 0V to 30V power supply with 30A source current capability
- Electronic load capable of sinking 25A
- Digital Multimeters (DMMs)
- 100MHz Quad-Trace Oscilloscope

Quick Test Setup

1. Ensure that the Eval board is correctly connected to the power supply and the electronic load prior to apply any power. Please refer to Figure 2 for proper set-up.
2. Connect jumpers J1 to the Internal Reference position; Connect jumper J8 to the Disable position.
3. Turn on the power supply, V_{IN} = 12V. The PWM should be inhibited at this time.
4. Connect jumper J8 to the Enable position. Adjust input voltage VIN within the specified range and observe output voltage. The output voltage variation should be within 4.75V to 5.25V.
5. Adjust load current within 25A. The output voltage variation should be within 4.75V to 5.25V.
6. Use oscilloscope to observe output ripple voltage and phase node ringing. For accurate measurement, please refer to Figure 3 for proper probe set-up.
7. Optimization. Please refer to Table 2 for optimization recommendation.

NOTE: Test points: VOUT, GND, GND, VIN are for voltage measurement only. Do not allow high current through these test points.

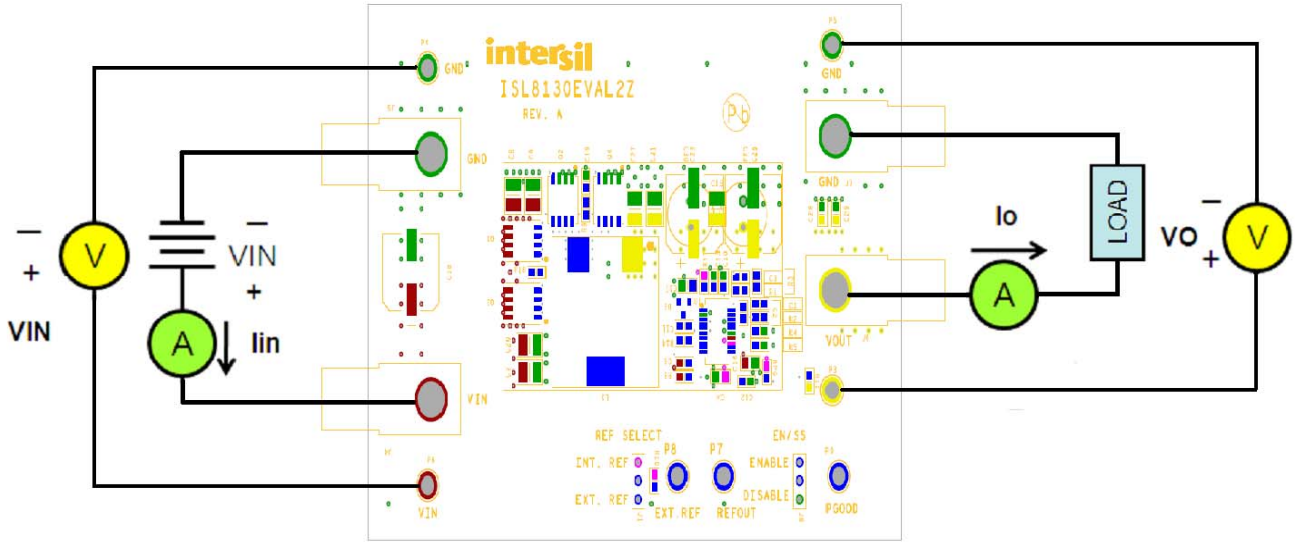

FIGURE 2. ISL8130EVAL2Z TEST SET-UP

Probe Set-up

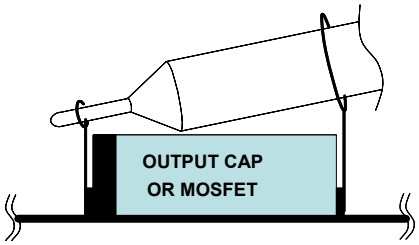

FIGURE 3. OSCILLOSCOPE PROBE SET-UP

External Reference

If REFIN pin is tied to VCC5, then the internal 0.6V reference is used as the error amplifier non-inverting input. If the REFIN is connected to an external voltage source between 0.6V to 1.25V, then this external voltage is used as the reference voltage at the positive input of the error amplifier.

Typical Performance Curves

Input voltage is 12V and output voltage is 5V unless otherwise specified.

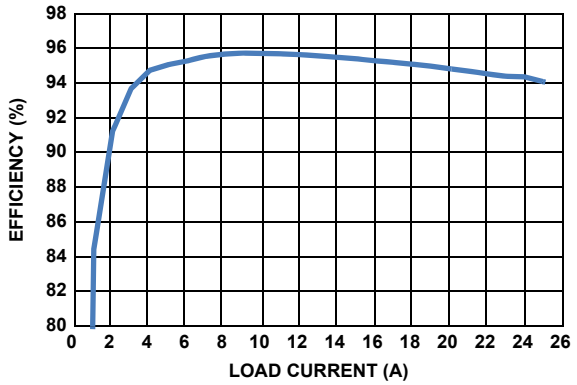

FIGURE 4. EFFICIENCY vs LOAD CURRENT

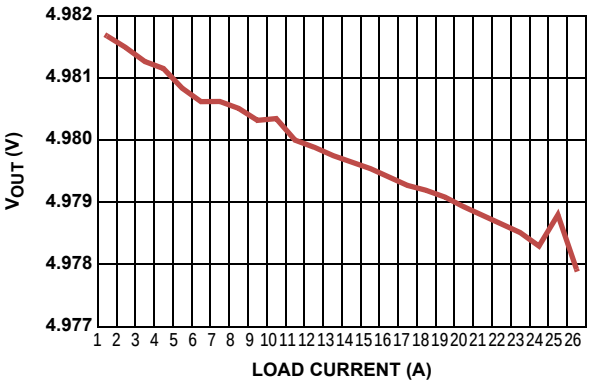

FIGURE 5. LOAD REGULATION, (V_{IN} = 12V, I_{MAX} = 25A)

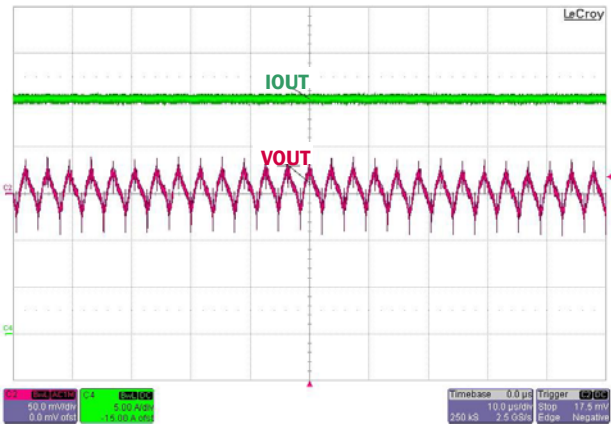

FIGURE 6. OUTPUT RIPPLE (VO = 5V, LOAD = 25A)

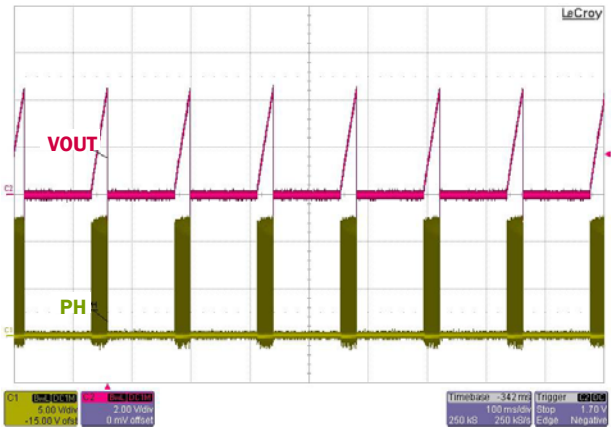

FIGURE 7. OVERCURRENT PROTECTION (VO = 5V, LOAD = 40A)

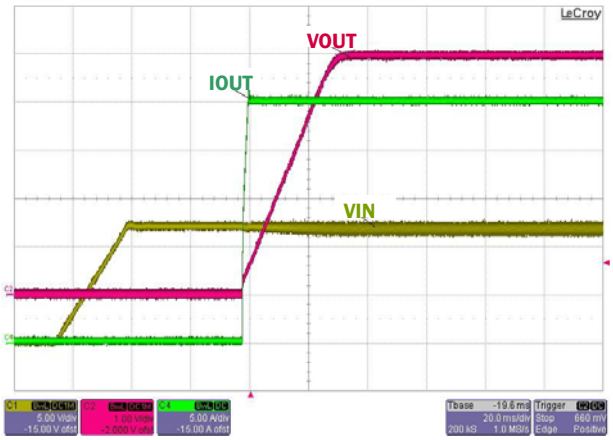

FIGURE 8. SOFT-START AT FULL LOAD

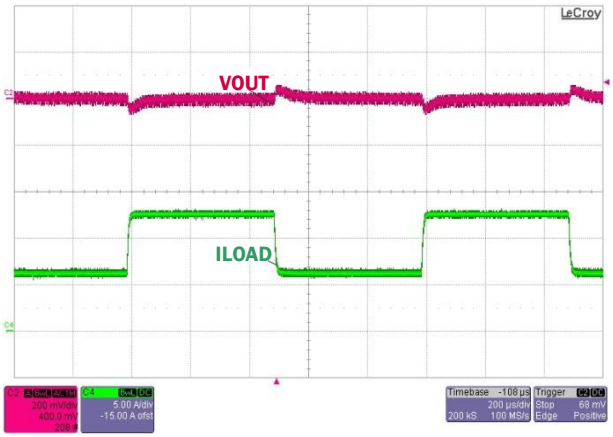

FIGURE 9. LOAD TRANSIENT (25% TO 50% AT 2A/µs)

ISL8130EVAL2Z Schematic

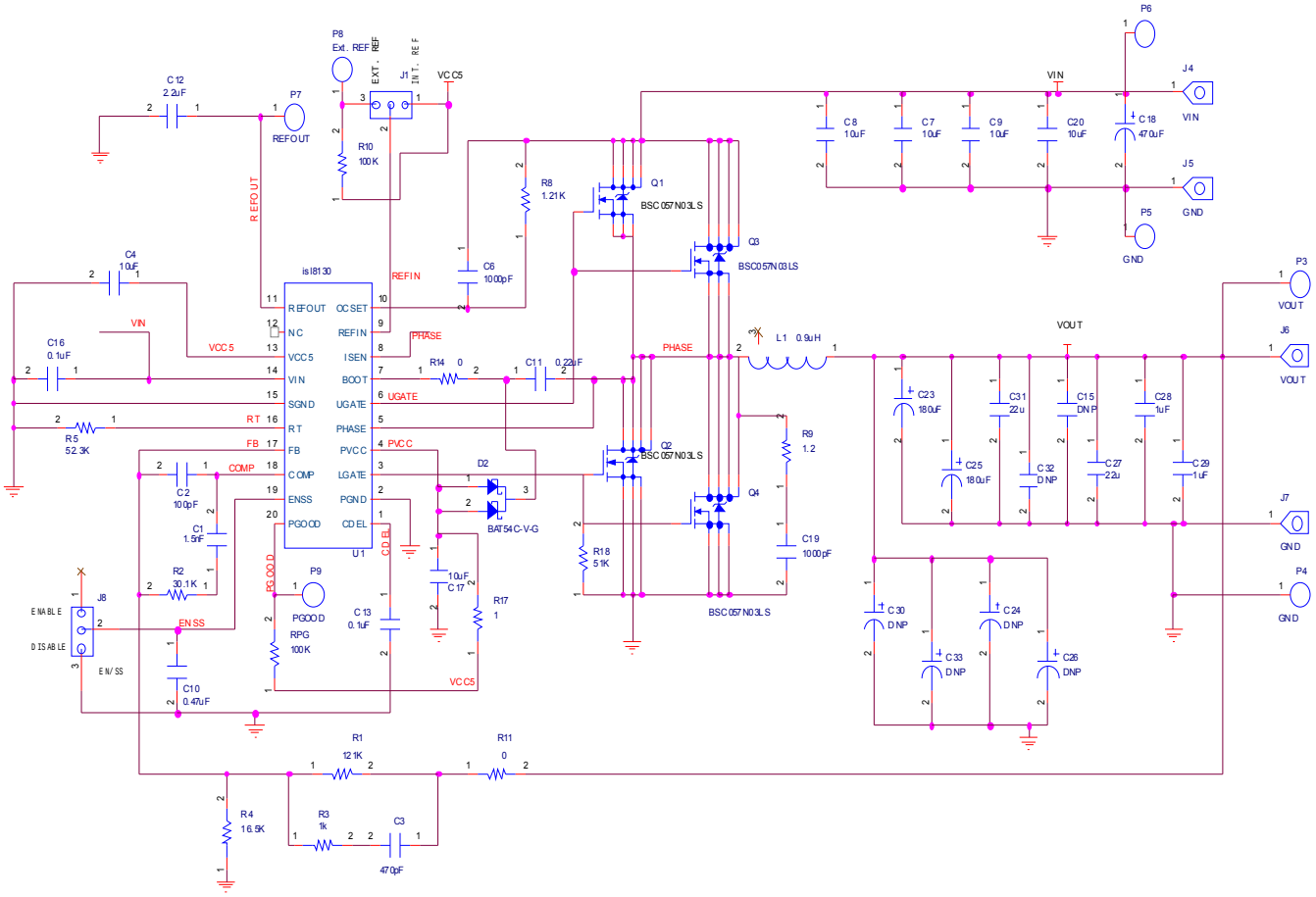

TABLE 3. ISL8130EVAL2Z BILL OF MATERIALS

ITEM	QTY	PART REFERENCE	VALUE	DESCRIPTION	PART NUMBER	MANUFACTURER
ESSENTIAL COMPONENTS						
1	1	C3	470pF	Ceramic CAP, NP0 or C0G, sm0603	GENERIC	GENERIC
2	2	C13, C16	0.1µF	Ceramic CAP, X5R, 50V, sm0603	GENERIC	GENERIC
3	2	C4, C17	10µF	Ceramic CAP, X5R, 10V, sm0805	GENERIC	GENERIC
4	1	C10	0.47µF	Ceramic CAP, X5R, 16V, sm0603	GENERIC	GENERIC
5	3	C27, C31	22µF	Ceramic CAP, X5R, 25V, sm1210	GENERIC	GENERIC
6	1	C12	2.2µF	Ceramic CAP, X5R, 16V, sm0603	GENERIC	GENERIC
7	2	C6, C19	1000pF	Ceramic CAP, NP0 or C0G, sm0603	GENERIC	GENERIC
8	2	C23, C25	180µF	OSCON, 16V, Radial 8x9	16SEPC180MX	SANYO
9	4	C7, C8, C9, C20	10µF	Ceramic CAP, X5R, 25V, sm1210	GENERIC	GENERIC
10	1	C2	100pF	Ceramic CAP, NP0 or C0G, sm0603	GENERIC	GENERIC
11	2	C28, C29	1µF	Ceramic CAP, X5R, 25V,sm0603	GENERIC	GENERIC
12	1	C1	1500pF	Ceramic CAP, NP0 or C0G, sm0603	GENERIC	GENERIC
13	1	C11	0.22µF	Ceramic CAP, X5R, 16V,sm0603	GENERIC	GENERIC
14	1	C18	470µF	Alum. Cap, 50V	16SVPE470M	SANYO
15	1	D2		Schottky Diode, 30V, SOT23	BAT54C	Fairchild
16	1	L1	0.9µH	Inductor	SER2010-901ML	Coilcraft
17	4	Q1, Q2, Q3, Q4		Single Channel NFET, 30V	BSC057N03LS G	Infineon
18	1	R5	52.3k	Resistor, sm0603, 1%	GENERIC	GENERIC
19	1	R9	1.2	Resistor, sm0603, 10%	GENERIC	GENERIC
20	1	R2	30.1k	Resistor, sm0603, 1%	GENERIC	GENERIC
21	2	R11, R14	0	Resistor, sm0603, 10%	GENERIC	GENERIC
22	1	R4	16.5k	Resistor, sm0603, 1%	GENERIC	GENERIC
23	1	R17	1	Resistor, sm0603, 10%	GENERIC	GENERIC
24	1	R18	51k	Resistor, sm0603, 1%	GENERIC	GENERIC
25	1	R1	121k	Resistor, sm0603, 1%	GENERIC	GENERIC
26	1	R8	1.21k	Resistor, sm0603, 1%	GENERIC	GENERIC
27	1	R3	1k	Resistor, sm0603, 1%	GENERIC	GENERIC
28	2	R10, RPG	100k	Resistor, sm0603, 1%	GENERIC	GENERIC
29	1	U1		PWM CONTROLLER, 20 Ld QSOP	ISL8130IAZ	INTERSIL
OPTIONAL COMPONENTS						
30	6	C15, C24, C26, C30, C32, C33	DO NOT POPULATE			
EVALUATION HARDWARE						
31	4	J4, J5, J6, J7		HARDWARE, MTG, CABLE TERMINAL, 6-14AWG, LUG&SCRE , ROHS	KPA8CTP	BERG/FCI
32	2	J1, J8		1x3 Header	GENERIC	GENERIC
33	7	P3, P4, P5, P6, P7, P8, P9		Test Points	1514-2	Keystone

ISL8130EVAL2Z PCB Layout

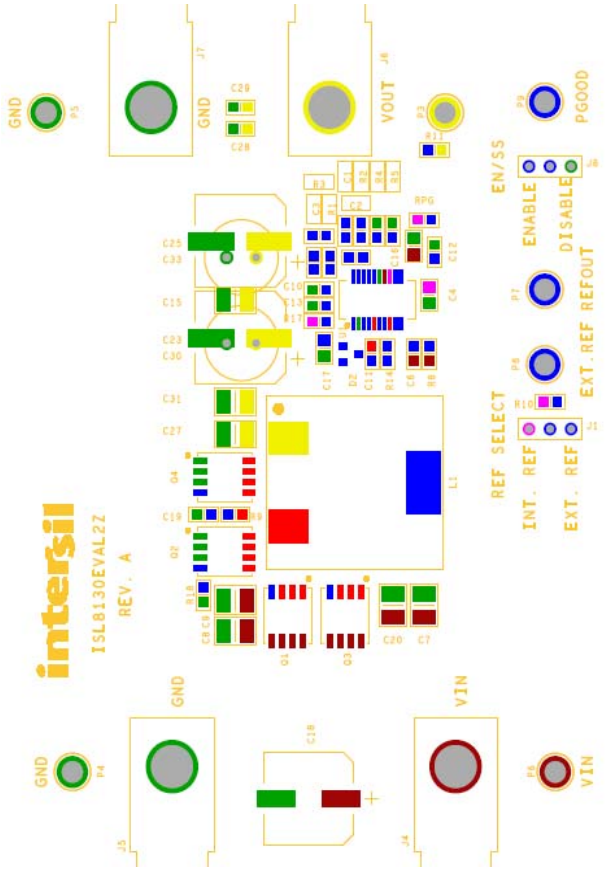

FIGURE 10. TOP SILKSCREEN

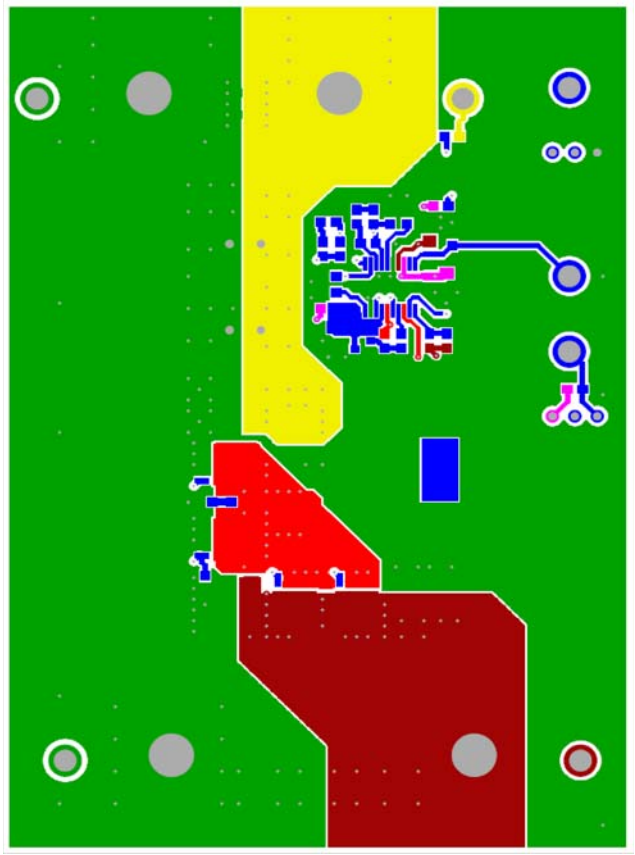

FIGURE 11. TOP LAYER

ISL8130EVAL2Z PCB Layout (Continued)

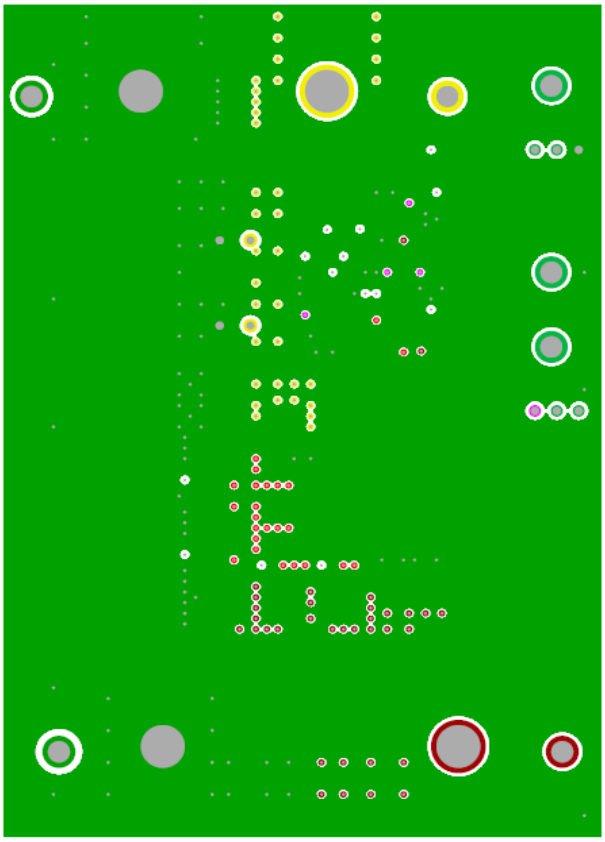

FIGURE 12. SECOND LAYER(SOLID GROUND)

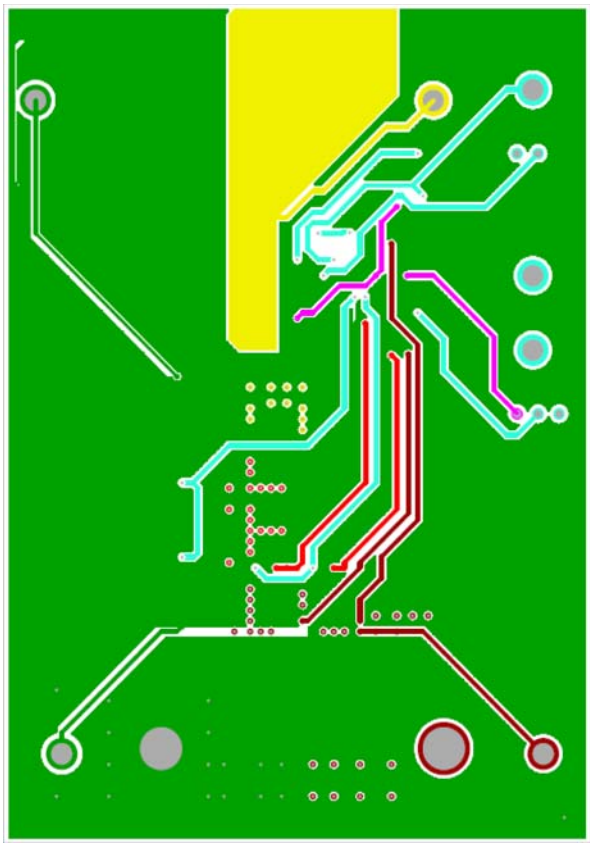

FIGURE 13. THIRD LAYER

ISL8130EVAL2Z PCB Layout (Continued)

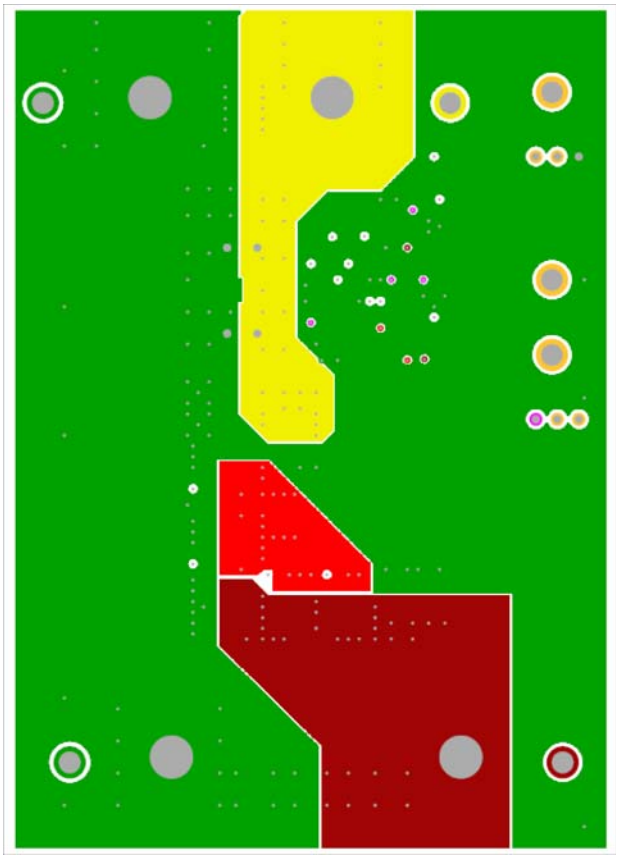

FIGURE 14. BOTTOM LAYER

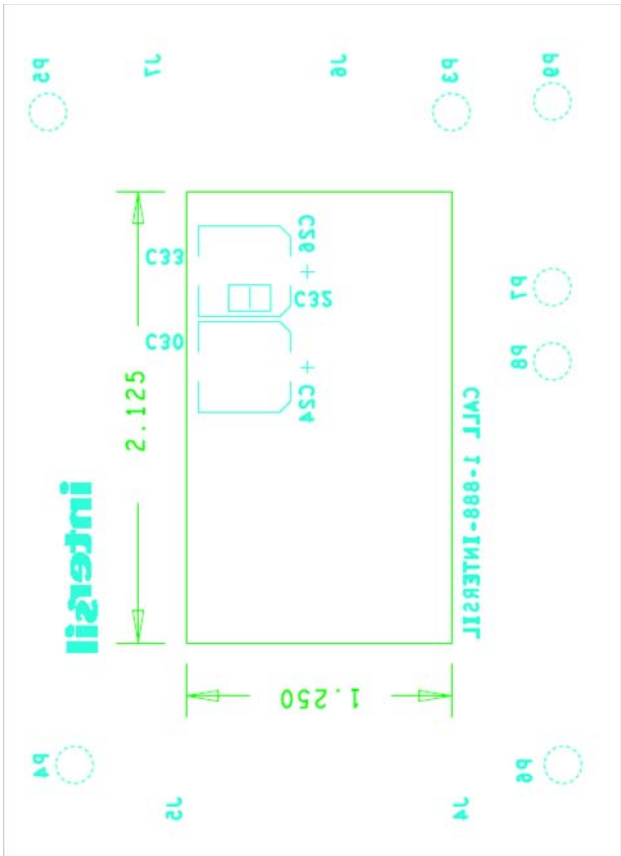

FIGURE 15. BOTTOM SILKSCREEN