ISL8487, ISL81483, ISL81487

1/8 Unit Load, 5V, Low Power, High Speed or Slew Rate Limited, RS-485/RS-422 Transceivers

FN6050
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These Intersil RS-485/RS-422 devices are “fractional” unit load (UL), BiCMOS, 5V powered, single transceivers that meet both the RS-485 and RS-422 standards for balanced communication. Unlike competitive devices, this Intersil family is specified for 10% tolerance supplies (4.5V to 5.5V).

The ISL81483 and ISL81487 present a 1/8 unit load to the RS-485 bus, which allows up to 256 transceivers on the network for large node count systems (e.g., process automation, remote meter reading systems). The 1/4 UL ISL8487 allows up to 128 transceivers on the bus. In a remote utility meter reading system, individual (apartments for example) utility meter readings are routed to a concentrator via an RS-485 network, so the high allowed node count minimizes the number of repeaters required to network all the meters. Data for all meters is then read out from the concentrator via a single access port, or a wireless link.

Slew rate limited drivers on the ISL8487 and ISL81483 reduce EMI, and minimize reflections from improperly terminated transmission lines, or unterminated stubs in multidrop and multipoint applications. Data rates up to 250kbps are achievable with these devices.

Data rates up to 5Mbps are achievable by using the ISL81487, which features higher slew rates.

Receiver (Rx) inputs feature a “fail-safe if open” design, which ensures a logic high Rx output if Rx inputs are floating.

Driver (Tx) outputs are short circuit protected, even for voltages exceeding the power supply voltage. Additionally, on-chip thermal shutdown circuitry disables the Tx outputs to prevent damage if power dissipation becomes excessive.

These half duplex devices multiplex the Rx inputs and Tx outputs to allow transceivers with Rx and Tx disable functions in 8 lead packages.

Features

- Fractional Unit Load Allows up to 256 Devices on the Bus
- Specified for 10% Tolerance Supplies
- Class 3 ESD Protection (HBM) on all Pins. . . . . >7kV
- High Data Rate Version (ISL81487). . . . . . . up to 5Mbps
- Slew Rate Limited Versions for Error Free Data Transmission (ISL8487, ISL81483) . . . . . . .up to 250kbps
- Low Current Shutdown Mode (Except ISL81487) . . 0.5μA
- Low Quiescent Supply Current:
  - ISL8487, ISL81483. . . . . 145μA (Max.)
  - ISL81487 . . . . 420μA (Max.)
- -7V to +12V Common Mode Input Voltage Range
- Three State Rx and Tx Outputs
- 30ns Propagation Delays, 5ns Skew (ISL81487)
- Half Duplex Pinouts
- Operate from a Single +5V Supply (10% Tolerance)
- Current Limiting and Thermal Shutdown for Driver Overload Protection
- Drop-In Replacements for: MAX487 (ISL8487); MAX1483 (ISL81483); MAX1487, LMS1487 (ISL81487)
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

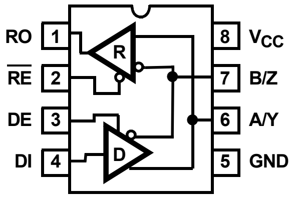
- High Node Count Networks
- Automated Utility Meter Reading Systems
- Factory Automation
- Security Networks
- Building Environmental Control Systems
- Industrial/Process Control Networks

TABLE 1. SUMMARY OF FEATURES

PART NUMBER	HALF/FULL DUPLEX	NO. OF DEVICES ALLOWED ON BUS	DATA RATE (Mbps)	SLEW-RATE LIMITED?	RECEIVER/ DRIVER ENABLE?	QUIESCENT I_{CC} (μA)	LOW POWER SHUTDOWN?	PIN COUNT
ISL8487 **(No longer available or supported)**	Half	128	0.25	Yes	Yes	120	Yes	8
ISL81483	Half	256	0.25	Yes	Yes	120	Yes	8
ISL81487	Half	256	5	No	Yes	350	No	8

Pinout

ISL8487, ISL81483, ISL81487 (PDIP, SOIC)
TOP VIEW



Truth Tables

TRANSMITTING				
INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	Z	Y
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	High-Z *	High-Z *

*Shutdown Mode for ISL8487, ISL81483 (see Note 7)

RECEIVING			
INPUTS			OUTPUT
$\overline{RE}$	DE	A-B	RO
0	0	≥ +0.2V	1
0	0	≤ -0.2V	0
0	0	Inputs Open	1
1	0	X	High-Z *
1	1	X	High-Z

*Shutdown Mode for ISL8487, ISL81483 (see Note 7)

Ordering Information

PART NO.	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL8487IBZ (Note) **(No longer available, recommended replacement ISL8487EIBZ)**	8487IBZ	-40 to 85	8 Ld SOIC* (Pb-free)	M8.15
ISL8487IPZ (Note) **(No longer available, recommended replacement ISL8487EIPZ)**	8487IPZ	-40 to 85	8 Ld PDIP** (Pb-free)	E8.3
ISL81483IBZ (Note)	81483IBZ	-40 to 85	8 Ld SOIC* (Pb-free)	M8.15
ISL81483IPZ (Note)	81483IPZ	-40 to 85	8 Ld PDIP** (Pb-free)	E8.3
ISL81487IBZ (Note)	81487IBZ	-40 to 85	8 Ld SOIC* (Pb-free)	M8.15

*SOIC also available in Tape and Reel; Add “-T” to suffix.
**Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

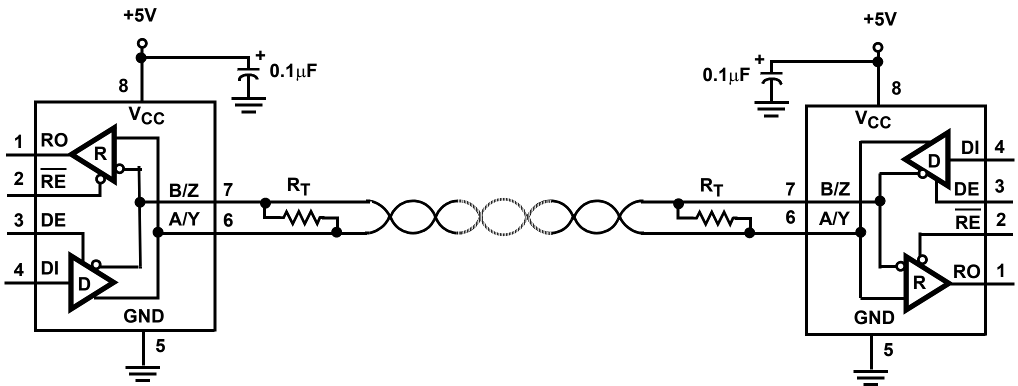
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pin Descriptions

PIN	FUNCTION
RO	Receiver output: If A > B by at least 0.2V, RO is high; If A < B by 0.2V or more, RO is low; RO = High if A and B are unconnected (floating).
$\overline{RE}$	Receiver output enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high.
DE	Driver output enable. The driver outputs, Y and Z, are enabled by bringing DE high. They are high impedance when DE is low.
DI	Driver input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
GND	Ground connection.
A/Y	RS-485/422 level, noninverting receiver input and noninverting driver output. Pin is an input (A) if DE = 0; pin is an output (Y) if DE = 1.
B/Z	RS-485/422 level, inverting receiver input and inverting driver output. Pin is an input (B) if DE = 0; pin is an output (Z) if DE = 1.
V_{CC}	System power supply input (4.5V to 5.5V).

Typical Operating Circuits

ISL8487, ISL81483, ISL81487



Absolute Maximum Ratings

V_{CC} to Ground 7V
Input Voltages
DI, DE, $\overline{RE}$ . . . . -0.5V to (V_{CC} +0.5V)
Input/Output Voltages
A/Y, B/Z . . . . -8V to +12.5V
RO . . . . -0.5V to (V_{CC} +0.5V)
Short Circuit Duration
Y, Z . . . . Continuous
ESD Rating
HBM (Per MIL-STD-883, Method 3015.7) . . . . >7kV

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
8 Ld SOIC Package 170
8 Ld PDIP Package* 140
Maximum Junction Temperature (Plastic Package) . . . . 150°C
Maximum Storage Temperature Range . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
(SOIC - Lead Tips Only)

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

Operating Conditions

Temperature Range
ISL8XXXIX . . . . -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Test Conditions: V_{CC} = 4.5V to 5.5V; Unless Otherwise Specified. Typicals are at V_{CC} = 5V, T_A = 25°C, (Note 2)

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS								
Driver Differential V_{OUT} (no load)	V_{OD1}			Full	-	-	V_{CC}	V
Driver Differential V_{OUT} (with load)	V_{OD2}	R = 50Ω (RS-422), (Figure 1)		Full	2	3	-	V
		R = 27Ω (RS-485), (Figure 1)		Full	1.5	2.3	5	V
Change in Magnitude of Driver Differential V_{OUT} for Complementary Output States	ΔV_{OD}	R = 27Ω or 50Ω, (Figure 1)		Full	-	0.01	0.2	V
Driver Common-Mode V_{OUT}	V_{OC}	R = 27Ω or 50Ω, (Figure 1)		Full	-	-	3	V
Change in Magnitude of Driver Common-Mode V_{OUT} for Complementary Output States	ΔV_{OC}	R = 27Ω or 50Ω, (Figure 1)		Full	-	0.01	0.2	V
Logic Input High Voltage	V_{IH}	DE, DI, $\overline{RE}$		Full	2	-	-	V
Logic Input Low Voltage	V_{IL}	DE, DI, $\overline{RE}$		Full	-	-	0.8	V
Logic Input Current	I_{IN1}	DE, DI, $\overline{RE}$		Full	-2	-	2	µA
Input Current (A/Y, B/Z), (Note 10) (ISL81483, ISL81487)	I_{IN2}	DE = 0V, V_{CC} = 4.5 to 5.5V	V_{IN} = 12V	Full	-	-	140	µA
			V_{IN} = -7V	Full	-	-	-120	µA
	I_{IN2}	DE = 0V, V_{CC} = 0V	V_{IN} = 12V	Full	-	-	180	µA
			V_{IN} = -7V	Full	-	-	-100	µA
Input Current (A/Y, B/Z), (Note 11) (ISL8487 Only)	I_{IN2}	DE = 0V, V_{CC} = 0V, or 4.5 to 5.5V	V_{IN} = 12V	Full	-	-	250	µA
			V_{IN} = -7V	Full	-	-	-100	µA
Receiver Differential Threshold Voltage	V_{TH}	$-7V \le V_{CM} \le 12V$		Full	-0.2	-	0.2	V
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V		25	-	70	-	mV
Receiver Output High Voltage	V_{OH}	I_O = -4mA, V_{ID} = 200mV		Full	3.5	-	-	V
Receiver Output Low Voltage	V_{OL}	I_O = -4mA, V_{ID} = 200mV		Full	-	-	0.4	V
Three-State (high impedance) Receiver Output Current	I_{OZR}	$0.4V \le V_O \le 2.4V$		Full	-	-	±1	µA

Electrical Specifications

Test Conditions: V_{CC} = 4.5V to 5.5V; Unless Otherwise Specified. Typicals are at V_{CC} = 5V, T_A = 25°C, (Note 2) **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN	TYP	MAX	UNITS
Receiver Input Resistance	R_{IN}	$-7V \le V_{CM} \le 12V$	ISL81483, ISL81487	Full	96	-	-	kΩ
			ISL8487	Full	48	-	-	kΩ
No-Load Supply Current, (Note 3)	I_{CC}	ISL81487, DI, $\overline{RE}$ = 0V or V_{CC}	DE = V_{CC}	Full	-	400	500	µA
			DE = 0V	Full	-	350	420	µA
		ISL8487, ISL81483, DI, $\overline{RE}$ = 0V or V_{CC}	DE = V_{CC}	Full	-	160	200	µA
			DE = 0V	Full	-	120	145	µA
Shutdown Supply Current	I_{SHDN}	(Note 7), DE = 0V, $\overline{RE}$ = V_{CC}, DI = 0V or V_{CC}		Full	-	0.5	8	µA
Driver Short-Circuit Current, V_O = High or Low	I_{OSD1}	DE = V_{CC}, $-7V \le V_Y$ or $V_Z \le 12V$, (Note 4)		Full	35	-	250	mA
Receiver Short-Circuit Current	I_{OSR}	$0V \le V_O \le V_{CC}$		Full	7	-	85	mA
SWITCHING CHARACTERISTICS (ISL81487)								
Driver Input to Output Delay	t_{PLH}, t_{PHL}	R_{DIFF} = 54Ω, C_L = 100pF, (Figure 2)		Full	15	24	50	ns
Driver Output Skew	t_{SKEW}	R_{DIFF} = 54Ω, C_L = 100pF, (Figure 2)		Full	-	2	10	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_{DIFF} = 54Ω, C_L = 100pF, (Figure 2)		Full	3	12	25	ns
Driver Enable to Output High	t_{ZH}	C_L = 100pF, SW = GND, (Figure 3)		Full	-	14	70	ns
Driver Enable to Output Low	t_{ZL}	C_L = 100pF, SW = V_{CC}, (Figure 3)		Full	-	14	70	ns
Driver Disable from Output High	t_{HZ}	C_L = 15pF, SW = GND, (Figure 3)		Full	-	44	70	ns
Driver Disable from Output Low	t_{LZ}	C_L = 15pF, SW = V_{CC}, (Figure 3)		Full	-	21	70	ns
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	(Figure 4)		Full	30	90	150	ns
Receiver Skew | t_{PLH} - t_{PHL} |	t_{SKD}	(Figure 4)		25	-	5	-	ns
Receiver Enable to Output High	t_{ZH}	C_L = 15pF, SW = GND, (Figure 5)		Full	-	9	50	ns
Receiver Enable to Output Low	t_{ZL}	C_L = 15pF, SW = V_{CC}, (Figure 5)		Full	-	9	50	ns
Receiver Disable from Output High	t_{HZ}	C_L = 15pF, SW = GND, (Figure 5)		Full	-	9	50	ns
Receiver Disable from Output Low	t_{LZ}	C_L = 15pF, SW = V_{CC}, (Figure 5)		Full	-	9	50	ns
Maximum Data Rate	f_{MAX}			Full	5	-	-	Mbps
SWITCHING CHARACTERISTICS (ISL8487, ISL81483)								
Driver Input to Output Delay	t_{PLH}, t_{PHL}	R_{DIFF} = 54Ω, C_L = 100pF, (Figure 2)		Full	250	650	2000	ns
Driver Output Skew	t_{SKEW}	R_{DIFF} = 54Ω, C_L = 100pF, (Figure 2)		Full	-	160	800	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_{DIFF} = 54Ω, C_L = 100pF, (Figure 2)		Full	250	900	2000	ns
Driver Enable to Output High	t_{ZH}	C_L = 100pF, SW = GND, (Figure 3, Note 5)		Full	250	1000	2000	ns
Driver Enable to Output Low	t_{ZL}	C_L = 100pF, SW = V_{CC}, (Figure 3, Note 5)		Full	250	860	2000	ns
Driver Disable from Output High	t_{HZ}	C_L = 15pF, SW = GND, (Figure 3)		Full	300	660	3000	ns
Driver Disable from Output Low	t_{LZ}	C_L = 15pF, SW = V_{CC}, (Figure 3)		Full	300	640	3000	ns
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	(Figure 4)		Full	250	500	2000	ns
Receiver Skew | t_{PLH} - t_{PHL} |	t_{SKD}	(Figure 4)		25	-	60	-	ns
Receiver Enable to Output High	t_{ZH}	C_L = 15pF, SW = GND, (Figure 5, Note 6)		Full	-	10	50	ns
Receiver Enable to Output Low	t_{ZL}	C_L = 15pF, SW = V_{CC}, (Figure 5, Note 6)		Full	-	10	50	ns
Receiver Disable from Output High	t_{HZ}	C_L = 15pF, SW = GND, (Figure 5)		Full	-	10	50	ns
Receiver Disable from Output Low	t_{LZ}	C_L = 15pF, SW = V_{CC}, (Figure 5)		Full	-	10	50	ns
Maximum Data Rate	f_{MAX}			Full	250	-	-	kbps
Time to Shutdown	t_{SHDN}	(Note 7)		Full	50	120	600	ns

Electrical Specifications Test Conditions: V_{CC} = 4.5V to 5.5V; Unless Otherwise Specified. Typicals are at V_{CC} = 5V, T_A = 25°C, (Note 2) **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNITS
Driver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	C_L = 100pF, SW = GND, (Figure 3, Notes 7, 8)	Full	-	1000	2000	ns
Driver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	C_L = 100pF, SW = V_{CC}, (Figure 3, Notes 7, 8)	Full	-	1000	2000	ns
Receiver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	C_L = 15pF, SW = GND, (Figure 5, Notes 7, 9)	Full	-	800	2500	ns
Receiver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	C_L = 15pF, SW = V_{CC}, (Figure 5, Notes 7, 9)	Full	-	800	2500	ns

NOTES:

2. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
3. Supply current specification is valid for loaded drivers when DE = 0V.
4. Applies to peak current. See "Typical Performance Curves" for more information.
5. When testing the ISL8487 and ISL81483, keep $\overline{RE}$ = 0 to prevent the device from entering SHDN.
6. When testing the ISL8487 and ISL81483, the $\overline{RE}$ signal high time must be short enough (typically <200ns) to prevent the device from entering SHDN.
7. The ISL8487 and ISL81483 are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 50ns, the parts are guaranteed not to enter shutdown. If the inputs are in this state for at least 600ns, the parts are guaranteed to have entered shutdown. See "Low-Power Shutdown Mode" section.
8. Keep $\overline{RE}$ = V_{CC}, and set the DE signal low time >600ns to ensure that the device enters SHDN.
9. Set the $\overline{RE}$ signal high time >600ns to ensure that the device enters SHDN.
10. Devices meeting these limits are denoted as "1/8 unit load (1/8 UL)" transceivers. The RS-485 standard allows up to 32 Unit Loads on the bus, so there can be 256 1/8 UL devices on a bus.
11. Devices meeting these limits are denoted as "1/4 unit load (1/4 UL)" transceivers. The RS-485 standard allows up to 32 Unit Loads on the bus, so there can be 128 1/4 UL devices on a bus.

Test Circuits and Waveforms

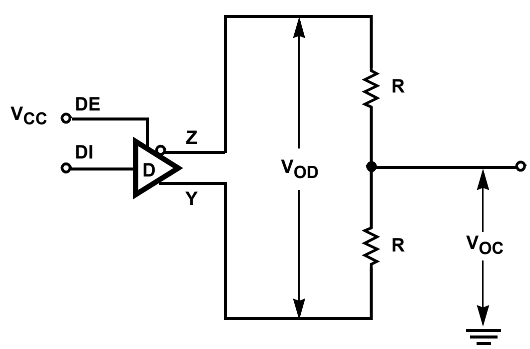


FIGURE 1. DRIVER V_{OD} AND V_{OC}

Test Circuits and Waveforms (Continued)

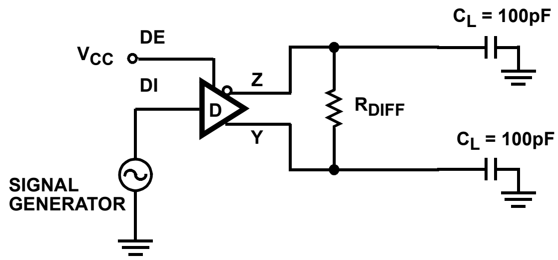


FIGURE 2A. TEST CIRCUIT

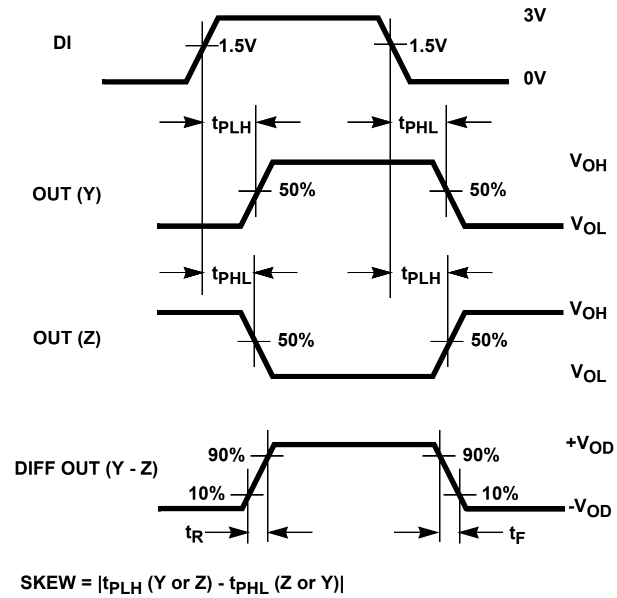
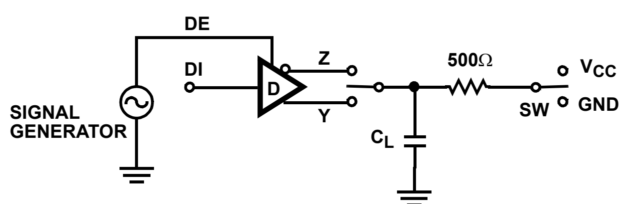


FIGURE 2B. MEASUREMENT POINTS

FIGURE 2. DRIVER PROPAGATION DELAY AND DIFFERENTIAL TRANSITION TIMES



(SHDN) for ISL8487 and ISL81483 only.

PARAMETER	OUTPUT	$\overline{RE}$	DI	SW	C_L (pF)
t_{HZ}	Y/Z	X	1/0	GND	15
t_{LZ}	Y/Z	X	0/1	V_{CC}	15
t_{ZH}	Y/Z	0 (Note 5)	1/0	GND	100
t_{ZL}	Y/Z	0 (Note 5)	0/1	V_{CC}	100
$t_{ZH(SHDN)}$	Y/Z	1 (Note 7)	1/0	GND	100
$t_{ZL(SHDN)}$	Y/Z	1 (Note 7)	0/1	V_{CC}	100

FIGURE 3A. TEST CIRCUIT

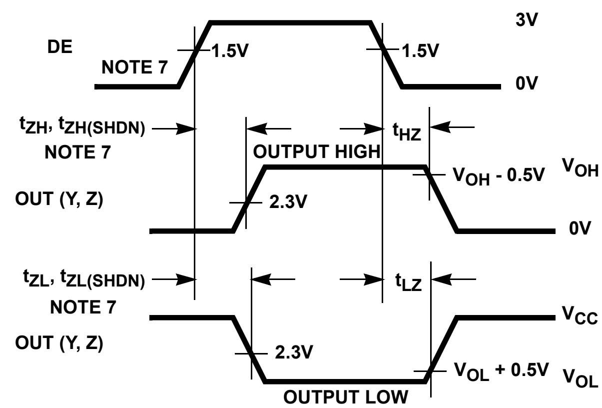


FIGURE 3B. MEASUREMENT POINTS

FIGURE 3. DRIVER ENABLE AND DISABLE TIMES

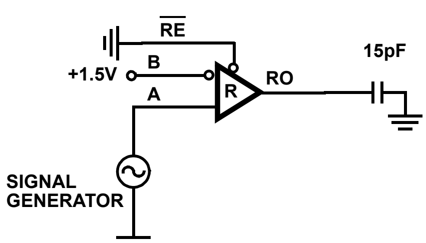


FIGURE 4A. TEST CIRCUIT

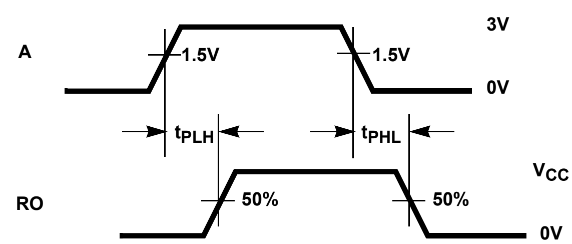
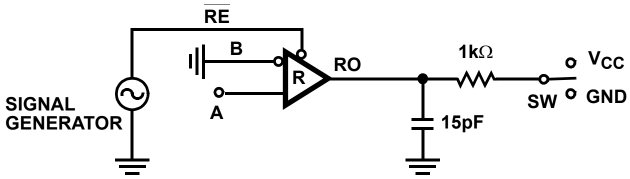


FIGURE 4B. MEASUREMENT POINTS

FIGURE 4. RECEIVER PROPAGATION DELAY

Test Circuits and Waveforms (Continued)



(SHDN) for ISL8487 and ISL81483 only.

PARAMETER	DE	A	SW
t_{HZ}	0	+1.5V	GND
t_{LZ}	0	-1.5V	V_{CC}
t_{ZH} (Note 6)	0	+1.5V	GND
t_{ZL} (Note 6)	0	-1.5V	V_{CC}
$t_{ZH(SHDN)}$ (Note 7)	0	+1.5V	GND
$t_{ZL(SHDN)}$ (Note 7)	0	-1.5V	V_{CC}

FIGURE 5A. TEST CIRCUIT

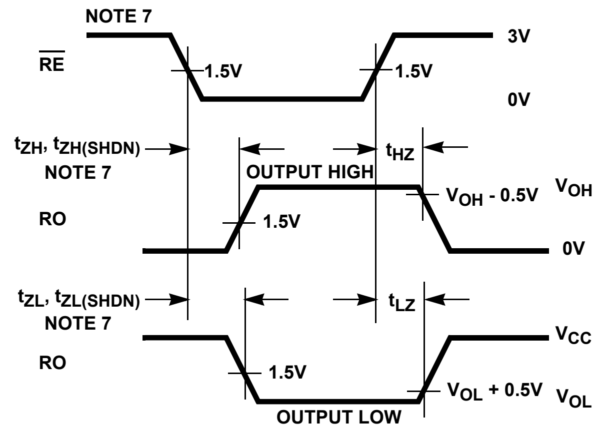


FIGURE 5B. MEASUREMENT POINTS

FIGURE 5. RECEIVER ENABLE AND DISABLE TIMES

Application Information

RS-485 and RS-422 are differential (balanced) data transmission standards for use in long haul or noisy environments. RS-422 is a subset of RS-485, so RS-485 transceivers are also RS-422 compliant. RS-422 is a point-to-multipoint (multidrop) standard, which allows only one driver and up to 10 (assuming one unit load devices) receivers on each bus. RS-485 is a true multipoint standard, which allows up to 32 one unit load devices (any combination of drivers and receivers) on each bus. To allow for multipoint operation, the RS-485 spec requires that drivers must handle bus contention without sustaining any damage.

Another important advantage of RS-485 is the extended common mode range (CMR), which specifies that the driver outputs and receiver inputs withstand signals that range from +12V to -7V. RS-422 and RS-485 are intended for runs as long as 4000', so the wide CMR is necessary to handle ground potential differences, as well as voltages induced in the cable by external fields.

Receiver Features

These devices utilize a differential input receiver for maximum noise immunity and common mode rejection. Input sensitivity is ±200mV, as required by the RS-422 and RS-485 specifications.

Receiver input resistance of 96kΩ surpasses the RS-422 spec of 4kΩ, and is eight times the RS-485 "Unit Load (UL)" requirement of 12kΩ minimum. Thus, these products are known as "one-eighth UL" transceivers, and there can be up to 256 of these devices on a network while still complying with the RS-485 loading spec.

Receiver inputs function with common mode voltages as great as ±7V outside the power supplies (i.e., +12V and -7V), making them ideal for long networks where induced voltages are a realistic concern.

All the receivers include a "fail-safe if open" function that guarantees a high level receiver output if the receiver inputs are unconnected (floating).

Receivers easily meet the data rates supported by the corresponding driver, and receiver outputs are three-statable via the active low $\overline{RE}$ input.

Driver Features

The RS-485 and RS-422 driver is a differential output device that delivers at least 1.5V across a 54Ω load (RS-485), and at least 2V across a 100Ω load (RS-422). The drivers feature low propagation delay skew to maximize bit width, and to minimize EMI.

Driver outputs are three-statable via the active high DE input.

The ISL8487 and ISL81483 driver outputs are slew rate limited to minimize EMI, and to minimize reflections in unterminated or improperly terminated networks. Data rate on these slew rate limited versions is a maximum of 250kbps. ISL81487 drivers are not limited, so faster output transition times allow data rates of at least 5Mbps.

Data Rate, Cables, and Terminations

RS-485 and RS-422 are intended for network lengths up to 4000', but the maximum system data rate decreases as the transmission length increases. Devices operating at 5Mbps are limited to lengths less than a few hundred feet, while the

250kbps versions can operate at full data rates with lengths in excess of 1000’.

Twisted pair is the cable of choice for RS-485/RS-422 networks. Twisted pair cables tend to pick up noise and other electromagnetically induced voltages as common mode signals, which are effectively rejected by the differential receivers in these ICs.

To minimize reflections, proper termination is imperative when using the 5Mbps device. Short networks using the 250kbps versions need not be terminated, but, terminations are recommended unless power dissipation is an overriding concern.

In point-to-point, or point-to-multipoint (single driver on bus) networks, the main cable should be terminated in its characteristic impedance (typically 120Ω) at the end farthest from the driver. In multi-receiver applications, stubs connecting receivers to the main cable should be kept as short as possible. Multipoint (multi-driver) systems require that the main cable be terminated in its characteristic impedance at both ends. Stubs connecting a transceiver to the main cable should be kept as short as possible.

Built-In Driver Overload Protection

As stated previously, the RS-485 spec requires that drivers survive worst case bus contentions undamaged. These devices meet this requirement via driver output short circuit current limits, and on-chip thermal shutdown circuitry.

The driver output stages incorporate short circuit current limiting circuitry which ensures that the output current never exceeds the RS-485 spec, even at the common mode voltage range extremes. Additionally, these devices utilize a foldback circuit which reduces the short circuit current, and thus the power dissipation, whenever the contending voltage exceeds either supply.

In the event of a major short circuit condition, these devices also include a thermal shutdown feature that disables the drivers whenever the die temperature becomes excessive. This eliminates the power dissipation, allowing the die to cool. The drivers automatically re-enable after the die temperature drops about 15 degrees. If the contention persists, the thermal shutdown/re-enable cycle repeats until the fault is cleared. Receivers stay operational during thermal shutdown.

Low Power Shutdown Mode (Excluding ISL81487)

These CMOS transceivers all use a fraction of the power required by their bipolar counterparts, but the ISL8487 and ISL81483 include a shutdown feature that reduces the already low quiescent I_{CC} to a 500nA trickle. They enter shutdown whenever the receiver and driver are ***simultaneously*** disabled ($\overline{RE}$ = V_{CC} and DE = GND) for a period of at least 600ns. Disabling both the driver and the receiver for less than 50ns guarantees that shutdown is not entered.

Note that receiver and driver enable times increase when enabling from shutdown. Refer to Notes 5-9, at the end of the Electrical Specification table, for more information.

Typical Performance Curves V_{CC} = 5V, T_A = 25°C, ISL8487, ISL81483 and ISL81487; Unless Otherwise Specified

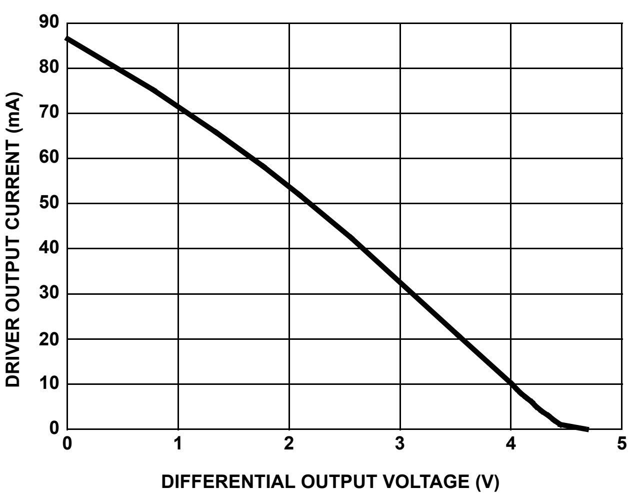


FIGURE 6. DRIVER OUTPUT CURRENT vs DIFFERENTIAL OUTPUT VOLTAGE

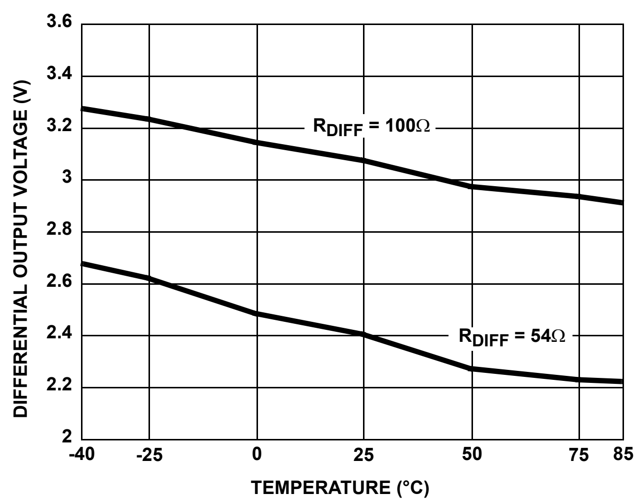


FIGURE 7. DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs TEMPERATURE

Typical Performance Curves V_{CC} = 5V, T_A = 25°C, ISL8487, ISL81483 and ISL81487; Unless Otherwise Specified **(Continued)**

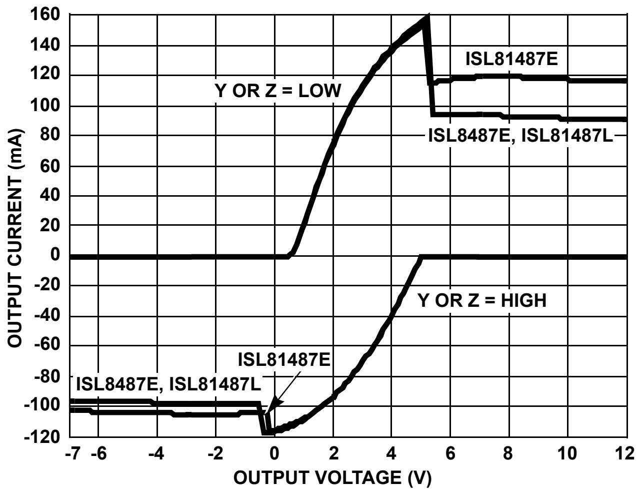


FIGURE 8. DRIVER OUTPUT CURRENT vs SHORT CIRCUIT VOLTAGE

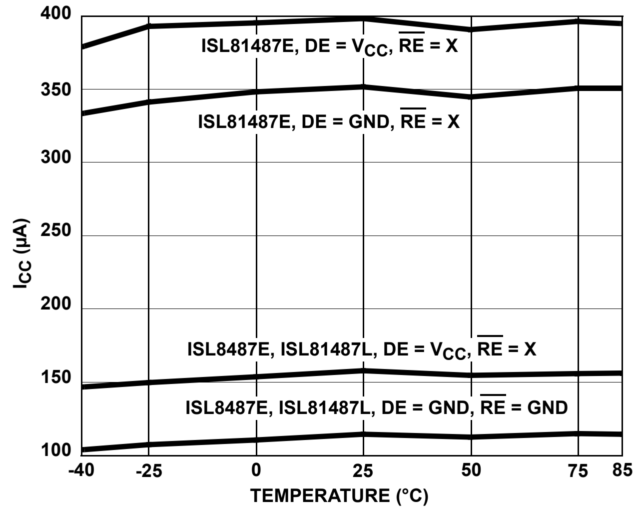


FIGURE 9. SUPPLY CURRENT vs TEMPERATURE

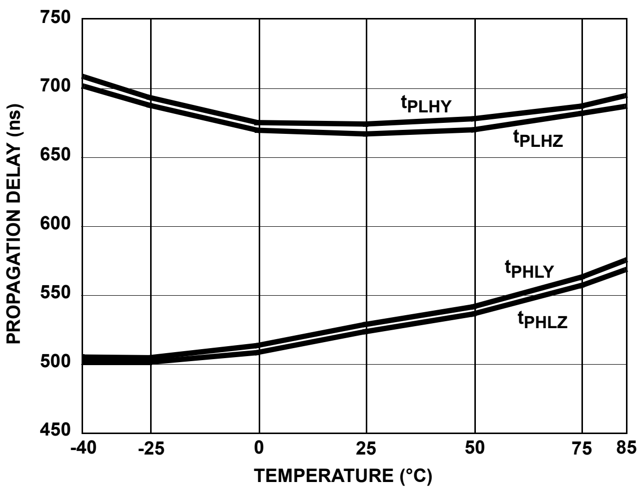


FIGURE 10. DRIVER PROPAGATION DELAY vs TEMPERATURE (ISL8487, ISL81483)

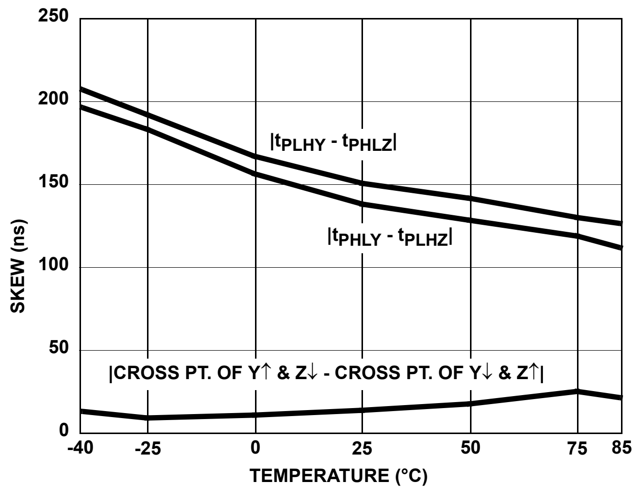


FIGURE 11. DRIVER SKEW vs TEMPERATURE (ISL8487, ISL81483)

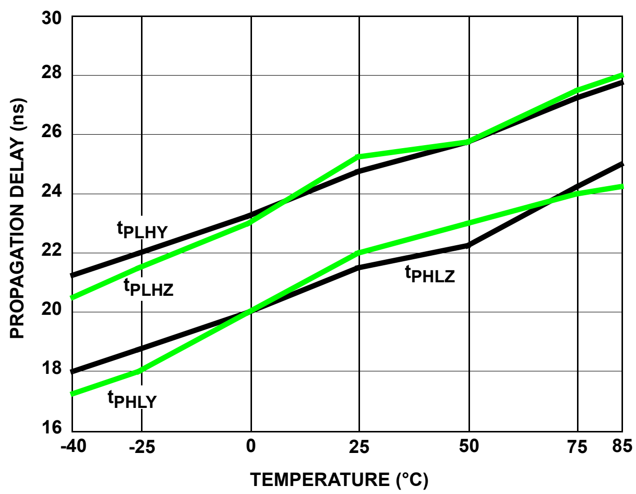


FIGURE 12. DRIVER PROPAGATION DELAY vs TEMPERATURE (ISL81487)

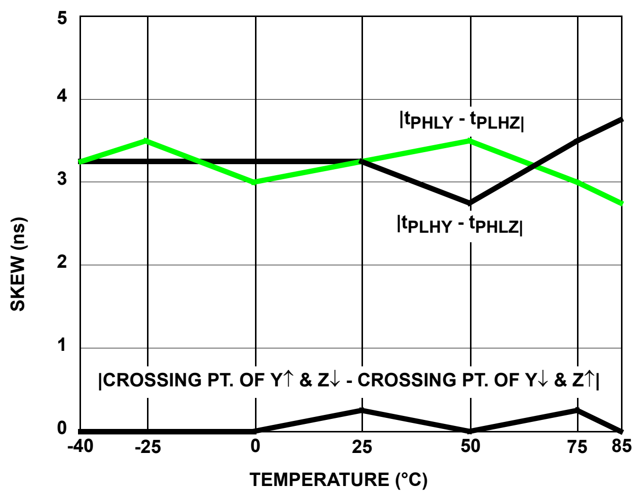


FIGURE 13. DRIVER SKEW vs TEMPERATURE (ISL81487)

Typical Performance Curves V_{CC} = 5V, T_A = 25°C, ISL8487, ISL81483 and ISL81487; Unless Otherwise Specified **(Continued)**

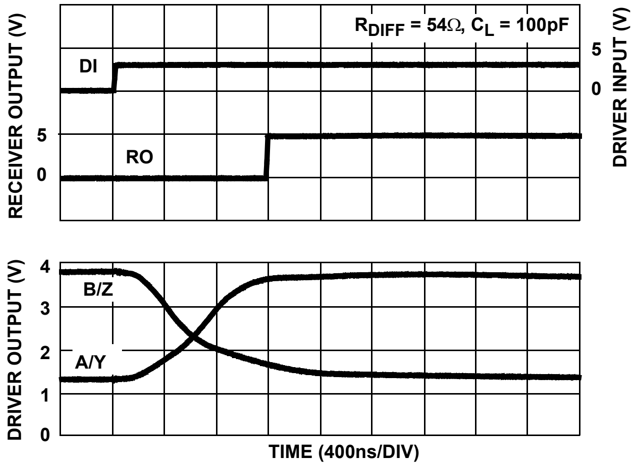


FIGURE 14. DRIVER AND RECEIVER WAVEFORMS, LOW TO HIGH (ISL8487, ISL81483)

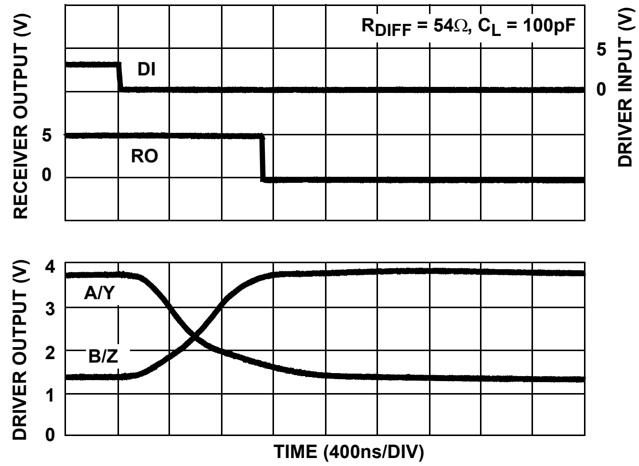


FIGURE 15. DRIVER AND RECEIVER WAVEFORMS, HIGH TO LOW (ISL8487, ISL81483)

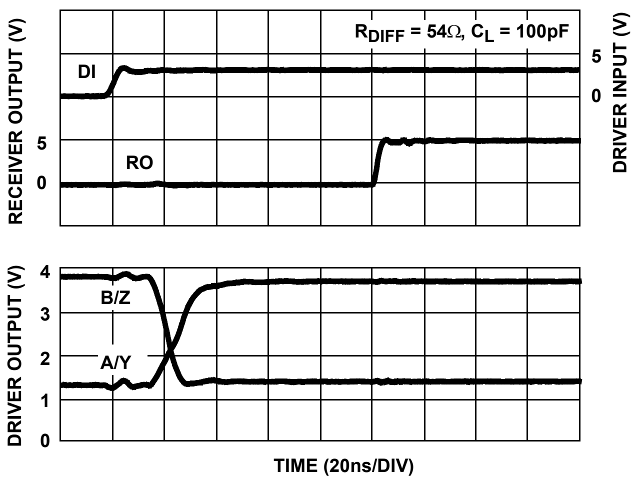


FIGURE 16. DRIVER AND RECEIVER WAVEFORMS, LOW TO HIGH (ISL81487)

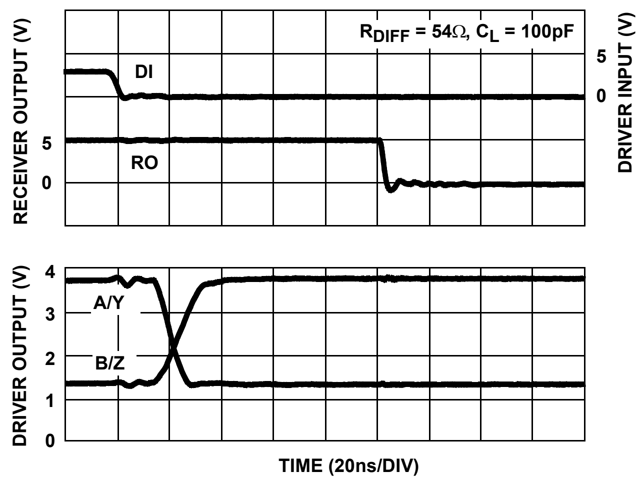


FIGURE 17. DRIVER AND RECEIVER WAVEFORMS, HIGH TO LOW (ISL81487)

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

518

PROCESS:

Si Gate CMOS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
March 14, 2016	FN6050.8	Added Rev History and About Intersil Verbiage. Updated “Ordering Information” table on page 2. Updated M8.15 to current revision. POD revision changes are as follows: Note 1 "1982" to "1994 Changed in Typical Recommended Land Pattern the following: 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205) Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern.

About Intersil

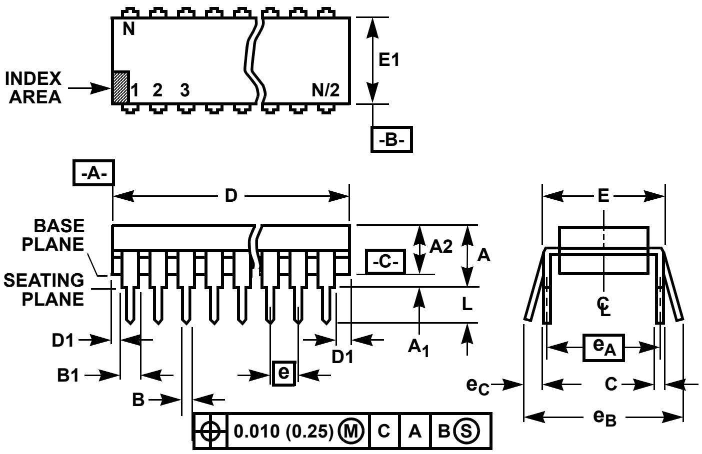
Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

Dual-In-Line Plastic Packages (PDIP)



E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C- .
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).