RENESAS

Demonstration Board

The ISL81801DEMO1Z demonstration board (shown in [Figure 8\)](#page-6-0) features the [ISL81801](http://www.renesas.com/products/isl81801), a 80V high voltage synchronous buck-boost controller that provides external soft-start, independent enable functions, and integrates UV/OV/OC/OT protection. Programmable switching frequency ranging from 100kHz to 600kHz helps to optimize the inductor size while the strong gate driver delivers up to 20A for the buck-boost output.

Key Features

- Wide input range: 32V to 80V
- Bidirectional operation
- High light-load efficiency in pulse skipping DEM operation
- Programmable soft-start
- Optional DEM/PWM operation
- Optional CC/HICCUP OCP protection
- Supports prebias output with soft-start
- PGOOD indicator
- OVP, OTP, and UVP protection
- Parallelable operation

Specifications

The ISL81801DEMO1Z demonstration board is designed for high current applications. The current rating of the ISL81801DEMO1Z is limited by the FETs and inductor selected. The ISL81801DEMO1Z electrical ratings are shown in [Table 1.](#page-0-0)

Table 1. Electrical Ratings

Ordering Information

Related Literature

For a full list of related documents, visit our website:

• **ISL81801** product page

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Figure 1. ISL81801DEMO1Z Block Diagram

1. Functional Description

The ISL81801DEMO1Z demonstrates the performance of the ISL81801 TQFN IC. The board provides an easy and complete demonstration of all the IC and board functions.

As shown in [Figure 7,](#page-4-0) 32V to 80V V_{IN} is supplied to J₁ (+) and J₂ (-). The regulated 48V output on J₄ (+) and J₅ (-) can supply up to 10A to the load. Because of the high power efficiency, the demonstration board can run at 5A continuously without airflow at room temperature ambient conditions.

Test points TP_1 through TP_{28} provide easy access to the IC pin and external signal injection terminals.

As shown in **[Figure 3](#page-4-1)**, connector J₈ provides selection of either Forced PWM mode (shorting Pin 1 and Pin 2) or DEM mode (shorting Pin 2 and Pin 3). Connector J_9 provides selection of either constant current limit (shorting Pin 1 and Pin 2) or HICCUP OCP (shorting Pin 2 and Pin 3). Connector J_3 provides an option to disable the converter by shorting its Pin 1 and Pin 2.

1.1 Recommended Testing Equipment

The following materials are recommended for testing:

- 0V to 80V power supply with at least 15A source current capability
- Electronic loads capable of sinking current up to 15A
- Digital Multimeters (DMMs)
- 100MHz quad-trace oscilloscope

1.2 Operating Range

The input voltage range is from 32V to 80V for an output voltage of 48V. If the output voltage is set to a lower value, the minimum V_{IN} can be reset to a lower value by changing the ratio of R₂ and R₃. The minimum EN threshold that V_{IN} can be set to is 4.5V.

The rated load current is 10A with the OCP point set at minimum 11A at ambient room temperature conditions. The operating temperature range of this board is from -40°C to +85°C.

Note: Airflow is needed for higher temperature ambient conditions.

1.3 Parallel Operation

The ISL81801DEMO1Z demonstration board can operate in parallel, in a daisy chain setup.

[Figure 2](#page-2-0) shows the wiring of two units in parallel and **[Figure 3](#page-2-1)** shows three units in parallel. The phase shift between the units are set by J_6 and J_7 . [Table 2](#page-3-0) shows the combination.

Figure 2. Setup for Two Units in Parallel Figure 3. Setup for Three Units in Parallel

Figure 4. Current Sharing Among Three Units

Total Load (A)

| | CLK Lag RT by $(°)$ FBI | 90 | 60 | 180 | 120 |
|-------|---|------------------|----------------|------------------------|------------------------|
| J_7 | | | | | |
| | | VC5(1) | VC5(1) | GND (Active) | GND (Active) |
| J_6 | IIN B | Open (Active) | Shorted (1) | Open (Active) | Shorted (1) |

1.4 Bidirectional Operation

See [Figure 5](#page-3-1) for proper setup. Float the FBI pin (J_7) and set the mode to PWM before powering on the board. The rated voltage of the super capacitor must be higher than 48V.

- 1. Adjust the input voltage higher than 36V. Switch on the input power source.
- 2. Switch off the input power source after the super capacitor is fully charged.

Figure 5. Proper Set-Up for Bidirectional Operation

1.5 Quick Test Guide

- 1. Jumper J₈ provides the option to select PWM or DEM. Jumper J₉ provides the option to select Constant current limit or HICCUP. See [Table 3](#page-4-1) for the operating options. Ensure that the circuit is correctly connected to the supply and electronic loads prior to applying any power. See **Figure 7** for proper setup.
- 2. Turn on the power supply.
- 3. Adjust input voltage V_{IN} within the specified range and observe the output voltage. The output voltage variation should be within 3%.
- 4. Adjust the load current within the specified range and observe the output voltage. The output voltage variation should be within 3%.
- 5. Use an oscilloscope to observe output voltage ripple and phase node ringing. For accurate measurement, see [Figure 6](#page-4-2) for proper test setup.

Table 3. Operating Options

Figure 6. Proper Probe Set-Up to Measure Output Ripple and Phase Node Ringing

Figure 7. Proper Test Setup

2. PCB Layout Guidelines

Careful attention to layout requirements is necessary for successful implementation of an ISL81801 based DC/DC converter. The ISL81801 switches at a high frequency; therefore the switching times are short. At these switching frequencies, even the shortest trace has significant impedance. The peak gate drive current also rises significantly in an extremely short time. Transition speed of the current from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, generate EMI, and increase device voltage stress and ringing. Careful component selection and proper PC board layout minimizes the magnitude of these voltage spikes.

Three sets of components are critical when using the ISL81801 DC/DC converter:

- Controller
- Switching power components
- Small signal components

The switching power components are the most critical to the layout because they switch a large amount of energy, which tends to generate a large amount of noise. The critical small signal components are those connected to sensitive nodes or those supplying critical bias currents. A multilayer printed circuit board is recommended.

Complete the following steps to optimize the PCB layout.

- 1. Place the input capacitors, buck FETs, inductor, boost FETs, and output capacitor first. Isolate these power components on dedicated areas of the board with their ground terminals adjacent to one another. Place the input and output high frequency decoupling ceramic capacitors close to the MOSFETs.
- 2. If signal components and the IC are placed separately from the power train, Renesas recommends using full ground planes in the internal layers with shared SGND and PGND to simplify the layout design. Otherwise, use separate ground planes for the power ground and the small signal ground. Connect the SGND and PGND together close to the IC. DO NOT connect them together anywhere else.
- 3. **Important:** Keep the loop formed by the input capacitor, the buck top FET, and the buck bottom FET as small as possible. Also, keep the loop formed by the output capacitor, the boost top FET, and the boost bottom FET as small as possible.
- 4. Ensure the current paths from the input capacitor to the buck FETs, the power inductor, the boost FETs, and the output capacitor are as short as possible with maximum allowable trace widths.
- 5. Place the PWM controller IC close to the lower FETs. The low-side FETs gate drive connections should be short and wide. Place the IC over a quiet ground area. Avoid switching ground loop currents in this area.
- 6. Place the VDD bypass capacitor close to the VDD pin of the IC and connect its ground end to the PGND pin. Connect the PGND pin to the ground plane by a via. **Note:** Do not connect the PGND pin directly to the SGND EPAD.
- 7. Place the gate drive components (BOOT diodes and BOOT capacitors) together near the controller IC.
- 8. Place the output capacitors as close to the load as possible. Use short, wide copper regions to connect output capacitors to the load to avoid inductance and resistance.
- 9. Use copper filled polygons or wide, short traces to connect the junction of the buck or boost upper FET, buck or boost lower FET, and output inductor. Keep the buck and boost PHASE nodes connection to the IC short. **Important:** DO NOT unnecessarily oversize the copper islands for the PHASE nodes. Because the phase nodes are subjected to high dv/dt voltages, the stray capacitor formed between these islands and the surrounding circuitry tend to couple switching noise.
- 10. Route all high speed switching nodes away from the control circuitry.
- 11. Create a separate small analog ground plane near the IC. Connect the SGND pin to this plane. Connect all small signal grounding paths including feedback resistors, current monitoring resistors and capacitors, soft-starting capacitors, loop compensation capacitors and resistors, and EN pull-down resistors to this SGND plane.

- 12. Use a pair of traces with minimum loop for the input or output current sensing connection.
- 13. Ensure the feedback connection to the output capacitor is short and direct.

2.1 ISL81801DEMO1Z Demonstration Board

Figure 8. ISL81801DEMO1Z Demonstration Board (Top)

Figure 9. ISL81801DEMO1Z Demonstration Board (Bottom)

2.3 Bill of Materials

2.4 Board Layout

Figure 11. Assembly Top

Figure 12. Top Layer

Figure 13. Layers 2 and 3 (Solid Ground), Identical

Figure 14. Bottom Layer

Figure 15. Assembly Bottom

3. Typical Performance Curves

 V_{1N} = 48V, R_{62} = 4.7k, unless otherwise noted.

Figure 20. DEM vs CCM at Light Load, V_{IN} = 60V

Figure 21. Input Port CV/CC Regulation (R₆₂ = 8.45k) Figure 22. Output Port CV/CC Regulation (48V, 11A)

Figure 26. Phase 1, Phase 2, V_{OUT} and Inductor Current, V_{IN} = 48V, I_{OUT} = 5A

V_{1N} = 48V, R_{62} = 4.7k, unless otherwise noted. **(Continued)**

Figure 28. Load Transient, V_{IN} = 36V, I_{OUT} = 0A to 5A **2.5A/µs, CCM**

Figure 29. Load Transient, V_{IN} = 48V, I_{OUT} = 0A to 5A **2.5A/µs, CCM**

Figure 30. Load Transient, V_{IN} = 80V, I_{OUT} = 0A to 5A **2.5A/µs, CCM**

V_{1N} = 48V, R_{62} = 4.7k, unless otherwise noted. **(Continued)**

Figure 33. Start-Up Waveform, V_{IN} = 80V, I_{OUT} = 5A, CCM Figure 34. Short-Circuit Waveform

Figure 37. Line Transient, V_{IN} = 80V to 36V, 1V/ms, I_{OUT} = 0A

4. Revision History

