# RENESAS

### ISL81802EVAL3Z

Evaluation Board

The ISL81802EVAL3Z 4-phase evaluation board (shown in [Figure 4\)](#page-5-0) features the [ISL81802](https://www.renesas.com/products/isl81802), a 80V high-voltage dual synchronous buck controller that offers external soft-start, independent enable functions, and integrates UV/OV/OC/OT protection. A programmable switching frequency ranging from 100kHz to 1MHz helps optimize inductor size while the strong gate driver delivers up to 40A for the buck output.

### **Key Features**

- Wide input range: 18V to 80V
- High light-load efficiency in pulse skipping DEM operation
- Programmable soft-start
- Optional DEM/PWM operation
- Optional CC/HICCUP OCP protection
- Supports pre-bias output with soft-start
- PGOOD indicator
- OVP, OTP, and UVP protection
- Back biased from output to improve efficiency

The ISL81802EVAL3Z 4-phase evaluation board is designed for high current applications. The current rating of the ISL81802EVAL3Z is limited by the FETs and inductor selected. The ISL81802EVAL3Z electrical ratings are shown in [Table 1.](#page-0-0)

#### <span id="page-0-0"></span>**Table 1. Electrical Rating**



### **Ordering Information**



#### **Related Literature**

For a full list of related documents, visit our website:

• [ISL81802](https://www.renesas.com/products/isl81802) device page





**Figure 1. ISL81802EVAL3Z Block Diagram**



### **1. Functional Description**

The ISL81802EVAL3Z is the same test board used by Renesas application engineers and IC designers to evaluate the performance of the ISL81802 HTSSOP IC. The board provides an easy and complete evaluation of all the IC and board functions.

As shown in **[Figure 2](#page-3-0)**, 18V to 80V VIN is supplied to J1/J13 (+) and J2/J14 (-). The regulated 12V output on J4/J10 (+) and J5/J11 (-) can supply up to 40A to the load. Because of the high power efficiency, the evaluation board can run at 40A continuously without airflow at room temperature ambient conditions.

Test points TP1 through TP36 provide easy access to the IC pin and external signal injection terminals.

As shown in **[Table 2](#page-2-0)**, connectors J6 and J8 provide a selection of either Forced PWM mode (shorting Pin 1 and Pin 2) or DEM mode (shorting Pin 2 and Pin 3). Connectors J7 and J12 provide a selection of either constant current limit (shorting Pin 1 and Pin 2) or HICCUP OCP (shorting Pin 2 and Pin 3). Connectors J3 and J9 provide an option to disable the converter by shorting its Pin 1 and Pin 2.

#### **1.1 Recommended Testing Equipment**

The following materials are recommended for testing:

- 0V to 80V power supply with at least 40A source current capability
- Electronic loads capable of sinking current up to 50A
- Digital Multimeters (DMMs)
- 100MHz quad-trace oscilloscope

#### **1.2 Operating Range**

The input voltage range is from 18V to 80V for an output voltage of 12V. If the output voltage is set to a lower value, the minimum V<sub>IN</sub> can be reset to a lower value by changing both the ratio of R<sub>1</sub> and R<sub>5</sub>, and the ratio of R<sub>58</sub> and  $R_{63}$ . The minimum EN threshold that  $V_{IN}$  can be set to is 4.5V.

The rated load current is 40A with the OCP point set at minimum 44A at ambient room temperature conditions. The operating temperature range of this board is -40°C to +85°C.

**Note:** Airflow is needed for higher temperature ambient conditions.

#### **1.3 Quick Test Guide**

1. Jumper J6 provides the option to select PWM or DEM. Jumper J7 provides the option to select constant current limit or HICCUP. See [Table 2](#page-2-0) for the operating options. Ensure that the circuit is correctly connected to the supply and electronic loads before applying any power. See **[Figure 2](#page-3-0)** for proper setup.



#### <span id="page-2-0"></span>**Table 2. Operating Options**





**Figure 2. Proper Test Setup**

- <span id="page-3-0"></span>2. Turn on the power supply.
- 3. Adjust the input voltage ( $V_{IN}$ ) within the specified range and observe the output voltage. The output voltage variation should be within 3%.
- 4. Adjust the load current within the specified range and observe the output voltage. The output voltage variation should be within 3%.
- 5. Use an oscilloscope to observe output voltage ripple and phase node ringing. For accurate measurement, see [Figure 3](#page-3-1) for proper test setup.



<span id="page-3-1"></span>**Figure 3. Proper Probe Setup to Measure Output Ripple and Phase Node Ringing**



### **2. PCB Layout Guidelines**

Careful attention to Printed Circuit Board (PCB) layout requirements is necessary for successful implementation of an ISL81802 based DC/DC converter. The ISL81802 switches at a high frequency; therefore, the switching times are short. At these switching frequencies, even the shortest trace has significant impedance and the peak gate drive current rises significantly in an extremely short time. The transition speed of the current from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, generate EMI, and increase device voltage stress and ringing. Careful component selection and proper PCB layout minimizes the magnitude of these voltage spikes.

The following are critical components

when using the ISL81802 DC/DC converter:

- Controller
- Switching power components
- Small-signal components

The switching power components are the most critical to the layout because they switch a large amount of energy that tend to generate a large amount of noise. The critical small-signal components are those connected to sensitive nodes or those supplying critical bias currents. A multilayer PCB is recommended.

Complete the following steps to optimize the PCB layout.

- 1. Place the input capacitors, FETs, inductor, and output capacitor first. Isolate these power components on dedicated areas of the board with their ground terminals adjacent to one another. Place the input and output high frequency decoupling ceramic capacitors close to the MOSFETs.
- 2. If signal components and the IC are placed separately from the power train, Renesas recommends using full ground planes in the internal layers with shared SGND and PGND to simplify the layout design. Otherwise, use separate ground planes for the power ground and the small signal ground. Connect the SGND and PGND together close to the IC. **Note: DO NOT** connect them together anywhere else.
- 3. Keep the loop formed by the input capacitor, the top FET, and the bottom FET as small as possible.
- 4. Ensure the current paths from the input capacitor to the FETs, the power inductor, and the output capacitor are as short as possible with maximum allowable trace widths.
- 5. Place the PWM controller IC close to the lower FETs. The low-side FETs gate drive connections should be short and wide. Place the IC over a quiet ground area. Avoid switching ground loop currents in this area.
- 6. Place the VDD bypass capacitor close to the VDD pin of the IC and connect its ground end to the PGND pin. Connect the PGND pin to the ground plane by a via. **Note: DO NOT** connect the PGND pin directly to the SGND EPAD.
- 7. Place the gate drive components (BOOT diodes and BOOT capacitors) together near the controller IC.
- 8. Place the output capacitors as close to the load as possible. To avoid inductance and resistances, use short, wide copper regions to connect output capacitors to load.
- 9. Use copper filled polygons or wide, short traces to connect the junction of the upper FET, lower FET, and output inductor. Keep the PHASE nodes connection to the IC short. **Note: DO NOT** unnecessarily oversize the copper islands for the PHASE nodes. Because the phase nodes are subjected to extreme dv/dt voltages, the stray capacitor formed between these islands and the surrounding circuitry tends to couple switching noise.
- 10. Route all high-speed switching nodes away from the control circuitry.
- 11. Create a separate small analog ground plane near the IC. Connect the SGND pin to this plane. Connect all small signal grounding paths including feedback resistors, current monitoring resistors and capacitors, soft-starting capacitors, loop compensation capacitors and resistors, and EN pull-down resistors to this SGND plane.
- 12. Use a pair of traces with minimum loop for the input or output current sensing connection.
- 13. Ensure the feedback connection to the output capacitor is short and direct.



### **2.1 ISL81802EVAL3Z Evaluation Board**



<span id="page-5-0"></span>**Figure 4. ISL81802EVAL3Z Evaluation Board, Top View**





**Figure 5. ISL81802EVAL3Z Evaluation Board, Bottom View**





**Figure 6. Schematic (1/3)**









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### **2.3 Bill of Materials**









#### **2.4 Board Layout**



**Figure 9. Silkscreen Top**



**Figure 10. Top Layer**





**Figure 11. Second Layer (Solid Ground)**



**Figure 12. Third Layer**





**Figure 13. Bottom Layer**



**Figure 14. Silkscreen Bottom**



### **3. Typical Performance Curves**

 $V_{IN}$  = 48V, T<sub>A</sub> = 25°C, unless otherwise noted.





**Figure 17. Inductor Current I<sub>L1</sub>, I<sub>L2</sub>, I<sub>L3</sub>, I<sub>L4</sub>, V<sub>IN</sub> = 18V,**  $I_{OUT} = 40A$ 



**Figure 19. Inductor Current I<sub>L1</sub>, I<sub>L2</sub>, I<sub>L3</sub>, I<sub>L4</sub>, V<sub>IN</sub> = 80V,**  $I_{OUT} = 40A$ 



Figure 15. Load Current Sharing, V<sub>IN</sub> = 48V, CCM Figure 16. Output Voltage Ripple, V<sub>IN</sub> = 48V, I<sub>OUT</sub> = 40A, **CCM**



**Figure 18. Inductor Current I<sub>L1</sub>, I<sub>L2</sub>, I<sub>L3</sub>, I<sub>L4</sub>, V<sub>IN</sub> = 48V,**  $I_{OUT} = 40A$ 



Figure 20. Load Transient,  $V_{IN}$  = 18V,  $I_{OUT}$  = 0A to 40A, **2.5A/µs, CCM**







Figure 21. Load Transient,  $V_{IN}$  = 48V,  $I_{OUT}$  = 0A to 40A, **2.5A/µs, CCM**



Figure 22. Load Transient, V<sub>IN</sub> = 80V, I<sub>OUT</sub> = 0A to 40A, **2.5A/µs, CCM**





Figure 23. Start-Up Waveform, V<sub>IN</sub> = 18V, I<sub>OUT</sub> = 40A, CCM Figure 24. Start-Up Waveform, V<sub>IN</sub> = 48V, I<sub>OUT</sub> = 40A, CCM



Figure 25. Start-Up Waveform, V<sub>IN</sub> = 80V, I<sub>OUT</sub> = 40A, CCM Figure 26. Phase1, Phase2, Phase3, Phase4, V<sub>IN</sub> = 18V,  $I_{OUT} = 40A$ , CCM **2µs/Div**

20.0 V & 20.0 V & 30.0 V & 30 20.0 V & 3 20.0 V & 3  $(2.00 \text{µs})$ 

**Phase1 20V/Div**

Tek Prevu

**Phase2 20V/Div**

**Phase3 20V/Div**

**Phase4 20V/Div**

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 $\frac{2.50GS/s}{1M \text{ points}}$ 

#### $V_{IN}$  = 48V,  $T_A$  = 25°C, unless otherwise noted. **(Continued)**







Figure 28. Phase1, Phase2, Phase3, Phase4, V<sub>IN</sub> = 80V,  $I_{OUT} = 40A$ , CCM



## **4. Revision History**



