ISL83483, ISL83485, ISL83488, ISL83490, ISL83491

3.3V, Low Power, High Speed or Slew Rate Limited, RS-485/RS-422 Transceivers

FN6052
Rev.5.00
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These Renesas RS-485/RS-422 devices are BiCMOS 3.3V powered, single transceivers that meet both the RS-485 and RS-422 standards for balanced communication. Unlike competitive devices, this Renesas family is specified for 10% tolerance supplies (3V to 3.6V).

The ISL83483 and ISL83488 use slew rate limited drivers which reduce EMI, and minimize reflections from improperly terminated transmission lines, or unterminated stubs in multidrop and multipoint applications.

Data rates up to 10Mbps are achievable by using the ISL83485, ISL83490, or ISL83491, which feature higher slew rates.

Logic inputs (for example, DI and DE) accept signals in excess of 5.5V, making them compatible with 5V logic families.

Receiver (Rx) inputs feature a “fail-safe if open” design, which ensures a logic high output if Rx inputs are floating. All devices present a “single unit load” to the RS-485 bus, which allows up to 32 transceivers on the network.

Driver (Tx) outputs are short-circuit protected, even for voltages exceeding the power supply voltage. Additionally, on-chip thermal shutdown circuitry disables the Tx outputs to prevent damage if power dissipation becomes excessive.

The ISL83488, ISL83490, and ISL83491 are configured for full duplex (separate Rx input and Tx output pins) applications. The ISL83488 and ISL83490 are offered in space saving 8 Ld packages for applications not requiring Rx and Tx output disable functions (for example, point-to-point and RS-422). Half duplex configurations (ISL83483, ISL83485) multiplex the Rx inputs and Tx outputs to provide transceivers with Rx and Tx disable functions in 8 Ld packages.

Features

- Operate from a single +3.3V supply (10% tolerance)
- Interoperable with 5V logic
- High data rates. . . . . up to 10Mbps
- Single unit load allows up to 32 devices on the bus
- Slew rate limited versions for error free data transmission (ISL83483, ISL83488) . . . . . .up to 250kbps
- Low current Shutdown mode (ISL83483, ISL83485, ISL83491). 15nA
- -7V to +12V common-mode input voltage range
- Three-state Rx and Tx outputs (except ISL83488, ISL83490)
- 10ns propagation delay, 1ns skew (ISL83485, ISL83490, ISL83491)
- Full duplex and half duplex pinouts
- Current limiting and thermal shutdown for driver overload protection
- Pb-free (RoHS compliant)

Applications

- Factory automation
- Security networks
- Building environmental control systems
- Industrial/process control networks
- Level translators (for example, RS-232 to RS-422)
- RS-232 “Extension Cords”

Related Literature

For a full list of related documents, visit our website:

- ISL83483, ISL83485, ISL83488, ISL83490, ISL83491 device pages

TABLE 1. SUMMARY OF FEATURES

PART NUMBER	HALF/FULL DUPLEX	DATA RATE (Mbps)	SLEW-RATE LIMITED?	RECEIVER/DRIVER ENABLE?	QUIESCENT I_{CC} (mA)	LOW POWER SHUTDOWN?	PIN COUNT
ISL83483	Half	0.25	Yes	Yes	0.65	Yes	8
ISL83485	Half	10	No	Yes	0.65	Yes	8
ISL83488	Full	0.25	Yes	No	0.65	No	8
ISL83490	Full	10	No	No	0.65	No	8
ISL83491	Full	10	No	Yes	0.65	Yes	14

Ordering Information

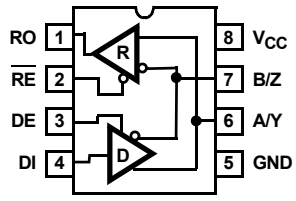
PART NUMBER (Notes 2, 3)	PART MARKING	TEMP. RANGE (°C)	TAPE AND REEL (UNITS) (Note 1)	PACKAGE	PKG. DWG. #
ISL83483IBZ	83483 IBZ	-40 to +85	-	8 Ld SOIC (RoHS compliant)	M8.15
ISL83483IBZ-T	83483 IBZ	-40 to +85	2.5k	8 Ld SOIC (RoHS compliant)	M8.15
ISL83483IBZ-T7A	83483 IBZ	-40 to +85	250	8 Ld SOIC (RoHS compliant)	M8.15
ISL83483IP (No longer available or supported)	ISL 83483IP	-40 to +85	-	8 Ld PDIP	E8.3
ISL83485IBZ	83485 IBZ	-40 to +85	-	8 Ld SOIC (RoHS compliant)	M8.15
ISL83485IBZ-T	83485 IBZ	-40 to +85	2.5k	8 Ld SOIC (RoHS compliant)	M8.15
ISL83485IBZ-T7A	83485 IBZ	-40 to +85	250	8 Ld SOIC (RoHS compliant)	M8.15
ISL83488IBZ	83488 IBZ	-40 to +85	-	8 Ld SOIC (RoHS compliant)	M8.15
ISL83488IBZ-T	83488 IBZ	-40 to +85	2.5k	8 Ld SOIC (RoHS compliant)	M8.15
ISL83490IBZ	83490 IBZ	-40 to +85	-	8 Ld SOIC (RoHS compliant)	M8.15
ISL83490IBZ-T	83490 IBZ	-40 to +85	2.5k	8 Ld SOIC (RoHS compliant)	M8.15
ISL83491IBZ	83491IBZ	-40 to +85	-	14 Ld SOIC (RoHS compliant)	M14.15
ISL83491IBZ-T	83491IBZ	-40 to +85	2.5k	14 Ld SOIC (RoHS compliant)	M14.15
ISL83491IBZ-T7A	83491IBZ	-40 to +85	250	14 Ld SOIC (RoHS compliant)	M14.15
ISL83491IP (No longer available, recommended replacement: ISL83491IBZ)	ISL83491IP	-40 to +85	-	14 Ld PDIP	E14.3

NOTES:

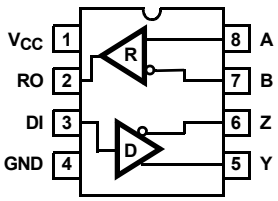
1. Refer to TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), refer to the ISL83483, ISL83485, ISL83488, ISL83490, and ISL83491 device pages. For more information about MSL, refer to TB363.

Pinouts

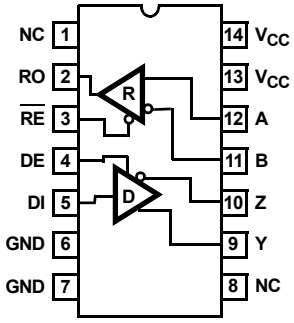
ISL83483, ISL83485 (PDIP, SOIC)
TOP VIEW



ISL83488, ISL83490 (SOIC)
TOP VIEW



ISL83491 (PDIP, SOIC)
TOP VIEW



NOTE: PDIP packages are no longer supported

Truth Tables

TRANSMITTING				
INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	Z	Y
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	High-Z *	High-Z *

NOTE: *Shutdown Mode for ISL83483, ISL83485, ISL83491

RECEIVING				
INPUTS				OUTPUT
$\overline{RE}$	DE Half Duplex	DE Full Duplex	A-B	RO
0	0	X	≥ +0.2V	1
0	0	X	≤ -0.2V	0
0	0	X	Inputs Open	1
1	0	0	X	High-Z *
1	1	1	X	High-Z

NOTE: *Shutdown Mode for ISL83483, ISL83485, ISL83491

Pin Descriptions

PIN	FUNCTION
RO	Receiver output: If A > B by at least 0.2V, RO is high; If A < B by 0.2V or more, RO is low; RO = High if A and B are unconnected (floating).
$\overline{RE}$	Receiver output enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high.
DE	Driver output enable. The driver outputs, Y and Z, are enabled by bringing DE high. They are high impedance when DE is low.
DI	Driver input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
GND	Ground connection.
A/Y	Noninverting receiver input and noninverting driver output. Pin is an input if DE = 0; pin is an output if DE = 1.
B/Z	Inverting receiver input and inverting driver output. Pin is an input if DE = 0; pin is an output if DE = 1.
A	Noninverting receiver input.
B	Inverting receiver input.
Y	Noninverting driver output.
Z	Inverting driver output.
V_{CC}	System power supply input (3V to 3.6V).
NC	No Connection.

Typical Operating Circuits

For calculating the resistor values refer to TB509, “Detecting Bus Signals Correctly with Failsafe Biased RS-485 Receivers”

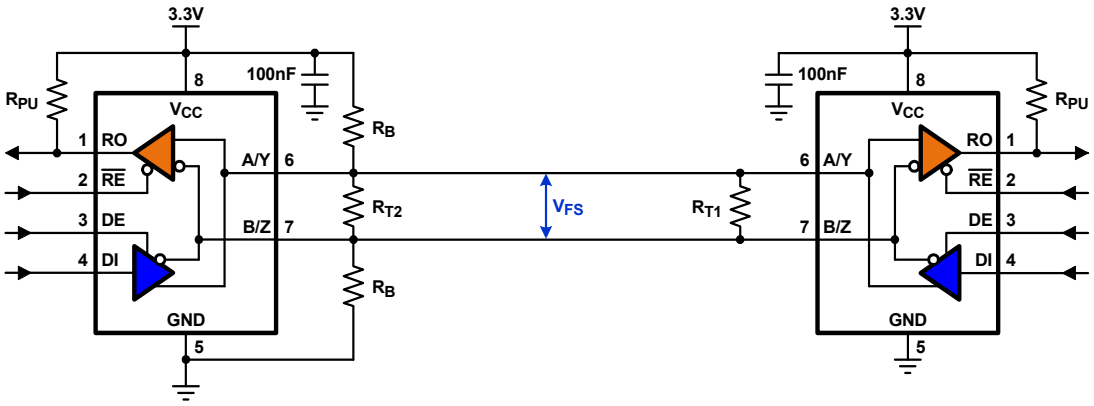


FIGURE 1. ISL83483, ISL83485

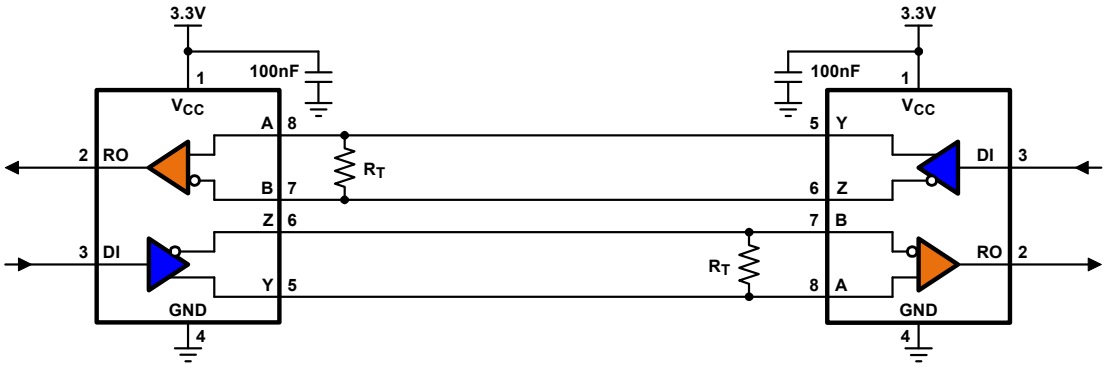


FIGURE 2. ISL83488, ISL83490

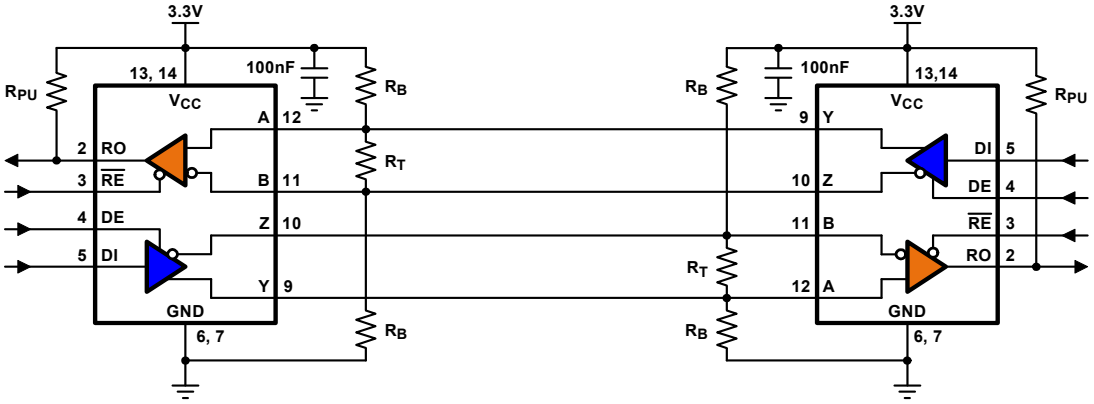


FIGURE 3. ISL83491

Absolute Maximum Ratings

V_{CC} to Ground 7V
Input Voltages
DI, DE, $\overline{RE}$ . . . . . -0.5V to +7V
Input/Output Voltages
A, B, Y, Z . . . . . -8V to +12.5V
RO . . . . . -0.5V to (V_{CC} +0.5V)
Short-Circuit Duration
Y, Z . . . . . Continuous

Operating Conditions

Temperature Range
ISL834xxIx . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} (°C/W)
8 Ld SOIC Package	170
8 Ld PDIP Package*	140
14 Ld SOIC Package	130
14 Ld PDIP Package*	105

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile (SOIC only) . . . . . see TB493

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" can cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

4. θ_{JA} is measured with the component mounted on a low-effective thermal conductivity test board in free air. See TB379.

Electrical Specifications

Test conditions: V_{CC} = 3V to 3.6V; unless otherwise specified. Typicals are at V_{CC} = 3.3V, T_A = +25°C, Note 5.

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN	TYP	MAX	UNIT
DC CHARACTERISTICS								
Driver Differential V_{OUT} (no load)	V_{OD1}			Full	-	-	V_{CC}	V
Driver Differential V_{OUT} (with load)	V_{OD2}	R_L = 100Ω (RS-422) (Figure 4A)		Full	2	2.7	-	V
		R_L = 54Ω (RS-485) (Figure 4A)		Full	1.5	2.3	V_{CC}	V
		R_L = 60Ω, -7V ≤ V_{CM} ≤ 12V (Figure 4B)		Full	1.5	2.6	-	V
Change in Magnitude of Driver Differential V_{OUT} for Complementary Output States	ΔV_{OD}	R_L = 54Ω or 100Ω (Figure 4A)		Full	-	0.01	0.2	V
Driver Common-Mode V_{OUT}	V_{OC}	R_L = 54Ω or 100Ω (Figure 4A)		Full	-	1.8	3	V
Change in Magnitude of Driver Common-Mode V_{OUT} for Complementary Output States	ΔV_{OC}	R_L = 54Ω or 100Ω (Figure 4A)		Full	-	0.01	0.2	V
Logic Input High Voltage	V_{IH}	DE, DI, $\overline{RE}$		Full	2	-	-	V
Logic Input Low Voltage	V_{IL}	DE, DI, $\overline{RE}$		Full	-	-	0.8	V
Logic Input Current	I_{IN1}	DE, DI		Full	-2	-	2	µA
		$\overline{RE}$		Full	-25	-	25	µA
Input Current (A, B)	I_{IN2}	DE = 0V, V_{CC} = 0V or 3.6V	V_{IN} = 12V	Full	-	0.6	1	mA
			V_{IN} = -7V	Full	-	-0.3	-0.8	mA
Output Leakage Current (Y, Z) (ISL83491)	I_{IN3}	$\overline{RE}$ = 0V, DE = 0V, V_{CC} = 0V or 3.6V	V_{IN} = 12V	Full	-	14	20	µA
			V_{IN} = -7V	Full	-20	-11	-	µA
Output Leakage Current (Y, Z) in Shutdown Mode (ISL83491)	I_{IN3}	$\overline{RE}$ = V_{CC}, DE = 0V, V_{CC} = 0V or 3.6V	V_{IN} = 12V	Full	-	0.03	1	µA
			V_{IN} = -7V	Full	-1	-0.01	-	µA
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ 12V		Full	-0.2	-	0.2	V
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V		+25	-	50	-	mV
Receiver Output High Voltage	V_{OH}	I_O = -4mA, V_{ID} = 200mV		Full	V_{CC} - 0.4	-	-	V
Receiver Output Low Voltage	V_{OL}	I_O = -4mA, V_{ID} = 200mV		Full	-	-	0.4	V

Electrical Specifications Test conditions: V_{CC} = 3V to 3.6V; unless otherwise specified. Typicals are at V_{CC} = 3.3V, T_A = +25°C, Note 5. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN	TYP	MAX	UNIT
Three-State (high impedance) Receiver Output Current	I_{OZR}	0.4V ≤ V_O ≤ 2.4V		Full	-1	-	1	µA
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V		Full	12	19	-	kΩ
No-Load Supply Current (Note 6)	I_{CC}	DI = 0V or V_{CC}	$\overline{DE}$ = V_{CC}, $\overline{RE}$ = 0V or V_{CC}	Full	-	0.75	1.2	mA
			$\overline{DE}$ = 0V, $\overline{RE}$ = 0V	Full	-	0.65	1	mA
Shutdown Supply Current (Except ISL83488 and ISL83490)	I_{SHDN}	DE = 0V, $\overline{RE}$ = V_{CC}, DI = 0V or V_{CC}		Full	-	15	100	nA
Driver Short-Circuit Current, V_O = High or Low	I_{OSD1}	DE = V_{CC}, -7V ≤ V_Y or V_Z ≤ 12V (Note 7)		Full	-	-	250	mA
Receiver Short-Circuit Current	I_{OSR}	0V ≤ V_O ≤ V_{CC}		Full	8	-	60	mA
DRIVER SWITCHING CHARACTERISTICS (ISL83485, ISL83490, ISL83491)								
Maximum Data Rate	f_{MAX}			Full	12	15	-	Mbps
Driver Differential Output Delay	t_{DD}	R_{DIFF} = 60Ω, C_L = 15pF (Figure 5A)		Full	1	10	35	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_{DIFF} = 60Ω, C_L = 15pF (Figure 5A)		Full	3	5	20	ns
Driver Input to Output Delay	t_{PLH}, t_{PHL}	R_L = 27Ω, C_L = 15pF (Figure 5C)		Full	6	10	35	ns
Driver Output Skew	t_{SKEW}	R_L = 27Ω, C_L = 15pF (Figure 5C)		Full	-	1	8	ns
Driver Enable to Output High (Except ISL83490)	t_{ZH}	R_L = 110Ω, C_L = 50pF, SW = GND (Figure 6), (Note 8)		Full	-	45	90	ns
Driver Enable to Output Low (Except ISL83490)	t_{ZL}	R_L = 110Ω, C_L = 50pF, SW = V_{CC} (Figure 6), (Note 8)		Full	-	45	90	ns
Driver Disable from Output High (Except ISL83490)	t_{HZ}	R_L = 110Ω, C_L = 50pF, SW = GND (Figure 6)		+25	-	65	80	ns
				Full	-	-	110	ns
Driver Disable from Output Low (Except ISL83490)	t_{LZ}	R_L = 110Ω, C_L = 50pF, SW = V_{CC} (Figure 6)		+25	-	65	80	ns
				Full	-	-	110	ns
Driver Enable from Shutdown to Output High (Except ISL83490)	$t_{ZH(SHDN)}$	R_L = 110Ω, C_L = 50pF, SW = GND (Figure 6), (Notes 10, 11)		Full	-	115	150	ns
Driver Enable from Shutdown to Output Low (Except ISL83490)	$t_{ZL(SHDN)}$	R_L = 110Ω, C_L = 50pF, SW = V_{CC} (Figure 6), (Notes 10, 11)		Full	-	115	150	ns
DRIVER SWITCHING CHARACTERISTICS (ISL83483, ISL83488)								
Maximum Data Rate	f_{MAX}			Full	250	-	-	kbps
Driver Differential Output Delay	t_{DD}	R_{DIFF} = 60Ω, C_L = 15pF (Figure 5A)		Full	600	930	1400	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_{DIFF} = 60Ω, C_L = 15pF (Figure 5A)		Full	400	900	1200	ns
Driver Input to Output Delay	t_{PLH}, t_{PHL}	R_L = 27Ω, C_L = 15pF (Figure 5C)		+25	600	930	1500	ns
				Full	400	-	1500	ns
Driver Output Skew	t_{SKEW}	R_L = 27Ω, C_L = 15pF (Figure 5C)		Full	-	140	-	ns
Driver Enable to Output High (Except ISL83488)	t_{ZH}	R_L = 110Ω, C_L = 50pF, SW = GND (Figure 6), (Note 8)		Full	-	385	800	ns
Driver Enable to Output Low (Except ISL83488)	t_{ZL}	R_L = 110Ω, C_L = 50pF, SW = V_{CC} (Figure 6), (Note 8)		Full	-	55	800	ns
Driver Disable from Output High (Except ISL83488)	t_{HZ}	R_L = 110Ω, C_L = 50pF, SW = GND (Figure 6)		+25	-	63	80	ns
				Full	-	-	110	ns

Electrical Specifications Test conditions: V_{CC} = 3V to 3.6V; unless otherwise specified. Typicals are at V_{CC} = 3.3V, T_A = +25°C, Note 5. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNIT
Driver Disable from Output Low (Except ISL83488)	t_{LZ}	R_L = 110Ω, C_L = 50pF, SW = V_{CC} (Figure 6)	+25	-	70	80	ns
			Full	-	-	110	ns
Driver Enable from Shutdown to Output High (Except ISL83488)	$t_{ZH(SHDN)}$	R_L = 110Ω, C_L = 50pF, SW = GND (Notes 10, 11)	Full	-	450	2000	ns
Driver Enable from Shutdown to Output Low (Except ISL83488)	$t_{ZL(SHDN)}$	R_L = 110Ω, C_L = 50pF, SW = V_{CC} (Figure 6), (Notes 10, 11)	Full	-	126	2000	ns
RECEIVER SWITCHING CHARACTERISTICS (All Versions)							
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	(Figure 7)	Full	25	45	90	ns
Receiver Skew | t_{PLH} - t_{PHL} |	t_{SKD}	(Figure 7)	+25	-	2	10	ns
			Full	-	2	12	ns
Receiver Enable to Output High (Except ISL83488 and ISL83490)	t_{ZH}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 8), (Note 9)	Full	-	11	50	ns
Receiver Enable to Output Low (Except ISL83488 and ISL83490)	t_{ZL}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 8), (Note 9)	Full	-	11	50	ns
Receiver Disable from Output High (Except ISL83488 and ISL83490)	t_{HZ}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 8)	Full	-	7	45	ns
Receiver Disable from Output Low (Except ISL83488 and ISL83490)	t_{LZ}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 8)	Full	-	7	45	ns
Time to Shutdown (Except ISL83488 and ISL83490)	t_{SHDN}	(Note 10)	Full	80	190	300	ns
Receiver Enable from Shutdown to Output High (Except ISL83488 and ISL83490)	$t_{ZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 8), (Notes 10, 11)	Full	-	240	600	ns
Receiver Enable from Shutdown to Output Low (Except ISL83488 and ISL83490)	$t_{ZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 8), (Notes 10, 11)	Full	-	240	600	ns

NOTES:

5. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
6. Supply current specification is valid for loaded drivers when DE = 0V.
7. Applies to peak current. See "Typical Performance Curves" on page 11 for more information.
8. When testing the ISL83483, ISL83485, and ISL83491, keep $\overline{RE}$ = 0 to prevent the device from entering SHDN.
9. When testing the ISL83483, ISL83485, and ISL83491, the $\overline{RE}$ signal high time must be short enough (typically <100ns) to prevent the device from entering SHDN.
10. The ISL83483, ISL83485, and ISL83491 are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 80ns, the parts are ensured not to enter shutdown. If the inputs are in this state for at least 300ns, the parts are ensured to have entered shutdown. See "Low Power Shutdown Mode (ISL83483, ISL83485, ISL83491 Only)" on page 11.
11. Keep $\overline{RE}$ = VCC, and set the DE signal low time >300ns to ensure that the device enters SHDN.
12. Set the $\overline{RE}$ signal high time >300ns to ensure that the device enters SHDN.

Test Circuits and Waveforms

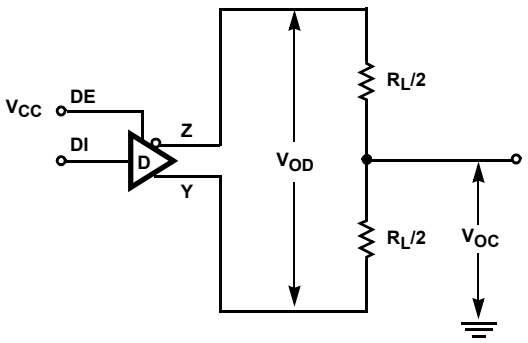


FIGURE 4A. V_{OD} AND V_{OC}

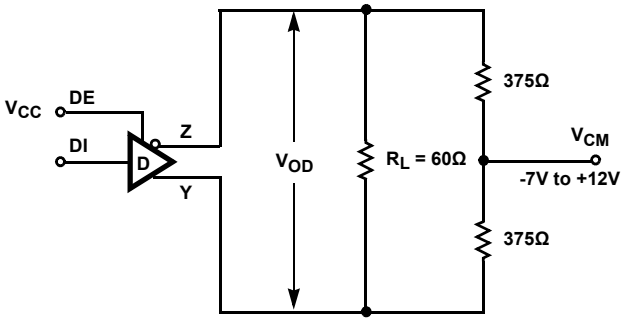


FIGURE 4B. V_{OD} WITH COMMON MODE LOAD

FIGURE 4. DC DRIVER TEST CIRCUITS

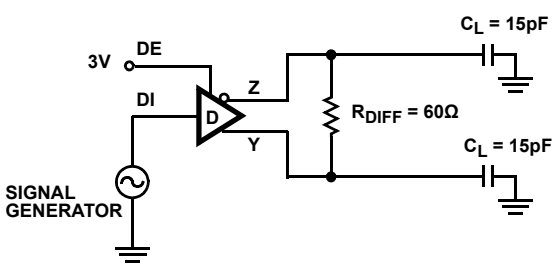


FIGURE 5A. DIFFERENTIAL TEST CIRCUIT

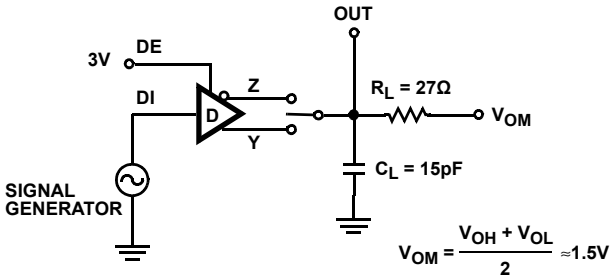


FIGURE 5C. SINGLE ENDED TEST CIRCUIT

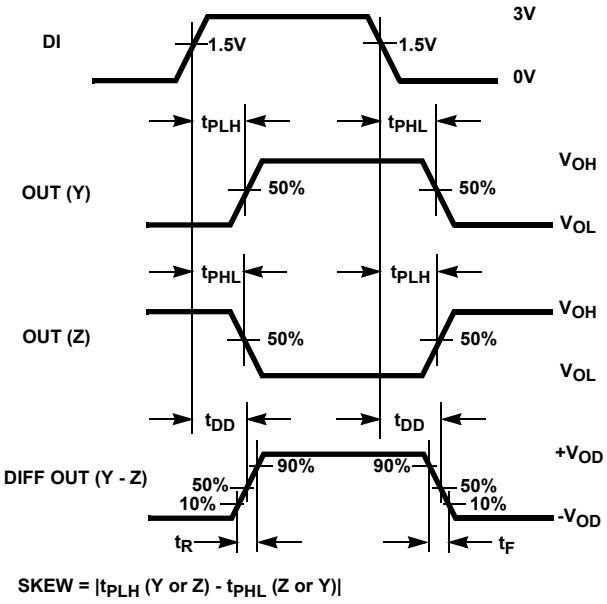
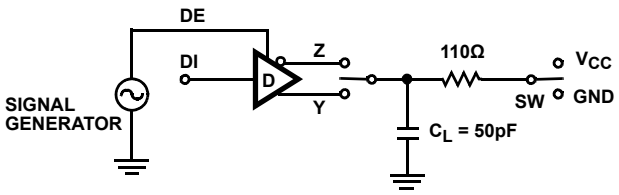


FIGURE 5B. MEASUREMENT POINTS

FIGURE 5. DRIVER PROPAGATION DELAY AND DIFFERENTIAL TRANSITION TIMES

Test Circuits and Waveforms (Continued)



PARAMETER	OUTPUT	$\overline{RE}$	DI	SW
t_{HZ}	Y/Z	X	1/0	GND
t_{LZ}	Y/Z	X	0/1	V_{CC}
t_{ZH}	Y/Z	0 (Note 8)	1/0	GND
t_{ZL}	Y/Z	0 (Note 8)	0/1	V_{CC}
$t_{ZH(SHDN)}$	Y/Z	1 (Note 11)	1/0	GND
$t_{ZL(SHDN)}$	Y/Z	1 (Note 11)	0/1	V_{CC}

FIGURE 6A. TEST CIRCUIT

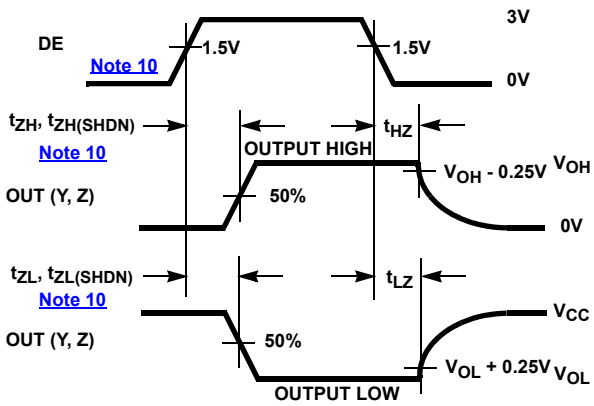


FIGURE 6B. MEASUREMENT POINTS

FIGURE 6. DRIVER ENABLE AND DISABLE TIMES (EXCLUDING ISL83488, ISL83490)

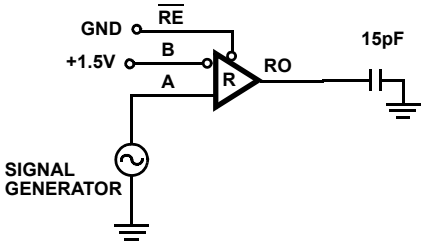


FIGURE 7A. TEST CIRCUIT

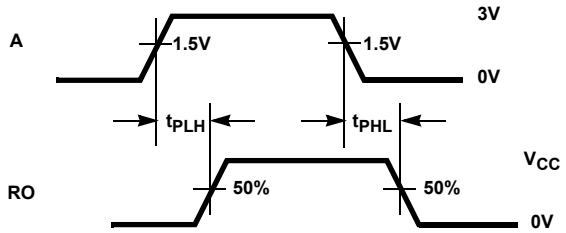
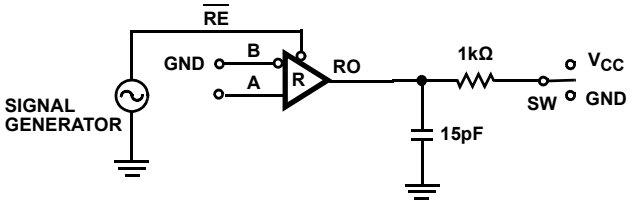


FIGURE 7B. MEASUREMENT POINTS

FIGURE 7. RECEIVER PROPAGATION DELAY



PARAMETER	DE	A	SW
t_{HZ}	0	+1.5V	GND
t_{LZ}	0	-1.5V	V_{CC}
t_{ZH} (Note 9)	0	+1.5V	GND
t_{ZL} (Note 9)	0	-1.5V	V_{CC}
$t_{ZH(SHDN)}$ (Note 12)	0	+1.5V	GND
$t_{ZL(SHDN)}$ (Note 12)	0	-1.5V	V_{CC}

FIGURE 8A. TEST CIRCUIT

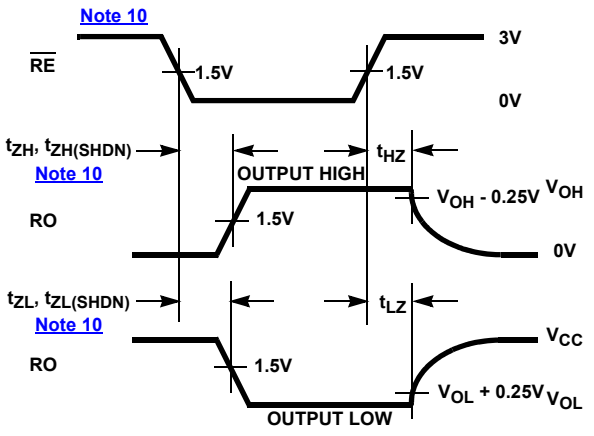


FIGURE 8B. MEASUREMENT POINTS

FIGURE 8. RECEIVER ENABLE AND DISABLE TIMES (EXCLUDING ISL83488, ISL83490)

Application Information

RS-485 and RS-422 are differential (balanced) data transmission standards for use in long haul or noisy environments. RS-422 is a subset of RS-485, so RS-485 transceivers are also RS-422 compliant. RS-422 is a point-to-multipoint (multidrop) standard, which allows only one driver and up to 10 (assuming one unit load devices) receivers on each bus. RS-485 is a true multipoint standard, which allows up to 32 one unit load devices (any combination of drivers and receivers) on each bus. To allow for multipoint operation, the RS-485 specification requires that drivers must handle bus contention without sustaining any damage.

Another important advantage of RS-485 is the extended Common-Mode Range (CMR), which specifies that the driver outputs and receiver inputs withstand signals that range from +12V to -7V. RS-422 and RS-485 are intended for runs as long as 4000', so the wide CMR is necessary to handle ground potential differences, as well as voltages induced in the cable by external fields.

Receiver Features

These devices use a differential input receiver for maximum noise immunity and common-mode rejection. Input sensitivity is ±200mV, as required by the RS422 and RS-485 specifications.

Receiver input impedance surpasses the RS-422 spec of 4kΩ, and meets the RS-485 "Unit Load" requirement of 12kΩ minimum.

Receiver inputs function with common-mode voltages as great as +9V/-7V outside the power supplies (that is, +12V and -7V), making them ideal for long networks where induced voltages are a realistic concern.

All the receivers include a "fail-safe if open" function that ensures a high level receiver output if the receiver inputs are unconnected (floating).

Receivers easily meet the data rates supported by the corresponding driver.

ISL83483, ISL83485, ISL83491 receiver outputs are tri-statable using the active low $\overline{RE}$ input.

Driver Features

The RS-485, RS-422 driver is a differential output device that delivers at least 1.5V across a 54Ω load (RS-485), and at least 2V across a 100Ω load (RS-422) even with V_{CC} = 3V. The drivers feature low propagation delay skew to maximize bit width, and to minimize EMI.

Drivers of the ISL83483, ISL83485, and ISL83491 are tri-statable using the active high DE input.

ISL83483 and ISL83488 driver outputs are slew rate limited to minimize EMI, and to minimize reflections in unterminated or improperly terminated networks. Data rate on these slew rate limited versions is a maximum of 250kbps. Outputs of ISL83485, ISL83490, and ISL83491 drivers are not limited, so faster output transition times allow data rates of at least 10Mbps.

Data Rate, Cables, and Terminations

RS-485 and RS-422 are intended for network lengths up to 4000', but the maximum system data rate decreases as the transmission length increases. Devices operating at 10Mbps are limited to lengths of a few hundred feet, while the 250kbps versions can operate at full data rates with lengths in excess of 1000'.

Twisted pair is the cable of choice for RS-485 and RS-422 networks. Twisted pair cables tend to pick up noise and other electromagnetically induced voltages as common-mode signals, which are effectively rejected by the differential receivers in these ICs.

Proper termination is imperative, when using the 10Mbps devices, to minimize reflections. Short networks using the 250kbps versions need not be terminated, but, terminations are recommended unless power dissipation is an overriding concern.

In point-to-point, or point-to-multipoint (single driver on bus) networks, the main cable should be terminated in its characteristic impedance (typically 120Ω) at the end farthest from the driver. In multi-receiver applications, stubs connecting receivers to the main cable should be kept as short as possible. Multipoint (multi-driver) systems require that the main cable be terminated in its characteristic impedance at both ends. Stubs connecting a transceiver to the main cable should be kept as short as possible.

Built-In Driver Overload Protection

As stated previously, the RS-485 specification requires that drivers survive worst case bus contentions undamaged. The ISL834xx devices meet this requirement through driver output short-circuit current limits, and on-chip thermal shutdown circuitry.

The driver output stages incorporate short-circuit current limiting circuitry, which ensures that the output current never exceeds the RS-485 specification, even at the common-mode voltage range extremes. Additionally, these devices use a foldback circuit which reduces the short-circuit current, and thus the power dissipation, whenever the contending voltage exceeds either supply.

In the event of a major short-circuit condition, the ISL834xx devices also include a thermal shutdown feature that disables the drivers whenever the die temperature becomes excessive. This eliminates the power dissipation, allowing the die to cool. The drivers automatically re-enable after the die temperature drops about 15°. If the contention persists, the thermal shutdown/re-enable cycle repeats until the fault is cleared. Receivers stay operational during thermal shutdown.

Low Power Shutdown Mode (ISL83483, ISL83485, ISL83491 Only)

These CMOS transceivers all use a fraction of the power required by their bipolar counterparts, but the ISL83483, ISL83485, and ISL83491 include a shutdown feature that reduces the already low quiescent I_{CC} to a 15nA trickle. They enter shutdown whenever the receiver and driver are ***simultaneously*** disabled ($\overline{RE}$ = V_{CC} and DE = GND) for a period of at least 300ns. Disabling both the driver and the receiver for less than 80ns ensures that shutdown is not entered.

Note that receiver and driver enable times increase when these devices enable from shutdown. For more information refer to Notes 8 through 12 on page 7 at the end of the Electrical Specification table.

Typical Performance Curves V_{CC} = 3.3V, T_A = +25°C, ISL83483 thru ISL83491; Unless otherwise specified

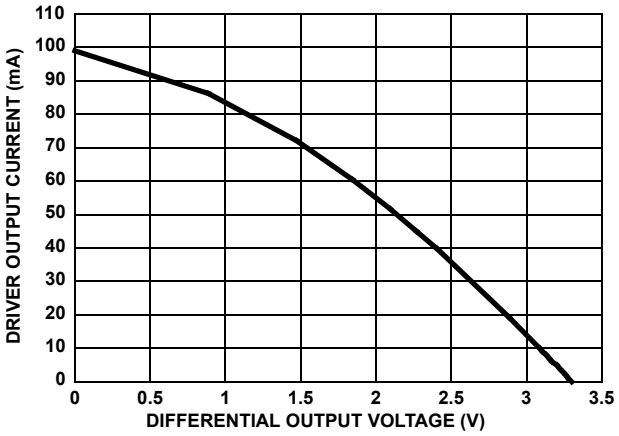


FIGURE 9. DRIVER OUTPUT CURRENT vs DIFFERENTIAL OUTPUT VOLTAGE

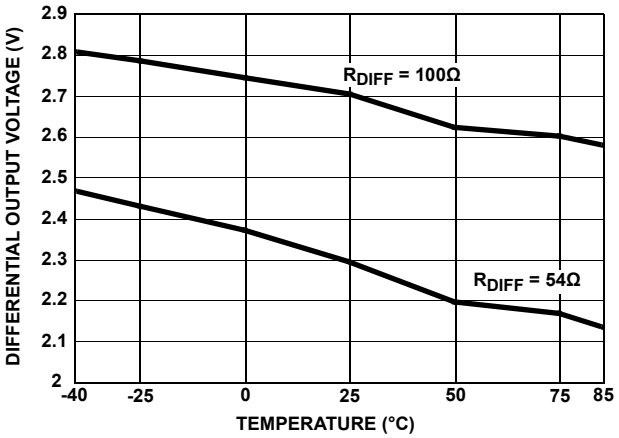


FIGURE 10. DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs TEMPERATURE

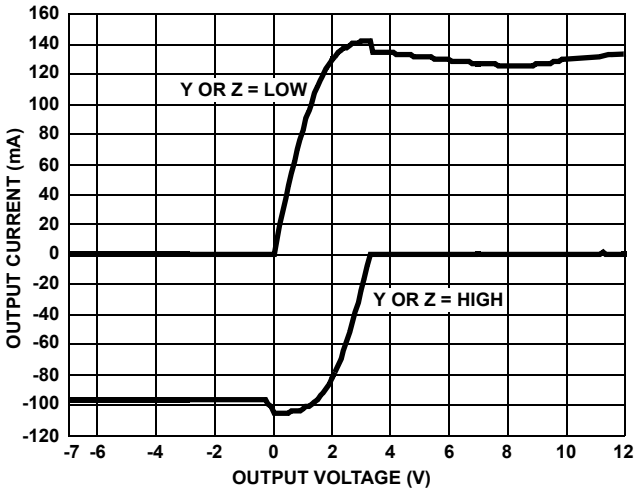


FIGURE 11. DRIVER OUTPUT CURRENT vs SHORT-CIRCUIT VOLTAGE

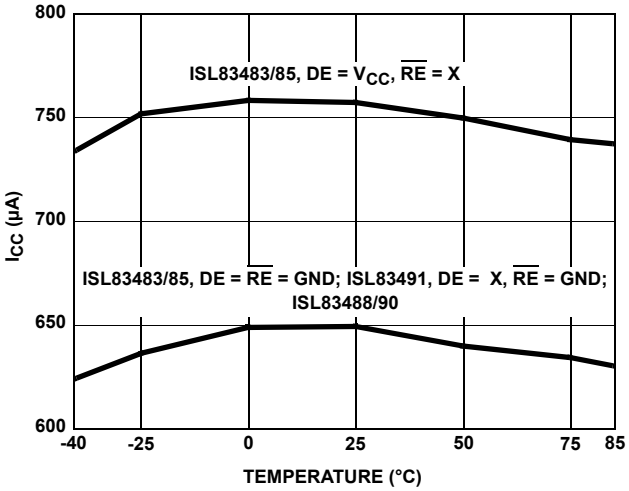


FIGURE 12. SUPPLY CURRENT vs TEMPERATURE

Typical Performance Curves V_{CC} = 3.3V, T_A = +25°C, ISL83483 thru ISL83491; Unless otherwise specified **(Continued)**

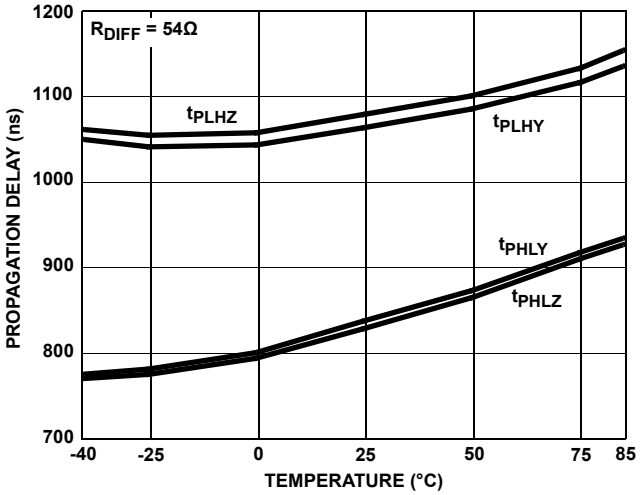


FIGURE 13. DRIVER PROPAGATION DELAY vs TEMPERATURE (ISL83483, ISL83488)

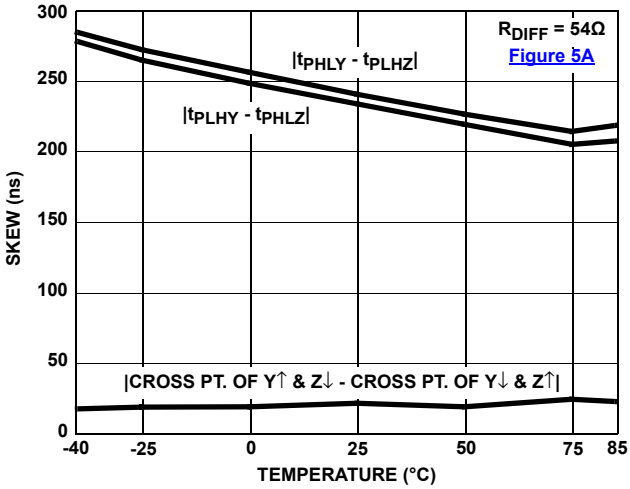


FIGURE 14. DRIVER SKEW vs TEMPERATURE (ISL83483, ISL83488)

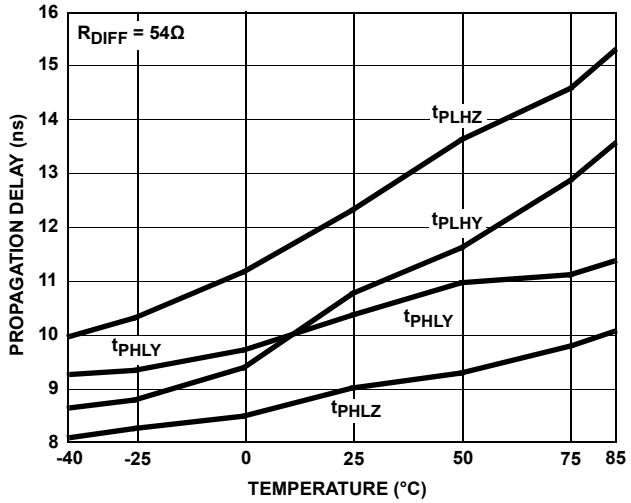


FIGURE 15. DRIVER PROPAGATION DELAY vs TEMPERATURE (ISL83485, ISL83490, ISL83491)

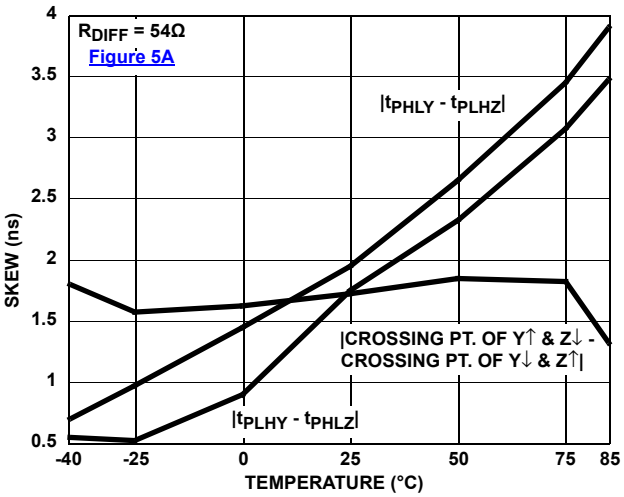


FIGURE 16. DRIVER SKEW vs TEMPERATURE (ISL83485, ISL84390, ISL83491)

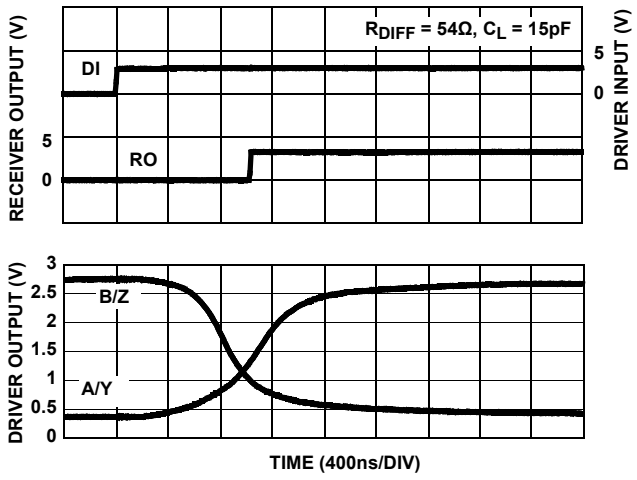


FIGURE 17. DRIVER AND RECEIVER WAVEFORMS, LOW TO HIGH (ISL83483, ISL83488)

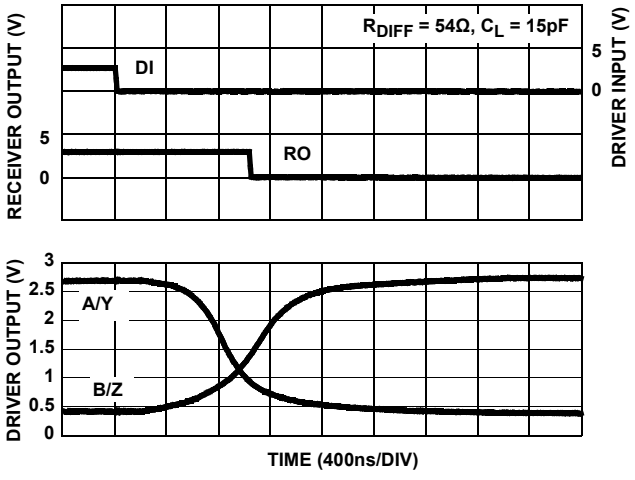


FIGURE 18. DRIVER AND RECEIVER WAVEFORMS, HIGH TO LOW (ISL83483, ISL83488)

Typical Performance Curves V_{CC} = 3.3V, T_A = +25°C, ISL83483 thru ISL83491; Unless otherwise specified **(Continued)**

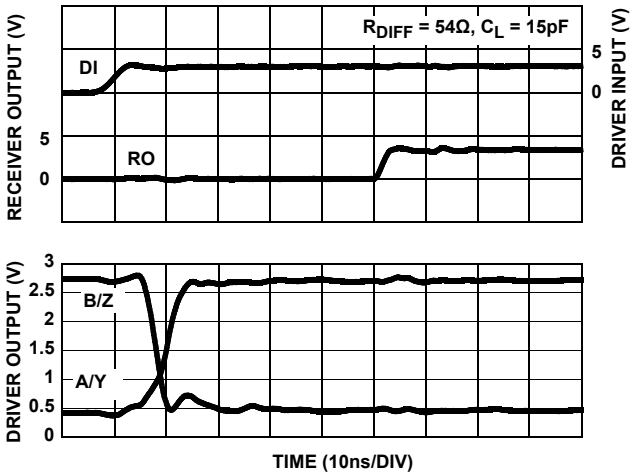


FIGURE 19. DRIVER AND RECEIVER WAVEFORMS, LOW TO HIGH (ISL83485, ISL83490, ISL83491)

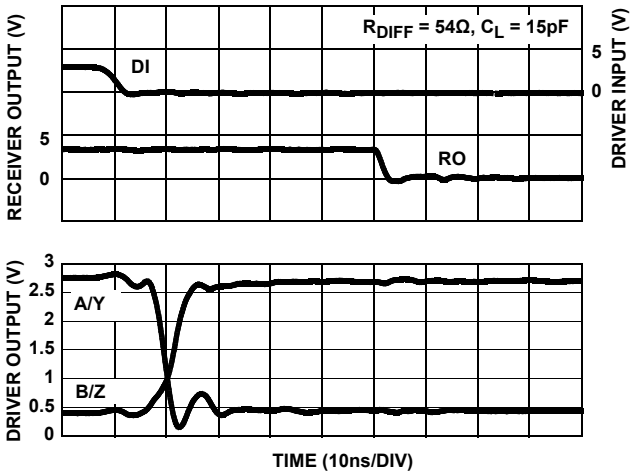


FIGURE 20. DRIVER AND RECEIVER WAVEFORMS, HIGH TO LOW (ISL83485, ISL83490, ISL83491)

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

528

PROCESS:

Si Gate CMOS

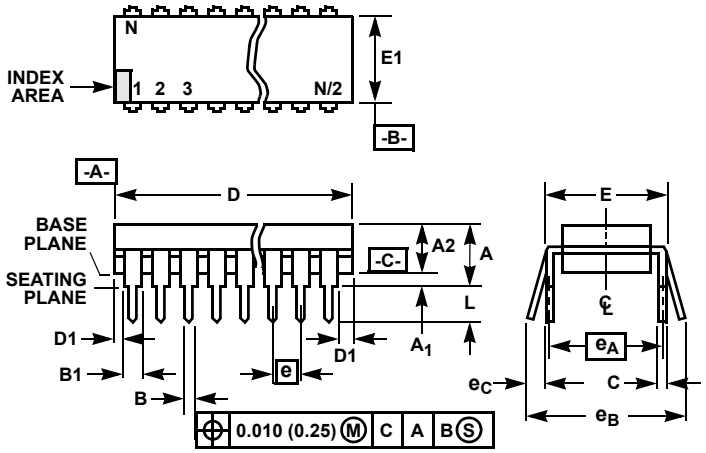
Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Nov 21, 2018	FN6052.5	Updated part marking in the ordering information table to represent what the brand has been on the products. Added PDIP note in the thermal information section and specified the Pb-free reflow note is applicable to SOIC pages only. Updated disclaimer.
Jul 27, 2018	FN6052.4	Added Related Literature on page 1. Updated Ordering Information table. Removed Retired parts, added tape and reel quantity column, and added MSL note. Updated Typical Operating Circuits on page 4. Thermal Information on page 5: Removed Maximum Lead Temperature (Soldering 10s)+300°C (SOIC - Lead Tips Only) Added Pb-Free Reflow information Updated POD M8.15 from rev 0 to rev 4. Changes since rev 0: Removed "u" symbol from drawing (overlaps the "a" on Side View). Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern Changed in Typical Recommended Land Pattern the following: 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205) Changed Note 1 "1982" to "1994" Updated POD M14.15 from rev 0 to rev 1. Changes since rev 0: Added land pattern and moved dimensions from table onto drawing Added Revision History. Updated disclaimer.

Package Outline Drawings

For the most recent package outline drawing, see E8.3.



NOTES:

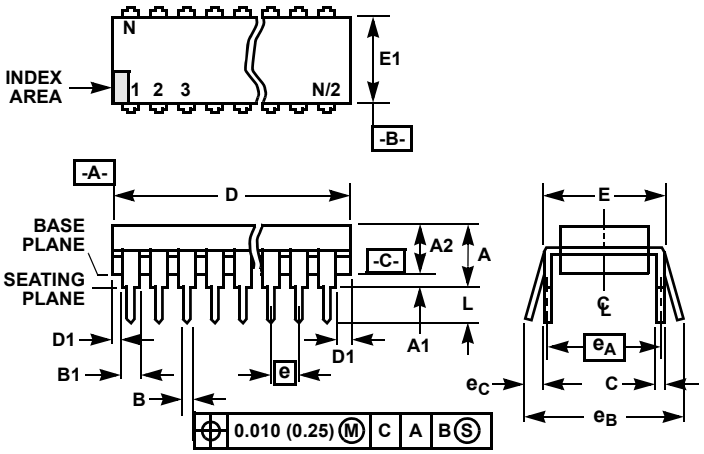
13. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
14. Dimensioning and tolerancing per ANSI Y14.5M-1982.
15. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
16. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
17. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
18. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
19. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
20. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
21. N is the maximum number of terminal positions.
22. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

Rev. 0 12/93

For the most recent package outline drawing, see E14.3.



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

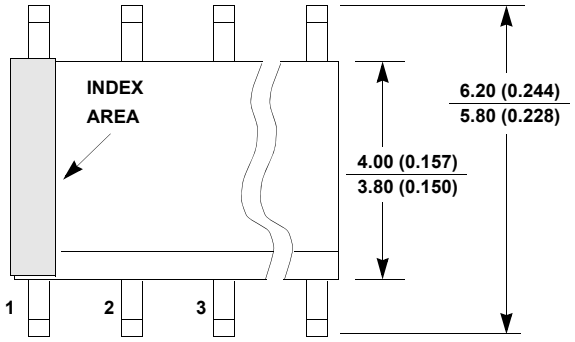
E14.3 (JEDEC MS-001-AA ISSUE D)
14 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	14		14		9

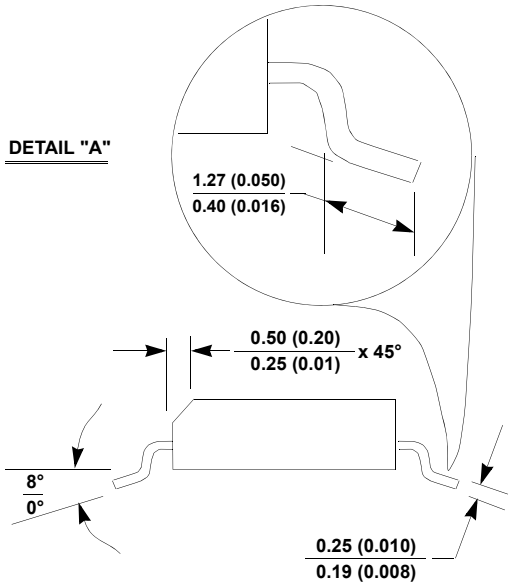
Rev. 0 12/93

M8.15
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 4, 1/12

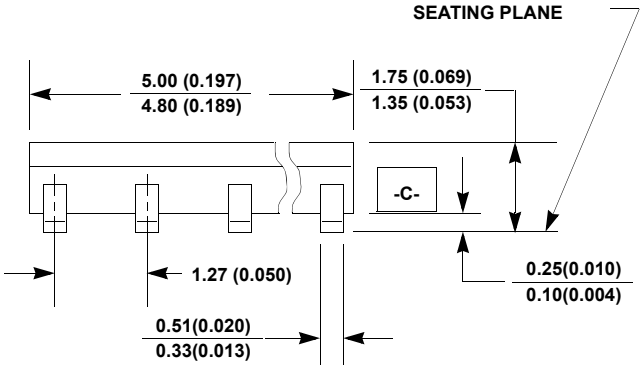
For the most recent package outline drawing, see M8.15.



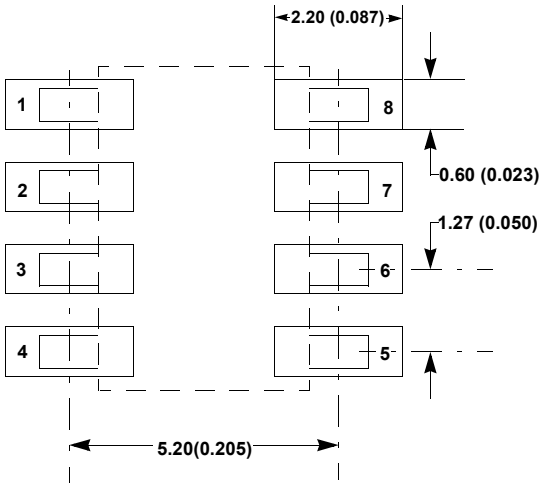
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



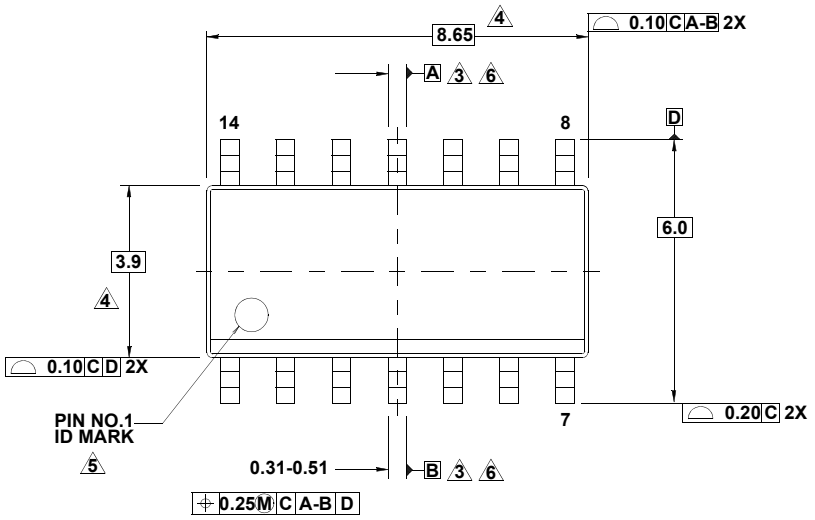
TYPICAL RECOMMENDED LAND PATTERN

NOTES:

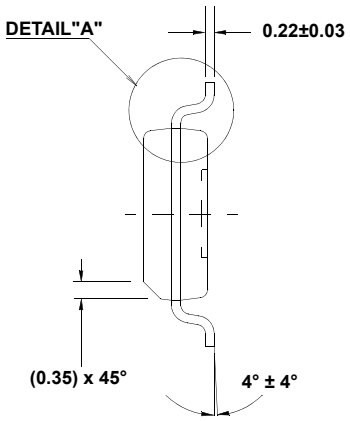
1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

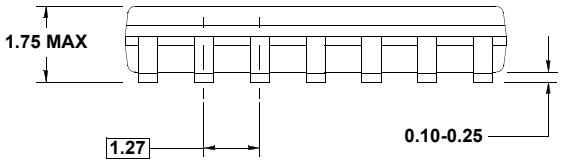
M14.15
14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 1, 10/09

For the most recent package outline drawing, see M14.15.

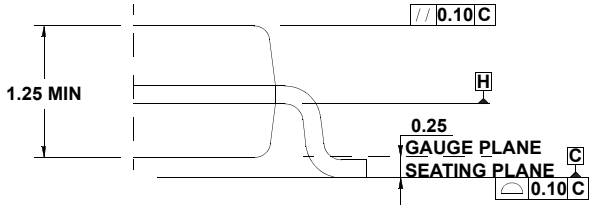


TOP VIEW

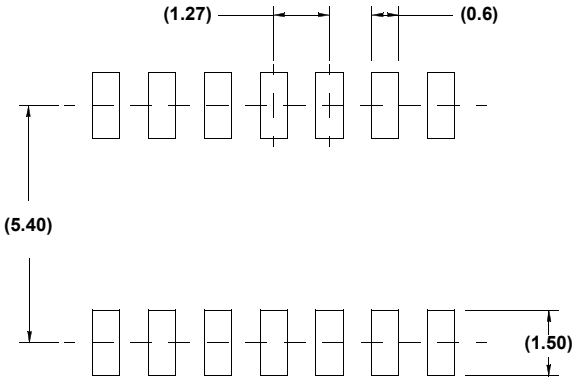




SIDE VIEW



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSEY14.5m-1994.
3. Datums A and B to be determined at Datum H.
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 indentifier may be either a mold or mark feature.
6. Does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of lead width at maximum condition.
7. Reference to JEDEC MS-012-AB.