ISL84541, ISL84544

Low-Voltage, Single Supply, Dual SPST, SPDT Analog Switches

FN6016
Rev.8.0
Feb 25, 2021

The ISL84541 and ISL84544 devices are precision, dual analog switches designed to operate from a single +2.7V to +12V supply. Targeted applications include battery powered equipment that benefit from the devices' low power consumption (5µW), low leakage currents (100pA max), and fast switching speeds (t_{ON} = 35ns, t_{OFF} = 25ns). Cell phones, for example, often face ASIC functionality limitations. The number of analog input or GPIO pins may be limited and digital geometries are not well suited to analog switch performance. This family of parts may be used to mux-in additional functionality while reducing ASIC design risk. Some of the smallest packages are available alleviating board space limitations.

The ISL84541 is a dual single-pole/single-throw (SPST) device. The ISL84541 has two normally open (NO) switches. The ISL84544 is a committed SPDT, which is perfect for use in 2-to-1 multiplexer applications.

Table 1 summarizes the performance of this family. For higher performance, pin compatible versions, see the ISL43120 - 22 and ISL43210 datasheet.

Applications

- Battery Powered, Handheld, and Portable Equipment
  - Cellular/Mobile Phones
  - Pagers
  - Laptops, Notebooks, Palmtops
- Communications Systems
  - Military Radios
  - PBX, PABX
- Test Equipment
  - Ultrasound
  - Electrocardiograph
- Heads-Up Displays
- Audio and Video Switching
- Various Circuits
  - +3V/+5V DACs and ADCs
  - Sample and Hold Circuits
  - Digital Filters
  - Operational Amplifier Gain Switching Networks
  - High Frequency Analog Switching
  - High Speed Multiplexing
  - Integrator Reset Circuits

Features

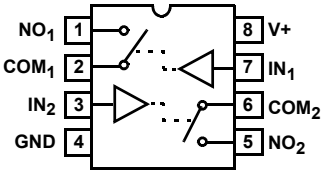
- Drop-in Replacements for MAX4541, MAX4544, DG9263
- Fully Specified at 3.3V and 5V Supplies
- Pin Compatible with MAX323
- ON Resistance (R_{ON}) 30Ω
- R_{ON} Matching Between Channels. . . . . <1Ω
- Low Charge Injection . . . . . 5pC (Max)
- Single Supply Operation. . . . . +2.7V to +12V
- Low Power Consumption (P_D). . . . . <5µW
- Low Leakage Current (Max at 85°C) 10nA
- Fast Switching Action
  - t_{ON} 35ns
  - t_{OFF} 25ns
- Guaranteed Break-Before-Make (ISL84544 only)
- Minimum 2000V ESD Protection per Method 3015.7
- TTL, CMOS Compatible
- Available in SOT-23 Packaging

TABLE 1. FEATURES AT A GLANCE

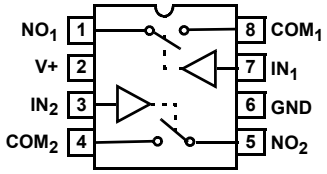
DEVICE	NUMBER OF SWITCHES	SW 1 / SW 2	3.3V R_{ON}	3.3V t_{ON} / t_{OFF}	5V R_{ON}	5V t_{ON} / t_{OFF}	PACKAGES
ISL84541	2	NO / NO	50Ω	50 / 20ns	30Ω	35 / 25ns	8 Ld SOIC, 8 Ld SOT-23,
ISL84544	1	SPDT	50Ω	50 / 20ns	30Ω	35 / 25ns	8 Ld SOIC, 6 Ld SOT-23

Pinouts (Note 1)

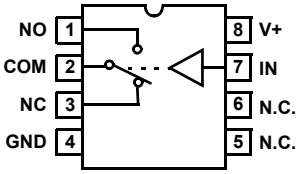
ISL84541 (SOIC)
TOP VIEW



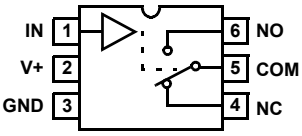
ISL84541 (SOT-23)
TOP VIEW



ISL84544 (SOIC)
TOP VIEW



ISL84544 (SOT-23)
TOP VIEW



NOTE:

1. Switches Shown for Logic “0” Input.

Truth Table

LOGIC	ISL84541	ISL84544	
	SW 1, 2	PIN NC	PIN NO
0	OFF	ON	OFF
1	ON	OFF	ON

NOTE: Logic “0” ≤ 0.8V. Logic “1” ≥ 2.4V.

Pin Descriptions

PIN	FUNCTION
V+	System Power Supply Input (+2.7V to +12V)
GND	Ground Connection
IN	Digital Control Input
COM	Analog Switch Common Pin
NO	Analog Switch Normally Open Pin
NC	Analog Switch Normally Closed Pin
N.C.	No Internal Connection

Ordering Information

PART NUMBER (Notes 3, 4)	PART MARKING	PACKAGE DESCRIPTION (RoHS Compliant)	PKG. DWG. #	CARRIER TYPE (Note 2)	TEMP. RANGE (°C)
ISL84541IBZ	84541 IBZ	8 Ld SOIC	M8.15	Tube	-40 to 85
ISL84541IBZ-T	84541 IBZ	8 Ld SOIC	M8.15	Reel, 2.5k units	
ISL84541IHZ-T	541Z (Note 5)	8 Ld SOT-23	P8.064	Reel, 3k units	
ISL84544IBZ	84544 IBZ	8 Ld SOIC	M8.15	Tube	-40 to 85
ISL84544IBZ-T	84544 IBZ	8 Ld SOIC	M8.15	Reel, 2.5k units	
ISL84544IHZ-T	544Z (Note 5)	6 Ld SOT-23	P6.064	Reel, 3k units	

NOTES:

2. See TB347 for details about reel specifications.
3. Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.
4. For Moisture Sensitivity Level (MSL), see the ISL84541 and ISL84544 device pages. For more information about MSL, see TB363.
5. The part marking is located on the bottom of the part.

Absolute Maximum Ratings

V+ to GND . . . . . -0.3 to15V
Input Voltages
IN (Note 6). . . . . -0.3 to ((V+) + 0.3V)
NO, NC (Note 6) . . . . . -0.3 to ((V+) + 0.3V)
Output Voltages
COM (Note 6) . . . . . -0.3 to ((V+) + 0.3V)
Continuous Current (Any Terminal) 10mA
Peak Current, IN, NO, NC, or COM
(Pulsed 1ms, 10% Duty Cycle, Max) 20mA
ESD Rating (Per MIL-STD-883 Method 3015). . . . . .>2kV

Thermal Information

Thermal Resistance (Typical, Note 7)	θ_{JA} (^{o}C/W)
6 Ld SOT-23 Package	230
8 Ld SOT-23 Package	215
8 LD SOIC Package	170

Maximum Junction Temperature (Plastic Package). . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Pb-Free Reflow Profile. . . . . see TB493

Operating Conditions

Temperature Range . . . . . -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" can cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

6. Signals on NC, NO, COM, or IN exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to maximum current ratings.
7. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications - 5V Supply

Test Conditions: V+ = +4.5V to +5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 8), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 4.5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3.5V, See Figure 4	25	-	30	60	Ω
		Full	-	-	75	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V+ = 5V, I_{COM} = 1.0mA, V_{NO} or V_{NC}= 3.5V	25	-	0.8	2	Ω
		Full	-	-	4	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1V, 2V, 3V	Full	-	7	8	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 5.5V, V_{COM} = 1V, 4.5V, V_{NO} or V_{NC} = 4.5V, 1V, Note 10	25	-0.1	0.01	0.1	nA
		Full	-5	-	5	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	V+ = 5.5V, V_{COM} = 4.5V, 1V, V_{NO} or V_{NC} = 1V, 4.5V, Note 10	25	-0.1	-	0.1	nA
		Full	-5	-	5	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 5.5V, V_{COM} = 1V, 4.5V, or V_{NO} or V_{NC} = 1V, 4.5V, or Floating, Note 10	25	-0.2	-	0.2	nA
		Full	-10	-	10	nA

Electrical Specifications - 5V Supply Test Conditions: V+ = +4.5V to +5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 8), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V_{NO} or V_{NC} = 3V, R_L =1kΩ, C_L = 35pF, V_{IN} = 0 to 3V, See Figure 1	25	-	35	100	ns
		Full	-	-	240	ns
Turn-OFF Time, t_{OFF}	V_{NO} or V_{NC} = 3V, R_L =1kΩ, C_L = 35pF, V_{IN} = 0 to 3V, See Figure 1	25	-	25	75	ns
		Full	-	-	150	ns
Break-Before-Make Time Delay (ISL84544 Only), t_D	R_L = 300Ω, C_L = 35pF, V_{NO} = V_{NC} = 3V, V_{IN} = 0 to 3V, See Figure 2	Full	2	10	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω, See Figure 2	25	-	1	5	pC
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 1MHz, See Figure 3	25	-	76	-	dB
Crosstalk (Channel-to-Channel)	R_L = 50Ω, C_L = 5pF, f = 1MHz, See Figure 5	25	-	-90	-	dB
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 6	25	-	8	-	pF
COM OFF Capacitance, $C_{COM(OFF)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 6	25	-	8	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 6, ISL84541/2/3	25	-	13	-	pF
	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 6, ISL84544	25	-	20	-	pF
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	2.7		12	V
Positive Supply Current, I+	V+ = 5.5V, V_{IN} = 0V or V+, all channels on or off	Full	-1	0.0001	1	µA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	-	0.8	V
Input Voltage High, V_{INH}		Full	2.4	-	-	V

NOTES:

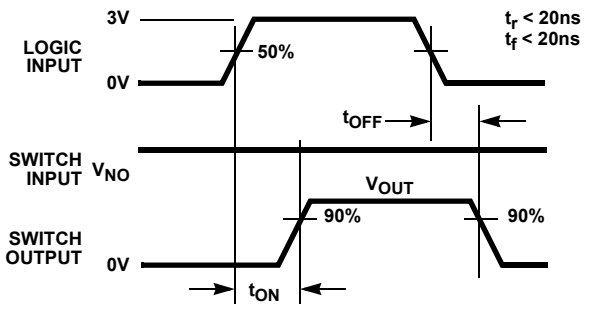
8. V_{IN} = input voltage to perform proper function.
9. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
10. Leakage parameter is 100% tested at high temp, and guaranteed by correlation at 25°C.

Electrical Specifications - 3.3V Supply

Test Conditions: V+ = +3.0V to +3.6V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 8), Unless Otherwise Specified

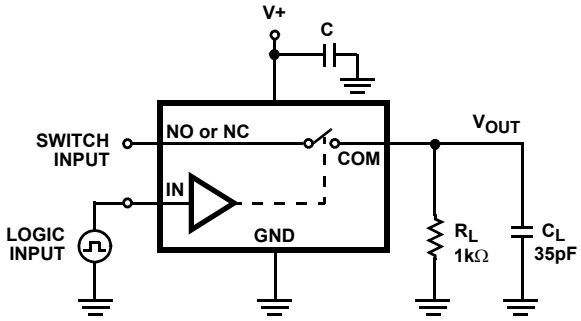
PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 3V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1.5V	25	-	50	80	Ω
		Full	-	-	140	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V+ = 3.3V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1.5V	25	-	0.8	2	Ω
		Full	-	-	4	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 3.3V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 0.5V, 1V, 1.5V	25	-	6	10	Ω
		Full	-	7	12	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 3.6V, V_{COM} = 1V, 3V, V_{NO} or V_{NC} = 3V, 1V, Note 10	25	-0.1	0.01	0.1	nA
		Full	-5	-	5	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	V+ = 3.6V, V_{COM} = 3V, 1V, V_{NO} or V_{NC} = 1V, 3V, Note 10	25	-0.1	0.01	0.1	nA
		Full	-5	-	5	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 3.6V, V_{COM} = 1V, 3V, or V_{NO} or V_{NC} = 1V, 3V, or floating, Note 10	25	-0.2	-	0.2	nA
		Full	-10	-	10	nA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V_{NO} or V_{NC} = 1.5V, R_L =1kΩ, C_L = 35pF, V_{IN} = 0 to 3V	25	-	50	120	ns
		Full			200	ns
Turn-OFF Time, t_{OFF}	V_{NO} or V_{NC} = 1.5V, R_L =1kΩ, C_L = 35pF, V_{IN} = 0 to 3V	25	-	20	50	ns
		Full	-	-	120	ns
Break-Before-Make Time Delay (ISL84544 Only), t_D	R_L = 300Ω, C_L = 35pF, V_{NO} or V_{NC} = 1.5V, V_{IN} = 0 to 3V	Full	3	30	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω	25	-	1	5	pC
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 1MHz	25	-	76	-	dB
Crosstalk (Channel-to-Channel)		25	-	-90	-	dB
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V	25	-	8	-	pF
COM OFF Capacitance, $C_{COM(OFF)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V	25	-	8	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, ISL84541/2/3	25	-	13	-	pF
	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, ISL84544	25	-	20	-	pF
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 3.6V, V_{IN} = 0V or V+, all channels on or off	Full	-1	-	1	µA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	-	0.8	V
Input Voltage High, V_{INH}		Full	2.4	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 3.6V, V_{IN} = 0V or V+	Full	-1	-	1	µA

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + R_{(ON)}}$$

FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

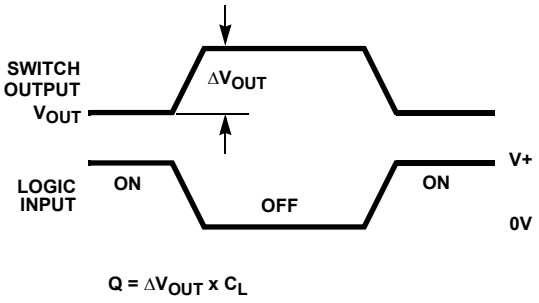


FIGURE 2A. MEASUREMENT POINTS

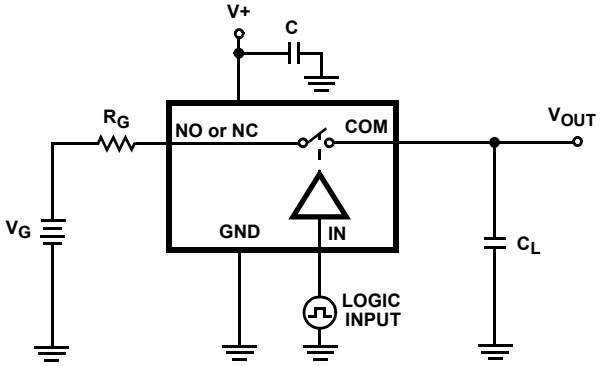


FIGURE 2B. TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

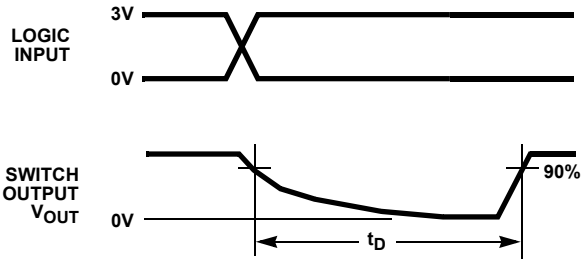
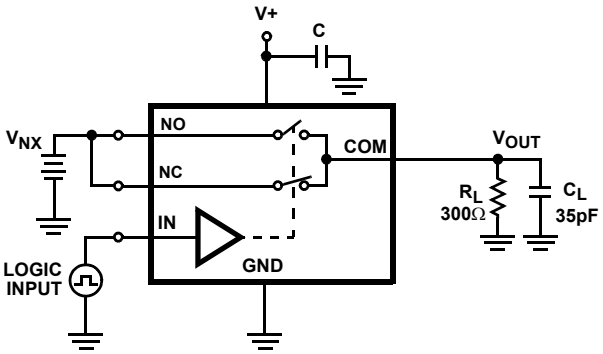


FIGURE 2C. MEASUREMENT POINTS (ISL84544 ONLY)



C_L includes fixture and stray capacitance.

FIGURE 2D. TEST CIRCUIT (ISL84544 ONLY)

FIGURE 2. BREAK-BEFORE-MAKE TIME

Test Circuits and Waveforms (Continued)

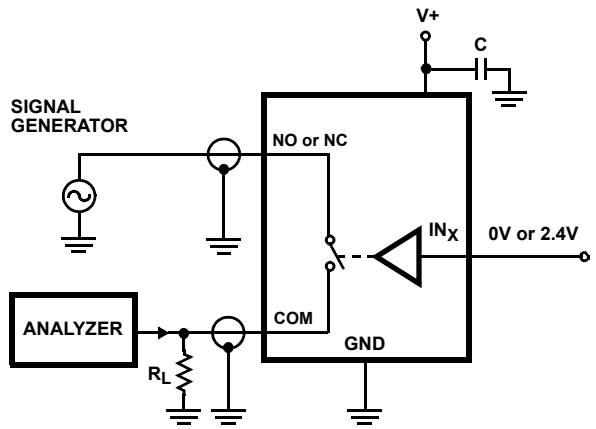


FIGURE 3. OFF ISOLATION TEST CIRCUIT

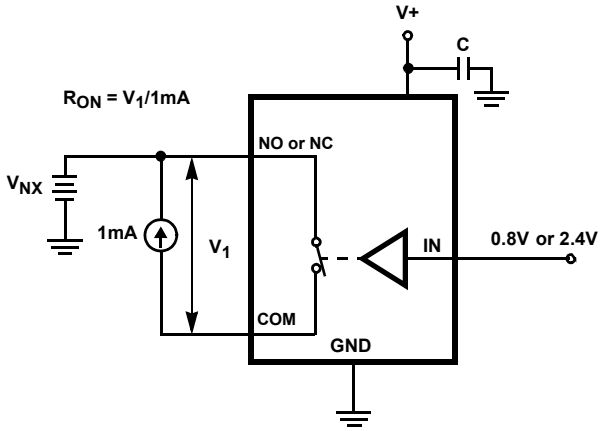


FIGURE 4. R_{ON} TEST CIRCUIT

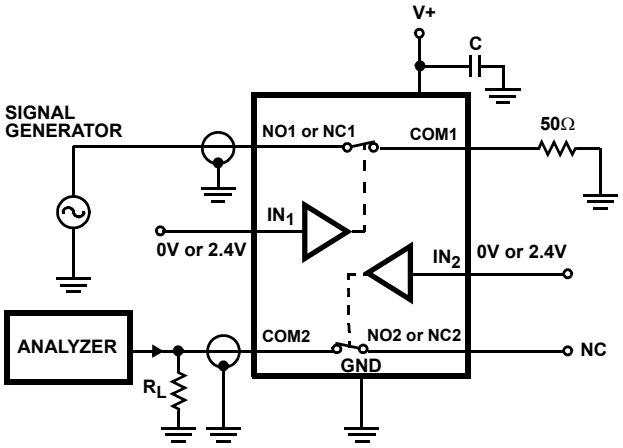


FIGURE 5. CROSSTALK TEST CIRCUIT

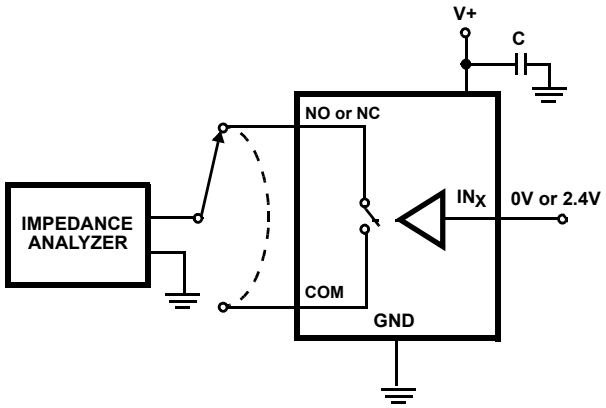


FIGURE 6. CAPACITANCE TEST CIRCUIT

Detailed Description

The ISL84541 and ISL84544 dual analog switches offer precise switching capability from a single 2.7V to 12V supply with low on-resistance (30Ω) and high speed operation (t_{ON} = 35ns, t_{OFF} = 25ns). The devices are especially well suited to portable battery powered equipment thanks to the low operating supply voltage (2.7V), low power consumption (5µW), low leakage currents (100pA max), and the tiny SOT-23 packaging. High frequency applications also benefit from the wide bandwidth, and the very high off isolation and crosstalk rejection.

Supply Sequencing And Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to GND (see Figure 7). To prevent forward biasing these diodes, V+ must be applied before any input signals, and input signal voltages must remain between V+ and GND. If these conditions cannot be guaranteed, then one of the following two protection methods should be employed.

Logic inputs can easily be protected by adding a 1kΩ resistor in series with the input (see Figure 7). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

Adding a series resistor to the switch input defeats the purpose of using a low R_{ON} switch, so two small signal diodes can be added in series with the supply pins to provide overvoltage protection for all pins (see Figure 7). These additional diodes limit the analog signal from 1V below V+ to 1V above GND. The low leakage current performance is unaffected by this approach, but the switch resistance may increase, especially at low supply voltages.

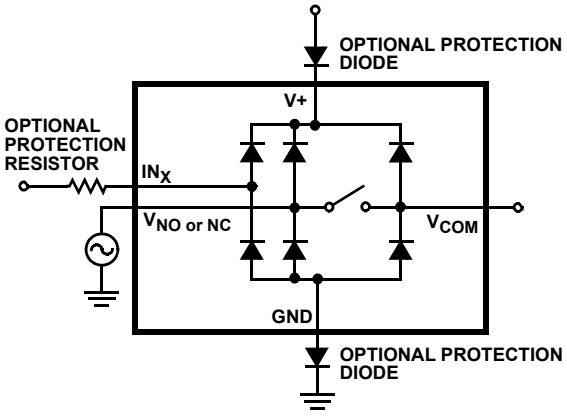


FIGURE 7. OVERVOLTAGE PROTECTION

Power-Supply Considerations

The ISL8454X construction is typical of most CMOS analog switches, except that they have only two supply pins: V+ and GND. V+ and GND drive the internal CMOS switches and set their analog voltage limits. Unlike switches with a 13V maximum supply voltage, the ISL8454X 15V maximum supply voltage provides plenty of room for the 10% tolerance of 12V supplies, as well as room for overshoot and noise spikes.

The minimum recommended supply voltage is 2.7V. It is important to note that the input signal range, switching times, and on-resistance degrade at lower supply voltages. Refer to the electrical specification tables and *Typical Performance* curves for details.

V+ and GND also power the internal logic and level shifters. The level shifters convert the logic levels to switched V+ and GND signals to drive the analog switch gate terminals.

This family of switches cannot be operated with bipolar supplies, because the input switching point becomes negative in this configuration.

Logic-Level Thresholds

This switch family is TTL compatible (0.8V and 2.4V) over a supply range of 3V to 11V (see Figure 14). At 12V the V_{IH} level is about 2.5V. This is still below the TTL guaranteed high output minimum level of 2.8V, but noise margin is reduced. For best results with a 12V supply, use a logic family the provides a V_{OH} greater than 3V.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat even past 300MHz (see Figure 15). Figure 15 also illustrates that the frequency response is very consistent over a wide V+ range, and for varying analog signal levels.

An off switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feedthrough from a switch's input to its output. Off Isolation is the resistance to this feedthrough, while Crosstalk indicates the amount of feedthrough from one switch to another. Figure 16 details the high Off Isolation and Crosstalk rejection provided by this family. At 10MHz, off isolation is about 50dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease Off Isolation and Crosstalk rejection due to the voltage divider action of the switch OFF impedance and the load impedance.

Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND.

Virtually all the analog leakage current comes from the ESD diodes to V+ or GND. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog-signal paths and V+ or GND.

Typical Performance Curves T_A = 25°C, Unless Otherwise Specified

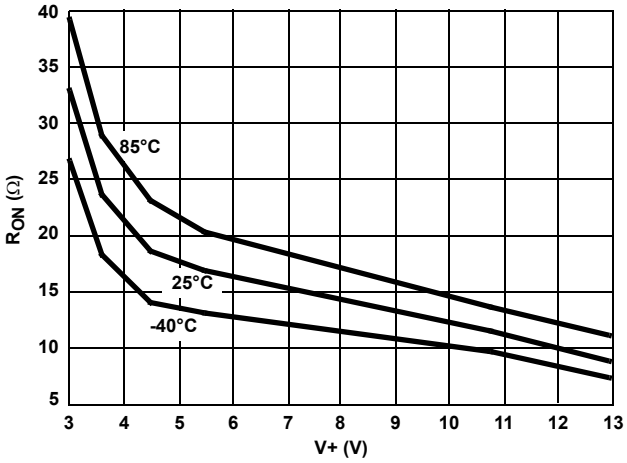


FIGURE 8. ON-RESISTANCE vs SUPPLY VOLTAGE

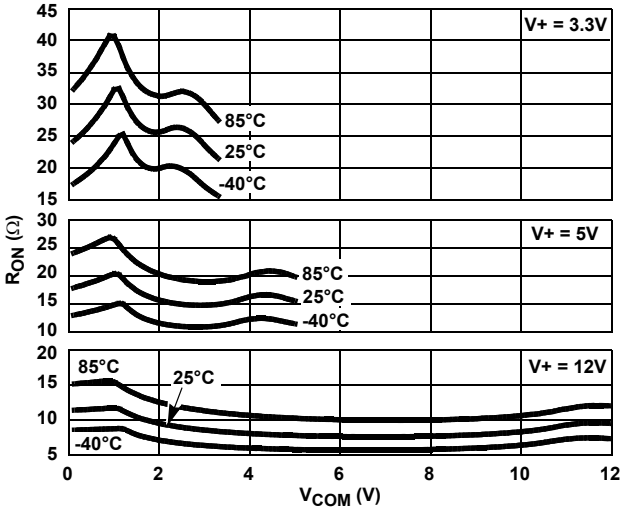


FIGURE 9. ON-RESISTANCE vs SWITCH VOLTAGE

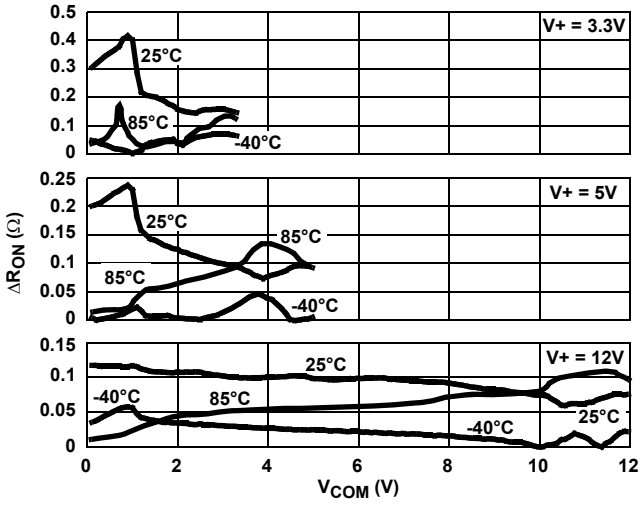


FIGURE 10. R_{ON} MATCH vs SWITCH VOLTAGE

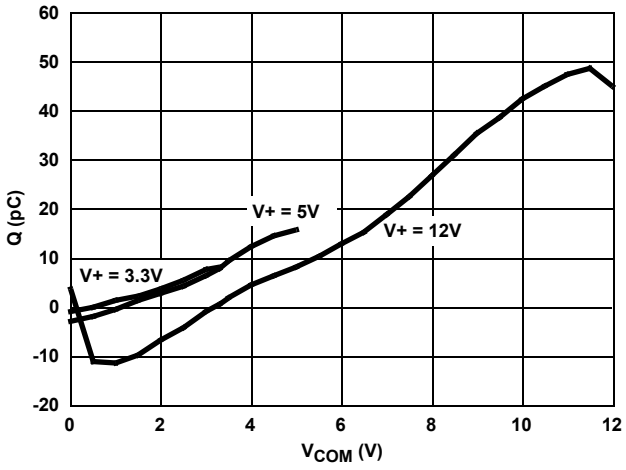


FIGURE 11. CHARGE INJECTION vs SWITCH VOLTAGE

Typical Performance Curves T_A = 25°C, Unless Otherwise Specified **(Continued)**

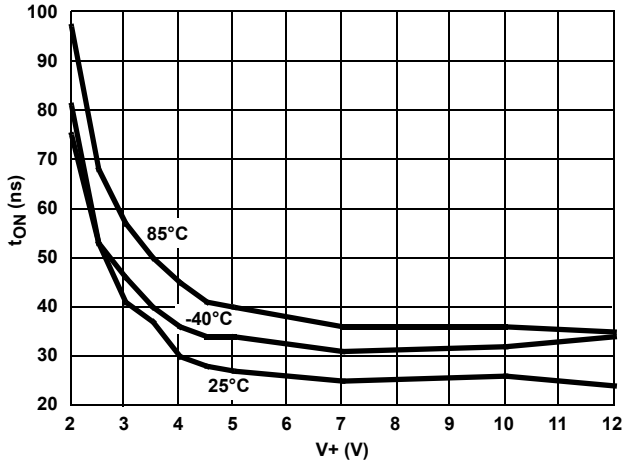


FIGURE 12. TURN-ON TIME vs SUPPLY VOLTAGE

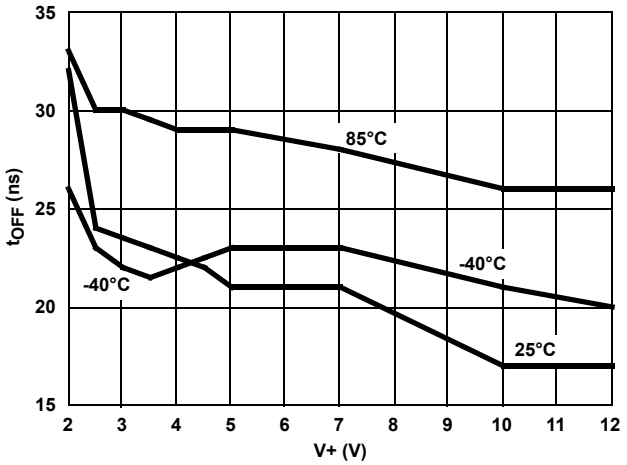


FIGURE 13. TURN-OFF TIME vs SUPPLY VOLTAGE

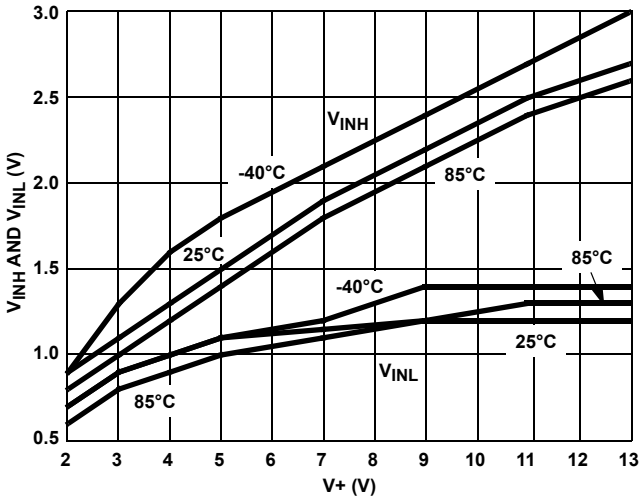


FIGURE 14. DIGITAL SWITCHING POINT vs SUPPLY VOLTAGE

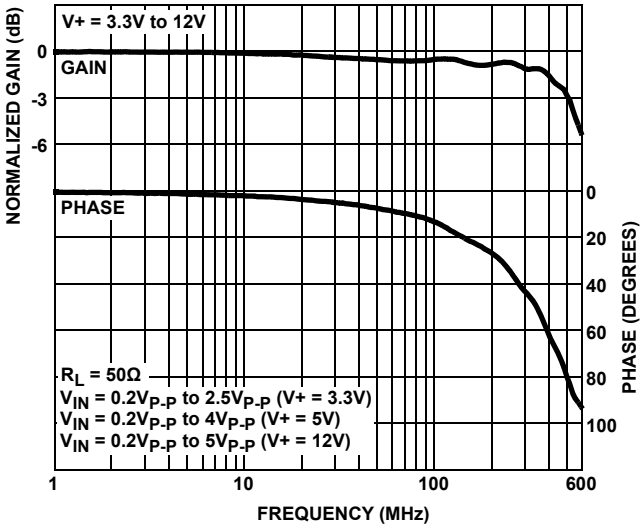


FIGURE 15. FREQUENCY RESPONSE

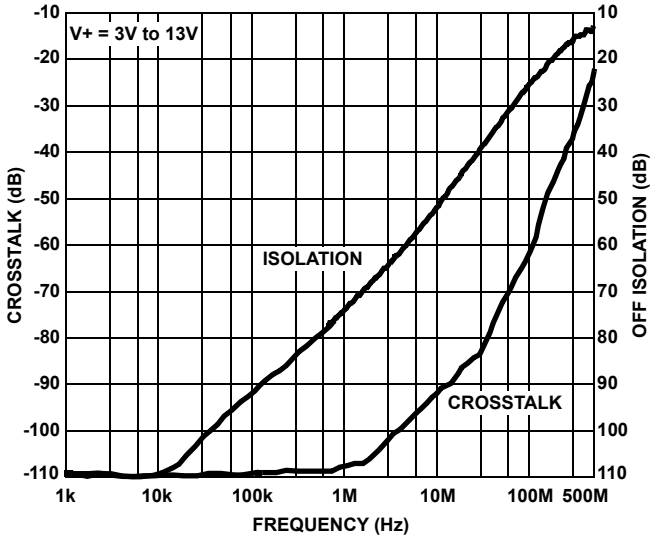


FIGURE 16. CROSSTALK AND OFF ISOLATION

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

ISL84541: 66
ISL84544: 58

PROCESS:

Si Gate CMOS

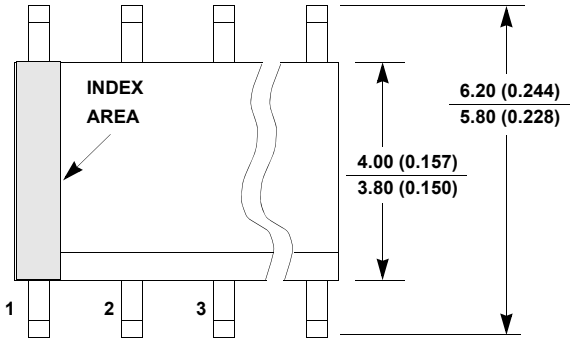
Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

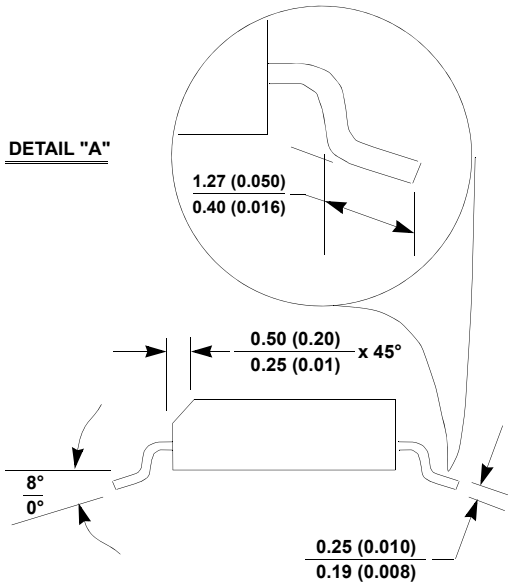
DATE	REVISION	CHANGE
Feb 25, 2021	8.0	Removed retired parts and applicable information throughout document. Updated links throughout. Removed Related literature section. Updated ordering Information table by adding ISL84541IHZ-T, adding notes, and reformatting table. Removed About Intersil section.
Aug 19, 2015	7.0	- Ordering Information Table on page 3. - Added Revision History. - Added About Intersil Verbiage. *Updated POD M8.118 to most recent revision, changes are as follows: -Revision 2 to Revision 3 Changes: Updated to new intersil format by adding land pattern and moving dimensions from table onto drawing -Revision 3 to Revision 4 Changes: Corrected lead width dimension in side view 1 from "0.25 - 0.036" to "0.25 - 0.36" *Updated POD M8.15 to most current revision with changes as follows: -Revision 0 to Revision 1 Changes: POD created from MCOL M8.15 -Revision 1 to Revision 2 Changes: Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern -Revision 2 to Revision 3 Changes: Changed Note 1 "1982" to "1994" Changed in Typical Recommended Land Pattern the following: 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205) -Revision 3 to Revision 4 Changes: Changed Note 1 "1982" to "1994" *Updated POD P6.064 to most current revision with changes as follows: Updated to new format (same dimensions, added land pattern and moved dimensions from table onto drawing)

Package Outline Drawings

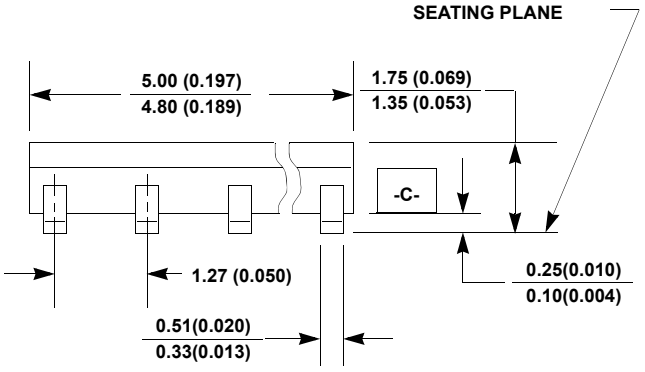
M8.15
8 Lead Narrow Body Small Outline Plastic Package
Rev 4, 1/12



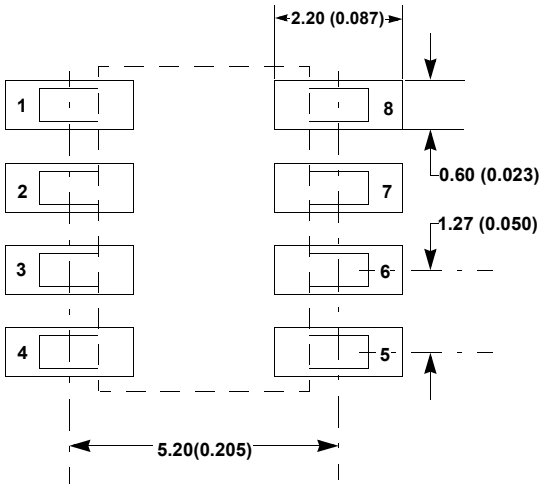
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"

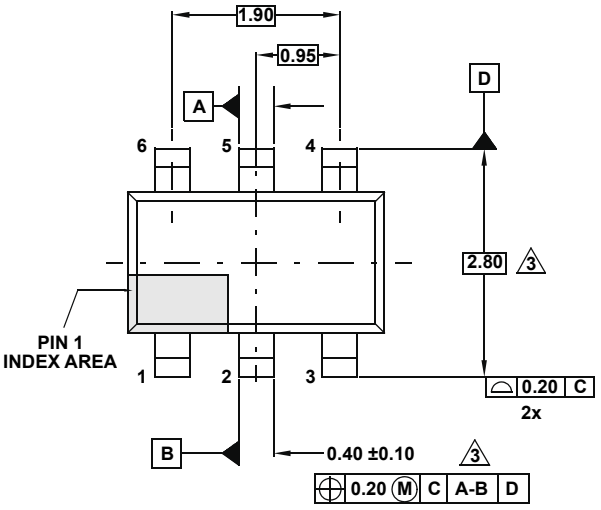


TYPICAL RECOMMENDED LAND PATTERN

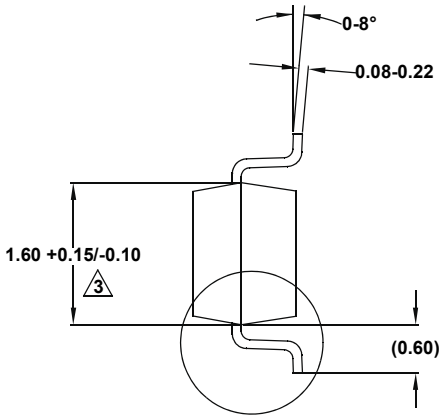
NOTES:

11. Dimensioning and tolerancing per ANSI Y14.5M-1994.
12. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
13. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
14. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
15. Terminal numbers are shown for reference only.

P6.064
6 Lead Small Outline Transistor Plastic Package
Rev 4, 2/10

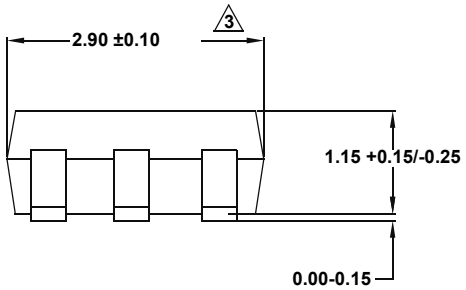


TOP VIEW

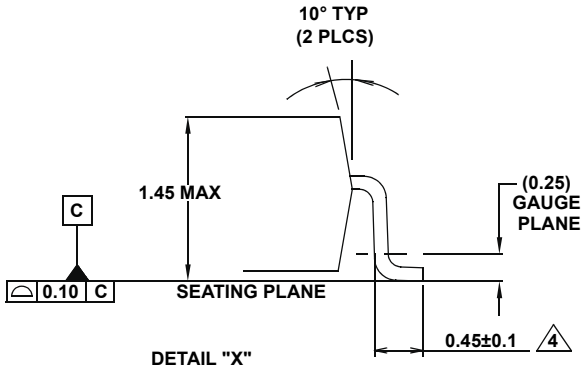


SEE DETAIL X

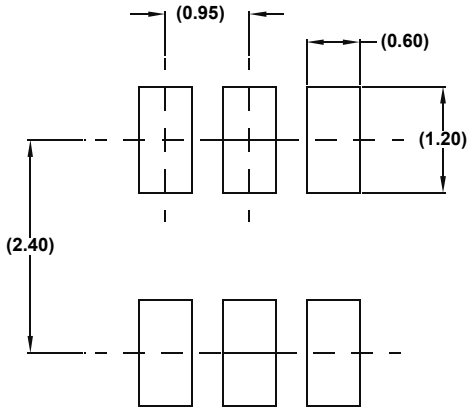
END VIEW



SIDE VIEW



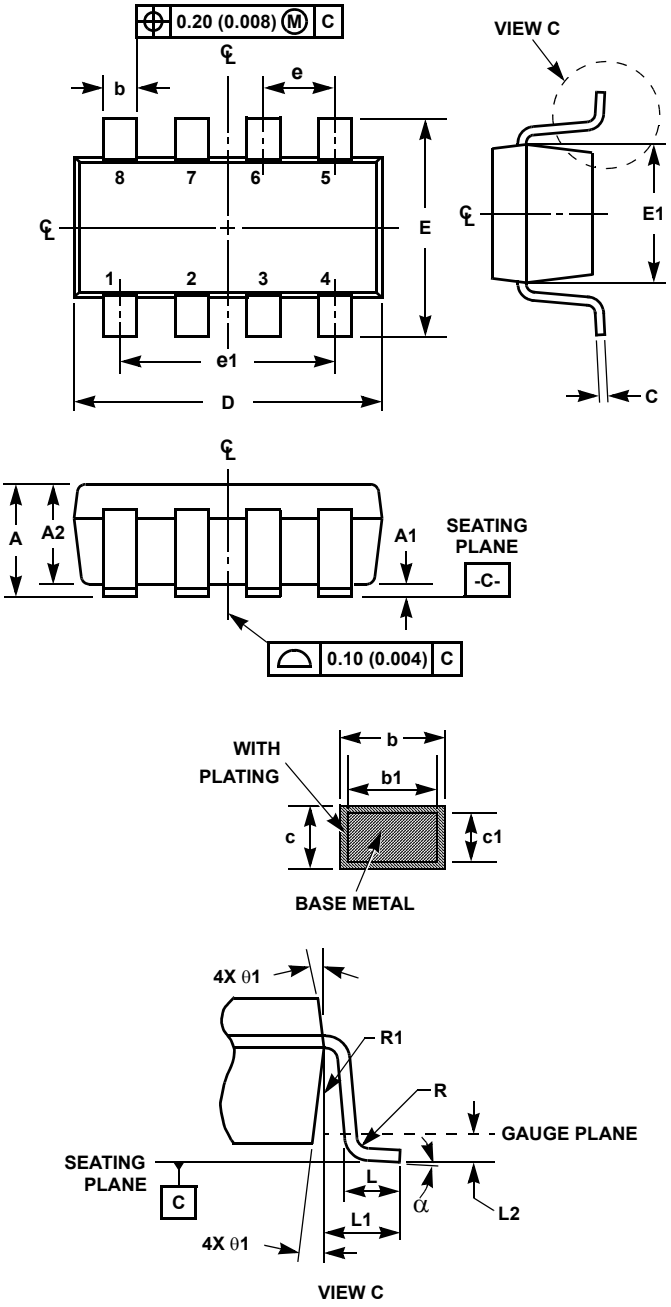
DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Dimension is exclusive of mold flash, protrusions or gate burrs.
4. Foot length is measured at reference to guage plane.
5. Package conforms to JEDEC MO-178AB.



P8.064

8 Lead Small Outline Transistor Plastic Package (SOT23-8)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.036	0.057	0.90	1.45	-
A1	0.000	0.0059	0.00	0.15	-
A2	0.036	0.051	0.90	1.30	-
b	0.009	0.015	0.22	0.38	-
b1	0.009	0.013	0.22	0.33	
c	0.003	0.009	0.08	0.22	6
c1	0.003	0.008	0.08	0.20	6
D	0.111	0.118	2.80	3.00	3
E	0.103	0.118	2.60	3.00	-
E1	0.060	0.067	1.50	1.70	3
e	0.0256 Ref		0.65 Ref		-
e1	0.0768 Ref		1.95 Ref		-
L	0.014	0.022	0.35	0.55	4
L1	0.024 Ref.		0.60 Ref.		
L2	0.010 Ref.		0.25 Ref.		
N	8		8		5
R	0.004	-	0.10	-	
R1	0.004	0.010	0.10	0.25	
α	0^o	8^o	0^o	8^o	-

Rev. 2 9/03

NOTES:

19. Dimensioning and tolerance per ASME Y14.5M-1994.
20. Package conforms to EIAJ SC-74 and JEDEC MO178BA.
21. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
22. Footlength L measured at reference to gauge plane.
23. “N” is the number of terminal positions.
24. These Dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
25. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only