ISL85009EVAL1Z

Evaluation Board User Guide

UG112
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Description

The ISL85009 is a 3.8V to 18V input, 9A synchronous buck regulator for applications with input voltage from multi-cell batteries or regulated 5V and 12V power rails. The device also provides an integrated bootstrap diode for the high-side gate driver to reduce the external parts count. The ISL85009EVAL1Z platform allows quick evaluation of the high-performance features of the ISL85009 buck regulator.

Specifications

This board has been configured and optimized for the following operating conditions:

- Input voltage range from 4.5V to 18V
- 1.8V nominal output voltage
- Up to 9A output current capability
- Default internally set to 600kHz switching frequency
- Default internally set to 3ms soft-start
- Operating temperature range: -40°C to +85°C

Key Features

- Switch selectable EN (enabled/disabled)
- Frequency synchronization option
- Jumper selectable mode (DEM/Forced CCM)
- Jumper selectable OCP mode (Hiccup/Latch-Off)
- Jumper selectable frequency (600kHz/300kHz)
- Connectors and test points for easy probing
- Compact design

Related Literature

- For a full list of related documents, visit our website
  - ISL85009 product page

Ordering Information

PART NUMBER	DESCRIPTION
ISL85009EVAL1Z	Evaluation board for ISL85009

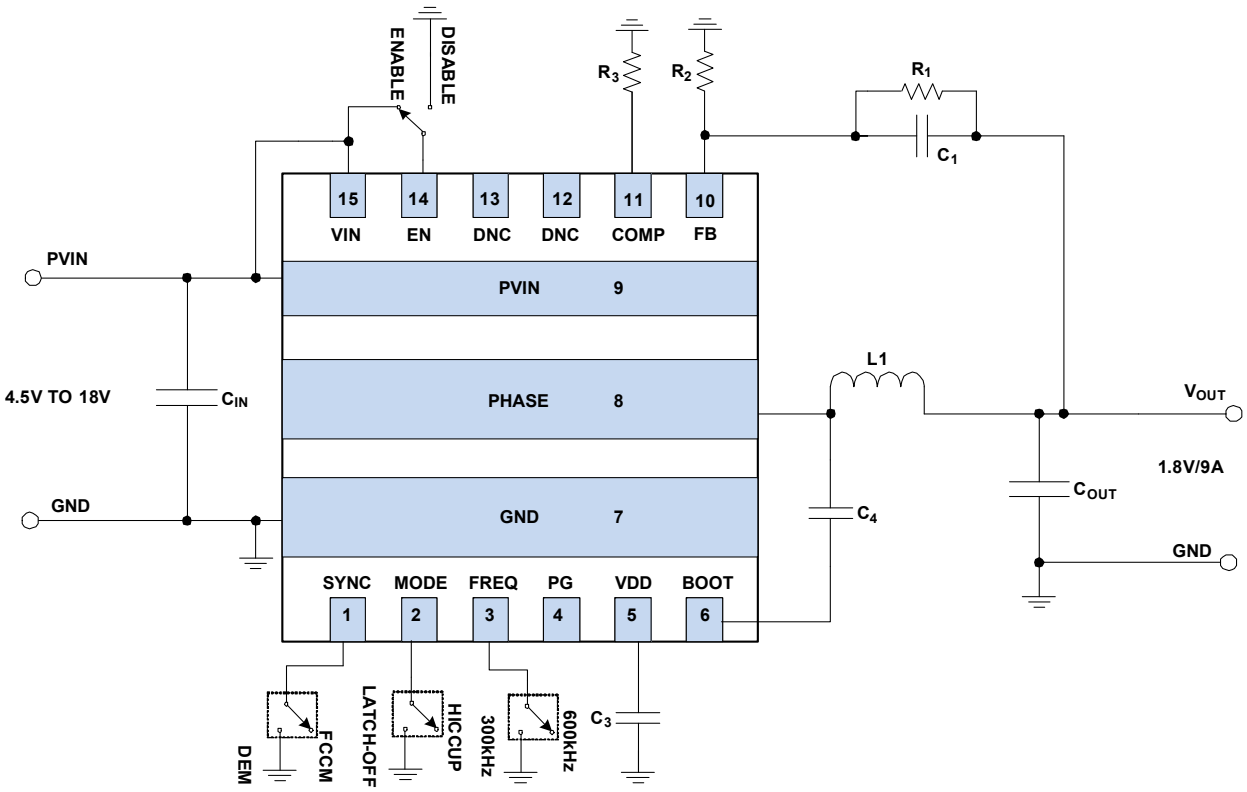

FIGURE 1. BLOCK DIAGRAM

Connector and Test Point Descriptions

The ISL85009EVAL1Z evaluation board includes I/O connectors and test points as shown in Table 1.

TABLE 1. CONNECTORS AND TEST POINTS

REFERENCE DESIGNATOR	DESCRIPTION
J1	Input voltage positive connection
J2	Output voltage positive connection
J3	Input voltage return connection
J4	Output voltage return connection
J6	Two-position socket connector for PHASE to GND test
J7	Two-position socket connector for VOUT to GND test
PVIN	PVIN positive test point
GND	GND test point
VIN	VIN positive test point
VOUT	Output voltage positive test point
SYNC	External synchronization clock connection
EN	Enable test point
VDD	Internal LDO output test point
PG	Power-good output

Selection Switch and Jumper Descriptions

- Switch SW5 (Enable)
  The switch enables and disables the ISL85009:
  - When the switch is in the ON position, ISL85009 enabled.
  - When the switch is in the OFF position, ISL85009 disabled.
- Jumper J9
  The jumper provides selection of different operating modes detailed as following:
  - When the jumper is in the FCCM position, the ISL85009 operates in Forced CCM.
  - When the jumper is in the DEM position, the ISL85009 operates in Diode Emulation mode and enables automatic transition from CCM to DCM at light-load conditions.
- Jumper J10 sets the switching frequency at either 600kHz or 300kHz.
- Jumper J11 sets the OCP scheme in either Hiccup mode or Latch-Off mode.

Quick Setup Guide

Refer to the following instructions to configure and power-up the board for proper operation.

1. Set the power supply voltage to 12V and turn off the power supply. Connect the positive output of the power supply to J1 (PVIN) and the negative output to J3 (GND).
2. Connect an electronic load to J2 (VOUT) for the positive connection and J4 (GND) for the negative connection.
3. Measure the output voltage (test points VOUT and GND) with the voltmeter.
4. Place scope probes on VOUT test point (J7) and other test points of interest.
5. Toggle selection switch SW5 to ON position.
6. Set the load current to be 0.1A and turn on the power supply. The output voltage should be in regulation with a nominal 1.8V output.
7. Slowly increase the load up to 9A while monitoring the output voltage, which should remain in regulation with a nominal 1.8V output.
8. Slowly sweep VIN from 4.5V to 18V. The output voltage should remain in regulation with a nominal 1.8V output.
9. Decrease the input voltage to 0V to shut down the regulator.

Frequency Synchronization

The ISL85009 can be synchronized to an external clock with frequency ranges from 100kHz to 1MHz by applying the external clock to test point SYNC on the ISL85009EVAL1Z evaluation board. The external clock should meet the specifications of pulse width and voltage level described in the ISL85009 datasheet.

Evaluating Other Output Voltages

The ISL85009EVAL1Z has a nominal 1.8V output voltage. The output voltage is programmable by an external resistor divider formed by R_1 and R_2 as shown in Figure 1 on page 1. R_1 is usually chosen first, then the value for R_2 can be calculated based on R_1 and the desired output voltage using Equation 1.

$$R_2 = \frac{R_1 \cdot 0.6V}{V_{OUT} - 0.6V} \quad \text{(EQ. 1)}$$

PCB Layout Considerations

The PCB layout is critical for proper operation of the ISL85009. The following guidelines should be followed to achieve good performance.

1. Use a multilayer PCB structure to achieve optimized performance. A four-layer PCB is recommended for this design.
2. Use a combination of bulk capacitors and smaller ceramic capacitors with lower ESL for the input capacitors, and place them as close to the IC as possible.
3. Place the VDD decoupling capacitor close to the IC between VDD and GND. A 1µF ceramic capacitor is typically used.
4. Place a bootstrap capacitor close to the IC between the BOOT and PHASE pins. A 0.1µF ceramic capacitor is typically used.
5. Connect the feedback resistor divider between the output capacitor positive terminal and AGND pin of the IC, and place the resistors close to the FB pin of the IC.
6. Connect the GND of the IC to the ground planes underneath using multiple thermal vias to improve thermal performance.

ISL85009EVAL1Z Evaluation Board

FIGURE 2. TOP VIEW

ISL85009EVAL1Z Schematic

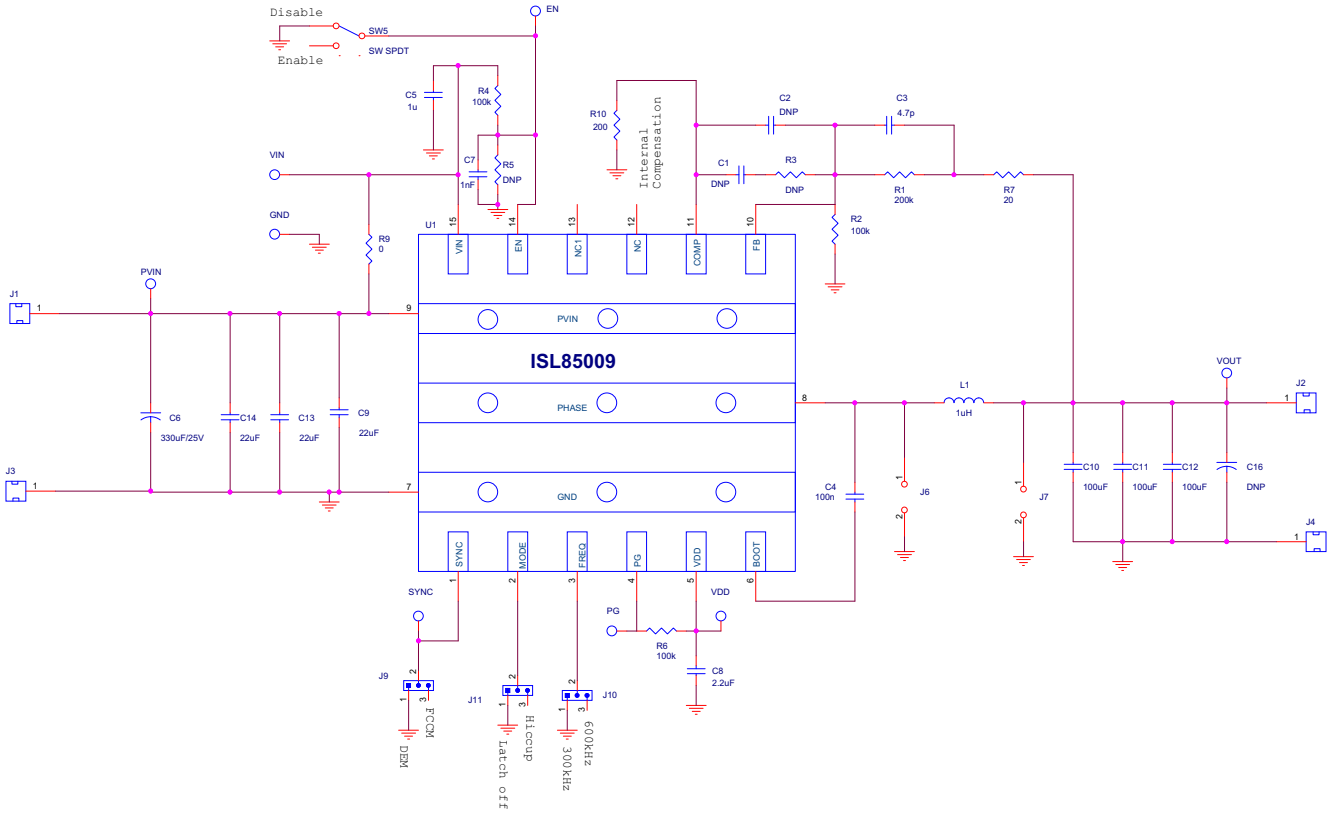

FIGURE 3. SCHEMATIC

Bill of Materials

MANUFACTURER PART	QTY	UNITS	REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURER
ISL85009EVAL1ZREVAPCB	1	ea		PWB-PCB, ISL85009EVAL1Z, REVA, ROHS	IMAGINEERING INC
25SVPF330M	1	ea	C6	CAP-OSCON, SMD, 10mm, 330µF, 25V, 20%, 14mΩ, ROHS	PANASONIC
GRM32ER71E226KE15L	3	ea	C9, C13, C14	CAP, SMD, 1210, 22µF, 25V, 10%, X7R, ROHS	MURATA
C0402X7R500-102KNE	1	ea	C7	CAP, SMD, 0402, 1000pF, 50V, 10%, X7R, ROHS	VENKEL
C1005X7R1H104K	1	ea	C4	CAP, SMD, 0402, 0.1µF, 50V, 10%, X7R, ROHS	TDK
04025A4R7CAT2A	1	ea	C3	CAP, SMD, 0402, 4.7PF, 50V, 0.25pF, NPO, ROHS	AVX
GRM188R61E105KA12D	1	ea	C5	CAP, SMD, 0603, 1µF, 25V, 10%, X5R, ROHS	MURATA
GRM188R71A225KE15D	1	ea	C8	CAP, SMD, 0603, 2.2µF, 10V, 10%, X7R, ROHS	MURATA
GRM31CR60J107ME39L	3	ea	C10, C11, C12	CAP, SMD, 1206, 100µF, 6.3V, 20%, X5R, ROHS	MURATA
7443340100	1	ea	L1	COIL-PWR INDUCTOR, SMD, 8.4x7.9, 1.0µH, 20%, 17A, WW, ROHS	WURTH ELECTRONICS
111-0702-001	2	ea	J1, J2	CONN-GEN, BIND.POST, INSUL-RED, THMBNUT-GND	JOHNSON COMPONENTS
111-0703-001	2	ea	J3, J4	CONN-GEN, BIND.POST, INSUL-BLK, THMBNUT-GND	JOHNSON COMPONENTS
5002	8	ea	VDD, SYNC, PG, EN, GND, VIN, PVIN, VOUT	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	KEYSTONE
68000-236HLF	3	ea	J9, J10, J11	CONN-HEADER, 1x3, BREAKAWY 1x36, 2.54mm, ROHS	BERG/FCI
929950-00	1	ea	Jumper	CONN-JUMPER, SHORTING, 2PIN, BLK, OPEN TOP, 2.54mmPITCH, ROHS	3M
ISL85009FRZ	1	ea	U1	IC-9A BUCK REGULATOR, 15P, TDFN 3.5x3.5, ROHS	INTERSIL
ERJ2RKF20R0	1	ea	R7	RES, SMD, 0402, 20Ω, 1/16W, 1%, TF, ROHS	PANASONIC
CR0402-16W-00T	1	ea	R9	RES, SMD, 0402, 0Ω, 1/16W, 5%, TF, ROHS	VENKEL
ERJ2RKF1003	3	ea	R2, R4, R6	RES, SMD, 0402, 100k, 1/16W, 1%, TF, ROHS	PANASONIC
ERJ-2RKF2000X	1	ea	R10	RES, SMD, 0402, 200Ω, 1/16W, 1%, TF, ROHS	PANASONIC
MCR01MZPF2003	1	ea	R1	RES, SMD, 0402, 200k, 1/16W, 1%, TF, ROHS	ROHM
	0	ea	R3, R5	RES, SMD, 0402, DNP, DNP, DNP, TF, ROHS	
GT11MSCBE	1	ea	SW5	SWITCH-TOGGLE, SMD, 6PIN, SPDT, 2POS, ON-NONE-ON, ROHS	ITT INDUSTRIES/C&K DIVISION
PMSSS 440 0025 PH	4	ea	Four corners	SCREW, 4-40x1/4in, PHILLIPS, PANHEAD, STAINLESS, ROHS	BUILDING FASTENERS
2204	4	ea	Four corners	STANDOFF, 4-40x3/4in, F/F, HEX, ALUMINUM, 0.25 OD, ROHS	KEYSTONE
212403-013	1	ea	Place assy in bag	BAG, STATIC, 5x8, ZIPLOC, ROHS	INTERSIL
310-87-102-41-001101	2	ea	J6, J7	CONN-SOCKET STRIP, TH, 2P, 2.54mm PITCH, ROHS	PRECI-DIP
	0	ea	C1, C2, C16	DO NOT POPULATE OR PURCHASE	
LABEL-DATE CODE	1	ea	AFFIX TO BACK OF PCB	LABEL-DATE CODE_LINE 1: YRWK/REV#, LINE 2: BOM NAME	INTERSIL

ISL85009EVAL1Z PCB Layout

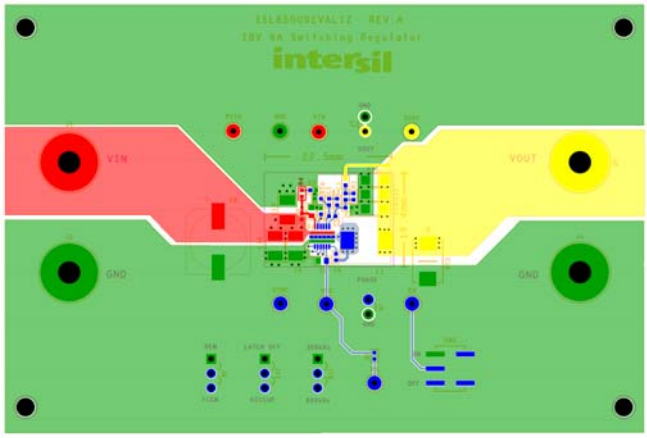

FIGURE 4. TOP LAYER

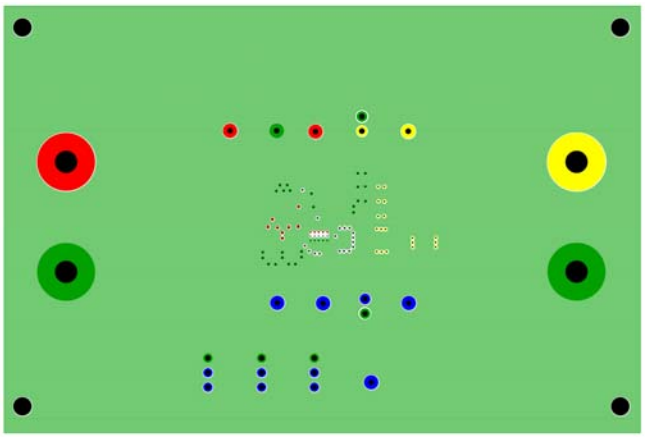

FIGURE 5. LAYER 2

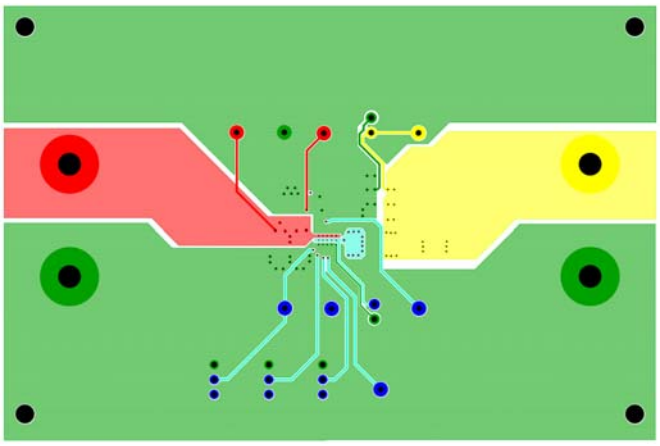

FIGURE 6. LAYER 3

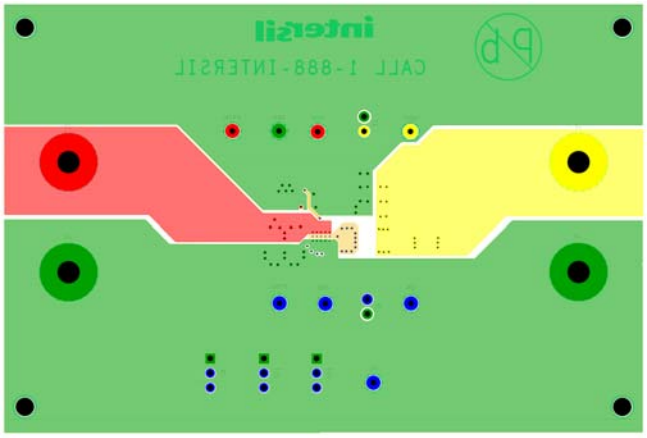

FIGURE 7. BOTTOM LAYER