ISL89163, ISL89164, ISL89165

High Speed, Dual Channel, 6A, Power MOSFET Driver with Enable Inputs

The ISL89163, ISL89164, and ISL89165 are high-speed, 6A, dual channel MOSFET drivers with enable inputs.

Precision thresholds on all logic inputs allow the use of external RC circuits to generate accurate and stable time delays on both the main channel inputs, INA and INB, and the enable inputs, ENA and ENB. The precision delays capable of these precise logic thresholds make these parts valuable for dead time control and synchronous rectifiers. Note, the enable and input logic inputs can be interchanged for alternate logic implementations.

Three input logic thresholds are available:

- 3.3V (CMOS)
- 5.0V (CMOS or TTL compatible)
- CMOS thresholds that are proportional to V_{DD}

At high switching frequencies, these MOSFET drivers use a minimal amount of internal bias currents. Separate, non-overlapping drive circuits are used to drive each CMOS output FET to prevent shoot-through currents in the output stage.

The start-up sequence is designed to prevent unexpected glitches when V_{DD} is being turned on or turned off. When V_{DD} < ~1V, an internal 10kΩ resistor between the output and ground helps to keep the output voltage low. When ~1V < V_{DD} < UV, both outputs are driven low with significantly low resistance as the logic inputs are ignored, which ensures that the driven FETs are off. When V_{DD} > UVLO, and after a short delay, the outputs begin to respond to the logic inputs.

Features

- Dual output, 6A peak currents, can be paralleled
- Dual AND-ed input logic, (input and enable)
- Typical ON-resistance <1Ω
- Specified Miller plateau drive currents
- Very low thermal impedance (θ_{JC} = 3°C/W)
- Hysteretic Input logic levels for 3.3V CMOS, 5V CMOS, TTL, and Logic levels proportional to V_{DD}
- Precision threshold inputs for time delays with external RC components
- 20ns rise and fall time driving a 10nF load.

Applications

- Synchronous Rectifier (SR) driver
- Switch mode power supplies
- Motor drives, Class D amplifiers, UPS, inverters
- Pulse transformer driver
- Clock/line driver

Related Literature

For a full list of related documents, visit our website:

- ISL89163, ISL89164, ISL89165 device pages

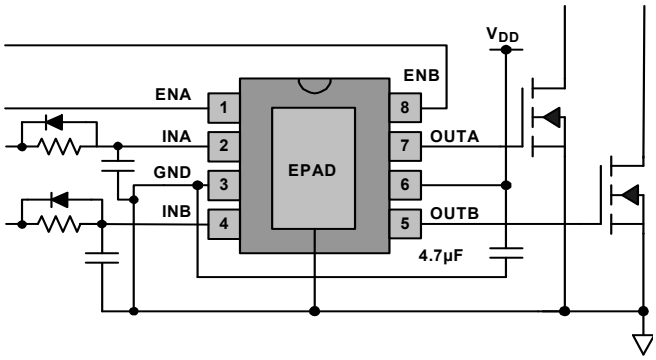

Figure 1. Typical Application

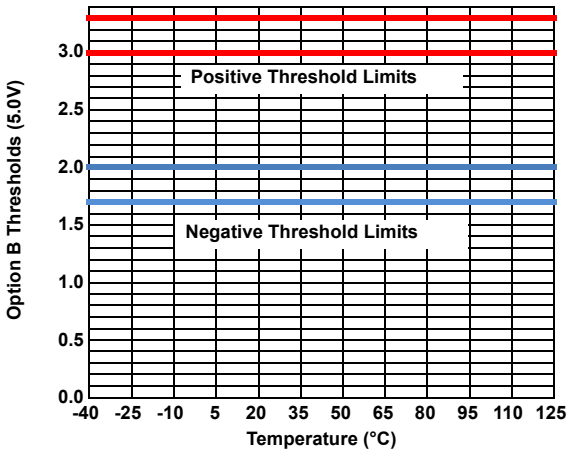

Figure 2. Temperature Stable Logic Thresholds

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1. Overview

1.1 Block Diagram

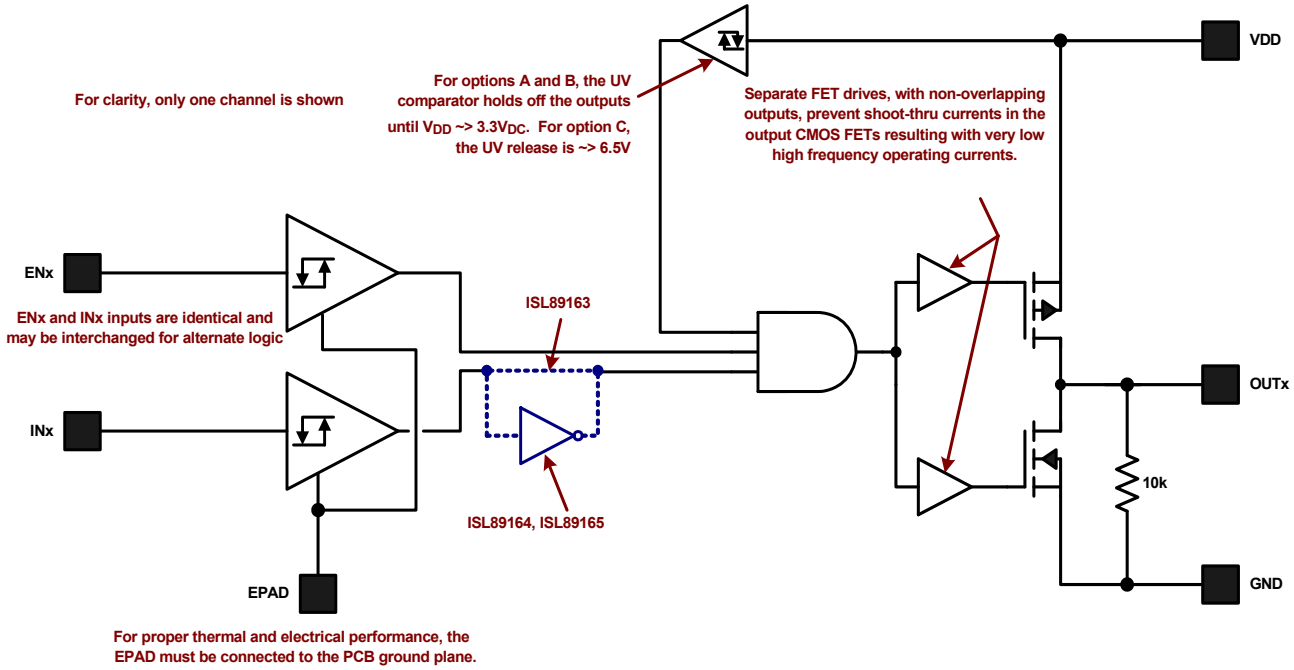


Figure 3. Block Diagram

1.2 Ordering Information

Part Number (Notes 2, 3, 4)	Part Marking	Temp Range (°C)	Input Configuration	Input Logic (V)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
ISL89163FRTAZ	163A	-40 to +125	Non-inverting	3.3	-	8 Ld 3x3 TDFN	L8.3x3I
ISL89163FRTAZ-T	163A	-40 to +125		3.3	6k	8 Ld 3x3 TDFN	L8.3x3I
ISL89163FRTBZ	163B	-40 to +125		5.0	-	8 Ld 3x3 TDFN	L8.3x3I
ISL89163FRTBZ-T	163B	-40 to +125		5.0	6k	8 Ld 3x3 TDFN	L8.3x3I
ISL89164FRTAZ	164A	-40 to +125	Inverting	3.3	-	8 Ld 3x3 TDFN	L8.3x3I
ISL89164FRTAZ-T	164A	-40 to +125		3.3	6k	8 Ld 3x3 TDFN	L8.3x3I
ISL89164FRTBZ	164B	-40 to +125		5.0	-	8 Ld 3x3 TDFN	L8.3x3I
ISL89164FRTBZ-T	164B	-40 to +125		5.0	6k	8 Ld 3x3 TDFN	L8.3x3I
ISL89165FRTAZ	165A	-40 to +125	Inverting + Non-inverting	3.3	-	8 Ld 3x3 TDFN	L8.3x3I
ISL89165FRTAZ-T	165A	-40 to +125		3.3	6k	8 Ld 3x3 TDFN	L8.3x3I
ISL89165FRTBZ	165B	-40 to +125		5.0	-	8 Ld 3x3 TDFN	L8.3x3I
ISL89165FRTBZ-T	165B	-40 to +125		5.0	6k	8 Ld 3x3 TDFN	L8.3x3I
ISL89163FBEAZ	89163 FBEAZ	-40 to +125	Non-inverting	3.3	-	8 Ld EPSOIC	M8.15D
ISL89163FBEAZ-T	89163 FBEAZ	-40 to +125		3.3	2.5k	8 Ld EPSOIC	M8.15D
ISL89163FBEBZ	89163 FBEBZ	-40 to +125		5.0	-	8 Ld EPSOIC	M8.15D
ISL89163FBEBZ-T	89163 FBEBZ	-40 to +125		5.0	2.5k	8 Ld EPSOIC	M8.15D
ISL89164FBEAZ	89164 FBEAZ	-40 to +125	Inverting	3.3	-	8 Ld EPSOIC	M8.15D
ISL89164FBEAZ-T	89164 FBEAZ	-40 to +125		3.3	2.5k	8 Ld EPSOIC	M8.15D
ISL89164FBEBZ	89164 FBEBZ	-40 to +125		5.0	-	8 Ld EPSOIC	M8.15D
ISL89164FBEBZ-T	89164 FBEBZ	-40 to +125		5.0	2.5k	8 Ld EPSOIC	M8.15D

Part Number (Notes 2, 3, 4)	Part Marking	Temp Range (°C)	Input Configuration	Input Logic (V)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
ISL89165FBEAZ	89165 FBEAZ	-40 to +125	Inverting + Non-inverting	3.3V	-	8 Ld EPSOIC	M8.15D
ISL89165FBEAZ -T	89165 FBEAZ	-40 to +125		3.3V	2.5k	8 Ld EPSOIC	M8.15D
ISL89165FBEBZ	89165 FBEBZ	-40 to +125		5.0V	-	8 Ld EPSOIC	M8.15D
ISL89165FBEBZ-T	89165 FBEBZ	-40 to +125		5.0V	2.5k	8 Ld EPSOIC	M8.15D

Notes:

1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. Input Logic Voltage: A = 3.3V, B = 5.0V.
4. For Moisture Sensitivity Level (MSL), see the ISL89163, ISL89164, ISL89165 device pages. For more information about MSL, see TB363.

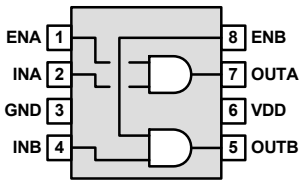
Table 1. Key Differences Between Family of Parts

Part Number	I/O Pins					
	ENA	ENB	INA	INB	OUTA	OUTB
ISL89163	NINV	NINV	NINV	NINV	NINV	NINV
ISL89164	NINV	NINV	INV	INV	NINV	NINV
ISL89165	NINV	NINV	INV	NINV	NINV	NINV

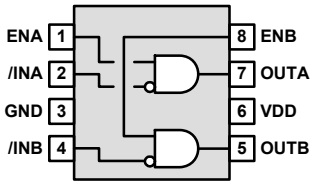
Note: INV: Inverting Input, NINV: Non-inverting input.

1.3 Pin Configurations

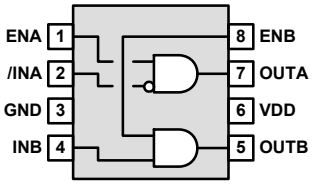
ISL89163FR, ISL89163FB
(8 Ld TDFN, EPSOIC)
Top View



ISL89164FR, ISL89164FB
(8 Ld TDFN, EPSOIC)
Top View



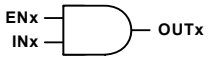
ISL89165FR, ISL89165FB
(8 Ld TDFN, EPSOIC)
Top View



1.4 Pin Descriptions

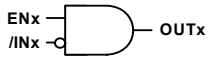
Pin Number	Symbol	Description (See Table 2)
1	ENA	Channel A enable, 0V to VDD
2	INA, /INA	Channel A input, 0V to VDD
3	GND	Power Ground, 0V
4	INB, /INB	Channel B enable, 0V to VDD
5	OUTB	Channel B output
6	VDD	Power input, 4.5V to 16V
7	OUTA	Channel A output, 0V to VDD
8	ENB	Channel B enable, 0V to VDD
	EPAD	Power Ground, 0V

Table 2. Truth Table for Logic Polarities



Non-Inverting

UV	ENx*	INx*	OUTx*
0	x	x	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1



Inverting

UV	ENx*	/INx*	OUTx*
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

*Substitute A or B for x

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Supply Voltage, VDD Relative to GND	-0.3	18	V
Logic Inputs (INA, INB, ENA, ENB)	GND - 0.3	V_{DD} + 0.3	V
Outputs (OUTA, OUTB)	GND - 0.3	V_{DD} + 0.3	V
Average Output Current (Note 5)		150	mA
ESD Rating	**Value**		**Unit**
Human Body Model Class 2 (Tested per JESD22-A114E)	2		kV
Machine Model Class B (Tested per JESD22-A115-A)	200		V
Charged Device Model Class IV	1		kV
Latch-Up (Tested per JESD-78B; Class 2, Level A) Output Current	500		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Note:

5. The average output current, when driving a power MOSFET or similar capacitive load, is the average of the rectified output current. The peak output currents of this driver are self limiting by trans conductance or $r_{DS(ON)}$ and do not required any external components to minimize the peaks. If the output is driving a non-capacitive load, such as an LED, maximum output current must be limited by external means to less than the specified absolute maximum.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld TDFN Package (Notes 6, 7)	44	3
8 Ld EPSOIC Package (Notes 6, 7)	42	3

Notes:

6. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See TB379.
7. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Max Power Dissipation at +25°C in Free Air		2.27	W
Max Power Dissipation at +25°C with Copper Plane		33.3	W
Storage Temperature Range	-65	+150	°C
Maximum Operating Junction Temperature Range	-40	+150	°C
Pb-Free Reflow Profile	see TB493		

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Junction Temperature	-40	+125	°C
Options A and B			
Supply Voltage, VDD Relative to GND	4.5	16	V
Logic Inputs (INA, INB, ENA, ENB)	0	V_{DD}	V
Outputs (OUTA, OUTB)	0	V_{DD}	V
Option C			
Supply Voltage, VDD Relative to GND	7.5	16	V
Logic Inputs (INA, INB, ENA, ENB)	0	V_{DD}	V
Outputs (OUTA, OUTB)	0	V_{DD}	V

2.4 Electrical Specifications

2.4.1 DC Electrical Specifications

V_{DD} = 12V, GND = 0V, No load on OUTA or OUTB, unless otherwise specified. **Boldface limits apply across the operating junction temperature range, -40°C to +125°C.**

Parameters	Symbol	Test Conditions	T_J = +25°C			T_J = -40°C to +125°C		Unit
			Min	Typ	Max	Min (Note 8)	Max (Note 8)	
Power Supply								
Voltage Range (Option A and B)	V_{DD}					**4.5**	**16**	V
Voltage Range (Option C)	V_{DD}					**7.5**	**16**	V
V_{DD} Quiescent Current	I_{DD}	ENx = INx = GND		5				mA
		INA = INB = 1MHz, square wave		25				mA
Undervoltage								
VDD Undervoltage Lockout (Options A and B) (Note 12, Figure 10)	V_{UV}	ENA = ENB = True INA = INB = True		3.3				V
VDD Undervoltage Lockout (Option C) (Note 12, Figure 10)	V_{UV}	ENA = ENB = True INA = INB = True (Note 9)		6.5				V
Hysteresis (Option A or B)				~25				mV
Hysteresis (Option C)				~0.95				V
Inputs								
Input Range for INA, INB, ENA, ENB	V_{IN}	Option A, B, or C				GND	V_{DD}	V
Logic 0 Threshold for INA, INB, ENA, ENB (Note 11)	V_{IL}	Option A, nominally 37% x 3.3V		1.22		**1.12**	**1.32**	V
		Option B, nominally 37% x 5.0V		1.85		**1.70**	**2.00**	V
		Option C, nominally 20% x 12V (Note 9)		2.4		**2.00**	**2.76**	V
Logic 1 Threshold for INA, INB, ENA, ENB (Note 11)	V_{IH}	Option A, nominally 63% x 3.3V		2.08		**1.98**	**2.18**	V
		Option B, nominally 63% x 5.0V		3.15		**3.00**	**3.30**	V
		Option C, nominally 80% x 12V (Note 9)		9.6		**9.24**	**9.96**	V
Input Capacitance of INA, INB, ENA, ENB (Note 10)	C_{IN}			2				pF
Input Bias Current for INA, INB, ENA, ENB	I_{IN}	GND < V_{IN} < V_{DD}				**-10**	**+10**	µA
Outputs								
High Level Output Voltage	V_{OHA} V_{OHB}					**V_{DD} - 0.1**	**V_{DD}**	V

V_{DD} = 12V, GND = 0V, No load on OUTA or OUTB, unless otherwise specified. **Boldface limits apply across the operating junction temperature range, -40°C to +125°C. (Continued)**

Parameters	Symbol	Test Conditions	T_J = +25°C			T_J = -40°C to +125°C		Unit
			Min	Typ	Max	Min (Note 8)	Max (Note 8)	
Low Level Output Voltage	V_{OLA} V_{OLB}					**GND**	**GND + 0.1**	V
Peak Output Source Current	I_O	V_O (initial) = 0V, C_{LOAD} = 10nF		-6				A
Peak Output Sink Current	I_O	V_O (initial) = 12V, C_{LOAD} = 10nF		+6				A

Notes:

8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
9. The nominal 20% and 80% thresholds for option C are valid for any value within the specified range of VDD.
10. This parameter is taken from the simulation models for the input FET. The actual capacitance on this input is dominated by the PCB parasitic capacitance.
11. The true state input voltage for the non-inverted inputs is greater than the Logic 1 threshold voltage. The true state input voltage for the inverted inputs is less than the Logic 0 threshold voltage.
12. A 400µs delay further inhibits the release of the output state when the UV positive going threshold is crossed. See Figure 10 on page 10.

2.5 AC Electrical Specifications

V_{DD} = 12V, GND = 0V, No Load on OUTA or OUTB, unless otherwise specified. **Boldface limits apply across the operating junction temperature range, -40°C to +125°C.**

Parameters	Symbol	Test Conditions	T_J = +25°C			T_J = -40°C to +125°C		Unit
			Min	Typ	Max	Min	Max	
Output Rise Time (see Figure 5)	t_R	C_{LOAD} = 10nF, 10% to 90%		20			**40**	ns
Output Fall Time (see Figure 5)	t_F	C_{LOAD} = 10nF, 90% to 10%		20			**40**	ns
Output Rising Edge Propagation Delay for Non-Inverting Inputs (Note 13) (see Figure 4)	t_{RDLYn}	V_{DD} = 12V Options A and B		25			**50**	ns
		V_{DD} = 8V Option C		25			**50**	ns
Output Rising Edge Propagation Delay with Inverting Inputs (Note 13) (see Figure 4)	t_{RDLYi}	V_{DD} = 12V Options A and B		25			**50**	ns
		V_{DD} = 8V Option C		25			**50**	ns
Output Falling Edge Propagation Delay with Non-Inverting Inputs (Note 13) (see Figure 4)	t_{FDLYn}	V_{DD} = 12V Options A and B		25			**50**	ns
		V_{DD} = 8V Option C		25			**50**	ns
Output Falling Edge Propagation Delay with Inverting Inputs (Note 13) (see Figure 4)	t_{FDLYi}	V_{DD} = 12V Options A and B		25			**50**	ns
		V_{DD} = 8V Option C		25			**50**	ns
Rising Propagation Matching (see Figure 4)	t_{RM}	No load		<1				ns
Falling Propagation Matching (see Figure 4)	t_{FM}	No load		<1				ns
Miller Plateau Sink Current (See Test Circuit Figure 6)	$-I_{MP}$	V_{DD} = 10V, V_{MILLER} = 5V	-	6	-	-	-	A
	$-I_{MP}$	V_{DD} = 10V, V_{MILLER} = 3V	-	4.7	-	-	-	A
	$-I_{MP}$	V_{DD} = 10V, V_{MILLER}= 2V	-	3.7	-	-	-	A
Miller Plateau Source Current (See Test Circuit Figure 7)	I_{MP}	V_{DD} = 10V, V_{MILLER} = 5V	-	5.2	-	-	-	A
	I_{MP}	V_{DD} = 10V, V_{MILLER} = 3V	-	5.8	-	-	-	A
	I_{MP}	V_{DD} = 10V, V_{MILLER} = 2V	-	6.9	-	-	-	A
Turn-On Delay (Note 12, Figure 10)	t_{on_delay}	see Figure 10		400				µs

Note:

13. Propagation delays for Option C are typically the same for the recommended operating range (7.5V ≤ V_{DD} ≤ 16V).

2.6 Test Waveforms and Circuits

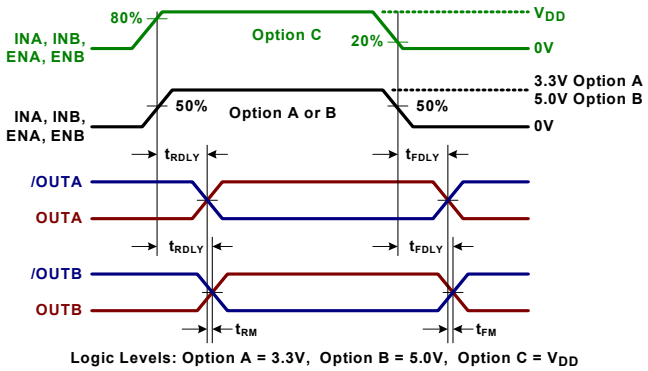


Figure 4. Prop Delays and Matching

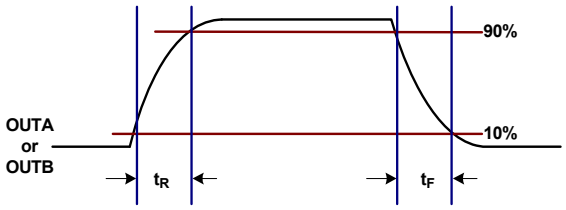


Figure 5. Rise/Fall Times

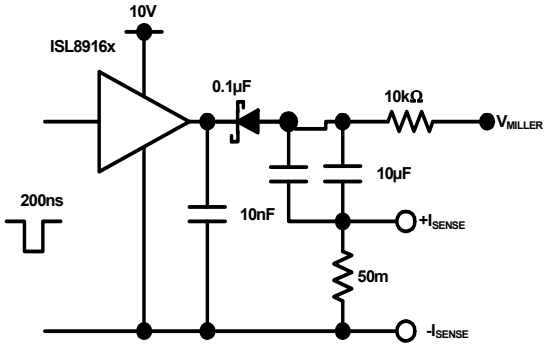


Figure 6. Miller Plateau Sink Current Test Circuit

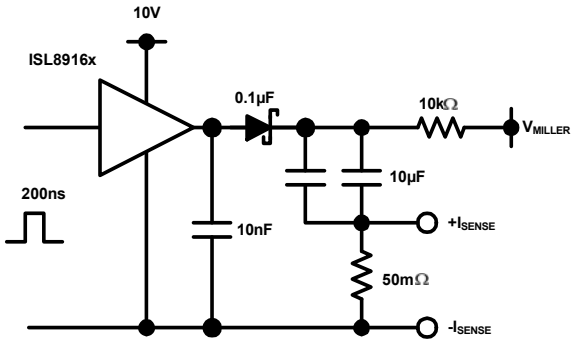


Figure 7. Miller Plateau Source Current Test Circuit

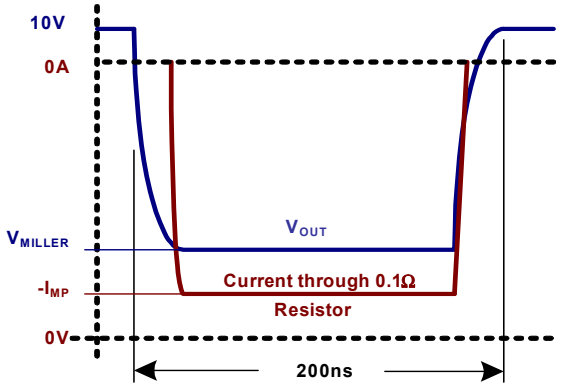


Figure 8. Miller Plateau Sink Current

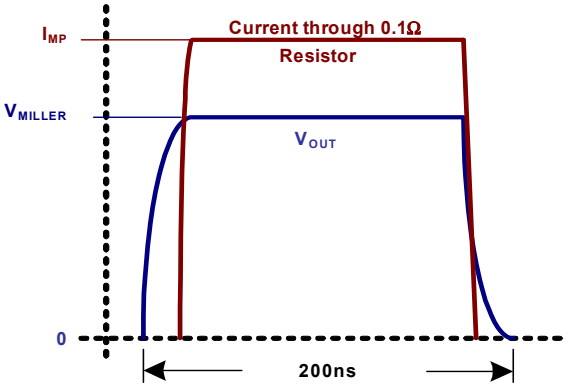


Figure 9. Miller Plateau Source Current

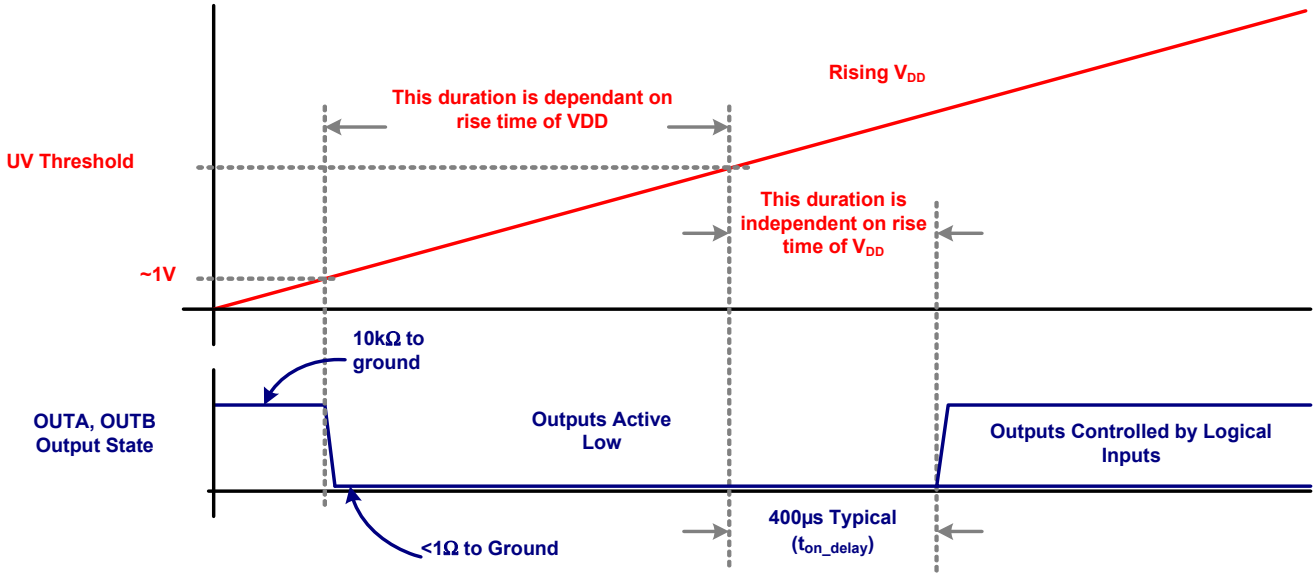


Figure 10. Start-Up Output Characteristic

3. Typical Performance Curves

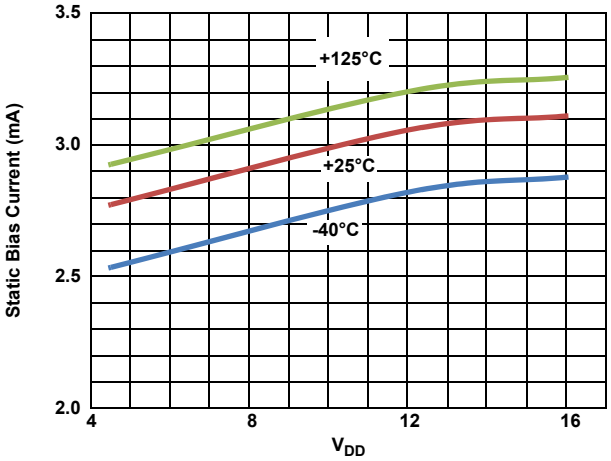


Figure 11. I_{DD} vs V_{DD} (STATIC)

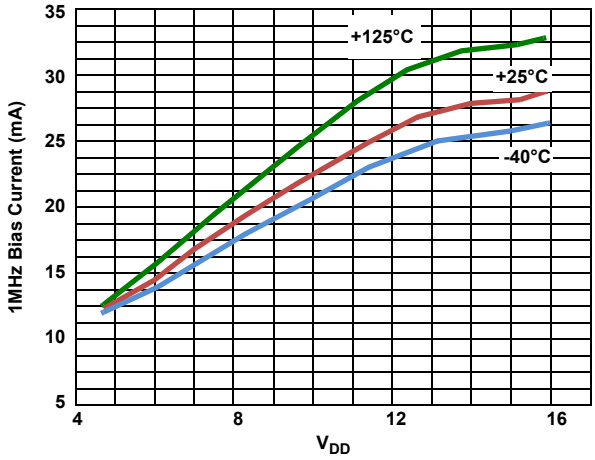


Figure 12. I_{DD} vs V_{DD} (1MHz)

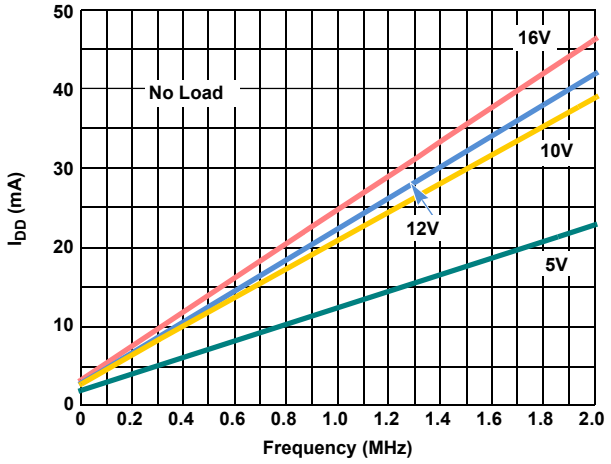


Figure 13. I_{DD} vs Frequency (+25°C)

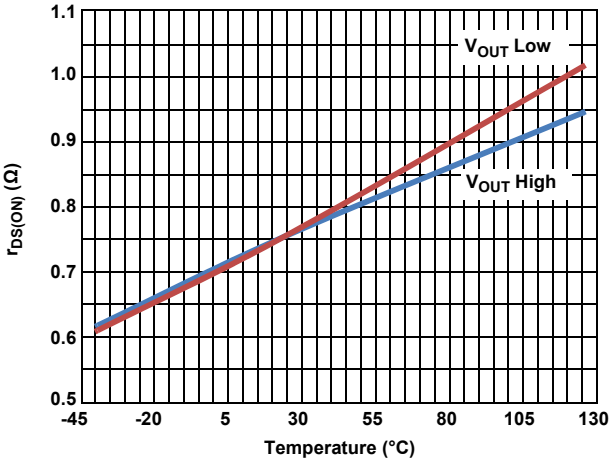


Figure 14. $r_{DS(ON)}$ vs Temperature

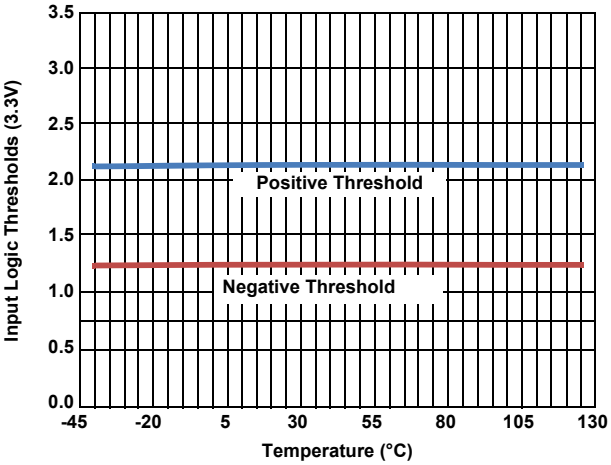


Figure 15. Option A Thresholds

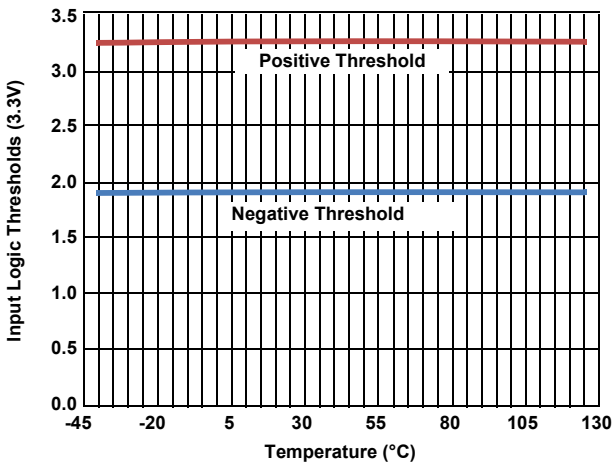


Figure 16. Option B Thresholds

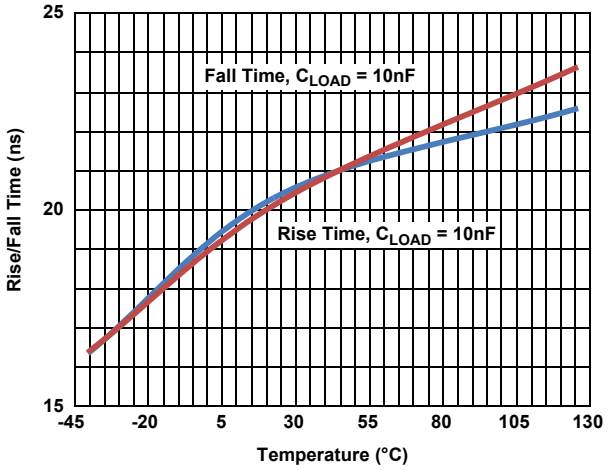


Figure 17. Output Rise/Fall Time

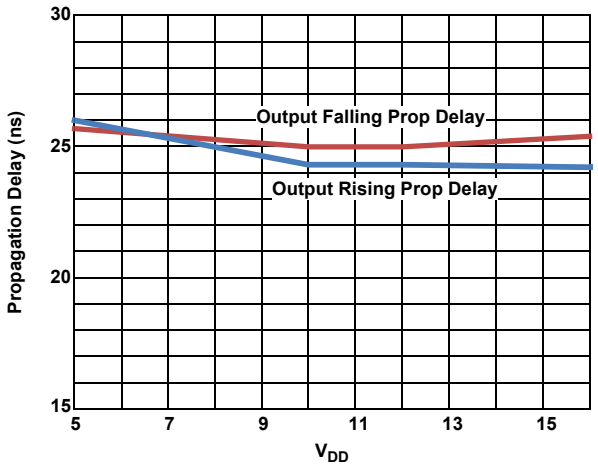


Figure 18. Propagation Delay vs V_{DD}

4. Functional Description

The ISL89163, ISL89164, ISL89165 MOSFET drivers incorporate several features optimized for Synchronous Rectifier (SR) driver applications including precision input logic thresholds, enable inputs, undervoltage lockout, and high-amplitude output drive currents.

The precision input thresholds facilitate the use of an external RC network to delay the rising or falling propagation of the driver output; this feature is useful for adjusting when the SRs turn on relative to the primary side FETs. In a similar manner, these drivers can also be used to control the turn-on/off timing of the primary side FETs.

The enable inputs (ENA, ENB) are used to emulate diode operation of the SRs by disabling the driver output, as necessary, to prevent negative currents in the output filter inductors. One example is turning off the SRs when the power supply output is turned off, which prevents the output capacitor from being discharged through the output inductor. If this is allowed to happen, the voltage across the output capacitor rings negative possibly damaging the capacitor (if it is polarized) and probably damaging the load. Another example is preventing circulating currents between paralleled power supplies during no or light-load conditions. During light-load conditions (especially when active load sharing is not active), energy is transferred from the paralleled power supply that has a higher voltage to the paralleled power supply with the lower voltage. Consequently, the energy that is absorbed by the low voltage output transfers to the primary side causing the bus voltage to increase until the primary side is damaged by excessive voltage.

The start-up sequence for input threshold Options A, B, and C prevents unexpected glitches when V_{DD} is being turned on or turned off. When V_{DD} < ~1V, an internal 10kΩ resistor connected between the output and ground helps keep the gate voltage close to ground. When ~1V < V_{DD} < UV, both outputs are driven low while ignoring the logic inputs. This low state has the same current sinking capacity as during normal operation, and it ensures that the driven FETs are held off even if there is a switching voltage on the drains that can inject charge into the gates using the Miller capacitance. When V_{DD} > UVLO, and after a 400µs delay, the outputs now respond to the logic inputs. See Figure 10 for complete details.

For the negative transition of V_{DD} through the UV lockout voltage, the outputs of input threshold Options A or B are active low when V_{DD} < ~3.2V_{DC} regardless of the input logic states. Similarly, the C option outputs are active low when V_{DD} < ~6.5V_{DC}.

5. Application Information

5.1 Precision Thresholds for Time Delays

Three input logic voltage levels are supported by the ISL89163, ISL89164, ISL89165. Option A uses 3.3V logic, Option B uses 5.0V logic, and Option C uses higher voltage logic when it is desired to have voltage thresholds that are proportional to V_{DD}. The A and B options have nominal thresholds that are 37% and 63% of 3.3V and 5.0V, respectively and the C option is 20% and 80% of V_{DD}.

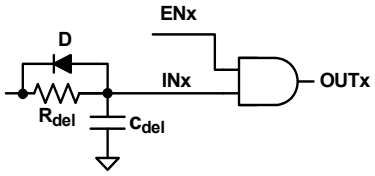


Figure 19. Delay Using RCD Network

In Figure 19, R_{del} and C_{del} delay the rising edge of the input signal. For the falling edge of the input signal, the diode shorts out the resistor resulting in a minimal falling edge delay.

The 37% and 63% thresholds of Options A and B were chosen to simplify the calculations for the desired time delays. When using an RC circuit to generate a time delay, the delay is simply T (secs) = R (ohms) x C (farads). Note: The equation only applies if the input logic voltage is matched to the 3.3V or 5V threshold options. If the logic high amplitude is not equal to 3.3V or 5V, the equations shown in Equation 1 can be used for more precise delay calculations.

(EQ. 1)

$V_H = 10V$ High level of the logic signal into the RC

$V_{thres} = 63\% \times 5V$ Positive going threshold for 5V logic (B option)

$V_L = .3V$ Low level of the logic signal into the RC

$R_{del} = 100\Omega$ Timing values

$C_{del} = 1nF$

$$t_{del} = -R_{del} C_{del} \times \ln\left(\frac{V_L - V_{thres}}{V_H - V_L} + 1\right)$$

$t_{del} = 34.788\ ns$ nominal delay time for this example

In this example, the high logic voltage is 10V, the positive threshold is 63% of 5V and the low level logic is 0.3V. Note the rising edge propagation delay of the driver must be added to this value.

The minimum recommended value of C is 100pF. The parasitic capacitance of the PCB and any attached scope probes introduces significant delay errors if smaller values are used. Larger values of C further minimize errors.

Acceptable values of R are primarily effected by the source resistance of the logic inputs. Generally, 100Ω resistors or larger are usable.

5.2 Paralleling Outputs to Double the Peak Drive Currents

The typical propagation matching of the ISL89163 and ISL89164 is less than 1ns. The matching is so precise that carefully matched and calibrated scope probes and channels must be used to make this measurement. Because of the excellent performance, these driver outputs can be safely paralleled to double the current drive capacity. It is important that the INA and INB inputs are connected together on the PCB with the shortest possible trace, which is also required of OUTA and OUTB. However, the ISL89165 cannot be paralleled because of the complementary logic.

5.3 Power Dissipation of the Driver

The power dissipation of the ISL89163, ISL89164, ISL89165 is dominated by the losses associated with the gate charge of the driven bridge FETs and the switching frequency. The internal bias current also contributes to the total dissipation, but it is usually not significant as compared to the gate charge losses.

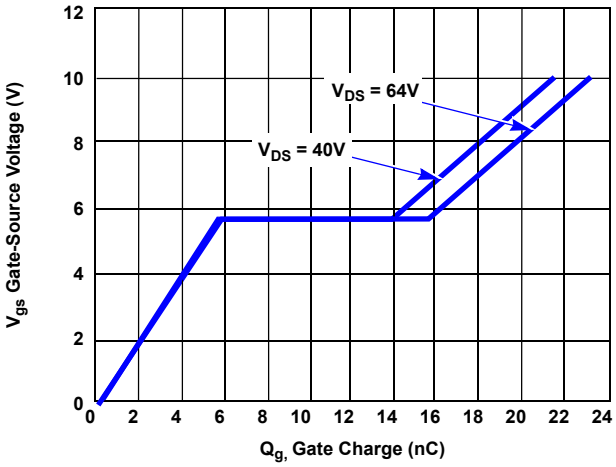


Figure 20. MOSFET Gate Charge vs Gate Voltage

Figure 20 illustrates how the gate charge varies with the gate voltage in a typical power MOSFET. In this example, the total gate charge for V_{gs} = 10V is 21.5nC when V_{DS} = 40V. This is the charge that a driver must source to turn on the MOSFET and must sink to turn-off the MOSFET.

Equation 2 shows calculating the power dissipation of the driver:

$$\text{(EQ. 2)} \quad P_D = 2 \bullet Q_c \bullet freq \bullet V_{GS} \bullet \frac{R_{gate}}{R_{gate} + r_{DS(ON)}} + I_{DD}(freq) \bullet V_{DD}$$

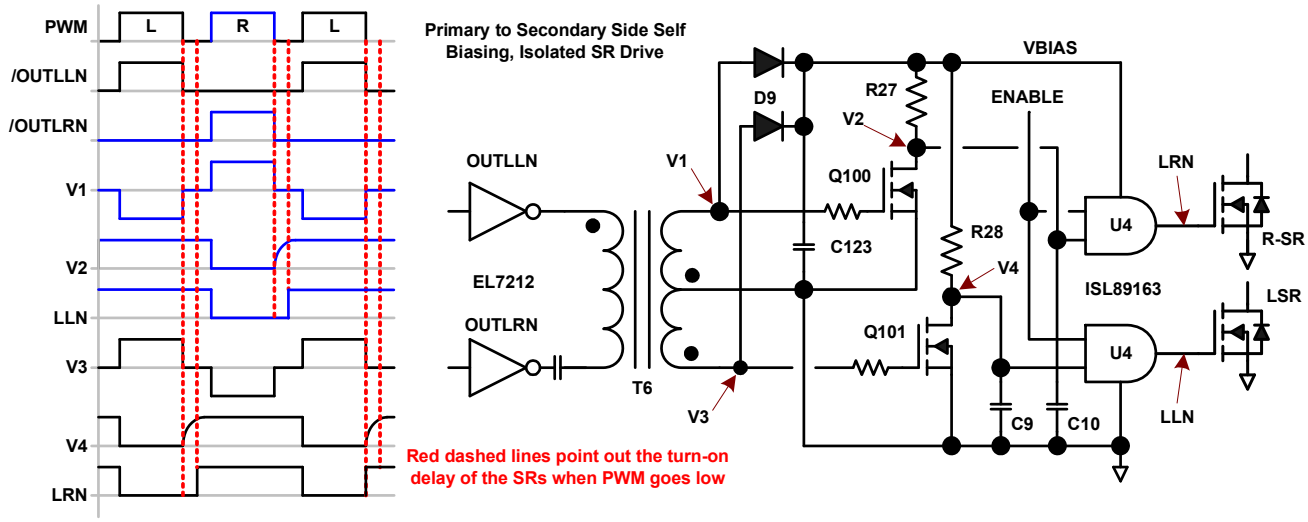
where:

- freq = Switching frequency,
- V_{GS} = V_{DD} bias of the ISL89163, ISL89164, ISL89165
- Q_c = Gate charge for V_{GS}
- I_{DD}(freq) = Bias current at the switching frequency (see Figure 11)
- $r_{DS(ON)}$ = ON-resistance of the driver
- R_{gate} = External gate resistance (if any).

Note: The gate power dissipation is proportionally shared with the external gate resistor. Do not overlook the power dissipated by the external gate resistor.

5.4 Typical Application Circuits

The drive circuit provides primary-to-secondary line isolation. A controller, on the primary side, is the source of the SR control, OUTLLN, and OUTLRN signals. The secondary side signals, V1 and V2 are rectified by the dual diode, D9, to generate the secondary side bias for U4. V1 and V3 are also inverted by Q100 and Q101, and the rising edges are delayed by R_{27}/C_{10} and R_{28}/C_9 respectively to generate the SR drive signals, LRN and LLN. For complete information on this SR drive circuit, and other applications for the ISL89163, ISL89164, ISL89165, see AN1603, “ISL6752/54EVAL1Z ZVS DC/DC Power Supply with Synchronous Rectifiers User Guide”.


PWM
L
R
L
/OUTLLN
/OUTLRN
V1
V2
LLN
V3
V4
LRN
Primary to Secondary Side Self Biasing, Isolated SR Drive
OUTLLN
OUTLRN
EL7212
T6
D9
V1
V2
V3
V4
R27
Q100
C123
R28
Q101
C9
C10
VBIAS
ENABLE
U4
U4
ISL89163
LRN
LLN
R-SR
LSR
Red dashed lines point out the turn-on delay of the SRs when PWM goes low

6. General PCB Layout Guidelines

The AC performance of the ISL89163, ISL89164, ISL89165 depends significantly on the design of the PC board. The following layout design guidelines are recommended to achieve optimum performance:

- Place the driver as close as possible to the driven power FET.
- Understand where the switching power currents flow. The high-amplitude di/dt currents of the driven power FET will induce significant voltage transients on the associated traces.
- Keep power loops as short as possible by paralleling the source and return traces.
- Use planes where practical; they are usually more effective than parallel traces.
- Avoid paralleling high-amplitude di/dt traces with low level signal lines. High di/dt will induce currents and consequently, noise voltages in the low level signal lines.
- When practical, minimize impedances in low level signal circuits. The noise, magnetically induced on a 10kΩ resistor, is 10x larger than the noise on a 1kΩ resistor.
- Be aware of magnetic fields emanating from transformers and inductors. Gaps in the magnetic cores of these structures are especially bad for emitting flux.
- If you must have traces close to magnetic devices, align the traces so that they are parallel to the flux lines to minimize coupling.
- The use of low inductance components, such as chip resistors and chip capacitors, is highly recommended.
- Use decoupling capacitors to reduce the influence of parasitic inductance in the V_{DD} and GND leads. To be effective, these caps must also have the shortest possible conduction paths. If vias are used, connect several paralleled vias to reduce the inductance of the vias.
- It may be necessary to add resistance to dampen resonating parasitic circuits especially on OUTA and OUTB. If an external gate resistor is unacceptable, the layout must be improved to minimize lead inductance.
- Keep high dv/dt nodes away from low level circuits. Guard banding can be used to shunt away dv/dt injected currents from sensitive circuits, which is especially true for control circuits that source the input signals to the ISL89163, ISL89164, ISL89165.
- Avoid having a signal ground plane under a high-amplitude dv/dt circuit, which injects di/dt currents into the signal ground paths.
- Do power dissipation and voltage drop calculations of the power traces. Many PCB/CAD programs have built in tools for calculation of trace resistance.
- Large power components (Power FETs, Electrolytic caps, power resistors, etc.) have internal parasitic inductance which cannot be eliminated. This must be accounted for in the PCB layout and circuit design.
- If you simulate your circuits, consider including parasitic components especially parasitic inductance.

7. General EPAD Heatsinking Considerations

The thermal pad is electrically connected to the GND supply through the IC substrate. The EPAD of the ISL89163, ISL89164, ISL89165 has two main functions:

- Provide a quiet GND for the input threshold comparators
- Provide heat sinking for the IC

The EPAD must be connected to a ground plane, and no switching currents from the driven FET should pass through the ground plane under the IC.

Figure 21 is a PCB layout example of how to use vias to remove heat from the IC through the EPAD.

For maximum heatsinking, Renesas recommends that a ground plane, connected to the EPAD, is added to both sides of the PCB. A via array, within the area of the EPAD, conducts heat from the EPAD to the GND plane on the bottom layer. The number of vias and the size of the GND planes required for adequate heatsinking is determined by the power dissipated by the ISL89163, ISL89164, ISL89165, the air flow, and the maximum temperature of the air around the IC.

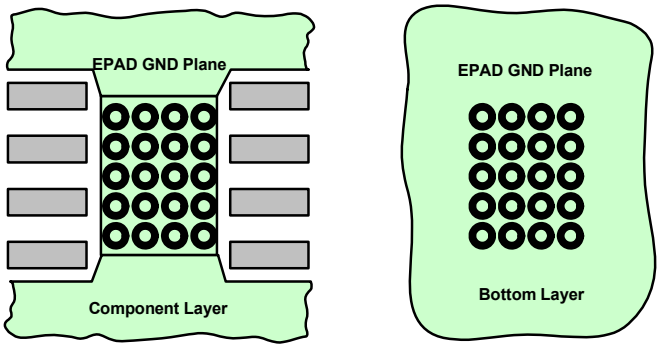


Figure 21. Typical PCB Pattern for Thermal Vias

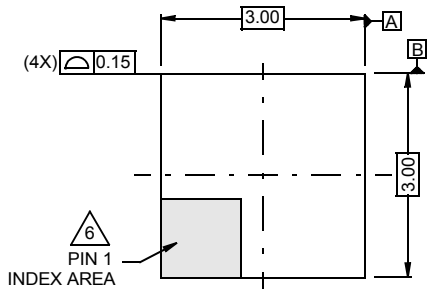
8. Revision History

Rev.	Date	Description
6.00	Jul.9.19	Applied new formatting Updated 1st paragraph on page 1. Updated links throughout document. Updated Ordering Information table adding tape and reel information to table and updating notes, and removed Note 1. Removed About Intersil section Updated disclaimer.
5.00	Oct.13.16	t_{on_delay} parameter added to the AC Electrical Specifications. The “up to 400µs” label of Figure 9 is changed to “400µs typical (t_{on_delay})”.
4.00	Sep.30.15	Updated the Ordering Information table on page 3. Replaced Products section with About Intersil section. Updated Package Outline Drawing L8.3x3I to the latest revision. Changes are as follows: -Tiebar Note updated From: Tiebar shown (if present) is a non-functional feature. To: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
3.00	Feb.22.12	(page 5) ENA and ENB added to the Input Range parameter (page 6) Propagation delay testing parameters changed for option C (page 6) Note 13 added (page 7) Figure 3 modified to show different input thresholds for testing prop delays for option C (page 4) The startup sequence references for the VDD Undervoltage Lock-out parameters for Option C is now the same as Options A and B. Options A, B, and C now have the same startup sequence. (page 5) Note 9 is rewritten to be more precise. (page 8) The old startup sequence for Option C has been deleted (formerly Figure 10) (page 10) The old startup sequence description in the Functional Description Overview has been deleted.
2.00	Jan.9.12	(page 1) vertical part numbers in the right margin are deleted to conform to new datasheet standards. (page 1) Last paragraph of the product description is changed to better describe the improved turn on characteristics. (page 1) features list is reduced in size to 8 features. Some features are reworded to improve readability. (page 1) a reference to a non-existent application note is deleted from the Related Literature section. (page 2) pin configuration pictures are redrawn and relabeled for readability. (page 2) some pins description names are changed to corollate to the pin name in the pin configuration pictures. Some descriptions are also corrected. The truth table associated with the pin descriptions is expanded to include the logic performance of the under-voltage. (these revisions are not a change to function). (page 4) note and figure references are added to the VDD Under-voltage lock-out parameter for options A, B, and C (page 5) note 12 is revised to more clearly describe the turn-on characteristics of options A, B, and C. (page 6) no load test conditions added to the rising and falling propagation matching parameters. (page 8) figures 7 and 8 added to clearly define the startup characteristics (page 10) the last paragraph of the Functional Description overview is replaced by 3 paragraphs to more clearly describe the under voltage and turn-on and turn-off characteristics. (page 11). A new section is added to the application information describing how the drivers outputs can be paralleled. (pages 1..13) various minor corrections to text for grammar and spelling.
1.00	Aug.26.11	(page 8) Note 12 revised from 200µs to 400µs (page 6) The Operating Junction Temp Range in the “Thermal Information” was revised to read “Maximum Operating Junction Temp Range....-40°C to +150°C” from “-40°C to +125°C” Updated POD M8.15D by converting to new POD format. Removed table of dimensions and moved dimensions onto drawing. Added land pattern.
0.00	Oct.12.10	Initial release

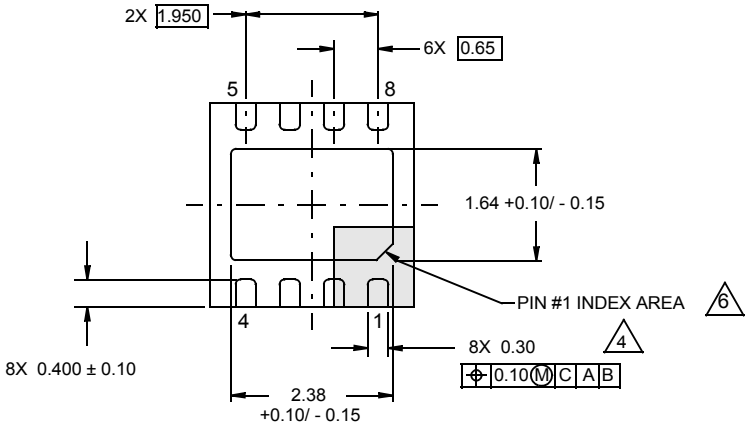
9. Package Outline Drawings

For the most recent package outline drawing, see L8.3x3I.

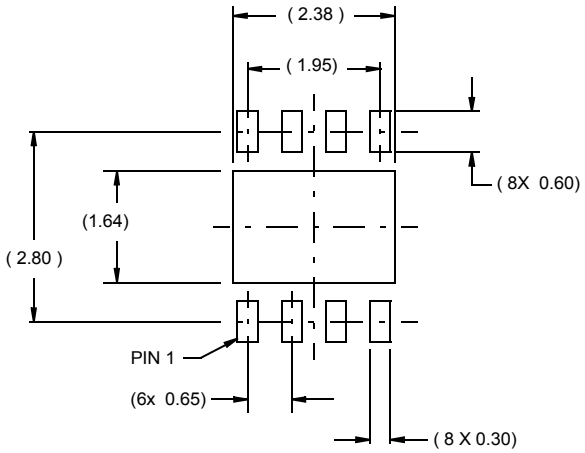
L8.3x3I
8 Lead Thin Dual Flat No-Lead Plastic Package
Rev 2 5/15



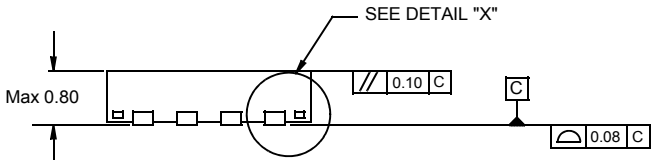
TOP VIEW



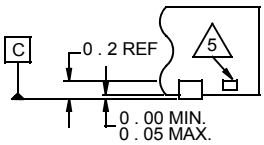
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



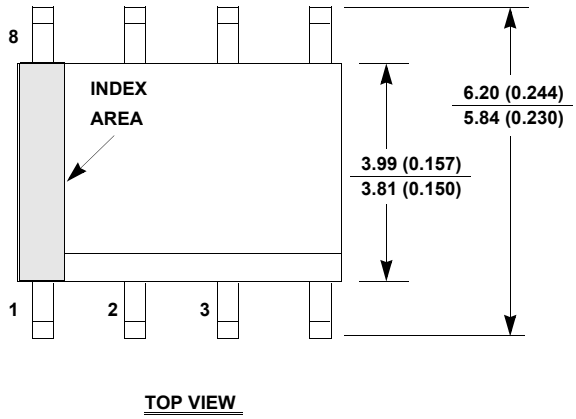
DETAIL "X"

NOTES:

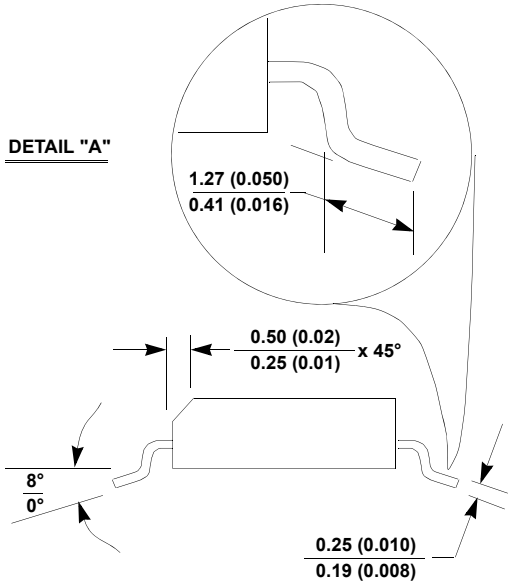
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

M8.15D
8 Lead Narrow Body Small Outline Exposed Pad Plastic Package
Rev 1, 3/11

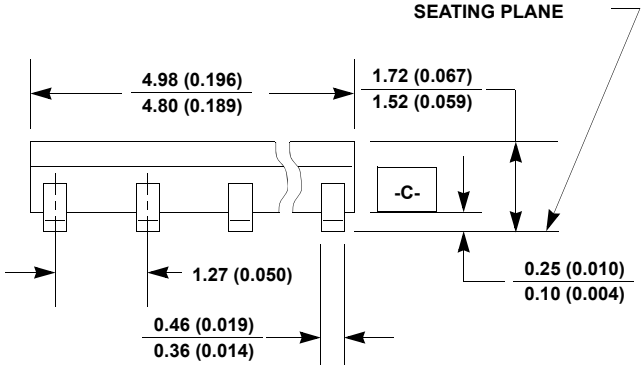
For the most recent package outline drawing, see M8.15D.



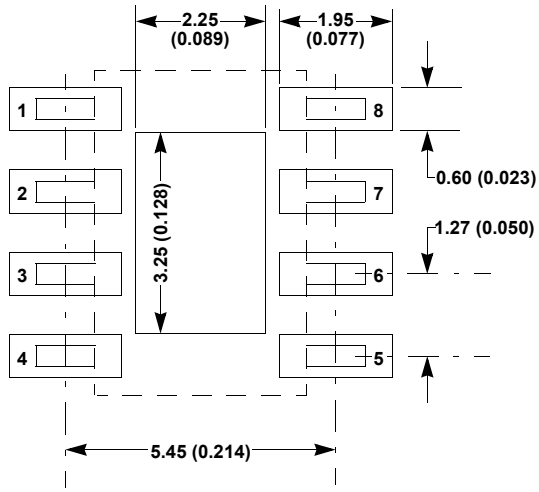
TOP VIEW



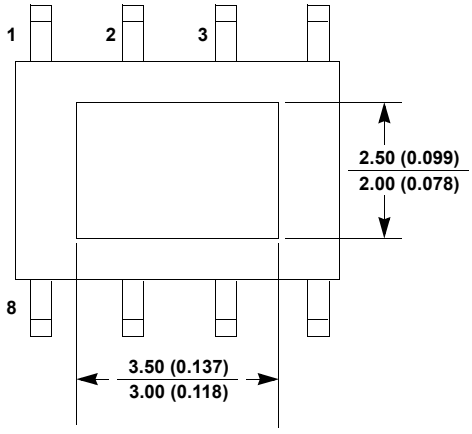
SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN



BOTTOM VIEW

Notes:

1. Dimensions are in millimeters. Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing per ASME-Y14.5M-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05.
4. Dimension does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The Pin 1 identifier may be either a mold or a mark feature.
6. The chamfer on the body is optional. If it is not present, a visual index