ISL91107

High Efficiency Buck-Boost Regulator with 3.6A Switches

FN8584
Rev 3.00
May 3, 2018

The ISL91107 is a highly-integrated buck-boost switching regulator that accepts input voltages either above or below the regulated output voltage. Unlike other buck-boost regulators, this regulator automatically transitions between operating modes without significant output disturbance.

This device is capable of delivering up to 2A of output current (PVIN = 2.8V, V_{OUT} = 3.3V) and provides excellent efficiency due to its fully synchronous 4-switch architecture. No-load quiescent current of only 45µA also optimizes efficiency under light-load conditions.

The ISL91107 is designed for standalone applications and supports 3.3V fixed output voltages or variable output voltages with an external resistor divider. Output voltages as low as 1V or as high as 5.2V are supported using an external resistor divider.

The ISL91107 requires only a single inductor and very few external components. Power supply solution size is minimized by a 2.15mmx1.51mm WLCSP and a 2.5MHz switching frequency, which further reduces the size of external components.

Related Literature

For a full list of related documents, visit our website

- ISL91107 product page

Features

- Accepts input voltages above or below regulated output voltage
- Automatic and seamless transitions between Buck and Boost modes
- Input voltage range: 1.8V to 5.5V
- Output current: up to 2A (PVIN = 2.8V, V_{OUT} = 3.3V)
- High efficiency: up to 96%
- 45µA quiescent current maximizes light-load efficiency
- 2.5MHz switching frequency minimizes external component size
- Selectable forced PWM mode
- Fully protected for short-circuit, over-temperature and undervoltage
- Small 2.15mmx1.51mm WLCSP

Applications

- Smartphones and tablet PCs
- Wireless communication devices
- 2G/3G/4G power amplifiers

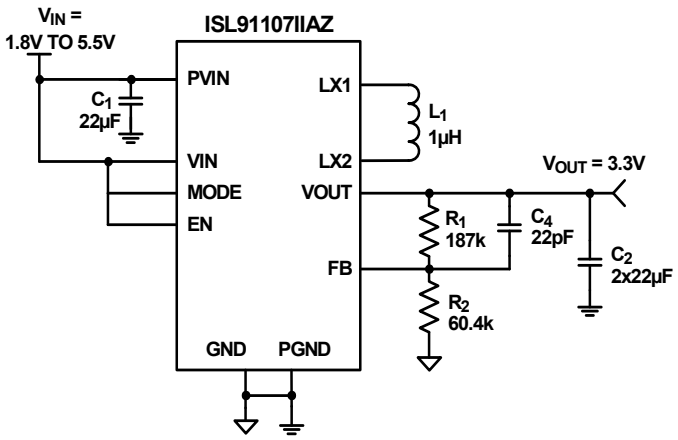


FIGURE 1. TYPICAL APPLICATION

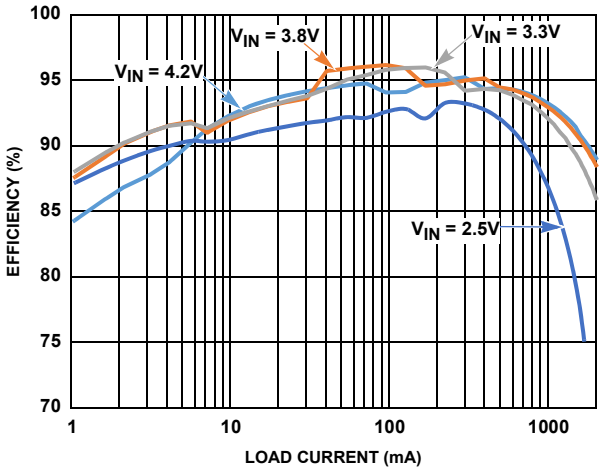
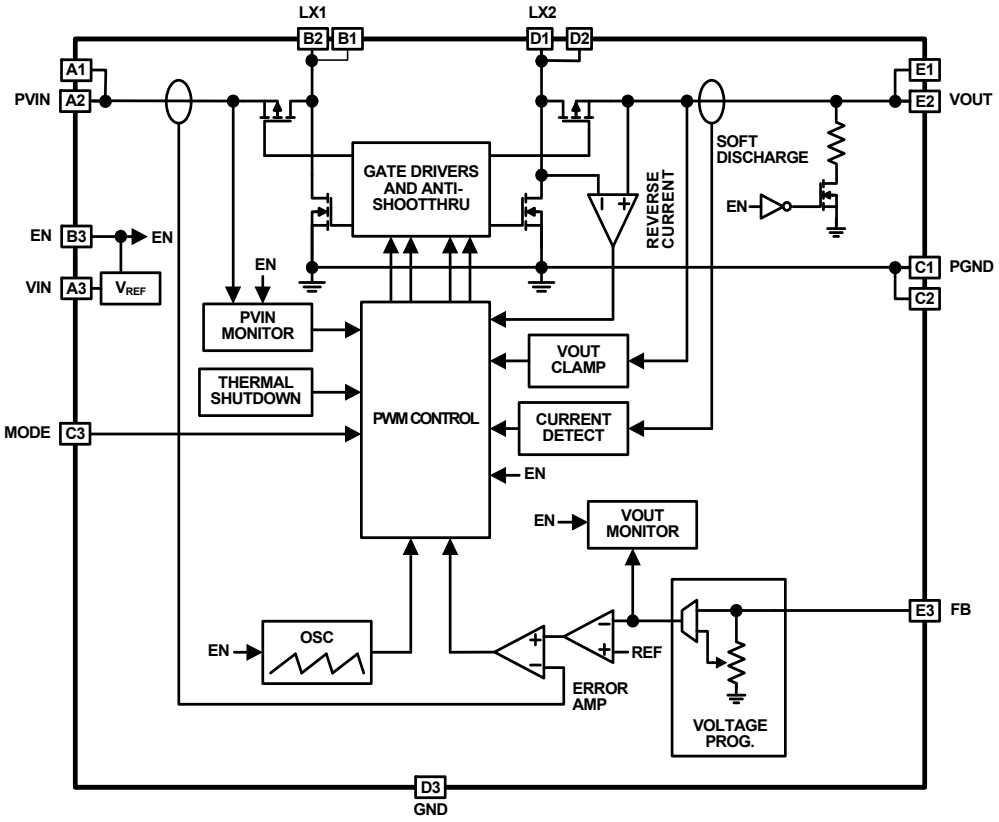


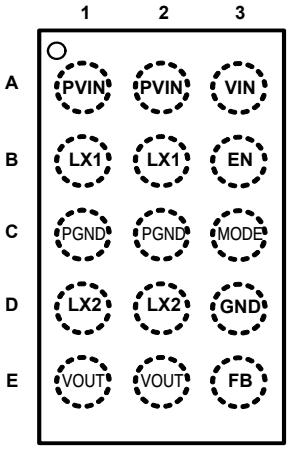
FIGURE 2. EFFICIENCY vs OUTPUT CURRENT (V_{OUT} = 3.3V)

Block Diagram



Pin Configuration

ISL91107
(15 BUMP WLCSP)
TOP VIEW



Pin Descriptions

PIN #	PIN NAMES	DESCRIPTION
A1, A2	PVIN	Power input. Range: 1.8V to 5.5V. Connect 22µF capacitor to PGND.
A3	VIN	Supply input. Range: 1.8V to 5.5V.
B1, B2	LX1	Inductor connection, input side.
B3	EN	Logic input for enable. Drive HIGH to enable device, LOW to disable.
C1, C2	PGND	Power ground for high switching current.
C3	MODE	Logic input, HIGH for auto PFM mode. LOW for forced PWM operation.
D1, D2	LX2	Inductor connection, output side.
D3	GND	Analog ground pin
E1, E2	VOUT	Buck-boost output. Connect 2x22µF capacitor to PGND.
E3	FB	Voltage feedback pin

Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	VOUT (V)	TEMP RANGE (°C)	TAPE AND REEL (UNITS) (Note 1)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL91107IINZ-T	GAXK	3.3	-40 to +85	3k	15 Bump WLCSP	W3x5.15
ISL91107IINZ-T7A	GAXK	3.3	-40 to +85	250	15 Bump WLCSP	W3x5.15
ISL91107IIAZ-T	GAXJ	Adj	-40 to +85	3k	15 Bump WLCSP	W3x5.15
ISL91107IIAZ-T7A	GAXJ	Adj	-40 to +85	250	15 Bump WLCSP	W3x5.15
ISL91107IIN-EVZ	Evaluation Board for ISL91107IINZ					
ISL91107IIA-EVZ	Evaluation Board for ISL91107IIAZ					

NOTES:

1. Refer to TB347 for details about reel specifications.
2. These Pb-free WLCSP packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCuNi - e8 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free WLCSP packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL91107 product information page. For more information about MSL, see TB363.

Absolute Maximum Ratings

PVIN, VIN . . . . . -0.3V to 6.5V
LX1, LX2 . . . . . -0.3V to 6.5V
FB . . . . . -0.3V to 6.5V
GND, PGND . . . . . -0.3V to 0.3V
All Other Pins . . . . . -0.3V to 6.5V
ESD Rating
Human Body Model (Tested per JESD22-A114E) 3kV
Machine Model (Tested per JESD22-A115-A) 300V
Charged Device Model 1kV
Latch-Up (Tested per JESD-78B; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JB} (°C/W)
15 Bump WLCSP (Notes 4, 5)	78	20

Maximum Junction Temperature . . . . . +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Temperature Range . . . . . -40°C to +85°C
Supply Voltage (V_{IN}) Range . . . . . 1.8V to 5.5V
Load Current (I_{OUT}) Range (DC) . . . . . 0A to 2A

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379.
5. For θ_{JB}, the board temp is taken on the board near the edge of the package, on a trace at the middle of one side. See TB379.

Analog Specifications

V_{IN} = PVIN = EN = 3.6V, V_{OUT} = 3.3V, L_1 = 1µH, C_1 = 1x22µF, C_2 = 2x22µF, T_A = +25°C. **Boldface limits apply across the recommended operating temperature range, -40°C to +85°C and input voltage range (1.8V to 5.5V).**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
POWER SUPPLY						
Input Voltage Range	VIN		**1.8**		**5.5**	V
V_{IN} Undervoltage Lockout Threshold	V_{UVLO}	Rising		1.75	**1.795**	V
		Falling	**1.60**	1.71		V
V_{IN} Supply Current	I_{VIN}	PFM mode, no external load on V_{OUT}, no switching, $V_{IN} \le 5V$		45	**60**	µA
		PFM mode, no external load on V_{OUT}, with switching		60		µA
V_{IN} Supply Current, Shutdown	I_{SD}	EN = GND, $V_{IN} \le 5V$		0.05	**0.6**	µA
OUTPUT VOLTAGE REGULATION						
Output Voltage Accuracy	VOUT	I_{OUT} = 1mA, PWM mode	**-2**		**+2**	%
		I_{OUT} = 1mA, PFM mode	**-3**		**+4**	%
Feedback Voltage	VFB	For adjustable version only	**0.788**	0.8	**0.812**	V
Line Regulation, PWM Mode	ΔVOUT/ ΔVIN	I_{OUT} = 500mA, MODE = GND, V_{IN} step from 2.3V to 5.5V		±0.005		mV/mV
Load Regulation, PWM Mode	ΔVOUT/ ΔIOUT	V_{IN} = 3.7V, MODE = GND, I_{OUT} step from 0mA to 500mA		±0.005		mV/mA
Line Regulation, PFM Mode	ΔVOUT/ ΔVIN	I_{OUT} = 100mA, MODE = V_{IN}, V_{IN} step from 2.3V to 5.5V		±12.5		mV/V
Load Regulation, PFM Mode	ΔVOUT/ ΔIOUT	V_{IN} = 3.7V, MODE = V_{IN}, I_{OUT} step from 0mA to 100mA		±0.4		mV/mA
Output Voltage Clamp	V_{CLAMP}	Rising	**5.35**		**5.85**	V
Output Voltage Clamp Hysteresis				400		mV
DC/DC SWITCHING SPECIFICATIONS						
Oscillator Frequency	f_{SW}	$2.5 \le V_{IN} \le 5V$	**2.25**	2.5	**2.75**	MHz
Minimum On Time	t_{ONMIN}			80		ns
LX1 Pin Leakage Current	$I_{PFETLEAK}$		**-0.1**		**0.1**	µA
LX2 Pin Leakage Current	$I_{NFETLEAK}$		**-0.1**		**0.1**	µA

Analog Specifications V_{IN} = PVIN = EN = 3.6V, V_{OUT} = 3.3V, L_1 = 1µH, C_1 = 1x22µF, C_2 = 2x22µF, T_A = +25°C. **Boldface limits apply across the recommended operating temperature range, -40°C to +85°C and input voltage range (1.8V to 5.5V). (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
SOFT-START and SOFT DISCHARGE						
Soft-Start Time	t_{SS}	Time from when EN signal asserts to when output voltage ramp starts.		1		ms
		Time from when output voltage ramp starts to when output voltage reaches 95% of its nominal value with device operating in Buck mode. V_{IN} = 4V, I_{OUT} = 200mA		1		ms
		Time from when output voltage ramp starts to when output voltage reaches 95% of its nominal value with device operating in Boost mode. V_{IN} = 2V, I_{OUT} = 200mA		2		ms
V_{OUT} Soft Discharge ON-Resistance	r_{DISCHG}	V_{IN} = 3.6V, EN < V_{IL}		35		Ω
POWER MOSFET						
P-Channel MOSFET ON-Resistance	r_{DSON_P}	V_{IN} = 3.6V		45		mΩ
N-Channel MOSFET ON-Resistance	r_{DSON_N}	V_{IN} = 3.6V		32		mΩ
P-Channel MOSFET Peak Current Limit	I_{PK_LMT}	V_{IN} = 3.6V	**3.3**	3.8	**4.3**	A
PFM/PWM TRANSITION						
Load Current Threshold, PFM to PWM				375		mA
Load Current Threshold, PWM to PFM				300		mA
Thermal Shutdown				150		°C
Thermal Shutdown Hysteresis				30		°C
LOGIC INPUTS						
Input Leakage	I_{LEAK}			0.05	**0.1**	µA
Input HIGH Voltage	V_{IH}		**1.4**			V
Input LOW Voltage	V_{IL}				**0.4**	V

NOTE:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves

Unless otherwise noted, operating conditions are: T_A = +25 °C, V_{IN} = EN = 3.6V, L = 1µH, C_1 = 22µF, C_2 = 2x22µF, V_{OUT} = 3.3V, I_{OUT} = 0A to 2A.

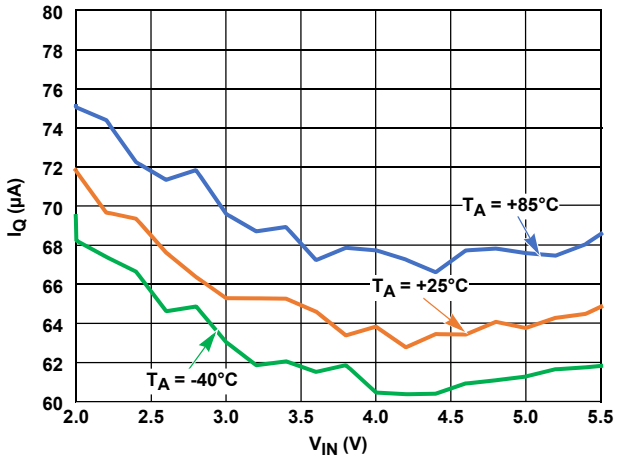


FIGURE 3. QUIESCENT CURRENT vs INPUT VOLTAGE (MODE = HIGH, V_{OUT} = 3.3V)

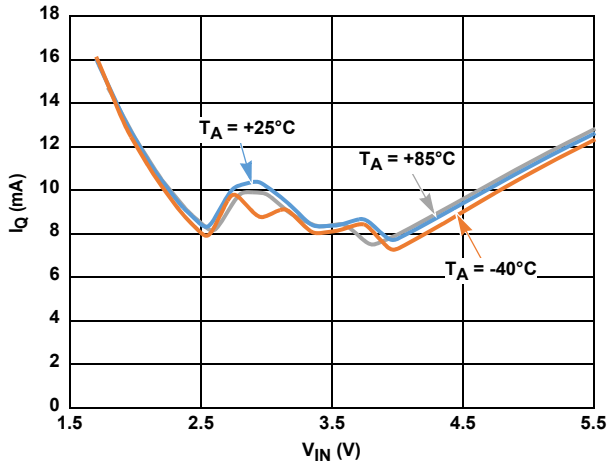


FIGURE 4. QUIESCENT CURRENT vs INPUT VOLTAGE (MODE = LOW, V_{OUT} = 3.3V)

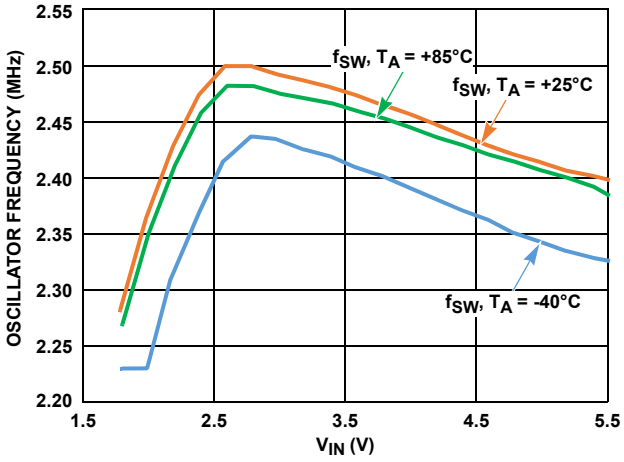


FIGURE 5. SWITCHING FREQUENCY vs INPUT VOLTAGE

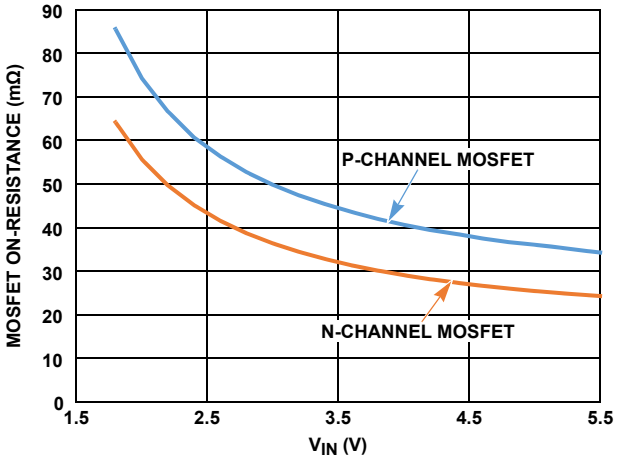


FIGURE 6. MOSFET ON-RESISTANCE vs INPUT VOLTAGE

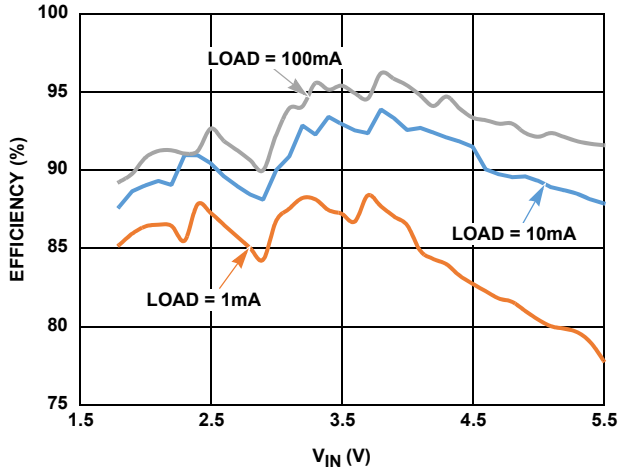


FIGURE 7. LIGHT-LOAD EFFICIENCY vs INPUT VOLTAGE (V_{OUT} = 3.3V)

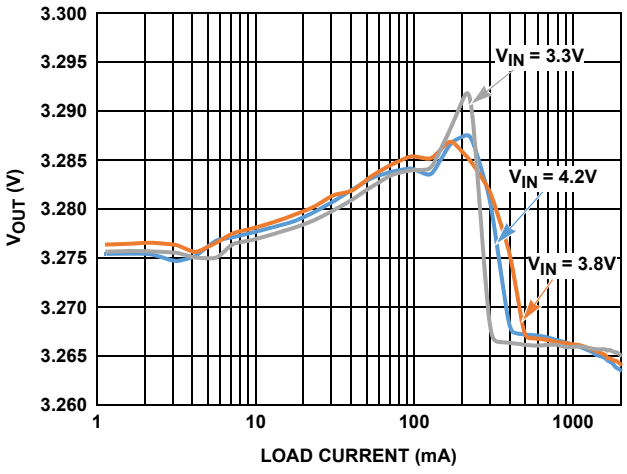


FIGURE 8. OUTPUT VOLTAGE vs LOAD CURRENT

Typical Performance Curves

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = EN = 3.6V, L = 1µH, C_1 = 22µF, C_2 = 2x22µF, V_{OUT} = 3.3V, I_{OUT} = 0A to 2A. **(Continued)**

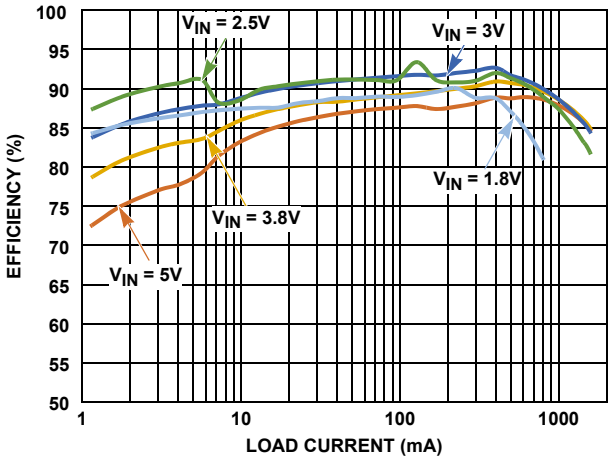


FIGURE 9. EFFICIENCY vs LOAD CURRENT (V_{OUT} = 2V)

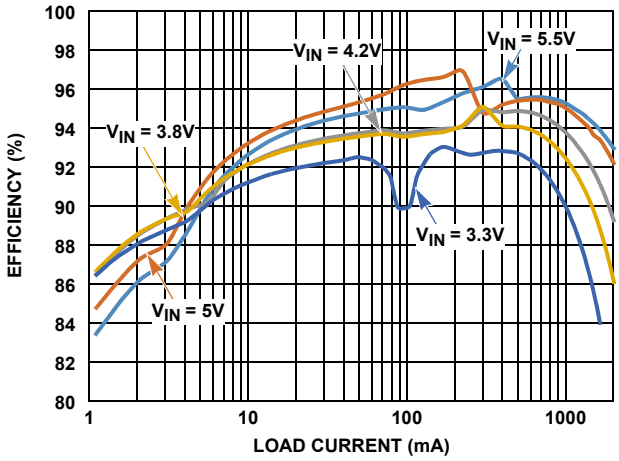


FIGURE 10. EFFICIENCY vs LOAD CURRENT (V_{OUT} = 5V)

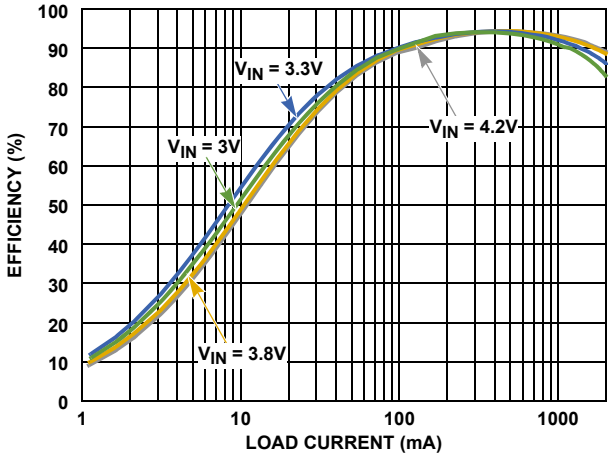


FIGURE 11. EFFICIENCY vs LOAD CURRENT (MODE = LOW, V_{OUT} = 3.3V)

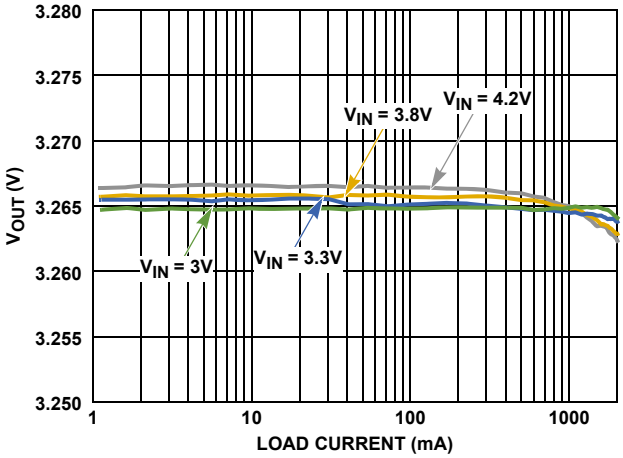


FIGURE 12. OUTPUT VOLTAGE vs LOAD CURRENT (MODE = LOW, V_{OUT} = 3.265V)

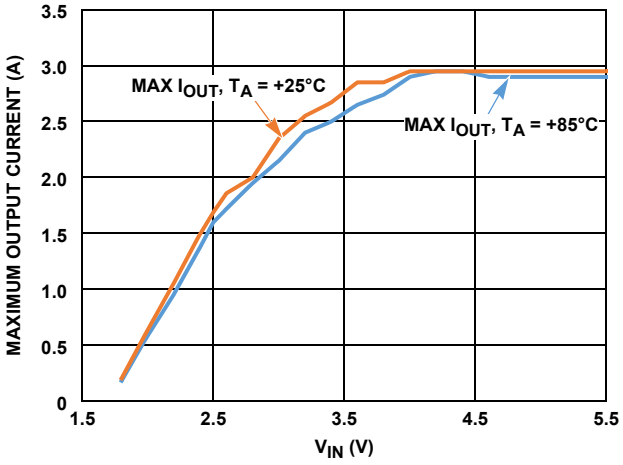


FIGURE 13. MAXIMUM OUTPUT CURRENT vs INPUT VOLTAGE (V_{OUT} = 3.3V)

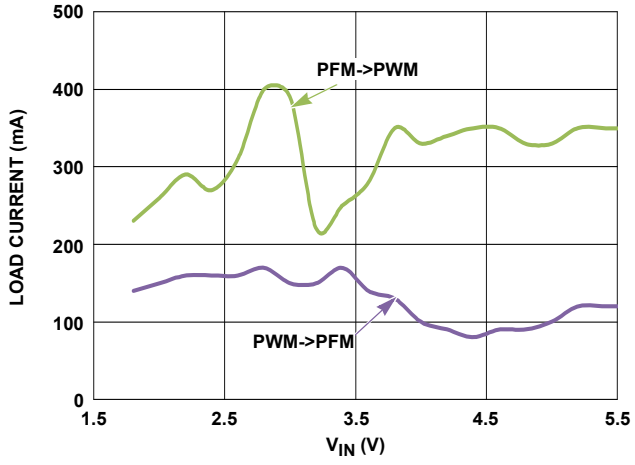


FIGURE 14. PFM<->PWM TRANSITION THRESHOLDS vs V_{IN} (V_{OUT} = 3.3V)

Typical Performance Curves

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = EN = 3.6V, L = 1µH, C_1 = 22µF, C_2 = 2x22µF, V_{OUT} = 3.3V, I_{OUT} = 0A to 2A. **(Continued)**

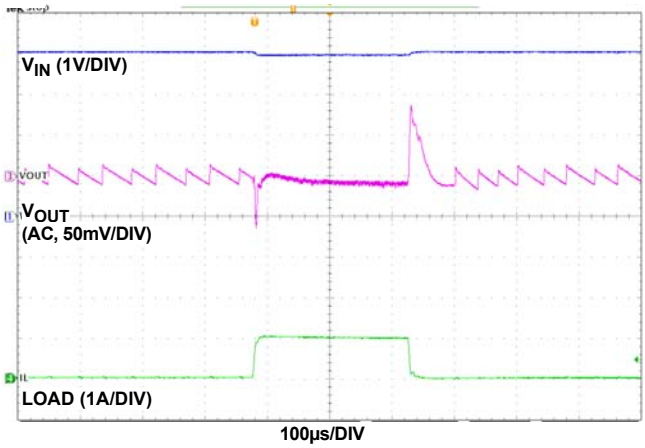


FIGURE 15. 0A TO 1A LOAD TRANSIENT, V_{IN} = 4V

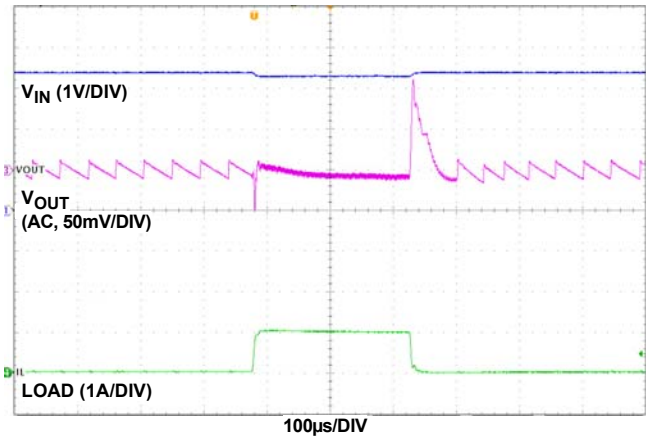


FIGURE 16. 0A TO 1A LOAD TRANSIENT, V_{IN} = 3.3V

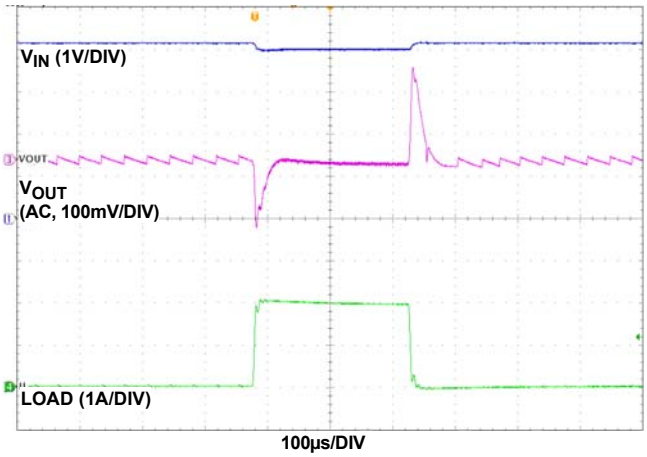


FIGURE 17. 0A TO 2A LOAD TRANSIENT, V_{IN} = 4V

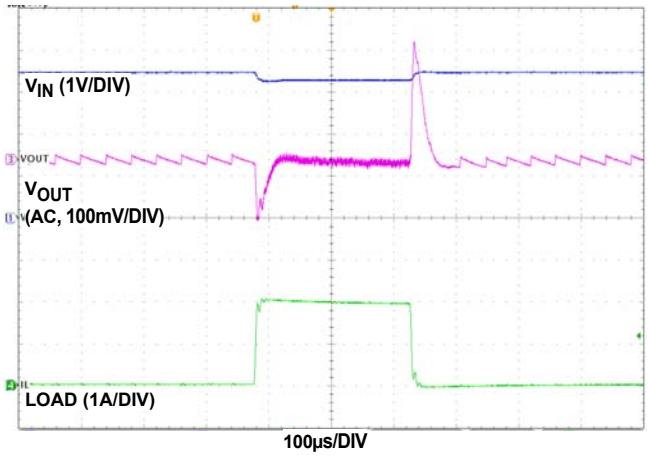


FIGURE 18. 0A TO 2A LOAD TRANSIENT, V_{IN} = 3.3V

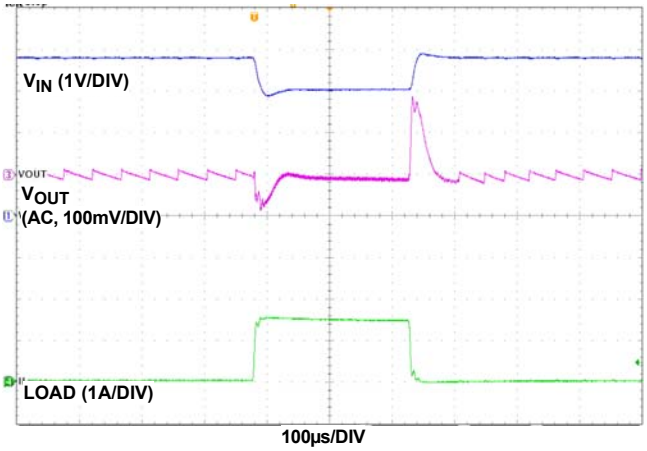


FIGURE 19. 0A TO 1.5A LOAD TRANSIENT WITH 3.8V TO 3V LINE TRANSIENT

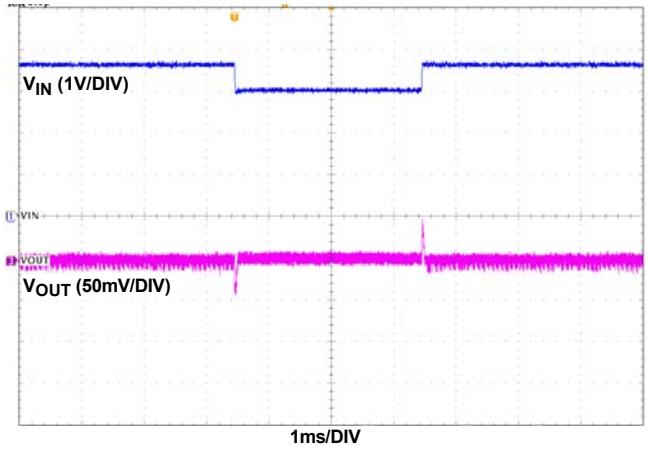


FIGURE 20. 3.6V TO 3V LINE TRANSIENT RESPONSE, V_{OUT} = 3.3V, LOAD = 1.5A

Typical Performance Curves

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = EN = 3.6V, L = 1µH, C_1 = 22µF, C_2 = 2x22µF, V_{OUT} = 3.3V, I_{OUT} = 0A to 2A. **(Continued)**

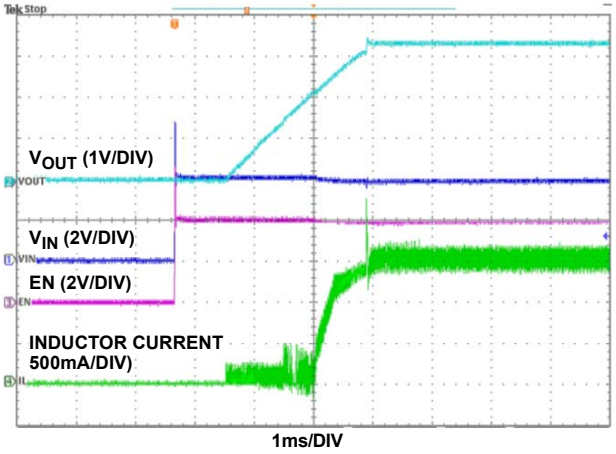


FIGURE 21. START-UP WITH V_{IN} = 4V, R_{LOAD} = 1.5A, V_{OUT} = 3.3V

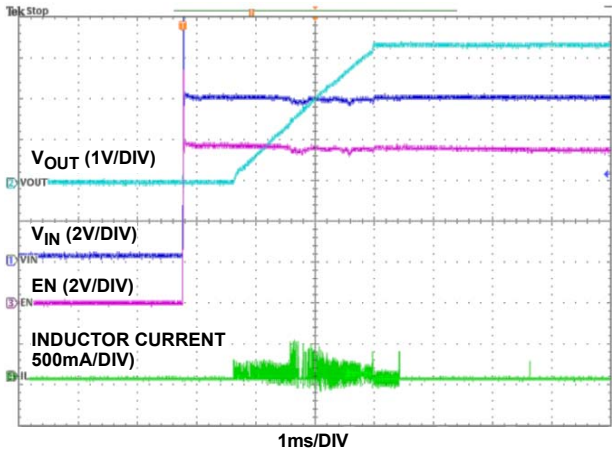


FIGURE 22. START-UP WITH V_{IN} = 4V, NO LOAD, V_{OUT} = 3.3V

Functional Description

Functional Overview

The ISL91107 implements a complete buck-boost switching regulator with PWM controller, internal switches, references, protection circuitry and control inputs. Refer to the "Block Diagram" on page 2.

The PWM controller automatically switches between Buck and Boost modes as necessary to maintain a steady output voltage with changing input voltages and dynamic external loads.

Internal Supply and References

Referring to the "Block Diagram", the ISL91107 provides two PVIN power input pins. The PVIN pins supply input power to the DC/DC converter. An additional VIN pin provides an operating voltage source required for stable V_{REF} generation. Separate ground pins (PGND and GND) are provided to avoid problems caused by ground shift due to the high switching currents.

Enable Input

A master enable pin, EN, allows the device to be enabled. Driving EN LOW invokes a power-down mode, where most internal device functions are disabled.

Soft Discharge

When the device is disabled by driving EN LOW, an internal resistor between VOUT and GND is activated. This internal resistor has a typical resistance of 35Ω.

POR Sequence and Soft-Start

Bringing the EN pin HIGH allows the device to power up. A number of events occur during the start-up sequence. The internal voltage reference powers up and stabilizes. The device then starts operating. There is a 1ms (typical) delay between assertion of the EN pin and the start of the switching regulator soft-start ramp.

The soft-start feature minimizes output voltage overshoot and input inrush currents. During soft-start, the reference voltage is ramped to provide a ramping V_{OUT} voltage. While output voltage is lower than approximately 20% of the target output voltage, switching frequency is reduced to a fraction of the normal switching frequency to aid in producing low duty cycles necessary to avoid input inrush current spikes. Once the output voltage exceeds 20% of the target voltage, the switching frequency is increased to its nominal value.

When the target output voltage is higher than the input voltage, there will be a transition from Buck mode to Boost mode during the soft-start sequence. At the time of this transition, the ramp rate of the reference voltage is decreased, such that the output voltage slew rate is decreased. This provides a slower output voltage slew rate.

The V_{OUT} ramp time is not constant for all operating conditions. Soft-start into Boost mode will take longer than soft-start into Buck mode. The total soft-start time into Buck mode is typically 2ms, whereas the typical soft-start time into Boost mode is typically 3ms. Increasing the load current will increase these typical soft-start times.

Overcurrent Protection

The ISL91107 provides short-circuit protection by monitoring the FB voltage. When the FB voltage is sensed to be lower than a certain threshold, the PWM oscillator frequency is reduced in order to protect the device from damage. The P-channel MOSFET peak current limit remains active during this state.

When the current in the P-channel MOSFET is sensed to reach the current limit for 16 consecutive switching cycles, the internal protection circuit is triggered and switching is stopped for approximately 40ms. The device then performs a soft-start cycle. If the external output overcurrent condition exists after the soft-start cycle, the device will again detect 16 consecutive switching cycles reaching the peak current threshold and turns off for 40ms. The process will repeat as long as the external overcurrent condition is present. This behavior is called 'Hiccup mode'.

Undervoltage Lockout

The Undervoltage Lockout (UVLO) feature prevents abnormal operation in the event that the supply voltage is too low to ensure proper operation. When the V_{IN} voltage falls below the UVLO threshold, the regulator is disabled.

Thermal Shutdown

A built-in thermal protection feature protects the ISL91107, if the die temperature reaches +150°C (typical). At this die temperature, the regulator is completely shut down. The die temperature continues to be monitored in this thermal shutdown mode. When the die temperature falls to +120°C (typical), the device will resume normal operation.

When exiting thermal shutdown, the ISL91107 will execute its soft-start sequence.

Buck-Boost Conversion Topology

The ISL91107 operates in either Buck or Boost mode. When operating in conditions where V_{IN} is close to V_{OUT}, the ISL91107 alternates between Buck and Boost modes as necessary to provide a regulated output voltage.

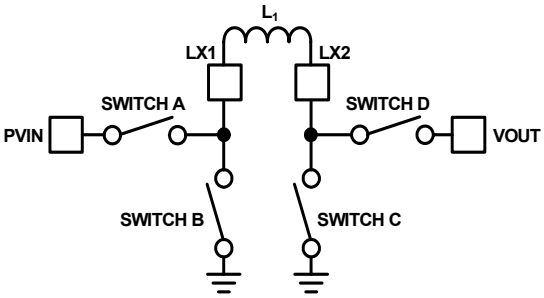


FIGURE 23. BUCK-BOOST TOPOLOGY

Figure 23 shows a simplified diagram of the internal switches and external inductor.

PWM Operation

During PWM operation in Buck mode, Switch D is continuously closed and Switch C is continuously open. Switches A and B operate as a synchronous buck converter when in this mode.

During PWM operation in Boost mode, Switch A remains closed and Switch B remains open. Switches C and D operate as a synchronous boost converter when in this mode.

PFM Operation

During PFM operation in Buck mode, Switch D is continuously closed and Switch C is continuously open. Switches A and B operate in discontinuous mode during PFM operation. During PFM operation in Boost mode, the ISL91107 closes Switch A and Switch C to ramp up the current in the inductor. When the inductor current reaches a certain threshold, the device turns OFF Switches A and C, then turns ON Switches B and D. With Switches B and D closed, output voltage increases as the inductor current ramps down.

In most operating conditions, there will be multiple PFM pulses to charge up the output capacitor. These pulses continue until V_{OUT} has achieved the upper threshold of the PFM hysteretic controller. Switching then stops, and remains stopped until V_{OUT} decays to the lower threshold of the hysteretic PFM controller.

Operation with V_{IN} Close to V_{OUT}

When the output voltage is close to the input voltage, the ISL91107 will rapidly and smoothly switch from Boost to Buck mode as needed to maintain the regulated output voltage. This behavior provides excellent efficiency and very low output voltage ripple.

Applications Information

Component Selection

The fixed output versions of the ISL91107 require only three external power components to implement the buck boost converter: an inductor, an input capacitor and an output capacitor.

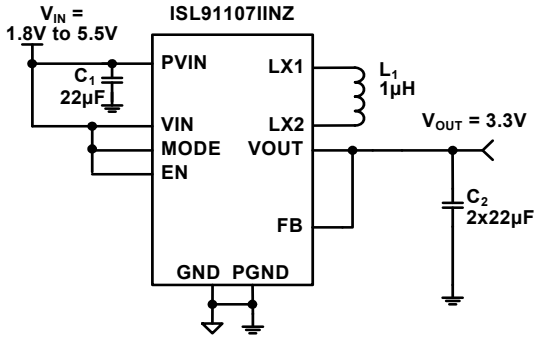


FIGURE 24. TYPICAL ISL91107IINZ APPLICATION

The adjustable ISL91107 version requires three additional components to program the output voltage. Two external resistors program the output voltage, and a small capacitor is added to improve stability and response.

Setting and controlling the output voltage of the ISL91107 (adjustable output version) can be accomplished by selecting the external resistor values.

Equation 1 can be used to derive the R_1 and R_2 resistor values:

$$V_{OUT} = 0.8V \bullet \left(1 + \frac{R_1}{R_2}\right) \quad \text{(EQ. 1)}$$

When designing a PCB, include a GND guard band around the feedback resistor network to reduce noise and improve accuracy and stability. Resistors R_1 and R_2 should be positioned close to the FB pin.

Inductor Selection

An inductor with high frequency core material (for example, ferrite core) should be used to minimize core losses and provide good efficiency. The inductor must be able to handle the peak switching currents without saturating.

A 1µH inductor with ≥3.8A saturation current rating is recommended. Select an inductor with low DCR to provide good efficiency. In applications where radiated noise must be minimized, a toroidal or shielded inductor can be used.

TABLE 1. INDUCTOR VENDOR INFORMATION

MANUFACTURER	MFR P/N	DESCRIPTION
Cyntec	PIFE32251B-1R0MS	1µH, 3.2x2.5x1.2mm
TOKO	DFE322512C	1µH, 3.2x2.5x1.2mm

PVIN and V_{OUT} Capacitor Selection

The input and output capacitors should be ceramic X5R type with low ESL and ESR. The recommended input capacitor value is 22µF. This would provide adequate RMS current to minimize the input voltage ripple.

The recommended output capacitor is 2x 22µF, 10V, X5R. Note that the effective value of a ceramic capacitor derates with DC voltage bias across it. This derating may be up to 70% of the rated capacitance.

TABLE 2. CAPACITOR VENDOR INFORMATION

MANUFACTURER	PN	DESCRIPTION
Murata	GRM188R61A226ME15D	22µF, 0603, 10V, X5R
TDK	C1608X5R1A226M080AC	22µF, 0603, 10V, X5R

Refer to the capacitor datasheet to ensure the combined effective output capacitance is at least 14µF for proper operation over the entire recommended load current range. Low output capacitance may lead to large output voltage drop during load transient or unstable operation.

Recommended PCB Layout

Correct PCB layout is critical for proper operation of the ISL91107. The following are some general guidelines for layout:

1. Place the input and output capacitors as close to the IC as possible.
2. The ground connections of the input and output capacitors should be kept as short as possible. The objective is to minimize the current loop between the ground pads of the input and output capacitors and the PGND pins of the IC. Use vias, if required, to take advantage of a PCB ground layer underneath the regulator.
3. Connect the analog ground pin (GND) to a large/low-noise ground plane on the top or an intermediate layer on the PCB, away from the switching current path of PGND. This ensures a low noise signal ground reference.
4. Minimize the trace lengths on the feedback loop to avoid switching noise pick-up. Avoid vias on the feedback loop to minimize the effect of board parasitic, particularly during load transients.
5. The LX1 and LX2 traces need to be short and routed on the same layer as the IC.

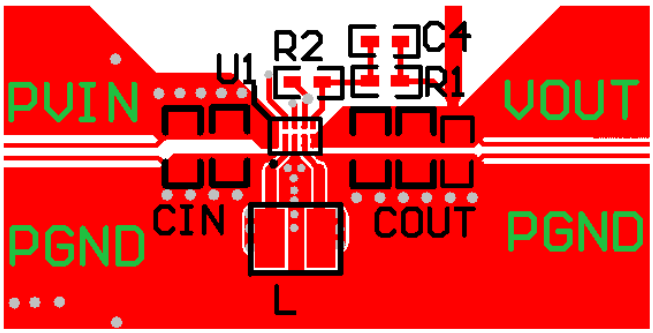


FIGURE 25. RECOMMENDED LAYOUT

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
May 3, 2018	FN8584.3	Updated Related Literature on page 1. Ordering Information table on page 3: Added Tape and Reel quantity column Added -T7A parts Updated Note 2 Removed About Intersil section. Updated Disclaimer and moved to page 14.
Mar 12, 2015	FN8584.2	Replaced Figure 14 on page 7.
Aug 22, 2014	FN8584.1	Replaced Figures 15 through 20. Added conditions to “Typical Performance Curves” on page 6. Removed Figure titled “3.3V to 2.5V LINE TRANSIENT, 1.5A LOAD” on page 9. Updated verbiage in section “PVIN and VOUT Capacitor Selection” on page 11. Updated verbiage in section “Recommended PCB Layout” on page 11.
Jun 30, 2014	FN8584.0	Initial Release.

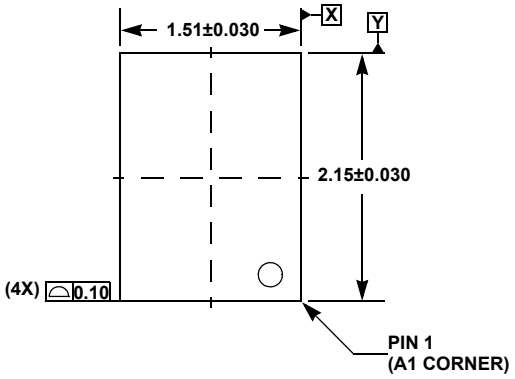
Package Outline Drawing

For the most recent package outline drawing, see W3x5.15.

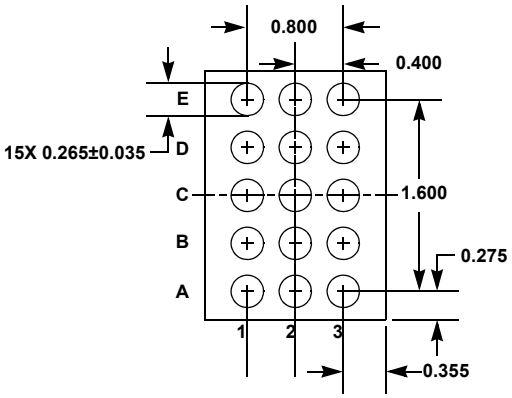
W3x5.15

15 BALL WAFER LEVEL CHIP SCALE PACKAGE (WLCSP 0.4mm pitch)

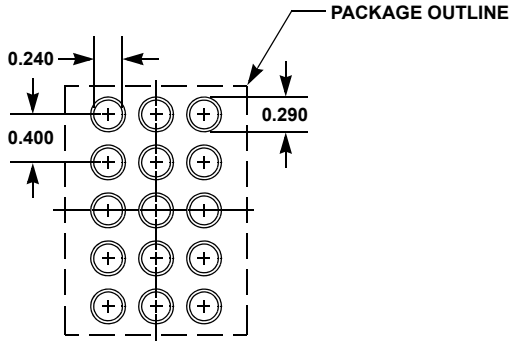
Rev 1, 6/14



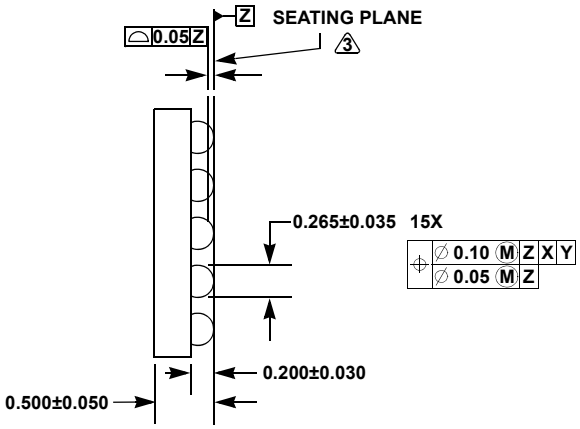
TOP VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW

NOTES:

1. Dimensions and tolerance per ASME Y 14.5M - 1994.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z .
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010.
5. There shall be a minimum clearance of 0.10mm between the edge of the bump and the body edge.