

ISL9120R5696

Compact High-Efficiency Low Power Buck-Boost Regulator

FN8894
Rev. 4.00
Jan 31, 2019

The [ISL9120R5696](#) is a highly integrated buck-boost switching regulator that accepts input voltages either above or below the regulated output voltage. This regulator automatically transitions between Buck and Boost modes without significant output disturbance. The ISL9120R5696 also has automatic bypass functionality for situations in which the input voltage is generally within 1% to 2% of the output voltage. In this case, there is a direct bypass connection between the VIN and VOUT pins. In addition to the automatic bypass functionality, the ISL9120R5696 has forced bypass functionality with the use of the BYP pin.

This device is capable of delivering up to 800mA of output current ($V_{IN} = 2.5V$, $V_{OUT} = 3.3V$) and provides excellent efficiency due to its adaptive current limit Pulse Frequency Modulation (PFM) control architecture.

The ISL9120R5696 is designed for stand-alone applications and supports a 3.3V fixed output voltage or variable output voltages with an external resistor divider. The Forced Bypass power saving mode can be chosen if voltage regulation is not required. The device consumes less than 3.5µA of current across the operating temperature range in Forced Bypass mode.

The ISL9120R5696 requires only a single inductor and very few external components. Power supply solution size is minimized by a 1.41mmx1.41mm WLCSP.

Related Literature

For a full list of related documents, visit our website:

- [ISL9120R5696](#) device page

Features

- Accepts input voltages above or below regulated output voltage
- Automatic Bypass mode functionality
- Automatic and seamless transitions between Buck and Boost modes
- Input voltage range: 1.8V to 5.5V
- Selectable Forced Bypass power saving mode
- Adaptive multilevel current limit scheme to optimize efficiency at low and high currents
- Output current: up to 800mA ($V_{IN} = 2.5V$, $V_{OUT} = 3.3V$)
- High efficiency: up to 98%
- 41µA quiescent current maximizes light-load efficiency
- Fully protected for over-temperature and undervoltage
- Small 1.41mmx1.41mm WLCSP
- Low profile 0.28mm total height (typical)

Applications

- Smartphones and tablets
- Portable consumer and wearable devices

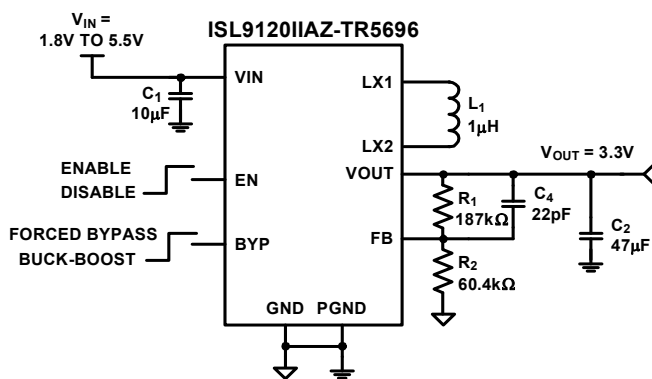


FIGURE 1. TYPICAL APPLICATION

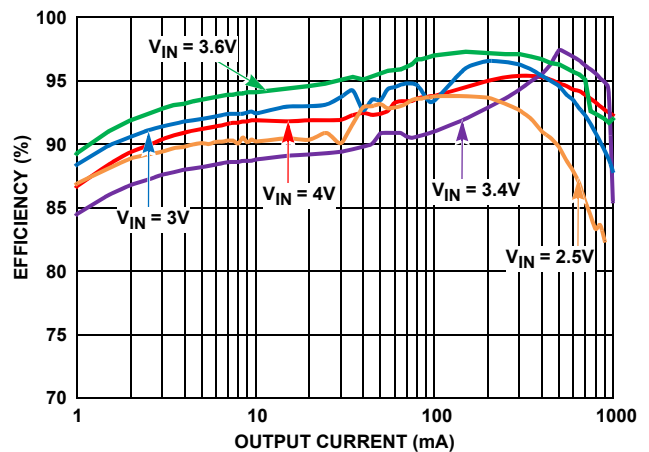


FIGURE 2. EFFICIENCY: $V_{OUT} = 3.3V$, $T_A = +25^\circ C$

Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	VOUT (V)	TEMP RANGE (°C)	TAPE AND REEL (UNITS) (Note 1)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL9120IIAZ-TR5696	20UT	ADJ.	-40 to +85	3k	9 Bump WLCSP	W3x3.9H
ISL9120IINZ-TR5696	20NT	3.3	-40 to +85	3k	9 Bump WLCSP	W3x3.9H

NOTES:

1. See [TB347](#) for details about reel specifications.
2. These Pb-free WLCSP packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e1 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free WLCSP packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. The Moisture Sensitivity Level (MSL) rating is 1. For more information about MSL, See [TB363](#).

Block Diagram

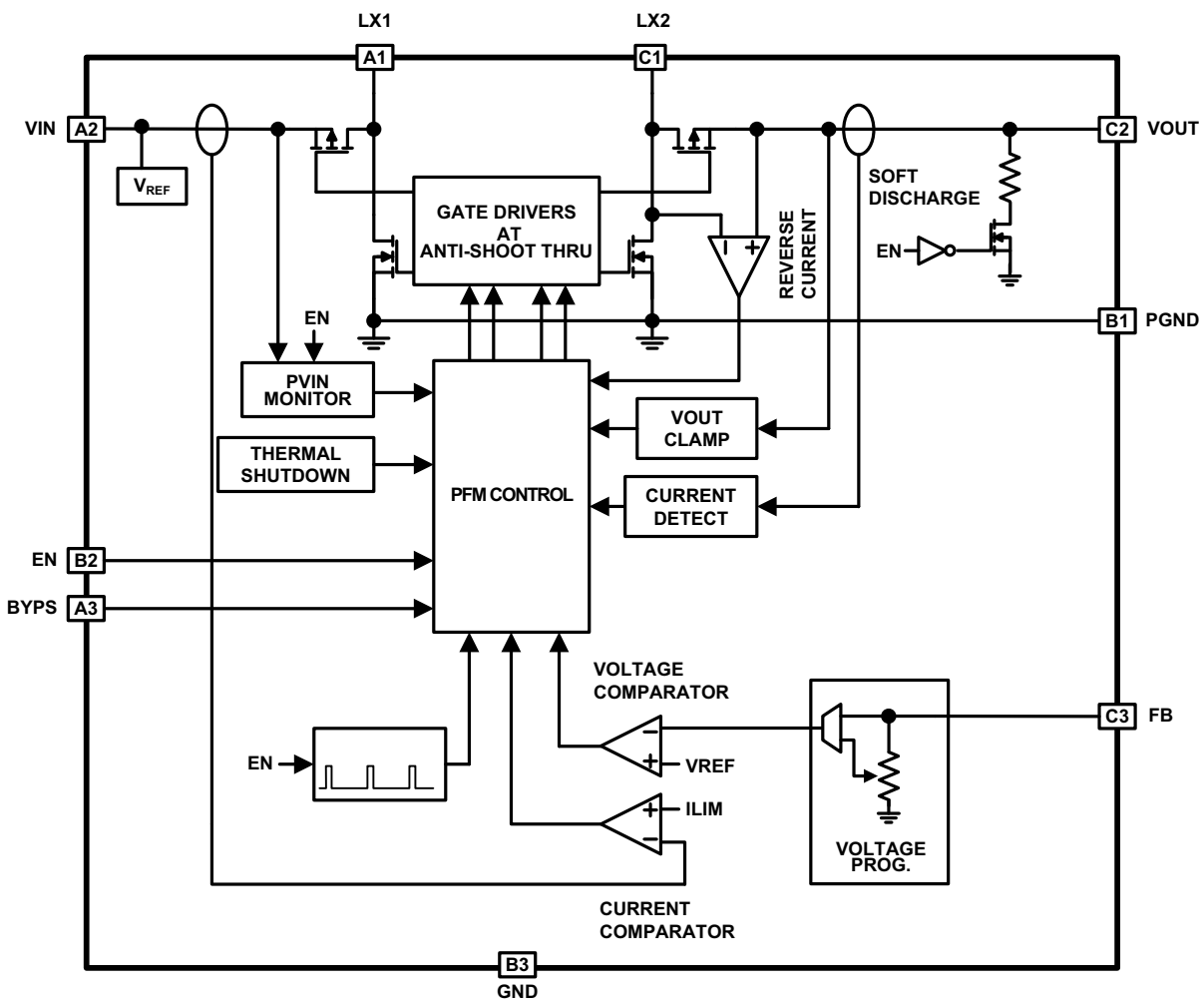
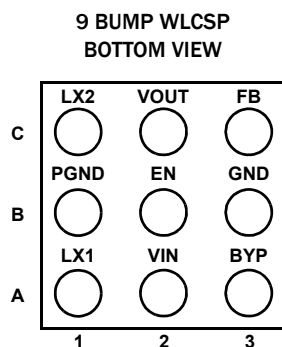


FIGURE 3. BLOCK DIAGRAM

Pin Configuration



Pin Descriptions

PIN #	PIN NAMES	DESCRIPTION
C2	VOUT	Buck-Boost output. Connect a 22 μ F or 47 μ F capacitor to PGND.
C1	LX2	Inductor connection, output side.
B1	PGND	Power ground for high switching current.
A1	LX1	Inductor connection, input side.
A2	VIN	Power supply input. Range: 1.8V to 5.5V. Connect a 10 μ F capacitor to PGND.
B2	EN	Logic input, drive HIGH to enable device. Do not leave floating.
A3	BYP	Forced Bypass mode enable pin. Logic high for Forced Bypass mode operation. Logic low for Buck-Boost mode operation. Do not leave floating.
B3	GND	Analog ground pin.
C3	FB	Voltage feedback pin. Connect directly to VOUT for the fixed version.

Absolute Maximum Ratings

V _{IN}	-0.3V to 6.5V
LX1, LX2	-0.3V to 6.5V
FB	-0.3V to 2.7V
GND, PGND	-0.3V to 0.3V
All Other Pins	-0.3V to 6.5V
ESD Rating	
Human Body Model (Tested per JESD22-A114F)	2.5kV
Machine Model (Tested per JESD22-A115C)	200V
Charged Device Model (Tested per JESD22-C101F)	2kV
Latch-Up (Tested per JESD78D; Class 2)	100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JB} (°C/W)
1.41x1.41 WLCSP (Notes 4, 5)	95	23
Maximum Junction Temperature	+125°C	
Storage Temperature Range	-65°C to +150°C	
Pb-Free Reflow Profile	see TB493	

Recommended Operating Conditions

Temperature Range	-40°C to +85°C
Supply Voltage (V _{IN}) Range	1.8V to 5.5V
Load Current (I _{OUT}) Range (DC)	0A to 800mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See [TB379](#).
- For θ_{JB} , the "board temp" is taken on the board near the edge of the package, on a copper trace at the center of one side. See [TB379](#).

Analog Specifications V_{IN} = V_{EN} = 3.6V, V_{OUT} = 3.3V, L₁ = 1μH, C₁ = 10μF, C₂ = 47μF, T_A = +25°C. **Boldface limits apply across the recommended operating temperature range, -40°C to +85°C and input voltage range (1.8V to 5.5V).**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
POWER SUPPLY						
Input Voltage Range	V _{IN}		1.8		5.5	V
V _{IN} Undervoltage Lockout Threshold	V _{UVLO}	Rising		1.725	1.795	V
		Falling	1.550	1.650		V
V _{IN} Supply Current	I _{VIN}	V _{OUT} = 3.7V (Note 7)		41	55	μA
V _{IN} Supply Current, Shutdown	I _{SD}	EN = GND		0.005	1	μA
V _{IN} Supply Current, Bypass Mode	I _{BYP}	BYP = logic high, V _{IN} ≤ 5V		0.8	3.5	μA
OUTPUT VOLTAGE REGULATION						
Output Voltage Range	V _{OUT}	I _{OUT} = 100mA. For adjustable output version (ISL9120IIAZ-TR5696)	1.00		5.20	V
Output Voltage Accuracy		V _{IN} = 3.7V, I _{OUT} = 1mA	-3		+4	%
FB Pin Voltage Regulation	V _{FB}	For adjustable output version (ISL9120IIAZ-TR5696)		0.80		V
FB Pin Bias Current	I _{FB}	For adjustable output version (ISL9120IIAZ-TR5696)			0.025	μA
Line Regulation, 500mA	$\Delta V_{OUT} / \Delta V_{IN}$	I _{OUT} = 500mA, V _{OUT} = 3.3V, V _{IN} step from 2.3V to 5.5V		0.00681		mV/mV
Load Regulation, 500mA	$\Delta V_{OUT} / \Delta I_{OUT}$	V _{IN} = 3.7V, V _{OUT} = 3.3V, I _{OUT} step from 0mA to 500mA		0.0072		mV/mA
Line Regulation, 100mA	$\Delta V_{OUT} / \Delta V_{I}$	I _{OUT} = 100mA, V _{OUT} = 3.3V, V _{IN} step from 2.3V to 5.5V		0.00273		mV/mV
Load Regulation, 100mA	$\Delta V_{OUT} / \Delta I_{OUT}$	V _{IN} = 3.7V, V _{OUT} = 3.3V, I _{OUT} step from 0mA to 100mA		0.05		mV/mA
Output Voltage Clamp	V _{CLAMP}	Rising	5.23		5.82	V
Output Voltage Clamp Hysteresis				400		mV
DC/DC SWITCHING SPECIFICATIONS						
LX1 Pin Leakage Current	I _{PFETLEAK}		-0.05		+0.05	μA
LX2 Pin Leakage Current	I _{NFETLEAK}	V _{IN} = 3.6V	-0.05		+0.05	μA

Analog Specifications $V_{IN} = V_{EN} = 3.6V$, $V_{OUT} = 3.3V$, $L_1 = 1\mu H$, $C_1 = 10\mu F$, $C_2 = 47\mu F$, $T_A = +25^\circ C$. **Boldface limits apply across the recommended operating temperature range, $-40^\circ C$ to $+85^\circ C$ and input voltage range (1.8V to 5.5V).** (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
SOFT-START AND SOFT DISCHARGE						
Soft-Start Time	t_{SS}	Time from when EN signal asserts to when output voltage ramp starts.		1		ms
		Time from when output voltage ramp starts to when output voltage reaches 95% of its nominal value with device operating in Buck mode. $V_{IN} = 4V$, $I_{OUT} = 500mA$		1		ms
		Time from when output voltage ramp starts to when output voltage reaches 95% of its nominal value with device operating in Boost mode. $V_{IN} = 3V$, $I_{OUT} = 500mA$		1		ms
V_{OUT} Soft-Discharge ON-Resistance	r_{DISCHG}	$EN < V_{IL}$		110		Ω
POWER MOSFET						
P-Channel MOSFET ON-Resistance	$r_{DS(on)_P}$	$I_{OUT} = 200mA$, measured with internal test mode		50		$m\Omega$
N-Channel MOSFET ON-Resistance	$r_{DS(on)_N}$	$I_{OUT} = 200mA$, measured with internal test mode		50		$m\Omega$
INDUCTOR PEAK CURRENT LIMIT						
Maximum Peak Current Limit	I_{LIM_MAX}			2		A
THERMAL PROTECTION						
Thermal Shutdown				150		$^\circ C$
Thermal Shutdown Hysteresis				35		$^\circ C$
LOGIC INPUTS						
Input Leakage	I_{LEAK}			0.013	0.500	μA
Input HIGH Voltage	V_{IH}		1.4			V
Input LOW Voltage	V_{IL}				0.4	V

NOTES:

- Parameters with MIN and/or MAX limits are 100% tested at $+25^\circ C$, unless otherwise specified. Temperature limits established by characterization and are not production tested.
- Quiescent current measurements are taken when the output is not switching.

Typical Performance Curves

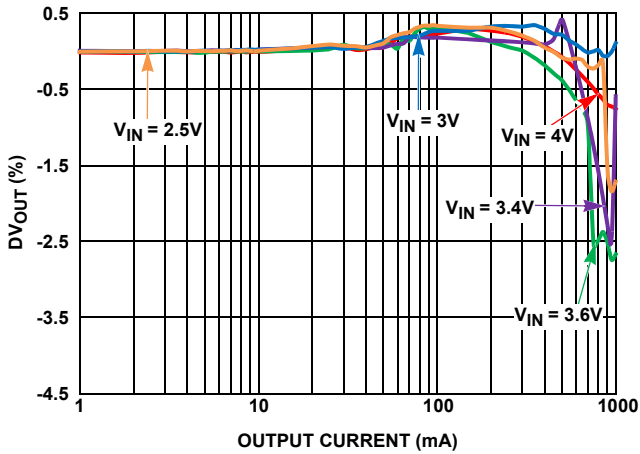


FIGURE 4. OUTPUT VOLTAGE vs OUTPUT CURRENT

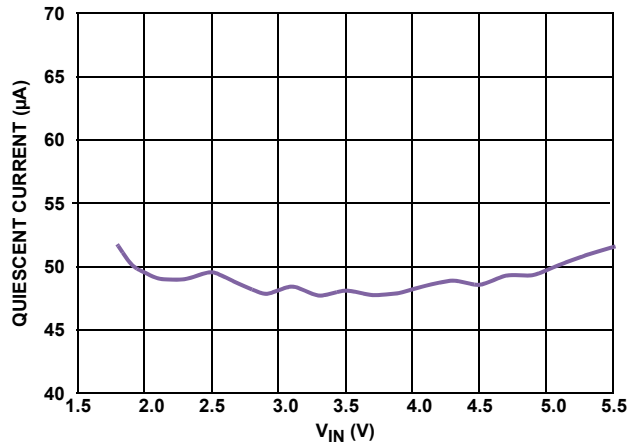


FIGURE 5. QUIESCENT CURRENT vs INPUT VOLTAGE (EN = HIGH)

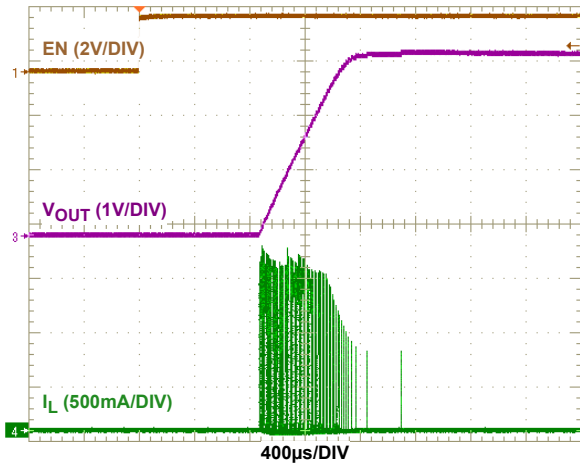


FIGURE 6. SOFT-START ($V_{IN} = 4V$, $V_{OUT} = 3.3V$, NO LOAD)

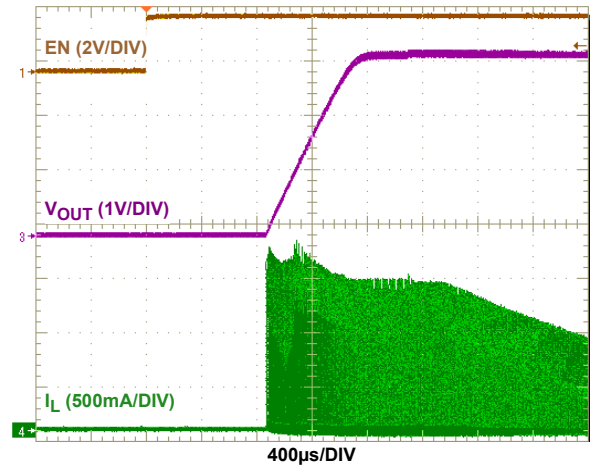


FIGURE 7. SOFT-START ($V_{IN} = 4V$, $V_{OUT} = 3.3V$, $0.5A R_{LOAD}$)

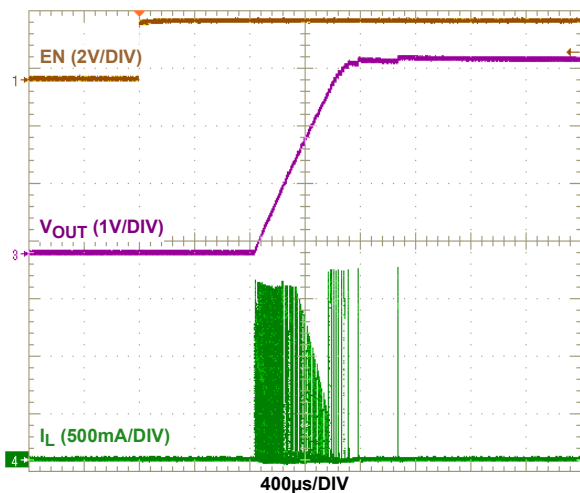


FIGURE 8. SOFT-START ($V_{IN} = 3V$, $V_{OUT} = 3.3V$, NO LOAD)

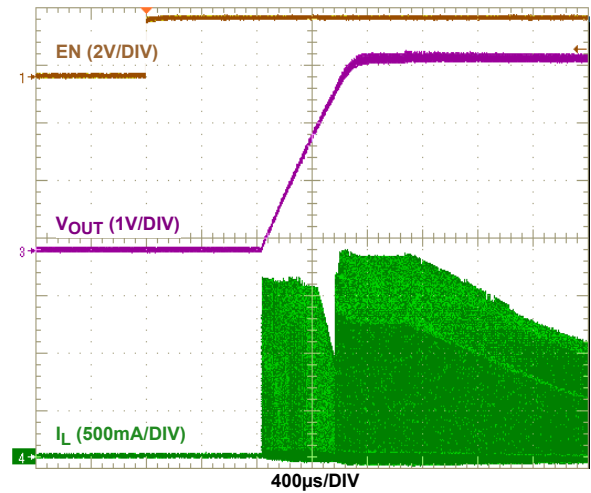


FIGURE 9. SOFT-START ($V_{IN} = 3V$, $V_{OUT} = 3.3V$, $0.5A R_{LOAD}$)

Typical Performance Curves (Continued)

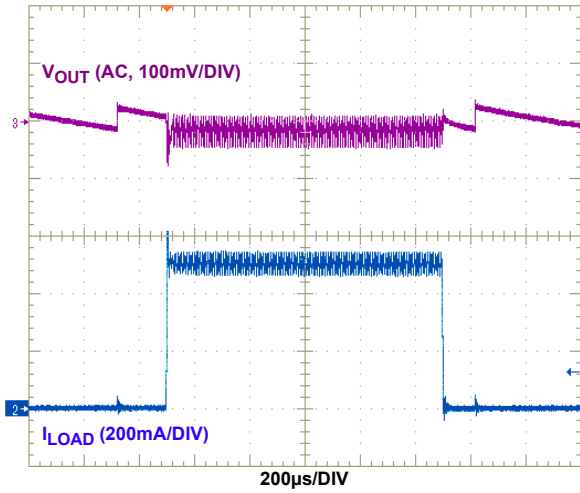


FIGURE 10. 0A TO 0.5A LOAD TRANSIENT ($V_{IN} = 4V$, $V_{OUT} = 3.3V$)

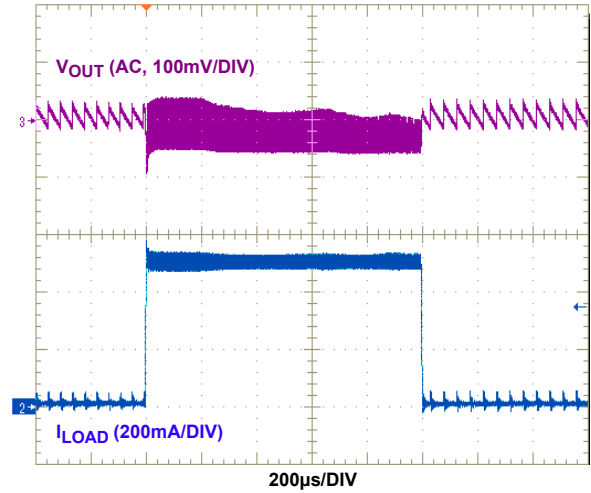


FIGURE 11. 0.01A TO 0.5A LOAD TRANSIENT ($V_{IN} = 4V$, $V_{OUT} = 3.3V$)

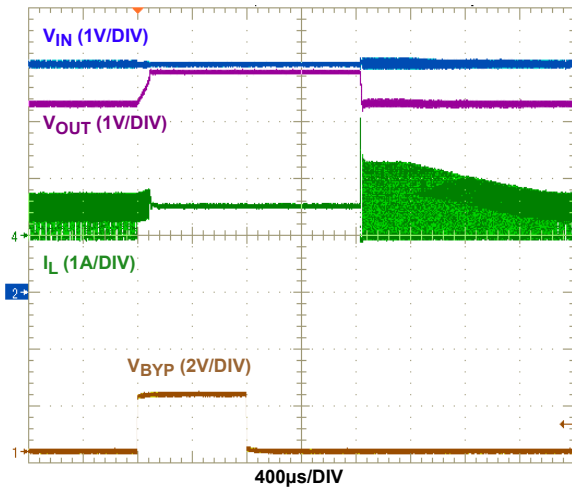


FIGURE 12. BYPASS FUNCTIONALITY ($V_{IN} = 4V$, $V_{OUT} = 3.3V$, $0.5A R_{LOAD}$)

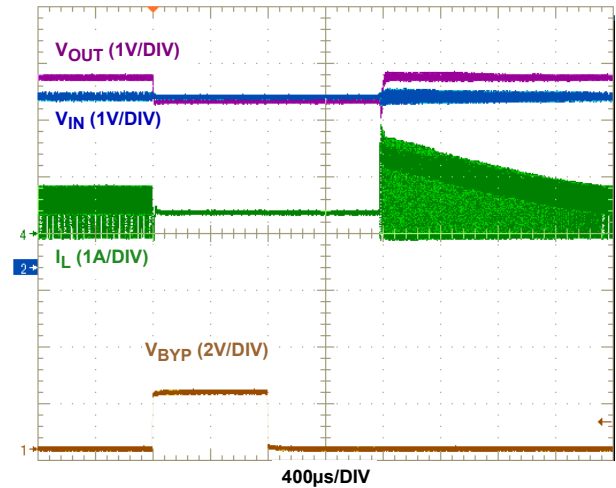


FIGURE 13. BYPASS FUNCTIONALITY ($V_{IN} = 3V$, $V_{OUT} = 3.3V$, $0.5A R_{LOAD}$)

Functional Description

Functional Overview

The ISL9120R5696 implements a complete buck-boost switching regulator with a PFM controller, internal switches, references, protection circuitry, and control inputs. For more information, see the [“Block Diagram” on page 2](#).

The PFM controller automatically switches between Buck and Boost modes as necessary to maintain a steady output voltage with changing input voltages and dynamic external loads.

Internal Supply and References

Referring to the [“Block Diagram” on page 2](#), the VIN pin supplies input power to the DC/DC converter and provides the operating voltage source required for stable VREF generation. Separate ground pins (GND and PGND) help avoid problems caused by ground shift due to the high switching currents.

Enable Input

A master enable pin, EN, allows the device to be enabled. Driving EN logic low invokes a power-down mode, in which most internal device functions, including input and output power-good detection, are disabled.

Bypass Input

The Bypass Enable pin, BYP, allows the device to provide a direct connection from the VIN pin to the VOUT pin. The connection between the VIN and VOUT pins is through the external inductor and two internal power transistors. This function, called Forced Bypass mode operation, provides a very low quiescent current state.

For Forced Bypass mode operation, the minimum time required while in forced bypass operation is 800µs. When exiting forced bypass operation, the minimum time required before reentering Forced Bypass mode operation is 1ms.

Soft Discharge

When the device is disabled by driving EN logic low, an internal resistor between the VOUT and GND pins is activated. This internal resistor has a typical resistance of 110Ω.

POR Sequence and Soft-Start

Bringing the EN pin logic high allows the device to power up. Several events occur during the start-up sequence. The internal voltage reference powers up and stabilizes. The device then starts operating. A 1ms (typical) delay occurs between assertion of the EN pin and the start of the switching regulator soft-start ramp.

The soft-start feature minimizes output voltage overshoot and input inrush currents. During soft-start, the reference voltage is ramped to provide a ramping output voltage.

When the target output voltage is higher than the input voltage, a transition from Buck mode to Boost mode occurs during the soft-start sequence. At the time of this transition, the reference voltage ramp rate is decreased, such that the output voltage slew rate is decreased. This provides a slower output voltage slew rate.

Undervoltage Lockout

The Undervoltage Lockout (UVLO) feature prevents abnormal operation if the supply voltage is too low to guarantee proper operation. The regulator is disabled when the VIN pin voltage falls below the UVLO threshold.

Thermal Shutdown

A built-in thermal protection feature protects the ISL9120R5696 if the die temperature reaches +150 °C (typical). At this die temperature, the regulator is completely shut down. The die temperature continues to be monitored in this thermal shutdown mode. When the die temperature falls to +115 °C (typical), the device resumes normal operation.

When exiting thermal shutdown, the ISL9120R5696 executes its soft-start sequence.

Buck-Boost Conversion Topology

The ISL9120R5696 operates in either Buck or Boost mode. When operating in conditions in which V_{IN} is close to V_{OUT} , the ISL9120R5696 alternates between Buck mode, Boost mode, and Automatic Bypass modes of operation as necessary to provide a regulated output voltage.

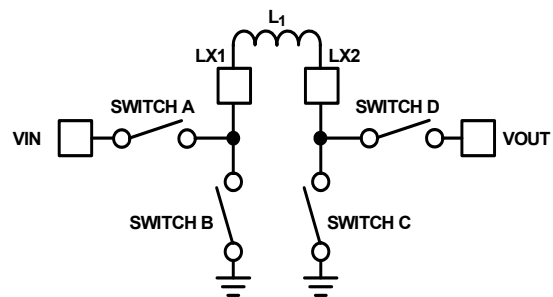


FIGURE 14. BUCK-BOOST TOPOLOGY

[Figure 14](#) shows a simplified diagram of the internal switches and external inductor.

PFM Operation

During PFM operation in Buck mode, Switch D is continuously closed and Switch C is continuously open. Switches A and B operate in discontinuous mode during PFM operation. During PFM operation in Boost mode, the ISL9120R5696 closes Switch A and Switch C to ramp-up the current in the inductor. When the inductor current reaches the current limit, the device turns OFF Switches A and C, then turns ON Switches B and D. With Switches B and D closed, output voltage increases as the inductor current ramps down.

As shown in [Figure 15 on page 9](#), multiple PFM pulses charge up the output capacitor, depending on output current. These pulses continue until V_{OUT} reaches the upper threshold of the PFM hysteretic, which is at 1.5% above the nominal output voltage. Switching then stops and remains stopped until V_{OUT} decays to the lower threshold of the voltage hysteretic, which is the nominal output voltage. PFM operation repeats when V_{OUT} decays to the nominal output voltage.

Variable Peak Current Limit Scheme

The ISL9120R5696 implements a multilevel current limit scheme with 32 levels between 350mA and 2A to optimize efficiency across the output current range. The transition from one level to the other is determined by the number of pulses in a PFM burst (pulse count) as shown in Figure 16. At a given peak current limit level, the pulse count increases as the output current increases. When the pulse count reaches the upper threshold at the existing current limit, the

current limit switches to the next higher level. Similarly, if the pulse count reaches the lower threshold at the existing current limit, the device switches to the next lower level of peak current limit. If the pulse count reaches the upper threshold at the highest current limit, the current limit does not rise any further. Increasing the output current beyond this point can cause the output to lose voltage regulation.

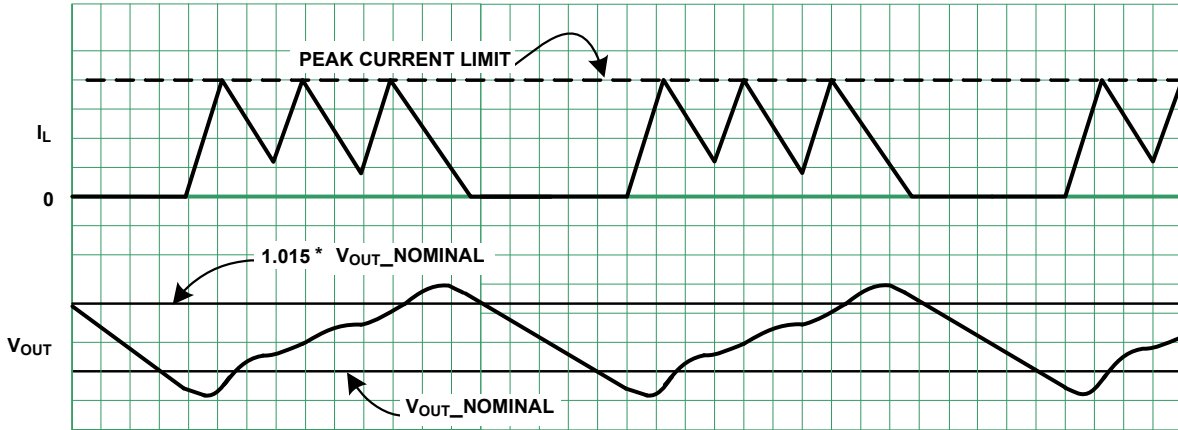


FIGURE 15. PFM MODE OPERATION CONCEPT

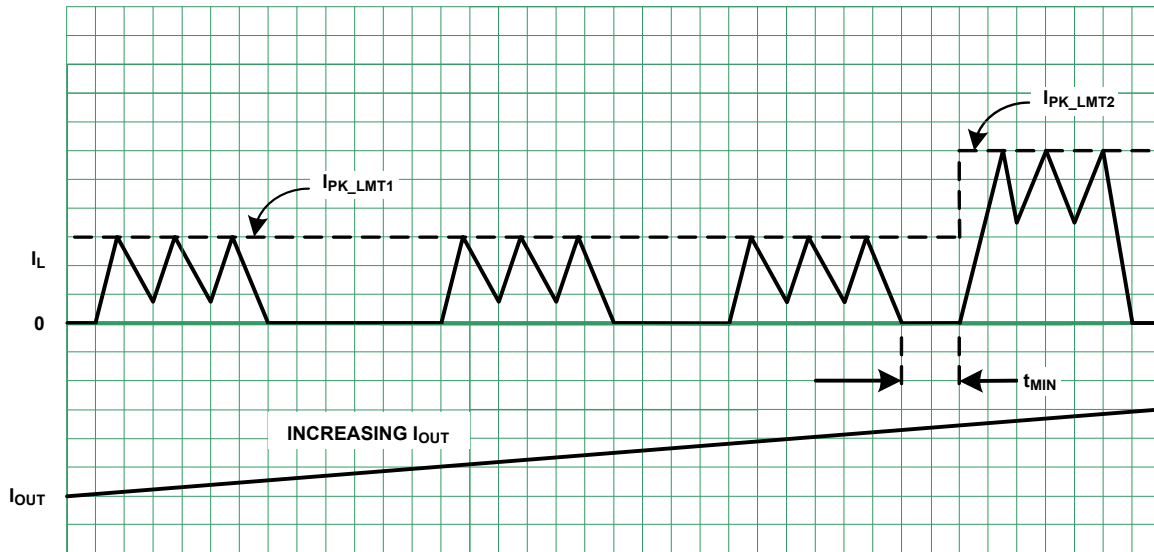


FIGURE 16. PEAK CURRENT LIMIT STEP UP TRANSITION

Automatic Bypass Mode Operation

When the output voltage is close to the input voltage, generally within 1% to 2%, the ISL9120R5696 engages Automatic Bypass mode operation, which produces a direct connection between the VIN and VOUT pins. This behavior provides excellent efficiency and very low output voltage ripple.

Forced Bypass Mode Operation

Forced Bypass mode operation is intended for applications in which the output regulation is not important but the device quiescent current consumption is important. One example is if the buck-boost regulator is providing power to an LDO and the LDO is in standby mode with near zero output current. Under this condition, putting the buck-boost regulator in Bypass mode has essentially no impact on the LDO but save the 41µA quiescent current consumption on the buck-boost regulator.

Because the Bypass mode is an extreme power saving mode, there is no overcurrent protection. Therefore, use caution not to overload or short-circuit the device. Power-up at Bypass mode is not recommended.

Applications Information

Component Selection

The adjustable output version (ISL9120IIAZ-TR5696) requires three components to program the output voltage. Two external resistors program the output voltage and a small capacitor improves transient response.

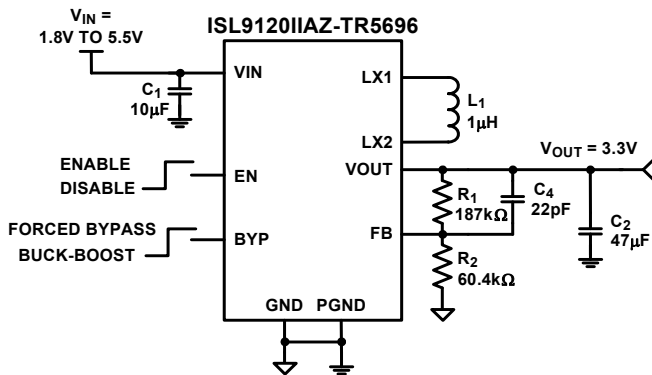


FIGURE 17. TYPICAL ISL9120IIAZ-TR6596 APPLICATION

Output Voltage Programming

Use an external resistor divider to program the output voltage.

Use Equation 1 to derive the R_1 and R_2 resistor values:

$$V_{OUT} = 0.8V \cdot \left(1 + \frac{R_1}{R_2}\right) \quad (\text{EQ. 1})$$

When designing a PCB, include a GND guard band around the FB resistor network to reduce noise and improve accuracy and stability. Place resistors R_1 and R_2 close to the FB pin. The suggested value of the R_1 resistor is 187k.

Feed-Forward Capacitor Selection

A small capacitor (C_4 in Figure 17) in parallel with resistor R_1 is required to provide the specified load and line regulation. The suggested value of this capacitor is 22pF for $R_1 = 187k$. An NPO type capacitor is recommended.

Fixed Output Version FB Pin Connection

The fixed output version (ISL9120IINZ-TR5696) does not require external resistors or a capacitor on the FB pin. Simply connect the VOUT directly to the FB pin.

Inductor Selection

Use an inductor with high frequency core material (such as ferrite core) to minimize core losses and provide good efficiency. The inductor must be able to handle the peak switching currents without saturating.

A 1µH inductor with $\geq 2A$ saturation current rating is recommended. Select an inductor with low DCR to provide good efficiency. A toroidal or shielded inductor can be used in applications in which radiated noise must be minimized.

TABLE 1. INDUCTOR VENDOR INFORMATION

MFR	SERIES	DIMENSION (mm)	DCR (mΩ) TYP	ISAT (A) TYP
Toko	DFE201610R-H-1R0M	2.0x1.6x1.0	66	2.7
Cyntec	PIFE20161T-1R0MS	2.0x1.6x1.0	65	2.8
TDK	TFM201610GHM-1R0MTAA	2.0x1.6x1.0	50	3.8

Capacitor Selection

The input and output capacitors should be ceramic X5R type with low ESL and ESR. The recommended input capacitor value is 10µF.

The recommended 10µF input capacitor should have the following minimum characteristics: 0603 case size, X5R temperature range, and 10V voltage rating. The recommended V_{OUT} capacitor values are 22µF or 47µF.

The recommended 47µF output capacitor should have the following minimum characteristics: 0603 case size, X5R temperature range, and 6.3V voltage rating.

The recommended 22µF output capacitor should have the following minimum characteristics: 0603 case size, X5R temperature range, and 10V voltage rating.

TABLE 2. CAPACITOR VENDOR INFORMATION

MANUFACTURER	SERIES	WEBSITE
AVX	X5R	www.avx.com
Murata	X5R	www.murata.com
TDK	X5R	www.tdk.com

Recommended PCB Layout

Correct PCB layout is critical for proper operation of the ISL9120R5696. The input and output capacitors should be positioned as close to the IC as possible. The ground connections of the input and output capacitors should be kept as short as possible and should be on the component layer to avoid problems that are caused by high switching currents flowing through PCB vias.

Revision History The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Jan 31, 2019	FN8894.4	Added Related Literature. Added fixed VOUT version information throughout. Ordering Information - added ISL9120IINZ-TR5696. Updated disclaimer
Apr 19, 2018	FN8894.3	Updated VIN Undervoltage Lockout Threshold maximum and Output Voltage Clamp minimum values in Analog Specifications on page 4.
Feb 2, 2018	FN8894.2	In the Features list on page 1, changed "0.3mm total height" to "0.28mm total height". Updated the POD to the current version. Changes since last revision: Side View: changed dimensions 0.132 +/- 0.030 to 0.130 +/-0.015 0.150 +/-0.050 to 0.150 +/-0.025 Removed About Intersil section and added Renesas disclaimer.
Nov 16, 2017	FN8894.1	Removed mention of the fixed output version. Removed the redundant "Output Voltage Programming" section Updated the part marking from "20AT" to "20UT".
May 26, 2017	FN8894.0	Initial release

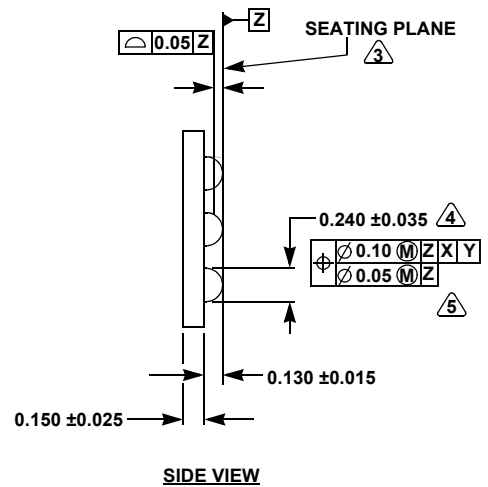
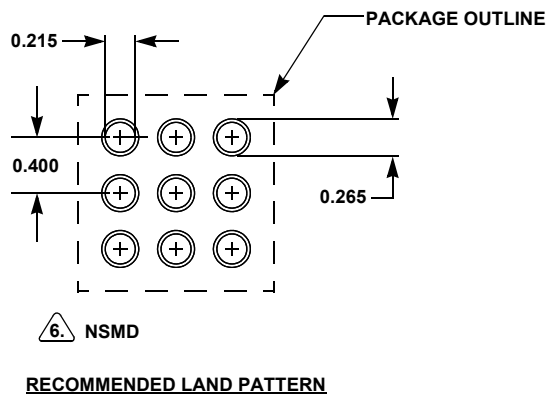
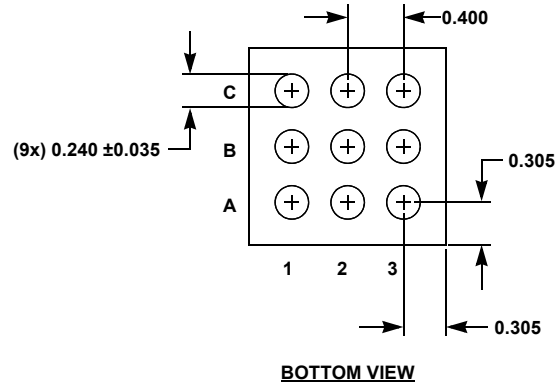
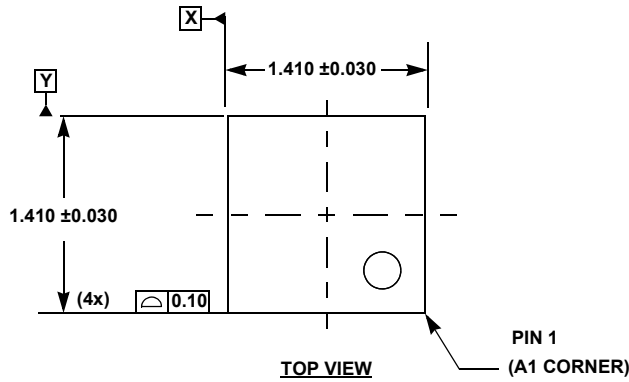
Package Outline Drawing

For the most recent package outline drawing, see [W3x3.9H](#).

W3x3.9H

9 BALL 3x3 ARRAY ULTRA THIN WAFER LEVEL CHIP SCALE PACKAGE (WLCSP) 0.4mm Pitch

Rev 2, 11/17



NOTES:

1. All dimensions are in millimeters.
2. Dimensions and tolerance per ASME Y14.5 - 1994.
3. Primary datum **Z** and seating plane are defined by the spherical crowns of the bump.
4. Dimension is measured at the maximum bump diameter parallel to primary datum **Z**.
5. Bump position designation per JESD 95-1, SPP-010.
6. NSMD refers to non-solder mask defined pad design per [TB451](#).