User's Manual

ISL91211A-BIK-REFZ, ISL91211AIK-REFZ, ISL91211BIK-REF2Z

User's Manual: Reference Boards

Core Power Solutions

Renesas Electronics Corporation
www.renesas.com

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ISL91211A-BIK-REFZ, ISL91211AIK-REFZ, ISL91211BIK-REF2Z

Reference Boards

The Renesas Xilinx FPGA reference board is an expandable power supply designed to provide the various Xilinx power rails to the Xilinx Artix-7, Spartan-7, and Zynq-7000 families. The design uses the power source from the DC power supply or a plug-in AC/DC adapter to the barrel jack of this reference board.

The ISL91211AIK and ISL91211BIK provide four independent One Time Programmable (OTP) voltage defaults for each buck output. This flexibility supports an expandable and optimized power supply from a Xilinx high-end product to a low-end product. This reference board is designed specifically to solve the complex FPGAs and SoC devices. You can combine this reference design with your Xilinx FPGA or SoC motherboard platform.

Key Features

- 5V AC/DC adapter or DC power input
- Power outputs support different skews Xilinx Artix-7, Spartan-7, and Zynq-7000 FPGAs
- Supports different output voltages through DVS control signals (pull-up/down resistors)
- Complete power validation hardware and software tools – I^2C interface and Power Navigator (GUI)
- Design files and documents are available to minimize system design efforts

Ordering Information

Part Number	Description
ISL91211A-BIK-REFZ	Renesas Xilinx Artix-7 (XC7A200T) reference board
ISL91211AIK-REFZ	Renesas Xilinx Zynq-7000 reference board
ISL91211BIK-REF2Z	Renesas Xilinx Spartan-7 Reference board

Related Literature

For a full list of related documents, visit our website:

- ISL91211AIK, ISL91211BIK, ISL21010DFH312, ISL9123, ISL80030 device pages

1. Functional Description

1.1 Power-Up Sequencing

The Xilinx Artix-7/Vertex-7/Zynq-7000 power sequence begins by turning on a mechanical switcher. When the input voltage ramps up and is stable, it triggers Power Enable signals (EN_1/EN_VCCIO_2V5/EN_VCCIO_3V3) with a timely order by an external RC time constant to the system, which is generated by turning on the mechanical switcher. The ISL91211AIK and the ISL91211BIK have an internal 1.4ms boot-up delay after EN_1 is asserted. The internal power delays (set by OTP) provide the necessary delays based on the Xilinx FPGA requirements. The timing diagram for the power sequencing is shown in Figure 1.

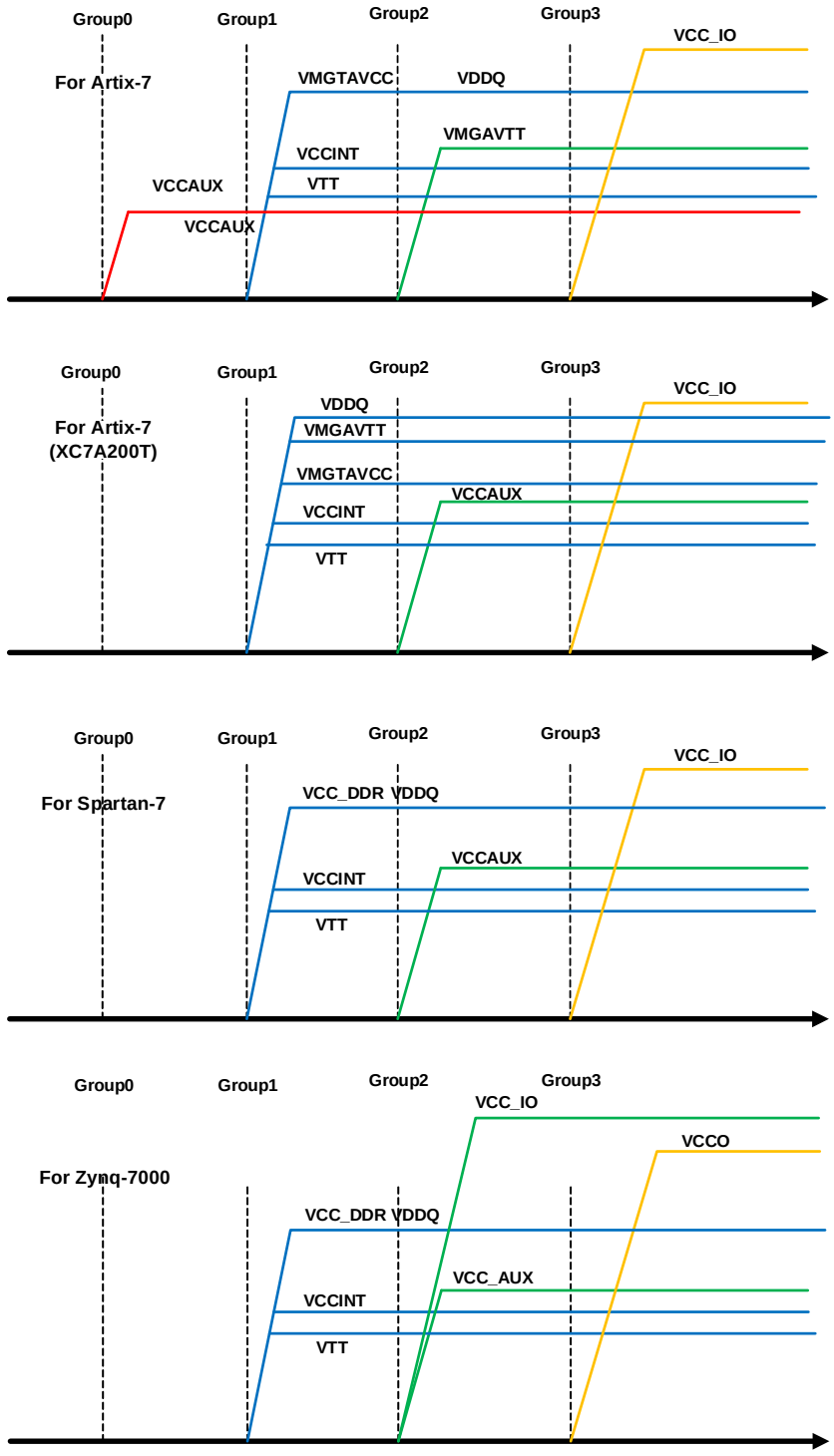


Figure 1. Xilinx Power-Up Sequence

1.2 Power Block Diagram

This Renesas FPGA reference board supports Xilinx Artix-7, Spartan-7, and Zynq-7000. The ISL91211AIK and ISL91211BIK are able to provide the multiple power rails for VCCINT, VCCAUX, VMGTAVTT, VMGTAVCC, and DDR3/DDR4/LPDDR2/LPDDR3/DDR3L by choosing the DVS option. The solution size for each reference board can be estimated with the silkscreen for the solution. To meet the recommended power-on sequence to achieve minimum current draw for VCCINT, VMGTAVCC, and VMGTAVTT, the power-up sequence is provided in a timely manner.

The ISL91211AIK and ISL91211BIK have four independently programmable voltage settings for each buck controller, that can be used to set the output voltage. They are DVS0, DVS1, DVS2, and DVS3. By changing the DVS number selected, the corresponding output voltage is selected. To configure DVS, DVS_PIN1(MPIO1), and DVS_PIN0(MPIO0), set the active DVS by setting IO_PINMODE = 0x4, which is in combination with BUCKx_DVSPIN_CTRL[1:0] = 0x3 (OTP factory value) in the BUCKx_DVSCFG register.

Table 1. Global DVS Pin Logic

DVS_PIN1 (MPIO1)	DVS_PIN0 (MPIO0)	Active DVS
0	0	DVS0
0	1	DVS1
1	0	DVS2
1	1	DVS3

1.3 Renesas FPGA Power Evaluation Board Outline

The evaluation board is classified into four different Xilinx FPGA applications, such as Artix-7, Artix-7(XC7A200T), Spartan-7, and Zynq-7000. The Artix-7 application requires the ISL91211AIK and ISL91211BIK PMICs, although the Spartan-7 and Zynq-7000 need only one PMIC. See Figure 2.

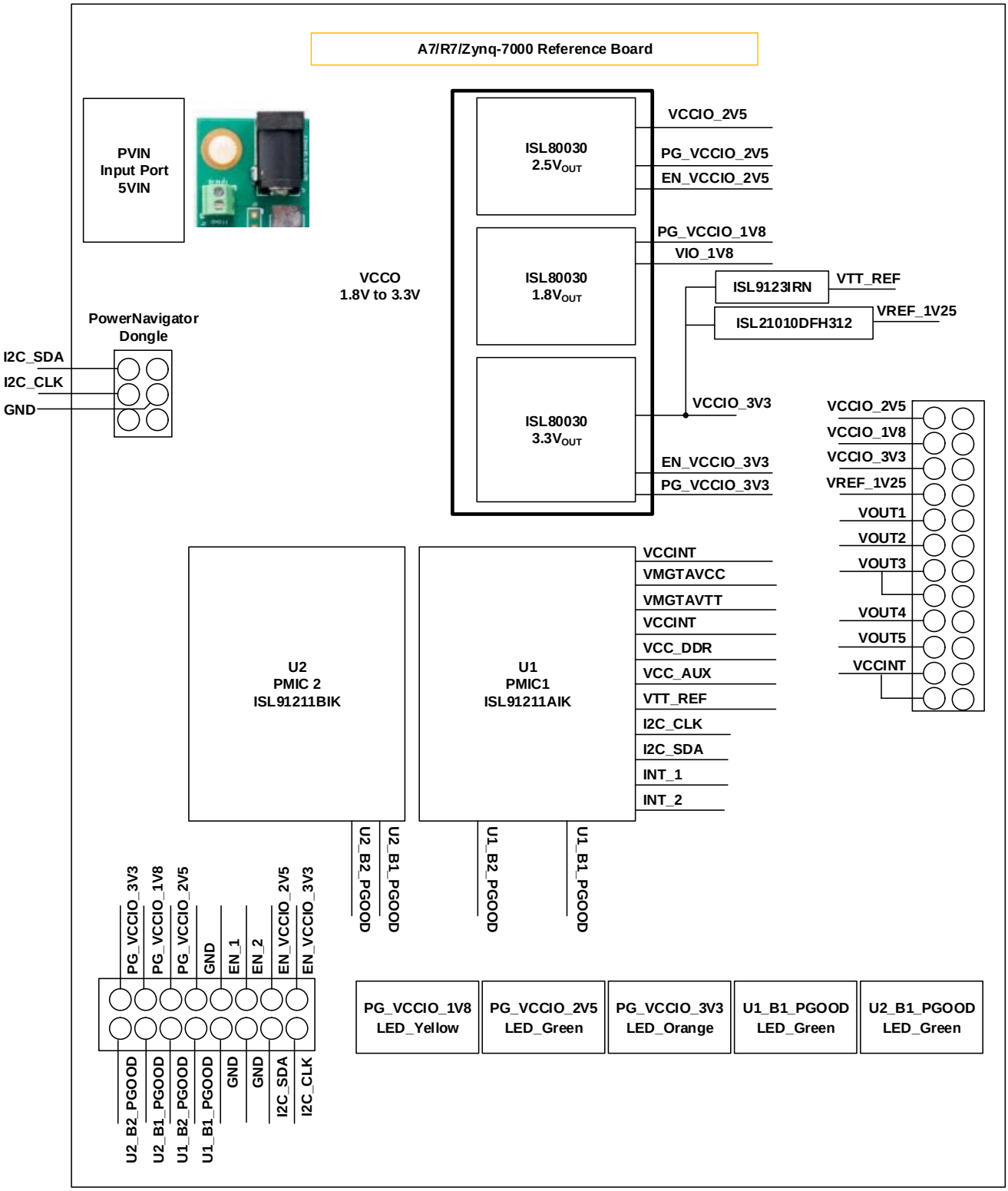


Figure 2. Renesas Evaluation Board Outline for Xilinx Artix-7/Spartan-7/Zynq-7000 FPGA

1.3.1 Artix-7 FPGA

Highlights for Aritx-7 FPGA solution:

- The reference board uses 5V input from a plug-in AC/DC (5V) adapter or DC power supply
- The ISL91211BIK is required for multiple power rails
- Optional ISL21010DFH312 is for XADC input voltage, 1.25V ±0.2% accuracy
- The ISL80030 supports VCCO and VCC_IO, 3.3V/2.5V/1.8V

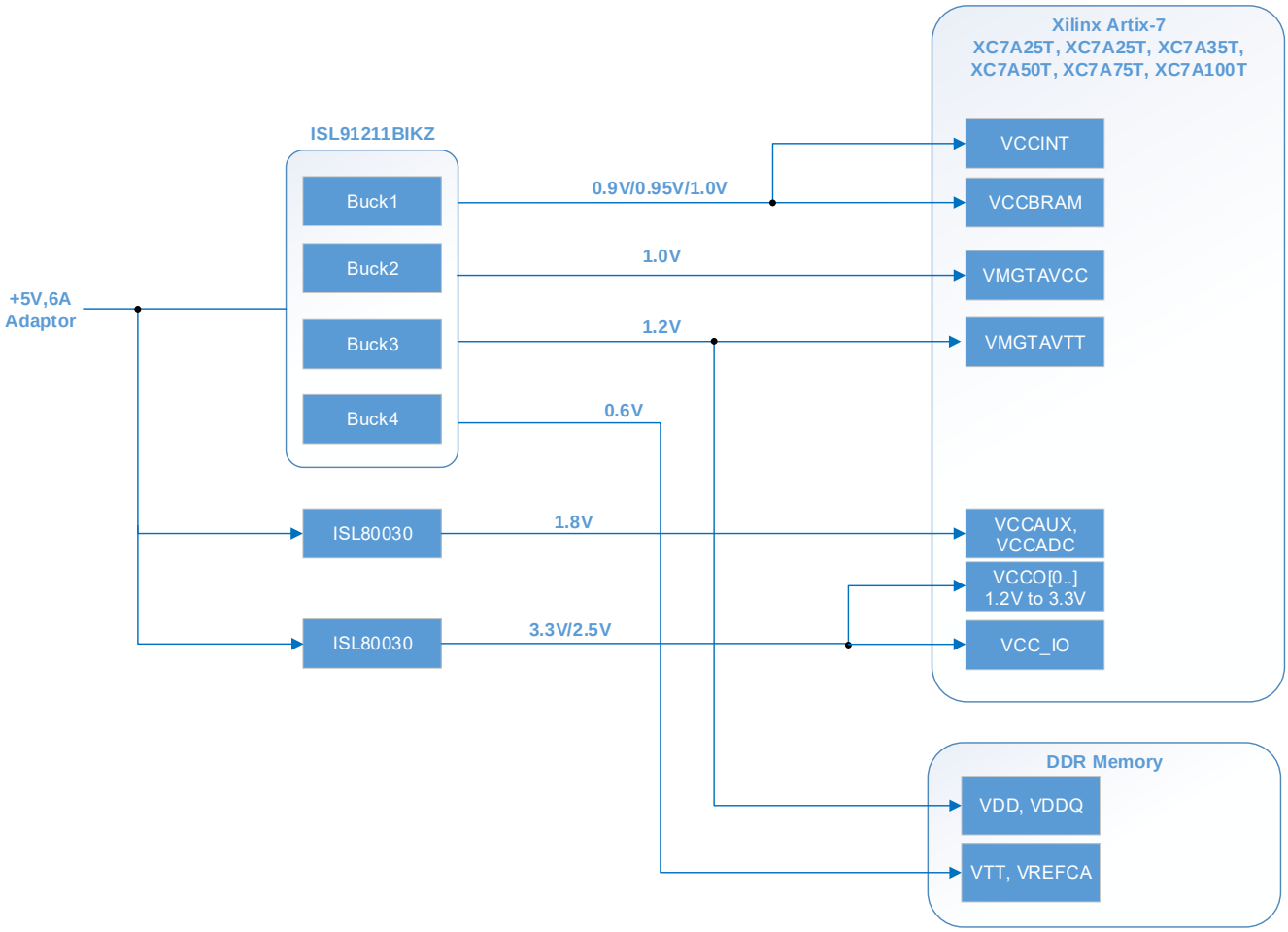


Figure 3. Artix-7 FPGA Block Diagram

Table 2. ISL91211BIKZ-TR5877 DVS Output Option for Artix-7 Power Rail

Artix-7 Rail	ISL91211BIK (1+1+1+1)	ISL91211BIKZ-TR5877 (I^2C Slave Address = 0x62)		
	DVS_PIN1/DVS_PIN0	00	01	11
VCCINT	VOUT1	0.90V	0.95V	1.0V
VMGTAVCC	VOUT2	1.0V	1.0V	1.0V
VMGAVTT, VDDQ	VOUT3	1.2V	1.2V	1.2V
VTT	VOUT4	0.6V	0.6V	0.6V

1.3.2 Artix-7(XC7A200T) FPGA

Highlights for Artix-7(XC7A200T) FPGA solution:

- A high-performance Xilinx Artix-7 XC7A200T solution
- The reference board uses 5V input from a plug-in AC/DC (5V) adapter or DC power supply
- The ISL91211AIK and ISL91211BIK are required for multiple power rails
- Optional ISL21010DFH312 is for XADC input voltage, 1.25V ±0.2% accuracy
- The ISL80030 supports VCCO and VCC_IO, 3.3V/2.5V/1.8V

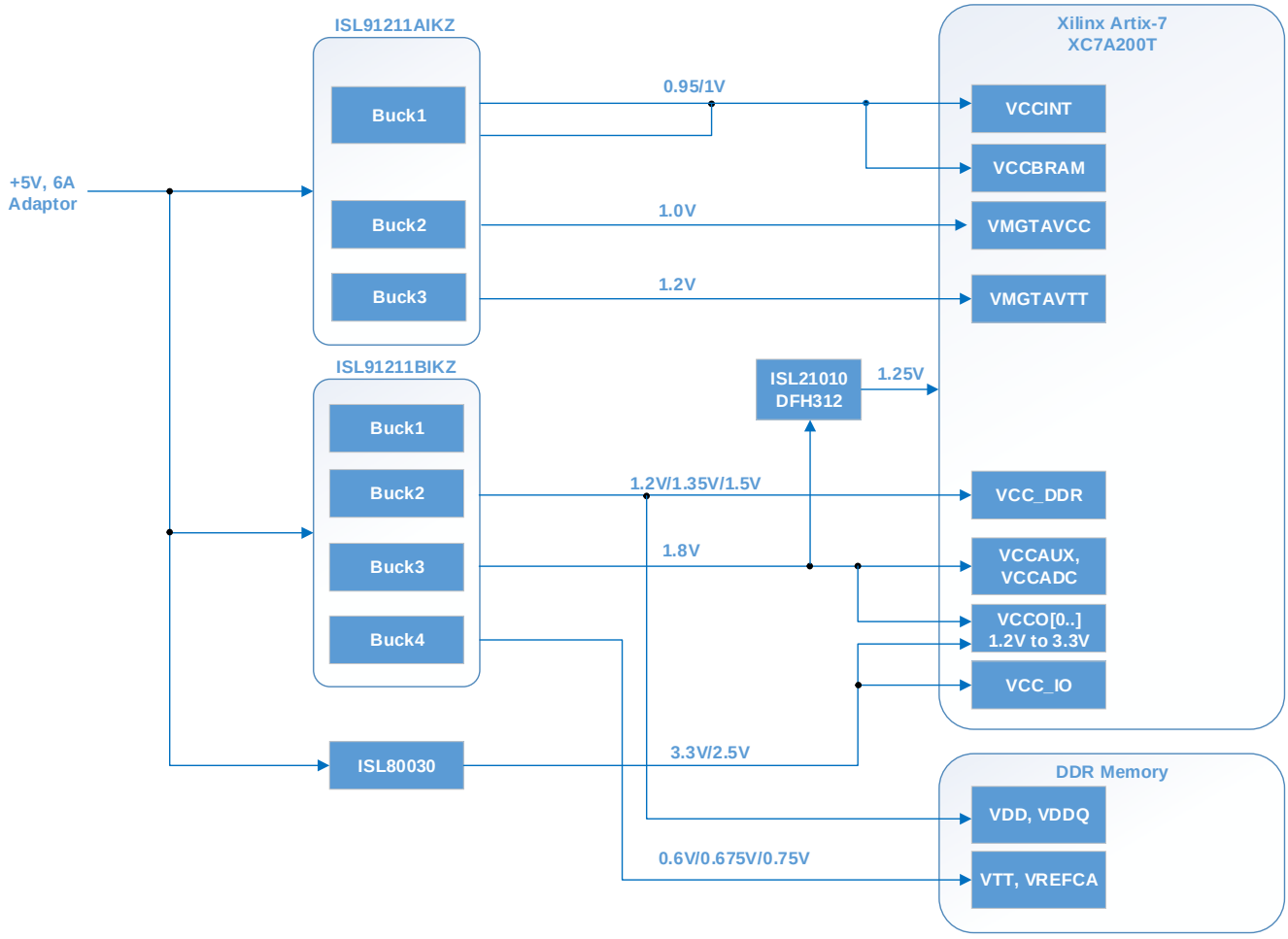


Figure 4. Artix-7 FPGA Block Diagram

Table 3. ISL91211AIKZ-TR5873 DVS Output Option for Artix-7 (XC7A200T) Power Rail

Artix-7 Rail	ISL91211AIK (2+1+1)	ISL91211AIKZ-TR5873 (I^2C Slave Address = 0x60)	
	DVS_PIN1/DVS_PIN0	00	01
VCCINT, VCCBRAM	VOUT1	0.95V	1.0V
VMGTAVCC	VOUT2	1.0V	1.0V
VMGTAVTT	VOUT3	1.2V	1.2V

Table 4. ISL91211BIKZ-TR5875 and ISL91211BIKZ-TR5876 DVS Output Option for Artix-7(XC7A200T) Power Rail

Artix-7 Rail	ISL91211BIK (1+1+1+1)	ISL91211BIKZ-TR5875 (I^2C Slave Address = 0x62)				ISL91211BIKZ-TR5876 (I^2C Slave Address = 0x62)			
	DVS_PIN1/DVS_PIN0	00	01	10	11	00	01	10	11
Reserved	VOUT1	Off	Off	Off	Off	Off	Off	Off	Off
VDDQ	VOUT2	1.35V	1.35V	1.5V	1.5V	1.2V	1.2V	1.5V	1.5V
VCCAUX/ADC	VOUT3	1.8V	1.8V	1.8V	1.8V	1.8V	1.8V	1.8V	1.8V
VTT	VOUT4	0.675V	0.675V	0.75V	0.75V	0.6V	0.6V	0.75V	0.75V

1.3.3 Spartan-7 FPGA

Highlights for Spartan-7 FPGA solution:

- The reference board uses 5V input from a plug-in AC/DC (5V) adapter or DC power supply
- The ISL91211BIK is required for VCCINT, VCCBRAM, VCC_DDR, VCCAUX, and VTT
- The ISL80030 supports VCCO and VCC_IO, 3.3V/2.5V/1.8V

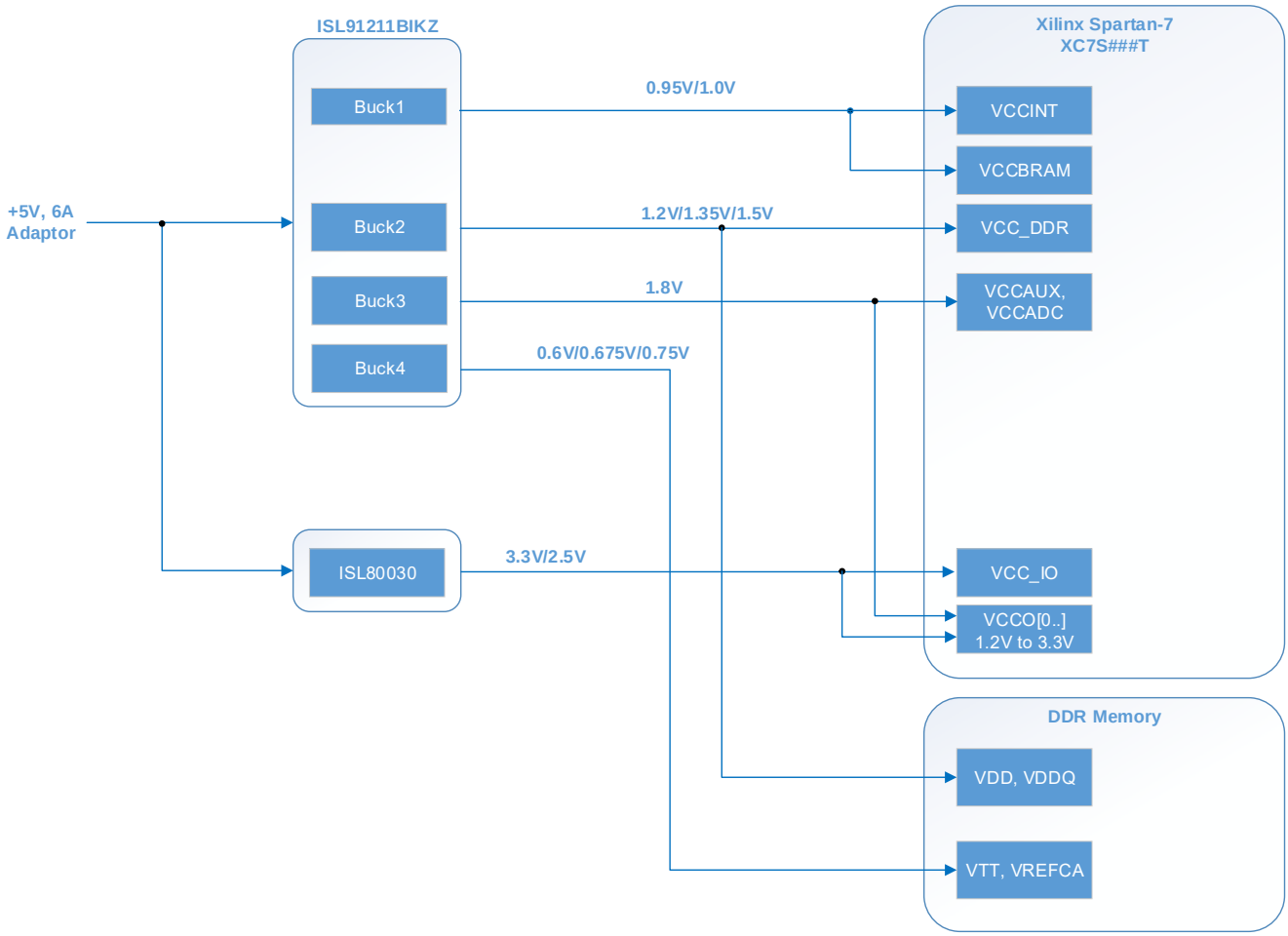


Figure 5. Spartan-7 FPGA Block Diagram

Table 5. ISL91211BIKZ-TR5878 and ISL91211BIKZ-TR5879 DVS Output Option for Spartan-7 Power Rail

Spartan-7 Rail	ISL91211BIK (1+1+1+1)	ISL91211BIKZ-TR5878 (I^2C Slave Address = 0x62)			
	DVS_PIN1/DVS_PIN0	00	01	10	11
VCCINT	VOUT1	0.95V	1.0V	0.95V	1.0V
VCC_DDR	VOUT2	1.35V	1.35V	1.5V	1.5V
VCCAUX/ADC	VOUT3	1.8V	1.8V	1.8V	1.8V
VTT	VOUT4	0.675V	0.675V	0.75V	0.75V

Spartan-7 Rail	ISL91211BIK (1+1+1+1)	ISL91211BIKZ-TR5879 (I^2C Slave Address = 0x62)			
	DVS_PIN1/DVS_PIN0	00	01	10	11
VCCINT	VOUT1	0.95V	1.0V	0.9V	0.9V
VCC_DDR	VOUT2	1.2V	1.2V	1.35V	1.35V
VCCAUX/ADC	VOUT3	1.8V	1.8V	1.8V	1.8V
VTT	VOUT4	0.6V	0.6V	0.675V	0.675V

1.3.4 Zynq-7000 FPGA

Highlights for Spartan-7 FPGA solution:

- The reference board uses 5V input from a plug-in AC/DC (5V) adapter or DC power supply
- The ISL91211AIK is required for VCCINT, VCCBRAM, VCC_DDR, and VCCAUX
- Optional ISL21010DFH312 is required for XADC, 1.25V ±0.2% accuracy
- The ISL80030 supports VCCO and VCC_IO, 3.3V/2.5V/1.8V

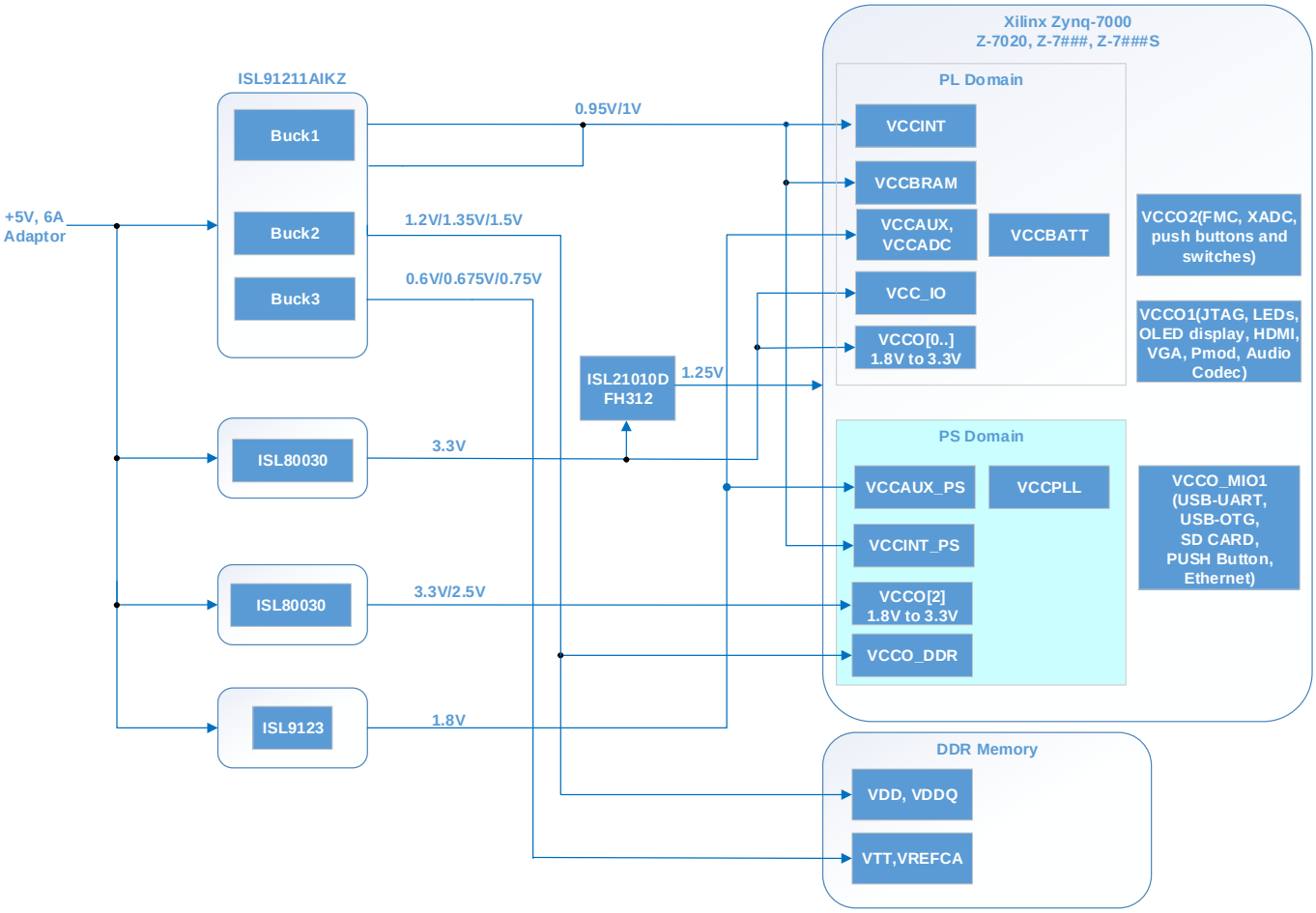


Figure 6. Zynq-7000 FPGA Block Diagram

Table 6. ISL91211AIKZ-TR5874 and ISL91211AIKZ-TR5873 DVS Output Option for Zynq-7000 Power Rail

Zynq-7000	ISL91211AIK (2+1+1)	ISL91211AIKZ-TR5874 (I^2C Slave Address = 0x60)			
	DVS_PIN1/DVS_PIN0	00	01	10	11
VCCINT VCCBRAM	VOUT1	1.0V	0.95V	0.95V	0.95V
VDDQ	VOUT2	1.2V	1.2V	1.35V	1.5V
VTT	VOUT3	0.6V	0.6V	0.675V	0.75V

Zynq-7000	ISL91211AIK (2+1+1)	ISL91211AIKZ-TR5873 (I_2C Slave Address = 0x60)	
	DVS_PIN1/DVS_PIN0	10	11
VCCINT VCCBRAM	VOUT1	1.0V	1.0V
VDDQ	VOUT2	1.35V	1.5V
VTT	VOUT3	0.675V	0.75V

1.3.5 PowerNavigator™ Software

The Renesas PowerNavigator software allows simple configuration and monitoring of multiple PMICs using a PC with a USB interface. PowerNavigator makes it easy to change all features and functions of your digital power supply design using a simple graphical user interface.

When the project file is complete, the Renesas USB to PMBus adapter dongle, ISLUSBEVAL1Z version V3.2, can be used to connect to the hardware. To connect to the PMBus interface of the controller, only I^2C_CLK, I^2C_SDA, and GND connections from the adapter to the board are required.

1.4 Recommended Products

1.4.1 ISL91211AIKZ and ISL91211BIKZ

The ISL91211AIK is a 4-phase, three output programmable Power Management IC (PMIC) and the ISL91211BIK is a 4-phase, four output programmable PMIC. They are optimized with highly efficient synchronous buck converters capable of multiphase and single-phase operations that can deliver up to 5A per phase continuous output current. Both devices feature four buck controllers and can reconfigure their power stages to these controllers. This flexibility allows seamless design-in for a wide range of applications in which high output power and small solution size are needed. The ISL91211AIK and ISL91211BIK integrate low ON-resistance MOSFETs and programmable PWM frequency, which allows the use of very small external inductors and capacitors. They feature automatic Diode emulation and Pulse Skipping modes under light-load conditions to improve efficiency and maximize battery life. The ISL91211AIK and ISL91211BIK deliver a highly robust power solution by featuring a controller based on the Renesas proprietary R5 technology, which provides tight output accuracy and load regulation, ultra-fast transient response, seamless DCM/CCM transitions, and requires no external compensation.

In addition to the standard interrupt, chip enable, and watchdog reset functions, the ISL91211AIK and ISL91211BIK also feature four MPIOs and three GPIOs that support SPI, I^2C communication protocol, and various other pin mode functions.

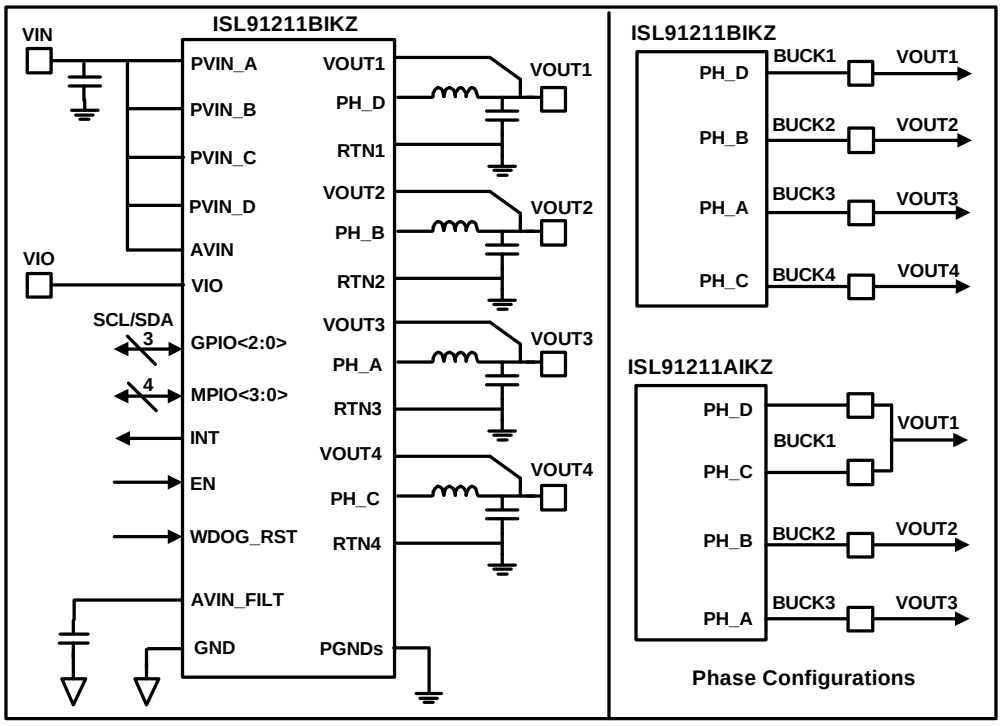


Figure 7. ISL91211BIKZ Simplified Application Circuit

The ISL91211AIK and ISL91211BIK have four independently programmable voltage settings for each buck controller that can set the output voltage. The four voltage settings are DVS0, DVS1, DVS2, and DVS3. By changing the DVS number selected, the corresponding output voltage is selected. Each output voltage is set by writing a 10-bit word to DVS Configuration 1 (BUCKx_DVS0CFG1 register) and DVS Configuration 0 (BUCKx_DVS0CFG0 register) in each buck. Configuration 1 holds the most significant eight bits and Configuration 0 holds the last two bits of the 10-bit word. The output voltage does not change until the LSB register is written.

When the master chip Enable pin (EN) is brought above 1.35[V], the ISL91211AIK and ISL91211BIK power up their key biasing circuits, load the OTP configuration registers, and start the power-up sequence.

1.4.1.1 Buck Start-Up from Master Chip Enable Pin (EN)

The Xilinx FPGA solution requires a different power-up sequence for each power rail to avoid the inrush current. The ISL91211AIK and ISL91211BIK supports programmable start-up and power-down delay times between the Master phases. The start-up and power-down sequence is initiated by EN pin with the internal BOOT time. The start-up and power-down delay times between the master phases are programmable from 0ms to 63ms. The soft-start rate from 1.25mV/µs to 50mV/µs are programmable. The controlled soft-start rate and buck regulator current limit limits the input inrush current to the output capacitor.

This is the example for the start-up sequence

- Run a prescribed start-up sequence for the buck outputs as soon as the internal BOOT signal is ready.
- An internal 1.4ms boot-up delay occurs from when EN is logic high to the time Buck1 starts powering up.
- Buck2, Buck3, and Buck4 then sequentially turn on with a 1ms delay in between. Each channel powers up at a slew rate of 3mV/µs.

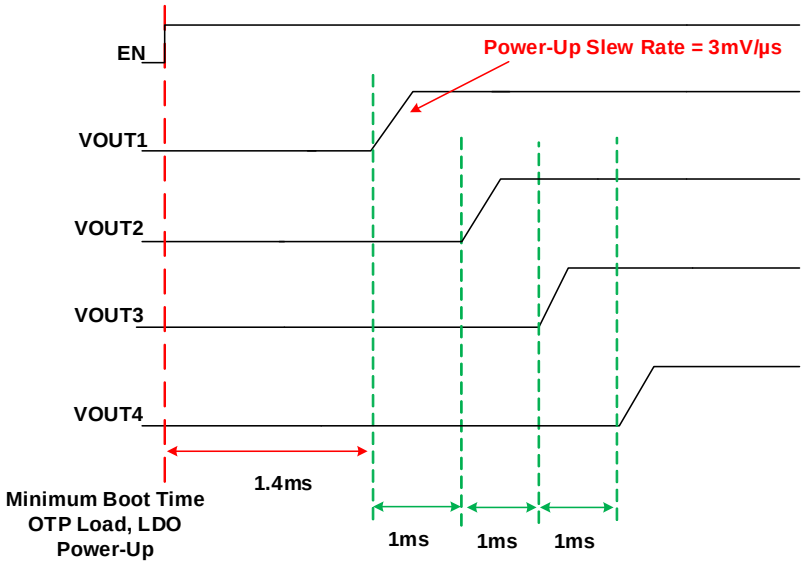


Figure 8. Chip Enable Power-Up Example

1.4.1.2 Buck Power-Down from Master Chip Enable Pin (EN)

When the master chip Enable pin (EN) is brought below the falling threshold of the comparator of 0.4V, all the bucks are ramped down at 3mV/µs at the same time. The bias circuits then power down, forcing the chip into shutdown. This slew rate is controlled until the output voltage is ~250mV, at which point the ISL91211AIK and ISL91211BIK engage a weak resistive pull-down that can discharge V_{OUT} to 0V.

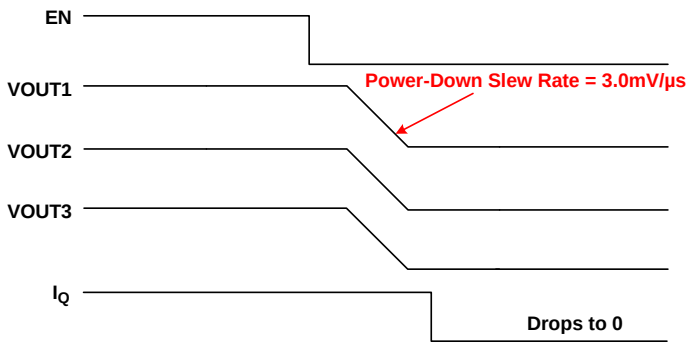


Figure 9. Chip Power-Down Example

1.4.2 ISL80030

The ISL80030 is a highly efficient, monolithic, synchronous step-down DC/DC converter that can deliver up to 3A of continuous output current from a 2.7V to 5.5V input supply. The ISL80030 uses peak current mode control architecture to allow very low duty cycle operation. These devices operate at a 1MHz switching frequency, thereby providing superior transient response and allowing for the use of small inductors. The ISL80030 also has excellent stability. The ISL80030 integrates very low $r_{DS(ON)}$ MOSFETs to maximize efficiency. In addition, because the high-side MOSFET is a PMOS, the need for a Boot capacitor is eliminated, thereby reducing external component count. The devices can operate at 100% duty cycle.

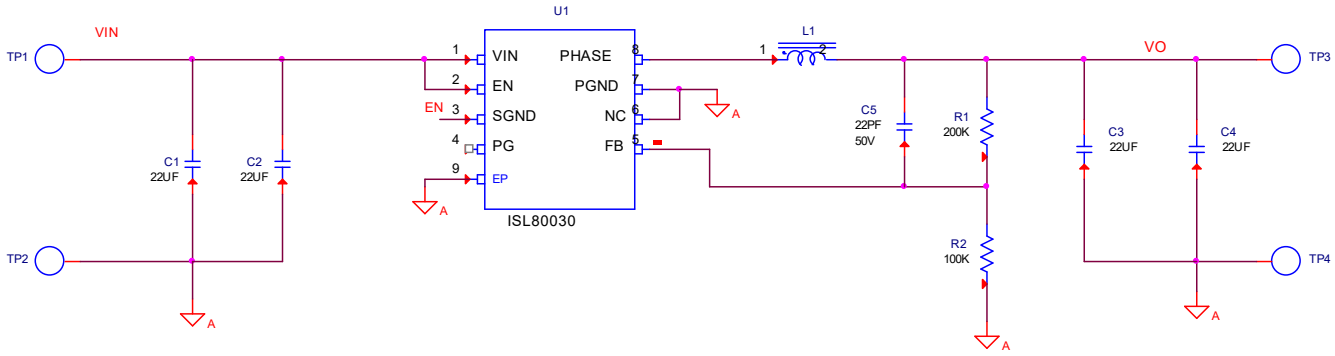


Figure 10. ISL80030 Simplified Application Circuit for VCCIO_1V8

The ISL80030 employs the current-mode Pulse-Width Modulation (PWM) control scheme for fast transient response and pulse-by-pulse current limiting. The current loop consists of the oscillator, PWM comparator, current sensing circuit, and the slope compensation for current loop stability. The slope compensation is 900mV/Ts, which changes with frequency. The gain for the current sensing circuit is typically 250mV/A. The control reference for the current loop comes from the Error Amplifier's (EAMP) output for fast transient. The reference voltage is 0.6V, which is used by feedback to adjust the output of the error amplifier. The error amplifier is a transconductance amplifier that converts the voltage error signal to a current output. The voltage loop is internally compensated with the 27pF and 200kΩ RC network. The maximum EAMP voltage output is precisely clamped to 1.6V.

1.4.3 ISL9123

The ISL9123 is a highly integrated buck switching regulator that is capable of supplying output voltage down to 0.4V. It features an extremely low quiescent current consumption of 940nA in Regulation mode, 170nA in Forced Bypass mode, and 9nA in Shutdown mode. It provides 80% efficiency at 10µA load and has a peak efficiency of 97%. It supports input voltages from 1.8V to 5.5V. The ISL9123 has automatic bypass functionality for situations in which the input voltage is close to the output voltage. In addition to the automatic bypass functionality, the Forced Bypass power saving mode can be chosen if voltage regulation is not required. Forced Bypass power saving mode is accessible using the I^2C interface bus. The ISL9123 is capable of delivering up to 600mA of output current (V_{IN} = 3.6V, V_{OUT} = 1.8V) and provides excellent efficiency due to its adaptive frequency hysteretic control architecture. The ISL9123 is designed for stand-alone applications and supports a default output voltage at Power-On Reset (POR). After POR, the output voltage can be adjusted in the range of 0.4V to 5.375V by using the I^2C interface bus. Specific default output voltages are available upon request.

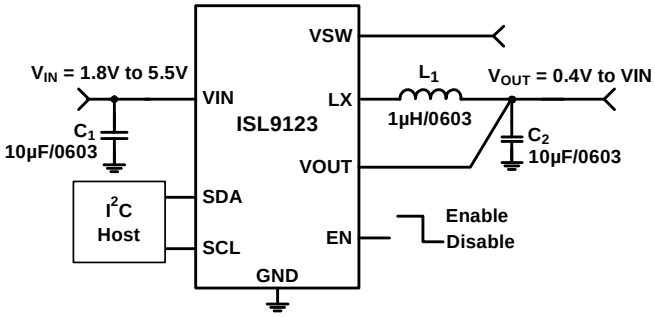


Figure 11. ISL9123 Simplified Application Circuit

1.4.4 ISL21010DFH312

The ISL21010 is a precision, low dropout micro-power bandgap voltage reference in a space-saving SOT-23 package. It operates from a single 2.2V to 5.5V supply (minimum voltage is dependent on voltage option) and provides a ±0.2% accurate reference. The ISL21010 provides up to 25mA output current sourcing with low 150mV dropout voltage. Output voltage options include 1.024V, 1.25V, 1.5V, 2.048V, 2.5V, 3.0V, 3.3V, and 4.096V. The low supply current and low dropout voltage combined with high accuracy make the ISL21010 ideal for precision XADC input reference on the Xilinx 7 series FPGA's. The XADC includes a 12-bit, 1M sample per second (MSPS) ADC and on-chip sensors.

2. Test Results

2.1 Testing and Results

2.1.1 VCCINT/VCCBRAM Power Rail Test – ISL91211AIK

Test condition: PVIN = 5.0V, VCCINT/VCCBRAM = 0.95V, L = 220nH, f_{SW} = 2MHz, 2PH Configuration

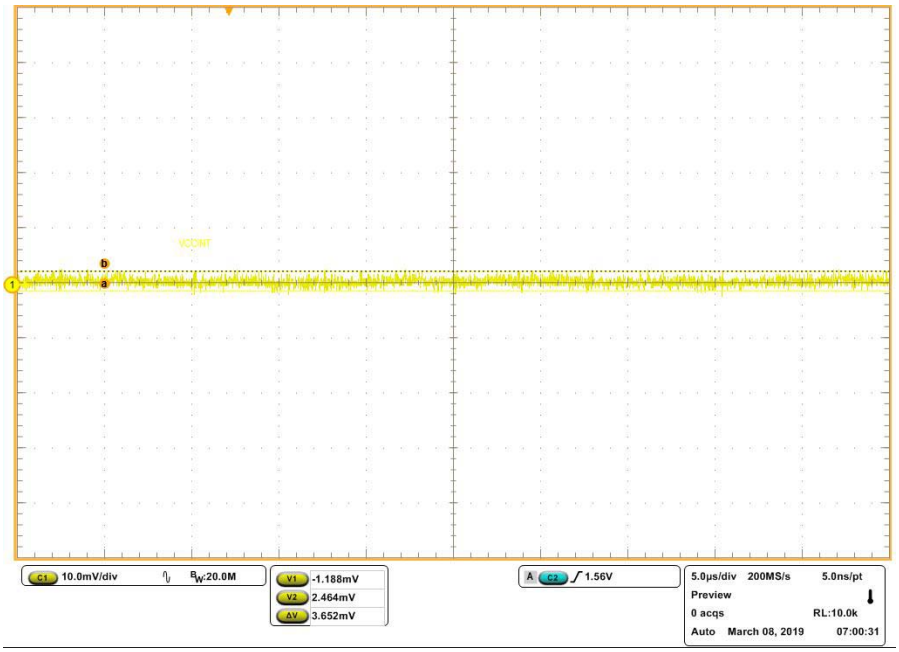


Figure 12. VCCINT Output Ripple at No Load, <5mV$_{P-P}$

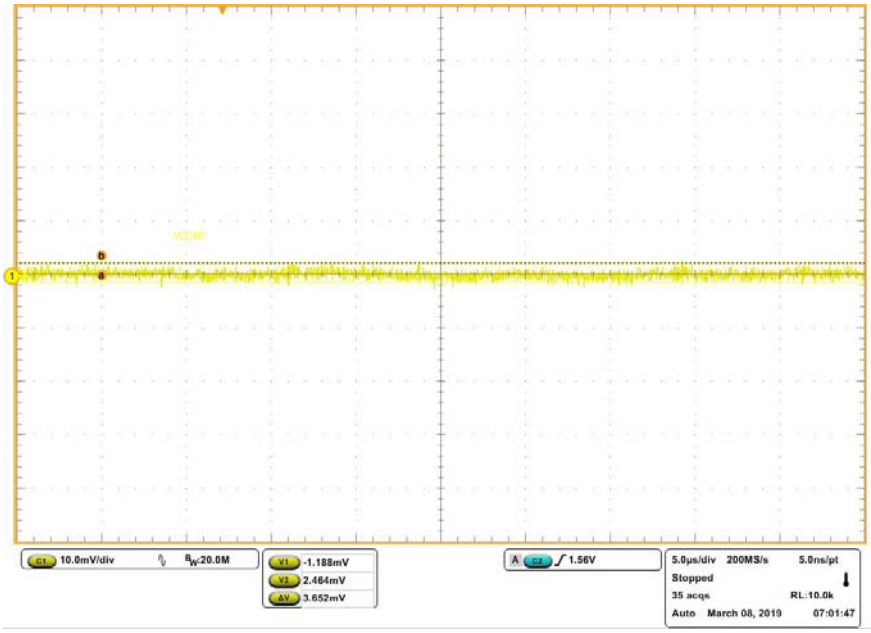


Figure 13. VCCINT Output Ripple at 6A Load, <5mV$_{P-P}$

Test condition: PVIN = 5.0V, VCCINT/VCCBRAM = 0.95V, L = 220nH, f_{SW} = 2MHz, 2PH Configuration **(Continued)**

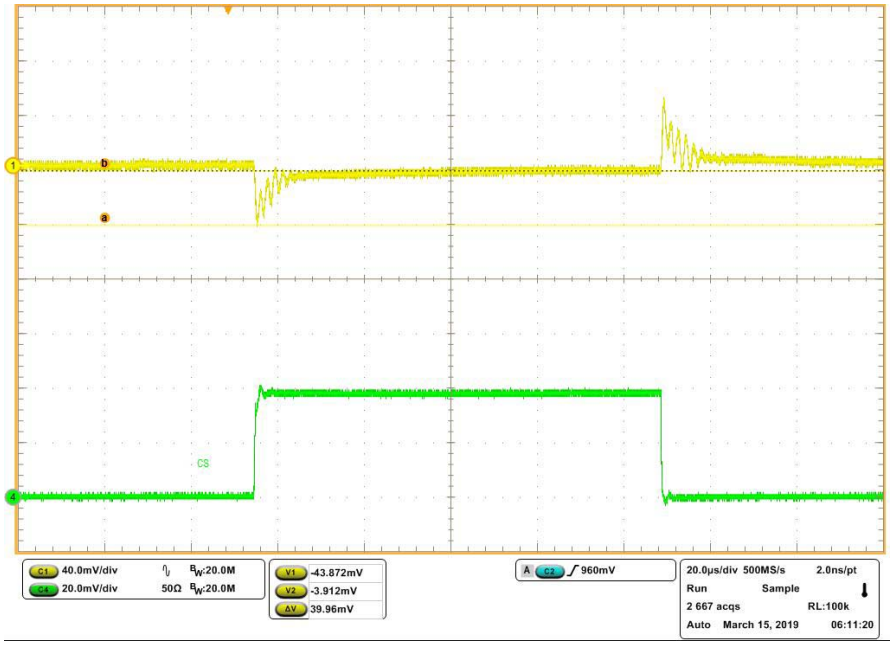


Figure 14. VCCINT Load Transient, 100mA to 4A, Undershoot: 39.96mV

2.1.2 VMGTAVCC Power Rail Test – ISL91211AIK

Test condition: PVIN = 5.0V, VMGTAVCC = 1.0V, L = 470nH, f_{SW} = 2MHz, 1PH Configuration

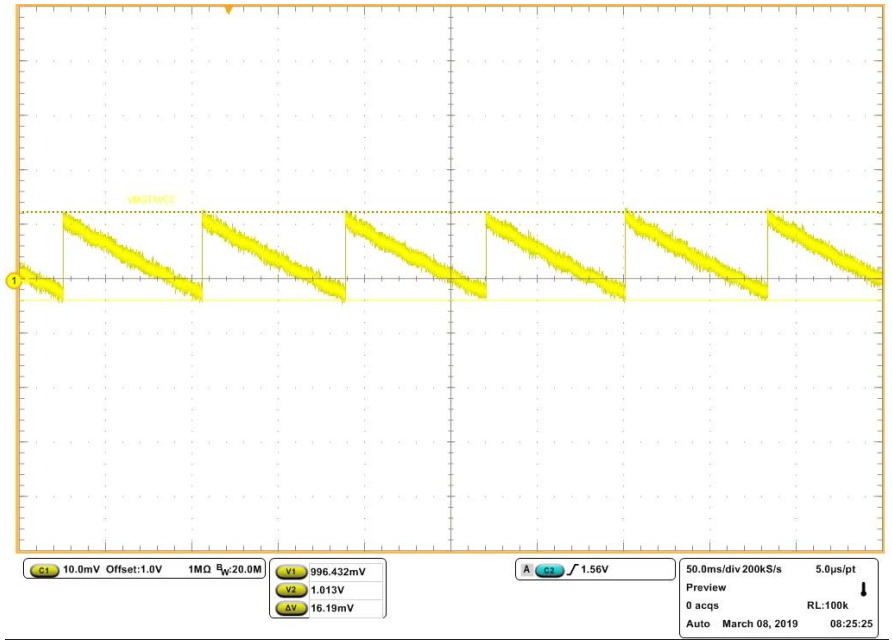


Figure 15. VMGTAVCC Output Ripple at No load, <16.19mV$_{P-P}$

Test condition: PVIN = 5.0V, VMGTAVCC = 1.0V, L = 470nH, f_{SW} = 2MHz, 1PH Configuration **(Continued)**

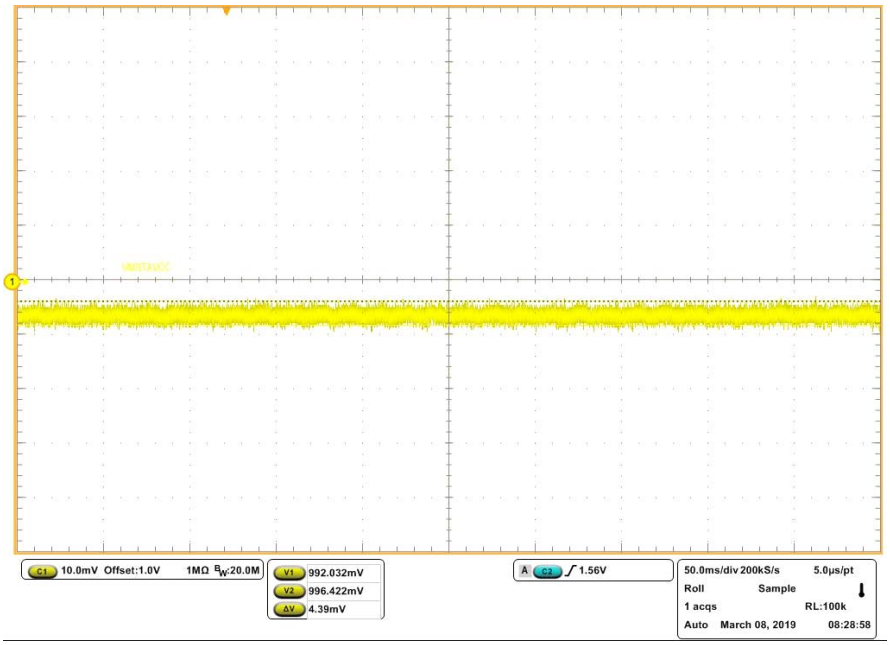


Figure 16. VMGTAVCC Output Ripple at 1A, <5mV$_{P-P}$

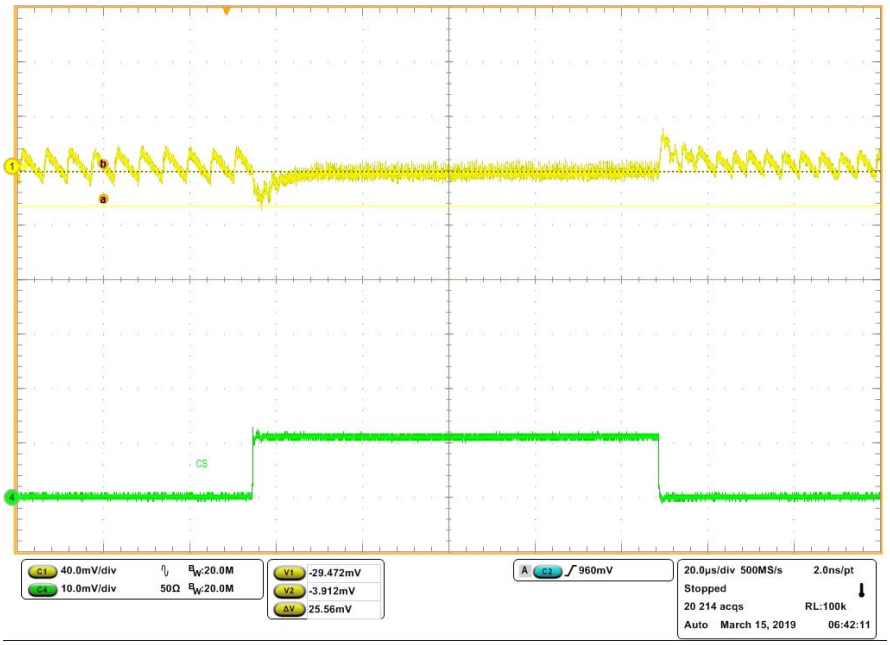


Figure 17. VMGTAVCC Load Transient, 100mA to 1A, Undershoot: 25.56mV

2.1.3 VMGTAVTT Power Rail Test - ISL91211AIK

Test condition: PVIN = 5.0V, VMGTAVTT = 1.2V, L = 470nH, f_{SW} = 2MHz, 1PH Configuration

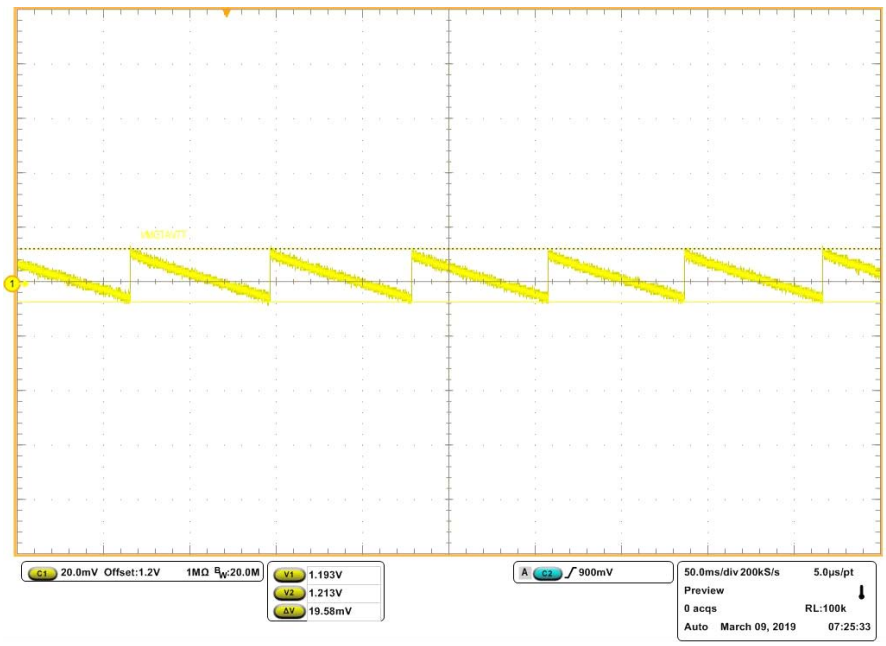


Figure 18. VMGTAVTT Output Ripple at No Load, <19.58mV$_{P-P}$

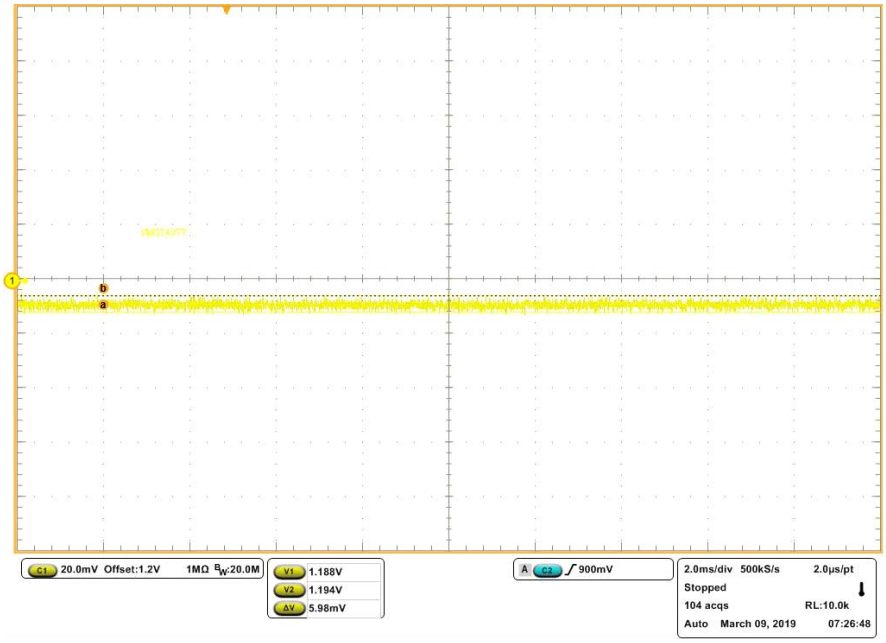


Figure 19. VMGTAVTT Output Ripple at 1A Load, <6mV$_{P-P}$

Test condition: PVIN = 5.0V, VMGTAVTT = 1.2V, L = 470nH, f_{SW} = 2MHz, 1PH Configuration **(Continued)**

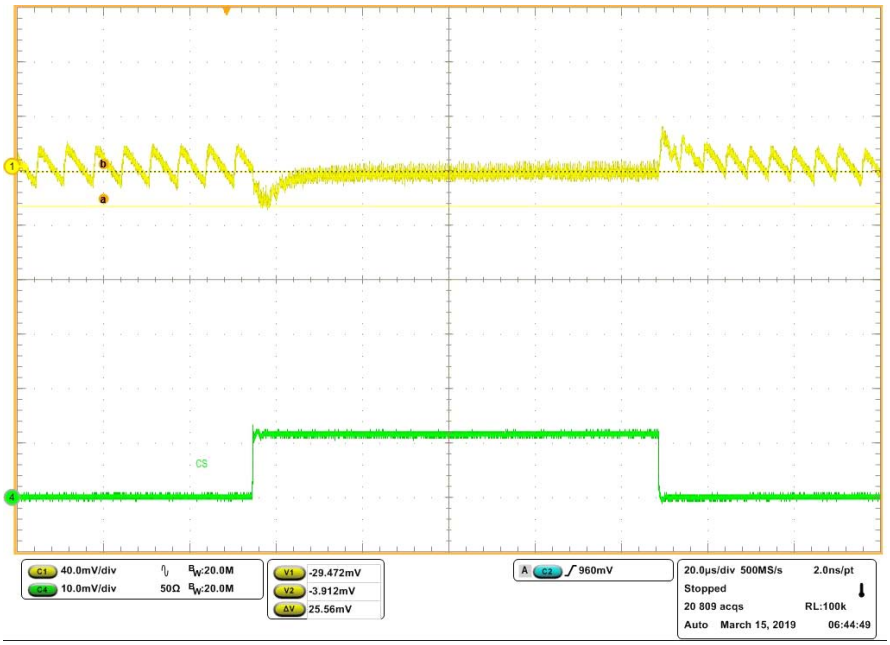


Figure 20. VMGTAVTT Load Transient, 100mA to 1A, Undershoot: 25.56mV

2.1.4 VCCDDR Power Rail Test - ISL91211BIK

Test condition: PVIN = 5.0V, VCCDDR = 1.35V, L = 220nH, f_{SW} = 2MHz, 1PH

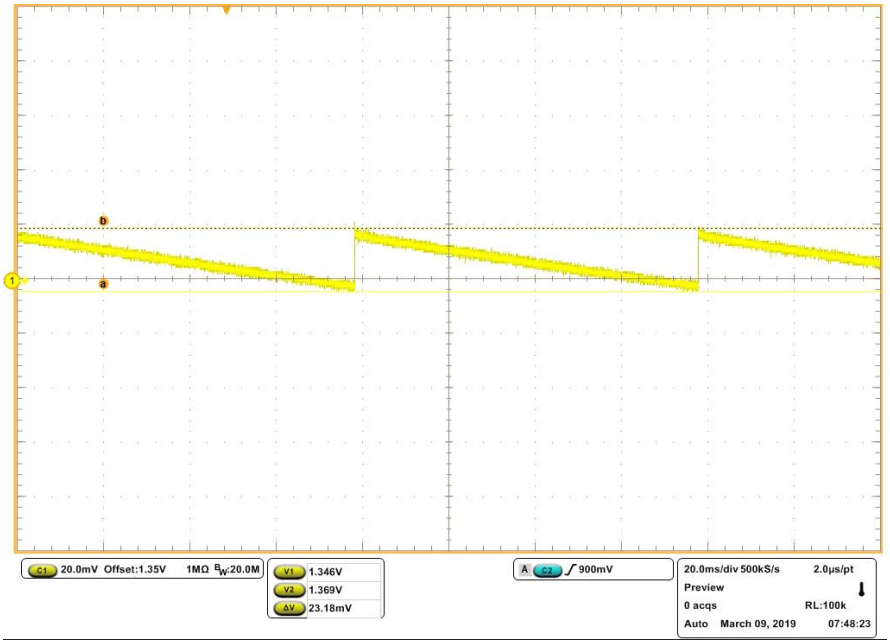


Figure 21. VCCDDR Output Ripple at No Load, <23.18mV$_{P-P}$

Test condition: PVIN = 5.0V, VCCDDR = 1.35V, L = 220nH, f_{SW} = 2MHz, 1PH **(Continued)**

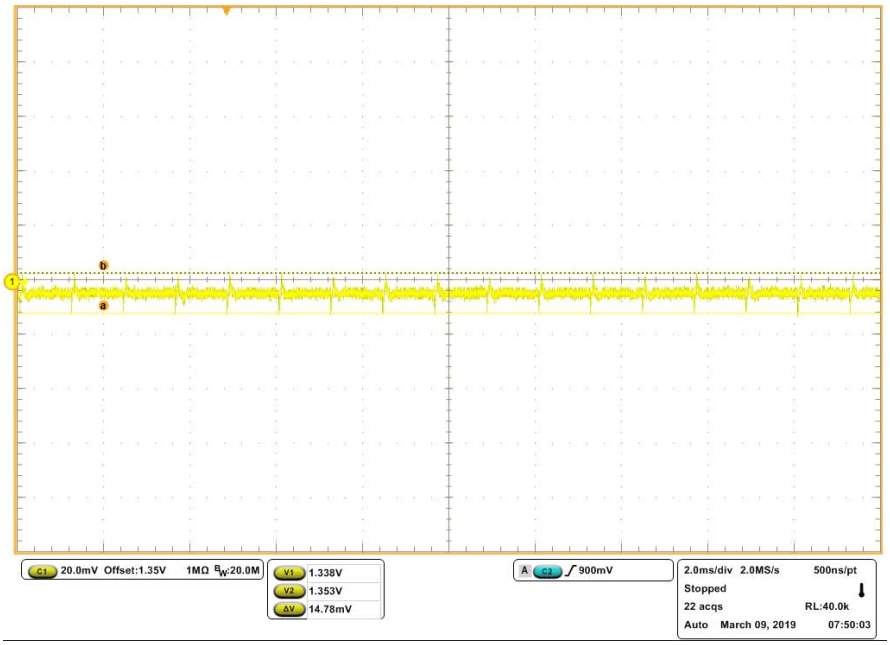


Figure 22. VCCDDR Output Ripple at 2A Load, <14.78mV$_{P-P}$

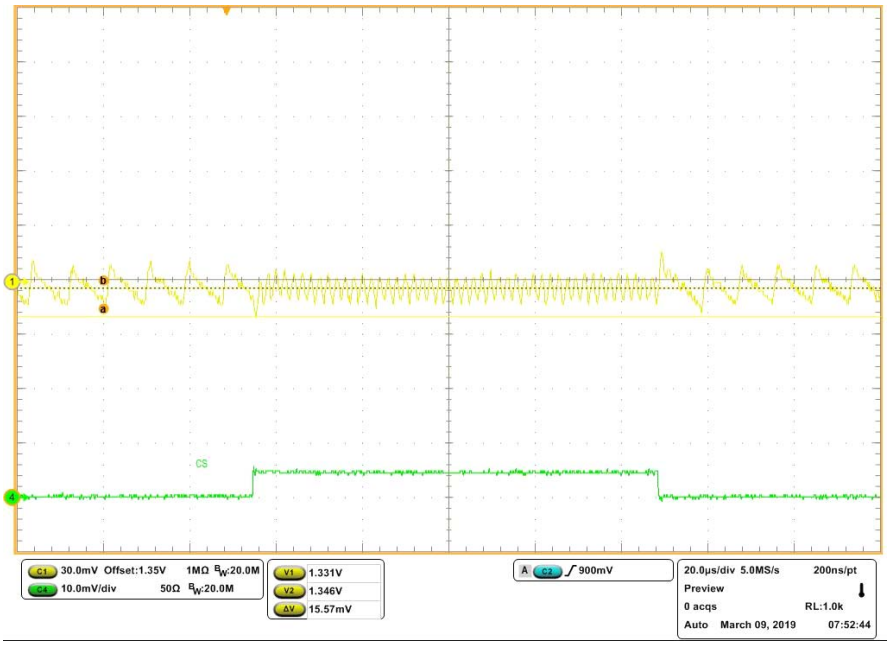


Figure 23. VCCDDR Load Transient, 100mA to 500mA, Undershoot: 15.57mV

2.1.5 VTT/VREFCA (VDDQ/2) Power Rail Test - ISL91211BIK

Test condition: PVIN = 5.0V, VTT = 0.75V, L = 470nH, f_{SW} = 2MHz, FPWM mode, 1PH

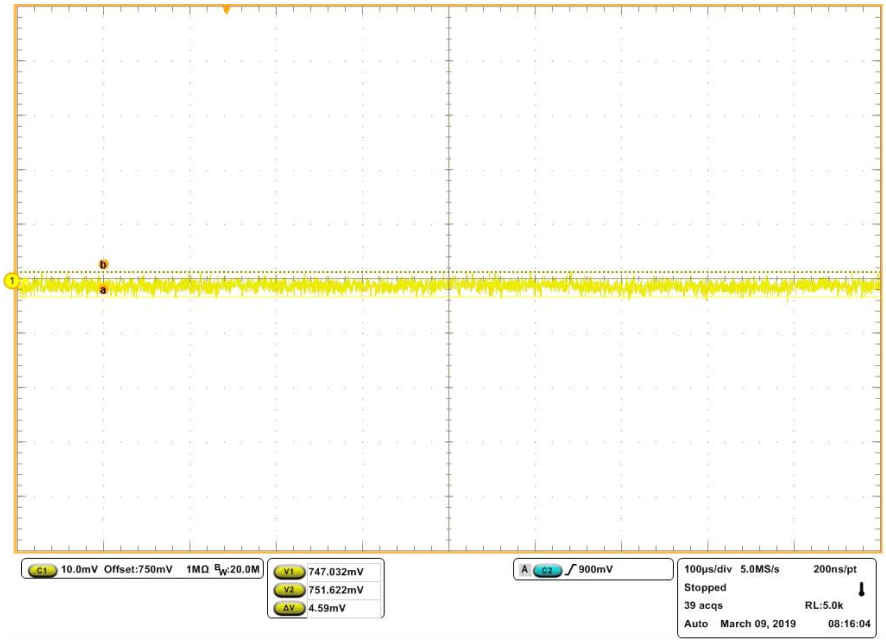


Figure 24. VTT Output Ripple at No Load, <5mV$_{P-P}$

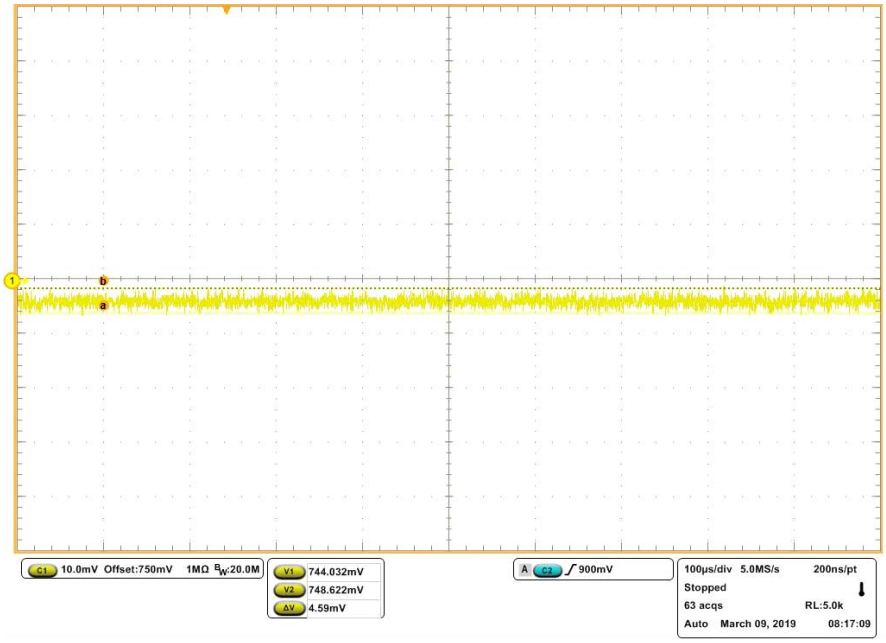


Figure 25. VTT Output Ripple at 2A, <5mV$_{P-P}$

Test condition: PVIN = 5.0V, VTT = 0.75V, L = 470nH, f_{SW} = 2MHz, FPWM mode, 1PH **(Continued)**

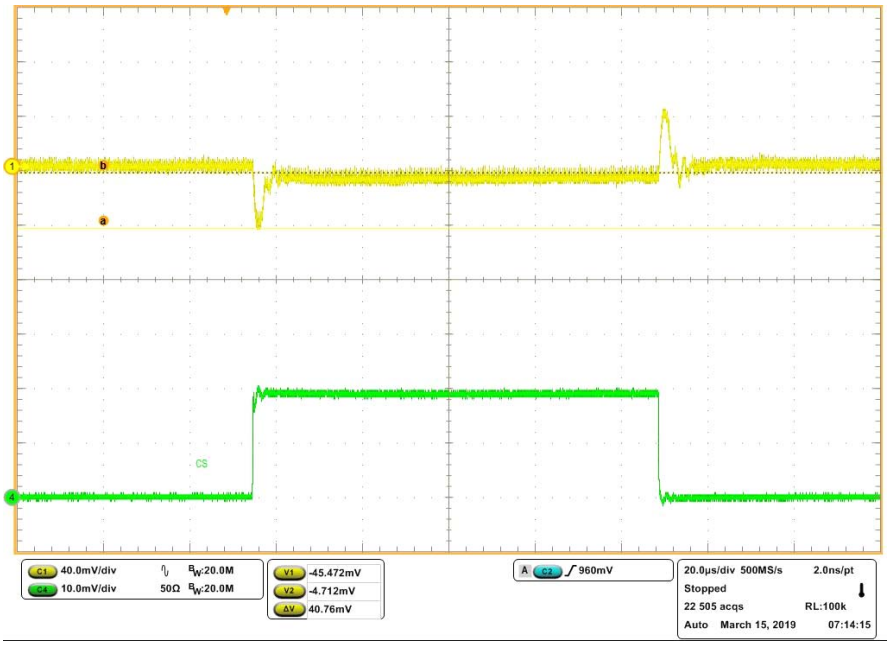


Figure 26. VTT Load Transient, FCCM Mode, 100mA to 2A, Undershoot: 40.76mV

2.1.6 VCCAUX/VCCADC Power Rail - ISL91211BIK

Test condition: PVIN = 5.0V, VCCAUX = 1.8V, L = 470nH, f_{SW} = 2MHz, 1PH

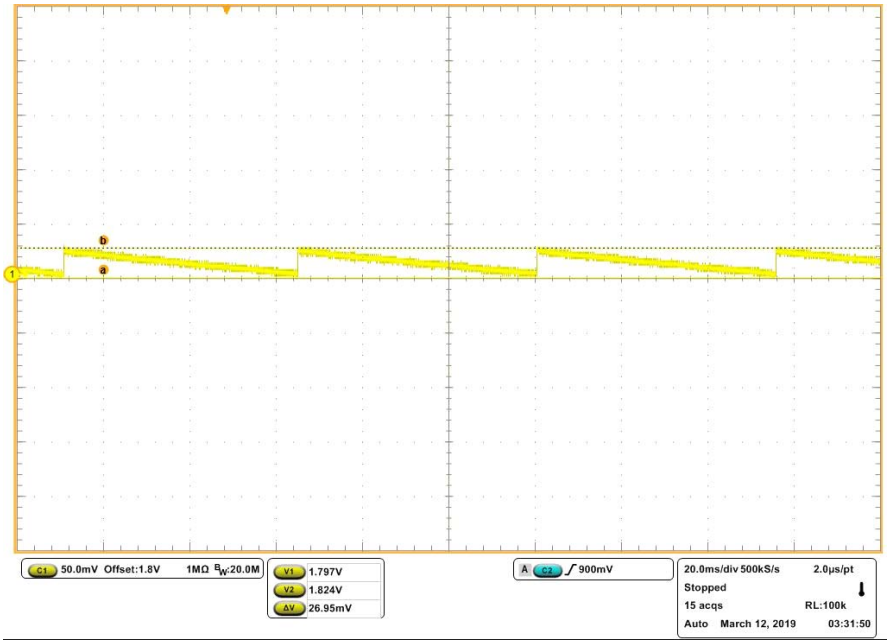


Figure 27. VCCAUX Output Ripple at No Load, <26.95mV$_{P-P}$

Test condition: PVIN = 5.0V, VCCAUX = 1.8V, L = 470nH, f_{SW} = 2MHz, 1PH **(Continued)**

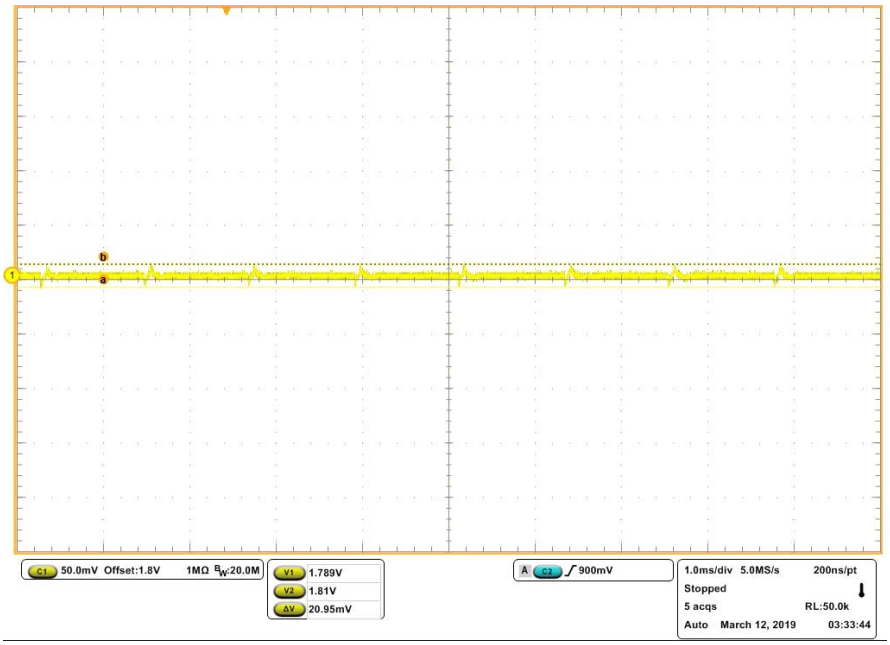


Figure 28. VCCAUX Output Ripple at 1A load, <21mV$_{P-P}$

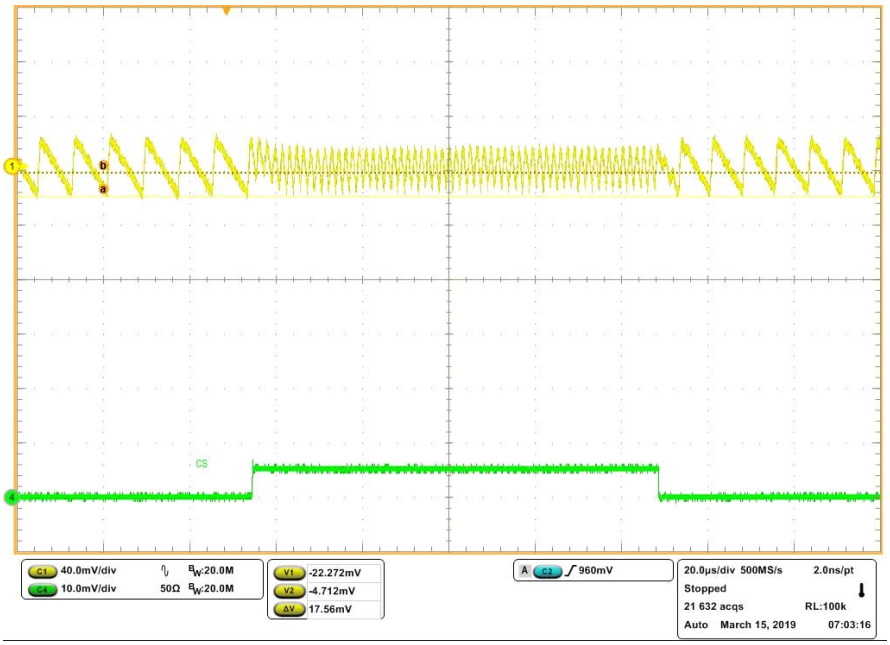


Figure 29. VCCAUX Load Transient, 100mA to 500mA, Undershoot: 17.56mV

2.1.7 VCCO Power Rail Test

2.1.7.1 VCCO 2.5V Power Rail - ISL80030

Test condition: PVIN = 5.0V, VCCO 2.5V = 2.5V, L = 2.2µH, f_{SW} = 1MHz, 1PH

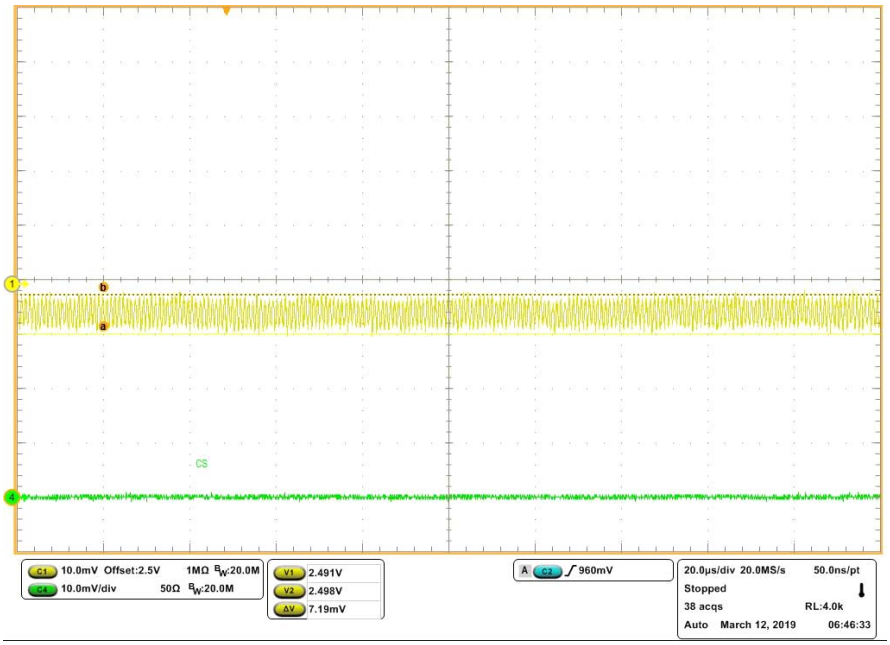


Figure 30. VCCO 2.5V Output Ripple at No Load, <7.19mV$_{P-P}$

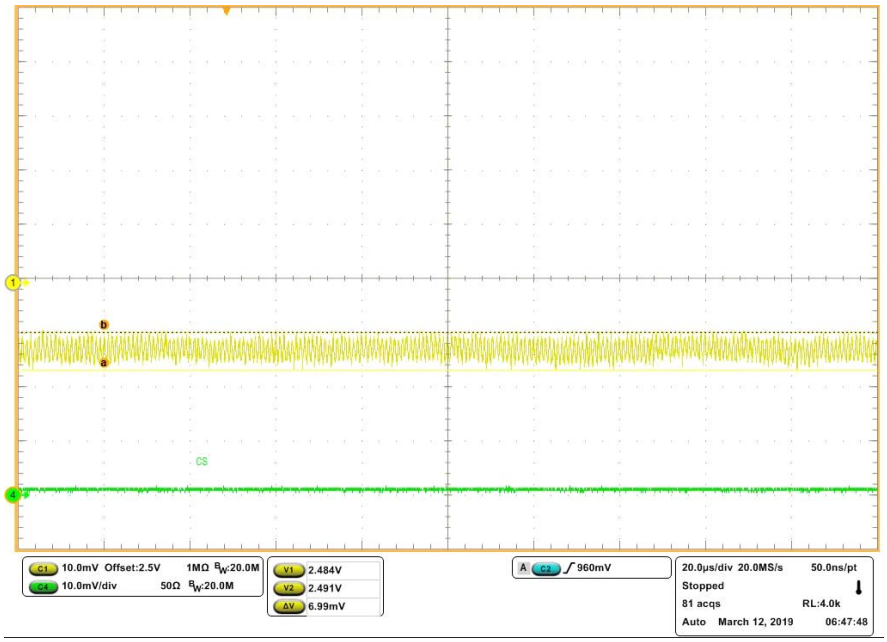


Figure 31. Output Ripple at No Load, <7.0mV$_{P-P}$

Test condition: PVIN = 5.0V, VCCO 2.5V = 2.5V, L = 2.2µH, f_{SW} = 1MHz, 1PH **(Continued)**

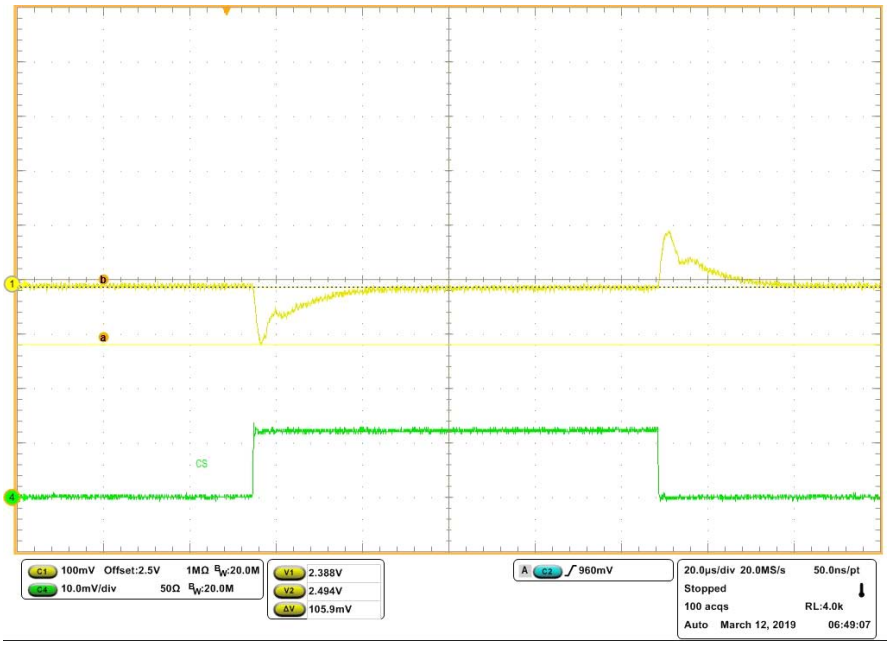


Figure 32. VCCO 2.5V Load Transient, 100mA to 1.5A, Undershoot: 105.9mV

2.1.7.2 VCCO 3.3V Power Rail - ISL80030

Test condition: PVIN = 5.0V, VCCO 3.3V = 3.3V, L = 2.2µH, f_{SW} = 1MHz, 1PH

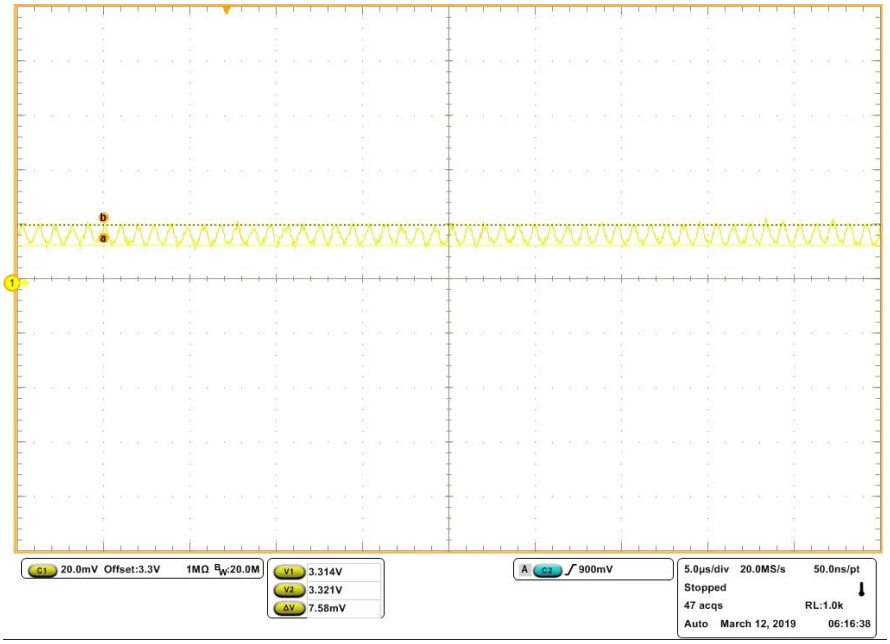


Figure 33. VCCO 3.3V Output Ripple at No Load, <7.58mV$_{P-P}$

Test condition: PVIN = 5.0V, VCCO 3.3V = 3.3V, L = 2.2µH, f_{SW} = 1MHz, 1PH **(Continued)**

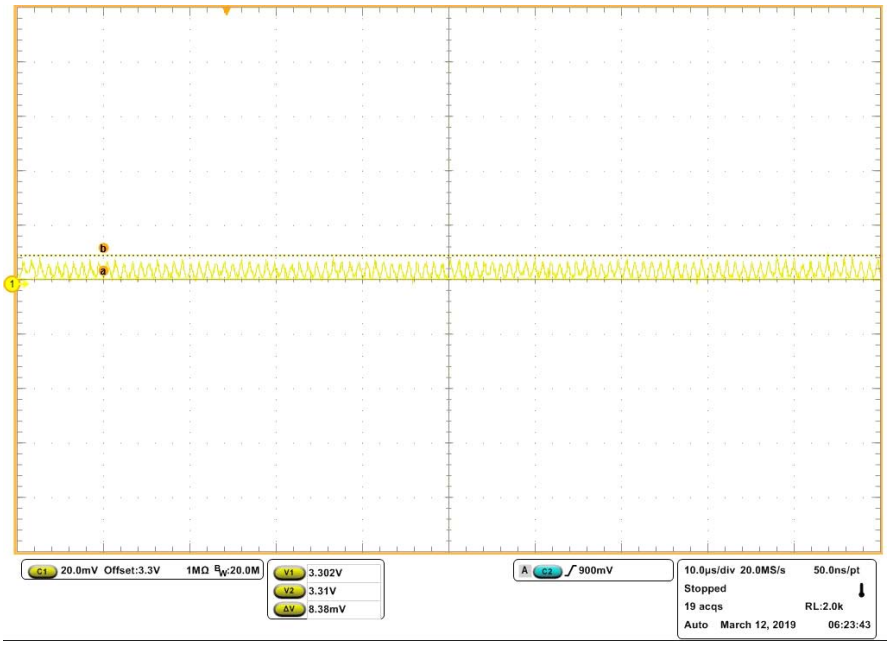


Figure 34. VCCO 3.3V Output Ripple at 3A, <8.3mV$_{P-P}$

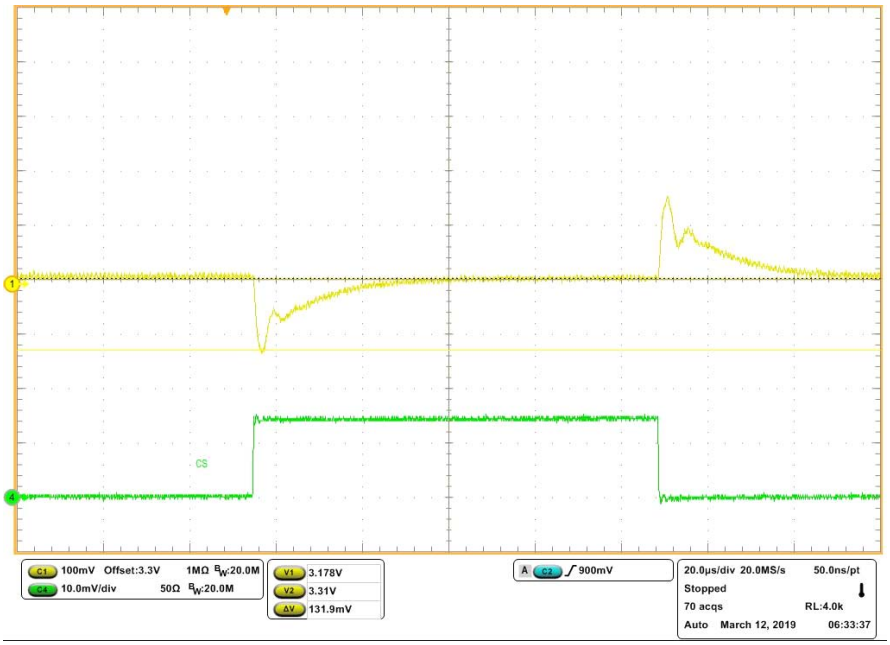


Figure 35. VCCO 3.3V Load Transient, 100mA to 1.5A, Undershoot: 131.9mV

2.1.8 XADC Power Rail Test - ISL21010DFH312

Test condition: V_{IN} = 3.3V, XADC = 1.25V

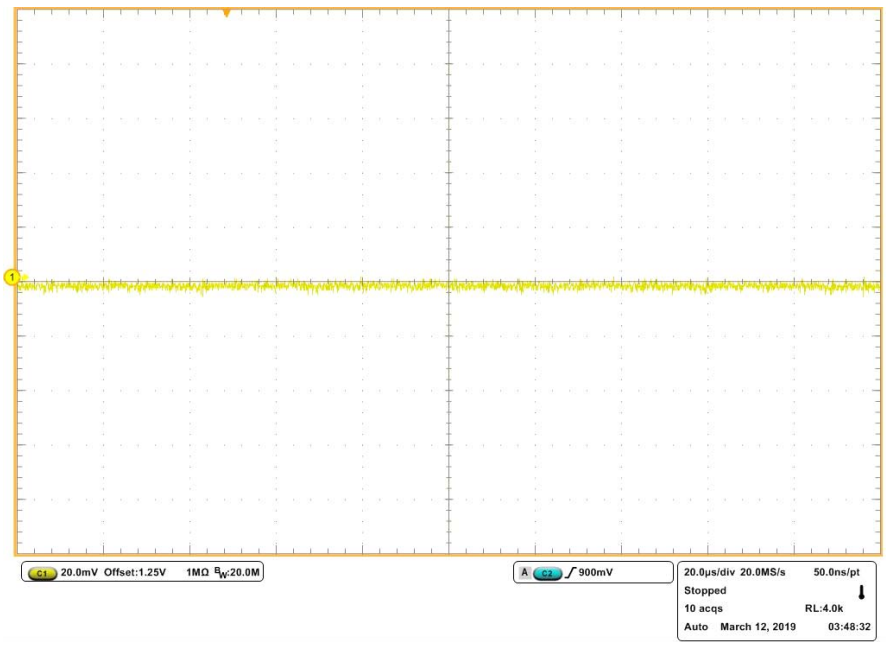


Figure 36. XADC Output Voltage Ripple, <2.5mV$_{P-P}$

3. Layout Guidelines

3.1 Reference Boards

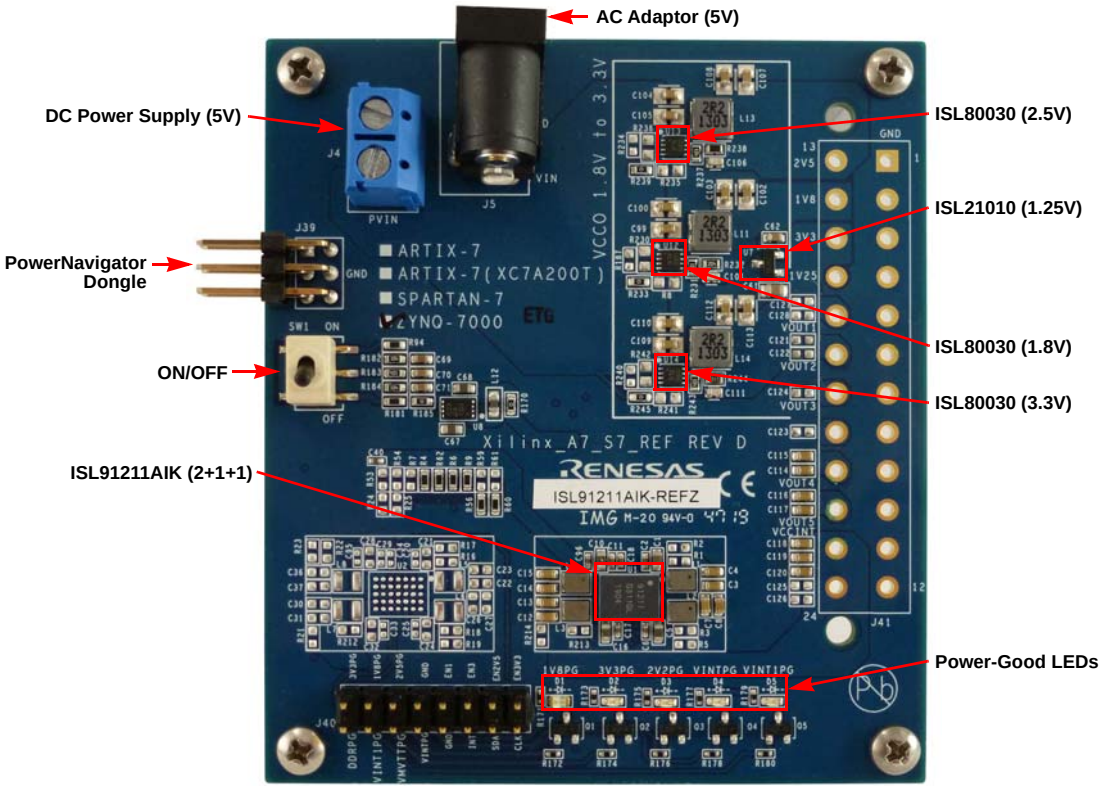


Figure 37. ISL91211AIK-REFZ Top

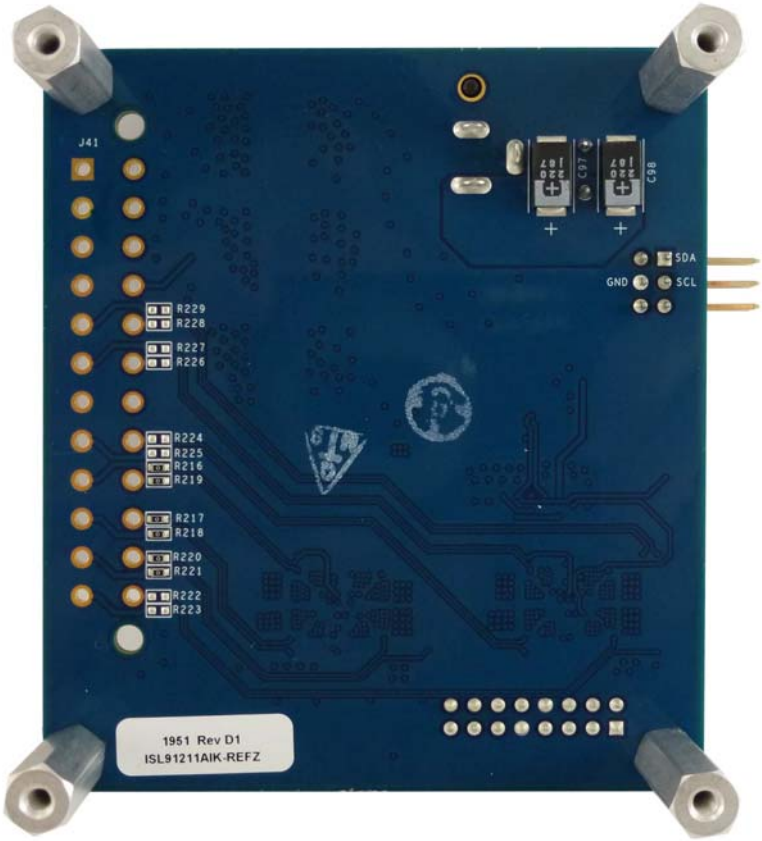


Figure 38. ISL91211AIK-REFZ Bottom

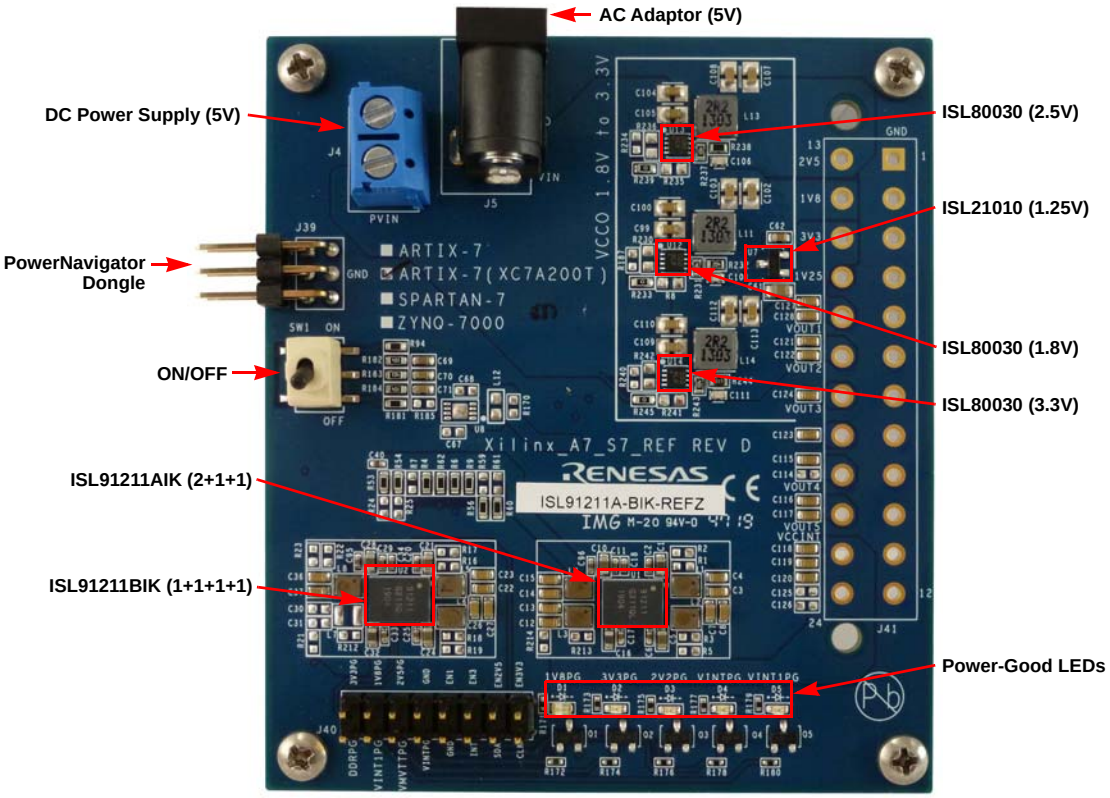


Figure 39. ISL91211A-BIK-REFZ Top

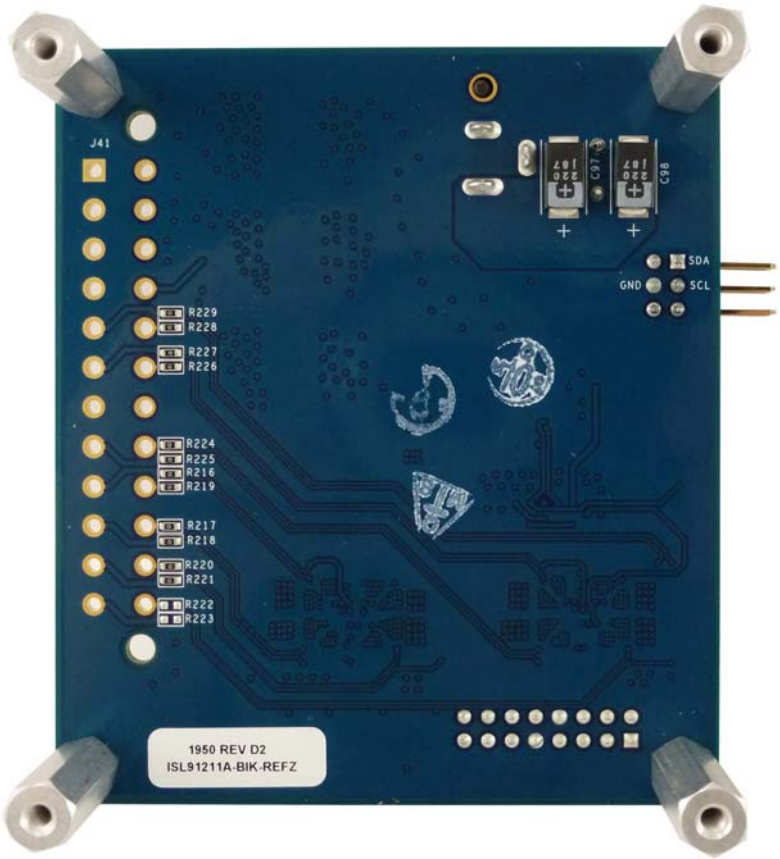


Figure 40. ISL91211A-BIK-REFZ Bottom

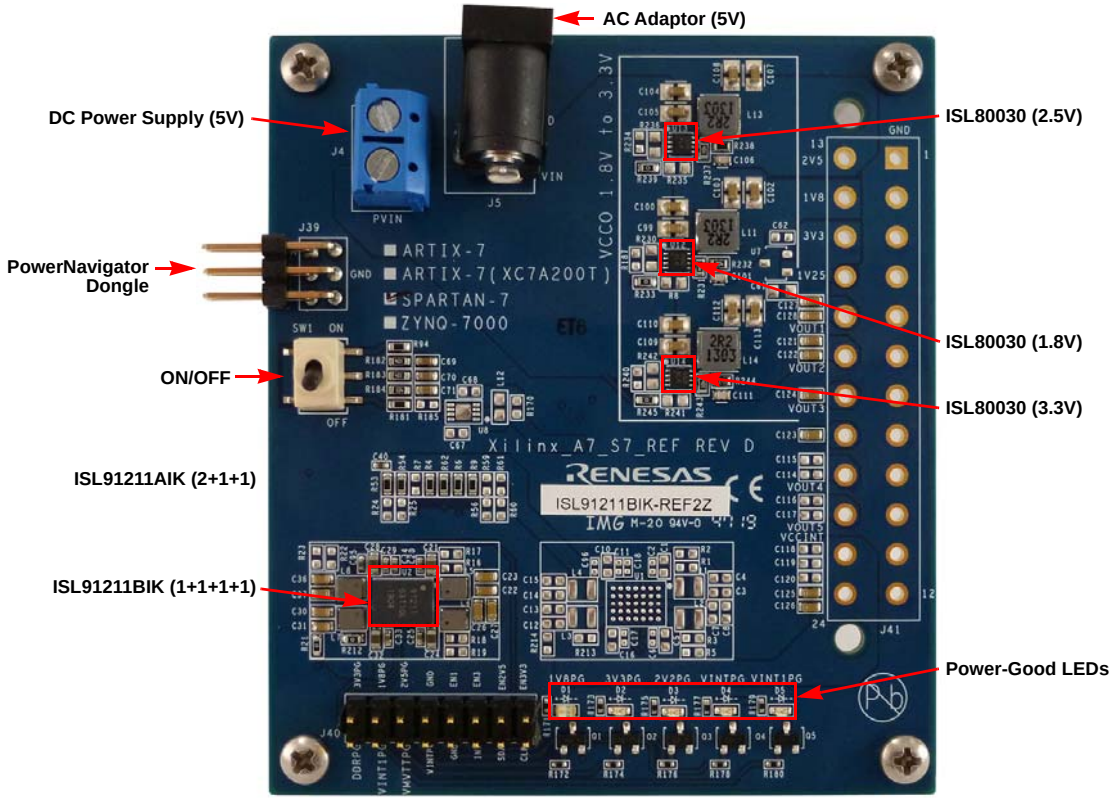


Figure 41. ISL91211BIK-REF2Z Top

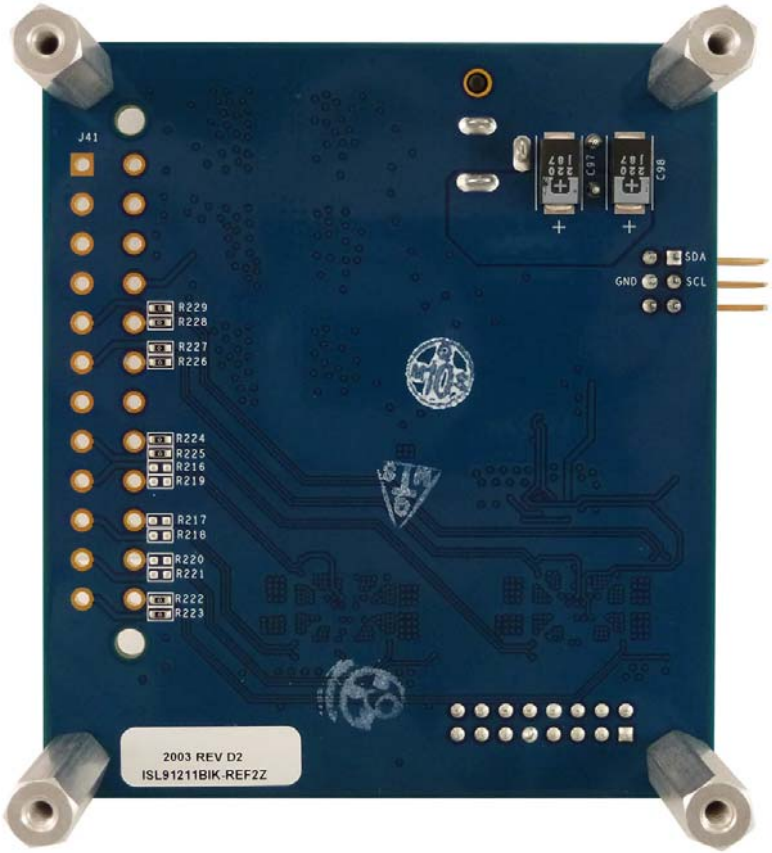


Figure 42. ISL91211BIK-REF2Z Bottom

3.2 Reference Board Schematics

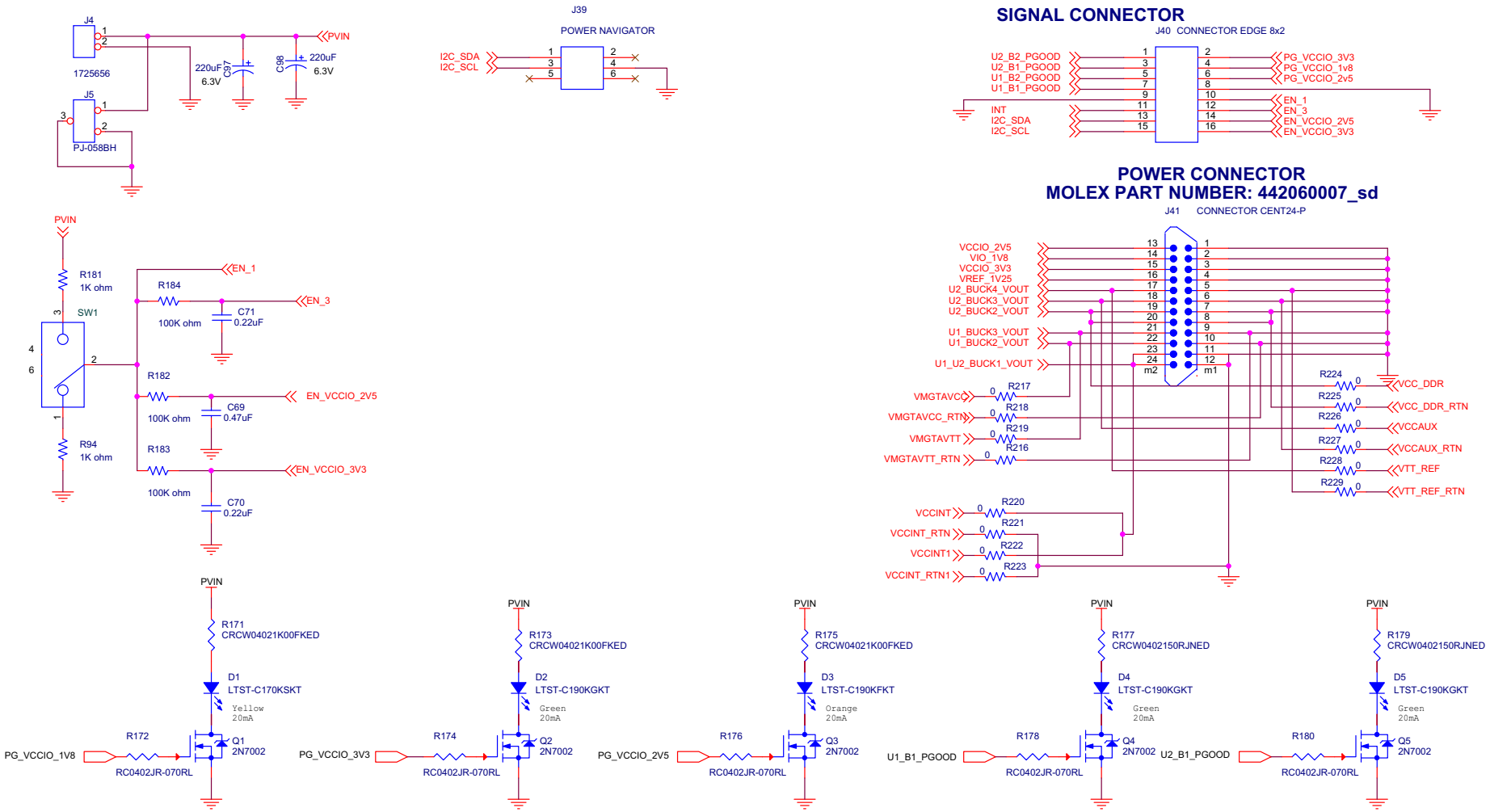
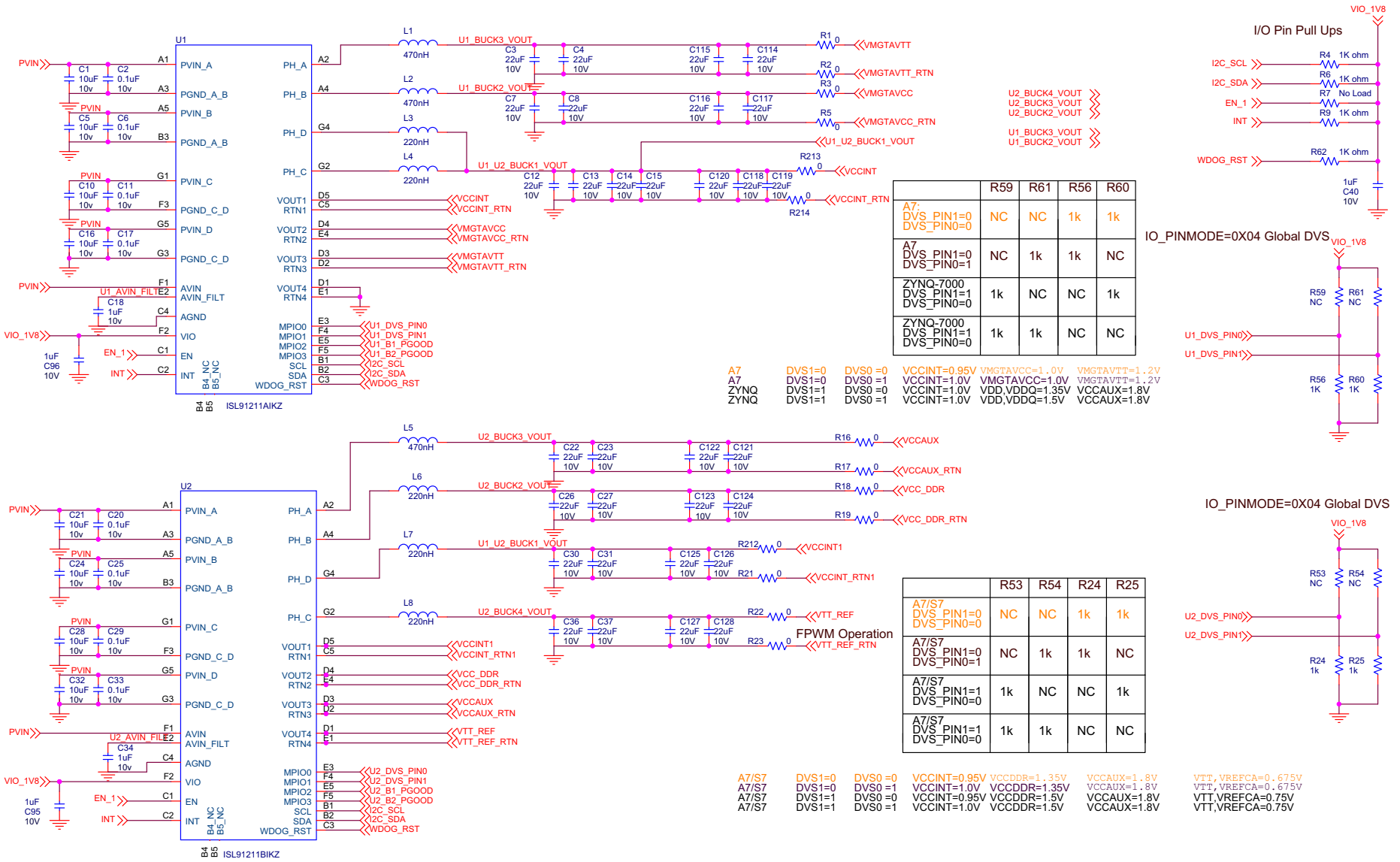


Figure 43. XILINX_A7_S7 Connectors and Power-Good LED Indicators



	R59	R61	R56	R60
A7: DVS_PIN1=0 DVS_PIN0=0	NC	NC	1k	1k
A7 DVS_PIN1=0 DVS_PIN0=1	NC	1k	1k	NC
ZYNQ-7000 DVS_PIN1=1 DVS_PIN0=0	1k	NC	NC	1k
ZYNQ-7000 DVS_PIN1=1 DVS_PIN0=0	1k	1k	NC	NC

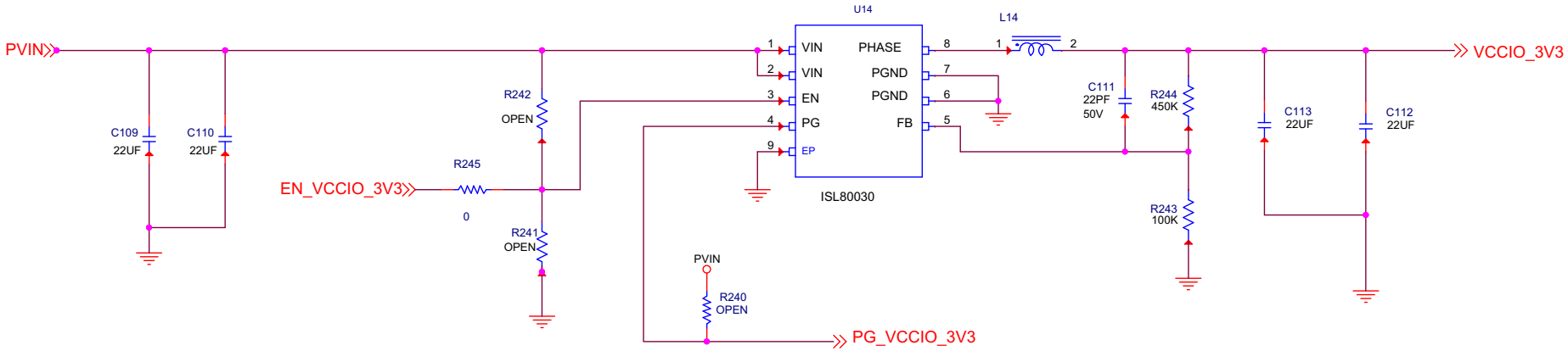
A7	DVS1=0	DVS0 =0	VCCINT=0.95V	VMGTAVCC=1.0V	VMGTAVTT=1.2V
A7	DVS1=0	DVS0 =1	VCCINT=1.0V	VMGTAVCC=1.0V	VMGTAVTT=1.2V
ZYNQ	DVS1=1	DVS0 =0	VCCINT=1.0V	VDD,VDDQ=1.35V	VCCAUX=1.8V
ZYNQ	DVS1=1	DVS0 =1	VCCINT=1.0V	VDD,VDDQ=1.5V	VCCAUX=1.8V

	R53	R54	R24	R25
A7/S7 DVS_PIN1=0 DVS_PIN0=0	NC	NC	1k	1k
A7/S7 DVS_PIN1=0 DVS_PIN0=1	NC	1k	1k	NC
A7/S7 DVS_PIN1=1 DVS_PIN0=0	1k	NC	NC	1k
A7/S7 DVS_PIN1=1 DVS_PIN0=0	1k	1k	NC	NC

A7/S7	DVS1=0	DVS0 =0	VCCINT=0.95V	VCCDDR=1.35V	VCCAUX=1.8V	VTT,VREFCA=0.675V
A7/S7	DVS1=0	DVS0 =1	VCCINT=1.0V	VCCDDR=1.35V	VCCAUX=1.8V	VTT,VREFCA=0.675V
A7/S7	DVS1=1	DVS0 =0	VCCINT=0.95V	VCCDDR=1.5V	VCCAUX=1.8V	VTT,VREFCA=0.75V
A7/S7	DVS1=1	DVS0 =1	VCCINT=1.0V	VCCDDR=1.5V	VCCAUX=1.8V	VTT,VREFCA=0.75V

Figure 44. ISL91211AIKZ, ISL91211BIKZ

ISL85003 SINGLE OUTPUT FOR VCCIO 3.3V



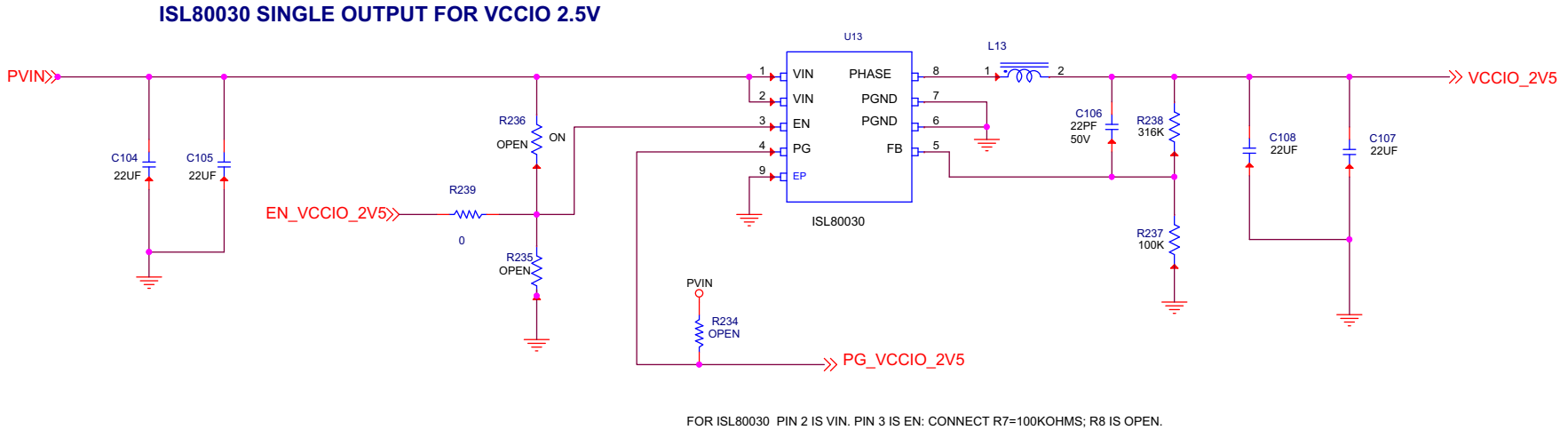
FOR ISL80030 PIN 2 IS VIN. PIN 3 IS EN: CONNECT R7=100KOHMS; R8 IS OPEN.

L=2.2uH	R=200K	Vout=1.8V
L=2.2uH	R=316K	Vout=2.5V
L=2.2uH	R=450K	Vout=3.3V

2.2uH: 74437324022 Wurth : 4x4x2 mm

3.3uH: 74437324033 Wurth : 4X4X2 mm

Figure 45. ISL80030 Single Output for VCCIO 3.3V



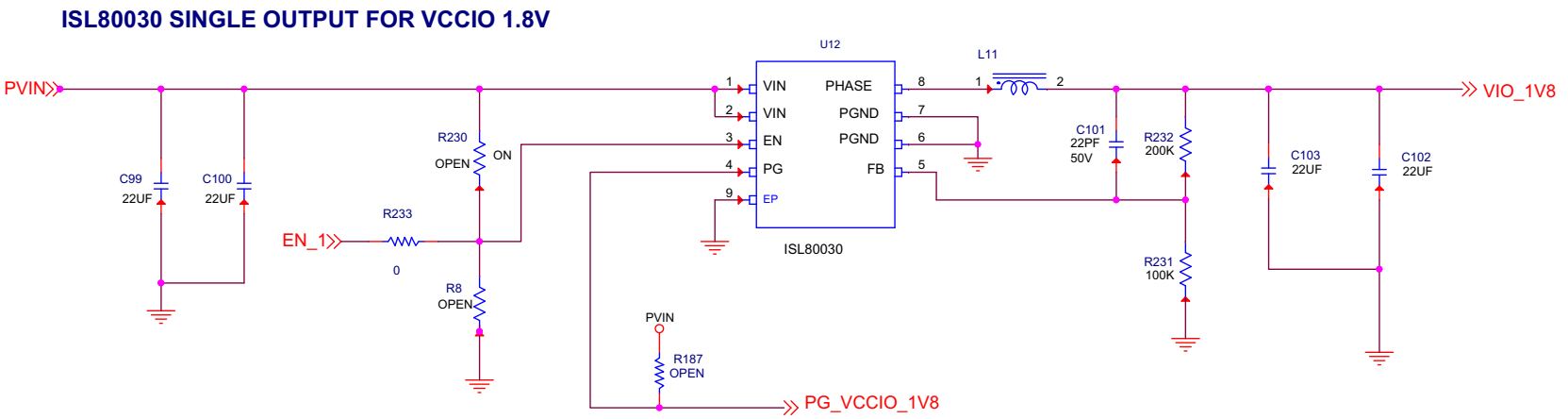
FOR ISL80030 PIN 2 IS VIN. PIN 3 IS EN: CONNECT R7=100KOHMS; R8 IS OPEN.

L=2.2uH	R=200K	Vout=1.8V
L=2.2uH	R=316K	Vout=2.5V
L=2.2uH	R=450K	Vout=3.3V

2.2uH: 74437324022 Wurth : 4x4x2 mm

3.3uH: 74437324033 Wurth : 4X4X2 mm

Figure 46. ISL80030 Single Output for VCCIO 2.5V



L=2.2uH R=200K Vout=1.8V
L=2.2uH R=316K Vout=2.5V
L=2.2uH R=450K Vout=3.3V

2.2uH: 74437324022 Wurth : 4x4x2 mm

3.3uH: 74437324033 Wurth : 4X4X2 mm

Figure 47. ISL80030 Single Output for VCCIO 1.8V

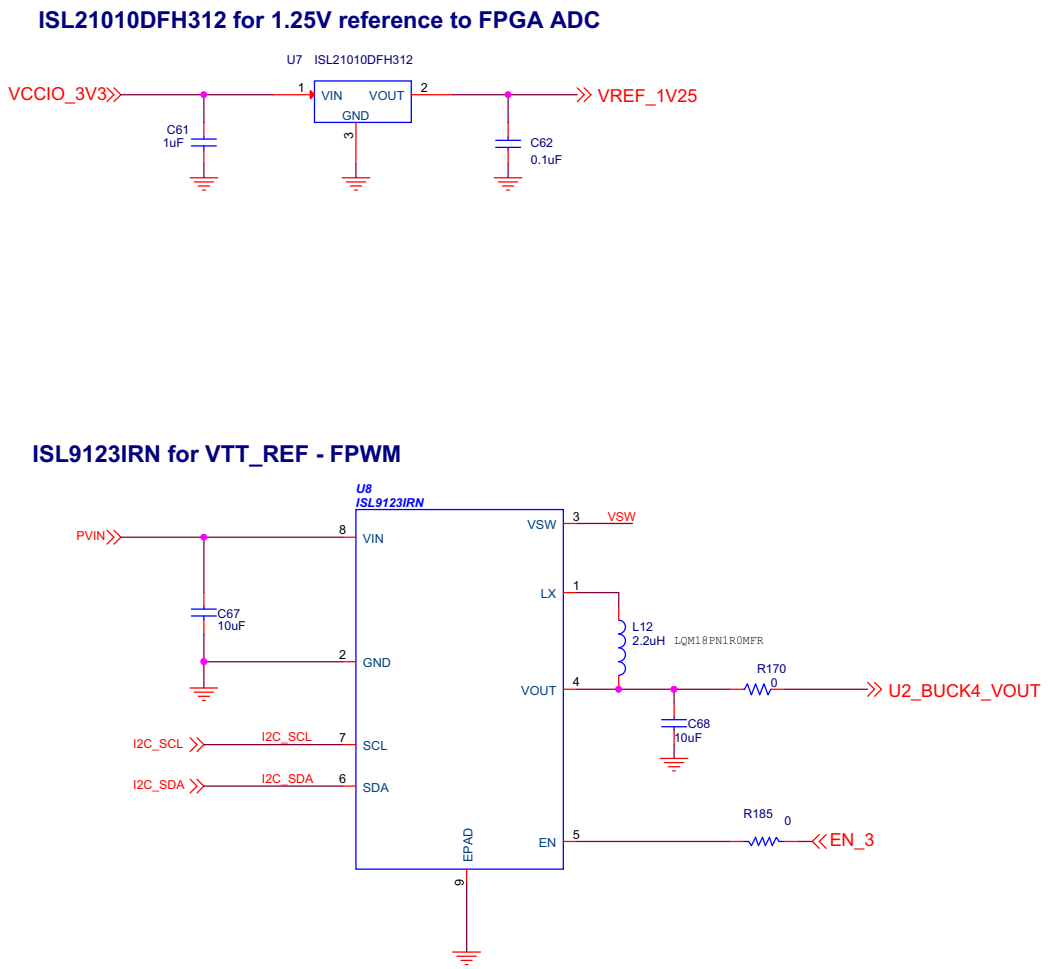


Figure 48. ISL21010DFH312 for 1.25V Reference to FPGA ADC, ISL9123IRN for VTT_REF - FPWM

3.3 PCB Layout and Bills of Materials

Contact Renesas support for PCB

4. Appendix

4.1 ARTIX-7 FPGA Power Solution Selection Table

Xilinx Device	Speed Grade	Renesas PMIC Part Number	DVS_PIN1	DVS_PIN0
XC7A12T	-1	ISL91211BIKZ-TR5877	1	1
XC7A12T	-2	ISL91211BIKZ-TR5877	1	1
XC7A12T	-1L(0.95V)	ISL91211BIKZ-TR5877	0	1
XC7A12T	-1L(0.95V)	ISL91211BIKZ-TR5877	0	1
XC7A12T	-2L	ISL91211BIKZ-TR5877	1	1
XC7A12T	-2L(0.9V)	ISL91211BIKZ-TR5877	0	0
XC7A12T	-3	ISL91211BIKZ-TR5877	1	1
XC7A12T	-3	ISL91211BIKZ-TR5877	1	1
XC7A15T	-1	ISL91211BIKZ-TR5877	1	1
XC7A15T	-2	ISL91211BIKZ-TR5877	1	1
XC7A15T	-1L(0.95V)	ISL91211BIKZ-TR5877	0	1
XC7A15T	-2L	ISL91211BIKZ-TR5877	1	1
XC7A15T	-2L(0.9V)	ISL91211BIKZ-TR5877	0	0
XC7A15T	-3	ISL91211BIKZ-TR5877	1	1
XC7A25T	-1	ISL91211BIKZ-TR5877	1	1
XC7A25T	-2	ISL91211BIKZ-TR5877	1	1
XC7A25T	-1L(0.95V)	ISL91211BIKZ-TR5877	0	1
XC7A25T	-1L(0.95V)	ISL91211BIKZ-TR5877	0	1
XC7A25T	-2L	ISL91211BIKZ-TR5877	1	1
XC7A25T	-2L(0.9V)	ISL91211BIKZ-TR5877	0	0
XC7A25T	-3	ISL91211BIKZ-TR5877	1	1
XC7A35T	-1	ISL91211BIKZ-TR5877	1	1
XC7A35T	-2	ISL91211BIKZ-TR5877	1	1
XC7A35T	-1L(0.95V)	ISL91211BIKZ-TR5877	0	1
XC7A35T	-2L	ISL91211BIKZ-TR5877	1	1
XC7A35T	-2L(0.9V)	ISL91211BIKZ-TR5877	0	0
XC7A35T	-3	ISL91211BIKZ-TR5877	1	1
XC7A50T	-1	ISL91211BIKZ-TR5877	1	1
XC7A50T	-2	ISL91211BIKZ-TR5877	1	1
XC7A50T	-1L(0.95V)	ISL91211BIKZ-TR5877	0	1
XC7A50T	-2L	ISL91211BIKZ-TR5877	1	1
XC7A50T	-2L(0.9V)	ISL91211BIKZ-TR5877	0	0
XC7A50T	-3	ISL91211BIKZ-TR5877	1	1
XC7A75T	-1	ISL91211BIKZ-TR5877	1	1
XC7A75T	-2	ISL91211BIKZ-TR5877	1	1
XC7A75T	-1L(0.95V)	ISL91211BIKZ-TR5877	0	1
XC7A75T	-2L	ISL91211BIKZ-TR5877	1	1
XC7A75T	-2L(0.9V)	ISL91211BIKZ-TR5877	0	0
XC7A75T	-3	ISL91211BIKZ-TR5877	1	1

Xilinx Device	Speed Grade	Renesas PMIC Part Number	DVS_PIN1	DVS_PIN0
XC7A75T	-2L	ISL91211BIKZ-TR5877	1	1
XC7A100T	-1	ISL91211BIKZ-TR5877	1	1
XC7A100T	-2	ISL91211BIKZ-TR5877	1	1
XC7A100T	-1L(0.95V)	ISL91211BIKZ-TR5877	0	1
XC7A100T	-2L	ISL91211BIKZ-TR5877	1	1
XC7A100T	-2L(0.9V)	ISL91211BIKZ-TR5877	0	0
XC7A100T	-3	ISL91211BIKZ-TR5877	1	1
XC7A200T	-1	ISL91211AIKZ-TR5873	0	1
XC7A200T	-2	ISL91211AIKZ-TR5873	0	1
XC7A200T	-1L(0.95V)	ISL91211AIKZ-TR5873	0	0
XC7A200T	-2L	ISL91211AIKZ-TR5873	0	1
XC7A200T	-3	ISL91211AIKZ-TR5873	0	1

4.2 Spartan-7 FPGA Power Solution Selection Table

Xilinx Device	Speed Grade	Renesas PMIC Part Number	DVS_PIN1	DVS_PIN0
XC7S6	-1	ISL91211BIKZ-TR5878	1	1
XC7S6	-2	ISL91211BIKZ-TR5878	1	1
XC7S6	-1L(0.95V)	ISL91211BIKZ-TR5878	1	0
XC7S15	-1	ISL91211BIKZ-TR5878	1	1
XC7S15	-2	ISL91211BIKZ-TR5878	1	1
XC7S15	-1L(0.95V)	ISL91211BIKZ-TR5878	1	0
XC7S25	-1	ISL91211BIKZ-TR5878	1	1
XC7S25	-2	ISL91211BIKZ-TR5878	1	1
XC7S25	-1L(0.95V)	ISL91211BIKZ-TR5878	1	0
XC7S50	-1	ISL91211BIKZ-TR5878	1	1
XC7S50	-2	ISL91211BIKZ-TR5878	1	1
XC7S50	-1L(0.95V)	ISL91211BIKZ-TR5878	1	0
XC7S75	-1	ISL91211BIKZ-TR5878	1	1
XC7S75	-2	ISL91211BIKZ-TR5878	1	1
XC7S75	-1L(0.95V)	ISL91211BIKZ-TR5878	1	0
XC7S100	-1	ISL91211BIKZ-TR5878	1	1
XC7S100	-2	ISL91211BIKZ-TR5878	1	1
XC7S100	-1L(0.95V)	ISL91211BIKZ-TR5878	1	0

5. Revision History

Rev.	Date	Description
1.00	Jan.30.20	Initial release

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