ISL91302BIK

Dual/Single Output PMIC with 12-Bit Telemetry ADC for Industrial and Computing Applications

The ISL91302BIK is a highly efficient, dual or single output, synchronous multiphase buck switching regulator that can deliver up to 5A per phase maximum output current. The ISL91302BIK features four integrated power stages and two controllers. The ISL91302BIK can assign its power stages and controllers to two dual-phase outputs (2+2) or one three-phase and one-phase output (3+1) or one-phase output (4+0). This flexibility allows seamless design-in for a wide range of applications in which dual, triple, or quad-phase outputs are needed, such as CPU and GPU core power mobile applications.

ISL91302BIK integrates low ON-resistance MOSFETs at 2MHz switching frequency, allowing very small external inductors and capacitors to be used. With automatic Diode Emulation and Pulse Skipping modes under light-load conditions, this feature improves efficiency and maximizes battery life. The ISL91302BIK delivers a highly robust power solution through a controller based on the Renesas proprietary Rapid Robust Ripple Regulator (R5) technology, offering tight output accuracy and load regulation, ultra-fast transient response, seamless DCM/CCM transitions, and no required external compensation.

In addition to the standard interrupt, chip enable, and watchdog reset functions, the ISL91302BIK also features four MPIOs and two GPIOs that support SPI, I2C communication protocol, external signal telemetry with an internal ADC, Dynamic Voltage Scaling (DVS) with selectable slew rates, and various other pin mode functions.

Features

- Dual output 3+1 or 2+2, or single output 4-phase
- 2.7V to 5.5V supply voltage
- 5A per phase output current capability
- Small solution size
- High efficiency (94% peak for 3.3V V_{IN}, 1.8V V_{OUT}, L = 220nH)
- Low I_Q in low power mode
- Proprietary control scheme reduces the output capacitor and supports fast load transients (such as 50A/µs per phase)
- Voltage, current, and temperature telemetry through integrated ADC plus auxiliary inputs
- ±0.7% system accuracy, remote voltage sensing
- I^2C and SPI programmable output from 0.3V to 2.0V
- Independent Dynamic Voltage Scaling (DVS) for each output
- Soft-start and fault detection (UV, OV, OC, OT), short-circuit protection
- 4.7mm x 6.3mm 35 ball TFBGA with 0.8mm pin pitch

Applications

- Industrial controls and FPGAs
- Computing servers and systems
- Home gateways and applicances

Related Literature

For a full list of related documents, visit our website

- ISL91302BIK product page

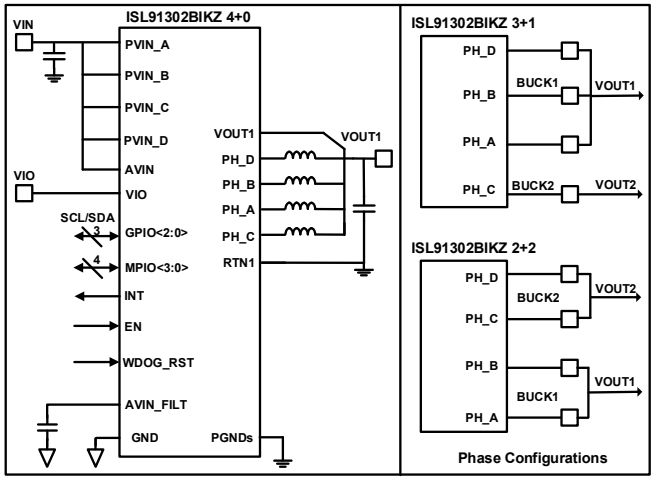


Figure 1. Simplified Block Diagram

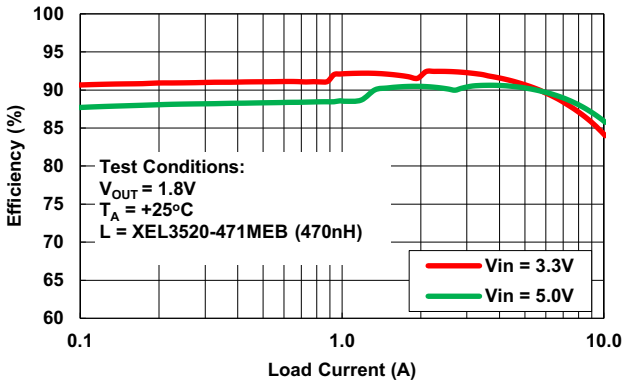


Figure 2. Efficiency vs Load Current

Contents

1. Overview

1.1 Typical Application Circuits

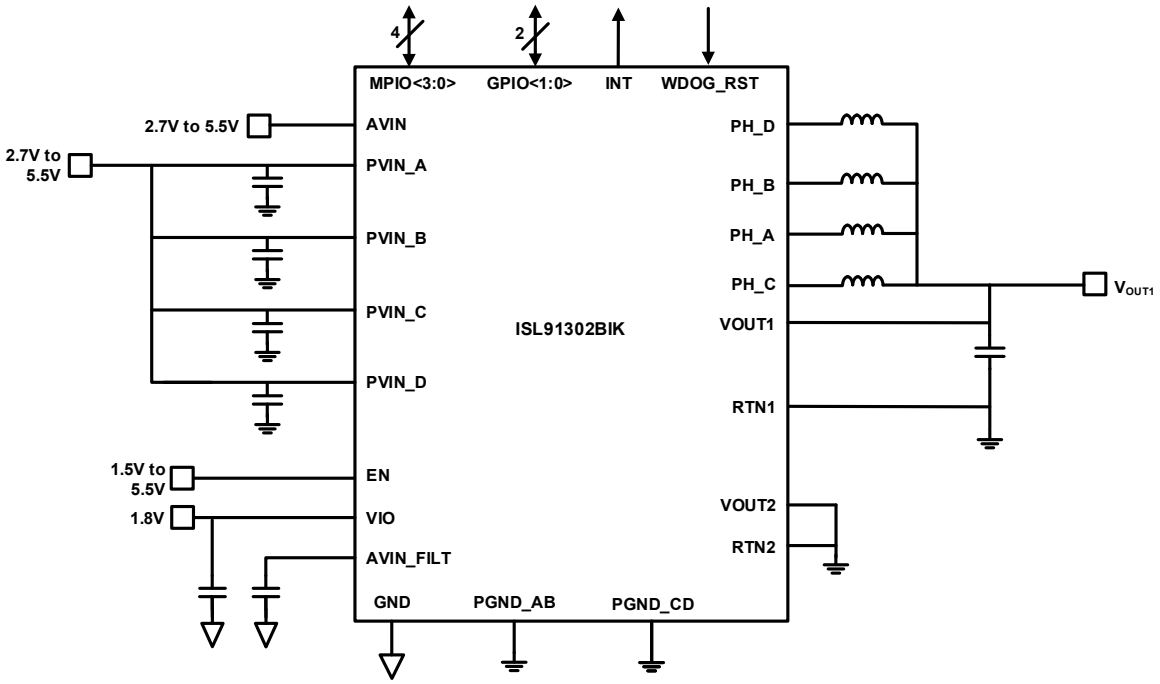


Figure 3. Typical Application 4-Phase Single Output

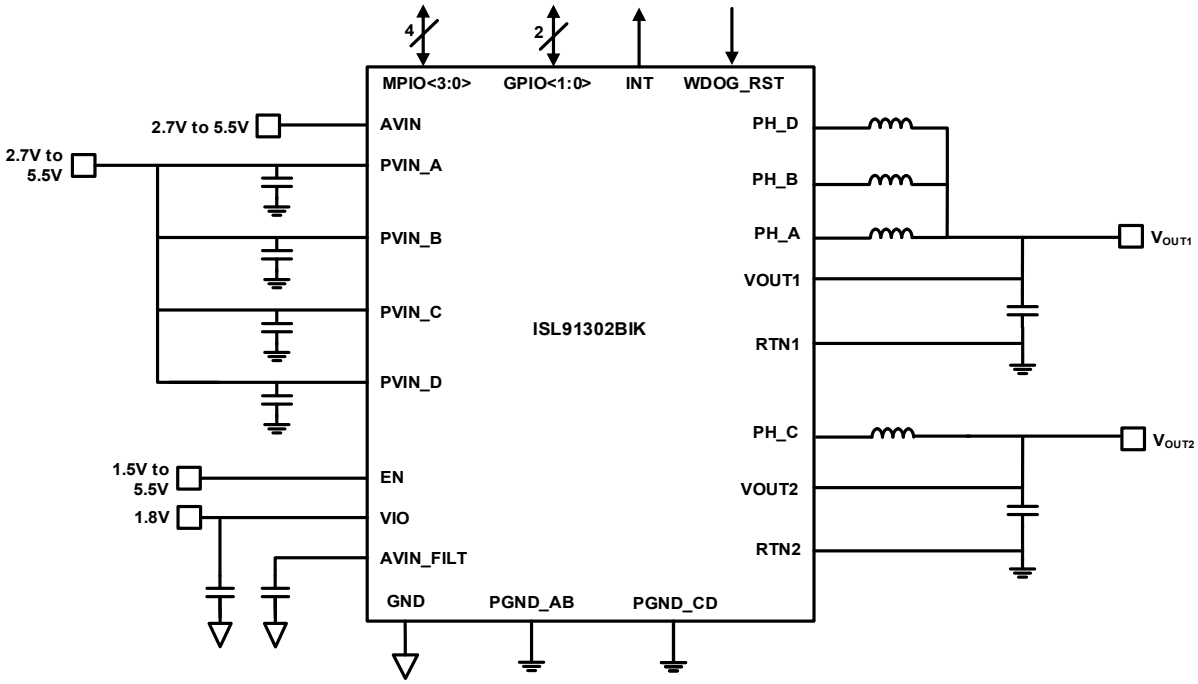


Figure 4. Typical Application Circuit: 3-Phase + 1-Phase

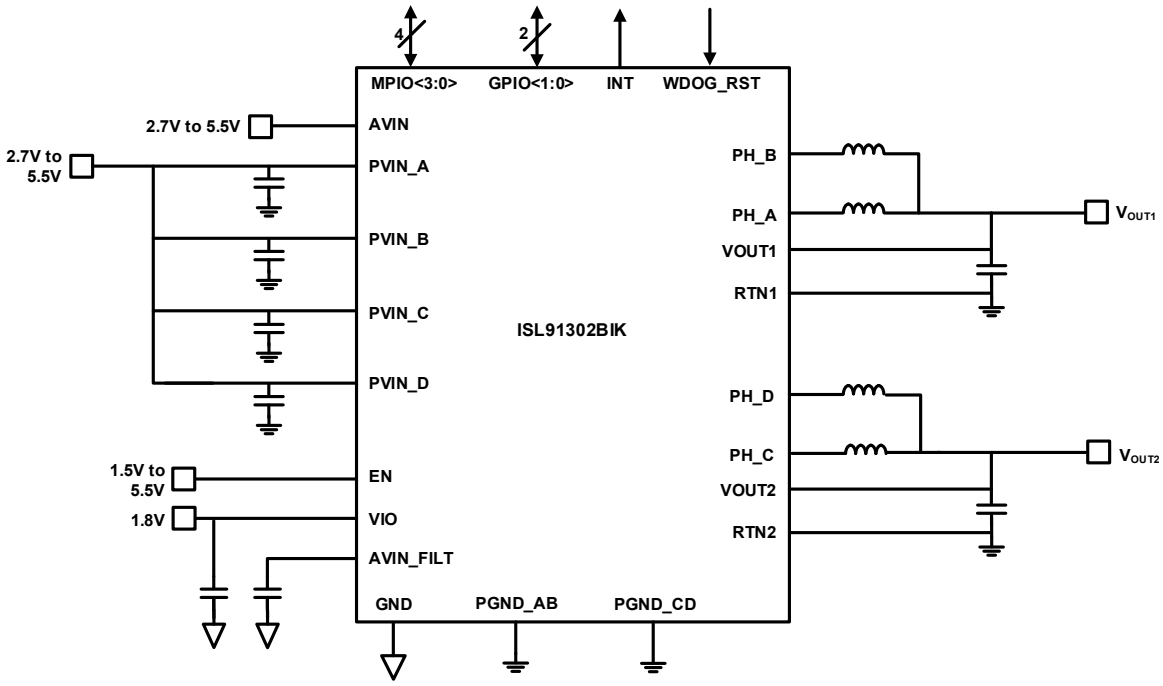


Figure 5. Typical Application Circuit: 2-Phase + 2-Phase

1.2 Block Diagram

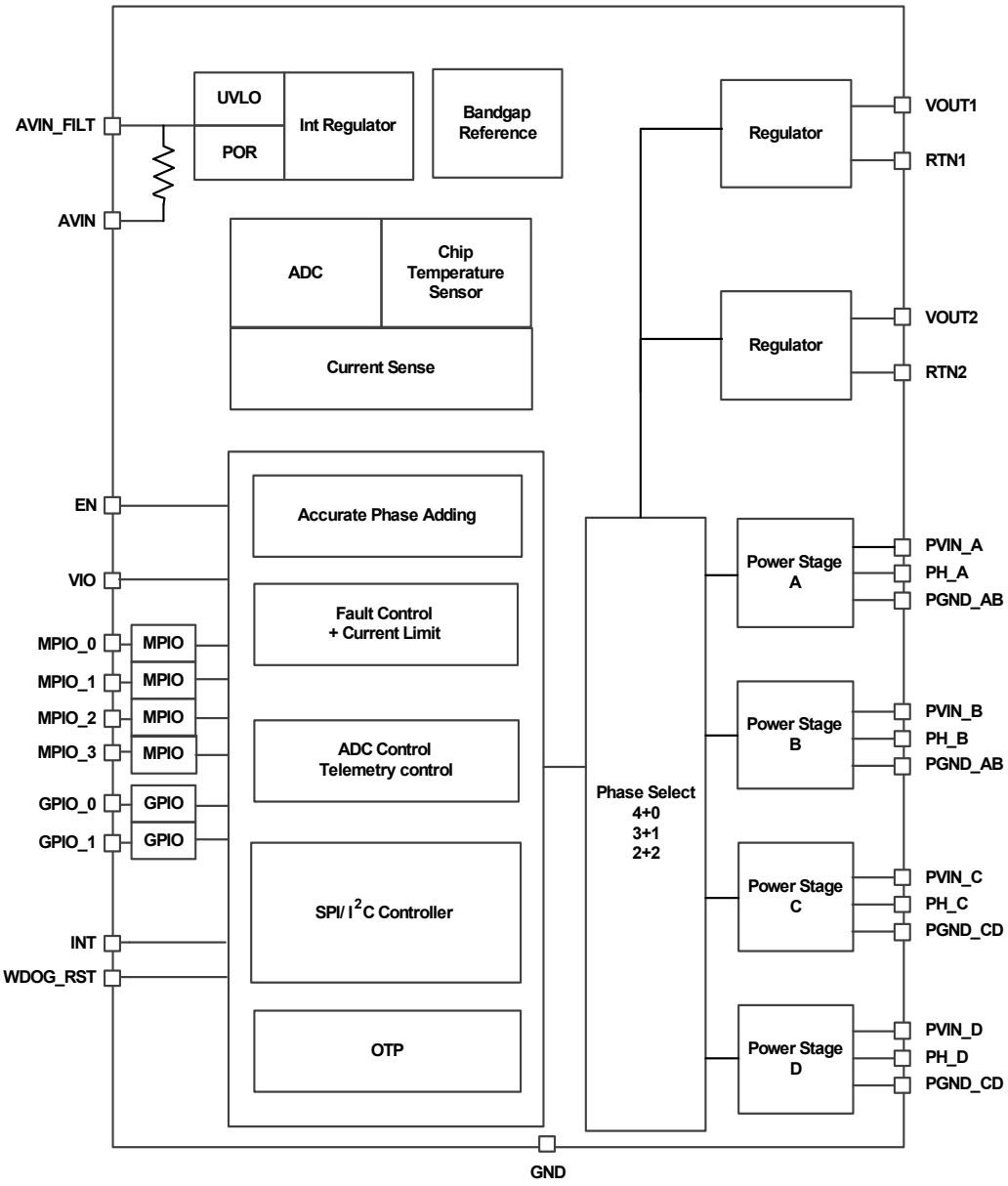


Figure 6. Block Diagram

1.3 Ordering Information

Part Number (Notes 1, 3, 4)	Part Marking	Temp Range (°C)	Tape and Reel (Units) (Note 2)	Package (RoHS Compliant)	Pkg. Dwg. #
ISL91302BIKZ-T	302BK	-40 to +85	3k	4.7mmx6.30mm, 35 ball TFBGA	V35.4.7x6.3
ISL91302BIIK22-EVZ	2-phase + 2-phase evlauation board				
ISL91302BIIK31-EVZ	3-phase + 1-phase evlauation board				
ISL91302BIIK40-EVZ	4-phase single output evaluation board				

Notes:

1. For additional part options contact your local sales office.
2. See TB347 for details about reel specifications.
3. These Pb-free BGA packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e6 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free BGA packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
4. For Moisture Sensitivity Level (MSL), see the ISL91302BIK device page. For more information about MSL, see TB363.

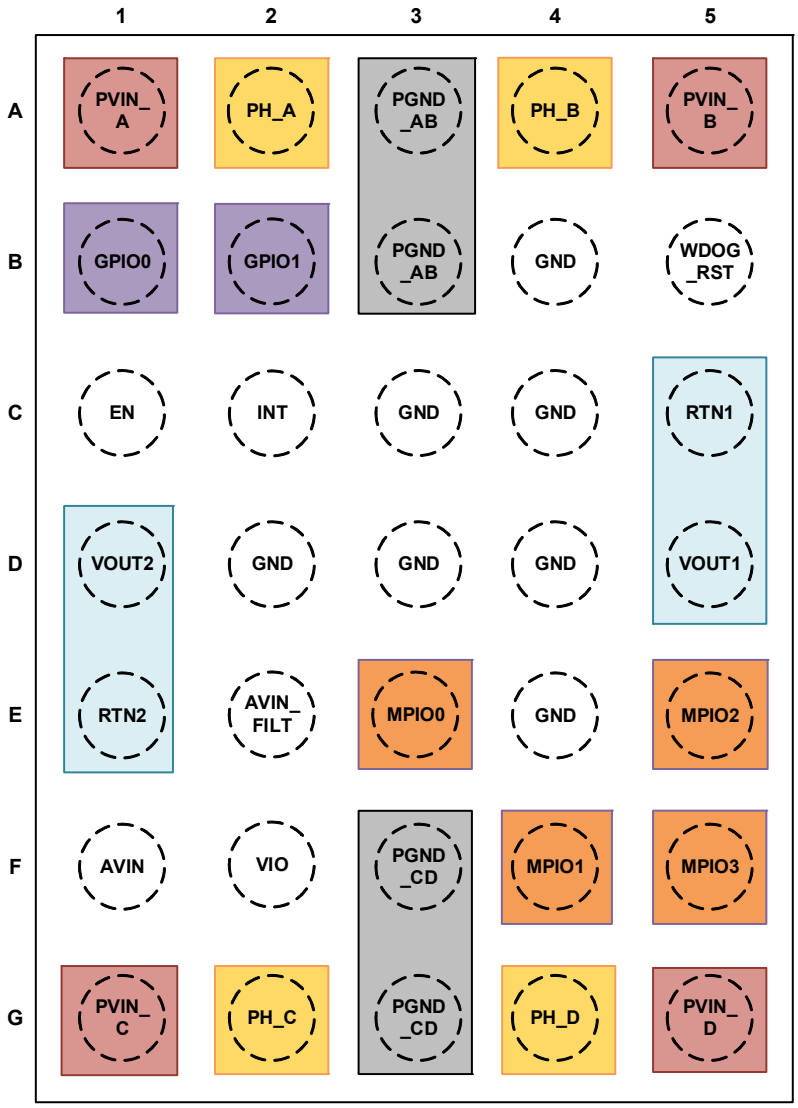
Table 1. Key Differences Between Family of Parts

Part Number	Pin Configuration	Pitch	Output Configuration	Maximum Load per Phase
ISL91302BIK	35 Ball 5x7 TFBGA	0.8mm	Single Output (4+0 Phase)	5A
	35 Ball 5x7 TFBGA	0.8mm	Dual Output (3+1 Phase)	5A
	35 Ball 5x7 TFBGA	0.8mm	Dual Output (2+2 Phase)	5A
ISL91211AIK	35 Ball 5x7 TFBGA	0.8mm	Triple Output (2+1+1 Phase)	5A
ISL91211BIK	35 Ball 5x7 TFBGA	0.8mm	Quad Output (1+1+1+1 Phase)	5A

1.4 Pin Configuration

35 Ball TFBGA
Top View

JEDEC Standard:
Balls Down, A1 Top Left Corner



1.5 Pin Descriptions

Pin Number	Pin Name	Type	Description
A1	PVIN_A	Input	Power supply for Power Stage A.
A2	PH_A	Output	Switching node for Power Stage A.
A3, B3	PGND_AB	Input	Ground connection for Power Stage A and B
A4	PH_B	Output	Switching node for Power Stage B.
A5	PVIN_B	Input	Power supply for Power Stage B.
B1	GPIO0	Input/Output	General purpose I/O pin, see Table 2.
B2	GPIO1		
B4, C3, C4, D2, D3, D4, E4	GND	Input	Analog chip ground. Ensure that pin D4 has a low impedance connection to the internal ground layer.
B5	WDOG_RST	Input	Digital input, resets the bucks to default output voltage.

Pin Number	Pin Name	Type	Description
C1	EN	Input	Master chip enable input, NMOS logic threshold.
C2	INT	Output	Interrupt line.
C5	RTN1	Input	Remote ground voltage sense for Buck #1.
D1	VOUT2	Input	Remote output voltage sense for Buck #2.
D5	VOUT1	Input	Remote output voltage sense for Buck #1.
E1	RTN2	Input	Remote ground voltage sense for Buck #2.
E2	AVIN_FILT	Output	Filtered analog supply voltage, 2.7 to 5.5V. Place a decoupling capacitor close to the IC.
E3	MPIO0	Input/Output	Multipurpose I/O, see Table 2.
E5	MPIO2		
F4	MPIO1		
F5	MPIO3		
F1	AVIN	Input	Analog supply voltage, 2.7V to 5.5V.
F2	VIO	Input	I/O supply voltage for digital communications. Normally connected to 1.8V supply.
F3, G3	PGND_CD	Input	Ground connection for Power Stage C and D
G1	PVIN_C	Input	Power supply connection for Power Stage C.
G2	PH_C	Output	Switching node for Power Stage C.
G4	PH_D	Output	Switching node for Power Stage D.
G5	PVIN_D	Input	Power supply connection for Power Stage D.

1.6 I/O Pin Configurations

The ISL91302BIK features two general purpose I/O (GPIO) pins for I^{2}C and other functions, along with four multipurpose I/O (MIO) pins. These pins perform different functions depending on the IO_PINMODE setting. The default factory setting for IO_PINMODE is 0x0. For features requiring IO_PINMODE to be different than the default value, contact Renesas support for factory OTP programming.

Table 2. I/O Pin Mode

IO_PINMODE	MPIO0	MPIO1	MPIO2	MPIO3	GPIO0	GPIO1	Description
0x0	SCK	SS_B	MOSI	MISO	SCL	SDA	I^{2}C/SPI both available
0x1	SCK	SS_B	MOSI	MISO	EN_A	EN_B	SPI mode with hardware enables for Bucks 1-2
0x3	SCK	SS_B	MOSI	MISO	DVS1_0	DVS2_0	SPI with hardware DVS pins
0x4	DVS_PIN1	DVS_PIN0	PGOOD1	PGOOD2	SCL	SDA	I^{2}C with global DVS mode with PGOOD1 and PGOOD2
0x5	BUCK1_DVS0	BUCK1_DVS1	BUCK2_DVS0	BUCK2_DVS1	SCL	SDA	I^{2}C with full pin controlled DVS for Buck1 and Buck2
0x6	BUCK1_DVS0	BUCK2_DVS0	PGOOD1	PGOOD2	SCL	SDA	I^{2}C with DVS and PGOOD for Buck1 and Buck2
0xD	ADC_IN0	ADC_IN1	PGOOD1	PGOOD2	SCL	SDA	I^{2}C with ADC input and PGOOD1 and PGOOD2
0xE	ADC_IN0	ADC_IN1	DVS_PIN1	DVS_PIN0	SCL	SDA	I^{2}C with ADC input and global DVS

Note: Pinmodes 0x7 through 0xC and 0xF are reserved.

Table 3. Pin Mode Descriptions

Name	Definition
SCK	SPI clock.
SS_B	SPI slave select (must be pulled to VIO when using I^2C).
MOSI	SPI master out slave in.
MISO	SPI master in slave out.
SCL	I^2C clock.
SDA	I^2C data.
PGOOD1, PGOOD2	Power-good output pins. PGOOD pins for BUCK1 and BUCK2
EN_A, EN_B	Buck enable input pins. Two buck enable input pins. A single buck enable pin can enable/disable up to two bucks. Enable/disable on a buck can be controlled from one enable pin (EN_A or EN_B)
DVS_PIN1, DVS_PIN0	Global DVS logic pins which references a look-up table to allow complete DVS control.
BUCK1_DVS0, BUCK1_DVS1	DVS input logic pins for Buck1.
BUCK2_DVS0, BUCK2_DVS1	DVS input logic pins for Buck2.
ADC_IN0, ADC_IN1	Input pins for auxiliary ADC.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
PVIN and AVIN Pins to PGND	-0.3	+6	V
VOUT Pin BUCKx_VOUTFBDIV = 0x0	-0.3	+2.0	V
VOUT Pin BUCKx_VOUTFBDIV = 0x1	-0.3	+2.4	V
VOUT Pin BUCKx_VOUTFBDIV = 0x2	-0.3	+3.0	V
PH to PGND	-0.3	+0.3 + PVIN	V
VIO EN Pins to GND	-0.3	+0.3 + AVIN	V
RTN, GND to PGND Pins	-0.3	+0.3	V
INT, WDOG_RST, MPIO, GPIO Pins to GND	-0.3	+0.3 + VIO	V
ESD Ratings (Note 5)	**Value**		**Unit**
Human Body Model (Tested per JS-001-2017)	2		kV
Charged Device Model (Tested per JS-002-2014)	750		V
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Note:

5. ESD ratings apply to external pins only.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
35 Ball TFBGA Package (Notes 6, 7)	47	3

Notes:

6. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
7. For θ_{JC}, the case temperature location is taken at the package top center.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+150	°C
Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	See TB493		

2.3 Recommended Operation Conditions

Parameter	Minimum	Maximum	Unit
Junction Temperature	-40	+125	°C
Supply Voltage			
AVIN to GND	2.7	5.5	V
PVIN to PGND	2.7	5.5	V
VIO Voltage (VIO to GND)	1.7	AVIN	V
INT, WDOG_RST, MPIO, GPIO Pins to GND	0	VIO	V

2.4 Analog Specifications

AVIN/PVIN = 3.7V, V_{OUT} = 1V, L = 220nH, Frequency = 2MHz, VIO = 1.8V, T_A = +25°C. **Boldface limits apply across the operating junction temperature range, -40°C to +85°C unless otherwise noted.**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
Input Supply						
Supply Voltage	AVIN		**2.7**		**5.5**	V
Supply Voltage	PVIN		**2.7**		**5.5**	V
AVIN Supply Current	I_Q	EN = 0V		0.1	1	µA
AVIN + PVIN Supply Current		EN = 0V		<1	6	µA
AVIN + PVIN Supply Current EN = AVIN = PVINx = 3.7V		BUCK1_EN[0] = 0x0 and BUCK2_EN[0] = 0x0		22		µA
		4+0 OTP configuration, not switching BUCK1_EN[0] = 0x1 DCM operation BUCK2_EN[0] = 0x0		75		µA
		4+0 OTP configuration, not switching BUCK1_EN[0] = 0x1 1PH CCM operation BUCK2_EN[0] = 0x0		635		µA
		4+0 OTP configuration, not switching BUCK1_EN[0] = 0x1 4PH CCM operation BUCK2_EN[0] = 0x0		765		µA
		2+2 OTP configuration, not switching BUCK1_EN[0] = 0x0 BUCK2_EN[0] = 0x1 DCM operation		85		µA
		2+2 OTP configuration, not switching BUCK1_EN[0] = 0x0 BUCK2_EN[0] = 0x1 1PH CCM operation		485		µA
		2+2 OTP configuration, not switching BUCK1_EN[0] = 0x0 BUCK2_EN[0] = 0x1 2PH CCM operation		560		µA
UVLO Rising Threshold	V_{UVLOR}	Rising	**2.52**	2.60	**2.67**	V
UVLO Falling Threshold	V_{UVLOF}	Falling	**2.28**	2.34	**2.39**	V
Buck Regulation						
Buck Output Voltage Range (Each Output)	V_{OUT}	BUCKx_VOUTFBDIV[1:0] = 0x00	**0.300**		**1.2**	V
		BUCKx_VOUTFBDIV[1:0] = 0x01	**0.375**		**1.5**	V
		BUCKx_VOUTFBDIV[1:0] = 0x02	**0.500**		**2.0**	V
Output Voltage Step Size	V_{STEP}	10-bit control, BUCKx_VOUTFBDIV[1:0] = 0x00		1.2		mV
		10-bit control, BUCKx_VOUTFBDIV[1:0] = 0x01		1.5		mV
		10-bit control, BUCKx_VOUTFBDIV[1:0] = 0x02		2.0		mV
Output Voltage Accuracy (Note 9)	V_{ACC}	CCM, V_{OUT} > 0.6V	-0.3		0.3	%
		CCM, V_{OUT} > 0.6V T_A = -10°C to +85°C	-0.7		0.7	%
		CCM, V_{OUT} < 0.6V	-4		4	mV
		CCM, V_{OUT} < 0.6V T_A = -10°C to +85°C	-5.5		5.5	mV
Current Matching	I_{MATCH}	I_{OUT} = 5A per phase		10		%
Dynamic Response						
Dynamic Voltage Scaling (Output Slew Rate)	V_{DVS}	2.7V < V_{IN} < 5.5V: factory default = 3mV/µs	**-15**		**15**	%

AVIN/PVIN = 3.7V, V_{OUT} = 1V, L = 220nH, Frequency = 2MHz, VIO = 1.8V, T_A = +25°C. **Boldface limits apply across the operating junction temperature range, -40°C to +85°C unless otherwise noted. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
Boot-Up Time	V_{BT}	Delay from when PVIN, AVIN, and EN are asserted to when the first buck's reference starts ramping. This time includes internal reference startup, OTP load and buck controller calibration time. BUCKx_EN_DELAY = 0x00		1.4		ms
Frequency						
CCM Frequency Tolerance	f_{SW_TOL}	Factory default = 2MHz	-15		15	%
Power Stage						
Buck Output Current (Each Phase)		2.7V < V_{IN} < 5.5V			5	A
High-Side Switch ON-Resistance	HS $r_{DS(ON)}$	Conditions: PVIN = 3.7V, Current = 300mA		32		mΩ
Low-Side Switch ON-Resistance	LS $r_{DS(ON)}$	Conditions: PVIN = 3.7V, Current = 300mA		17.5		mΩ
Protection						
HSD Current Limit (WOC)	I_{LIMIT}	2.7V < V_{IN} < 5.5V Phase Count = 2 or more; WOC = 11.35A	-10		10	%
		2.7V < V_{IN} < 5.5V Phase Count = 1; WOC = 8.38A	-10		10	
Thermal Shutdown Accuracy	T_{SPS}	2.7V < V_{IN} < 5.5V, factory default = +140°C	-10		10	%
Thermal Shutdown Hysteresis	T_{SPS_HYS}	2.7V < V_{IN} < 5.5V, factory default = +60°C	-10		10	%
Thermal Warning Alert	T_{ALERT}	2.7V < V_{IN} < 5.5V, factory default = +85°C	-10		10	%
Thermal Warning Hysteresis	T_{ALERT_HYS}	2.7V < V_{IN} < 5.5V, factory default = +12°C	-10		10	%
Output OVP Threshold Accuracy	V_{OVP}	Threshold: +250mV	-35		40	mV
Output UVP Threshold Accuracy	V_{UVP}	Threshold: -250mV	-35		35	mV
ADC						
Output Current Sense Offset	I_{SENSE_OFFSET}		-75		75	mA
Output Current Sense Accuracy	I_{SENSE_ADC}	I_{LOAD} = 500mA (minus offset)	-10		10	%
		3.0V < V_{IN} < 5.0V I_{LOAD} = 500mA (minus offset)	-15		15	%
MPIO/GPIO Operating Conditions						
Allowable Range of Supply for Operation	VIO		1.70	1.80	AVIN	V
Chip Enable Logic Threshold Level						
Low-Level Input Voltage	V_{IL}				0.5	V
High-Level Input Voltage	V_{IH}		1.35			V
Serial Interfaces						
I^2C Frequency Capability	f_{I2C}				3.4	MHz
SPI Frequency Capability	f_{SPI}			26		MHz
MPIO/GPIO Logic Threshold Levels						
Low Level Input Voltage	V_{IL}				0.25 * VIO	V
High Level Input Voltage	V_{IH}		0.75 * VIO			V
Hysteresis on Input	V_{HYS}		0.1 * VIO			V

AVIN/PVIN = 3.7V, V_{OUT} = 1V, L = 220nH, Frequency = 2MHz, VIO = 1.8V, T_A = +25°C. **Boldface limits apply across the operating junction temperature range, -40°C to +85°C unless otherwise noted. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
Low Level Output	V_{OL}	1mA			0.4	V
High Level Output	V_{OH}	1mA	VIO - 0.4			V

Note:

8. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
9. V_{OUT} feedback divider ratio equals 1 (BUCKx_VOUTFBDIV[1:0] = 0x00).
10. As per "Thermal Information" on page 10, operating beyond thermal limits can cause permanent damage.

3. Output Configurations

Table 4. Output Configurations

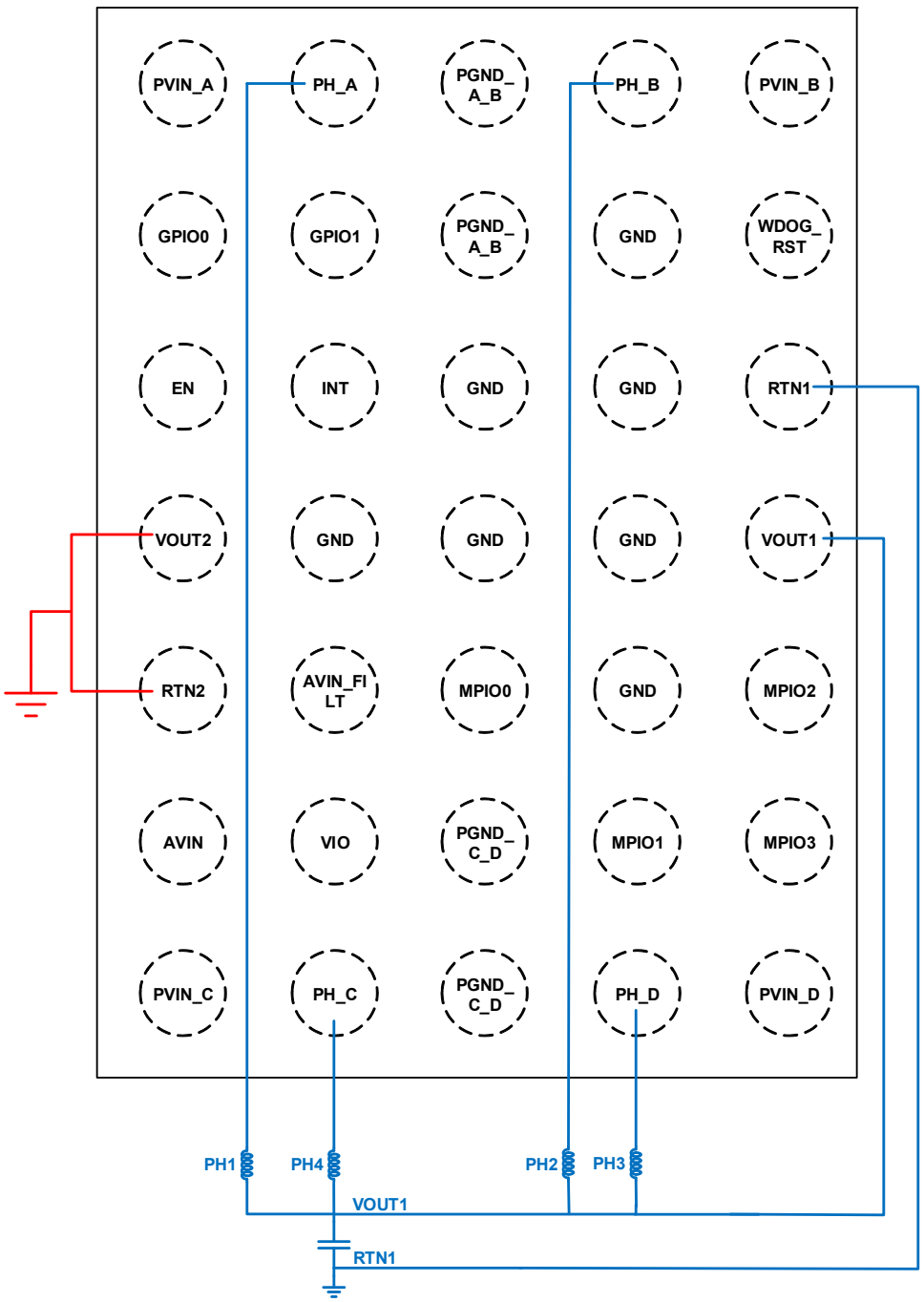
Output Configuration	Power Stage Assignment	Diagram
4-Phase Connect VOUT2 and RTN2 to PGND Plane	4-Phase: Buck #1 (VOUT1) • Ph1: PH_A • Ph2: PH_B • Ph3: PH_D • Ph4: PH_C	4+0 Configuration 

Table 4. Output Configurations (Continued)

Output Configuration	Power Stage Assignment	Diagram
3-Phase + 1-Phase	3+1 Configuration: • 3-phase: Buck #1 (VOUT1) Ph1: PH_A Ph2: PH_B Ph3: PH_D • 1-phase: Buck #2 (V_{OUT2}) Ph1: PH_C	3+1 Configuration

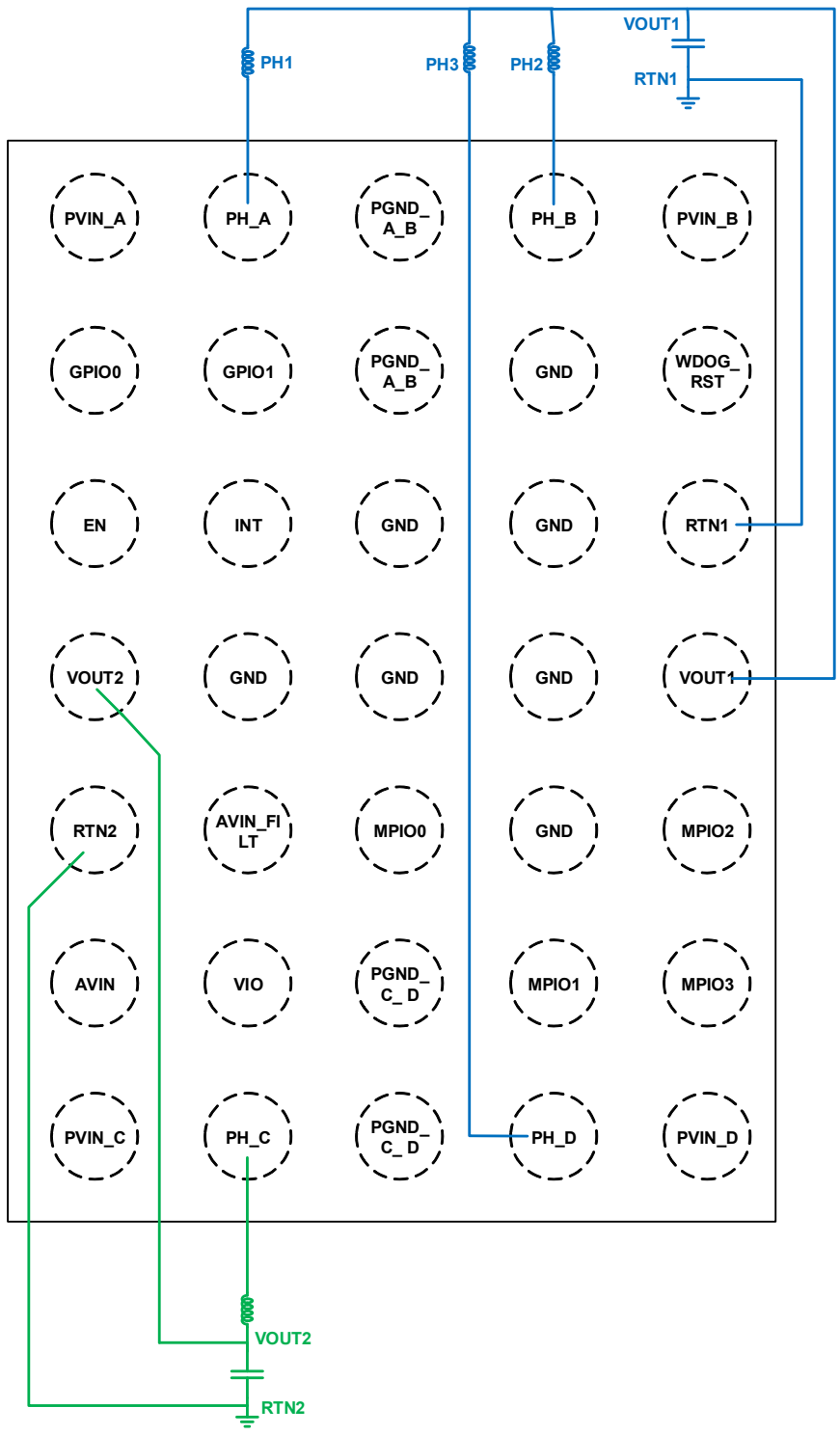
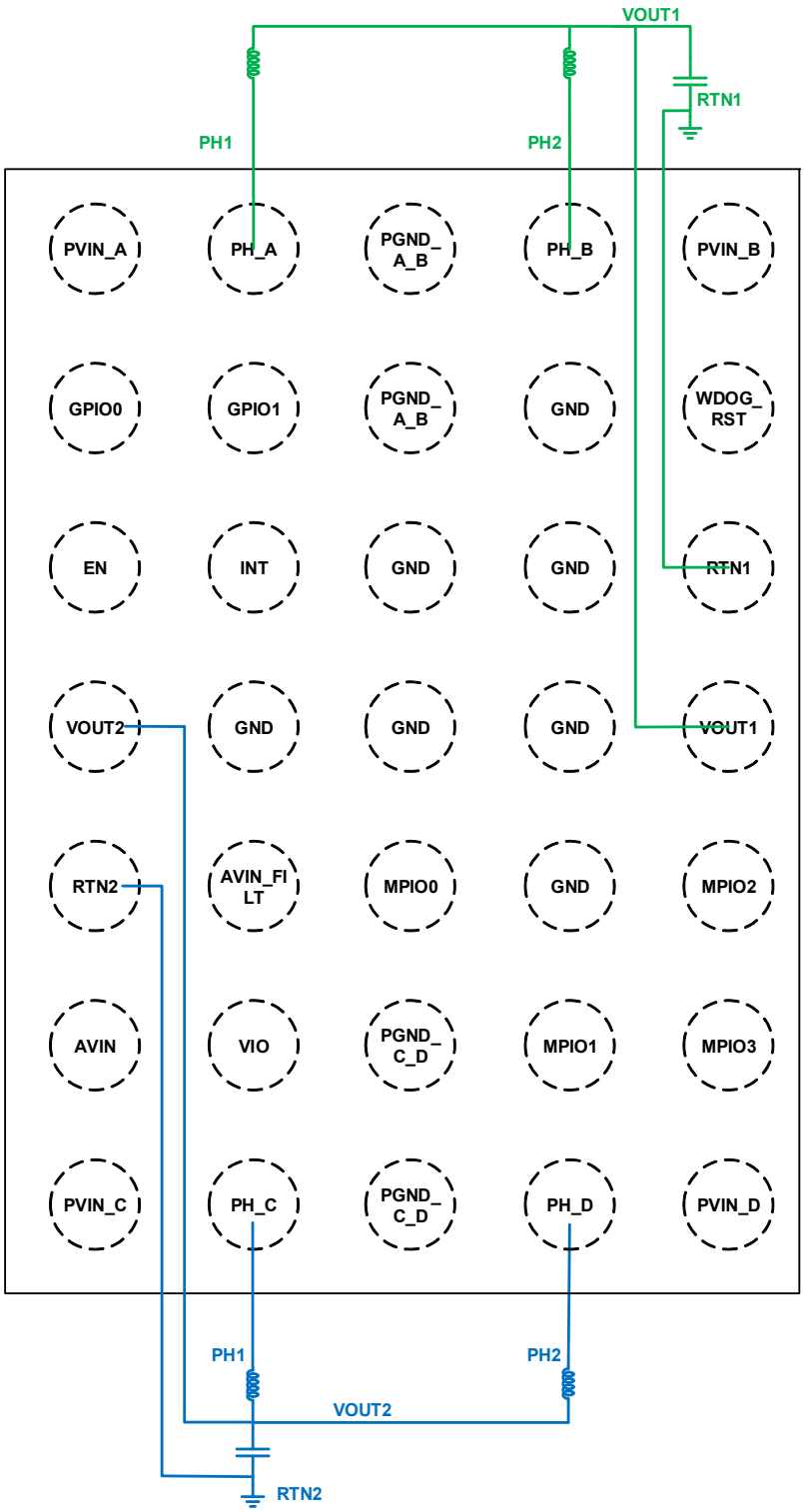


Table 4. Output Configurations (Continued)

Output Configuration	Power Stage Assignment	Diagram
2-Phase + 2-Phase	2+2 Configuration • 2-phase: Buck #1 (VOUT1) Ph1: PH_A Ph2: PH_B • 2-phase: Buck #2 (V_{OUT2}) Ph1: PH_C Ph2: PH_D	2+2 Configuration 

4. Typical Operating Performance

Unless otherwise noted, operating conditions are: V_{IN} = 3.8V, V_{OUT} = 1.1V, VIO and Enable = 1.8V, T_A = +25°C, f_{SW} = 2MHz, 2-phase operation, L = 220nH, C_{OUT} = 5x22µF.

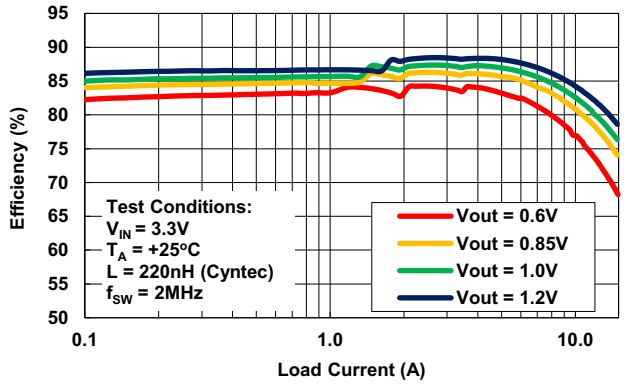


Figure 7. 3-Phase Configuration Efficiency

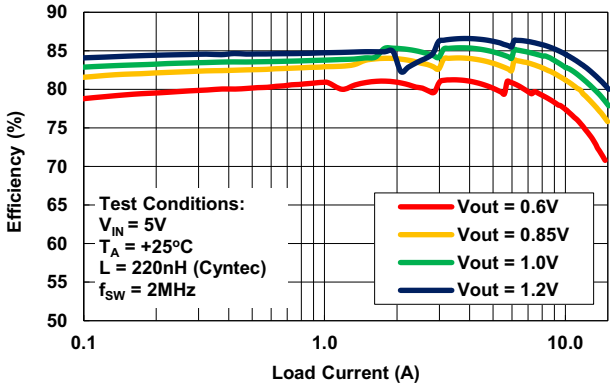


Figure 8. 3-Phase Configuration Efficiency

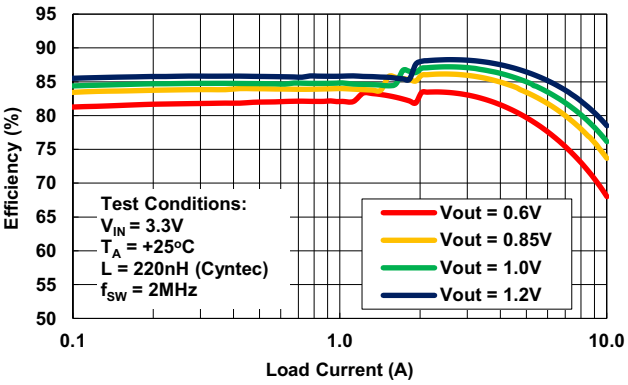


Figure 9. 2-Phase Configuration Efficiency

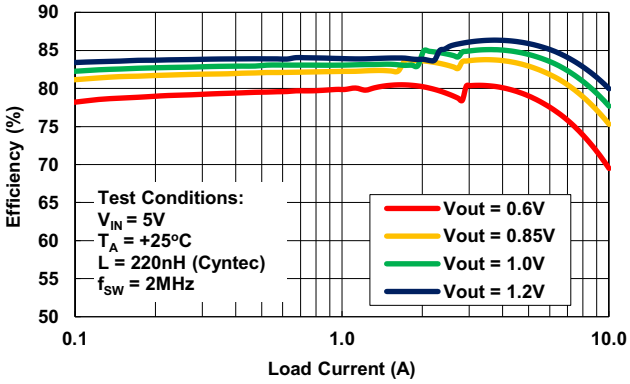


Figure 10. 2-Phase Configuration Efficiency

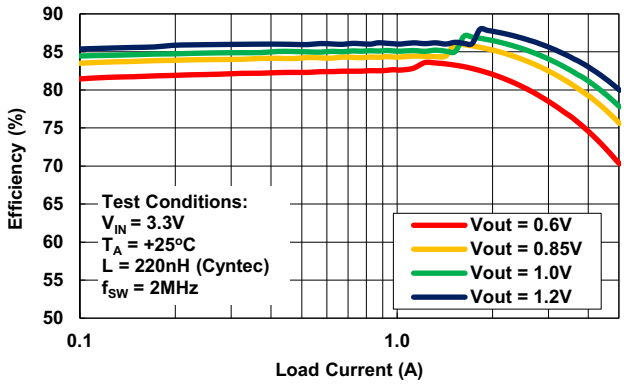


Figure 11. 1-Phase Configuration Efficiency

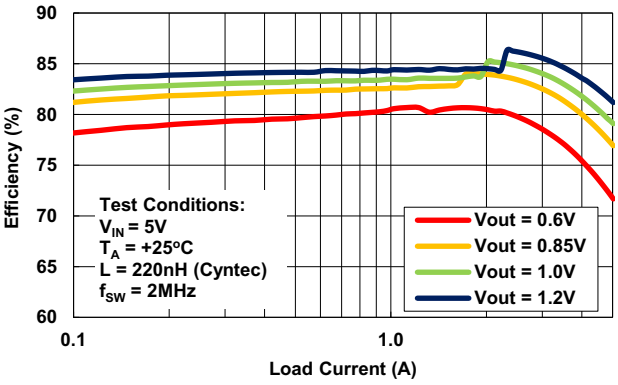


Figure 12. Single-Phase Configuration Efficiency

Unless otherwise noted, operating conditions are: V_{IN} = 3.8V, V_{OUT} = 1.1V, VIO and Enable = 1.8V, T_A = +25°C, f_{SW} = 2MHz, 2-phase operation, L = 220nH, C_{OUT} = 5x22µF. **(Continued)**

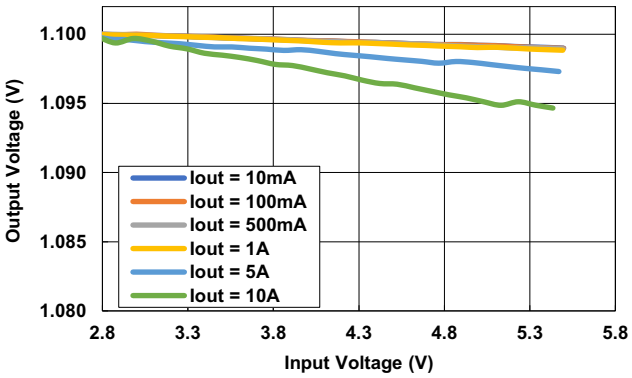


Figure 13. 2-Phase V_{OUT} vs V_{IN} (10mA to 10A)

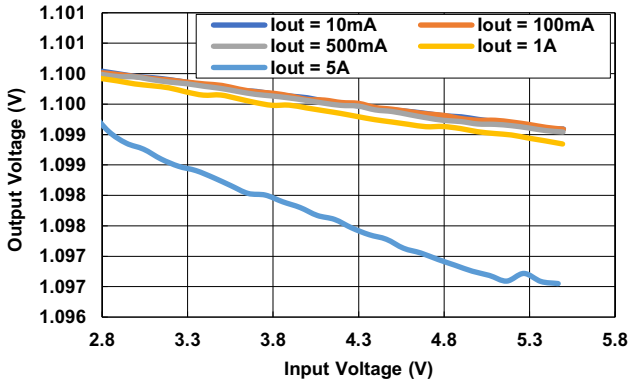


Figure 14. Single Phase V_{OUT} vs V_{IN} (10mA to 5A)

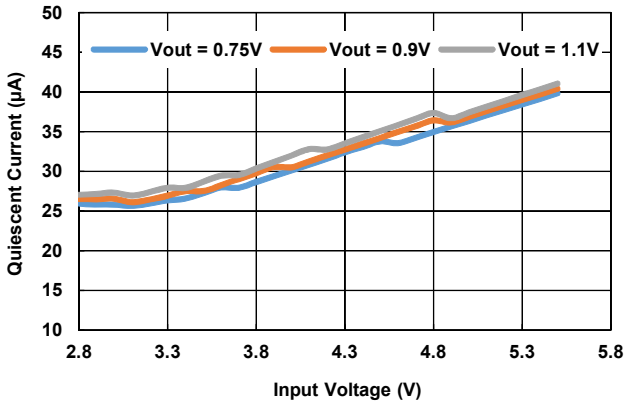


Figure 15. PVIN Quiescent Current (PFM Mode)

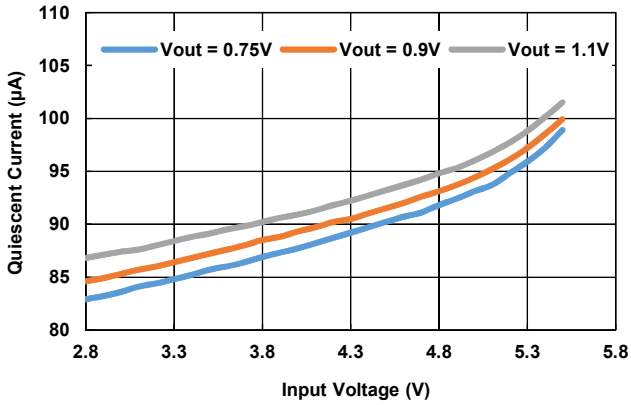


Figure 16. PVIN Quiescent Current (PWM Mode)

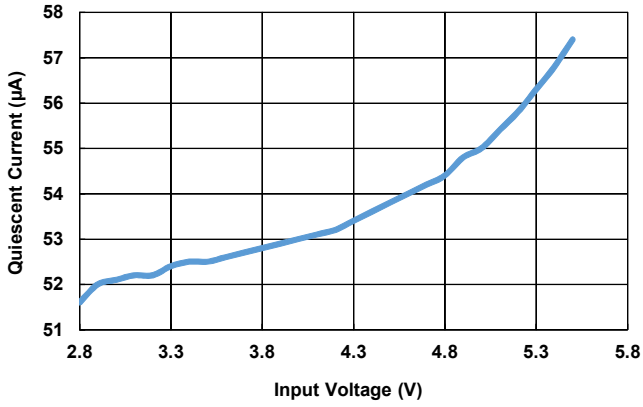


Figure 17. PVIN Quiescent Current (No Switching)

Unless otherwise noted, operating conditions are: V_{IN} = 3.8V, V_{OUT} = 1.1V, VIO and Enable = 1.8V, T_A = +25°C, f_{SW} = 2MHz, 2-phase operation, L = 220nH, C_{OUT} = 5x22µF. **(Continued)**

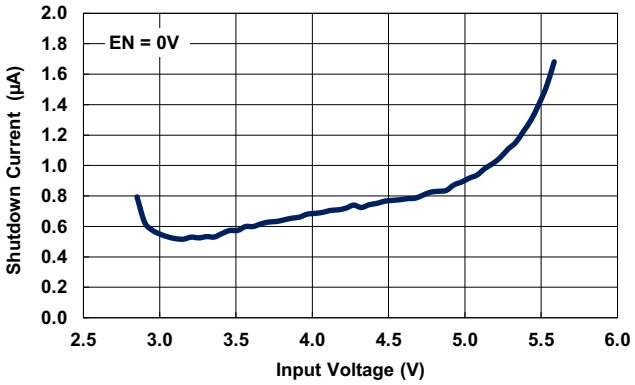


Figure 18. Shutdown EN = 0V

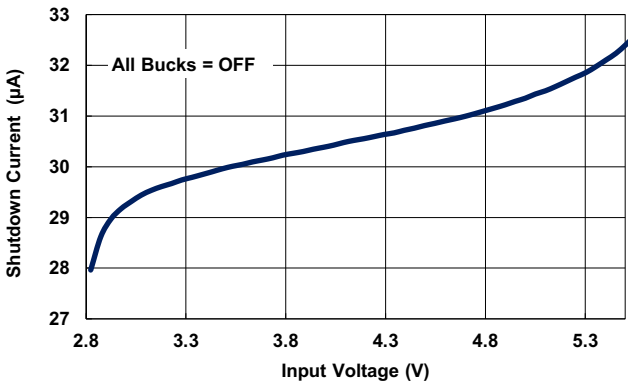


Figure 19. Shutdown All Bucks Off

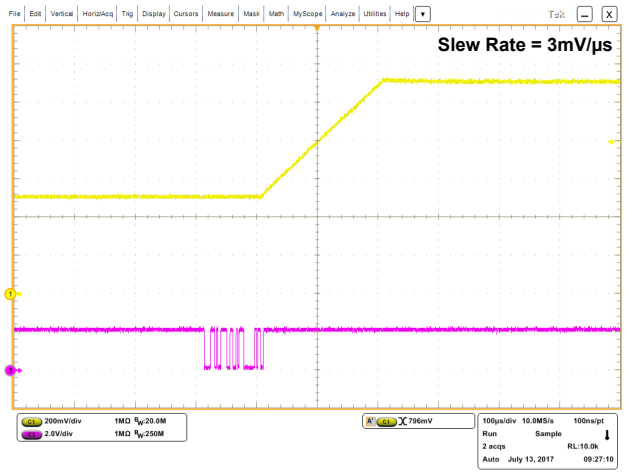


Figure 20. 0.5V to 1.1V DVS; Load = 5A

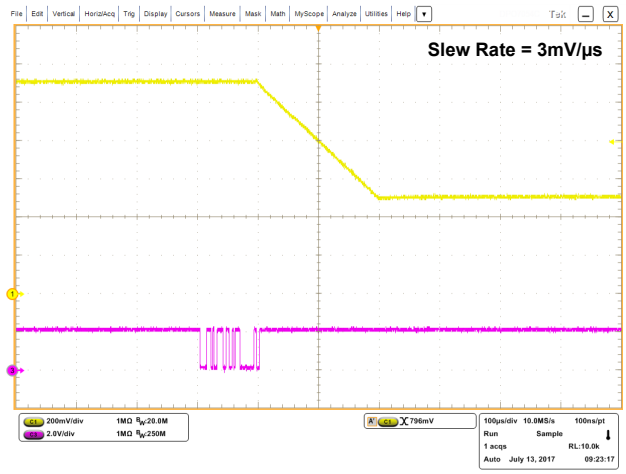


Figure 21. 1.1V to 0.5V DVS; Load = 5A

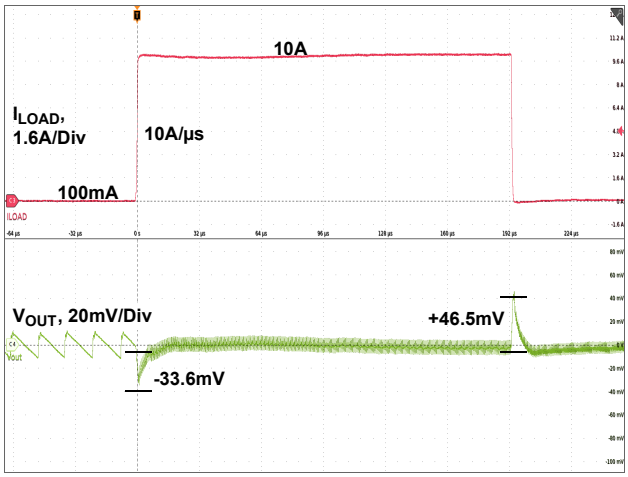


Figure 22. Dual-Phase Transient

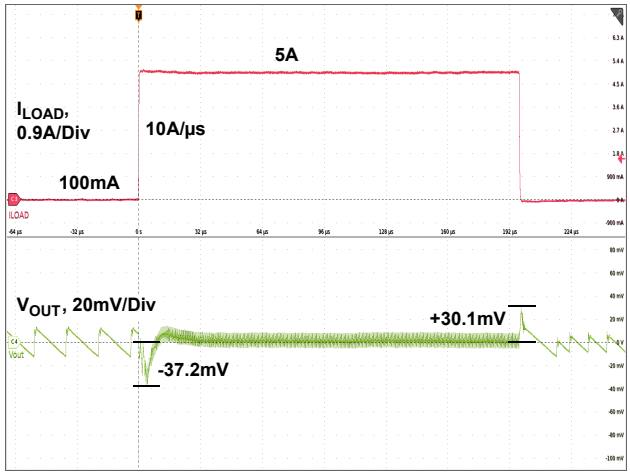


Figure 23. Single-Phase Transient

5. Applications Information

5.1 Inductor Selection

The ISL91302BIK is a high efficiency, high performance, dual output multiphase/single-phase synchronous buck converter that can deliver up to 5A of peak current per phase at 0.3V to 2.0V regulated voltage. The ISL91302BIK operates as one quad-phase output (4+0), one three-phase and one single-phase output (3+1), or two dual-phase outputs (2+2) at a switching frequency fixed at 2MHz. Switching MOSFETs are fully integrated and no additional external MOSFETs or diodes are needed. Each phase requires an equal external inductor, that can deliver up to the maximum load current divided by the number of phases used.

Table 5. Recommended Output Inductors

Manufacturer	Part Number	L x W x H (mm)	Value (nH)	DCR mΩ (Typ)	I_{SAT} (Typ)
Cyntec	HMLB25201T	2.5x2.0x1.0	220	9.4	7.0
Taiyo Yuden	MAKK2520HR22M	2.5x2.0x1.0	220	16	8.5
Cyntec	HTTN2016T	2.0x1.6x1.0	220	13	7.2
Murata	DFE2016E	2.0x1.6x1.0	240	16	7.0
Murata	DFE252012F	2.5x2.0x1.2	470	23	6.7

5.2 Output Capacitor Selection

Output capacitors are needed to provide filtering of square voltage at the phase node into a regulated output voltage. The amount of output capacitance required is based on the parameters of the maximum load step, the slew rate of the load step, and the maximum allowable voltage regulation tolerance during the transient. The amount of ripple voltage at the output capacitor is also a design constraint; the total peak-to-peak ripple voltages produced from the output capacitor is equal to its ESR multiplied by the worst case inductor ripple current.

Make sure to select X7R or X5R type capacitors and consider for DC bias effects. A wide range of output capacitor values can be used.

Table 6. Recommended Output Capacitors

Manufacturer	Part Number	Case Size	Value (µF)	Voltage Rating (V)
TDK	C1608X5R1A226M080AC	0603	22	10
TDK	C0510X6S0G105M030AC	0204	1	4
Murata	LLD154R60G435ME01	0402	4.3	4
Murata	LLL1U4R60G435ME22	0204	4.3	4

5.3 Input Capacitor Selection

Ceramic input capacitors source the AC component of the input current flowing into the high-side MOSFETs. Place them as close to the IC as possible. A 10µF local decoupling capacitor is recommended for each phase PVIN. If long wires are used to bring power to the IC, use additional Bulk capacitors between C_{IN} and the battery/power supply to dampen ringing and overshoot at start-up.

Internal analog reference circuits also require additional filtering at the AVIN_FLT pin.

Table 7. Recommended Input Capacitors

Manufacturer	Part Number	Case Size	Value (µF)	Volt (V)	Input
TDK Corp	CGB2A1X5R1A105M033BC	0402	1	10	AVIN
Kemet	C0402C104K8RACTU	0402	0.1	10	AVIN
Samsung	CL05A10MP5NUNC	0402	10	10	PVIN
Murata	GRM188R61A106MAAL	0603	10	10	PVIN

5.4 ADC Telemetry

The ISL91302BIK has an internal SAR ADC that monitors and reports the die temperature, individual phase currents, total buck output current, output voltage, and input voltage. Two additional channels provide internal or external monitoring. Using these channels requires OTP programming from the factory. The ADC is OTP programmed to be turned off during Discontinuous Conduction mode to save current and improve light-load efficiency.

Reading the ADC output is accomplished by reading the respective MSB (8-bit) and LSB (8-bit). Table 8 shows which registers hold the ADC data.

Table 8. ADC Register Addresses

Monitor	Register Name	Register Address MSB	Register Address LSB
Temperature	SAMPLE0	0x16	0x17
Buck1 Ph1 Current	SAMPLE1PH1	0x18	0x19
Buck1 Ph2 Current	SAMPLE1PH2	0x1A	0x1B
Buck1 Ph3 Current	SAMPLE1PH3	0x1C	0x1D
Buck1 Ph4 Current	SAMPLE1PH4	0x1E	0x1F
Buck1 Total Current	SAMPLE1T	0x20	0x21
PVIN for Buck1	SAMPLE2	0x22	0x23
VOUT1	SAMPLE3	0x24	0x25
Buck2 Ph1 Current	SAMPLE4PH1	0x26	0x27
Buck2 Ph2 Current	SAMPLE4PH2	0x28	0x29
Buck2 Total Current	SAMPLE4T	0x2A	0x2B
PVIN for Buck2	SAMPLE5	0x2C	0x2D
VOUT2	SAMPLE6	0x2E	0x2F
AUX INPUT0	AUX0	0x30	0x31
AUX INPUT1	AUX1	0x32	0x33

The ADC 16-bit output is a signed format in which the LSB is 0.25 when referring to temperature, voltage, or individual phase current. The total buck current measurement has an LSB of 1. Each channel is filtered through an internally programmable IIR filter. AUX input 0 and AUX input 1 allow the user to read the external values with the ISL91302BIK ADC.

Table 9. ADC Result Registers

Units	Phase Current (mA)	Total Buck Current (mA)	Temperature (°C)	Voltage (mV)
0x0000	0	0	0	0
0x0001	0.25	1	0.25	0.25
0x0002	0.5	2	0.5	0.5
0x0003	0.75	3	0.75	0.75
0x0004	1	4	1	1
…				
0x0010	4	16	4	4
…				
0x0100	64	256	64	64
…				
0x7FFF	8191.75	32767	8191.75	8191.75
0x8000	-8192	-32768	-8192	-8192

Table 9. ADC Result Registers (Continued)

Units	Phase Current (mA)	Total Buck Current (mA)	Temperature (°C)	Voltage (mV)
0x8001	-8191.75	-32767	-8191.75	-8191.75
…				
0xFFFF	-0.25	-1	-0.25	-0.25

5.5 Dynamic Voltage Scaling (DVS)

The ISL91302BIK has several options to achieve DVS. Each buck controller has four independently programmable voltage settings to set the output voltage. The settings are DVS0, DVS1, DVS2, and DVS3. Changing the selected DVS number selects the corresponding output voltage. The two methods to select the DVS are:

Method 1) - Use internal registers to select DVS by writing to the BUCKx_DVSSELECT[1:0] bits in the BUCKx_DVSSEL register for each respective buck using SPI or I^2C.

To use this method, the BUCKx_DVSCTRL[0] bit has to be set to 0x0 for the corresponding buck. The BUCKxDVSSELECT[1:0] setting allows the user to switch between the four different DVS settings, each of which corresponds to a set of DVS registers holding the DVS information.

For example, DVS0 correponds to BUCKx_DVS0VOUT92[7:0] and BUCKx_DVS0VOUT10[1:0]. The two register values combined represent the complete 10-bit DAC code for DVS0.

Table 10. DVS Method Selection

BUCKx_DVSCTRL[0]	
0x0	Use BUCKx_DVSSELECT[1:0] to select active DVS configuration
0x1	Use DVS pin(s) to control DVS selection

Table 11. DVS Pointers

BUCKx_DVSSELECT[1:0]	Active DVS for BUCKx
0x0	DVS0
0x1	DVS1
0x2	DVS2
0x3	DVS3

Each output voltage is set writing a 10-bit word to DVS Configuration 1 (BUCKx_DVS0CFG1 register) and DVS Configuration 0 (BUCKx_DVS0CFG0 register) in each buck. Configuration 1 holds the eight most significant bits and Configuration 0 holds the last two bits of the 10-bit word. The output voltage does not change until the LSB register has been written. Table 12 shows the relationship between the DVS word and V_{OUT}.

Table 12. 10-Bit DVS Code to Voltage Translation

FBDIV	1.0	0.8	0.6
DAC [9:0]	V_{OUT} (V)	V_{OUT} (V)	V_{OUT} (V)
0x000	0.0000	0.0000	0.0000
0x001	0.0012	0.0015	0.0020
…			
0x200	0.6144	0.768	1.024
0x201	0.6156	0.7695	1.026
…			
0x3E8	1.2	1.5	2.0

Method 2) - Using GPIO/MPIO pins to achieve DVS, there are five variations depending on the IO_PINMODE register setting. See Table 2.

NOTE: To use DVS by GPIO/MPIO pins requires IO_PINMODE to be OTP programmed before a start-up boot sequence is initiated. On-the-fly programming is not recommended for the following configurations.

(i) IO_PINMODE = 0x3: SPI with two Independent Buck DVS pins

MPIO0	MPIO1	MPIO2	MPIO3	GPIO0	GPIO1
SCK	SS_B	MOSI	MISO	DVS1_0	DVS2_0

BUCKx_DVSCTRL[0] should be OTP programmed high before the start-up sequence. The active DVS follows the DVSx_0 pin logic for the respective buck. See Table 13 for more information.

Table 13. Single DVS Pin Logic

Function	
DVS1_0	**Active DVS for BUCK1**
0	DVS0
1	DVS1
DVS2_0	**Active DVS for BUCK2**
0	DVS0
1	DVS1

(ii) IO_PINMODE = 0x4: I^2C with Global DVS and PGOOD pins

MPIO0	MPIO1	MPIO2	MPIO3	GPIO0	GPIO1
DVS_PIN1	DVS_PIN0	PGOOD1	PGOOD2	SCL	SDA

BUCKx_DVSPIN_CTRL[1:0] bits in BUCKx_DVSCFG register in combination with the DVS_PIN1 and DVS_PIN2 sets the active DVS for the respective BUCK. See Table 14 for more information. BUCKx_DVSCTRL[0] should be OTP programmed high before the start-up sequence.

Table 14. Global DVS Pin Logic

BUCKx_DVSPIN_CTRL[1:0]	DVS_PIN1	DVS_PIN0	Active DVS
0x0	X	X	DVS0
0x1	X	0	DVS0
	X	1	DVS1
0x2	0	X	DVS0
	1	X	DVS2
0x3	0	0	DVS0
	0	1	DVS1
	1	0	DVS2
	1	1	DVS3

Note: The 'X' indicates that either a 0 or 1 is acceptable.

(iii) IO_PINMODE = 0x5: I²C with 2 DVS pins for Buck1 and 2 DVS pins for Buck2

MPIO0	MPIO1	MPIO2	MPIO3	GPIO0	GPIO1
DVS1_0	DVS1_1	DVS2_0	DVS2_1	SCL	SDA

The active DVS is selected based off the combined DVSx_1 and DVSx_2 input pin logic. See Table 15 for more information. BUCKx_DVSCTRL[0] should be OTP programmed high before the start-up sequence.

Table 15. Active DVS for 2 DVS Pins Configuration

DVSx_1	DVSx_0	Active DVS for BUCKx
0	0	DVS0
0	1	DVS1
1	0	DVS2
1	1	DVS3

(iv) IO_PINMODE = 0x6: I²C with 2 DVS pins and 2 PGOOD pins

MPIO0	MPIO1	MPIO2	MPIO3	GPIO0	GPIO1
DVS1_0	DVS2_0	PGOOD1	PGOOD2	SCL	SDA

BUCKx_DVSCTRL[0] should be OTP programmed high before the start-up sequence. DVS1_0 and DVS2_0 follows the same active DVS table as in IO_PINMODE = 0x3. See Table 13 for more information.

(v) IO_PINMODE = 0xE: I2C with 2 DVS pins and 2 AUX ADC pins

MPIO0	MPIO1	MPIO2	MPIO3	GPIO0	GPIO1
ADC_IN0	ADC_IN1	DVS_PIN1	DVS_PIN2	SCL	SDA

DVS_PIN0 and DVS_PIN1 behave the same as in IO_PINMODE = 0x4. See Table 14 for more information. BUCKx_DVSCTRL[0] should be OTP programmed high before the start-up sequence.

5.6 Configuring DVS Speed

5.6.1 Power-Up and Shutdown Slew Rate Setting

The BUCKx_RSPPUP[2:0] bits in the BUCKx_RSPCFG0 register set the slew rates (DVS speed) in BUCKx only during V_{OUTx} power-up. Similarly, the BUCKx_RSPPDN[2:0] in the BUCKx_RSPCFG0 register sets the slew rates in BUCKx during normal V_{OUTx} shutdown. The achievable slew rates varies with different FBDIV settings (Factory OTP programmed). For more details, see Register BUCK1_RSPCFG0.

5.6.2 DVS Transition Slew Rate Setting

BUCKx_RSPUP[2:0] and BUCKx_RSPDN[2:0] in the BUCKx_RSPCFG1 register sets the slew rates (DVS speed) in BUCKx during normal DVS transtion. The achievable slew rates varies with different FBDIV settings (factory OTP programmed). For more details, see Register BUCK1_RSPCFG1.

5.7 Output Voltage Setting

Each output voltage is set by writing a 10-bit word to DVS Configuration 1 (BUCKx_DVS0CFG1 register) and DVS Configuration 0 (BUCKx_DVS0CFG0 register) in each buck. Configuration 1 holds the MSB and Configuration 0 holds the last two bits of the 10-bit word. The output voltage does not change until the LSB register has been written. BUCK1_DVS0CFG1 shows the relationship between the DVS word and V_{OUT}.

5.8 Power Sequencing

When the master chip Enable (EN) pin is brought above an NMOS threshold, the ISL91302BIK powers up its key biasing circuits, loads the OTP configuration registers, and does one of two things based on the preprogrammed OTP setting:

1. **Manual buck start-up:**
   Program the internal IO_BUCKx_EN bits to 1 from I^{2}C/SPI to enable the respective buck. When IO_PINMODE = 0x1, the EN_A and EN_B pins can also be used to enable the respective bucks. If using IO_PINMODE = 0x1, the internal IO_BUCKx_EN bits should be set high in OTP. The slew rate of each buck during its soft-start is specified by the BUCKx_RSPPUP[2:0] bits.

Note: The programmable (1ms to 63ms) delay using BUCKx_EN_DLY[5:0] is not used for Manual Buck start-up.

2. **Auto Buck start-up from master chip enable pin:**
   Run a predetermined start-up sequence for the buck outputs as soon as BOOT is complete. The slew rate of each buck during its soft-start is specified in BUCKx_RSPPUP[2:0].

Note: The delay, BUCKx_EN_DLY[5:0] shown in Figure 24 as EN_dlyx, is programmable from 0 to 63ms in 1ms steps.

Figure 24 provides an example of power-up configurability. The master chip enable pin (EN) transitions from 0 to 1 and OTP is loaded over 1.4ms. After the initial 1.4ms boot interval, the buck output start-up sequence begins. In the Figure 24 example, BUCK1_EN_DLY is set for 0ms and BUCK2_EN_DLY is set for 1ms.

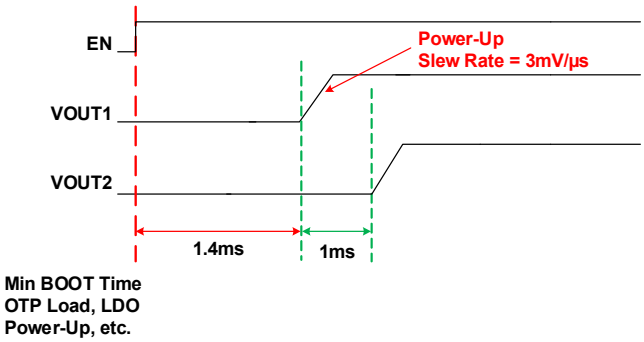


Figure 24. Master Chip Enable Power-Up Example

The buck outputs can also be programmed to execute a controlled shutdown in two ways:

1. **Manual buck power-down:**
   Program the internal IO_BUCKx_EN bit to 0 through I^{2}C/SPI or lower the Buck Enable pin (EN_A or EN_B when IO_PINMODE = 0x1). The manual method can be used to power down a specific buck (with a controlled slew rate) while keeping the rest of the chip alive.

Note: The programmable (0ms to 63ms) delay from BUCKx_SHUTDN_DLY[5:0] is not used for manual buck power-down.

2. **Auto Buck power-down from master chip enable pin:**
   When the master chip Enable pin (EN) is brought below the falling threshold of the comparator, the Bucks are ramped down at a controlled rate using preprogrammed delays. This is then followed by the power-down of the bias circuits forcing the chip into shutdown. The slew rate of each buck during its power-down (down to ~250mV) is specified in BUCKx_RSPPDN[2:0].

Note: The delay, BUCKx_ SHUTDN _DLY[5:0] shown in Figure 25 as Dis_dlyx, is programmable from 0 to 63ms in 1ms steps.

Figure 25 provides an example of power-down configurability. The master chip enable pin (EN) transitions from logic 1 to 0. In the Figure 25 example, BUCK1_SHUTDN_DLY is set for 1ms and BUCK2_SHUTDN_DLY is set for 2ms.

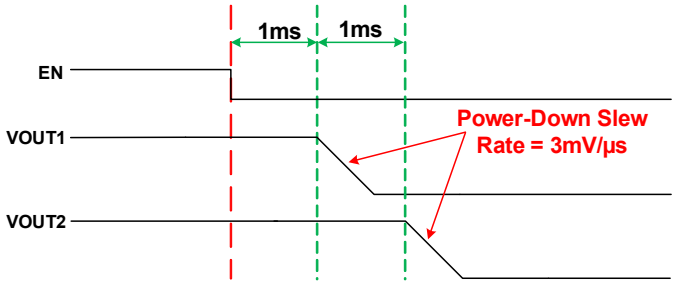


Figure 25. Auto Chip Power-Down Example

The actual slew rate that each buck ramps down to is specified by the register BUCKx_RSPSHUTDN. This slew rate is controlled until the output voltage is ~250mV, at which point the ISL91302BIK engages a weak resistive pull-down (if enabled by factory OTP) that can keep V_{OUT} = 0V when the buck is not enabled. Figure 26 shows an example of the weak pull-down behavior.

• **Option 1:** If the disable event for a buck output is the master chip enable pin (EN) falling below its logic low threshold, then when the output falls below 250mV, the output voltage decay is dictated by the system load passively discharging the buck output capacitance. PULL_DOWN_DISCHARGE IO_MPIO_DATA[4] bit per the IO_MPIO_DATA register is **not** used in this method.

• **Option 2:** If the disable event for a buck output is the master chip enable pin (EN) remaining high and the enable register bit (IO_BUCKx_EN) transitioning from a logic 1 to a logic 0, then PULL_DOWN_DISCHARGE IO_MPIO_DATA[4] bit per the IO_MPIO_DATA register is used enabling an internal weak pull down.

Note: The weak pull-down can be disabled (using factory OTP).

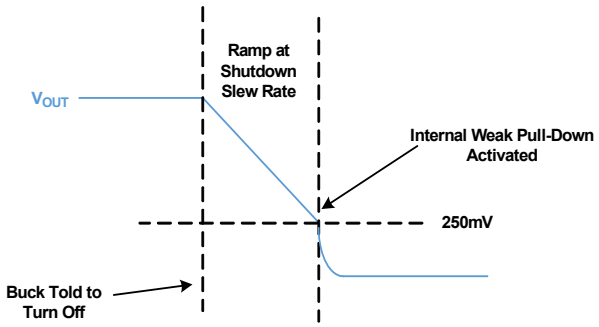


Figure 26. Buck Disable Waveform

5.9 Watchdog Time (WDOG_RST Pin)

The ISL91302BIK implements a watchdog function which allows the output voltages to return to a safe default when communication to the processor host is lost. This is determined by monitoring the state of the WDOG_RST pin. If the pin goes into the failure state for a duration greater than the programmed debounce time, the default voltages from OTP are restored.

Both bucks respond to the WDOG_RST pin. The polarity of the WDOG_RST pin is active low.

Table 16. WDOG_RST Function

Action	
At Boot Up	DVS registers are loaded with values stored in OTP.
After Debounce Time	Restore selected output voltages to their original values stored in OTP (DVS0), and slew the buck outputs to that voltage.

Total recovery time for the buck is the sum of the t_{SLEW} and $t_{DEBOUNCE}$. The target voltage WDOG_RST pin resets the ISL91302BIK buck output(s), set by DVS0, which reside in the BUCKx_DVS0CFG1 and BUCKx_DVS0CFG0 registers.

t_{SLEW} is determined by the default output voltage divided by 3mV/µs, while $t_{DEBOUNCE}$ is set at 10ms. $t_{DEBOUNCE}$ is factory programmable.

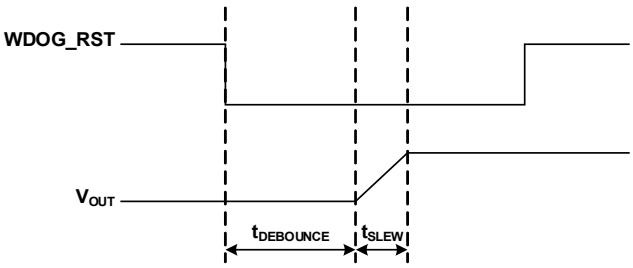


Figure 27. Watchdog Timer Example Case

5.10 Interrupt Pin

The ISL91302BIK can alert the host when a warning or a fault has occurred through an IRQ interrupt request signal with configurable masking options that is connected to a configurable interrupt (INT) pin. The interrupt pin can be programmed to be active high, active low, an open drain, or a CMOS output.

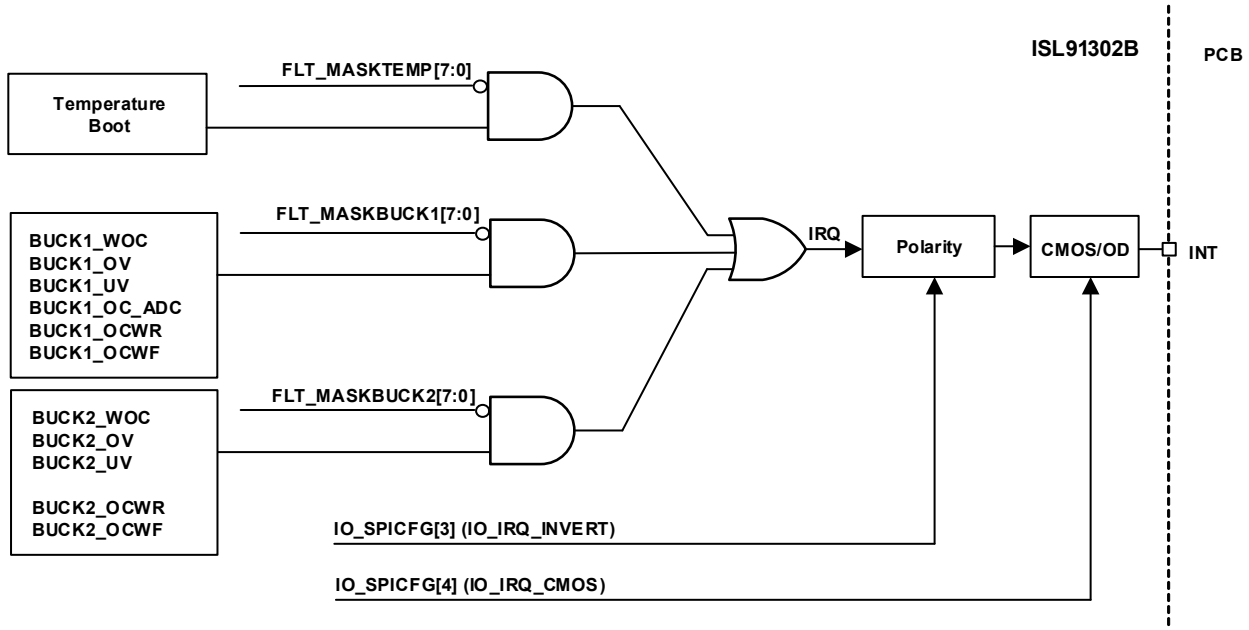


Figure 28. Interrupt Tree

6. Protection Features (Faults)

The ISL91302BIK has integrated Overcurrent (OC), Overvoltage (OV), Undervoltage (UV), and Over-Temperature (OT) protection features.

6.1 Over-Temperature Protection

The ISL91302BIK provides protection against over-temperature conditions. An over-temperature protection circuit continuously monitors the die temperature of the chip and raises a fault when the temperature exceeds a predefined limit programmed by Register FLT_TEMPSHUTDN. The ISL91302BIK also contains a programmable thermal warning threshold set by Register FLT_TEMPWARN. Programmable Hysteresis enables the circuit to clear the fault or warning once the temperature is below a user-defined safe temperature. The warning and shutdown hysteresis level are factory programmable. Contact Renesas support for custom settings. The over-temperature protection is disabled if all bucks are operating in PFM mode or in the off state.

6.2 Overcurrent Protection Mode

The ISL91302BIK has implemented a comparator-based OCP and an ADC-based OCP mechanism. The comparator based OCP or 'WOC' block has a current comparator, which compares the load current through the high-side power FET with the reference current level through a replica device. If the sensed FET current is higher than the WOC threshold, the WOC is triggered immediately, preventing a catastrophic condition. The WOC disables the buck and latches the power-stage into tri-state until the fault is cleared. The WOC fault is self-cleared when the OC condition is removed and the buck attempts to re-enable in a hiccup type fashion. The ADC based OCP monitors the averaged high-side and low-side MOSFET current for each phase and is slower but more accurate than the comparator based WOC. If the Buck total current is higher than the ADC based OCP threshold, the ADC OCP is triggered, which shutdowns the Buck and latches the power-stage into tri-state. ADC based OCP can only be cleared by recycling the PVIN/AVIN or by toggling the EN pin. Please note the ADC based OC cannot be cleared by toggling the IO_BUCKx_EN bit by I^2C/SPI.

Overcurrent protection can be enabled or disabled using the fault register setting in FLT_BUCKx_CTRL. ADC based current warning and shutdown limits can be adjusted with the FLT_BUCKx_ISENSEWARN and FLT_BUCKx_ISENSESHUTDN registers, respectively.

6.3 Overvoltage (OV)/Undervoltage (UV) Protection

The ISL91302BIK protects against output overvoltage and undervoltage fault conditions. The OV/UV protection circuitry has low power comparators configured with differential input and single-ended outputs capable of working over large common-mode input ranges. This comparator is used to monitor the output voltage in both DCM and CCM for faults. By default, when an OV/UV event is triggered, the buck converter is shut down until the fault is cleared. Fault control register FLT_BUCKx_CTRL is used to enable or disable the functionality. The OV/UV limits are adjustable using the BUCKx_UVOVTH[1:0] bits in the BUCKx_PROTCFG register. See Table 17 for more details.

Table 17. OV/UV Protection Thresholds

BUCKxUVOVTH[1:0]	OV/UV Threshold
0x0	±150mV around DAC target
0x1	±200mV around DAC target
0x2	±250mV around DAC target
0x3	±300mV around DAC target

7. Serial Communication Interface

The ISL91302BIK has two serial interface protocols to read/write the registers.

- SPI
- I^2C

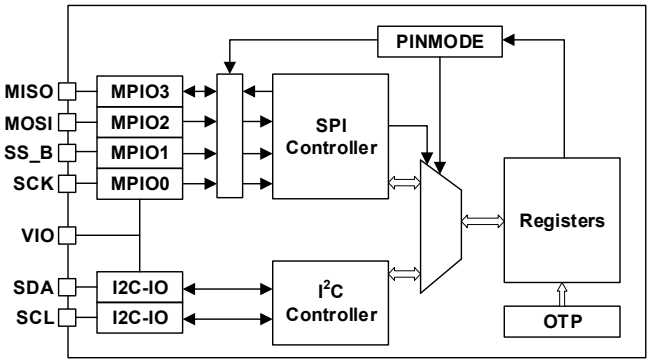


Figure 29. SPI and I^2C Interface Block Diagram

The arbitration of the register access bus between SPI and I^2C is determined by the pad MPIO1 when using IO_PINMODE = 0x0, as shown in Table 18:

Table 18. SPI/I^2C Register Access

Register IO_PINMODE	Pad MPIO_1 (SS_B)	Register Access
0	0	SPI (Read/Write Access (Note 11))
	1	I^2C (Note 12)

Notes:

11. When the device is configured for SPI access, the I^2C should not be addressed with the device ID.
12. When the device is configured for I^2C access, in PINMODE 0, the SS_B line must be held high.

After switching from SPI to I^2C or from I^2C to SPI, there is a minimum of 50ns wait time is required before starting a transaction.

7.1 SPI Serial Interface

The SPI interface is a general specification four-wire slave interface capable of operating at a clock speed of up to 26MHz. It is based on byte transfers.

7.1.1 SPI Data Protocol

Both Read and Write SPI transactions begin when SS_B goes low and end when SS_B goes high.

7.1.1.1 Write Operation

To write to the ISL91302BIK, the master (controller) needs to drive SS_B low and send the Control Byte, followed by the register address, packet length (if IO_SPIMODE = 1), Data bytes to be written, and finally drive SS_B high to terminate the transaction as shown below. The MSB of the Control byte is the R/W bit, which needs to be set to ‘write’ operation (see IO_SPIRWPOL). Bit 6, AI indicates if it is going to be a single-byte write operation or a multi-byte write. Bits 1 and 0 of the Control byte, indicate the page number of the register location desired to be written (MSBs of the register address). The register address byte is the 8-bit address of the register within the page specified by Page[1:0] bits. If IO_SPIMODE = 1, the register address needs to be followed by 8-bit packet length, which indicates the number of bytes to be written. Following the packet length field, the master needs to send the data bytes. When all eight bits of data are received, they get written to the specified register address and the ISL91302BIK increments the register address.

In single byte transactions, (AI = 0 or Packet length = 1), the ISL91302BIK goes into wait state and waits for SS_B to go high.

In multi-byte transactions with IO_SPIMODE = 1, the ISL91302BIK writes the subsequently received data bytes to sequentially incrementing addresses until the number of bytes, as specified by ‘packet length’, are received and then go into the wait state and wait for SS_B to go high. For multi-byte transactions with IO_SPIMODE = 0 and AI = 1, the ISL91302BIK keeps writing the subsequently received data bytes to sequentially incrementing addresses until SS_B goes high. If SS_B goes high in the middle of a transaction, the transaction is terminated. The data byte is written if all eight bits are received.

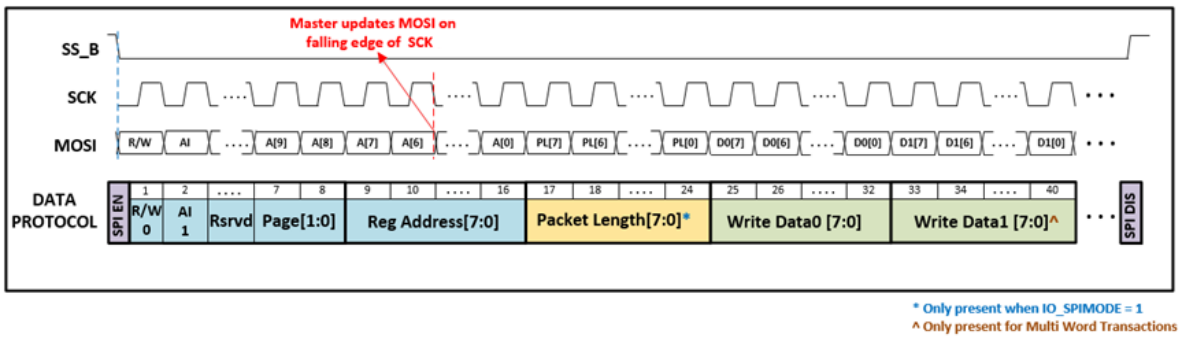


Figure 30. SPI Write Transaction with IO_SPIMODE = 1; IO_SPICPOL = 0; IO_SPICPHA = 0

7.1.1.2 Read Operation

To read from the ISL91302BIK, the master (controller) needs to drive SS_B low and then send the Control Byte, followed by register address, packet length (if IO_SPIMODE = 1). The ISL91302BIK then sends the data bytes from the requested registers and finally the master drives SS_B high to terminate the transaction. The MSB of the Control byte is the R/W bit which needs to be set to ‘read’ operation (see IO_SPIRWPOL). Bit 6, AI indicates if it is going to be a single-byte read operation or a multi-byte read. Bits 1 and 0 of the Control byte indicate the page number of the register location be read (MSBs of the register address). The register address byte is the 8-bit address of the register within the page specified by Page[1:0] bits. If IO_SPIMODE = 1, the register address needs to be followed by an 8-bit packet length, which indicates the number of bytes to be written. Following the packet length field, the ISL91302BIK sends the data from the requested register. When all eight bits of data from the requested register address are sent, the ISL91302BIK increments the register address.

In a single-byte transaction, (AI = 0 or Packet length = 1), the ISL91302BIK goes into a wait state and waits for SS_B to go high.

In a multi-byte transaction with IO_SPIMODE = 1, the ISL91302BIK sends the data bytes from sequentially incrementing addresses until the number of bytes as specified by ‘packet length’ are sent and then goes into a wait state and waits for SS_B to go high. For multi-byte transactions with IO_SPIMODE = 0 and AI = 1, the ISL91302BIK keeps sending data bytes from sequentially incrementing addresses until SS_B goes high.

Note: The MISO pin is pulled low while SS_B is high.

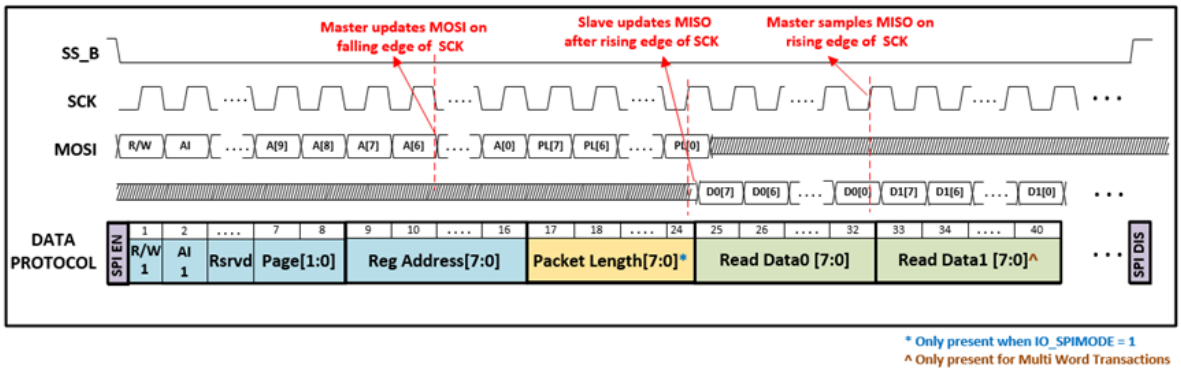


Figure 31. SPI Read Transaction with IO_SPIMODE = 1; IO_SPICPOL = 0; IO_SPICPHA = 0

R/W	Read/Write Bit Indicating Read or Write Operation
AI	Auto Increment. 1 indicates multi-byte transfer, 0 indicates single byte transfer
Page	2-bit page address of the register to be written/read
Address	8-bit register address of the register to be written/read
Packet Length	8-bit packet length indicating number of data bytes to be transferred. Overrides AI when IO_SPIMODE = 1
Read Data	Data in the register at address, Address [7:0] + n
Write Data	Data to be written to the register at address, Address [7:0] + n

7.1.2 SPI Configuration

The following register bits configure the SPI operation:

- **IO_SPICPOL:** SPI clock polarity, ISL91302BIK is configured as active high, IO_SPICPOL = 0
- **IO_SPICPHA:** SPI clock phase, ISL91302BIK samples data on rising edge of SPI clock, IO_SPICPHA = 0

The four possible modes of clocking are shown in Figure 32.

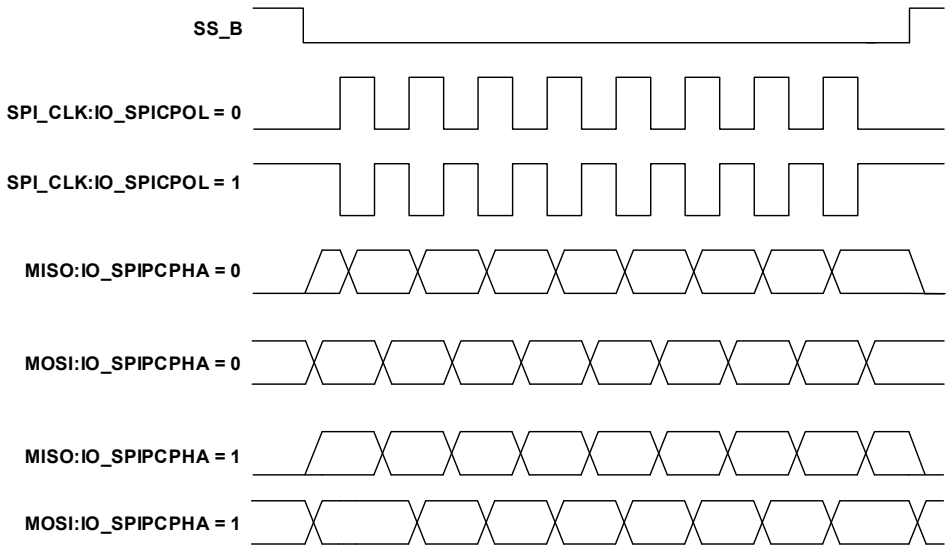


Figure 32. Four Possible Clocking Modes

- **IO_SPIRWPOL**: R/W bit polarity, ISL91302BIK SPI_RWPOL is set to 0, 1: Read, 0: Write.

SPI_RWPOL	R/W	Operation
0	0	Write
0	1	Read

- **IO_SPIMODE**: Packet length enable, the ISL91302BIK uses packet length mode by default, meaning the third data byte from master is the packet length and indicates the total number of data words to be sent/received in a burst transaction.

7.1.3 SPI Timing

Figure 33 shows SPI timing for IO_SPICPOL = 0; IO_SPICPHA = 0. The timing values in Tables 19 hold true for other values of IO_SPICPOL, IO_SPICHPA as well.

Table 19. Timing Values

Parameter	Symbol	Min	Max	Units
Clock Period	t_1	38.4		ns
Enable Lead Time	t_2	12		ns
Enable Lag Time	t_3	12		ns
Clock High or Low Time	t_4	15		ns
Data Setup Time (Input)	t_5	12		ns
Data Hold Time (Input)	t_6	10		ns
Time MISO is Stable before the Next Rising Edge of CLK	t_7	5		ns
Data Held after Clock Edge (Output)	t_8	5		ns
Load Capacitance	C_L		10	pF

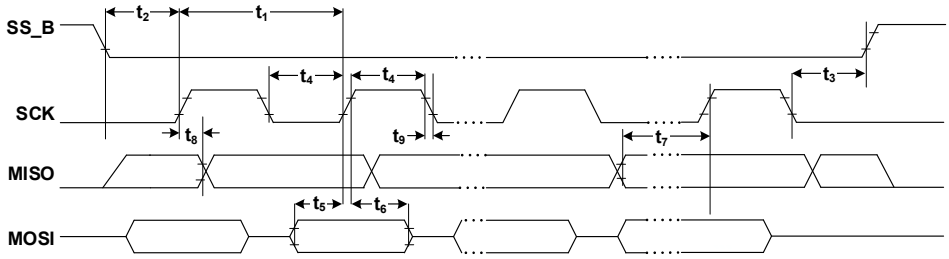


Figure 33. SPI Timing for IO_SPICPHA = 0, IO_SPICPOL = 0

7.2 I²C Interface

The I²C interface is a simple, bidirectional 2-wire bus protocol, consisting of the Serial Clock Control (SCL/I2C_CLK) and the Serial Data Signal (SDA/I2C_SDA). The ISL91302BIK hosts a slave I²C interface that supports data speeds up to 3.4Mbps. SCL is an input to the ISL91302BIK and is supplied by the controller, whereas SDA is bidirectional. The ISL91302BIK has an open-drain output to transmit data on SDA. An external pull-up resistor must be placed on the serial data line to pull the drain output high during data transmission.

The ISL91302BIK uses a 7-bit hardware address scheme. The default address is set to 0x1D by a one-time programmable fuse.

7.2.1 I²C Bus Operation

The chip supports 7-bit addressing. The ISL91302BIK I²C device address is reconfigurable through the OTP.

All communication over the I²C interface is conducted by sending the MSB of each byte of data first. Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 38).

All I²C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL91302BIK continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met. All I²C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH.

An Acknowledge (or ACK), is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (Figure 38). The ISL91302BIK responds with an ACK after recognition of a START condition, followed by a valid Identification (also known as I²C Address) Byte. The ISL91302BIK also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

7.2.1.1 Write Operation

A Write operation requires a START condition, followed by an ISL91302BIK I^{2}C Address byte with the R/W bit set to 0, a Register Address Byte, Data Bytes, and a STOP condition. After each byte, the ISL91302BIK responds with an ACK. After every data byte, the ISL91302BIK auto increments the register address so subsequent data bytes get written to sequentially incremental register locations. A STOP condition that terminates the write operation must be sent by the master after sending at least one full data byte and its associated ACK signal. If a STOP byte is issued in the middle of a data byte, then the write is not performed.

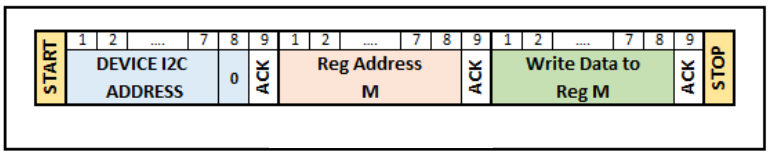


Figure 34. 1-Byte Write to Register M

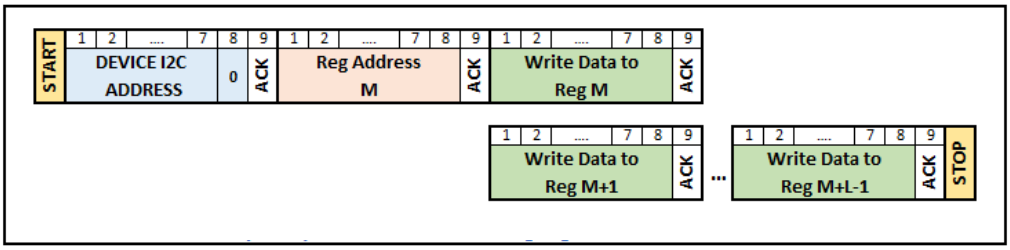


Figure 35. L-Byte Sequential Data Write Starting Register M

7.2.1.2 Read Operation

A Read operation consists of a three-byte dummy write instruction to send the register address to begin reading from, followed by a Current Address Read operation. The master initiates the operation, issuing the following sequence: a START condition, followed by an ISL91302BIK I^{2}C Address byte with the R/W bit set to 0, a Register Address Byte, a second START, and a second ISL91302BIK I^{2}C Address byte with the R/W bit set to 1. After each of the three bytes, the ISL91302BIK responds with an ACK. The ISL91302BIK then transmits Data Bytes. The master terminates the Read operation from the ISL91302BIK by issuing a STOP condition following the last bit of the last data byte. After every data byte, the ISL91302BIK auto increments the register address so subsequent data bytes are sent from sequentially incremental register locations.

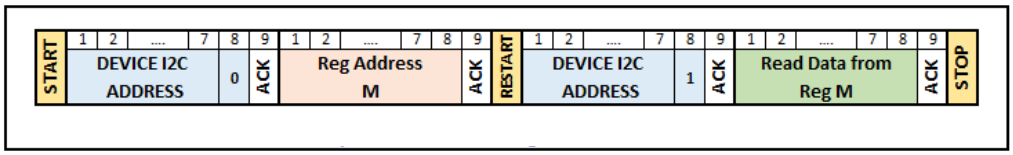


Figure 36. 1-Byte Data Read from Register M

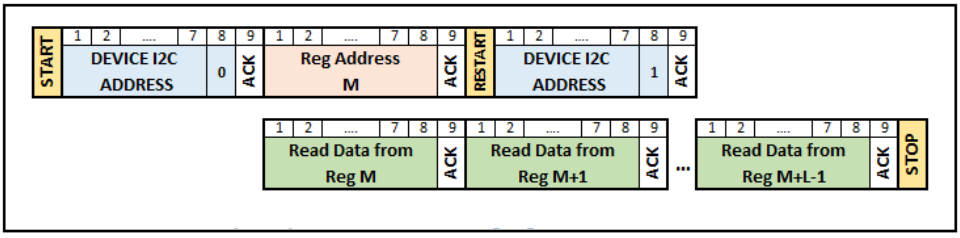


Figure 37. L-Byte Sequential Data Read Starting Register M

7.2.2 I²C Timing

The timing specifications of the I²C I/O from the I²C spec are shown in Figure 38 and Table 20. The I²C controller provides a slave I²C transceiver capable of interpreting I²C protocol in Standard, Fast, Fast+, and High Speed modes.

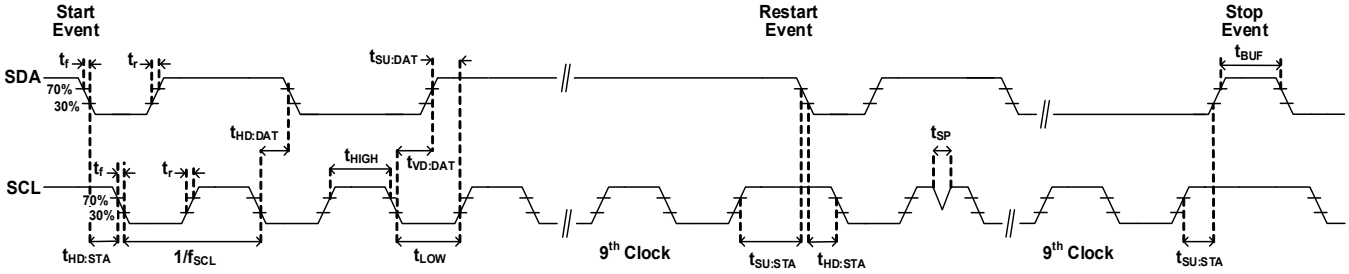


Figure 38. I²C Timing

Table 20. I²C Specification

Parameter	Symbol	Standard Mode		Fast Mode		Fast Mode Plus		High Speed Mode		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Clock Frequency	f_{SCL}	0	100	0	400	0	1000	0	3400	kHz
Hold Time (repeated) START Condition. (After this period, the first clock pulse is generated.)	$t_{HD;STA}$	4000	-	600	-	260	-	160	-	ns
LOW Period of the SCL Clock	t_{LOW}	4700	-	1300	-	500	-	160	-	ns
HIGH Period of the SCL Clock	t_{HIGH}	4000	-	600	-	260	-	60	-	ns
Setup Time for a Repeated START Condition	$t_{SU;STA}$	4700	-	600	-	260	-	160	-	ns
Data Hold Time	$t_{HD;DAT}$	15	-	15	-	15	-	15	70	ns
Data Setup Time	$t_{SU;DAT}$	250	-	100	-	50	-	10	-	ns
Rise Time of SCL	t_{rCL}	-	1000	-	300	-	120	-	40	ns
Fall Time of SCL	t_{fCL}	-	300	-	300	-	120	-	40	ns
Rise Time of SDA	t_{rDA}	-	1000	20	300	-	120	10 Note 14	80	ns
Fall Time of SDA	t_{fDA}	-	300	20 × (V_{DD}/5.5V) Note 13	300	20 × (V_{DD}/5.5V) Note 13	120	10 Note 14	80	ns
Setup Time for STOP Condition	$t_{SU;STO}$	4000	-	600	-	260	-	160	-	ns
Bus Free Time between a STOP and START Condition	t_{BUF}	4700	-	1300	-	500	-	-	-	ns
Capacitive Load for each Bus Line	C_b	-	400	-	400	-	400		100	pF
Output Fall Time from VIHmin to VILmax	t_{of}	-	250[5]	20 × (V_{DD} /5.5V)[6]	250[5]	20 × (V_{DD}/5.5V)[6]	120[7]	10 Note 14	80	ns
Pulse Width of Spikes Suppressed by the Input Filter	t_{SP}	-	-	0	50	0	50	0	10	ns

Notes:

13. Valid only for V_{DD} < 4V.
14. Valid only for V_{DD} < 1.9V.
15. V_{DD} is the pull-up source to the I²C lines (GPIO0, GPIO1).

8. Board Layout Recommendations

The ISL91302BIK is a high frequency multiphase switching regulator and the proper PCB layout is an important design practice to ensure a satisfactory performance. The power loop is composed of the output inductor L, the output capacitor C_{OUT}, the PH pin, and the PGND pin. It is important to make the power loop as small as possible and the connecting traces among them should be direct, short, and wide. The same practice should be applied to the connections of the PVIN pin, the input capacitor, and PGND. The switching node of the converter, the PH pin, and the traces connected to this node are very noisy, so keep the VOUT and RTN lines and other noise sensitive traces away from these traces. Place the input capacitors as close as possible to the PVIN(s) and PGND(s) pins. Connect the ground of the input and output capacitors as close as possible as well. In addition, a solid ground plane is helpful for a good EMI performance.

Inductor placement should also be as close to the phase pins as possible. Using wide traces and reducing the length helps to improve the overall efficiency and reduce the amount of radiated EMI. For the phase traces, Renesas recommends only descending one layer to reduce the effective path to the inductor. Ensure the length and width of each inductor trace and number of microvias used match to help ensure proper current sharing between phases.

Place an AVIN filter capacitor as close as possible to the AVIN_FILT pin but away from noise sources. Always reference the GND pad of the decoupling capacitor to a quiet GND plane.

Do not use plated through-holes when passing the BGA pins to lower layers. Renesas recommends to using microvias that are staggered if they are required to pass down multiple layers.

The VOUT and RTN lines are used to sense the output voltage and should be routed directly to the load. Connecting the RTN line to ground away from the load causes a ground error in the output voltage load regulation due to parasitic ground resistance. Keep these traces away from switching nodes, which could be a converter phase node or high-speed digital signals. The use of small low inductance capacitors at the load improves noise immunity and transient response to the ISL91302BIK.

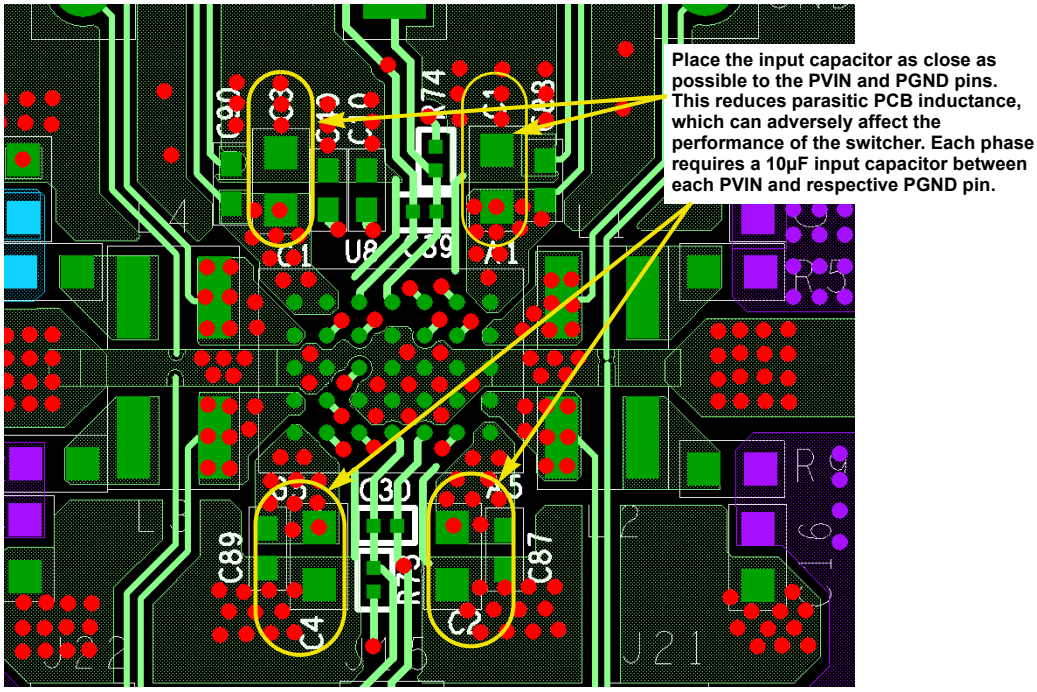


Figure 39. Recommended PCB Layout Top Layer

Provide a solid ground plane in the adjacent layer to provide a low impedance path to support high current flow. Copper planes need to be parallel with the phase traces on the top layer to minimize resistance, and they must be surrounded by a GND plane to prevent noise coupling.

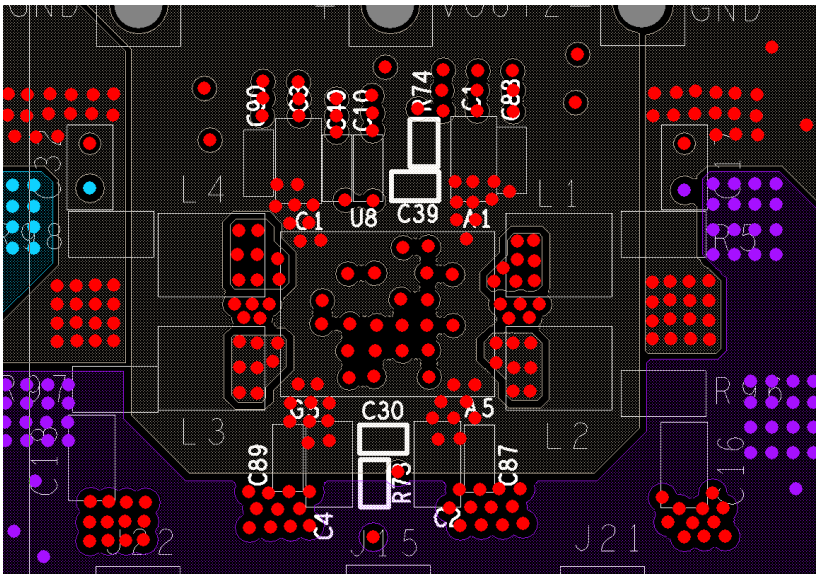


Figure 40. Recommended PCB Layout Second Layer

Feedback lines must be kept away from noise sources such as the switching node, inductor, and high-speed digital signals. Run the traces to cut through the surrounding ground plane areas to minimize noise pick up. Add ground planes above and below the signals when applicable.

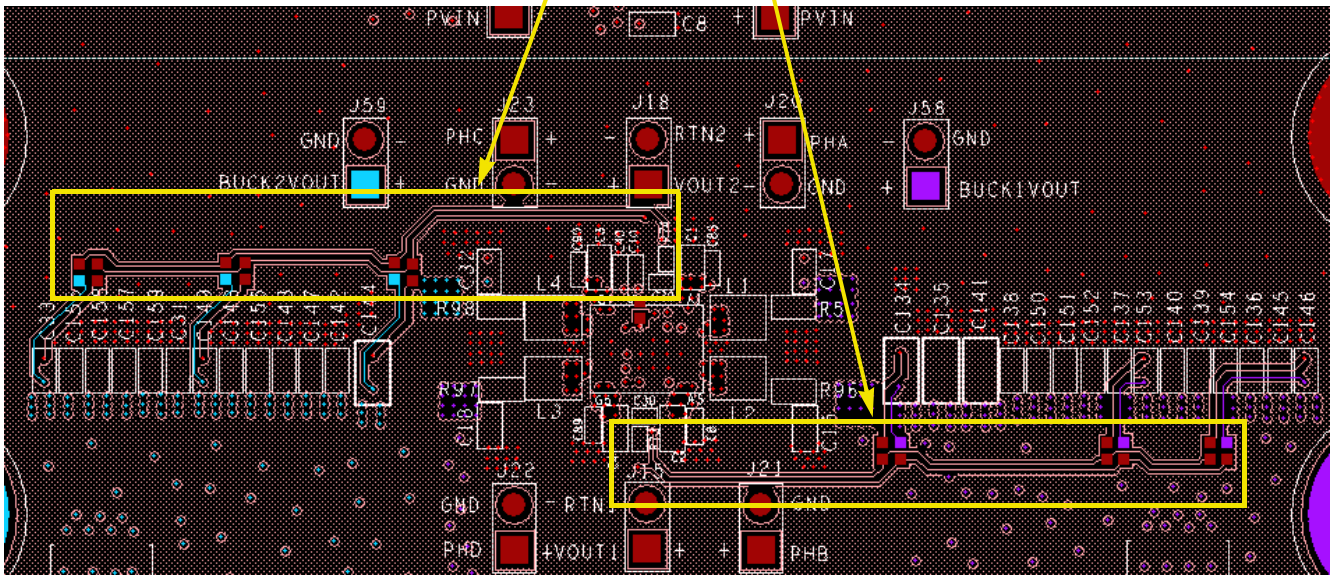


Figure 41. Recommended PCB Layout Bottom Layer

8.1 PCB Layout Summary

1. Place input capacitors as close as possible to their respective PVIN and PGND pins.
2. Route phase nodes with short, wide traces, and avoid any sensitive nodes.
3. Route VOUT and RTN lines differentially to the load and use small low ESL capacitors at the load for bypassing.
4. Output capacitors should be close to the inductors and have a low impedance path to the PGND pins.
5. Keep digital and phase nodes from intersecting AVIN_FILT, VOUT, and RTN lines on adjacent layers.

8.2 PCB Design for TFBGA Recommendations

Design Feature	Design Specification
Cu Pad Diameter	0.8mm pitch: 0.215 ±0.012mm
Microvia Structure	All microvias should be copper filled.
Microvia Stacking	Avoid microvia stacking if possible. Use staggered vias instead. If microvia stacking is absolutely necessary for the layout, the maximum number of recommended via stacks is two.
Plated Through-Hole (PTH) Location	No PTH should be placed under the BGA ball pads. Microvias and trace routing should be used to fan the PTH away from the BGA ball array.

9. Register Address Map

When communicating with registers that contain reserved bits, it is recommended to do a masked write/read to avoid modifying sensitive register values.

Address	Register	Address	Register	Address	Register
0x01	IO_CHIPNAME	0x2A	ADC_SAMPLE4TMSB	0x77	BUCK1_DVS2CFG0
0x13	FLT_RECORDTEMP	0x2B	ADC_SAMPLE4TLSB	0x78	BUCK1_DVS3CFG1
0x14	FLT_RECORDBUCK1	0x2C	ADC_SAMPLE5MSB	0x79	BUCK1_DVS3CFG0
0x15	FLT_RECORDBUCK2	0x2D	ADC_SAMPLE5LSB	0x7D	BUCK1_DVSSEL
0x16	ADC_SAMPLE0MSB	0x2E	ADC_SAMPLE6MSB	0x7E	BUCK1_RSPCFG1
0x17	ADC_SAMPLE0LSB	0x2F	ADC_SAMPLE6LSB	0x7F	BUCK1_RSPCFG0
0x18	ADC_SAMPLE1PH1MSB	0x30	ADC_AUX0MSB	0x80	BUCK1_EN_DLY
0x19	ADC_SAMPLE1PH1LSB	0x31	ADC_AUX0LSB	0x81	BUCK1_SHUTDN_DLY
0x1A	ADC_SAMPLE1PH2MSB	0x32	ADC_AUX1MSB	0x82	BUCK2_EA2
0x1B	ADC_SAMPLE1PH2LSB	0x33	ADC_AUX1LSB	0x85	BUCK2_DCM
0x1C	ADC_SAMPLE1PH3MSB	0043	IO_SPICFG	0x8E	BUCK2_DVS0CFG1
0x1D	ADC_SAMPLE1PH3LSB	0x44	IO_MODECTRL	0x8F	BUCK2_DVS0CFG0
0x1E	ADC_SAMPLE1PH4MSB	0x58	FLT_TEMPWARN	0x90	BUCK2_DVS1CFG1
0x1F	ADC_SAMPLE1PH4LSB	0x59	FLT_TEMPSHUTDN	0x91	BUCK2_DVS1CFG0
0x20	ADC_SAMPLE1TMSB	0x60	FLT_MASKTEMP	0x92	BUCK2_DVS2CFG1
0x21	ADC_SAMPLE1TLSB	0x61	FLT_MASKBUCK1	0x93	BUCK2_DVS2CFG0
0x22	ADC_SAMPLE2MSB	0x62	FLT_MASKBUCK2	0x94	BUCK2_DVS3CFG1
0x23	ADC_SAMPLE2LSB	0x66	BUCK1_EA2	0x95	BUCK2_DVS3CFG0
0x24	ADC_SAMPLE3MSB	0x69	BUCK1_DCM	0x99	BUCK2_DVSSEL
0x25	ADC_SAMPLE3LSB	0x72	BUCK1_DVS0CFG1	0x9A	BUCK2_RSPCFG1
0x26	ADC_SAMPLE4PH1MSB	0x73	BUCK1_DVS0CFG0	0x9B	BUCK2_RSPCFG0
0x27	ADC_SAMPLE4PH1LSB	0x74	BUCK1_DVS1CFG1	0x9C	BUCK2_EN_DLY
0x28	ADC_SAMPLE4PH2MSB	0x75	BUCK1_DVS1CFG0	0x9D	BUCK2_SHUTDN_DLY
0x29	ADC_SAMPLE4PH2LSB	0x76	BUCK1_DVS2CFG1		

Note: The registers not listed in the register map and RESERVED bits in the register map are reserved for factory use only. Changing these registers/bits can result in unexpected operation.

10. Register Description by Address

Address	Bit	Name	R/W	Default	Description
IO_CHIPNAME					
0x01	7:0	IO_CHIPNAME	R	0x02	Chip Name, Set by Renesas 0x02: ISL91302BIK, dual/single output PMIC
FLT_RECORDTEMP					
0x13	7	FLT_BOOT	R	0x0	BOOT Occurred Read only, cleared when read 0x0: No boot process has occurred since the last time this register was read. 0x1: Boot process has occurred (set high after OTP read is finished).
	6:4	Reserved	R	0x0	Reserved
	3	FLT_TEMPSDR	R	0x0	Over-Temperature (OT) Shutdown (Rising Threshold) Read only, cleared when read 0x0: No fault, less than threshold. 0x1: Fault, greater than threshold.
	2	FLT_TEMPWARNR	R	0x0	Over-Temperature (OT) Warning (Rising Threshold) Read only, cleared when read 0x0: No fault, less than threshold. 0x1: Fault, greater than threshold.
	1	FLT_TEMPWARNF	R	0x0	Over-Temperature (OT) Warning (Falling Threshold) (Warning1 Hysteresis) Read only, cleared when read 0x0: No fault, less than threshold. 0x1: Fault, greater than threshold.
	0	FLT_TEMPSDF	R	0x0	Over-Temperature (OT) Shutdown (Falling Edge) (Shutdown Hysteresis) Read only, cleared when read 0x0: No fault, less than threshold. 0x1: Fault, greater than threshold.

Address	Bit	Name	R/W	Default	Description
FLT_RECORDBUCK1					
0x14	7	Reserved	R	0x0	Reserved
	6	FLT_BUCK1_WOC	R	0x0	Way Overcurrent (WOC) for Buck1 Read only, cleared when read 0x0: No fault, less than threshold. 0x1: Fault, greater than threshold.
	5	FLT_BUCK1_OV	R	0x0	Overvoltage (OV) Read only, cleared when read 0x0: No fault, less than threshold. 0x1: Fault, greater than threshold.
	4	FLT_BUCK1_UV	R	0x0	Undervoltage (UV) Read only, cleared when read 0x0: No fault, greater than threshold. 0x1: Fault, less than threshold
	3	FLT_BUCK1_OCSDR	R	0x0	Overcurrent (OC) Shutdown (Rising Threshold) for Buck1 Read only, cleared when read 0x0: No fault, less than threshold. 0x1: Fault, greater than threshold.
	2	FLT_BUCK1_OCWR	R	0x0	Overcurrent (OC) Warning (Rising Threshold) for Buck1 Read only, cleared when read 0x0: No fault, less than threshold. 0x1: Fault, greater than threshold.
	1	FLT_BUCK1_OCWF	R	0x0	Overcurrent (OC) Warning (Falling Threshold) Buck1 Read only, cleared when read 0x0: No fault, less than threshold. 0x1: Fault, greater than threshold.
	0	Reserved	R	0x0	Reserved
FLT_RECORDBUCK2					
0x15	7	Reserved	R	0x0	See FLT_RECORDBUCK1
	6	FLT_BUCK2_WOC	R	0x0	
	5	FLT_BUCK2_OV	R	0x0	
	4	FLT_BUCK2_UV	R	0x0	
	3	FLT_BUCK2_OCSDR	R	0x0	
	2	FLT_BUCK2_OCWR	R	0x0	
	1	FLT_BUCK2_OCWF	R	0x0	
	0	Reserved	R	0x0	

<table>
<tr><th>Address</th><th>Bit</th><th>Name</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td colspan="6">ADC_SAMPLE0MSB</td></tr>
<tr><td>0x16</td><td>7:0</td><td>ADC_SAMPLE0MSB</td><td>R</td><td></td><td>
<table>
<tr><td colspan="2">Upper Byte of Temperature Sample
(combine with LSB for 16-bit value.)</td></tr>
<tr><td>Source</td><td>Temp. Sensor</td></tr>
<tr><td>Range</td><td>±200 °C</td></tr>
<tr><td>Format</td><td>s.13.2</td></tr>
<tr><td>Units</td><td>Temperature °C</td></tr>
<tr><td>0x0000</td><td>0</td></tr>
<tr><td>0x0001</td><td>0.25</td></tr>
<tr><td>0x0002</td><td>0.5</td></tr>
<tr><td>0x0003</td><td>0.75</td></tr>
<tr><td>0x0004</td><td>1</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0x0010</td><td>4</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0x0100</td><td>64</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0x0320</td><td>200</td></tr>
<tr><td>0xFCE0</td><td>-200</td></tr>
<tr><td>0xFCDF</td><td>-219.75</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0xFFFF</td><td>-0.25</td></tr>
</table>
</td></tr>
<tr><td colspan="6">ADC_SAMPLE0LSB</td></tr>
<tr><td>0x17</td><td>7:0</td><td>ADC_SAMPLE0LSB</td><td>R</td><td></td><td>Lower Byte of Temperature Sample (combine with MSB for 16-bit value)
See “ADC_SAMPLE0MSB” for decode.</td></tr>
</table>

<table>
<tr><th>Address</th><th>Bit</th><th>Name</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td colspan="6">ADC_SAMPLE1PH1MSB</td></tr>
<tr><td>0x18</td><td>7:0</td><td>ADC_SAMPLE1PH1MSB</td><td>R</td><td></td><td>
<table>
<tr><td colspan="2">Upper Byte of Buck1, Phase1 Output Current
(combine with LSB for 16-bit value.)</td></tr>
<tr><td>Source</td><td>I_{SENSE}</td></tr>
<tr><td>Range</td><td>±8.192A</td></tr>
<tr><td>Format</td><td>s.13.2</td></tr>
<tr><td>Units</td><td>Current (mA)</td></tr>
<tr><td>0x0000</td><td>0</td></tr>
<tr><td>0x0001</td><td>0.25</td></tr>
<tr><td>0x0002</td><td>0.5</td></tr>
<tr><td>0x0003</td><td>0.75</td></tr>
<tr><td>0x0004</td><td>1</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0x0010</td><td>4</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0x0100</td><td>64</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0x7FFF</td><td>8191.75</td></tr>
<tr><td>0x8000</td><td>-8192</td></tr>
<tr><td>0x8001</td><td>-8191.75</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0xFFFF</td><td>-0.25</td></tr>
</table>
</td></tr>
<tr><td colspan="6">ADC_SAMPLE1PH1LSB</td></tr>
<tr><td>0x19</td><td>7:0</td><td>ADC_SAMPLE1PH1LSB</td><td>R</td><td></td><td>Lower Byte of Buck1, Phase1 Output Current (combine with MSB for 16-bit value) See “ADC_SAMPLE1PH1MSB” for decode.</td></tr>
<tr><td colspan="6">ADC_SAMPLE1PH2MSB</td></tr>
<tr><td>0x1A</td><td>7:0</td><td>ADC_SAMPLE1PH2MSB</td><td>R</td><td></td><td>Upper Byte of Buck1, Phase2 Output Current (combine with LSB for 16-bit value.) See “ADC_SAMPLE1PH1MSB” for decode.</td></tr>
<tr><td colspan="6">ADC_SAMPLE1PH2LSB</td></tr>
<tr><td>0x1B</td><td>7:0</td><td>ADC_SAMPLE1PH2LSB</td><td>R</td><td></td><td>Lower Byte of Buck1, Phase2 Output Current (combine with MSB for 16-bit value) See “ADC_SAMPLE1PH1MSB” for decode.</td></tr>
<tr><td colspan="6">ADC_SAMPLE1PH3MSB</td></tr>
<tr><td>0x1C</td><td>7:0</td><td>ADC_SAMPLE1PH3MSB</td><td>R</td><td></td><td>Upper Byte of Buck1, Phase3 Output Current (combine with LSB for 16-bit value.) See “ADC_SAMPLE1PH1MSB” for decode.</td></tr>
<tr><td colspan="6">ADC_SAMPLE1PH3LSB</td></tr>
<tr><td>0x1D</td><td>7:0</td><td>ADC_SAMPLE1PH3LSB</td><td>R</td><td></td><td>Lower Byte of Buck1, Phase3 Output Current (combine with MSB for 16-bit value) See “ADC_SAMPLE1PH1MSB” for decode.</td></tr>
<tr><td colspan="6">ADC_SAMPLE1PH4MSB</td></tr>
<tr><td>0x1E</td><td>7:0</td><td>ADC_SAMPLE1PH4MSB</td><td>R</td><td></td><td>Upper Byte of Buck1, Phase4 Output Current (combine with LSB for 16-bit value.) See “ADC_SAMPLE1PH1MSB” for decode.</td></tr>
<tr><td colspan="6">ADC_SAMPLE1PH4LSB</td></tr>
<tr><td>0x1F</td><td>7:0</td><td>ADC_SAMPLE1PH4LSB</td><td>R</td><td></td><td>Lower Byte of Buck1, Phase4 Output Current (combine with MSB for 16-bit value) See “ADC_SAMPLE1PH1MSB” for decode.</td></tr>
</table>

<table>
<tr><th>Address</th><th>Bit</th><th>Name</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td colspan="6">ADC_SAMPLE1TMSB</td></tr>
<tr><td>0x20</td><td>7:0</td><td>ADC_SAMPLE1TMSB</td><td>R</td><td></td><td>
<table>
<tr><td colspan="2">Upper Byte of Buck1, Total Output Current Reading
(Combine with LSB for 16-bit value.)</td></tr>
<tr><td>Source</td><td>I_{SENSE}</td></tr>
<tr><td>Range</td><td>±32.768A</td></tr>
<tr><td>Format</td><td>s.15</td></tr>
<tr><td>Units</td><td>Current (mA)</td></tr>
<tr><td>0x0000</td><td>0</td></tr>
<tr><td>0x0001</td><td>1</td></tr>
<tr><td>0x0002</td><td>2</td></tr>
<tr><td>0x0003</td><td>3</td></tr>
<tr><td>0x0004</td><td>4</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0x0010</td><td>16</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0x0100</td><td>256</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0x7FFF</td><td>32767</td></tr>
<tr><td>0x8000</td><td>-32768</td></tr>
<tr><td>0x8001</td><td>-32767</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0xFFFF</td><td>-1</td></tr>
</table>
</td></tr>
<tr><td colspan="6">ADC_SAMPLE1TLSB</td></tr>
<tr><td>0x21</td><td>7:0</td><td>ADC_SAMPLE1TLSB</td><td>R</td><td></td><td>Lower Byte of Buck1, Total Output Current Reading (combine with MSB for 16-bit value) See “ADC_SAMPLE1TMSB” for decode.</td></tr>
</table>

<table>
<tr><th>Address</th><th>Bit</th><th>Name</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td colspan="6">ADC_SAMPLE2MSB</td></tr>
<tr><td>0x22</td><td>7:0</td><td>ADC_SAMPLE2MSB</td><td>R</td><td></td><td>
<table>
<tr><td colspan="2">Upper Byte of Buck1, PVIN Sample
(combine with LSB for 16-bit value.)</td></tr>
<tr><td>Source</td><td>PVIN</td></tr>
<tr><td>Range</td><td>±8.192V</td></tr>
<tr><td>Format</td><td>s.13.2</td></tr>
<tr><td>Units</td><td>Voltage (mV)</td></tr>
<tr><td>0x0000</td><td>0</td></tr>
<tr><td>0x0001</td><td>0.25</td></tr>
<tr><td>0x0002</td><td>0.5</td></tr>
<tr><td>0x0003</td><td>0.75</td></tr>
<tr><td>0x0004</td><td>1</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0x0010</td><td>4</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0x0100</td><td>64</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0x7FFF</td><td>8191.75</td></tr>
<tr><td>0x8000</td><td>-8192</td></tr>
<tr><td>0x8001</td><td>-8191.75</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0xFFFF</td><td>-0.25</td></tr>
</table>
</td></tr>
<tr><td colspan="6">ADC_SAMPLE2LSB</td></tr>
<tr><td>0x23</td><td>7:0</td><td>ADC_SAMPLE2LSB</td><td>R</td><td></td><td>Lower Byte of Buck1 PVIN Reading (combine with MSB for 16-bit value)
See “ADC_SAMPLE2MSB” for decode.</td></tr>
</table>

<table>
<tr><th>Address</th><th>Bit</th><th>Name</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td colspan="6">ADC_SAMPLE3MSB</td></tr>
<tr><td>0x24</td><td>7:0</td><td>ADC_SAMPLE3MSB</td><td>R</td><td></td><td>
<table>
<tr><td colspan="2">Upper Byte of Buck1, V_{OUT} Sample
(combine with LSB for 16-bit value.)</td></tr>
<tr><td>Source</td><td>V_{OUT}</td></tr>
<tr><td>Range</td><td>±8.192V</td></tr>
<tr><td>Format</td><td>s.13.2</td></tr>
<tr><td>Units</td><td>Voltage (mV)</td></tr>
<tr><td>0x0000</td><td>0</td></tr>
<tr><td>0x0001</td><td>0.25</td></tr>
<tr><td>0x0002</td><td>0.5</td></tr>
<tr><td>0x0003</td><td>0.75</td></tr>
<tr><td>0x0004</td><td>1</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0x0010</td><td>4</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0x0100</td><td>64</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0x7FFF</td><td>8191.75</td></tr>
<tr><td>0x8000</td><td>-8192</td></tr>
<tr><td>0x8001</td><td>-8191.75</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0xFFFF</td><td>-0.25</td></tr>
</table>
</td></tr>
<tr><td colspan="6">ADC_SAMPLE3LSB</td></tr>
<tr><td>0x25</td><td>7:0</td><td>ADC_SAMPLE3LSB</td><td>R</td><td></td><td>Lower Byte of Buck1 V_{OUT} Reading (combine with MSB for 16-bit value) See “ADC_SAMPLE3MSB” for decode.</td></tr>
<tr><td colspan="6">ADC_SAMPLE4PH1MSB</td></tr>
<tr><td>0x26</td><td>7:0</td><td>ADC_SAMPLE4PH1MSB</td><td>R</td><td></td><td>Upper Byte of Buck2, Phase1 Output Current (combine with LSB for 16-bit value) See ADC_SAMPLE1PH1MSB for decode.</td></tr>
<tr><td colspan="6">ADC_SAMPLE4PH1LSB</td></tr>
<tr><td>0x27</td><td>7:0</td><td>ADC_SAMPLE4PH1LSB</td><td>R</td><td></td><td>Lower Byte of Buck2, Phase1 Output Current (combine with MSB for 16-bit value) See ADC_SAMPLE1PH1MSB for decode.</td></tr>
<tr><td colspan="6">ADC_SAMPLE4PH2MSB</td></tr>
<tr><td>0x28</td><td>7:0</td><td>ADC_SAMPLE4PH2MSB</td><td>R</td><td></td><td>Upper Byte of Buck2, Phase2 Output Current (combine with LSB for 16-bit value) See ADC_SAMPLE1PH1MSB for decode.</td></tr>
<tr><td colspan="6">ADC_SAMPLE4PH2LSB</td></tr>
<tr><td>0x29</td><td>7:0</td><td>ADC_SAMPLE4PH2LSB</td><td>R</td><td></td><td>Lower Byte of Buck2, Phase2 Output Current (combine with MSB for 16-bit value) See ADC_SAMPLE1PH1MSB for decode.</td></tr>
<tr><td colspan="6">ADC_SAMPLE4TMSB</td></tr>
<tr><td>0x2A</td><td>7:0</td><td>ADC_SAMPLE4TMSB</td><td>R</td><td></td><td>Upper Byte of Buck2, Total Output Current (combine with LSB for 16-bit value) See ADC_SAMPLE1TMSB for decode.</td></tr>
<tr><td colspan="6">ADC_SAMPLE4TLSB</td></tr>
<tr><td>0x2B</td><td>7:0</td><td>ADC_SAMPLE4TLSB</td><td>R</td><td></td><td>Lower Byte of Buck2, Total Output Current (combine with MSB for 16-bit value) See ADC_SAMPLE1TMSB for decode.</td></tr>
</table>

<table>
<tr><th>Address</th><th>Bit</th><th>Name</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td colspan="6">ADC_SAMPLE5MSB</td></tr>
<tr><td>0x2C</td><td>7:0</td><td>ADC_SAMPLE5MSB</td><td>R</td><td></td><td>Upper Byte of Buck2, PVIN Reading (combine with LSB for 16-bit value)
See ADC_SAMPLE2MSB for decode.</td></tr>
<tr><td colspan="6">ADC_SAMPLE5LSB</td></tr>
<tr><td>0x2D</td><td>7:0</td><td>ADC_SAMPLE5LSB</td><td>R</td><td></td><td>Lower Byte of Buck2, PVIN Reading (combine with MSB for 16-bit value)
See ADC_SAMPLE2MSB for decode.</td></tr>
<tr><td colspan="6">ADC_SAMPLE6MSB</td></tr>
<tr><td>0x2E</td><td>7:0</td><td>ADC_SAMPLE6MSB</td><td>R</td><td></td><td>Upper Byte of Buck2, V_{OUT} Reading (Combine with LSB for 16-bit value.)
See ADC_SAMPLE3MSB for decode.</td></tr>
<tr><td colspan="6">ADC_SAMPLE6LSB</td></tr>
<tr><td>0x2F</td><td>7:0</td><td>ADC_SAMPLE6LSB</td><td>R</td><td></td><td>Lower Byte of Buck2, V_{OUT} Reading (combine with MSB for 16-bit value)
See ADC_SAMPLE3MSB for decode.</td></tr>
<tr><td colspan="6">ADC_AUX0MSB</td></tr>
<tr><td>0x30</td><td>7:0</td><td>ADC_AUX0MSB</td><td>R</td><td></td><td>Upper Byte of ADC Auxiliary Input #1
Can be used in IO_PINMODE = 0xC, 0xD to measure external voltage with internal ADC.
<table>
<tr><td>Source</td><td>AUX0</td></tr>
<tr><td>Range</td><td>±8.192V</td></tr>
<tr><td>Format</td><td>s.13.2</td></tr>
<tr><td>Units</td><td>Voltage (mV)</td></tr>
<tr><td>0x0000</td><td>0</td></tr>
<tr><td>0x0001</td><td>0.25</td></tr>
<tr><td>0x0002</td><td>0.5</td></tr>
<tr><td>0x0003</td><td>0.75</td></tr>
<tr><td>0x0004</td><td>1</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0x0010</td><td>4</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0x0100</td><td>64</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0x7FFF</td><td>8191.75</td></tr>
<tr><td>0x8000</td><td>-8192</td></tr>
<tr><td>0x8001</td><td>-8191.75</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0xFFFF</td><td>-0.25</td></tr>
</table></td></tr>
<tr><td colspan="6">ADC_AUX0LSB</td></tr>
<tr><td>0x31</td><td>7:0</td><td>ADC_AUX0LSB</td><td>R</td><td></td><td>Lower Byte of ADC Auxiliary Input #1 (combine with MSB for 16-bit value)
See “ADC_AUX0MSB” for decode.</td></tr>
<tr><td colspan="6">ADC_AUX1MSB</td></tr>
<tr><td>0x32</td><td>7:0</td><td>ADC_AUX1MSB</td><td>R</td><td></td><td>Upper Byte of ADC Auxiliary Input #2 (combine with LSB for 16-bit value)
Can be used in IO_PINMODE[3:0] = 0xC, 0xD to measure external voltage with internal ADC. See “ADC_AUX0MSB” for decode.</td></tr>
<tr><td colspan="6">ADC_AUX1LSB</td></tr>
<tr><td>0x33</td><td>7:0</td><td>ADC_AUX1LSB</td><td>R</td><td></td><td>Lower Byte of ADC Auxiliary Input #2 (combine with MSB for 16-bit value)
See “ADC_AUX0MSB” for decode.</td></tr>
</table>

Address	Bit	Name	R/W	Default	Description
IO_SPICFG					
0x43	7	IO_I2C_SPEED	R/W	0x0	I^2C Speed Control 0x0: Low speed glitch and slew filters by default, high speed filters selectable by bus command. 0x1: Glitch and slew filters set for high speed 3.4MHz mode.
	6	IO_SDA_SLEWFLTR	R/W	0x0	Transmit Slew Rate Control for I^2C SDA 0x0: Disabled slew filtering. 0x1: Enable slew filtering.
	5	IO_SPIRWPOL	R/W	0x0	R/W Polarity 0x0: R/W 1: Read, 0: Write 0x1: R/W 1: Write, 0: Read
	4	IO_IRQ_CMOS	R/W	0x1	IRQ Type 0x0: Open-drain output 0x1: CMOS output
	3	IO_IRQ_INVERT	R/W	0x1	IRQ Polarity 0x0: Active High 0x1: Active Low
	2	IO_SPICPOL	R/W	0x0	SPI Clock Polarity 0x0: Active High 0x1: Active Low
	1	IO_SPICPHA	R/W	0x0	SPI Clock Phase 0x0: Sample on the leading (first) clock edge **Note:** Data must be stable for a half cycle before the first clock cycle. 0x1: Sample on the trailing (second) clock edge, regardless of whether that clock edge is rising or falling.
	0	IO_SPIMODE	R/W	0x1	SPI Mode Selection 0x0: Byte Mode Command Byte R/W, AINC, 0x0, 0x0, 0x0, 0x0, P1, P0 Address Byte A7, A6, A5, A4, A3, A2, A1, A0 Data Byte D7, D6, D5, D4, D3, D2, D1, D0 0x1: Byte Mode with Packet Length Field Command Byte R/W, AINC, 0x0, 0x0, 0x0, 0x0, P1, P0 Address Byte A7, A6, A5, A4, A3, A2, A1, A0 Packet Length Byte L7, L6, L5, L4, L3, L2, L1, L0 Data Byte D7, D6, D5, D4, D3, D2, D1, D0

<table>
<tr><th>Address</th><th>Bit</th><th>Name</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td colspan="6">IO_MODECTRL</td></tr>
<tr><td rowspan="6">0x44</td><td>7</td><td>IO_BUCK1_EN</td><td>R/W</td><td>0x1</td><td>Enable for Buck1
0x0 Buck1 disabled.
0x1 Buck1 enabled.</td></tr>
<tr><td>6</td><td>IO_BUCK2_EN</td><td>R/W</td><td>0x1</td><td>Enable for Buck2
0x0 Buck2 disabled.
0x1 Buck2 enabled.</td></tr>
<tr><td>5:3</td><td>RSVD</td><td>R</td><td>0x0</td><td>Reserved</td></tr>
<tr><td>2</td><td>IO_ENVPPPULLDOWN</td><td>R/W</td><td>0x1</td><td>Enable for weak Pull-down on EN/VPP Pin
0x0 Weak pull-down disabled.
0x1 Weak pull-down enabled.</td></tr>
<tr><td>1</td><td>RSVD</td><td>R/W</td><td>0x0</td><td>Reserved</td></tr>
<tr><td>0</td><td>RSVD</td><td>R/W</td><td>0x0</td><td>Reserved</td></tr>
<tr><td colspan="6">FLT_TEMPWARN</td></tr>
<tr><td>0x58</td><td>7:0</td><td>FLT_TEMPWARN</td><td>R/W</td><td>0x55</td><td>Temperature Warning Threshold (highest)
°C = FLT_TEMPWARN[7:0] (Range 0°C to +255°C)
0x00 0
0x01 1
…
0x7F 127
0x80 128
0x81 129
…
0x8C 140
…
0xFF 255</td></tr>
</table>

<table>
<tr><th>Address</th><th>Bit</th><th>Name</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td colspan="6">FLT_TEMPSHUTDN</td></tr>
<tr><td>0x59</td><td>7:0</td><td>FLT_TEMPSHUTDN</td><td>R/W</td><td>0x8C</td><td>
<table>
<tr><td colspan="2">Temperature Shutdown threshold (highest)</td></tr>
<tr><td></td><td>°C = FLT_TEMPSHUTDN[7:0] (Range 0°C to +255°C)</td></tr>
<tr><td>0x00</td><td>0</td></tr>
<tr><td>0x01</td><td>1</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0x7F</td><td>127</td></tr>
<tr><td>0x80</td><td>128</td></tr>
<tr><td>0x81</td><td>129</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0x8C</td><td>140</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0xFF</td><td>255</td></tr>
</table>
</td></tr>
<tr><td colspan="6">FLT_BUCK1_ISENSEWARN</td></tr>
<tr><td rowspan="2">0x5B</td><td>7:4</td><td>FLT_BUCK1_
ISENSEWARNR</td><td>R/W</td><td>0x5</td><td>
<table>
<tr><td colspan="2">Buck1 Current Sense Warning Rising Threshold</td></tr>
<tr><td colspan="2">Hysteresis mA = 512mA * (FLT_BUCK1_ISENSEAWARNR–
FLT_BUCK1_ISENSEAWARNF)
Note: Hysteresis must be ≥ 0mA and small enough to ensure that the current goes below the falling threshold.</td></tr>
<tr><td></td><td>Current (mA) = 512mA * FLT_BUCK1_ISENSEWARNR</td></tr>
<tr><td>0x0</td><td>0</td></tr>
<tr><td></td><td></td></tr>
<tr><td>0x1</td><td>510</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0x4</td><td>2048</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0xF</td><td>8160</td></tr>
</table>
</td></tr>
<tr><td>3:0</td><td>FLT_BUCK1_
ISENSEWARNF</td><td>R/W</td><td>0x4</td><td>
<table>
<tr><td colspan="2">Buck1 Current Sense Warning Falling Threshold</td></tr>
<tr><td></td><td>Current (mA) = 510mA * FLT_BUCK1_ISENSEWARNF</td></tr>
<tr><td>0x0</td><td>0</td></tr>
<tr><td>0x1</td><td>510</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0x4</td><td>2048</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0xF</td><td>8160</td></tr>
</table>
</td></tr>
<tr><td colspan="6">FLT_BUCK2_ISENSEWARN</td></tr>
<tr><td rowspan="2">0x5C</td><td>7:4</td><td>FLT_BUCK2_
ISENSEWARNR</td><td>R/W</td><td>0x5</td><td>Buck2 Current Sense Warning Rising Threshold
See “FLT_BUCK1_ISENSEWARN” for decode.</td></tr>
<tr><td>3:0</td><td>FLT_BUCK2_
ISENSEWARNF</td><td>R/W</td><td>0x4</td><td>Buck2 Current Sense Warning Falling Threshold
See “FLT_BUCK1_ISENSEWARN” for decode.</td></tr>
</table>

<table>
<tr><th>Address</th><th>Bit</th><th>Name</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td colspan="6">FLT_BUCK1_ISENSESHUTDN</td></tr>
<tr><td>0x5D</td><td>7:0</td><td>FLT_BUCK1_
ISENSESHUTDN</td><td>R/W</td><td>0xA0</td><td>
<table>
<tr><td colspan="2">Buck1 Current Sense Shutdown Threshold (highest)</td></tr>
<tr><td colspan="2">Note: Hysteresis is accomplished by shutting down the Buck and resetting the filtered I_{SENSE} value.</td></tr>
<tr><td></td><td>Current (mA) = 32mA * FLT_BUCK1_ISENSESHUTDN[7:0]</td></tr>
<tr><td>0x00</td><td>0</td></tr>
<tr><td>0x01</td><td>32 * Nph</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0x7F</td><td>4064 * Nph</td></tr>
<tr><td>0x80</td><td>4096 * Nph</td></tr>
<tr><td>0x81</td><td>4128 * Nph</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0xA0</td><td>5120 * Nph</td></tr>
<tr><td>…</td><td></td></tr>
<tr><td>0xFF</td><td>8160 * Nph (via ENCF)</td></tr>
</table>
</td></tr>
<tr><td colspan="6">FLT_BUCK2_ISENSESHUTDN</td></tr>
<tr><td>0x5E</td><td>7:0</td><td>FLT_BUCK2_
ISENSESHUTDN</td><td>R/W</td><td>0xA0</td><td>Buck2 Current Sense Shutdown Threshold (Highest)
See “FLT_BUCK1_ISENSESHUTDN” for decode.</td></tr>
</table>

Address	Bit	Name	R/W	Default	Description
FLT_MASKTEMP					
0x60	7	FLT_MASKBOOT	R/W	0x0	Mask IRQ for FLT_BOOT 0x0: IRQ passed to output pin. 0x1: IQ masked from output pin.
	6:4	Reserved	R	0x0	Reserved
	3	FLT_MASKTEMPSDR	R/W	0x0	Mask IRQ for FLT_TEMPSDR 0x0: IRQ passed to output pin. 0x1: IRQ masked from output pin.
	2	FLT_MASKTEMPWARNR	R/W	0x0	Mask IRQ for FLT_TEMPWARNR 0x0: IRQ passed to output pin Note: FLT_MASKTEMPWARNF must also be set to 0x0. Otherwise the IRQ clears itself when the temperature drops below the falling threshold. 0x1: IRQ masked from output pin
	1	FLT_MASKTEMPWARNF	R/W	0x0	Mask IRQ for FLT_TEMPWARNF 0x0: IRQ passed to output pin Note: FLT_MASKTEMPWARNR must also be set to 0x0. Otherwise the IRQ clears itself when the temperature goes above the rising threshold. 0x1: IRQ masked from output pin
	0	FLT_MASKTEMPSDF	R/W	0x0	Mask IRQ for FLT_TEMPSDF 0x0: IRQ passed to output pin. 0x1: IQ masked from output pin.

Address	Bit	Name	R/W	Default	Description
FLT_MASKBUCK1					
0x61	7	Reserved	R	0x0	Reserved
	6	FLT_BUCK1_MASKWOC	R/W	0x0	Mask IRQ for FLT_BUCK1_WOC 0x0: IRQ passed to output pin 0x1: IRQ masked from output pin
	5	FLT_BUCK1_MASKOV	R/W	0x0	Mask IRQ for FLT_BUCK1_OV 0x0: IRQ passed to output pin 0x1: IRQ masked from output pin
	4	FLT_BUCK1_MASKUV	R/W	0x0	Mask IRQ for FLT_BUCK1_UV 0x0: IRQ passed to output pin 0x1: IRQ masked from output pin
	3	FLT_BUCK1_MASKOCSDR	R/W	0x0	Mask IRQ for FLT_BUCK1_OCSDR 0x0: IRQ passed to output pin 0x1: IRQ masked from output pin
	2	FLT_BUCK1_MASKOCWR	R/W	0x0	Mask IRQ for FLT_BUCK1_OCWR 0x0: IRQ passed to output pin Note: FLT_MASKOCWF must also be set to 0x0. Otherwise the IRQ clears itself when the current drops below the falling threshold. 0x1: IRQ masked from output pin
	1	FLT_BUCK1_MASKOCWF	R/W	0x0	Mask IRQ for FLT_BUCK1_OCWF 0x0: IRQ passed to output pin 0x1: IRQ masked from output pin
	0	Reserved	R	0x0	Reserved

<table>
<tr><th>Address</th><th>Bit</th><th>Name</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td colspan="6">FLT_MASKBUCK2</td></tr>
<tr><td rowspan="8">0x62</td><td>7</td><td>FLT_BUCK2_MASKRSVD1</td><td>R</td><td>0x0</td><td rowspan="8">IRQ Masks for Buck2
See <a>“FLT_MASKBUCK1” for description.</td></tr>
<tr><td>6</td><td>FLT_BUCK2_MASKWOC</td><td>R/W</td><td>0x0</td></tr>
<tr><td>5</td><td>FLT_BUCK2_MASKOV</td><td>R/W</td><td>0x0</td></tr>
<tr><td>4</td><td>FLT_BUCK2_MASKUV</td><td>R/W</td><td>0x0</td></tr>
<tr><td>3</td><td>FLT_BUCK2_MASKOCSDR</td><td>R/W</td><td>0x0</td></tr>
<tr><td>2</td><td>FLT_BUCK2_MASKOCWR</td><td>R/W</td><td>0x0</td></tr>
<tr><td>1</td><td>FLT_BUCK2_MASKOCWF</td><td>R/W</td><td>0x0</td></tr>
<tr><td>0</td><td>FLT_BUCK2_MASKRSVD2</td><td>R</td><td>0x0</td></tr>
<tr><td colspan="6">BUCK1_EA2</td></tr>
<tr><td rowspan="2">0x66</td><td>7:6</td><td>BUCK1_VOUTFBDIV</td><td>R/W</td><td>0x0</td><td>
<table>
<tr><th>Feedback Divider</th><th>Maximum V_{OUT} Setting</th></tr>
<tr><td>0x0</td><td>1.2000V</td></tr>
<tr><td>0x1</td><td>1.5000V</td></tr>
<tr><td>0x2</td><td>2.0000V</td></tr>
<tr><td>0x3</td><td>Reserved</td></tr>
</table>
</td></tr>
<tr><td></td><td>Reserved</td><td>R</td><td>0x1B</td><td>Reserved</td></tr>
<tr><td colspan="6">BUCK1_DCM</td></tr>
<tr><td rowspan="3">0x69</td><td>7:3</td><td>Reserved</td><td>N/A</td><td>0x0</td><td>Reserved</td></tr>
<tr><td>2</td><td>BUCK1_FCCM</td><td>R/W</td><td>0x0</td><td>
<table>
<tr><td colspan="2">Forced Continuous Conduction Mode</td></tr>
<tr><td>0x0</td><td>Discontinuous Conduction Mode (DCM) allowed when load reaches 0A.</td></tr>
<tr><td>0x1</td><td>Always operate in Continuous Conduction Mode (CCM).</td></tr>
</table>
</td></tr>
<tr><td>1:0</td><td>Reserved</td><td>R/W</td><td>0x0</td><td>Reserved</td></tr>
<tr><td colspan="6">BUCK1_DVS0CFG1</td></tr>
<tr><td>0x72</td><td>7:0</td><td>BUCK1_DVS0VOUT92[7:0]</td><td>R/W</td><td>TRIM</td><td>
Upper eight bits of a 10-bit DAC[9:0] value to generate V_{OUT} for DVS Configuration 0.
Note: V_{OUT} must be programmed above 0.3V.
FBDIV is set by factory OTP to 1x, 0.8x, 0.6x.
<table>
<tr><td>FBDIV</td><td>1.0</td><td>0.8</td><td>0.6</td></tr>
<tr><td>DAC</td><td>V_{OUT} (V)</td><td>V_{OUT} (V)</td><td>V_{OUT} (V)</td></tr>
<tr><td>0x000</td><td>0.0000</td><td>0.0000</td><td>0.0000</td></tr>
<tr><td>0x001</td><td>0.0012</td><td>0.0015</td><td>0.0020</td></tr>
<tr><td>…</td><td></td><td></td><td></td></tr>
<tr><td>0x200</td><td>0.6144</td><td>0.768</td><td>1.024</td></tr>
<tr><td>0x201</td><td>0.6156</td><td>0.7695</td><td>1.026</td></tr>
<tr><td>…</td><td></td><td></td><td></td></tr>
<tr><td>0x3E8</td><td>1.2</td><td>1.5</td><td>2.0</td></tr>
</table>
</td></tr>
</table>

Address	Bit	Name	R/W	Default	Description
BUCK1_DVS0CFG0					
0x73	7:6	BUCK1_DVS0VOUT10	R/W	TRIM	Lower two bits of a 10-bit DAC[9:0] value to generate V_{OUT} for DVS Configuration 0. Note: When DVS Configuration 0 is selected (by pins or registers) any write to BUCK1_DVS0CFG0 causes a DVS ramping to occur.
	5	RSVD	R/W	0x0	Reserved
	4:0	Reserved	R	0x0	Reserved
BUCK1_DVS1CFG1					
0x74	7:0	BUCK1_DVS1VOUT92	R/W	TRIM	Buck1 DVS1 Configuration 1, See "BUCK1_DVS0CFG1" for description
BUCK1_DVS1CFG0					
0x75	7:6	BUCK1_DVS1VOUT10	R/W	TRIM	Buck1 DVS1 Configuration 0, See "BUCK1_DVS0CFG0" for description
	5	BUCK1_DVS1DECAY	R/W	0x0	
	4:0	BUCK1_DVS1RSVD	R	0x0	
BUCK1_DVS2CFG1					
0x76	7:0	BUCK1_DVS2VOUT92	R/W	TRIM	Buck1 DVS2 Configuration 1, See "BUCK1_DVS0CFG1" for description
BUCK1_DVS2CFG0					
0x77	7:6	BUCK1_DVS2VOUT10	R/W	TRIM	Buck1 DVS2 Configuration 0, See "BUCK1_DVS0CFG0" for description
	5	BUCK1_DVS2DECAY	R/W	0x0	
	4:0	BUCK1_DVS2RSVD	R	0x0	
BUCK1_DVS3CFG1					
0x78	7:0	BUCK1_DVS3VOUT92	R/W	TRIM	Buck1 DVS3 Configuration 1, See "BUCK1_DVS0CFG1" for description
BUCK1_DVS3CFG0					
0x79	7:6	BUCK1_DVS3VOUT10	R/W	TRIM	Buck1 DVS3 Configuration 0. See "BUCK1_DVS0CFG0" for description
	5	BUCK1_DVS3DECAY	R/W	0x0	
	4:0	BUCK1_DVS3RSVD	R	0x0	
BUCK1_DVSSEL					
0x7D	7:3	Reserved	R	0x00	Reserved
	2	BUCK1_DVSCTRL	R/W	0x0	BUCK1 DVS Control 0x0: Use BUCK1_DVSSELECT[1:0] to select active DVS configuration. See Dynamic Voltage Scaling (DVS) for more detail on how to use.
	1:0	BUCK1_DVSSELECT	R/W	0x0	BUCK1 DVS Selection 0x0: Use DVS0 voltage setting 0x1: Use DVS1 voltage setting 0x2: Use DVS2 voltage setting 0x3: Use DVS3 voltage setting **Note:** When BUCK1_DVSCTRL[0] = 0x0 any write to the register BUCK1_DVSSEL causes a DVS ramping event to occur.

<table>
<tr><th>Address</th><th>Bit</th><th>Name</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td colspan="6">BUCK1_RSPCFG1</td></tr>
<tr><td>0x7E</td><td>7</td><td>BUCK1_RSPCFG1RSVD1</td><td>R</td><td>0x0</td><td>Reserved</td></tr>
<tr><td></td><td>6:4</td><td>BUCK1_RSPUP</td><td>R/W</td><td>0x7</td><td>This slew rate is used when the current voltage is less than the target voltage.
V_{OUT} Ramp Slew Rate
RSP = BUCK1_RSPUP[1:0], Ramp Speed
FBDIV = BUCK1_VOUTFBDIV[1:0] = (1.0, 0.8, 0.6)
Slow = BUCK1_RSPUP[2] = 0
Fast = BUCK1_RSPUP[2] = 1
<table>
<tr><th rowspan="2">RSP</th><th rowspan="2">FBDIV</th><th colspan="2">V_{OUT} Ramp Speed mV/µs</th></tr>
<tr><th>Fast</th><th>Slow</th></tr>
<tr><td>0x0</td><td>1.0</td><td>12</td><td>3</td></tr>
<tr><td>0x1</td><td>1.0</td><td>24</td><td>6</td></tr>
<tr><td>0x2</td><td>1.0</td><td>58</td><td>14</td></tr>
<tr><td>0x3</td><td>1.0</td><td>115</td><td>29</td></tr>
</table>
<table>
<tr><th rowspan="2">RSP</th><th rowspan="2">FBDIV</th><th colspan="2">V_{OUT} Ramp Speed mV/µs</th></tr>
<tr><th>Fast</th><th>Slow</th></tr>
<tr><td>0x0</td><td>0.8</td><td>12</td><td>3</td></tr>
<tr><td>0x1</td><td>0.8</td><td>24</td><td>6</td></tr>
</table>
<table>
<tr><th rowspan="2">RSP</th><th rowspan="2">FBDIV</th><th colspan="2">V_{OUT} Ramp Speed mV/µs</th></tr>
<tr><th>Fast</th><th>Slow</th></tr>
<tr><td>0x0</td><td>0.6</td><td>12</td><td>3</td></tr>
<tr><td>0x1</td><td>0.6</td><td>24</td><td>6</td></tr>
</table></td></tr>
<tr><td></td><td>3</td><td>Reserved</td><td>R</td><td>0x0</td><td>Reserved</td></tr>
<tr><td></td><td>2:0</td><td>BUCK1_RSPDN</td><td>R/W</td><td>0x3</td><td>This slew rate is used when the current voltage is greater than the target voltage.
See BUCK1_RSPUP above for decode information.</td></tr>
</table>

<table>
<tr><th>Address</th><th>Bit</th><th>Name</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td colspan="6">BUCK1_RSPCFG0</td></tr>
<tr><td>0x7F</td><td>7</td><td>Reserved</td><td>R</td><td>0x0</td><td>Reserved</td></tr>
<tr><td></td><td>6:4</td><td>BUCK1_RSPPUP</td><td>R/W</td><td>0x7</td><td>This slew rate is used when the current voltage is 0V and the target is greater than 0V.
V_{OUT} Ramp Slew Rate
RSP = BUCK1_RSPUP[1:0], Ramp Speed
FBDIV = BUCK1_VOUTFBDIV[1:0] = (1.0, 0.8, 0.6)
Slow = BUCK1_RSPUP[2] = 0
Fast = BUCK1_RSPUP[2] = 1
<table>
<tr><th rowspan="2">RSP</th><th rowspan="2">FBDIV</th><th colspan="2">V_{OUT} Ramp Speed mV/µs</th></tr>
<tr><th>Fast</th><th>Slow</th></tr>
<tr><td>0x0</td><td>1.0</td><td>6</td><td>1.2</td></tr>
<tr><td>0x1</td><td>1.0</td><td>12</td><td>3</td></tr>
<tr><td>0x2</td><td>1.0</td><td>29</td><td>7.2</td></tr>
<tr><td>0x3</td><td>1.0</td><td>58</td><td>15</td></tr>
</table>
<table>
<tr><th rowspan="2">RSP</th><th rowspan="2">FBDIV</th><th colspan="2">V_{OUT} Ramp Speed mV/µs</th></tr>
<tr><th>Fast</th><th>Slow</th></tr>
<tr><td>0x0</td><td>0.8</td><td>12</td><td>3</td></tr>
<tr><td>0x1</td><td>0.8</td><td>24</td><td>6</td></tr>
</table>
<table>
<tr><th rowspan="2">RSP</th><th rowspan="2">FBDIV</th><th colspan="2">V_{OUT} Ramp Speed mV/µs</th></tr>
<tr><th>Fast</th><th>Slow</th></tr>
<tr><td>0x0</td><td>0.6</td><td>12</td><td>3</td></tr>
<tr><td>0x1</td><td>0.6</td><td>24</td><td>6</td></tr>
</table></td></tr>
<tr><td></td><td>3</td><td>BUCK1_RSPCFG0RSVD0</td><td>R</td><td>0x0</td><td>Reserved</td></tr>
<tr><td></td><td>2:0</td><td>BUCK1_RSPPDN[2:0]</td><td>R/W</td><td>0x3</td><td>This slew rate is used when the current voltage is greater than 0V and the target voltage is 0V. See BUCK1_RSPPUP bits above for decode information.</td></tr>
<tr><td colspan="6">BUCK1_EN_DLY</td></tr>
<tr><td>0x80</td><td>7:6</td><td>Reserved</td><td>R</td><td>0x0</td><td>Reserved</td></tr>
<tr><td></td><td>5:0</td><td>BUCK1_EN_DLY</td><td>R/W</td><td>0x00</td><td>Delay time from BUCK1_EN and IO_REGVAID go high to actual Buck1 V_{OUT} ramping up.
Delay = (integer value of register) ms [1ms/LSB]
<table>
<tr><td></td><td>Delay</td></tr>
<tr><td>0x00</td><td>0</td></tr>
<tr><td>0x01</td><td>1ms</td></tr>
<tr><td>0x02</td><td>2ms</td></tr>
<tr><td>...</td><td></td></tr>
<tr><td>0x3F</td><td>63ms</td></tr>
</table></td></tr>
</table>

Address	Bit	Name	R/W	Default	Description
BUCK1_SHUTDN_DLY					
0x81	7:6	Reserved	R	0x0	Reserved
	5:0	BUCK1_SHUTDN_DLY	R/W	0x00	Delay time from BUCK1_EN and IO_REGVAID go low to actual Buck1 V_{OUT} ramping down. Delay = (integer value of register) ms [1ms/LSB] See "BUCK1_EN_DLY" for description
BUCK2_EA2					
0x82	7:6	BUCK2_VOUTFBDIV	R/W	0x0	Buck2 FBDIV Configuration. See BUCK1_EA2 for description
	5:0	Reserved	R	0x1B	Reserved
BUCK2_DCM					
0x85	7:3	Reserved	N/A	0x0	Reserved
	2	BUCK1_FCCM	R/W	0x0	Forced Continuous Conduction Mode 0x0: Discontinuous Conduction Mode (DCM) allowed when load reaches 0A. 0x1: Always operate in Continuous Conduction Mode (CCM).
	1:0	Reserved	R/W	0x0	Reserved
BUCK2_DVS0CFG1					
0x8E	7:0	BUCK2_DVS0VOUT92	R/W	TRIM	See BUCK1_DVS0CFG1
BUCK2_DVS0CFG0					
0x8F	7:6	BUCK2_DVS0VOUT10	R/W	TRIM	See BUCK1_DVS0CFG0
	5	BUCK2_DVS0DECAY	R/W	0x0	
	4:0	Reserved	R	0x0	
BUCK2_DVS1CFG1					
0x90	7:0	BUCK2_DVS1VOUT92	R/W	TRIM	See BUCK1_DVS0CFG0
BUCK2_DVS1CFG0					
0x91	7:6	BUCK2_DVS1VOUT10	R/W	TRIM	See BUCK1_DVS0CFG0
	5	BUCK2_DVS1DECAY	R/W	0x0	
	4:0	Reserved	R	0x0	
BUCK2_DVS2CFG1					
0x92	7:0	BUCK2_DVS2VOUT92[7:0]	R/W	TRIM	See BUCK1_DVS0CFG1
BUCK2_DVS2CFG0					
0x93	7:6	BUCK2_DVS2VOUT10	R/W	TRIM	See BUCK1_DVS0CFG0
	5	BUCK2_DVS2DECAY	R/W	0x0	
	4:0	Reserved	R	0x0	
BUCK2_DVS3CFG1					
0x94	7:0	BUCK2_DVS3VOUT92	R/W	TRIM	See BUCK1_DVS0CFG1
BUCK2_DVS3CFG0					
0x95	7:6	BUCK2_DVS3VOUT10	R/W	TRIM	See BUCK1_DVS0CFG0
	5	BUCK2_DVS3DECAY	R/W	0x0	
	4:0	Reserved	R	0x0	

Address	Bit	Name	R/W	Default	Description
BUCK2_VOUTMAXMSB					
0x96	7:2	Reserved	R	0x00	Reserved
	1:0	BUCK2_VOUTMAX98[1:0]	R/W	0x3	Upper two bits of V_{OUT} Maximum Programming Limit Data format is same as BUCK2_DVS[3:0]VOUT[9:0]
BUCK2_VOUTMAXLSB					
0x97	7:0	BUCK2_VOUTMAXLSB[7:0]	R/W	0xFF	Lower byte of V_{OUT} Maximum Programming Limit Data format is same as BUCK2_DVS[3:0]VOUT[9:0]
BUCK2_DVSSEL					
0x99	7:3	Reserved	R	0x00	See BUCK1_DVSSEL
	2	BUCK2_DVSCTRL	R/W	0x0	
	1:0	BUCK2_DVSSELECT	R/W	0x0	
BUCK2_RSPCFG1					
0x9A	7	Reserved	R	0x0	See BUCK1_RSPCFG1
	6:4	BUCK2_RSPUP	R/W	0x7	
	3	Reserved	R	0x0	
	2:0	BUCK2_RSPDN[2:0]	R/W	0x3	
BUCK2_RSPCFG0					
0x9B	7	Reserved	R	0x0	See BUCK1_RSPCFG0
	6:4	BUCK2_RSPPUP[2:0]	R/W	0x7	
	3	Reserved	R	0x0	
	2:0	BUCK2_RSPPDN[2:0]	R/W	0x3	
BUCK2_EN_DLY					
0x9C	7:6	Reserved	R	0x0	See BUCK1_EN_DLY
	5:0	BUCK2_EN_DLY	R/W	0x00	
BUCK2_SHUTDN_DLY					
0x9D	7:6	Reserved	R	0x0	See BUCK1_SHUTDN_DLY
	5:0	BUCK2_SHUTDN_DLY	R/W	0x00	

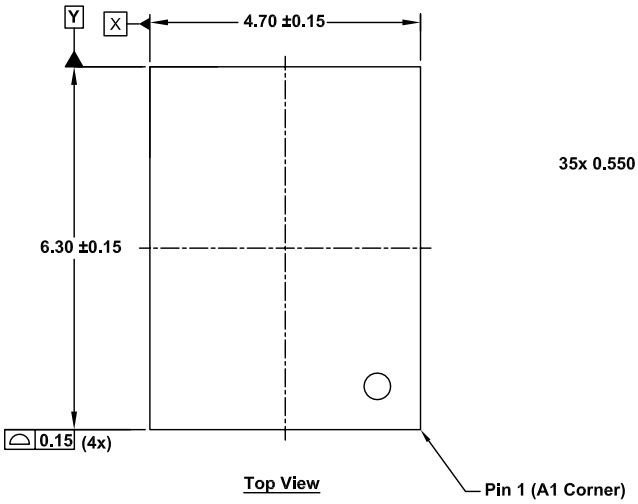
11. Revision History

Rev.	Date	Description
1.01	Feb.25.20	Removed addendum.
1.00	Dec.6.19	Rewrite throughout. Addendum added on page 61.
0.00	Jul.26.18	Initial release

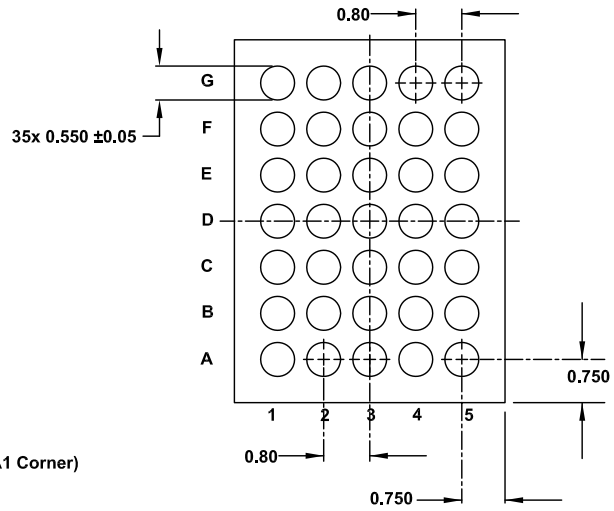
12. Package Outline Drawing

For the most recent package outline drawing, see V35.4.7x6.3.

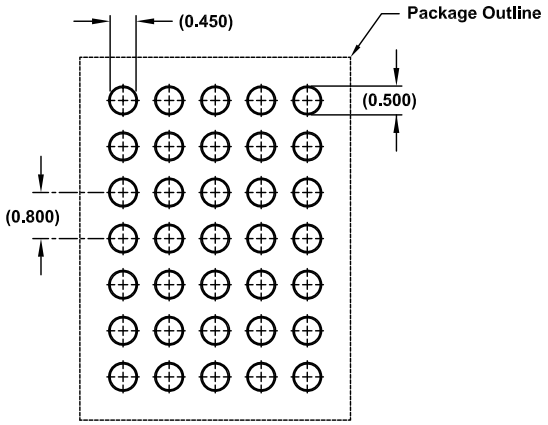
V35.4.7x6.3
35 Thin Profile Ball Grid Array Package (TFBGA)
Rev 3, 10/19



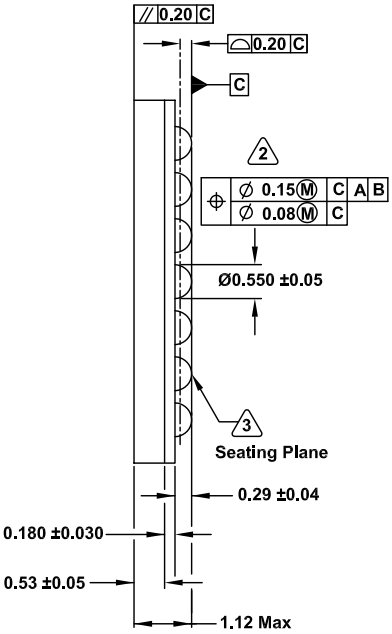
Top View



Bottom View



Typical Recommended Land Pattern



Side View

Notes:

1. All dimensions and tolerances conform to ASME Y14.5 - 2009.
2. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
3. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
4. Unless otherwise specified, dimensions are in millimeters.