

ISL9440EVAL2Z

Triple PWM Step-Down Synchronous Buck Controller and One LDO  
Evaluation Board

AN1550  
Rev 0.00  
Mar 8, 2010

**ISL9440EVAL2Z Evaluation Board**

The ISL9440EVAL2Z evaluation board features the ISL9440. The ISL9440 is a quad-output controller that integrates three PWM synchronous buck controllers and one low-dropout linear regulator controller. The ISL9440 offers internal soft-start, independent enable functions and integrates UV/OV/OC/OT protection. Its current mode control architecture and internal compensation network keep peripheral component count minimal. Switching frequency of 300kHz minimizes losses while the strong gate drivers deliver up to 12A to each PWM channel.

Table 1 shows the difference in terms of ISL944xx family features.

TABLE 1. FEATURES OF ISL944xx FAMILY

PART NUMBER	EARLY WARNING	SWITCHING FREQUENCY (kHz)	SOFT-STARTING TIME (ms)
ISL9440	Yes	300	1.7
ISL9440A	Yes	600	1.7
ISL9441	No	300	1.7
ISL9440B	Yes	300	Programmable
ISL9440C	Yes	600	Programmable

The ISL9440EVAL2Z is easy to set up to evaluate the performance of the ISL9440. Please refer to the "Electrical Specifications" table on page 2 for typical performance summary.

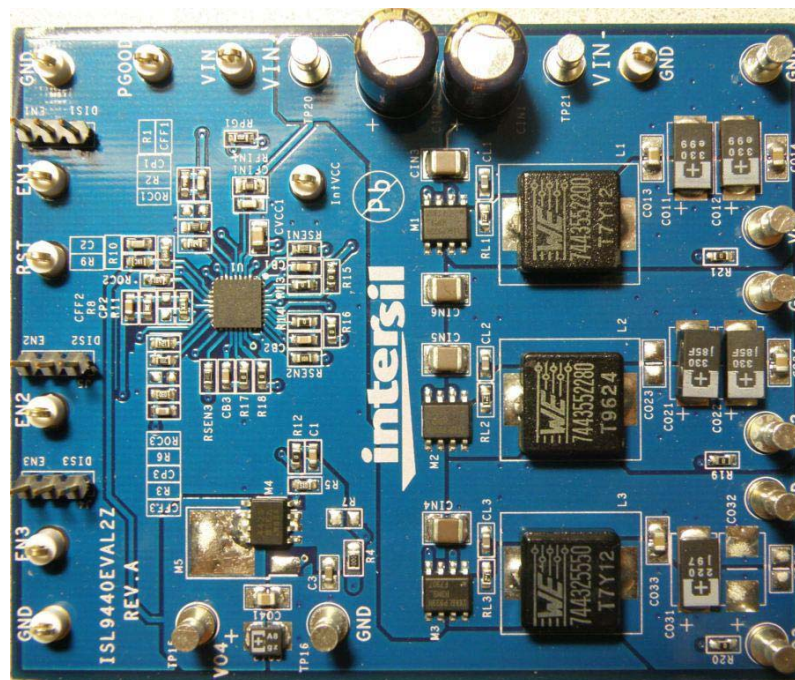


FIGURE 1. ISL9440EVAL2Z EVALUATION BOARD

## Electrical Specifications

Recommended operation conditions unless otherwise noted. Refer to the "Schematic" on page 7 and "Typical Evaluation Board Performance Curves" on page 4.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN}$	All outputs are in regulation	6.0	12	16	V
$V_{OUT1}$		1.45	1.50	1.54	V
$V_{OUT2}$		2.43	2.50	2.57	V
$V_{OUT3}$		4.85	5.0	5.15	V
$V_{OUT4}$		3.20	3.30	2.39	V
PWM1 Rated Current	$V_{IN} = 12V$ , $T_A = +25^\circ C$ , No forced airflow, All three PWM outputs are fully loaded		6	7	A
PWM2 Rated Current			6	7	A
PWM3 Rated Current			4	5	A
LDO Rated Current	$R_4 = 0\Omega$ , $R_7$ is not populated		0.8	1.0	A
$V_{OUT1}$ Peak-to-Peak Ripple	$V_{IN} = 12V$ , All three PWM outputs are fully loaded, Oscilloscope is with full bandwidth		29.4		mV <sub>P-P</sub>
$V_{OUT2}$ Peak-to-Peak Ripple			15.7		mV <sub>P-P</sub>
$V_{OUT3}$ Peak-to-Peak Ripple			31.4		mV <sub>P-P</sub>

## What's Inside

The evaluation board kit contains the following materials:

- The ISL9440EVAL2Z
- The ISL9440, ISL9440A, ISL9441 Datasheet [FN6383](#)
- This Evaluation Board Kit document (AN1550)

## Recommended Equipment

The following materials are recommended to perform testing:

- 0V to 20V Power Supply with at least 10A source current capability
- Three electronic loads capable of sinking current up to 7A
- Digital Multimeters (DMMs)
- 100MHz Quad-Trace Oscilloscope
- Signal Generator (for load transient tests)

## Quick Test Guide

1. Ensure that the circuit is correctly connected to the supply and electronic loads prior to applying any power. Please refer to Figure 2 for proper set-up.
2. Connect Jumpers  $J_3$ ,  $J_4$  and  $J_5$  in the ENx positions.
3. Turn on the power supply.
4. Adjust input voltage  $V_{IN}$  within the specified range and observe output voltage. The output voltage variation should be within 3%.
5. Adjust load current within the specified range and observe output voltage. The output voltage variation should be within 3%.
6. Use oscilloscope to observe output voltage ripple and phase node ringing. For accurate measurement, please follow setup shown in Figure 3.

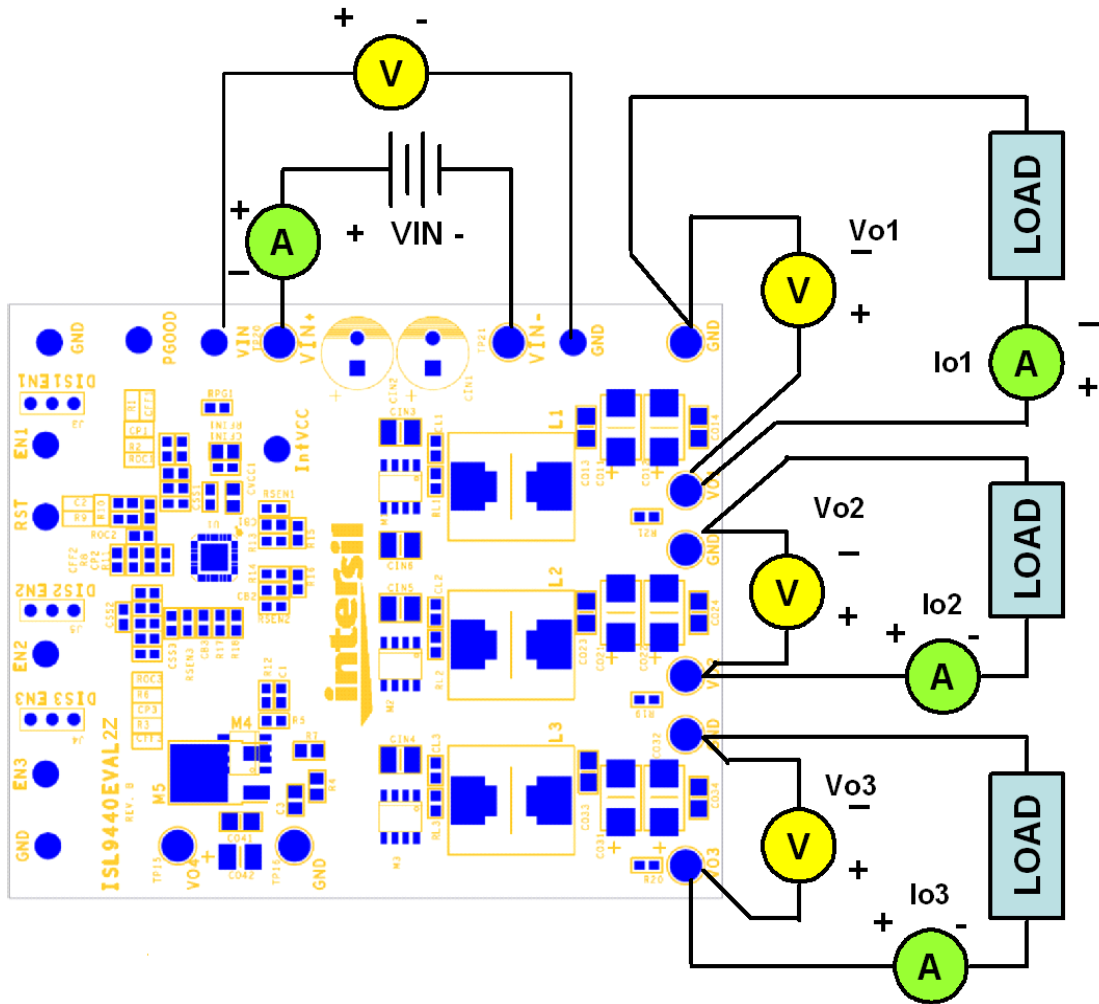


FIGURE 2. PROPER TEST SET-UP

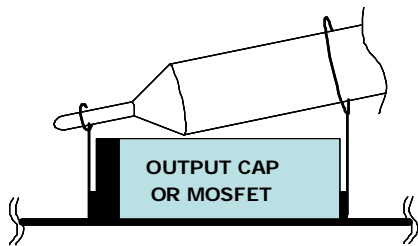


FIGURE 3. PROPER PROBE SET-UP TO MEASURE OUTPUT RIPPLE AND PHASE NODE RINGING

## Load Transient Circuit Set-up

1. Select a SOIC8 N-Channel MOSFET with VDS breakdown >20V.
2. Install the load transient circuit as indicated on the schematic. Refer to Figure 4 for detail.
3. R<sub>27</sub>, R<sub>22</sub> and R<sub>25</sub> are 10kΩ resistors for discharging the MOSFET gates.
4. R<sub>26</sub>, R<sub>23</sub> and R<sub>24</sub> are current sensing resistors to monitor the load step. For accurate measurement, please use 5% tolerance sensing resistor or better. To alleviate thermal stress, use 0.1Ω or smaller resistance. The resistance of the sensing resistors sets the current scale on the oscilloscope.
5. Apply pulse square waveform across R<sub>27</sub>, R<sub>22</sub> or R<sub>25</sub>. The duty cycle of the pulse waveform should be small (<5%) to limit thermal stress on current sensing resistor and the MOSFETs (M<sub>8</sub>, M<sub>6</sub> or M<sub>7</sub>).
6. The amplitude of the clock sets the current step amplitude. Adjust the clock amplitude and slew rate to set the current step and slew rate.
7. Monitor overshoot and undershoot at corresponding output.

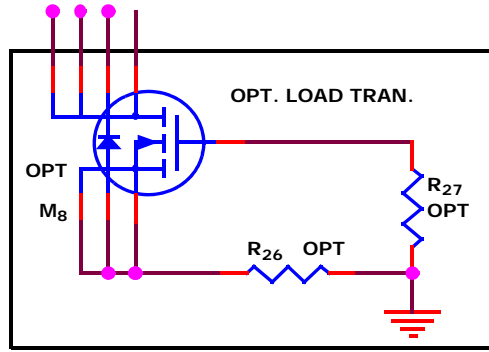


FIGURE 4. LOAD TRANSIENT CIRCUIT FOR PWM1

### Typical Evaluation Board Performance Curves

$V_{IN} = 12V$ ,  
Unless Otherwise Noted.

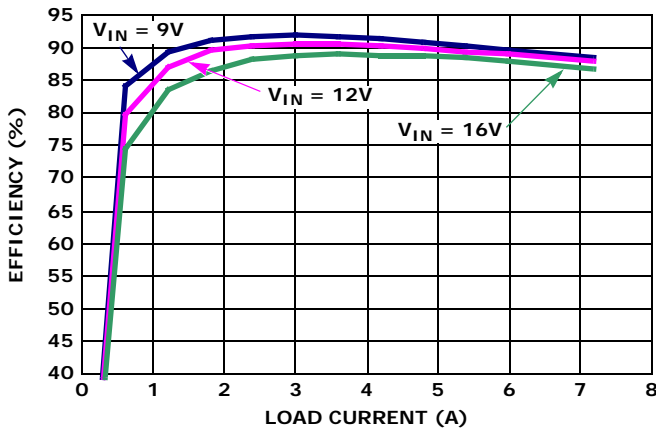


FIGURE 5. PWM1 EFFICIENCY vs LOAD ( $V_O = 1.5V$ )

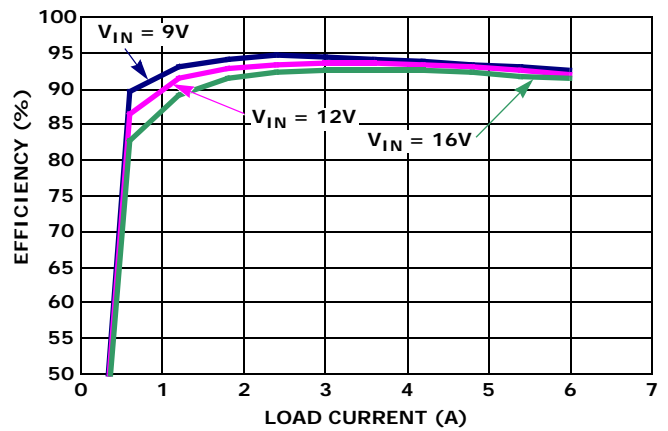


FIGURE 6. PWM2 EFFICIENCY vs LOAD ( $V_O = 2.5V$ )

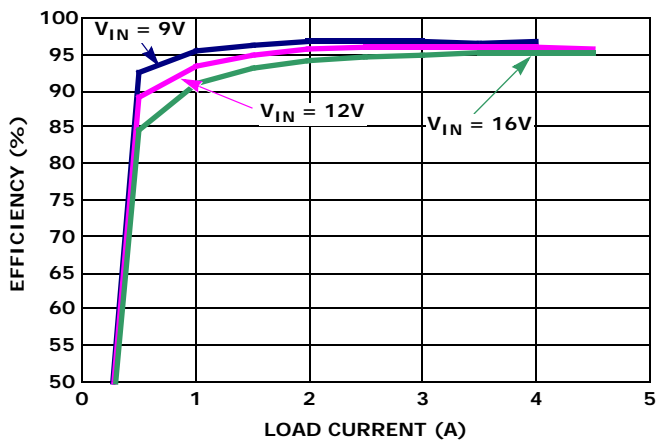


FIGURE 7. PWM3 EFFICIENCY vs LOAD ( $V_O = 5.0V$ )

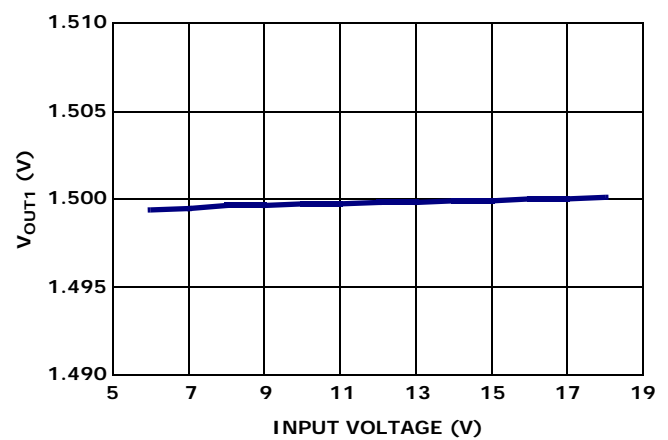


FIGURE 8. PWM1 LINE REGULATION ( $I_{O1} = I_{O2} = 6A$ ,  
 $I_{O3} = 4A$ )

**Typical Evaluation Board Performance Curves**  $V_{IN} = 12V$ ,  
Unless Otherwise Noted. (Continued)

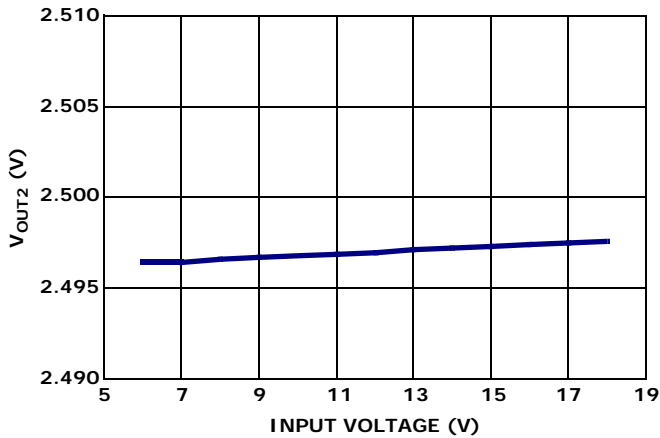


FIGURE 9. PWM2 LINE REGULATION ( $I_{O1} = I_{O2} = 6A$ ,  $I_{O3} = 4A$ )

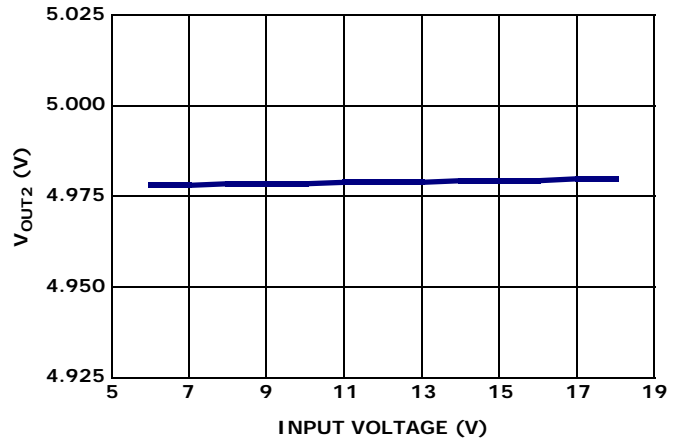


FIGURE 10. PWM3 LINE REGULATION ( $I_{O1} = I_{O2} = 6A$ ,  $I_{O3} = 4A$ )

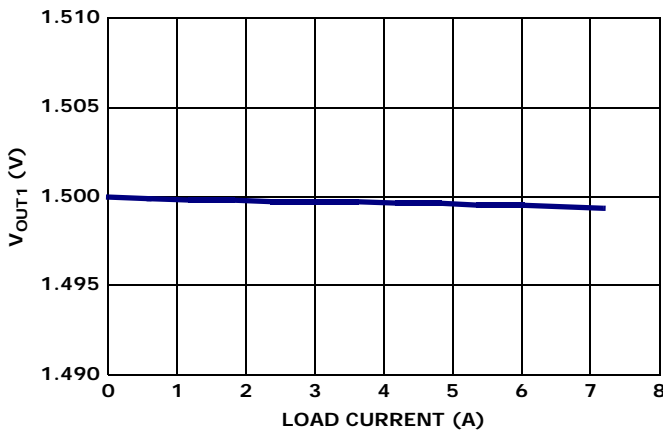


FIGURE 11. PWM1 LOAD REGULATION ( $V_{IN} = 12V$ ,  $I_{O2} = 6A$ ,  $I_{O3} = 4A$ )

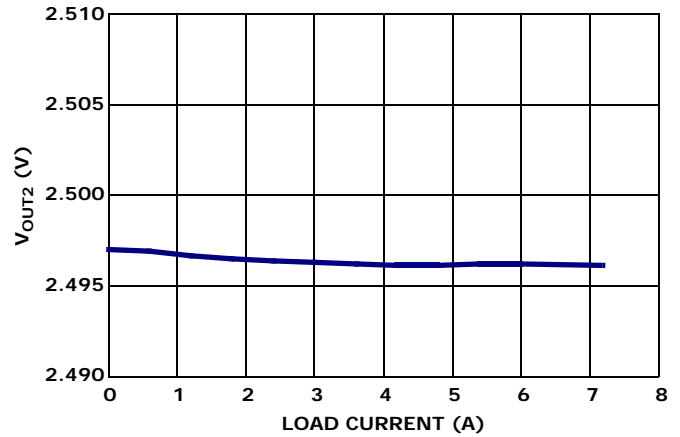


FIGURE 12. PWM2 LOAD REGULATION ( $V_{IN} = 12V$ ,  $I_{O1} = 6A$ ,  $I_{O3} = 4A$ )

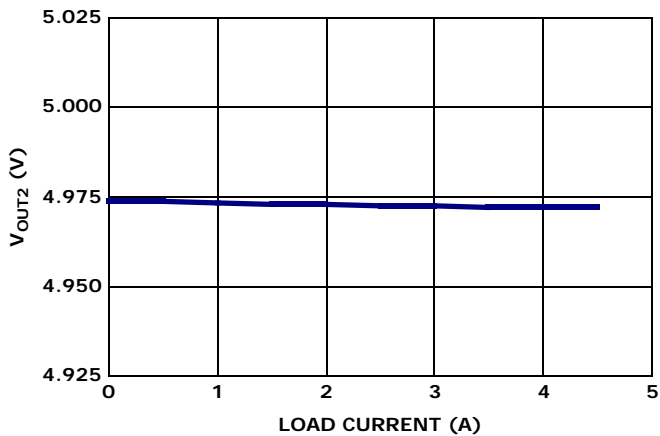


FIGURE 13. PWM3 LOAD REGULATION ( $V_{IN} = 12V$ ,  $I_{O1} = 6A$ ,  $I_{O2} = 3A$ )

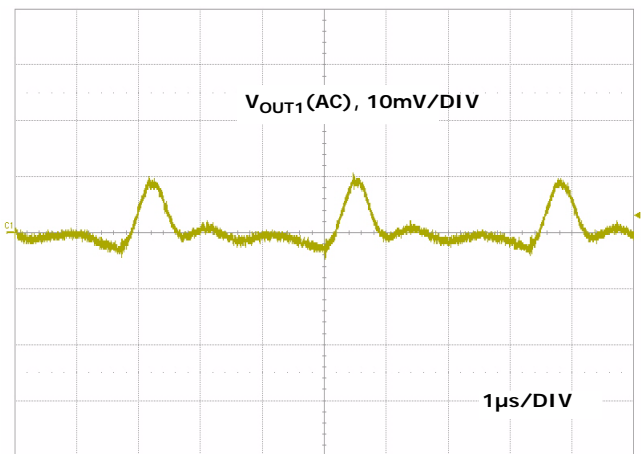


FIGURE 14. PWM1 OUTPUT RIPPLE UNDER MAX LOAD ( $V_{IN} = 12V$ ,  $I_{O1} = I_{O2} = 6A$ ,  $I_{O3} = 4A$ , FULL BANDWIDTH) AT  $V_O = 1.5V$

Typical Evaluation Board Performance Curves

$V_{IN} = 12V$ ,  
Unless Otherwise Noted. (Continued)

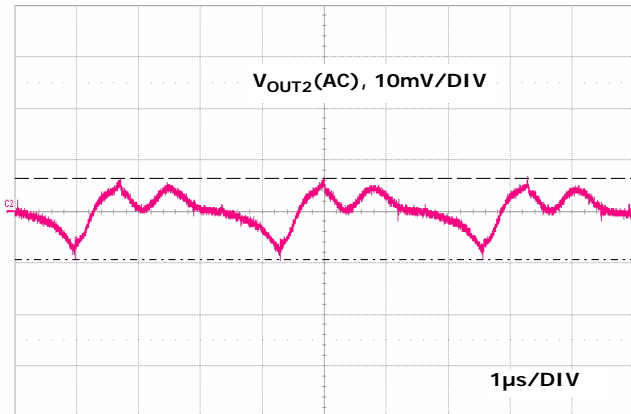


FIGURE 15. PWM2 OUTPUT RIPPLE UNDER MAX LOAD ( $V_{IN} = 12V$ ,  $I_{O1} = I_{O2} = 6A$ ,  $I_{O3} = 4A$ , FULL BANDWIDTH) AT  $V_O = 2.5V$

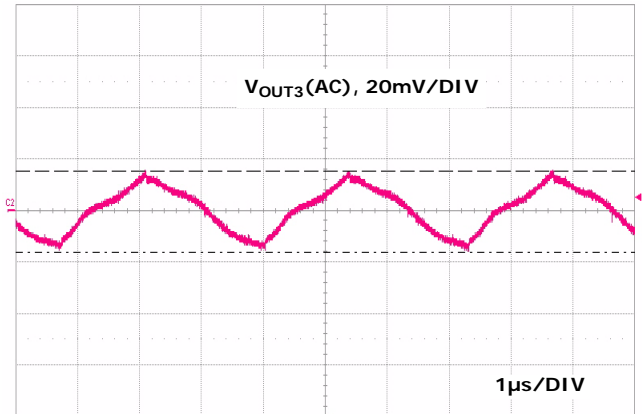


FIGURE 16. PWM3 OUTPUT RIPPLE UNDER MAX LOAD ( $V_{IN} = 12V$ ,  $I_{O1} = I_{O2} = 6A$ ,  $I_{O3} = 4A$ , FULL BANDWIDTH) AT  $V_O = 5V$

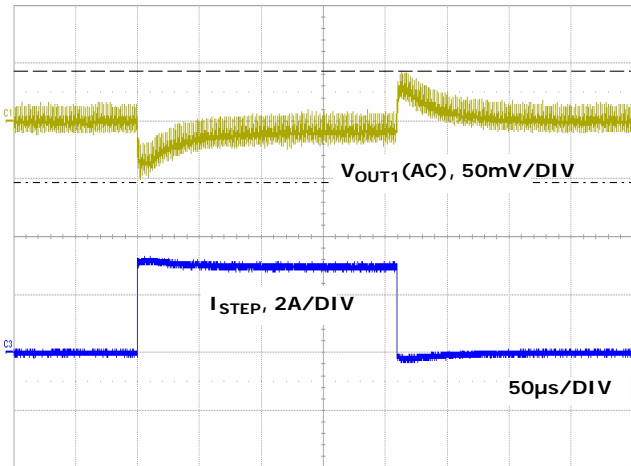


FIGURE 17. PWM1 LOAD TRANSIENT RESPONSE (LOAD STEP FROM 1.5A TO 4.5A) AT  $V_O = 1.5V$

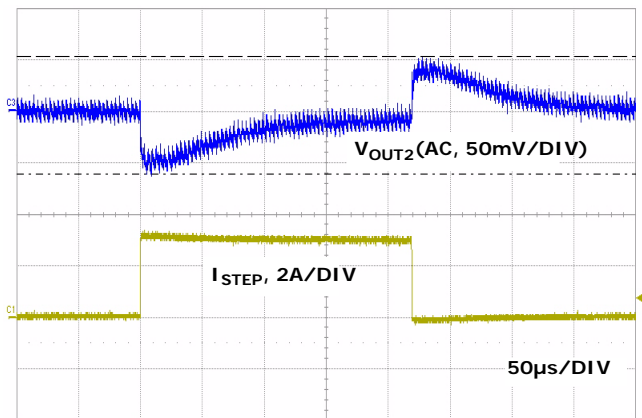


FIGURE 18. PWM2 LOAD TRANSIENT RESPONSE (LOAD STEP FROM 1.5A TO 4.5A) AT  $V_O = 2.5V$

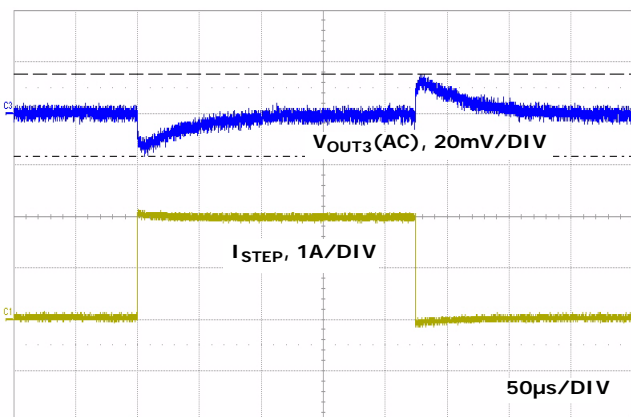


FIGURE 19. PWM3 LOAD TRANSIENT RESPONSE (LOAD STEP FROM 1A TO 3A) AT  $V_O = 5V$

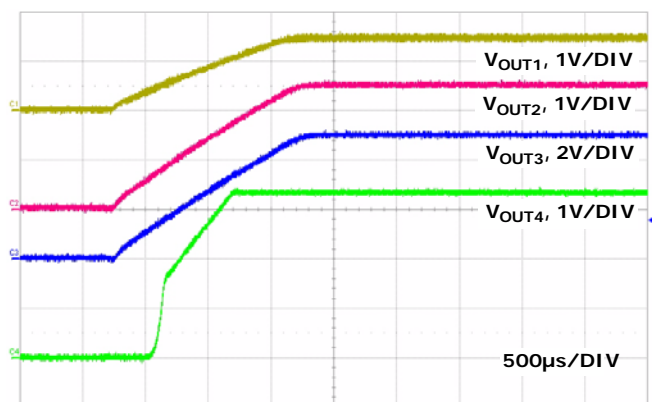


FIGURE 20. SOFT-START WAVEFORMS

# Schematic

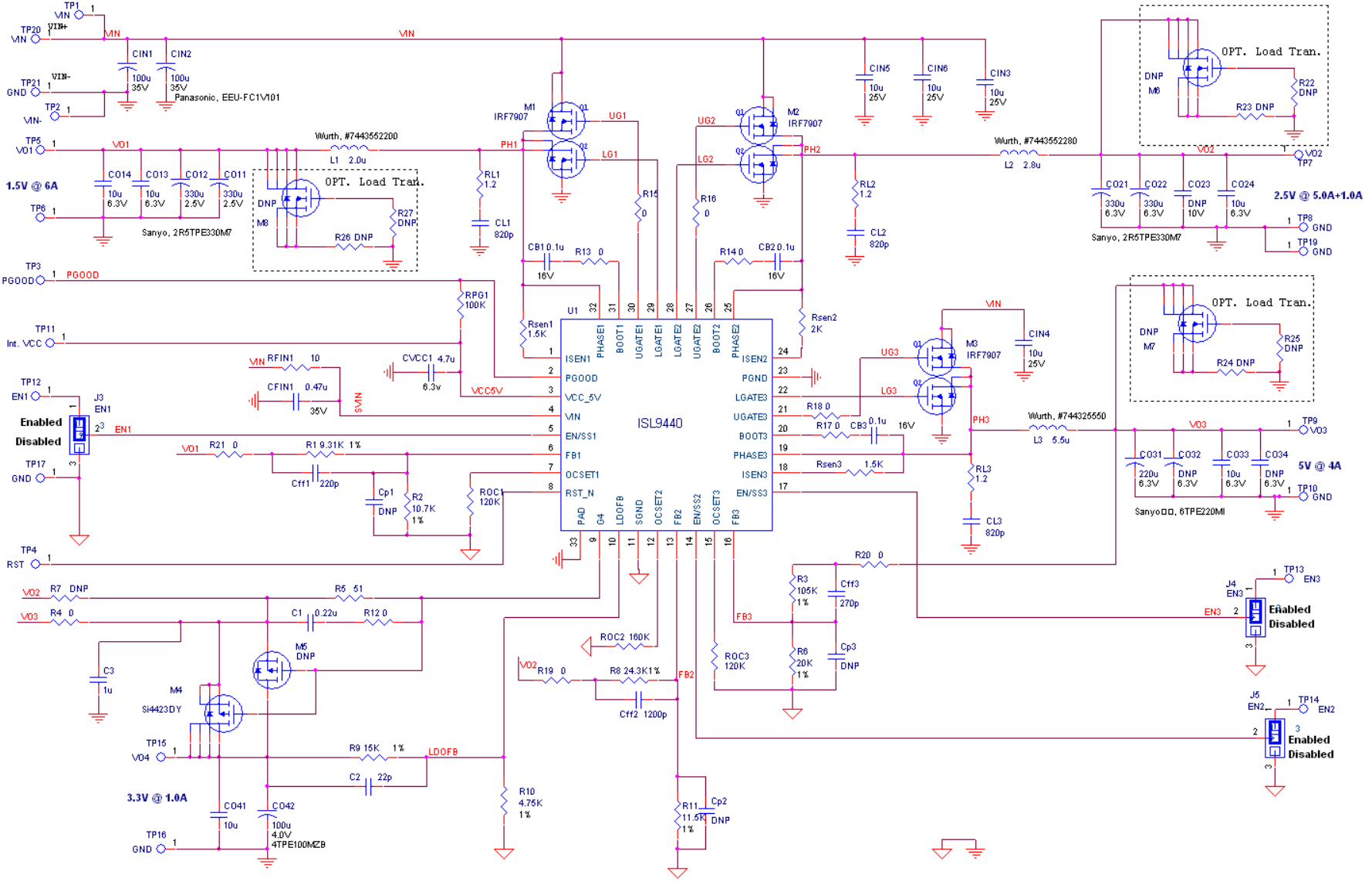




TABLE 2. BILL OF MATERIALS

ESSENTIAL COMPONENTS						
ITEM	QTY	PART REFERENCE	VALUE	DESCRIPTION	PART #	MANUFACTURER
1	3	CB1, CB2, CB3	0.1 $\mu$ F	CAP Ceramic X7R, 16V, SMD, 0603		Generic
2	1	CFIN1	0.47 $\mu$ F	CAP Ceramic Y5V, 50V, SMD, 0603		Generic
3	2	CIN1, CIN2	100 $\mu$ F	Alum. Elec. CAP 35V	EEU-FC1V101	Panasonic
4	4	CIN3, CIN4, CIN5, CIN6	10 $\mu$ F	CAP Ceramic X5R, 35V, SMD, 1210		Generic
5	3	CL1, CL2, CL3	820pF	CAP Ceramic X5R, 50V, SMD, 0603		Generic
6	2	CO11, CO12	330 $\mu$ F	POSCAP, 2.5V, SMD, D2E	2R5TPE330M7	Sanyo
7	5	CO13, CO14, CO24, CO33, CO41	10 $\mu$ F	CAP Ceramic X5R, 6.3V, SMD, 0805		Generic
8	2	CO21, CO22	330 $\mu$ F	POSCAP, 6.3V, SMD, D3L	6TPF330M9L	Sanyo
9	1	CO31	220uF	POSCAP, 6.3V, SMD	6TPE220MI	Sanyo
10	1	CO42	100 $\mu$ F	POSCAP, 4.0V, SMD, B	4TPE100MZB	Sanyo
11	1	CVCC1	4.7 $\mu$ F	CAP Ceramic X5R, 6.3V, SMD, 0805		Generic
12	1	Cff1	220pF	CAP Ceramic X7R, 50V, SMD, 0603		Generic
13	1	Cff2	1200pF	CAP Ceramic X7R, 50V, SMD, 0603		Generic
14	1	Cff3	270pF	CAP Ceramic X7R, 50V, SMD, 0603		
15	1	C1	0.22 $\mu$ F	CAP Ceramic X5R, 16V, SMD, 0603		Generic
16	1	C2	22pF	CAP Ceramic X5R, 16V, SMD, 0603		Generic
17	1	C3	1 $\mu$ F	CAP Ceramic X5R, 16V, SMD, 0603		Generic
18	1	L1	2.0 $\mu$ H	SHIELDED INDUCTOR	#744325550	Würth
19	1	L2	2.8 $\mu$ H	SHIELDED INDUCTOR	#7443552280	Würth
20	1	L3	5.5 $\mu$ H	SHIELDED INDUCTOR	#744325550	Würth
21	3	M1, M2, M3		Dual N MOSFET, 30V, SOIC8	IRF7907	International Rectifier
22	1	M4		P MOSFET, SOIC8	Si4423DY	Vishay
23	1	R <sub>FIN1</sub>	10 $\Omega$	RESISTOR, SMD, 0805, 10%		Generic
24	3	RL1, RL2, RL3	1.2 $\Omega$	RESISTOR, SMD, 0603, 10%		Generic
25	1	RPG1	100k $\Omega$	RESISTOR, SMD, 0603, 1%		Generic
26	1	ROC1, ROC3	120k $\Omega$	RESISTOR, SMD, 0603, 1%		Generic
27	1	ROC2	160k $\Omega$	RESISTOR, SMD, 0603, 1%		Generic
28	2	R <sub>SEN1</sub> , R <sub>SEN3</sub>	1.5k $\Omega$	RESISTOR, SMD, 0603, 1%		Generic
29	1	R <sub>SEN2</sub>	2k $\Omega$	RESISTOR, SMD, 0603, 1%		Generic
30	1	R1	9.31k $\Omega$	RESISTOR, SMD, 0603, 1%		Generic
31	1	R2	10.7k $\Omega$	RESISTOR, SMD, 0603, 1%		Generic
32	1	R3	105k $\Omega$	RESISTOR, SMD, 0603, 1%		Generic
33	1	R5	51 $\Omega$	RESISTOR, SMD, 0603, 1%		Generic
34	1	R6	20k $\Omega$	RESISTOR, SMD, 0603, 1%		Generic
35	1	R8	24.3k $\Omega$	RESISTOR, SMD, 0603, 1%		Generic
36	1	R9	15k $\Omega$	RESISTOR, SMD, 0603, 1%		Generic
37	1	R10	4.75k $\Omega$	RESISTOR, SMD, 0603, 1%		Generic



TABLE 2. BILL OF MATERIALS (Continued)

ESSENTIAL COMPONENTS						
ITEM	QTY	PART REFERENCE	VALUE	DESCRIPTION	PART #	MANUFACTURER
38	1	R11	11.5kΩ	RESISTOR, SMD, 0603, 1%		Generic
39	1	U1		QUAD OUTPUT CONTROLLER	ISL9440IRZ	Intersil
OPTIONAL COMPONENTS OR RESISTOR JUMPERS						
ITEM	QTY	REFERENCE	VALUE	DESCRIPTION	PART #	MANUFACTURER
40	10	R4, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21	0	RESISTOR Jumpers, SMD, 0603, 10%		Generic
41	2	CO23, CO32 CO34	DNP			
42	3	Cp1, Cp2, Cp3	DNP			
42	1	M5	DNP	P MOSFET TO-252		
43	3	M6, M7, M8	DNP	N MOSFET		
44	4	R7, R22, R25, R27	DNP	RESISTOR, SMD, 0603		
45	3	R23, R24, R26	DNP	RESISTOR, SMD, 1206		
EVALUATION BOARD HARDWARE						
ITEM	QTY	REFERENCE	VALUE	DESCRIPTION	PART #	MANUFACTURER
46	3	J3, J4, J5		3 Head Jumper	68000-236HLF	Generic
47	11	TP1, TP2, TP3, TP4, TP6, TP17, TP11, TP12, TP13, TP14, TP7		TEST POINT	5007	Keystone
48	9	TP8, TP10, TP16, TP19, TP21, TP9, TP5, TP15, TP20	GND	TURRET	1514-2	Keystone

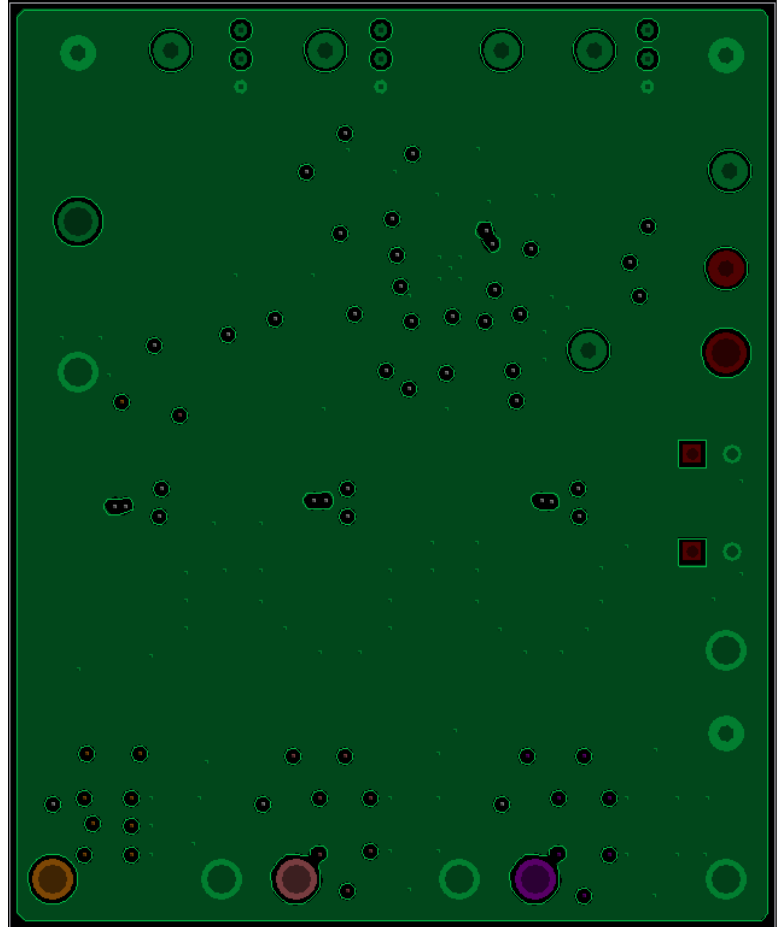


FIGURE 22. SECOND LAYER (SOLID GROUND)

# ISL9440EVAL2Z PCB Layout

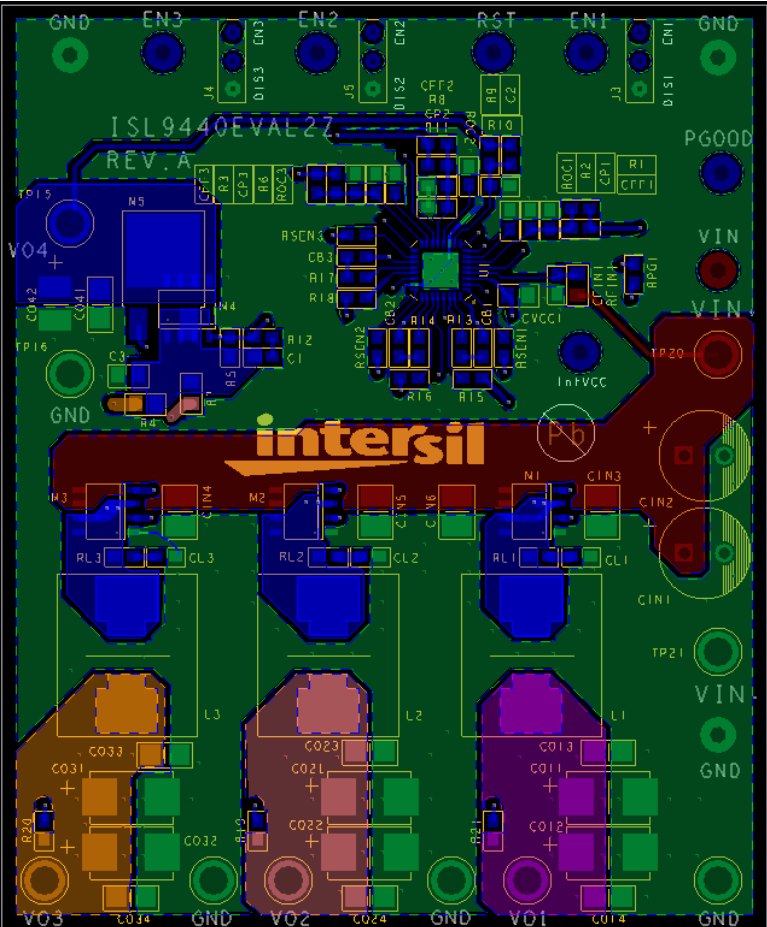


FIGURE 21. TOP LAYER

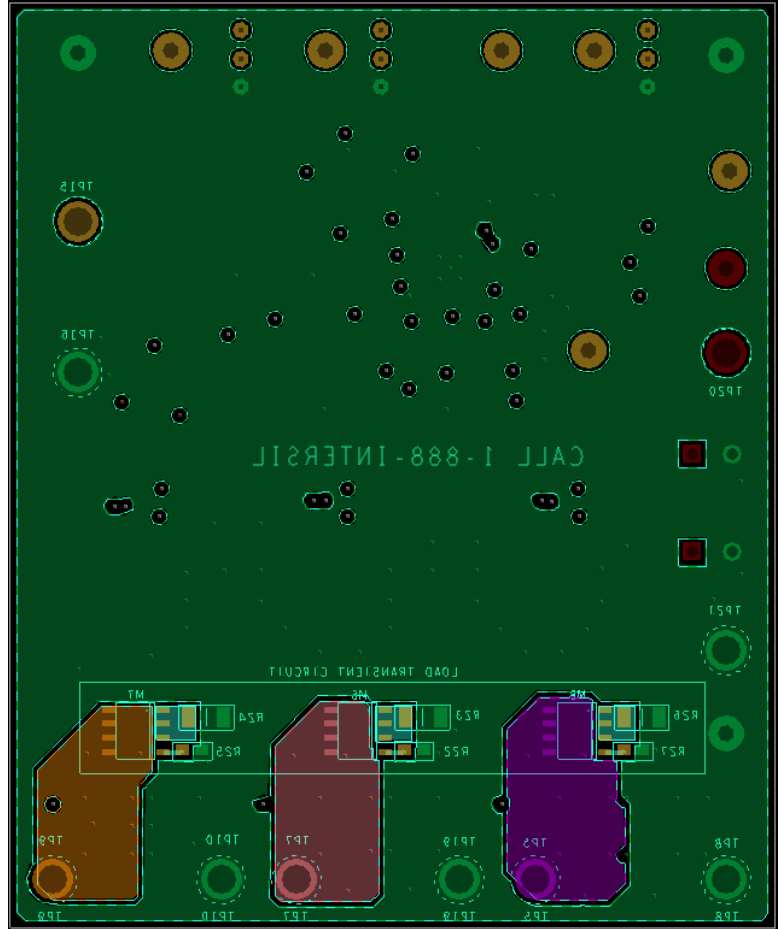


FIGURE 24. BOTTOM LAYER

# ISL9440EVAL2Z PCB Layout (Continued)

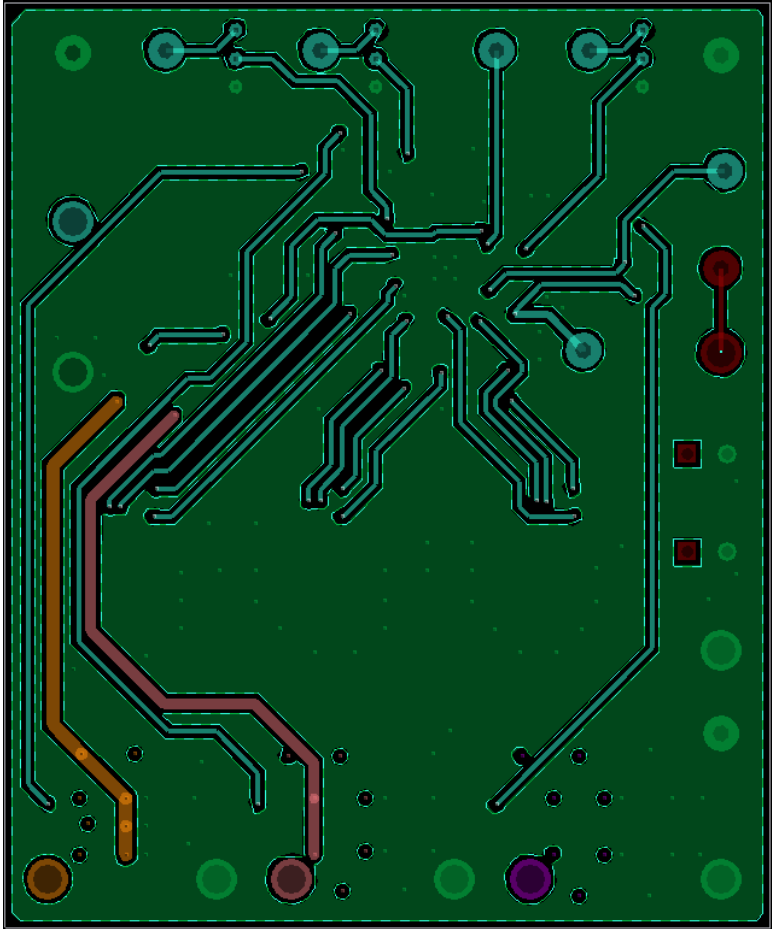


FIGURE 23. THIRD LAYER