ISL95311

Digitally Controlled Potentiometer (XDCP™),
Terminal Voltage 0V to 13.2V, 128 Taps I^2C Interface

FN8084
Rev 2.00
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The Intersil ISL95311 is a digitally controlled potentiometer (XDCP). The device consists of a resistor array, wiper switches, a control section, and nonvolatile memory. The wiper position is controlled by an I^2C interface.

The potentiometer is implemented by a resistor array composed of 127 resistive elements and a wiper switching network. Between each element and at either end are tap points accessible to the wiper terminal. The wiper of the potentiometer has an associated volatile Wiper Counter Register (WR) and a non-volatile Initial Value Register (IVR) that can be directly written to and read by the user. The contents of the WR controls the position of the wiper on the resistor array through the switches. At power-up, the device recalls the contents of the IVR to the corresponding WR.

The device can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications, including:

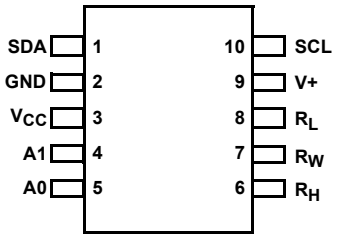
- LCD contrast control
- Parameter and bias adjustments
- Industrial and automotive control
- Mechanical pot replacement

Features

- Non-volatile solid-state potentiometer
- I^2C serial interface
- DCP terminal voltage, 0V to +13.2V
- 128 wiper tap points - 0.8% resolution
  - Wiper position stored in nonvolatile memory and recalled on power-up
- 127 resistive elements
  - Temperature compensated
  - Low wiper resistance 70Ω typical @ 3.3V
- Low power CMOS
  - Standby current, 2µA @ V_{CC} = +3.6V
- High reliability
  - Endurance, 200,000 data changes per bit
  - Register data retention 50 years @ T ≤ +75°C
- R_{TOTAL} values = 10kΩ, 50kΩ
- 10 Ld MSOP package
- Pb-free (RoHS compliant)

Pinout

ISL95311
(10-LD MSOP)
TOP VIEW



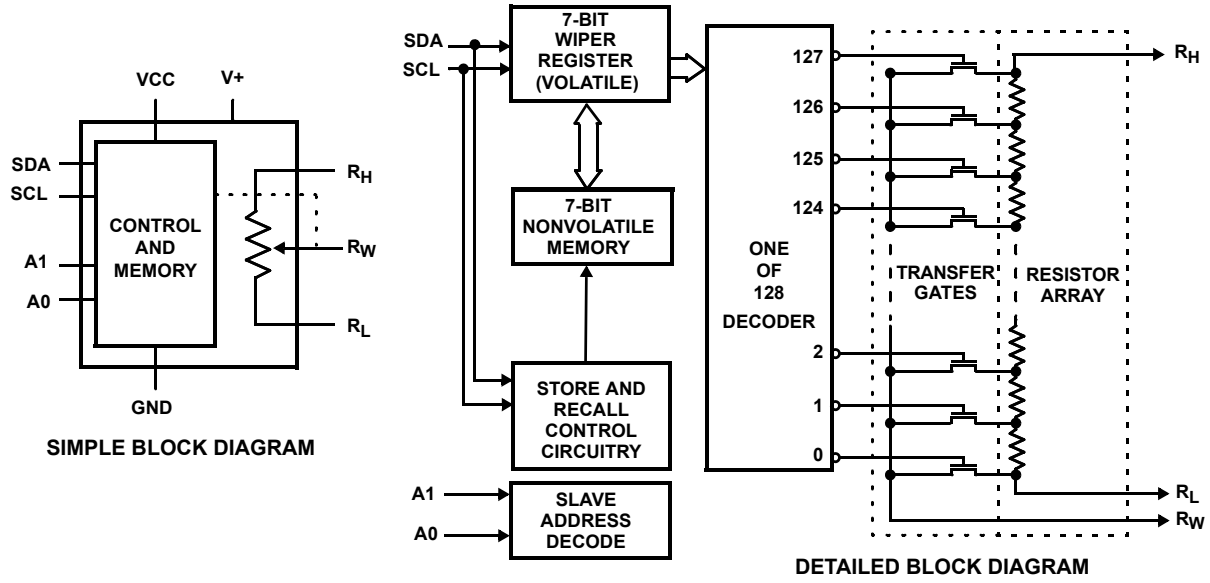
Ordering Information

PART NUMBER (Note)	PART MARKING	RESISTANCE OPTION (Ω)	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL95311WIU10Z	AJE	10k	-40 to +85	10-Ld MSOP	M10.118

Add “-TK” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Block Diagram



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	SDA	Data I/O for I^2C serial interface; it has an open drain output and may be wire-or'd with other open drain active low outputs
2	GND	Ground
3	VCC	Positive logic supply voltage
4	A1	Address select pin used to set the slave address for the I^2C serial interface
5	A0	Address select pin used to set the slave address for the I^2C serial interface
6	R_H	A fixed terminal for one end of the potentiometer resistor
7	R_W	The wiper terminal, which is equivalent to the movable terminal of a potentiometer
8	R_L	A fixed terminal for one end of the potentiometer resistor
9	V+	Positive bias voltage for the potentiometer wiper control
10	SCL	Clock input for the I^2C serial interface

Absolute Maximum Ratings

Storage temperature . . . . . -65°C to +150°C
Voltage on SDA, SCL, A0, A1
with respect to GND . . . . . -0.3V to V_{CC} + 0.3V
Voltage on V+ (referenced to GND) . . . . . +13.2V
$\Delta V = |V_{(RH)} - V_{(RL)}|$ . . . . . V+
R_H, R_L, R_W . . . . . V+
I_W (10s) . . . . . ±6mA
V_{CC} . . . . . -0.3V to +6V
Power rating of DCP 20mW

Recommended Operating Conditions

Temperature Range (Industrial) . . . . . -40°C to +85°C
V_{CC} . . . . . 2.7V to 5.5V
V+ . . . . . 8.0V to 13.2V
Wiper current of DCP . . . . . ±3.0mA
Pb-free reflow profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Analog Specifications

Over recommended operating conditions, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 15)	TYP (Note 1)	MAX (Note 15)	UNIT
R_{TOTAL}	R_H to R_L Resistance	W option		10		kΩ
		U option		50		kΩ
	R_H to R_L Resistance Tolerance		-20		+20	%
V_{RH}	R_H Terminal Voltage	V_{RL} = 0V	0		V+	V
R_W	Wiper Resistance	V+ = 12.0V, wiper current = V+/R_{TOTAL}		70	200	Ω
$C_H/C_L/C_W$	Potentiometer Capacitance			10/10/25		pF
I_{LkgDCP}	Leakage on DCP Pins	Voltage at pin from GND to V+		0.1	1	µA
VOLTAGE DIVIDER MODE (0V @ R_L; V+ @ R_H; measured at R_W, unloaded)						
INL (Note 6)	Integral Non-Linearity	W and U option	-1		1	LSB (Note 2)
DNL (Note 5)	Differential Non-Linearity	W and U option	-0.5		0.5	LSB (Note 2)
ZSerror (Note 3)	Zero-Scale Error	W option	0	1	7	LSB (Note 2)
		U option	0	0.5	2	
FSerror (Note 4)	Full-Scale Error	W option	-7	-1	0	LSB (Note 2)
		U option	-2	-0.5	0	
TC_V (Note 7)	Ratiometric Temperature Coefficient	DCP register set to 40 hex		±4		ppm/°C
RESISTOR MODE (Measurements between R_W and R_L with R_H not connected, or between R_W and R_H with R_L not connected)						
RINL (Note 11)	Integral Non-Linearity	DCP register set between 20 hex and 7F hex; monotonic over all tap positions	-1.0		1.0	MI (Note 8)
RDNL (Note 10)	Differential Non-Linearity	W and U option	-0.5		0.5	MI (Note 8)
Roffset (Note 9)	Offset	DCP Register set to 00 hex, W option	0	1	7	MI (Note 8)
		DCP Register set to 00 hex, U option	0	0.5	2	
TC_R (Note 12)	Resistance Temperature Coefficient	DCP register set between 20 hex and 7F hex		±45		ppm/°C

Operating Specifications Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 15)	TYP (Note 1)	MAX (Note 15)	UNIT
I_{CC1}	V_{CC} Supply Current, Volatile Write/read	f_{SCL} = 400kHz; SDA = Open; (for I^2C, active, read, and volatile write states only)			1	mA
I_{CC2}	V_{CC} Supply Current, Nonvolatile Write	f_{SCL} = 400kHz; SDA = Open; (for I^2C, active, nonvolatile write states only)			3	mA
I_{SB}	V_{CC} Current, Standby	V_{CC} = +5.5V, I^2C interface in standby state			5	µA
		V_{CC} = +3.6V, I^2C interface in standby state			2	µA
I_{V+}	V+ Bias Current	V+ = 13.2V, V_{CC} = +5.5V			1	µA
I_{LkgDig}	Leakage Current, at Pins SDA, SCL, A0, and A1 Pins	Voltage at pin from GND to V_{CC}	-10		10	µA
t_{DCP}	DCP Wiper Response Time	SCL falling edge of last bit of DCP data byte to wiper change			1	µs
Vpor	Power-On Recall Voltage	V_{CC} range at which memory recall occurs	1.5	1.8	2.6	V
V_{CC}Ramp	V_{CC} Ramp Rate		0.2			V/ms
t_D	Power-Up Delay	V_{CC} above Vpor, to DCP initial value register recall completed, and I^2C Interface in standby state			3	ms
EEPROM SPECS						
	EEPROM Endurance		200,000			Cycles
	EEPROM Retention	Temperature ≤ +75°C	50			Years
SERIAL INTERFACE SPECS						
V_{IL}	A0, A1, SDA, and SCL Input Buffer LOW Voltage		-0.3		0.3* V_{CC}	V
V_{IH}	A0, A1, SDA, and SCL Input Buffer HIGH Voltage		0.7* V_{CC}		V_{CC}+ 0.3	V
Hysteresis	SDA and SCL Input Buffer Hysteresis		0.05* V_{CC}			V
V_{OL}	SDA Output Buffer LOW Voltage, Sinking 4mA		0		0.4	V
Cpin	A0, A1, SDA, and SCL Pin Capacitance			10		pF
f_{SCL}	SCL Frequency				400	kHz
t_{IN}	Pulse Width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed			50	ns
t_{AA}	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of V_{CC}, until SDA exits the 30% to 70% of V_{CC} window			900	ns
t_{BUF}	Time the Bus Must be Free Before the Start of a New Transmission	SDA crossing 70% of V_{CC} during a STOP condition, to SDA crossing 70% of V_{CC} during the following START condition	1300			ns
t_{LOW}	Clock LOW Time	Measured at the 30% of V_{CC} crossing	1300			ns
t_{HIGH}	Clock HIGH Time	Measured at the 70% of V_{CC} crossing	600			ns
$t_{SU:STA}$	START Condition Set-up Time	SCL rising edge to SDA falling edge; both crossing 70% of V_{CC}	600			ns
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_{CC} to SCL falling edge crossing 70% of V_{CC}	600			ns
$t_{SU:DAT}$	Input Data Set-up Time	From SDA exiting the 30% to 70% of V_{CC} window, to SCL rising edge crossing 30% of V_{CC}	100			ns

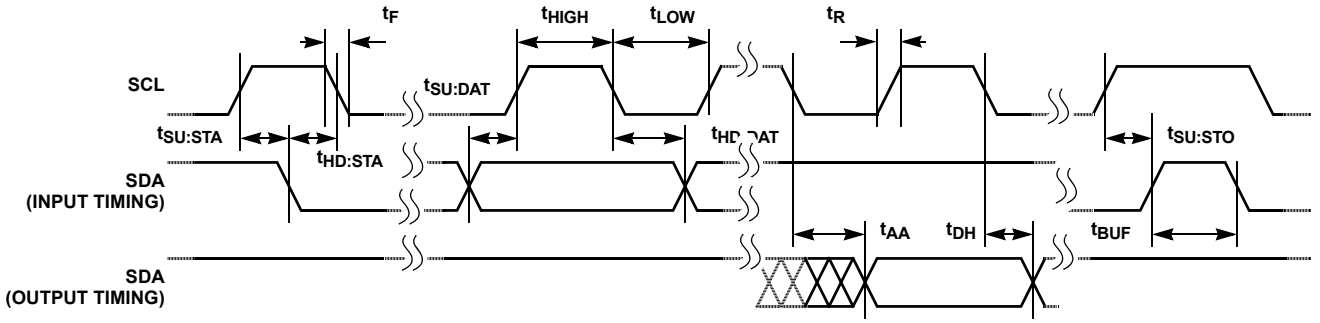
Operating Specifications Over the recommended operating conditions unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 15)	TYP (Note 1)	MAX (Note 15)	UNIT
$t_{HD:DAT}$	Input Data Hold Time	From SCL rising edge crossing 30% of V_{CC} to SDA entering the 30% to 70% of V_{CC} window	0			ns
$t_{SU:STO}$	STOP Condition Set-up time	From SCL rising edge crossing 70% of V_{CC}, to SDA rising edge crossing 30% of V_{CC}	600			ns
$t_{HD:STO}$	STOP Condition Hold Time	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{CC}	600			ns
t_{DH}	Output Data Hold Time	From SCL falling edge crossing 30% of V_{CC}, until SDA enters the 30% to 70% of V_{CC} window	0			ns
t_R (Note 14)	SDA and SCL Rise Time	From 30% to 70% of V_{CC}	20 + 0.1 * Cb		250	ns
t_F (Note 14)	SDA and SCL Fall Time	From 70% to 30% of V_{CC}	20 + 0.1 * Cb		250	ns
Cb (Note 14)	Capacitive Loading of SDA or SCL	Total on-chip and off-chip	10		400	pF
Rpu (Note 14)	SDA and SCL Bus Pull-Up Resistor Off-Chip	Maximum is determined by t_R and t_F. For Cb = 400pF, max is about 2kΩ~2.5kΩ. For Cb = 40pF, max is about 15kΩ~20kΩ.	1			kΩ
t_{WP} (Notes 13)	Non-Volatile Write Cycle Time			12	20	ms
$t_{SU:A}$	A0, A1 Set-up Time	Before START condition	600			ns
$t_{HD:A}$	A0, A1 Hold Time	After STOP condition	600			ns

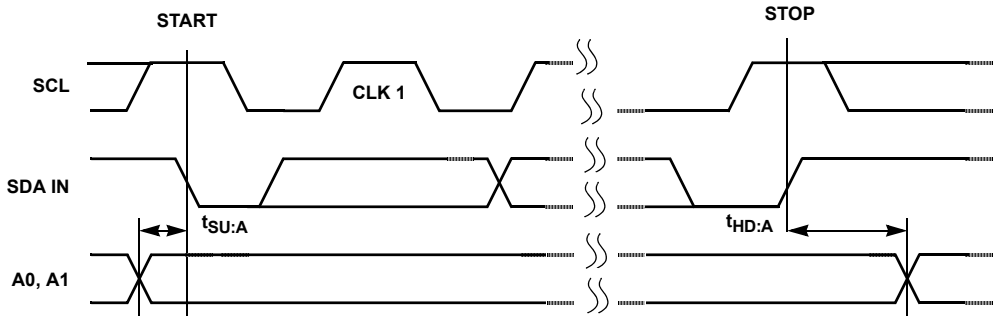
NOTES:

1. Typical values are for T_A = +25°C and 3.3V supply voltage.
2. LSB: $[V(R_W)_{127} – V(R_W)_0]/127$. $V(R_W)_{127}$ and $V(R_W)_0$ are $V(R_W)$ for the DCP register set to 7F hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
3. ZS error = $V(R_W)_0$/LSB.
4. FS error = $[V(R_W)_{127} – V+]$/LSB.
5. DNL = $[V(R_W)_i – V(R_W)_{i-1}]$/LSB-1, for i = 1 to 127. i is the DCP register setting.
6. INL = $V(R_W)_i – (i • LSB – V(R_W)_0)$ for i = 1 to 127.
7. $$TC_V = \frac{Max(V(RW)_i) - Min(V(RW)_i)}{[Max(V(RW)_i) + Min(V(RW)_i)]/2} \times \frac{10^6}{125°C}$$
   for i = 16 to 120 decimal, T = -40°C to 85°C. Max( ) is the maximum value of the wiper voltage and Min ( ) is the minimum value of the wiper voltage over the temperature range.
8. MI = $|R_{127} – R_0|/127$. R_{127} and R_0 are the measured resistances for the DCP register set to 7F hex and 00 hex respectively.
9. Roffset = R_0/MI, when measuring between R_W and R_L.
   Roffset = R_{127}/MI, when measuring between R_W and R_H.
10. RDNL = $(R_i – R_{i-1})$/MI, for i = 16 to 127.
11. RINL = $[R_i – (MI • i) – R_0]$/MI, for i = 16 to 127.
12. $$TC_R = \frac{[Max(Ri) - Min(Ri)]}{[Max(Ri) + Min(Ri)]/2} \times \frac{10^6}{125°C}$$
    for i = 16 to 127, T = -40°C to +85°C. Max( ) is the maximum value of the resistance and Min ( ) is the minimum value of the resistance over the temperature range.
13. t_{WP} is the minimum cycle time to be allowed for any non-volatile Write by the user, unless Acknowledge Polling is used. It is the time from a valid STOP condition at the end of a Write sequence of a I^2C serial interface Write operation, to the end of the self-timed internal non-volatile write cycle.
14. Recommended operating limits and are not production tested.
15. Parts are 100% tested at +85°C. Over temperature limits established by characterization and are not production tested.

SDA vs SCL Timing



A0, A1 Pin Timing



Pin Descriptions

Potentiometer Pins

R_H and R_L

R_L and R_H are referenced to the relative position of the wiper and not the voltage potential on the terminals. With WR set to 127, the wiper will be closest to R_H, and with the WR set to 00, the wiper is closest to R_L.

R_W

R_W is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the WR.

Bus Interface Pins

SERIAL DATA INPUT/OUTPUT (SDA)

The SDA is a bidirectional serial data input/output pin for the I^2C interface. It receives device address, operation code, wiper register address and data from a I^2C external master device at the rising edge of the serial clock SCL, and it shifts out data after each falling edge of the serial clock SCL.

SDA requires an external pull-up resistor, since it's an open drain input/output.

SERIAL CLOCK (SCL)

This input is the serial clock of the I^2C serial interface.

SCL requires an external pull-up resistor, since it's an open drain input.

DEVICE ADDRESS (A1–A0)

The Address inputs are used to set the least significant 2 bits of the 8-bit I^2C interface slave address. A match in the slave address serial data stream must be made with the Address input pins in order to initiate communication with the ISL95311. A maximum of four ISL95311 devices may occupy the I^2C serial bus.

Principles of Operation

The ISL95311 is an integrated circuit incorporating one DCP with their associated register, non-volatile memory, and a I^2C serial interface providing direct communication between a host and the potentiometers and memory. The resistor array is comprised of 127 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch between that point and the wiper.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

The electronic switches on the device operate in a "make before break" mode when the wiper changes tap positions.

When the device is powered-down, the last wiper position stored will be maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the wiper is set to the value last stored.

On applying power to the ISL95311, the V_{CC} supply should have a monotonic ramp to the specified operating voltage. It is important that once V_{CC} reaches 1V that it increases to at least 2.5V in less than 7.5ms (0.2V/ms). The ramp rate before and after these thresholds is not important.

V_{CC} must be applied prior to, or simultaneously, with V+. Under no condition should V+ be applied without V_{CC}. While the sequence of applying V+ and V_{CC} to the ISL95311 does not affect the proper recall of the wiper position, applying V+ before V_{CC} powers the electronic switches of the DCP before the electronic switch control signals are applied. This can result in multiple electronic switches being turned on, which could load the power supply and cause brief, unexpected potentiometer wiper settings.

To prevent unknown wiper positions on the ISL95311 on power-down, it is recommended that V+ turn off before or simultaneously with V_{CC}. If V+ remains on after V_{CC} turns off, the wiper position can remain unchanged from its previous setting or it can go to an undefined state.

DCP Description

The DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of the DCP are equivalent to the fixed terminals of a mechanical potentiometer (R_H and R_L pins). The R_W pin is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by a 7-bit volatile Wiper Register (WR). When the WR contains all zeroes (00h), the wiper terminal (R_W) is closest to its “Low” terminal (R_L). When the WR contains all ones (7Fh), the wiper terminal (R_W) is closest to its “High” terminal (R_H). As the value of the WR increases from all zeroes (00h) to all ones (7Fh), the wiper moves monotonically from the position closest to R_L to the position closest to R_H. At the same time, the resistance between R_W and R_L increases monotonically, while the resistance between R_H and R_W decreases monotonically.

While the ISL95311 is being powered up, the WR is reset to 20h (64 decimal), which locates the R_W at the center between R_L and R_H. Soon after the power supply voltage becomes large enough for reliable non-volatile memory reading, the ISL95311 reads the value stored on a non-volatile Initial Value Register (IVR) and loads it into the WR.

The WR and IVR can be read from or written to directly using the I^2C serial interface as described in the following sections.

Memory Description

The ISL95311 contains 1 non-volatile byte know as the Initial Value Register (IVR). It is accessed by the I^2C interface operations with Address 00h. The IVR contains the value which is loaded into the Volatile Wiper Register (WR) at power-up.

The volatile WR, and the non-volatile IVR of a DCP are accessed with the same address.

The Access Control Register (ACR) determines which word at address 00h is accessed (IVR or WR). The volatile ACR must be set as follows:

When the ACR is all zeroes, which is the default at power-up:

- A read operation to address 0 outputs the value of the non-volatile IVR.
- A write operation to address 0 writes the identical values to the WR and IVR of the DCP.
- When the ACR is 80h:
- A read operation to address 0 outputs the value of the volatile WR.
- A write operation to address 0 only writes to the volatile WR.

It is not possible to write to an IVR without writing the same value to its WR.

00h and 80h are the only values that should be written to address 2. All other values are reserved and must not be written to address 2.

TABLE 1. MEMORY MAP

ADDRESS	NON-VOLATILE	VOLATILE
2	-	ACR
1	Reserved	
0	IVR	WR

WR: Wiper Register, IVR: Initial value Register.

The ISL95311 is pre-programmed with 40h in the IVR.

I^2C Serial Interface

The ISL95311 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL95311 operates as a slave device in all applications.

All communication over the I^2C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 1). On power-up of the ISL95311, the SDA pin is in the input mode.

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while

SCL is HIGH. The ISL95311 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 1). A START condition is ignored during the power-up sequence and during internal non-volatile write cycles.

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 1). A STOP condition at the end of a read operation, or at the end of a write operation to volatile bytes only places the device in its standby mode. A STOP condition during a write operation to a non-volatile byte, initiates an internal non-volatile write cycle. The device enters its standby state when the internal non-volatile write cycle is completed.

An ACK, Acknowledge, is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 2).

The ISL95311 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL95311 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation

A valid Identification Byte contains 01010 as the five MSBs, and the following two bits matching the logic values present at pins A1, and A0. The LSB is in the Read/$\overline{\text{Write}}$ bit. Its value is “1” for a Read operation, and “0” for a Write operation (see Table 2.)

					LOGIC VALUES AT PINS A1, AND A0 RESPECTIVELY		
0	1	0	1	0	A1	A0	R/$\overline{\text{W}}$
(MSB)							(LSB)

TABLE 2. DENTIFICATION BYTE FORMAT

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition (see Figure 3). After each of the three bytes, the ISL95311 responds with an ACK. At this time, if the Data Byte is to be written only to volatile registers, then the device enters its standby state. If the Data Byte is to be written also to non-volatile memory, the ISL95311 begins its internal write cycle to non-volatile memory. During the internal non-volatile write cycle, the device ignores transitions at the SDA and SCL pins, and the SDA output is at a high impedance state. When the internal non-volatile write cycle is completed, the ISL95311 enters its standby state.

The byte at address 02h determines if the Data Byte is to be written to volatile and/or non-volatile memory (see “Memory Description” on page 7).

Data Protection

A STOP condition also acts as a protection of non-volatile memory. A valid Identification Byte, Address Byte, and total number of SCL pulses act as a protection of both volatile and non-volatile registers. During a Write sequence, the Data Byte is loaded into an internal shift register as it is received. If the Address Byte is 0 or 2, the Data Byte is transferred to the Wiper Register (WR) or to the Access Control Register respectively, at the falling edge of the SCL pulse that loads the last bit (LSB) of the Data Byte. If the Address Byte is 0, and the Access Control Register is all zeros (default), then the STOP condition initiates the internal write cycle to non-volatile memory.

Read Operation

A Read operation consists of a three byte instruction followed by one or more Data Bytes (See Figure 4). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/$\overline{\text{W}}$ bit set to “0”, an Address Byte, a second START, and a second Identification byte with the R/$\overline{\text{W}}$ bit set to “1”. After each of the three bytes, the ISL95311 responds with an ACK; then the ISL95311 transmits the Data Byte. The master then terminates the read operation (issuing a STOP condition) following the last bit of the Data Byte (See Figure 4).

The byte at address 02h determines if the Data Bytes being read are from volatile or non-volatile memory. (see “Memory Description” on page 7.)

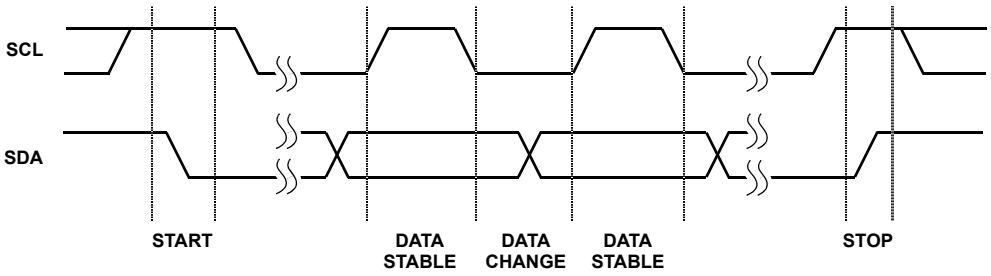


FIGURE 1. VALID DATA CHANGES, START, AND STOP CONDITIONS

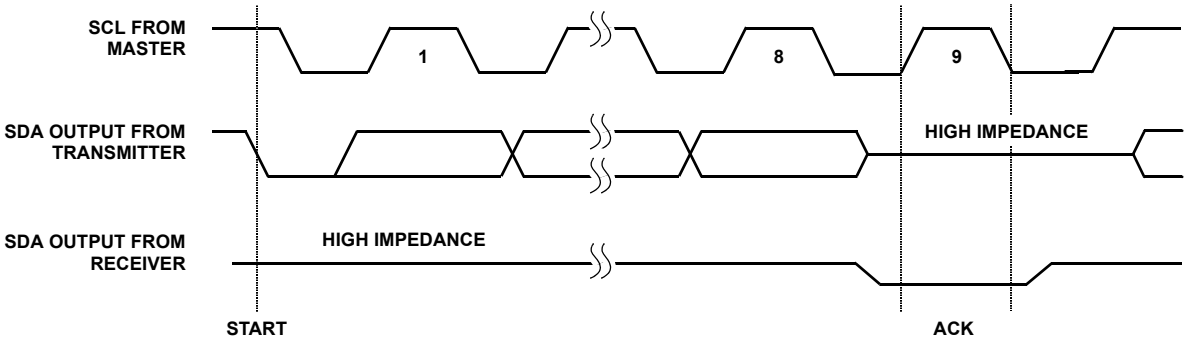


FIGURE 2. ACKNOWLEDGE RESPONSE FROM RECEIVER

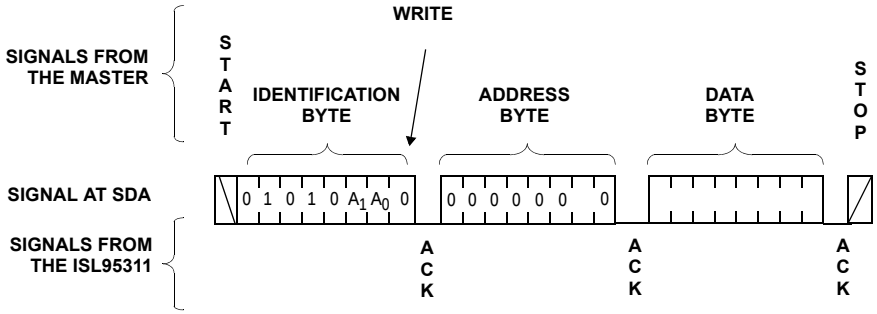


FIGURE 3. BYTE WRITE SEQUENCE

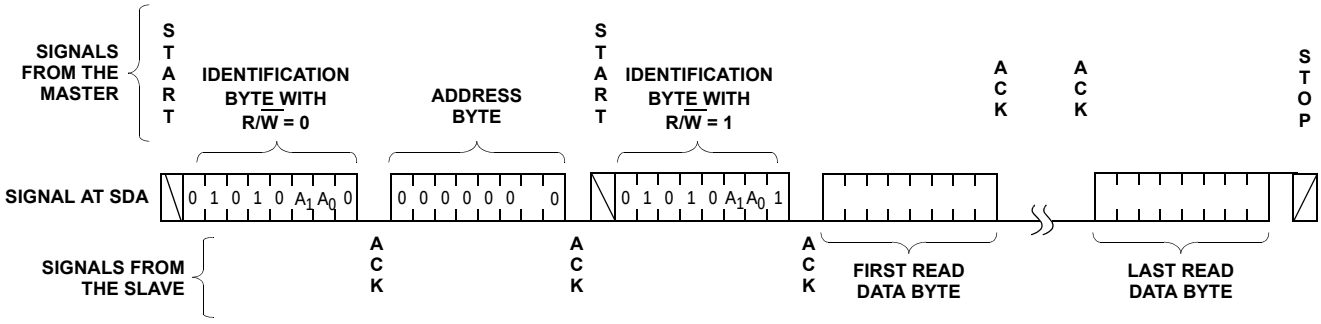


FIGURE 4. READ SEQUENCE

Communicating with the ISL95311

There are 3 register addresses in the ISL95311, of which two can be used. Address 00h and address 02h are used to control the device. Address 01h is reserved and should not be used. Address 00h contains the nonvolatile Initial Value Register (IVR), and the volatile Wiper Register (WR). Address 02h contains only a volatile word and is used as a pointer to either the IVR or WR. See Table 1.

Register Descriptions: Access Control

The Access Control Register (ACR) is volatile and is at address 02h. It is 8-bits, and only the MSB is significant, all other bits should be zero (0). The ACR controls which word is accessed at register 00h as follows:

00h = Nonvolatile IVR

80h = Volatile WR

All other bits of the ACR should be written to as zeros. Only the MSB can be either 0 or 1. Power-up default for this address is 00h.

Register Description: IVR and WR

The ISL95311 has a single potentiometer. The wiper of the potentiometer is controlled directly by the WR. Writes and reads can be made directly to this register to control and monitor the wiper position without any nonvolatile memory changes. This is done by setting address 02h to data 80h, then writing the data.

The nonvolatile IVR stores the power-up value of the wiper. On power-up, the contents of the IVR are transferred to the WR.

To write to the IVR, first address 02h is set to data 00h, then the data is written. Writing a new value to the IVR register will set a new power-up position for the wiper. Also, writing to this register will load the same value into the WR as the IVR. So, if a new value is loaded into the IVR, not only will the non-volatile IVR change, but the WR will also contain the same value after the write, and the wiper position will change. Reading from the IVR will not change the WR, if its contents are different.

Example 1

WRITING A NEW VALUE (77H) TO THE IVR:

Write to ACR first

S	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	1	0	A	0	0	0	0	0	0	0	0	A	P

Then, write to IVR

S	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	0	0	A	0	1	1	1	0	1	1	1	A	P

(Note that the WR will also reflect this new value since both registers get written to at the same time)

Example 2

READING FROM THE WR:

Write to the ACR first (to index the WR)

S	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	1	0	A	0	0	0	0	0	0	1	0	A	P

Then, Set the WR address

S	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	0	0	A

Read from the WR

S	0	1	0	1	0	0	0	1	A	x	x	x	x	x	x	x	x	P

Notes: A = acknowledge, x = data bit read

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
August 13, 2015	FN8084.2	Updated Ordering Information Table on page 1. Added Revision History and About Intersil sections. Updated POD M10.118 to latest rev. Changes: Updated to new POD template. Added land pattern

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

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