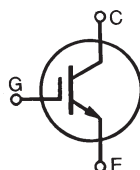


Polar™ High Speed IGBT

IXGQ240N30PB

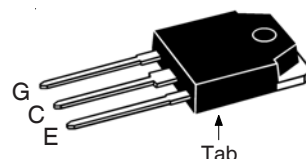
$V_{CES} = 300V$
 $I_{CP} = 500A$
 $V_{CE(sat)} \leq 1.6V$

For PDP Applications



Symbol	Test Conditions	Maximum Ratings	
V_{CES}	$T_J = 25^\circ C$ to $150^\circ C$	300	V
V_{GES}	Continuous	± 20	V
V_{GEM}	Transient	± 30	V
I_{C25}	$T_C = 25^\circ C$ (Chip Capability)	240	A
I_{CP}	$T_J \leq 150^\circ C$, $tp < 10\mu s$	500	A
$I_{C(RMS)}$	Lead Current Limit	75	A
SSOA (RBSOA)	$V_{GE} = 15V$, $T_{VJ} = 125^\circ C$, $R_G = 1\Omega$ Clamped Inductive Load	$I_{CM} = 240$ $V_{CE} \leq V_{CES}$	A
P_d	$T_C = 25^\circ C$	500	W
T_J		-55 ... +150	$^\circ C$
T_{JM}		150	$^\circ C$
T_{stg}		-55 ... +150	$^\circ C$
T_L	Maximum Lead Temperature for Soldering	300	$^\circ C$
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	$^\circ C$
M_d	Mounting Torque	1.13/10	Nm/lb.in.
Weight		5.5	g

TO-3P



G = Gate C = Collector
 E = Emitter Tab = Collector

Features

- Low $V_{CE(sat)}$
 - for Minimum On-State Conduction Losses
- MOS Gate Turn-On
 - Drive Simplicity

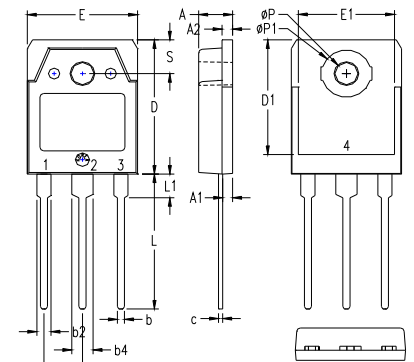
Applications

- PDP Screen Drivers

Symbol	Test Conditions ($T_J = 25^\circ C$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$	300		V
$V_{GE(th)}$	$I_C = 1mA$, $V_{CE} = V_{GE}$	3.0		5.0 V
I_{CES}	$V_{CE} = V_{CES}$, $V_{GE} = 0V$ $T_J = 125^\circ C$			1 μA 200 μA
I_{GES}	$V_{CE} = 0V$, $V_{GE} = \pm 20V$			± 100 nA
$V_{CE(sat)}$	$I_C = 120A$, $V_{GE} = 15V$, Note 1 $T_J = 125^\circ C$		1.35 1.40	V V
	$I_C = 240A$ $T_J = 125^\circ C$		1.85 2.10	V V

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$I_C = 120\text{A}$, $V_{CE} = 10\text{V}$, Note 1	75	130	S
C_{ies}	$V_{CE} = 25\text{V}$, $V_{GE} = 0\text{V}$, $f = 1\text{MHz}$		6900	pF
C_{oes}			435	pF
C_{res}			97	pF
Q_g	$I_C = 120\text{A}$, $V_{GE} = 15\text{V}$, $V_{CE} = 0.5 \cdot V_{CES}$		225	nC
Q_{ge}			37	nC
Q_{gc}			88	nC
$t_{d(on)}$	Resistive Switching Times, $T_J = 25^\circ\text{C}$ $I_C = 120\text{A}$, $V_{GE} = 15\text{V}$ $V_{CE} = 0.8 \cdot V_{CES}$, $R_G = 1\Omega$		30	ns
t_r			70	ns
$t_{d(off)}$			104	ns
t_f			45	ns
$t_{d(on)}$	Resistive Switching Times, $T_J = 125^\circ\text{C}$ $I_C = 120\text{A}$, $V_{GE} = 15\text{V}$ $V_{CE} = 0.8 \cdot V_{CES}$, $R_G = 1\Omega$		29	ns
t_r			104	ns
$t_{d(off)}$			103	ns
t_f			100	ns
R_{thJC}				0.25 $^\circ\text{C/W}$
R_{thCS}		0.21		$^\circ\text{C/W}$

TO-3P (IXGQ) Outline



Pins: 1 - Gate 2 - Drain
3 - Source 4, Tab - Drain

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.185	.193	4.70	4.90
A1	.051	.059	1.30	1.50
A2	.057	.065	1.45	1.65
b	.035	.045	0.90	1.15
b2	.075	.087	1.90	2.20
b4	.114	.126	2.90	3.20
c	.022	.031	0.55	0.80
D	.780	.791	19.80	20.10
D1	.665	.677	16.90	17.20
E	.610	.622	15.50	15.80
E1	.531	.539	13.50	13.70
e	.215 BSC		5.45 BSC	
L	.779	.795	19.80	20.20
L1	.134	.142	3.40	3.60
øP1	.126	.134	3.20	3.40
S	.272	.280	6.90	7.10
S	.193	.201	4.90	5.10

All metal area are tin plated.

Note 1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
	4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

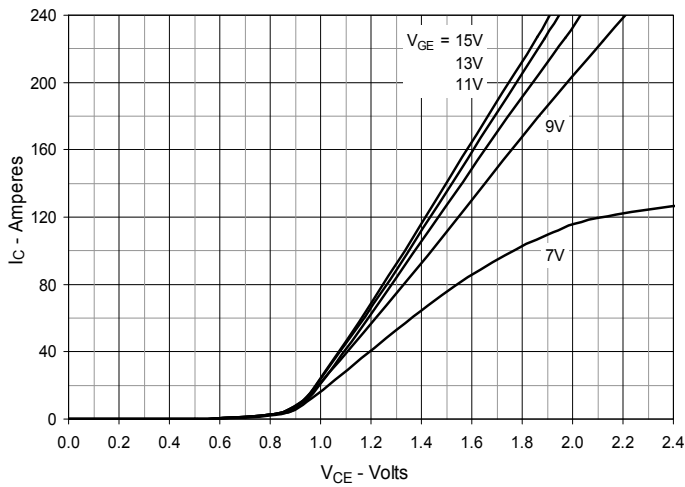


Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

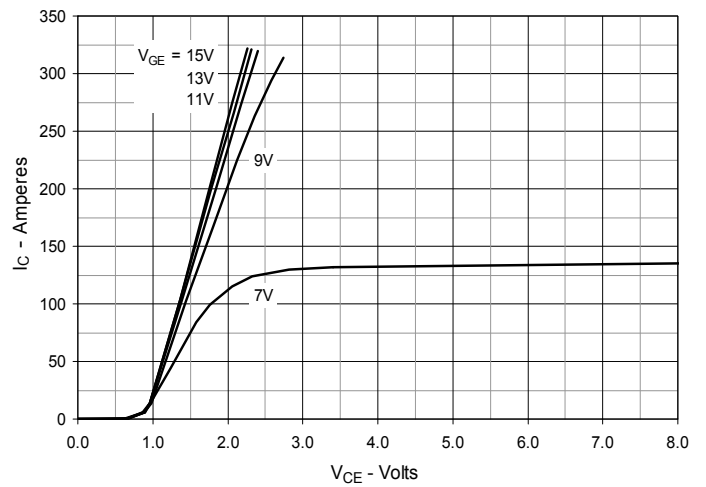


Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

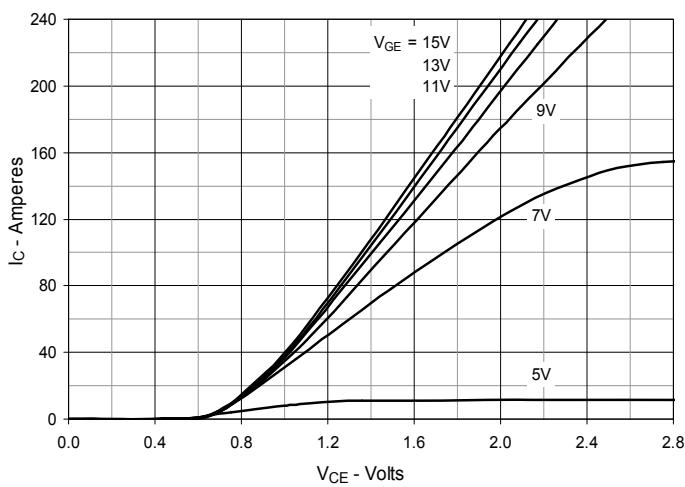


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

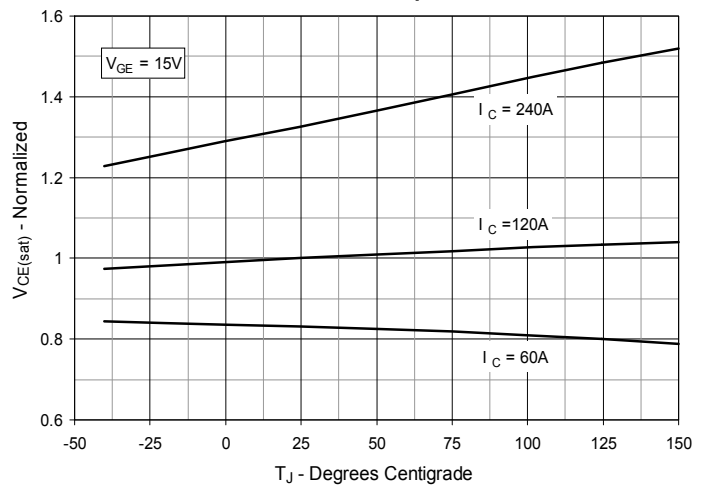


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

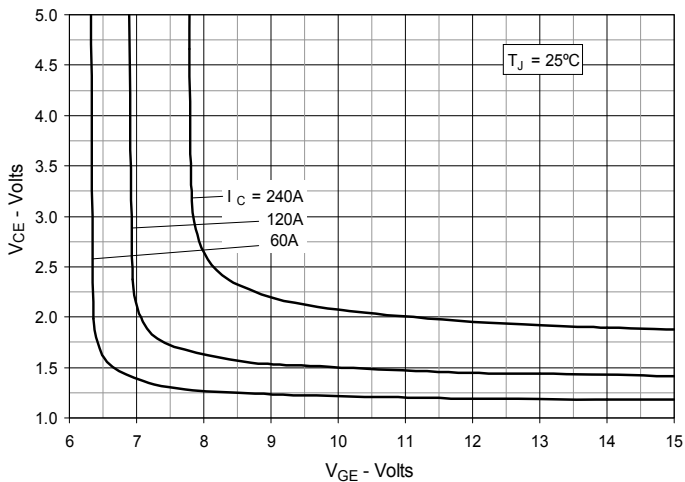


Fig. 6. Input Admittance

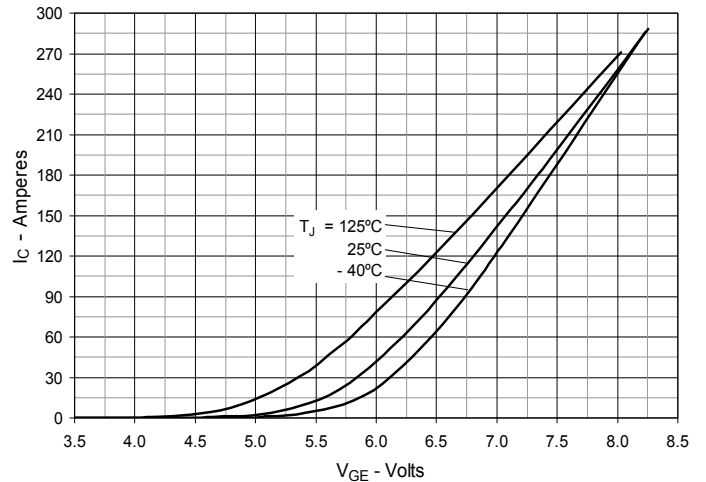


Fig. 7. Transconductance

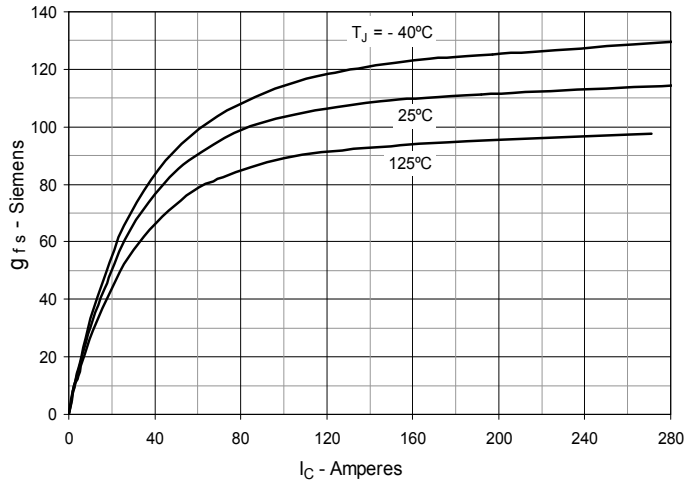


Fig. 8. Gate Charge

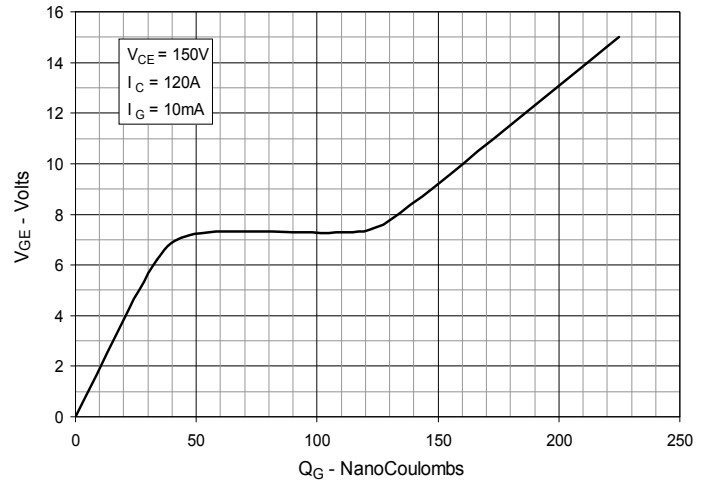


Fig. 9. Reverse-Bias Safe Operating Area

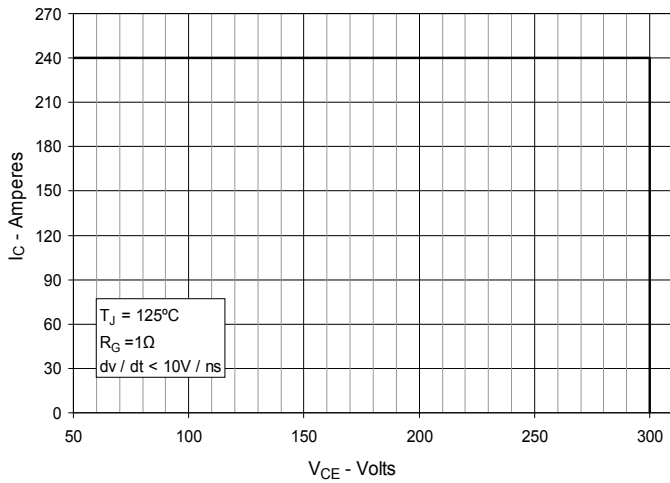


Fig. 10. Capacitance

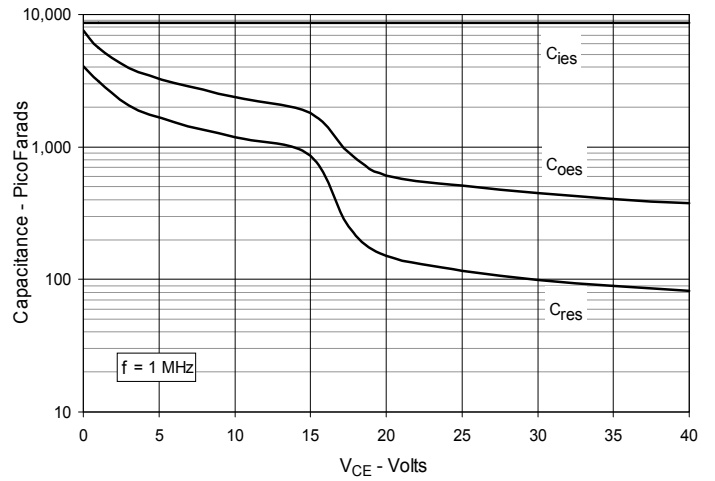


Fig. 11. Forward-Bias Safe Operating Area

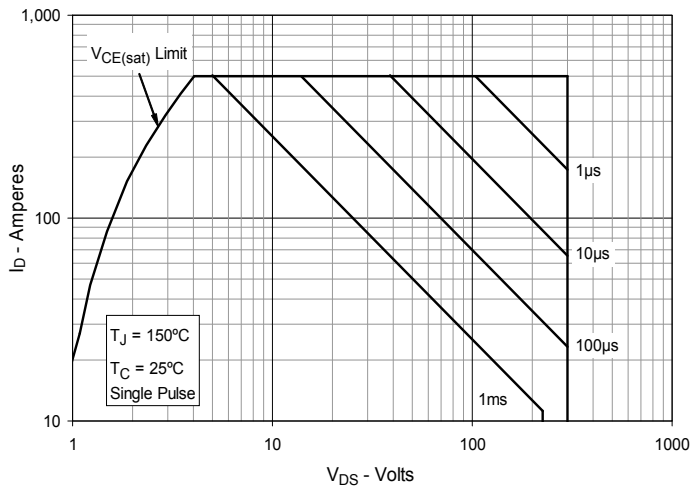


Fig. 12. Maximum Transient Thermal Impedance

