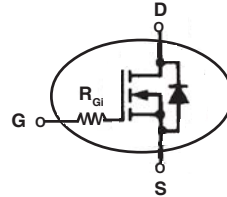


LinearL2™
Power MOSFET
w/ Extended FBSOA

IXTT38N30L2HV
IXTH38N30L2

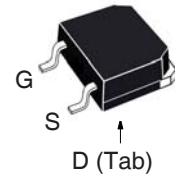
$$\begin{aligned}
 V_{DSS} &= 300V \\
 I_{D25} &= 38A \\
 R_{DS(on)} &\leq 100m\Omega
 \end{aligned}$$

N-Channel Enhancement Mode

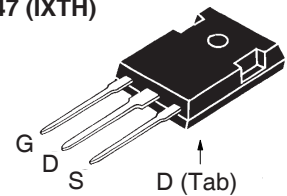


Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	300	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C , $R_{GS} = 1M\Omega$	300	V
V_{GSS}	Continuous	± 20	V
V_{GSM}	Transient	± 30	V
I_{D25}	$T_C = 25^\circ\text{C}$	38	A
I_{DM}	$T_C = 25^\circ\text{C}$, Pulse Width Limited by T_{JM}	120	A
I_A	$T_C = 25^\circ\text{C}$	38	A
E_{AS}	$T_C = 25^\circ\text{C}$	2.5	J
P_D	$T_C = 25^\circ\text{C}$	400	W
T_J		-55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		-55 ... +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering	300	$^\circ\text{C}$
T_{SOLD}	Plastic Body for 10s	260	$^\circ\text{C}$
M_d	Mounting Torque (TO-247)	1.13 / 10	Nm/lb.in
Weight	TO-268HV	4	g
	TO-247	6	g

TO-268HV (IXTT..HV)



TO-247 (IXTH)



G = Gate D = Drain
 S = Source Tab = Drain

Features

- Designed for Linear Operation
- International Standard Packages
- Avalanche Rated
- Guaranteed FBSOA at 75°C

Advantages

- Easy to Mount
- Space Savings
- High Power Density

Applications

- Solid State Circuit Breakers
- Soft Start Controls
- Linear Amplifiers
- Programmable Loads
- Current Regulators

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V$, $I_D = 250\mu\text{A}$	300		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	2.5		V
I_{GSS}	$V_{GS} = \pm 20V$, $V_{DS} = 0V$			± 100 nA
I_{DSS}	$V_{DS} = V_{DSS}$, $V_{GS} = 0V$ $T_J = 125^\circ\text{C}$			10 μA 100 μA
$R_{DS(on)}$	$V_{GS} = 10V$, $I_D = 0.5 \cdot I_{D25}$, Note 1			100 m Ω

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values			
		Min.	Typ.	Max.	
g_{fs}	$V_{DS} = 10\text{V}$, $I_D = 0.5 \cdot I_{D25}$, Note 1	12	16	20	S
C_{iss}	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{MHz}$		7200		pF
C_{oss}			700		pF
C_{rss}			200		pF
R_{Gi}	Integrated Gate Input Resistor		3.4		Ω
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 \cdot I_{D25}$ $R_G = 0\Omega$ (External)		30		ns
t_r			125		ns
$t_{d(off)}$			94		ns
t_f			36		ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 \cdot I_{D25}$		260		nC
Q_{gs}			43		nC
Q_{gd}			140		nC
R_{thJC}	TO-247			0.31	$^\circ\text{C/W}$
R_{thCS}			0.21		$^\circ\text{C/W}$

Safe Operating Area Specification

Symbol	Test Conditions	Characteristic Values			
		Min.	Typ.	Max.	
SOA	$V_{DS} = 300\text{V}$, $I_D = 0.8\text{A}$, $T_C = 75^\circ\text{C}$, $T_p = 2\text{s}$	240			W

Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values			
		Min.	Typ.	Max.	
I_S	$V_{GS} = 0\text{V}$			38	A
I_{SM}	Repetitive, pulse Width Limited by T_{JM}			152	A
V_{SD}	$I_F = I_S$, $V_{GS} = 0\text{V}$, Note 1			1.4	V
t_{rr}	$I_F = 19\text{A}$, $-di/dt = 100\text{A}/\mu\text{s}$ $V_R = 100\text{V}$		420		ns
Q_{RM}			5.4		μC
I_{RM}			27		A

Note 1: Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.

PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
by one or more of the following U.S. patents:	4,860,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

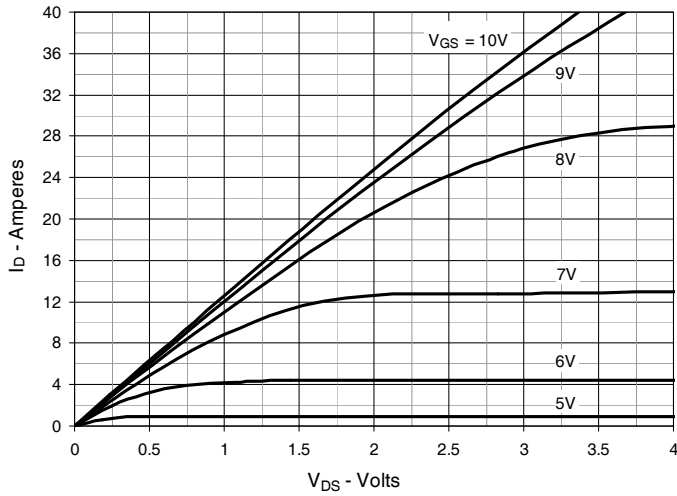


Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

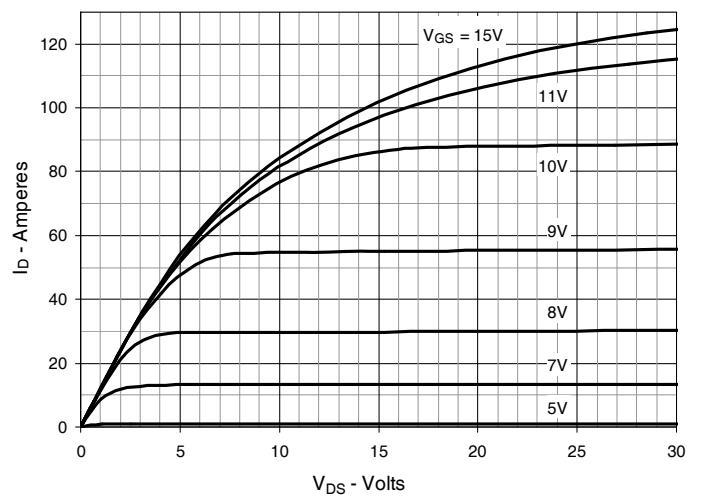


Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

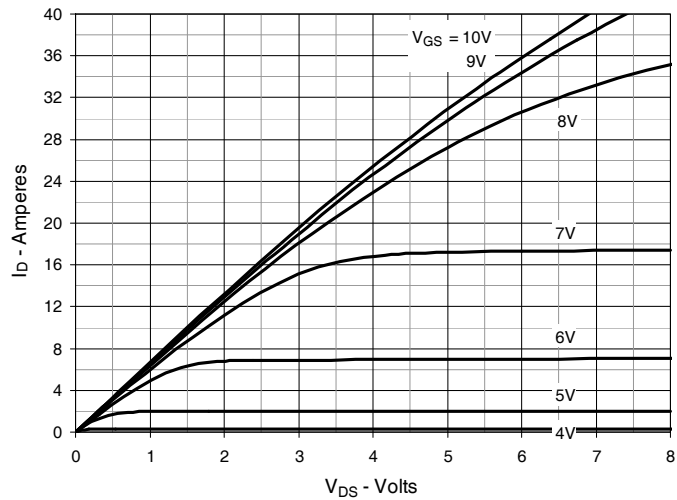


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 19\text{A}$ Value vs. Junction Temperature

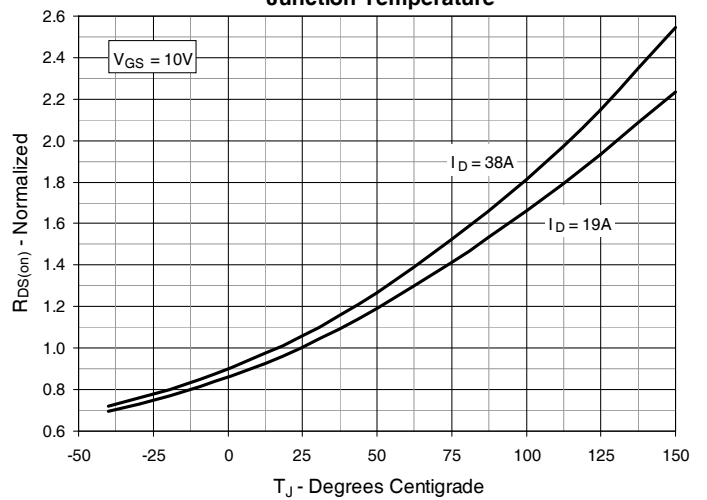


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 19\text{A}$ Value vs. Drain Current

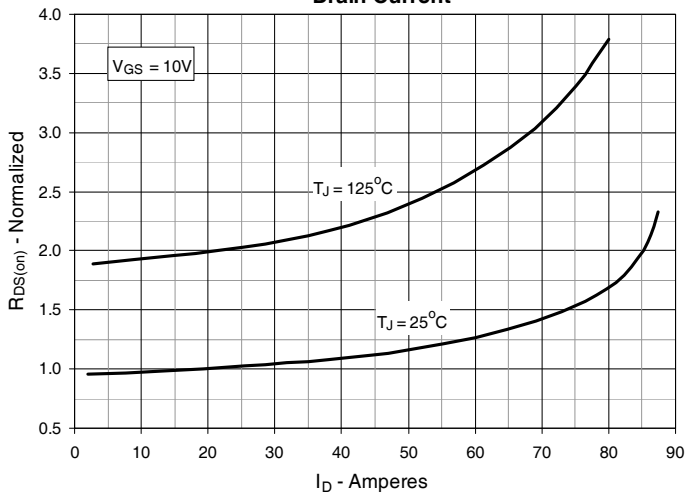


Fig. 6. Normalized Breakdown & Threshold Voltages vs. Junction Temperature

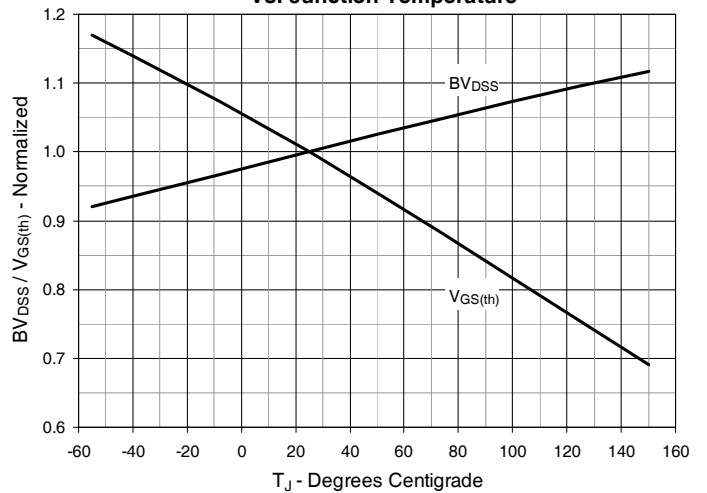


Fig. 7. Maximum Drain Current vs. Case Temperature

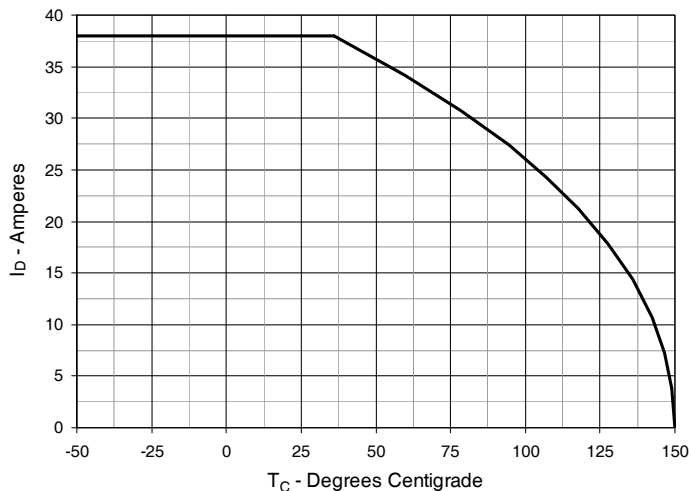


Fig. 8. Input Admittance

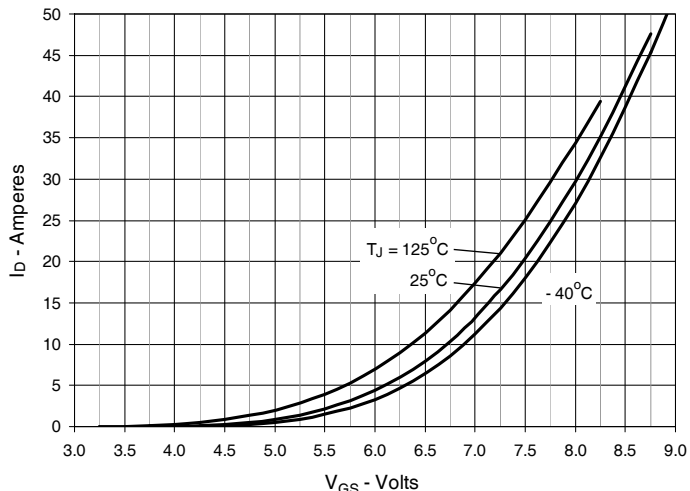


Fig. 9. Transconductance

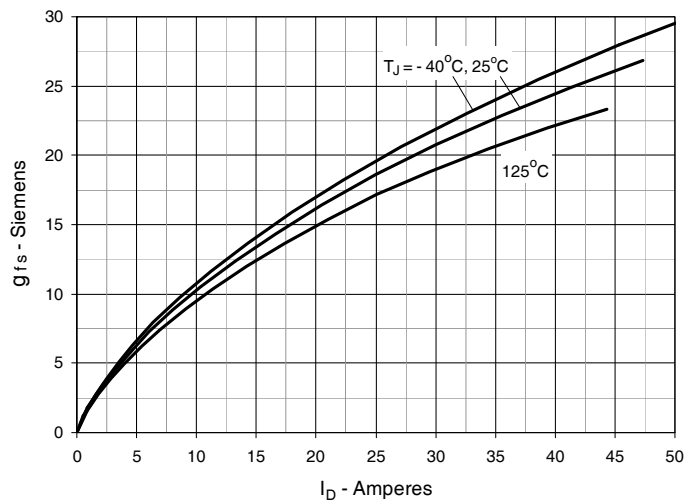


Fig. 10. Forward Voltage Drop of Intrinsic Diode

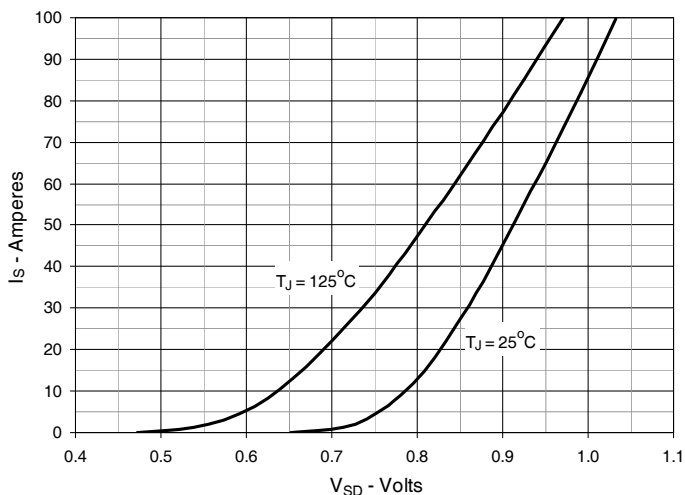


Fig. 11. Gate Charge

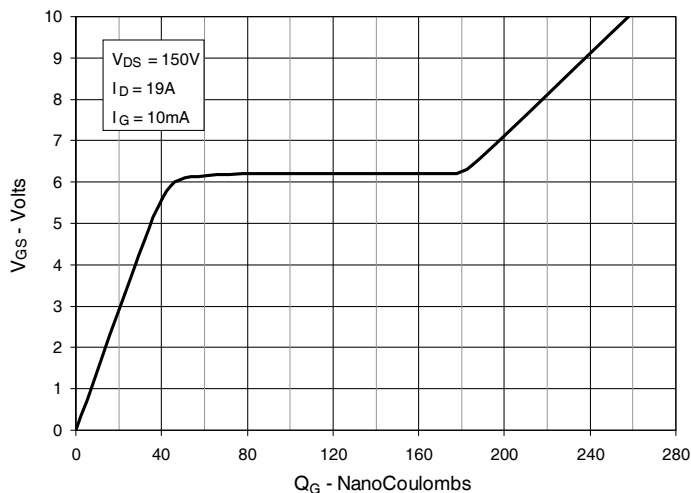


Fig. 12. Capacitance

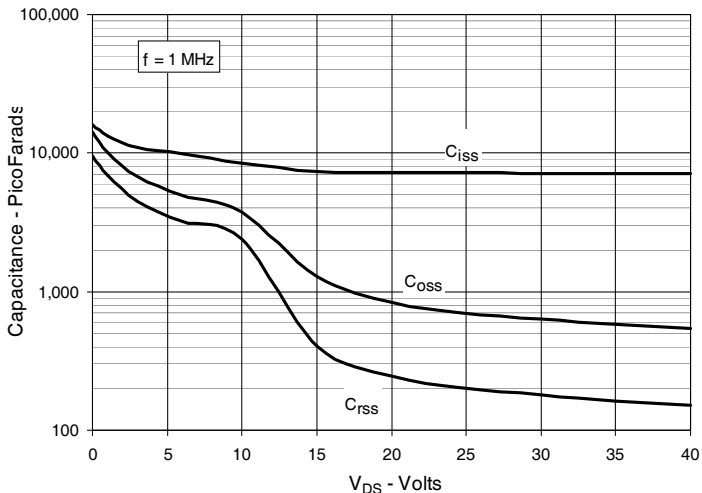


Fig. 13. Forward-Bias Safe Operating Area
@ $T_C = 25^\circ\text{C}$

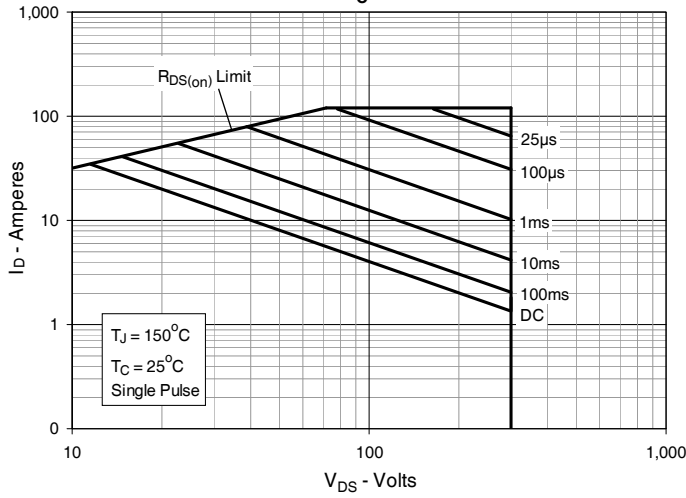


Fig. 14. Forward-Bias Safe Operating Area
@ $T_C = 75^\circ\text{C}$

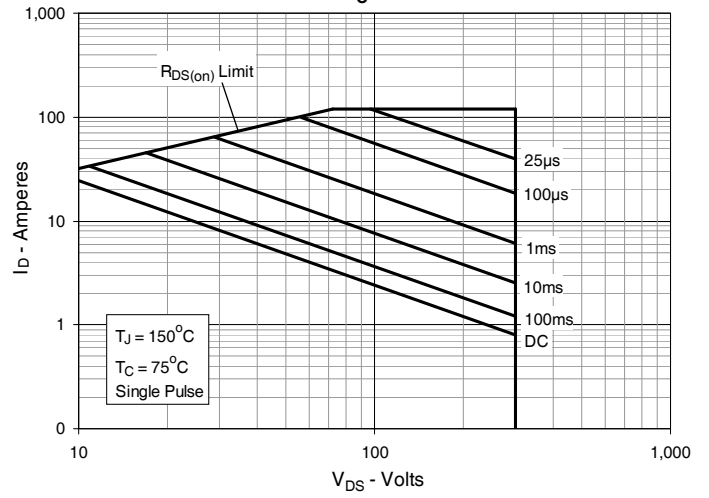


Fig. 15. Maximum Transient Thermal Impedance

