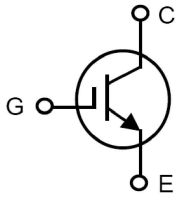
IXYS

1200V XPT™ IGBT GenX4™

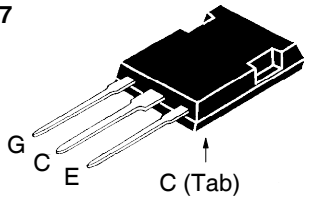
IXYX140N120A4

V_{CES} = 1200V
I_{C110} = 140A
$V_{CE(sat)}$ ≤ 1.70V
$t_{fi(typ)}$ = 320ns

Ultra Low-Vsat IGBT for up to 5kHz Switching



PLUS247 (IXYX)



G = Gate C = Collector
E = Emitter Tab = Collector

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_J = 25°C to 175°C	1200	V
V_{CGR}	T_J = 25°C to 175°C, R_{GE} = 1MΩ	1200	V
V_{GES}	Continuous	±20	V
V_{GEM}	Transient	±30	V
I_{C25}	T_C= 25°C (Chip Capability)	480	A
I_{LRMS}	Terminal Current Limit	160	A
I_{C110}	T_C= 110°C	140	A
I_{CM}	T_C = 25°C, 1ms	1200	A
SSOA	V_{GE} = 15V, T_{VJ} = 125°C, R_G = 2Ω	I_{CM} = 280	A
(RBSOA)	Clamped Inductive Load	0.8 • V_{CES}	V
P_C	T_C = 25°C	1500	W
T_J		-55 ... +175	°C
T_{JM}		175	°C
T_{stg}		-55 ... +175	°C
T_L	Maximum Lead Temperature for Soldering 1.6 mm (0.062 in.) from Case for 10s	300	°C
F_C	Mounting Force	20..120 /4.5..27	N/lb
Weight		6	g

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{CES}	I_C = 250μA, V_{GE} = 0V	1200			V
$V_{GE(th)}$	I_C = 4mA, V_{CE} = V_{GE}	4.5		6.5	V
I_{CES}	V_{CE} = V_{CES}, V_{GE} = 0V			25	μA
	T_J = 125°C			5	mA
I_{GES}	V_{CE} = 0V, V_{GE} = ±20V			±200	nA
$V_{CE(sat)}$	I_C = I_{C110}, V_{GE} = 15V, Note 1		1.34	1.70	V
	T_J = 150°C		1.50		V

Features

- Optimized for Low Conduction Losses
- Positive Thermal Coefficient of Vce(sat)
- International Standard Package

Advantages

- High Power Density
- Low Gate Drive Requirement

Applications

- Power Inverters
- UPS
- Motor Drives
- SMPS
- PFC Circuits
- Battery Chargers
- Welding Machines
- Lamp Ballasts
- Inrush Current Protection Circuits

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.
g_{fs}	I_C = 60A, V_{CE} = 10V, Note 1	60	100	S
C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz		8300	pF
C_{oes}			470	pF
C_{res}			300	pF
$Q_{g(on)}$	$I_C = I_{C110}$, V_{GE} = 15V, $V_{CE} = 0.5 \bullet V_{CES}$		420	nC
Q_{ge}			68	nC
Q_{gc}			210	nC
$t_{d(on)}$	**Inductive load, T_J = 25°C**		52	ns
t_{ri}	I_C = 70A, V_{GE} = 15V		47	ns
E_{on}	$V_{CE} = 0.5 \bullet V_{CES}$, R_G = 1.5Ω		4.9	mJ
$t_{d(off)}$	Note 2		590	ns
t_{fi}			320	ns
E_{off}			12.0	mJ
$t_{d(on)}$	**Inductive load, T_J = 150°C**		44	ns
t_{ri}	I_C = 70A, V_{GE} = 15V		42	ns
E_{on}	$V_{CE} = 0.5 \bullet V_{CES}$, R_G = 1.5Ω		7.4	mJ
$t_{d(off)}$	Note 2		710	ns
t_{fi}			530	ns
E_{off}			20.0	mJ
R_{thJC}				0.10 °C/W
R_{thCS}			0.15	°C/W

Notes:

1. Pulse test, t ≤ 300µs, duty cycle, d ≤ 2%.
2. Switching times & energy losses may increase for higher V_{CE}(clamp), T_J or R_G.

Fig. 1. Output Characteristics @ T_J = 25°C

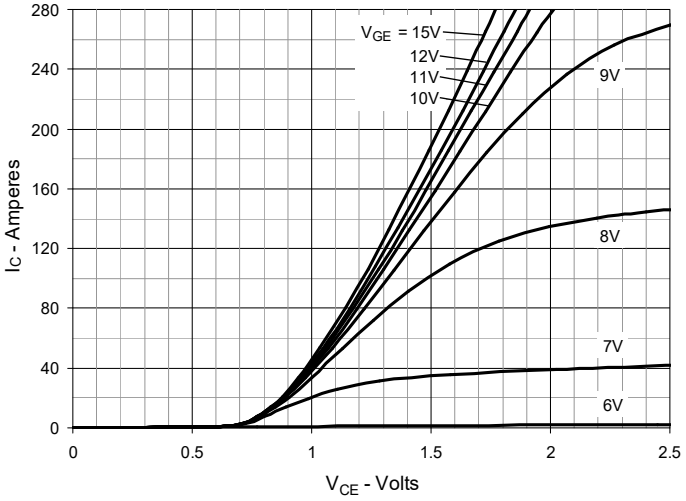


Fig. 2. Extended Output Characteristics @ T_J = 25°C

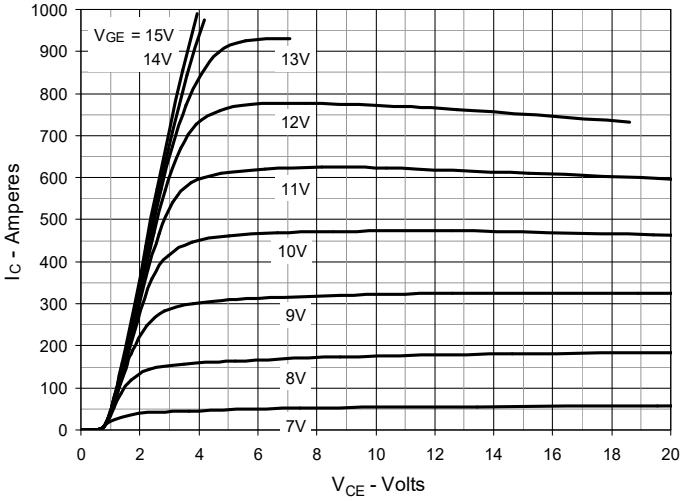


Fig. 3. Output Characteristics @ T_J = 150°C

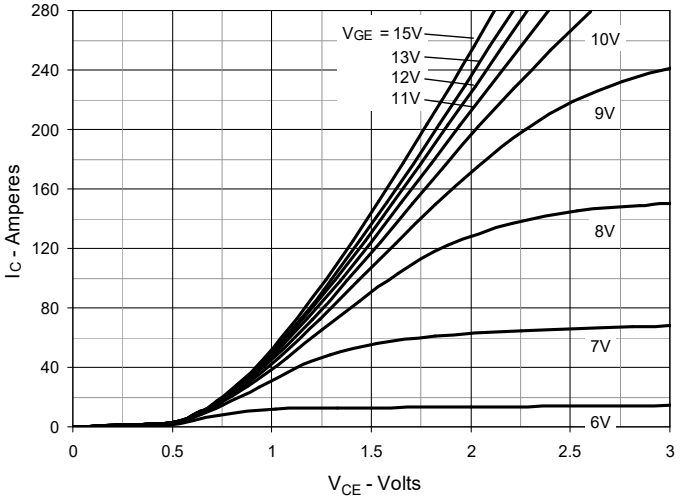


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

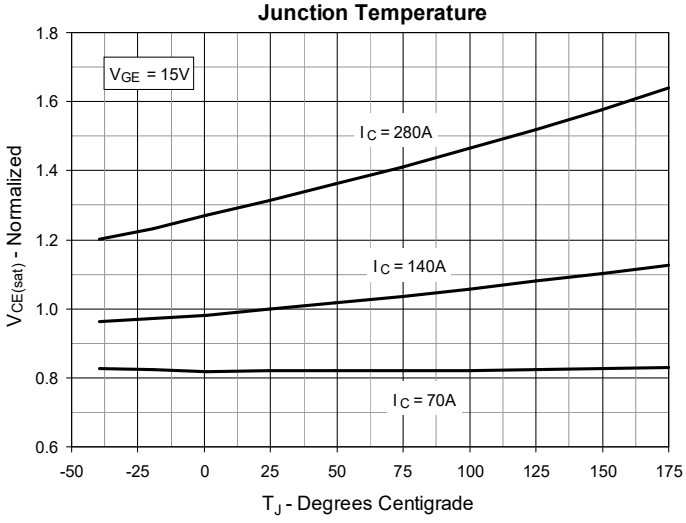


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

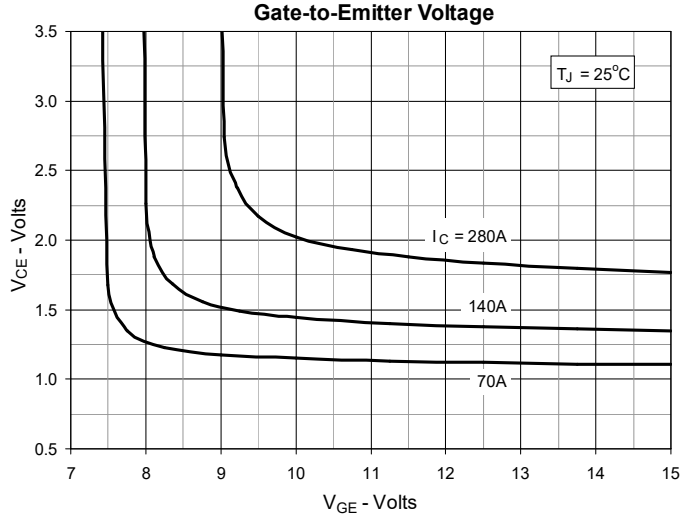


Fig. 6. Input Admittance

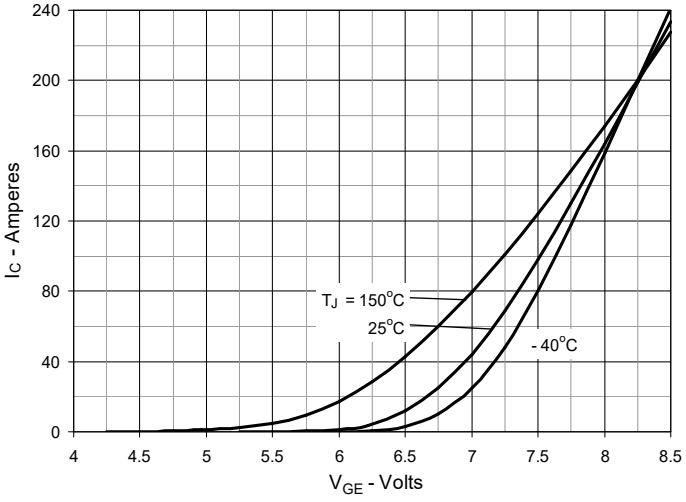


Fig. 7. Transconductance

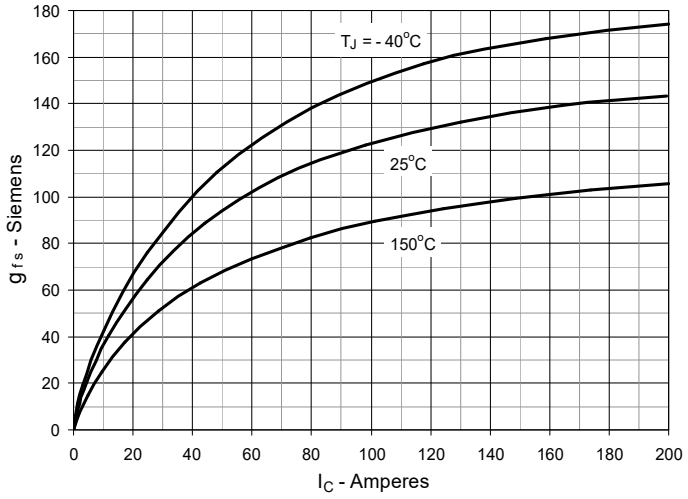


Fig. 8. Gate Charge

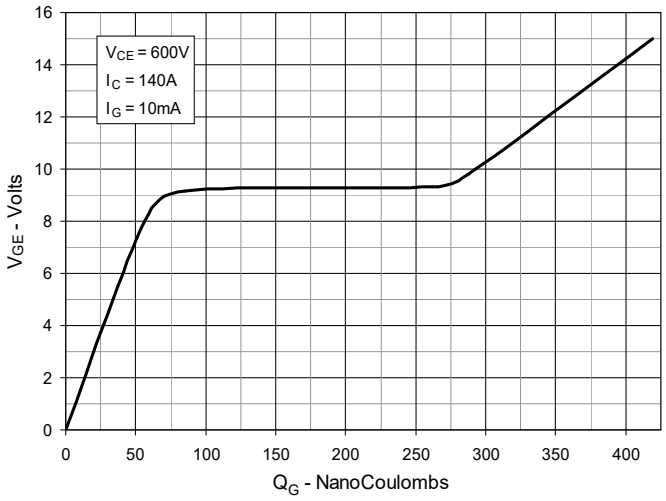


Fig. 9. Capacitance

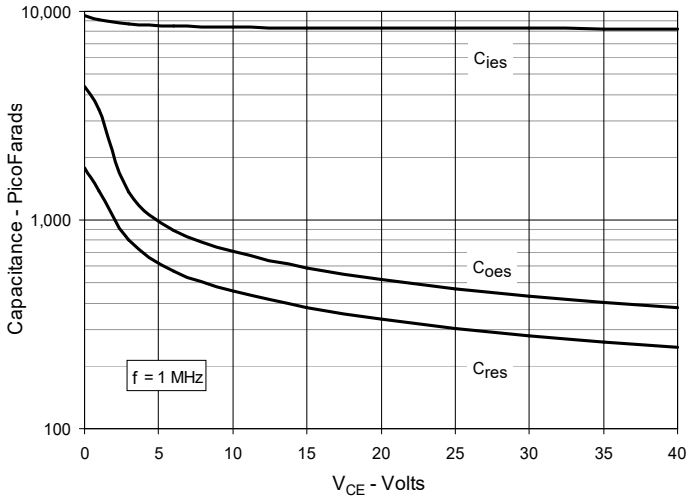


Fig. 10. Reverse-Bias Safe Operating Area

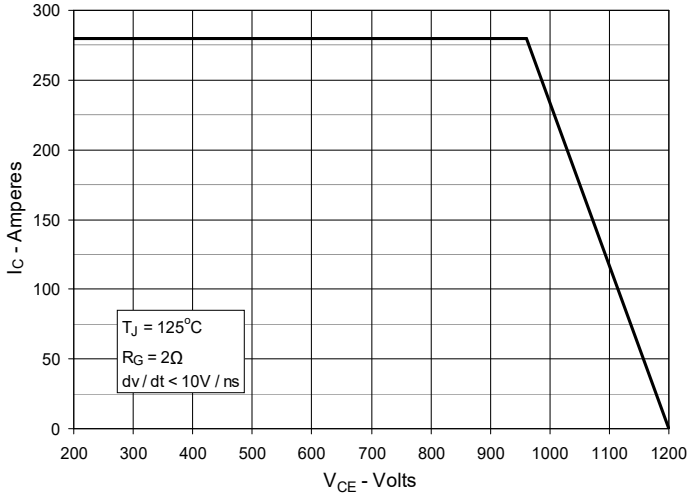


Fig. 11. Maximum Transient Thermal Impedance

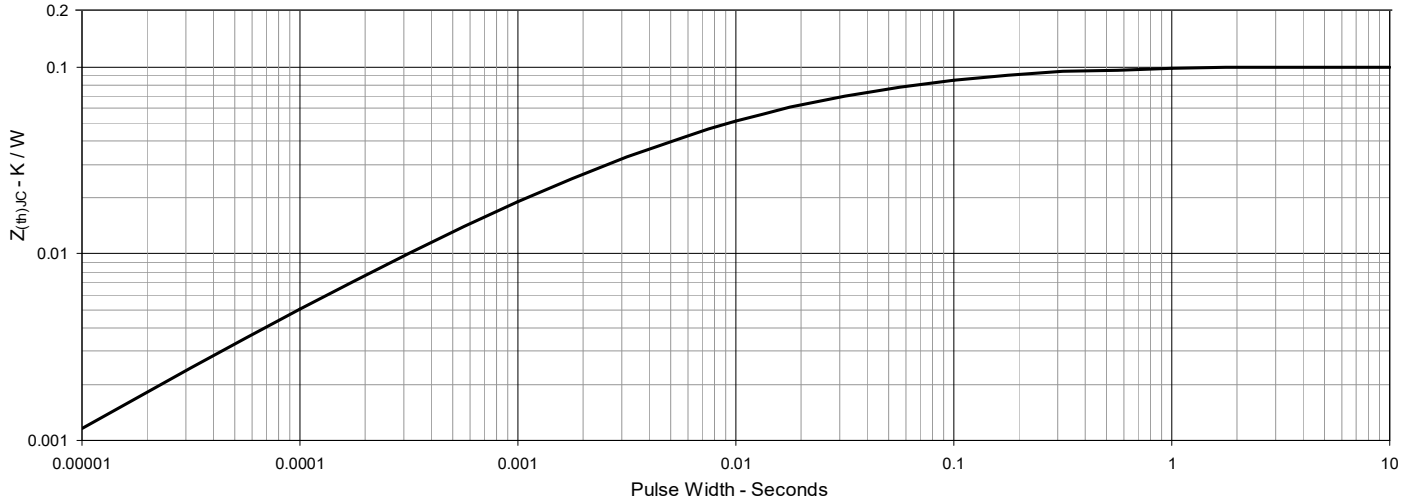


Fig. 12. Inductive Switching Energy Loss vs. Collector Current

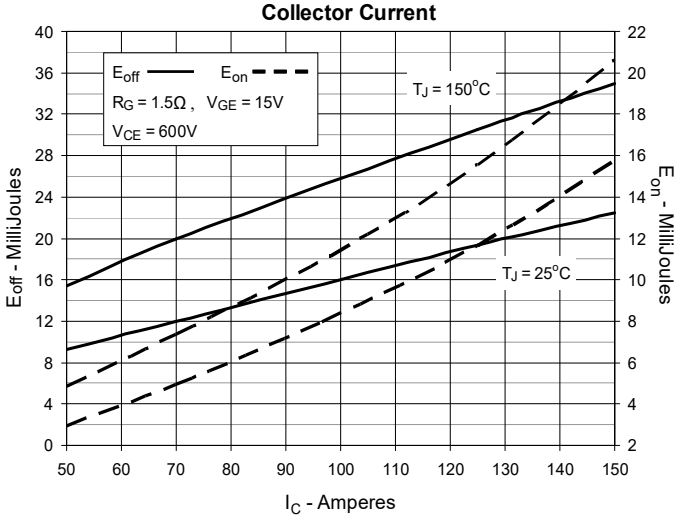


Fig. 13. Inductive Switching Energy Loss vs. Collector-Emitter Voltage

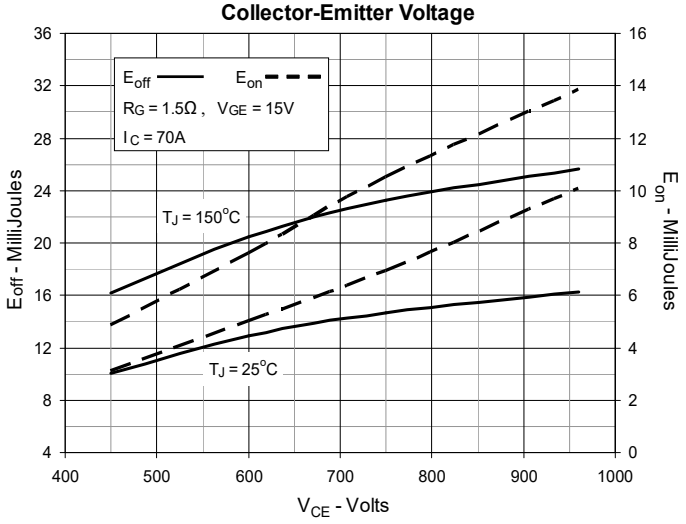


Fig. 14. Inductive Switching Energy Loss vs. Gate Resistance

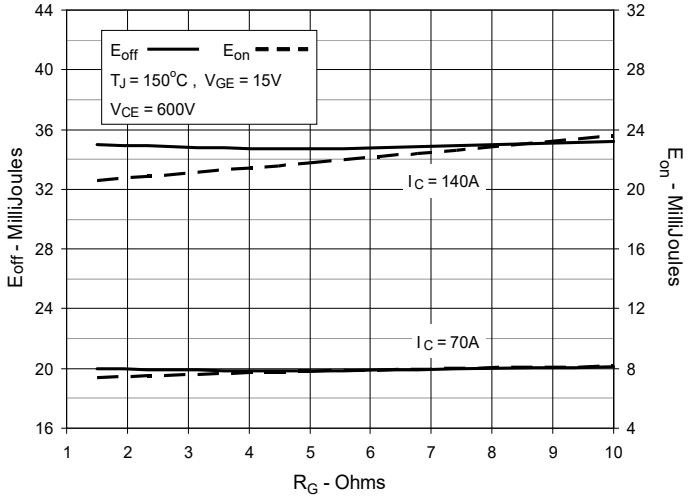


Fig. 15. Inductive Switching Energy Loss vs. Junction Temperature

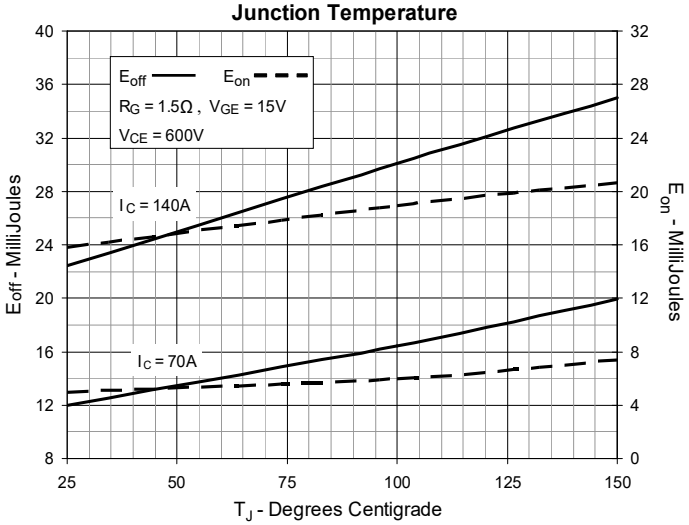


Fig. 16. Inductive Turn-off Switching Times vs. Gate Resistance

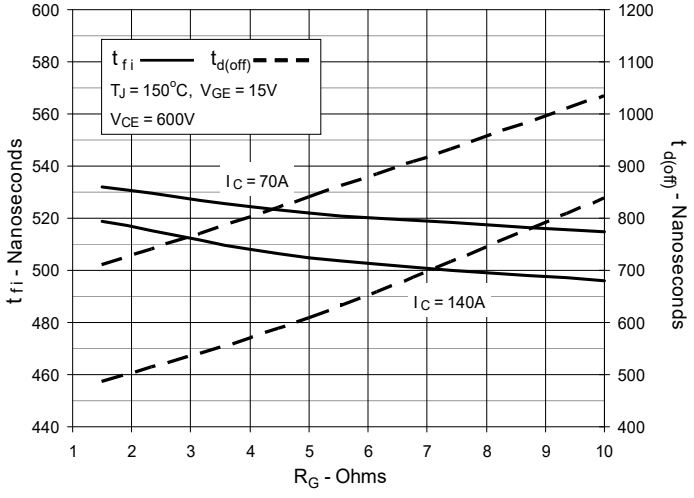


Fig. 17. Inductive Turn-off Switching Times vs. Collector Current

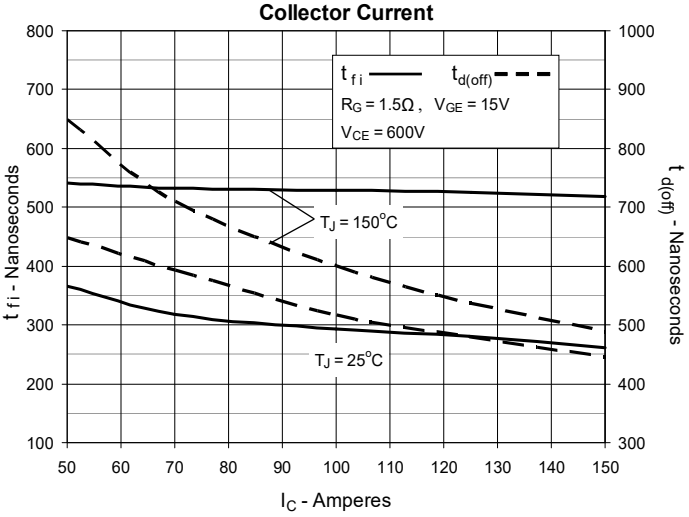


Fig. 18. Inductive Turn-off Switching Times vs. Junction Temperature

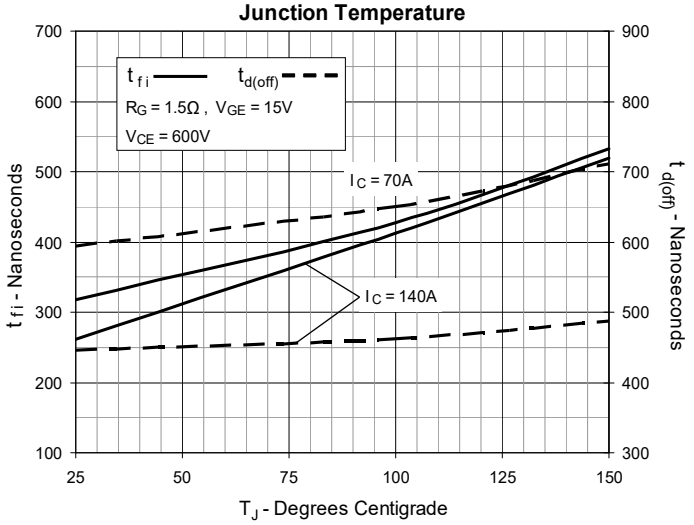


Fig. 19. Inductive Turn-on Switching Times vs. Gate Resistance

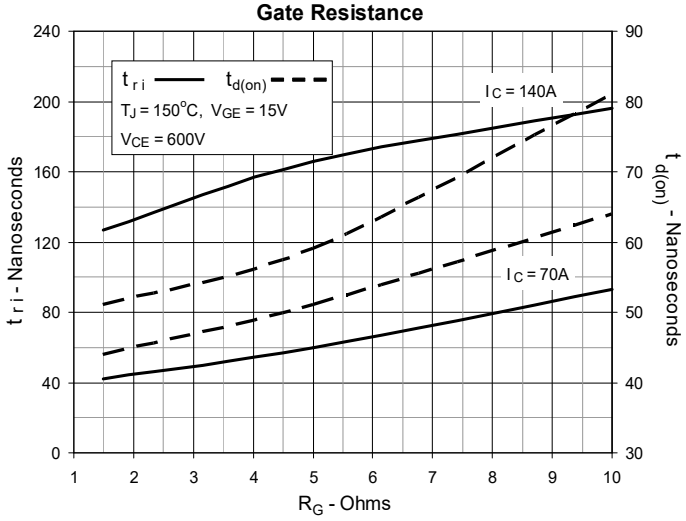


Fig. 20. Inductive Turn-on Switching Times vs. Collector Current

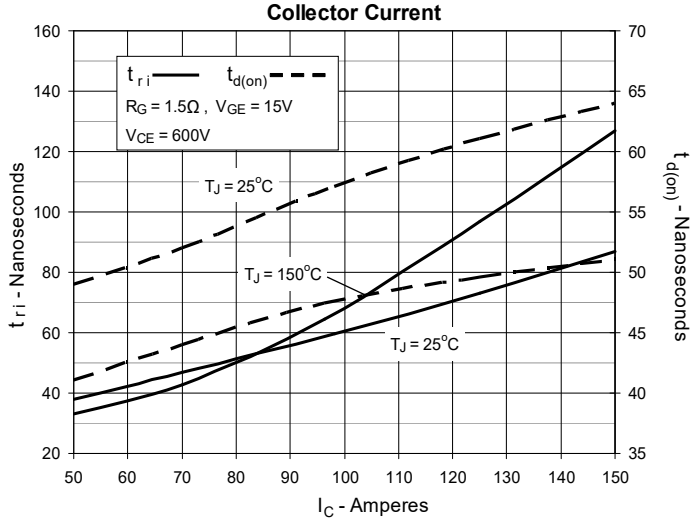
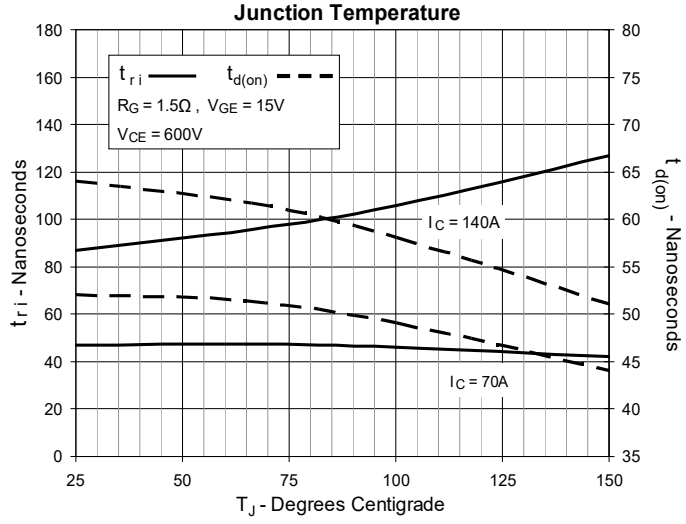
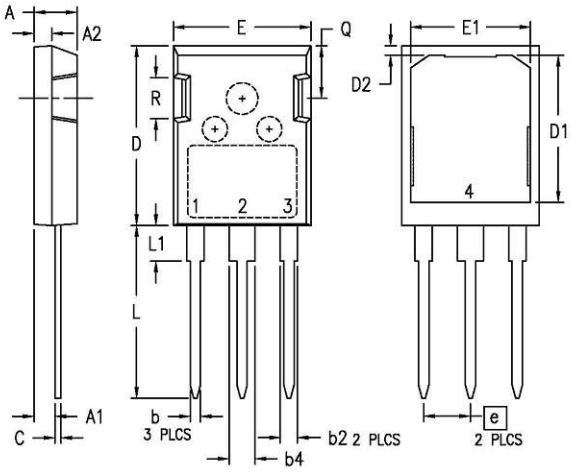


Fig. 21. Inductive Turn-on Switching Times vs. Junction Temperature



PLUS247 Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b2	.075	.087	1.91	2.20
b4	.115	.126	2.92	3.20
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
D1	.650	.690	16.51	17.53
D2	.035	.050	0.89	1.27
E	.620	.635	15.75	16.13
E1	.520	.560	13.08	14.22
e	.215 BSC		5.45 BSC	
L	.780	.810	19.81	20.57
L1	.150	.170	3.81	4.32
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83

1 - Gate
2,4 - Collector
3 - Emitter

NOTE:
1. This drawing will meet all dimensions requirement of JEDEC outline TO-247 AD (R-PSIP-F3) except screw mounting hole.
2. Pin #2 is connected to the bottom heatsink (#4).
3. Lead finish – One of the following depending on the packaging plants.
   3.1 Matte pure tin plating on the leads and back heatsink.
   3.2 Pb free solder dip on the leads and pre Ni plated back heatsink.