

N-Channel JFET

J109, MMBFJ108

Features

- This Device is Designed for Digital Switching Applications where Very Low On Resistance is Mandatory
- Sourced from Process 58
- These are Pb-Free Devices

MAXIMUM RATINGS (T_A = 25°C unless otherwise specified) (Notes 1, 2)

Symbol	Parameter	Value	Unit
V _{DG}	Drain–Gate Voltage	25	V
V _{GS}	Gate–Source Voltage	–25	V
I _{GF}	Forward Gate Current	10	mA
T _J , T _{STG}	Operating and Storage Junction Temperature Range	–55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. These ratings are based on a maximum junction temperature of 150°C.
2. These are steady-state limits. ON Semiconductor should be consulted on applications involving pulsed or low-duty-cycle operations.

THERMAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

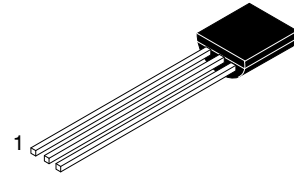
Symbol	Parameter	Max		Unit
		J109 (Note 3)	MMBFJ108 (Note 4)	
P _D	Total Device Dissipation	625	350	mW
	Derate Above 25°C	5.0	2.8	mW/°C
R _{θJC}	Thermal Resistance, Junction-to-Case	125	–	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient	200	357	°C/W

3. PCB size: FR-4, 76 mm x 114 mm x 1.57 mm (3.0 inch x 4.5 inch x 0.062 inch) with minimum land pattern size.
4. Device mounted on FR-4 PCB 36 mm x 18 mm x 1.5 mm; mounting pad for the collector lead minimum 6 cm².

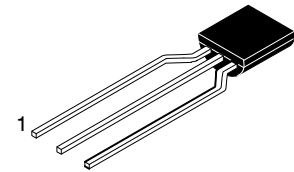


ON Semiconductor®

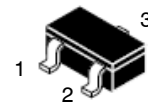
www.onsemi.com



TO-92 3 4.825x4.76
CASE 135AN



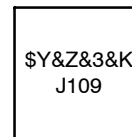
TO-92 3 4.83x4.76
LEADFORMED
CASE 135AR



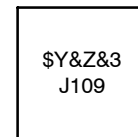
SOT-23/SUPERSOT™ -23,
3 LEAD, 1.4x2.9
CASE 527AG

1. Drain, 2. Source, 3. Gate

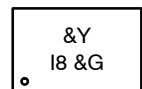
MARKING DIAGRAM



J109



J109-D26Z



MMBFJ108

J109, I8 = Specific Device Code
 \$Y = ON Semiconductor Logo
 &Y = Year Coding
 &G = Weekly Date Code
 &Z = Assembly Plant Code
 &3 = Date Code Format
 &K = Lot Run Traceability Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

J109, MMBFJ108

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Max	Unit	
OFF CHARACTERISTICS						
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	$I_G = -10 \mu\text{A}, V_{DS} = 0$	-25	-	V	
I_{GSS}	Gate Reverse Current	$V_{GS} = -15 \text{ V}, V_{DS} = 0$	-	-3.0	nA	
		$V_{GS} = -15 \text{ V}, V_{DS} = 0, T_A = 100^\circ\text{C}$	-	-200		
$V_{GS(off)}$	Gate-Source Cut-Off Voltage	$V_{DS} = 15 \text{ V}, I_D = 10 \text{ nA}$	MMBFJ108	-3.0	-10.0	V
			J109	-2.0	-6.0	

ON CHARACTERISTICS

I_{DSS}	Zero-Gate Voltage Drain Current (Note 5)	$V_{DS} = 15 \text{ V}, V_{GS} = 0$	MMBFJ108	80	-	mA
			J109	40	-	
$r_{DS(on)}$	Drain-Source On Resistance	$V_{DS} \leq 0.1 \text{ V}, V_{GS} = 0$	MMBFJ108	-	8.0	Ω
			J109	-	12	

SMALL SIGNAL CHARACTERISTICS

$C_{dg(on)}$ $C_{sg(off)}$	Drain-Gate & Source-Gate On Capacitance	$V_{DS} = 0, V_{GS} = 0, f = 1.0 \text{ MHz}$	-	85	pF
$C_{dg(off)}$	Drain-Gate Off Capacitance	$V_{DS} = 0, V_{GS} = -10 \text{ V}, f = 1.0 \text{ MHz}$	-	15	pF
$C_{sg(off)}$	Source-Gate Off Capacitance	$V_{DS} = 0, V_{GS} = -10 \text{ V}, f = 1.0 \text{ MHz}$	-	15	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse test: pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

TYPICAL PERFORMANCE CHARACTERISTICS

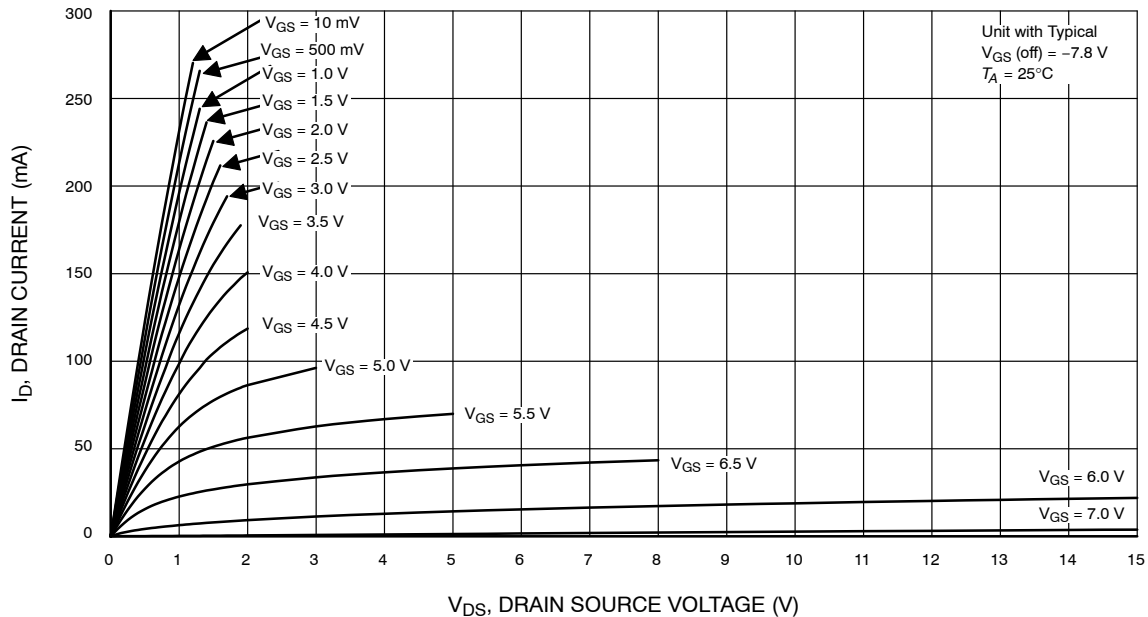


Figure 1. Common Drain-Source, MMBFJ108

J109, MMBFJ108

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

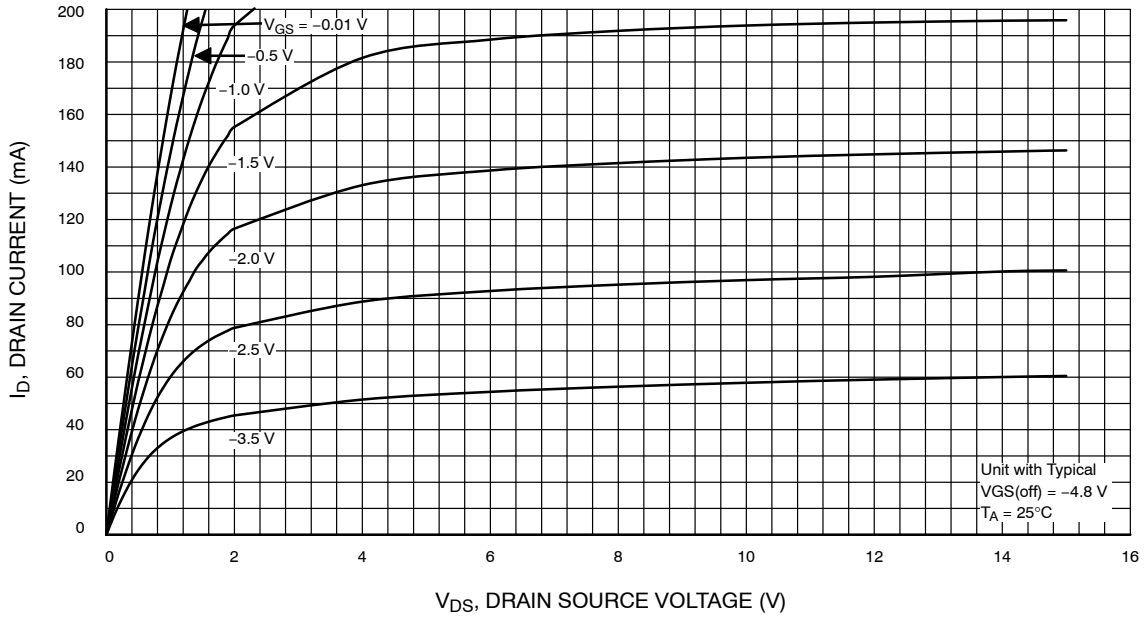


Figure 2. Common Drain-Source, MMBFJ108, J109

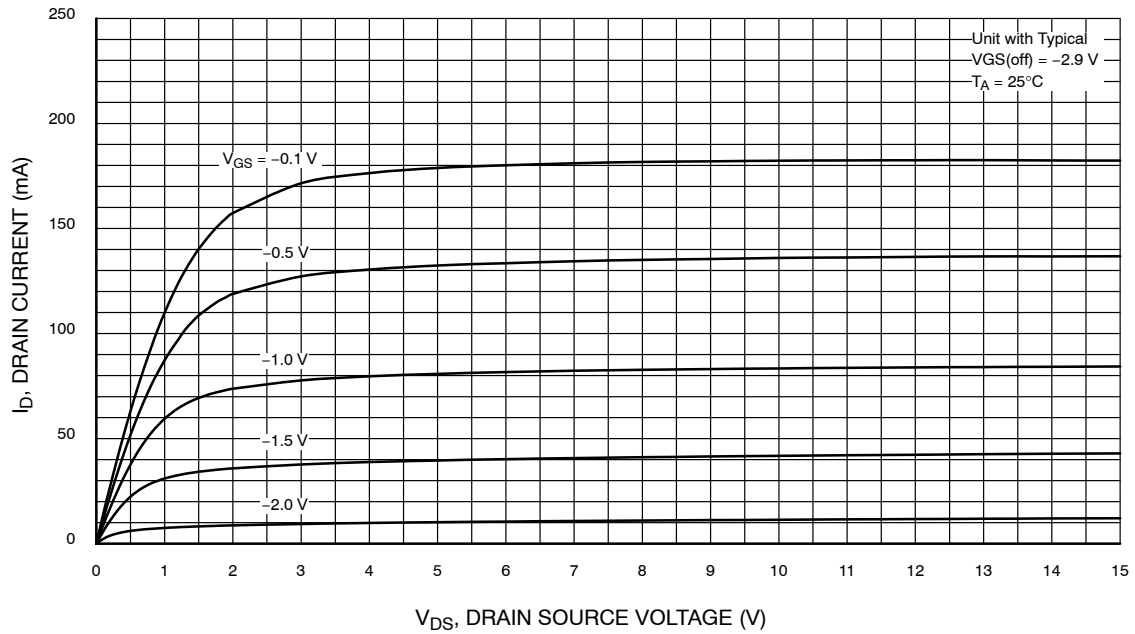


Figure 3. Common Drain-Source, J109

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

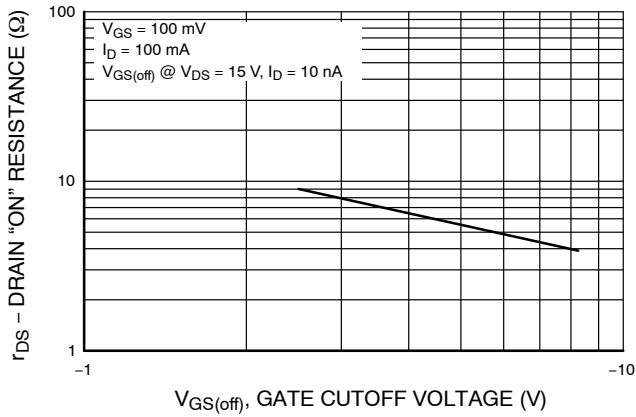


Figure 4. Drain ON Resistance

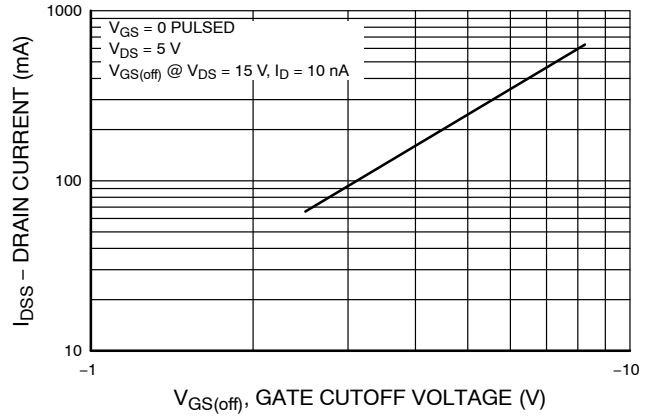


Figure 5. Drain Current vs. Gate-Source Cut-Off Voltage

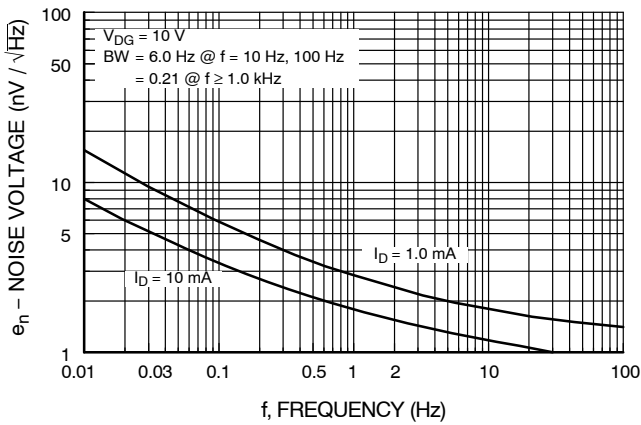


Figure 6. Noise Voltage vs. Frequency

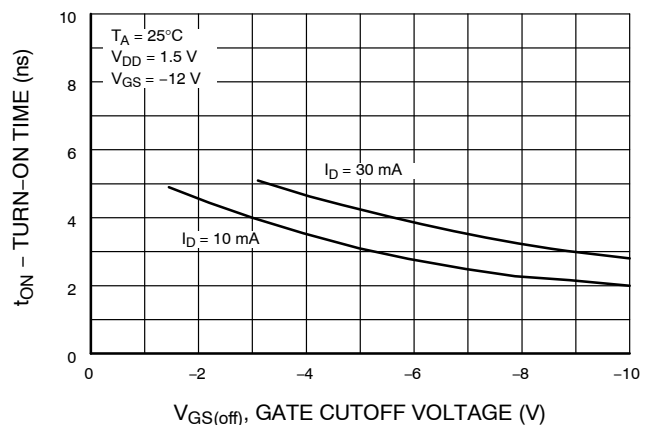


Figure 7. Switching Turn-On Time vs. Gate-Source Cut-Off Voltage

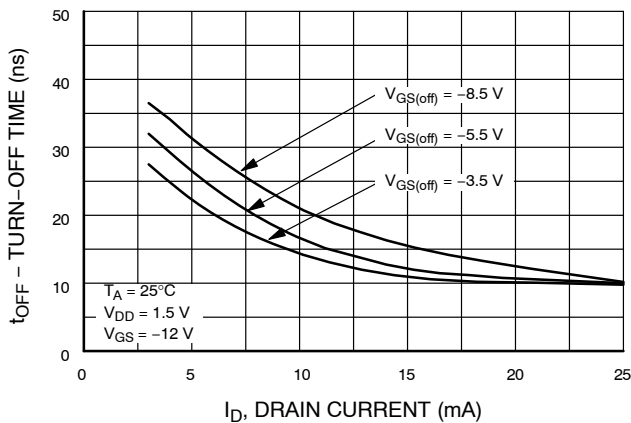


Figure 8. Switching Turn-Off Time vs. Drain Current

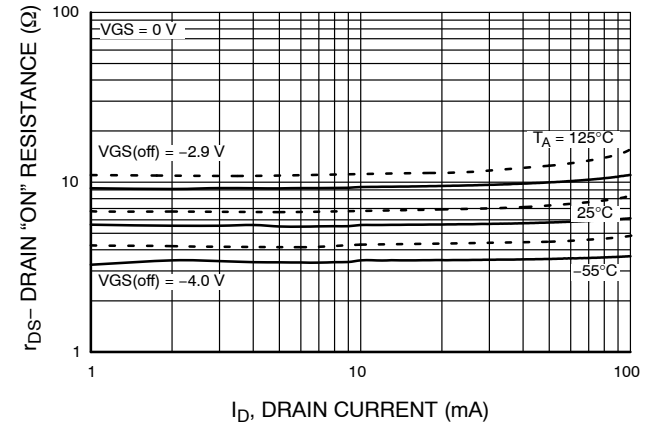


Figure 9. On Resistance vs. Drain Current

J109, MMBFJ108

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

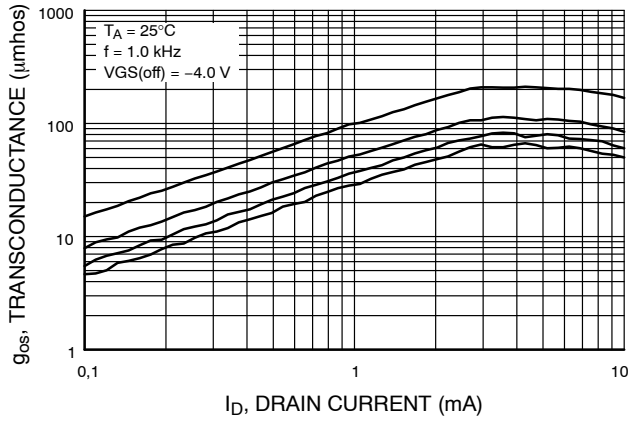


Figure 10. Output Conductance vs. Drain Current

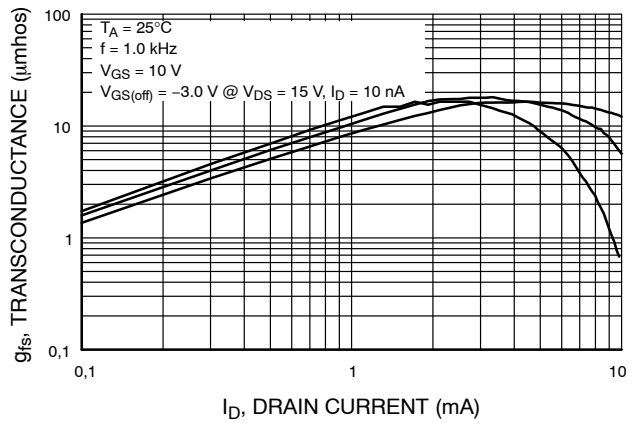


Figure 11. Output Conductance vs. Drain Current

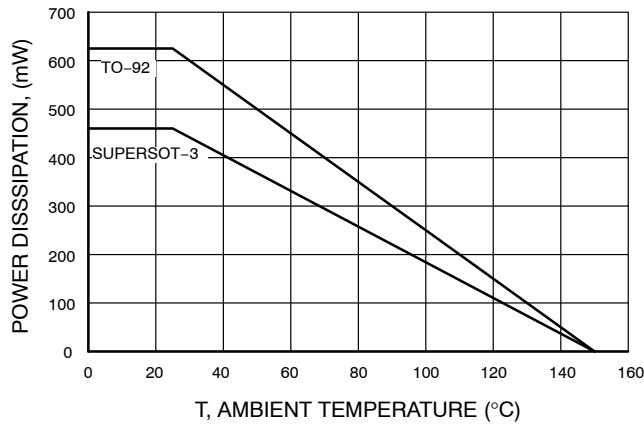


Figure 12. Power Dissipation vs. Ambient Temperature

ORDERING INFORMATION

Part Number	Top Mark	Package	Shipping [†]
J109	J109	TO-92 3L (Pb-Free)	10000 Units / Bulk
J109-D26Z	J109	TO-92 3L (Pb-Free)	2000 / Tape & Reel
MMBFJ108	l8	SSOT 3L (Pb-Free)	3000 / Tape & Reel

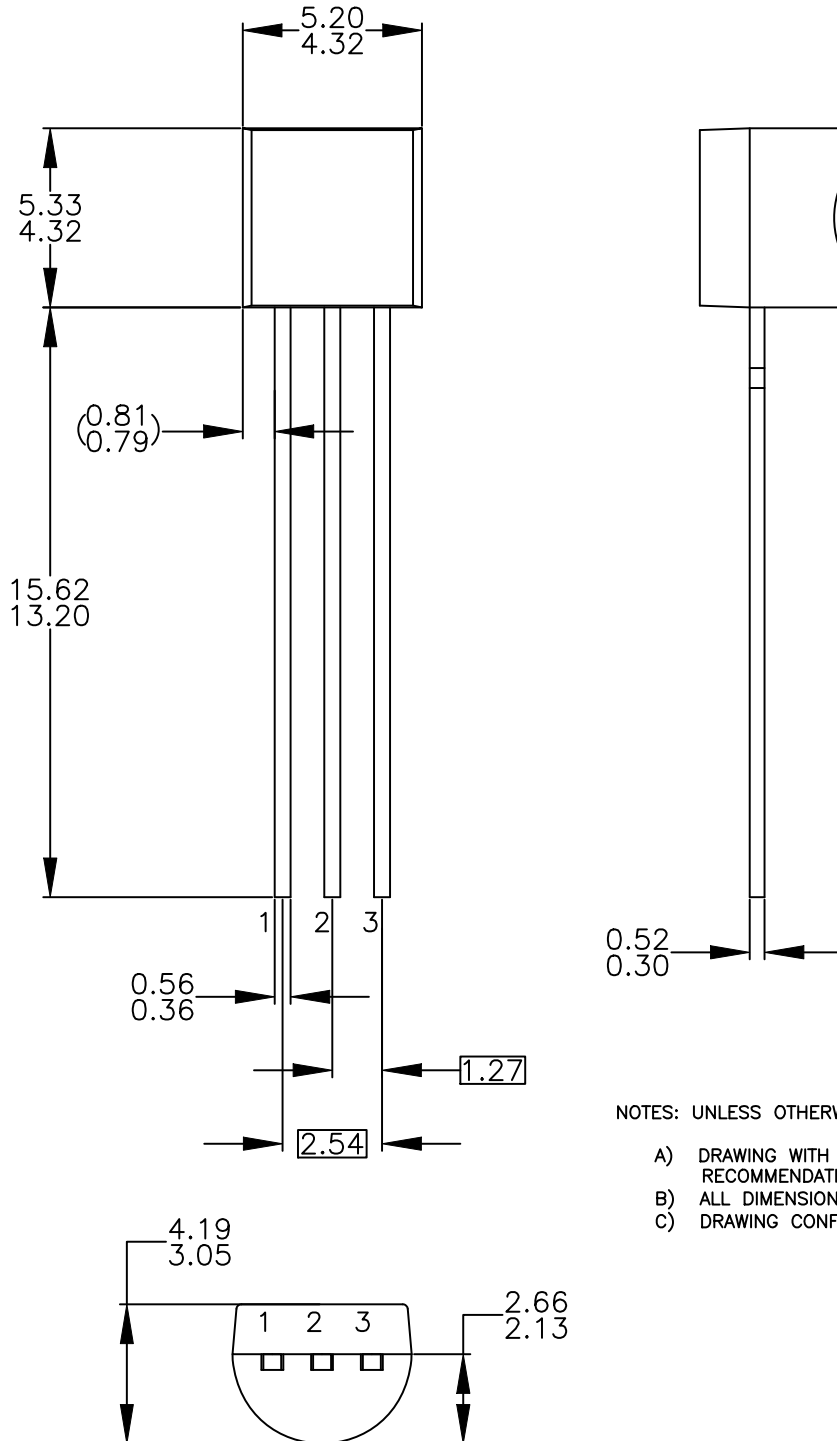
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

SUPERSOT is trademark of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

TO-92 3 4.825x4.76
CASE 135AN
ISSUE O

DATE 31 JUL 2016



NOTES: UNLESS OTHERWISE SPECIFIED

- A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DRAWING CONFORMS TO ASME Y14.5M-2009.

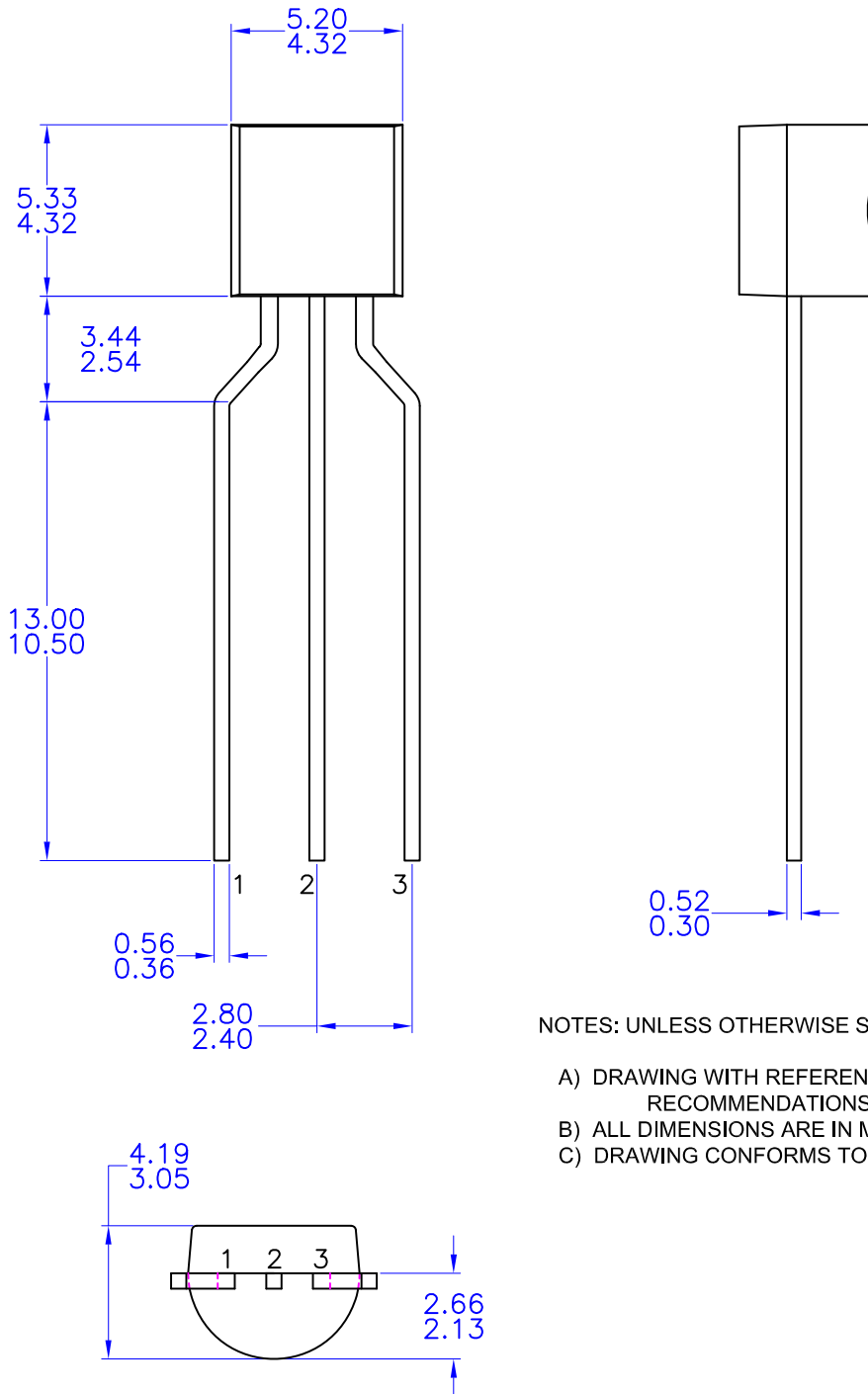
DOCUMENT NUMBER:	98AON13880G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TO-92 3 4.825X4.76	PAGE 1 OF 1

ON Semiconductor and **ON** are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

TO-92 3 4.83x4.76 LEADFORMED
CASE 135AR
ISSUE O


DATE 30 SEP 2016



NOTES: UNLESS OTHERWISE SPECIFIED

- A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DRAWING CONFORMS TO ASME Y14.5M-1994

DOCUMENT NUMBER:	98AON13879G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TO-92 3 4.83X4.76 LEADFORMED	PAGE 1 OF 1

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

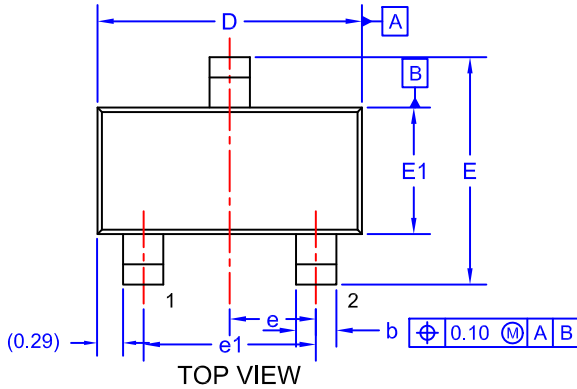
ON Semiconductor®



SOT-23/SUPERSOT™ -23, 3 LEAD, 1.4x2.9

CASE 527AG
ISSUE A

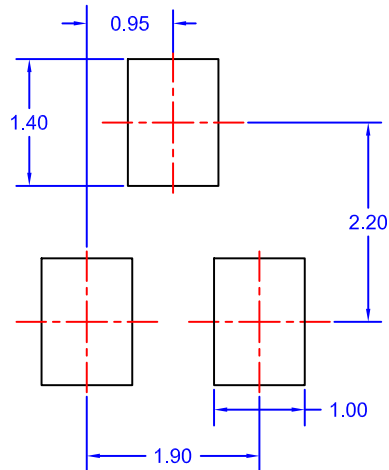
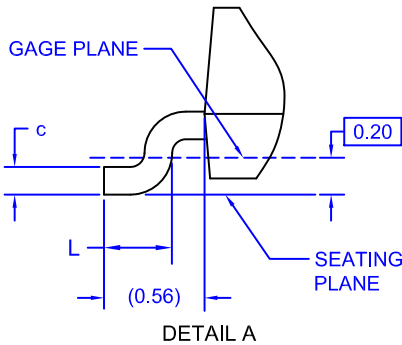
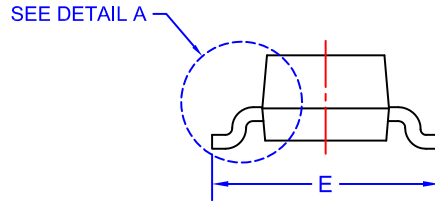
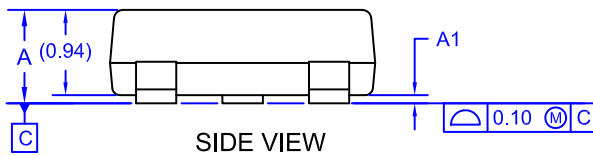
DATE 09 DEC 2019



NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.

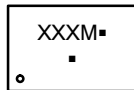
DIM	MIN.	NOM.	MAX.
A	0.85	0.95	1.12
A1	0.00	0.05	0.10
b	0.370	0.435	0.508
c	0.085	0.150	0.180
D	2.80	2.92	3.04
E	2.31	2.51	2.71
E1	1.20	1.40	1.52
e	0.95 BSC		
e1	1.90 BSC		
L	0.33	0.38	0.43



LAND PATTERN RECOMMENDATION*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXX = Specific Device Code
- M = Month Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON34319E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOT-23/SUPERSOT-23, 3 LEAD, 1.4X2.9	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.