J176, J177 P-Channel JFET

Features

- InterFET P0099F Geometry
- Low Noise: 8 nV/√Hz Typical
- Low Rds(on): 150 Ohms Typical
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

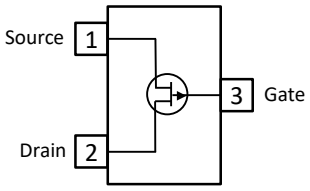
Applications

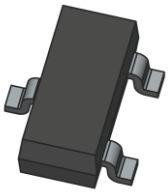
- Choppers
- Commutators
- Analog Switches

Description

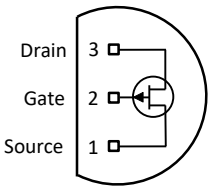
The 30V InterFET J176 and J177 JFET's are targeted for high gain low noise switching, commutator, and chopper applications.

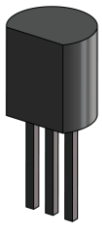
SOT23 Top View





TO-92 Bottom View





Product Summary

Parameters		J176 Min	J177 Min	Unit
BV_{GSS}	Gate to Source Breakdown Voltage	30	30	V
I_{DSS}	Drain to Source Saturation Current	-2	-1.5	mA
$V_{GS(off)}$	Gate to Source Cutoff Voltage	1	0.8	V

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
J176; J177	Through-Hole	TO-92	Bulk
SMPJ176; SMPJ177	Surface Mount	SOT23	Bulk
SMPJ176TR; SMPJ177TR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
J176COT; J177COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
J176CFT; J177CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		Value	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	30	V
I_{FG}	Continuous Forward Gate Current	50	mA
P_D	Continuous Device Power Dissipation	360	mW
P	Power Derating	3.27	mW/°C
T_J	Operating Junction Temperature	-55 to 125	°C
T_{STG}	Storage Temperature	-65 to 200	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

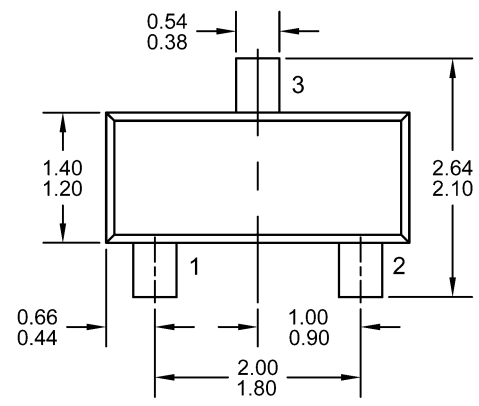
Parameters		Conditions	J176		J177		Unit
			Min	Max	Min	Max	
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	V_{DS} = 0V, I_G = 1µA	30		30		V
I_{GSS}	Gate to Source Reverse Current	V_{GS} = 20V, V_{DS} = 0V		1		1	nA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = -15V, I_D = -10nA	1	4	0.8	2.25	V
I_{DSS}	Drain to Source Saturation Current	V_{GS} = 0V, V_{DS} = -15V (Pulsed)	-2	-35	-1.5	-20	mA
$I_{D(OFF)}$	Drain Cutoff Current	V_{DS} = -15V, V_{GS} = 10V		-1		-1	nA

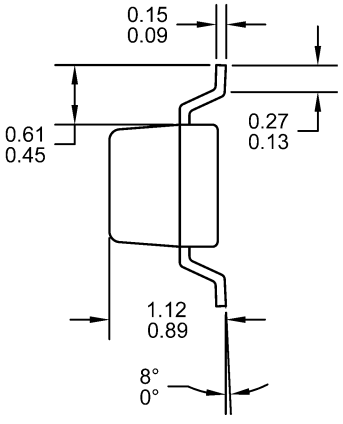
Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

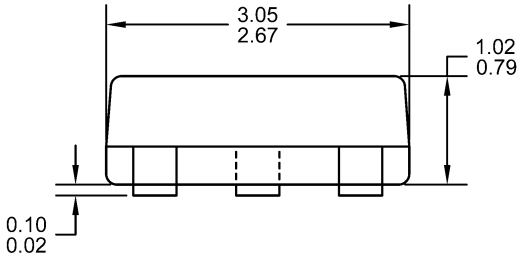
Parameters		Conditions	J176		J177		Unit
			Min	Max	Min	Max	
$R_{DS(ON)}$	Drain to Source ON Resistance	V_{DS} <= 0.1V, V_{GS} = 0V, f = 1kHz		250		300	Ω
C_{gd}	Drain Gate Capacitance	V_{DS} = 0V, V_{GS} = 10V, f = 1MHz	5.5 (typ)		5.5 (typ)		pF
C_{gs}	Input Capacitance	V_{DS} = 0V, V_{GS} = 10V, f = 1MHz	5.5 (typ)		5.5 (typ)		pF
$C_{gd} + C_{gs}$	Drain + Source Gate Capacitance	V_{DS} = V_{GS} = 0V, f = 1MHz	32 (typ)		32 (typ)		pF
$t_{d(ON)}$	Turn ON Delay Time	V_{DD} = -6V J176: $V_{GS(OFF)}$ = 6V, R_L = 5600 Ω J177: $V_{GS(OFF)}$ = 3V, R_L = 10000 Ω	15 (typ)		20 (typ)		ns
t_r	Rise Time		20 (typ)		25 (typ)		ns
$t_{d(OFF)}$	Turn OFF Delay Time		15 (typ)		20 (typ)		ns
t_f	Fall Time		20 (typ)		25 (typ)		ns

SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data

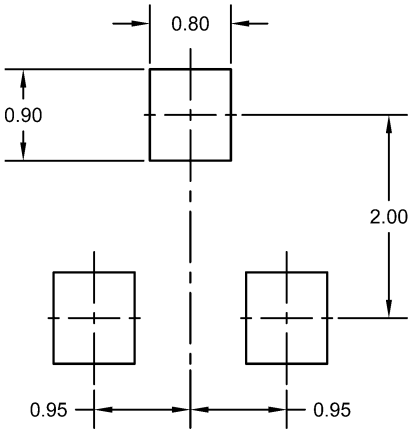






1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.