The documentation and process conversion measures necessary to comply with this document shall be completed by 30 June 2013.

INCH-POUND

MIL-PRF-19500/376K
30 March 2013
SUPERSEDING
MIL-PRF-19500/376J
20 November 2010

PERFORMANCE SPECIFICATION SHEET

* SEMICONDUCTOR DEVICE, TRANSISTOR, NPN, SILICON, LOW-POWER,
TYPES 2N2484, 2N2484UA, 2N2484UB, 2N2484UBC, 2N2484UBN, 2N2484UBCN JAN, JANTX, JANTXV,
JANS, JANSM, JANSD, JANSP, JANSL, JANSR, JANSF, JANSG, JANSH JANHCA, JANHCB, JANKCA,
JANKCB, JANKCM, JANKCD, JANKCP, JANKCL, JANKCR, JANKCF, JANKCG, AND JANKCH

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for NPN, silicon, low-power transistors. Four levels of product assurance are provided for each device type as specified in MIL-PRF-19500. Two levels of product assurance are provided for die. RHA level designators “M”, “D”, “P“, “L”, “R”, “F’, “G” and “H” are appended to the device prefix to identify devices, which have passed RHA requirements.

* 1.2 Physical dimensions. See figure 1 (similar to TO-18), figure 2, (surface mount case outlines UA), figure 3, (surface mount case outlines UB, UBC, UBN, and UBCN), and figures 4 and 5 (die).

* 1.3 Maximum ratings. Unless otherwise specified T_A = +25°C.

Types	P_T (1) T_A = +25°C	V_{CBO}	V_{EBO}	V_{CEO}	I_C	T_J and T_{STG}	$R_{\theta JA}$ (2)	$R_{\theta JSP}$ (2)
	mW	V dc	V dc	V dc	mA dc	°C	°C/W	°C/W
2N2484	360	60	6	60	50	-65 to +200	325	N/A
2N2484UA	360	60	6	60	50	-65 to +200	275	110
2N2484UB, UBN	360	60	6	60	50	-65 to +200	350	100
2N2484UBC, UBCN	360	60	6	60	50	-65 to +200	350	100

(1) For derating see figures 6, 7, and 8.
(2) For thermal impedance see figures 9, 10, 11, 12, and 13.

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil.

1.4 Primary electrical characteristics. Unless otherwise specified, T_A = +25°C.

Limits	h_{fe}	C_{obo}	$\|h_{fe}\|2$	$V_{CE(sat)}$ (1)
	V_{CE} = 5 V dc I_C = 1 mA dc f = 1 kHz	I_E = 0 V_{CB} = 5 V dc 100 kHz ≤ f ≤ 1 MHz	I_C = 500 μA dc V_{CE} = 5 V dc f = 30 MHz	I_C = 1.0 mA dc I_B = 0.1 mA dc
		pF		V dc
Min	250		2.0	
Max	900	5.0	7.0	0.3

Limits	NF I_C = 10 μA dc, V_{CE} = 5 V dc R_g = 10 kΩ			h_{FE2}	h_{FE5}
	f = 100 Hz	f = 1000 Hz	f = 10 kHz	V_{CE} = 5 V dc I_C = 10 μA dc	V_{CE} = 5 V dc I_C = 1 mA dc
	dB	dB	dB		
Min				200	250
Max	7.5	3	2	500	800

(1) Pulsed (see 4.5.1).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

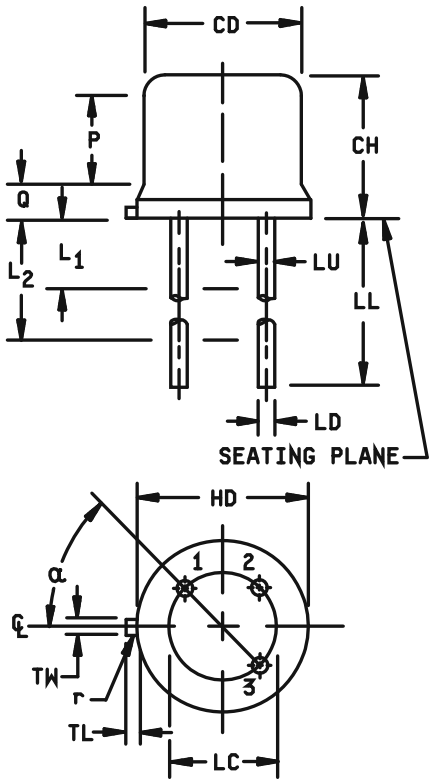
DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at https://assist.dla.mil/quicksearch or https://assist.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

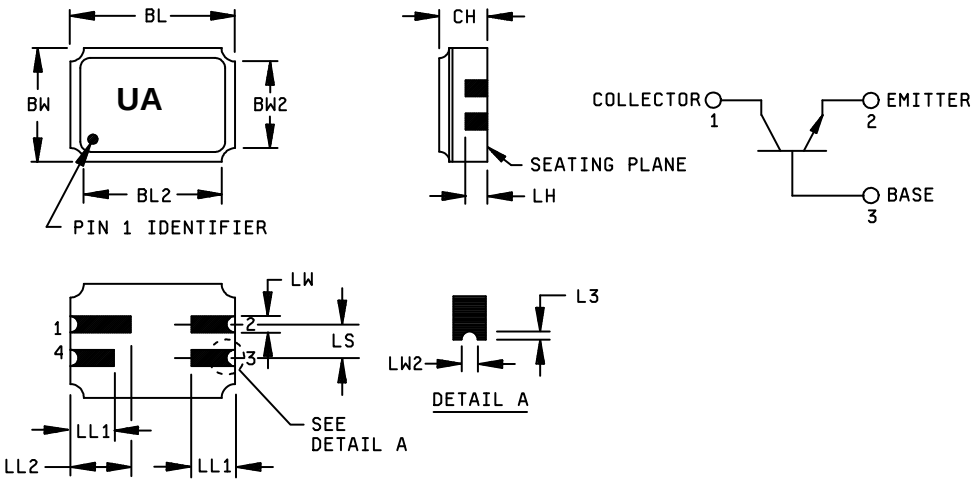
2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.178	.195	4.52	4.95	
CH	.170	.210	4.32	5.33	
HD	.209	.230	5.31	5.84	
LC	.100 TP		2.54 TP		6
LD	.016	.021	0.41	0.53	7,8
LL	.500	.750	12.70	19.05	7,8
LU	.016	.019	0.41	0.48	7,8
L_1		.050		1.27	7,8
L_2	.250		6.35		7,8
P	.100		2.54		
Q		.040		1.02	5
TL	.028	.048	0.71	1.22	3,4
TW	.036	.046	0.91	1.17	3
r		.010		0.25	10
α	45° TP		45° TP		6



NOTES:
1. Dimension are in inches.
2. Millimeters are given for general information only.
3. Beyond r (radius) maximum, TW shall be held for a minimum length of .011 inch (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC.
7. Dimension LU applies between L_1 and L_2. Dimension LD applies between L_2 and LL minimum. Diameter is uncontrolled in L_1 and beyond LL minimum.
8. All three leads.
9. The collector shall be internally connected to the case.
10. Dimension r (radius) applies to both inside corners of tab.
11. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
12. Lead 1 = emitter, lead 2 = base, lead 3 = collector.

FIGURE 1. Physical dimensions (similar to TO-18).

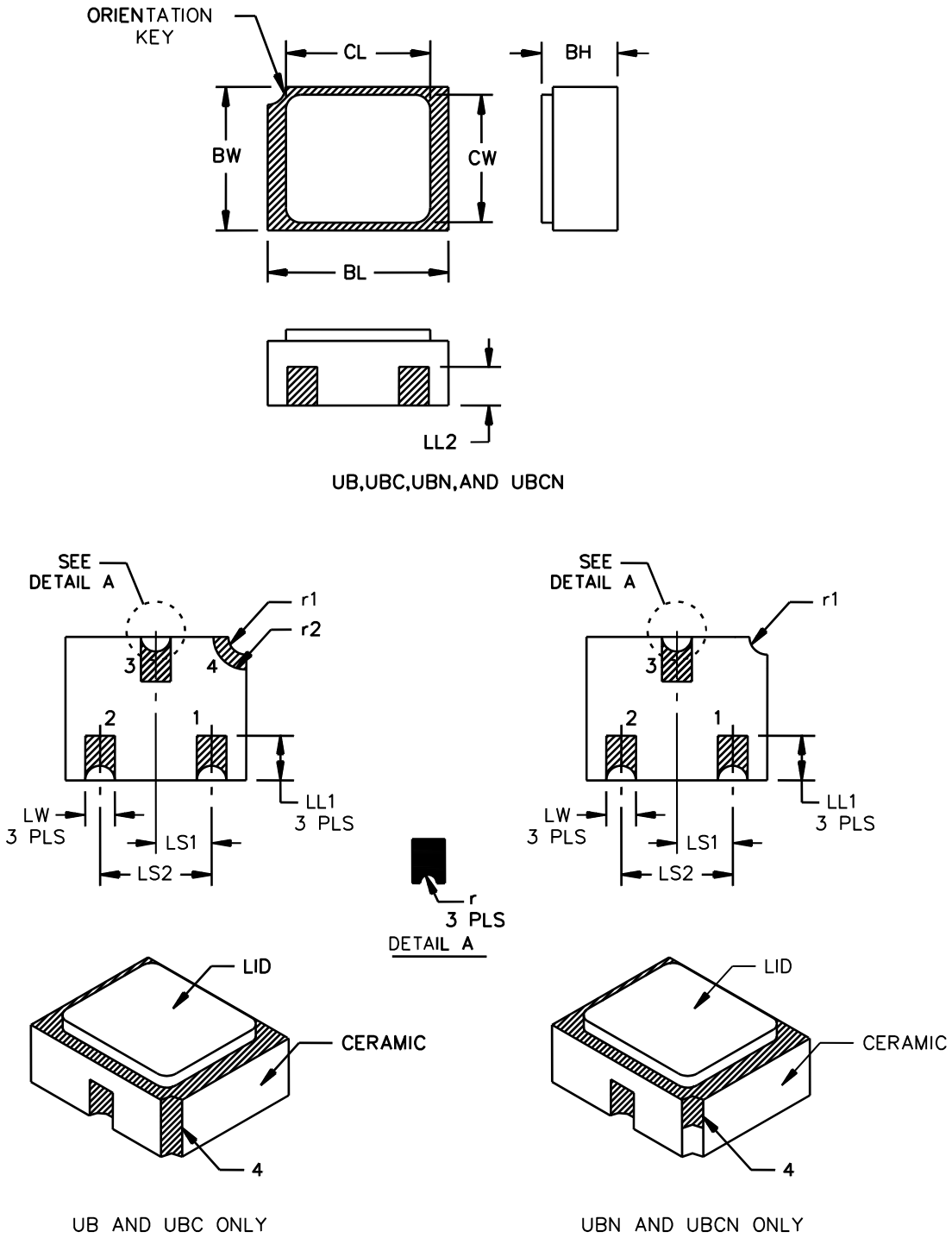


Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.215	.225	5.46	5.71	
BL2		.225		5.71	
BW	.145	.155	3.68	3.94	
BW2		.155		3.94	
CH	.061	.075	1.55	1.91	3
L3	.003		0.08		5
LH	.029	.042	0.74	1.07	
LL1	.032	.048	0.81	1.22	
LL2	.072	.088	1.83	2.24	
LS	.045	.055	1.14	1.39	
LW	.022	.028	0.56	0.71	
LW2	.006	.022	0.15	0.56	5

Pin no.	1	2	3	4
Transistor	Collector	Emitter	Base	N/C

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Dimension CH controls the overall package thickness. When a window lid is used, dimension CH must increase by a minimum of .010 inch (0.254 mm) and a maximum of .040 inch (1.020 mm).
4. The corner shape (square, notch, radius) may vary at the manufacturer's option, from that shown on the drawing.
* 5. Dimensions LW2 minimum and L3 minimum and the appropriate castellation length define an unobstructed three-dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on the bottom two layers, optional on the top ceramic layer.) Dimension LW2 maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.
6. The co-planarity deviation of all terminal contact points, as defined by the device seating plane, shall not exceed .006 inch (0.15 mm) for solder dipped leadless chip carriers.
7. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

* FIGURE 2. Physical dimensions, surface mount (2N2484UA).

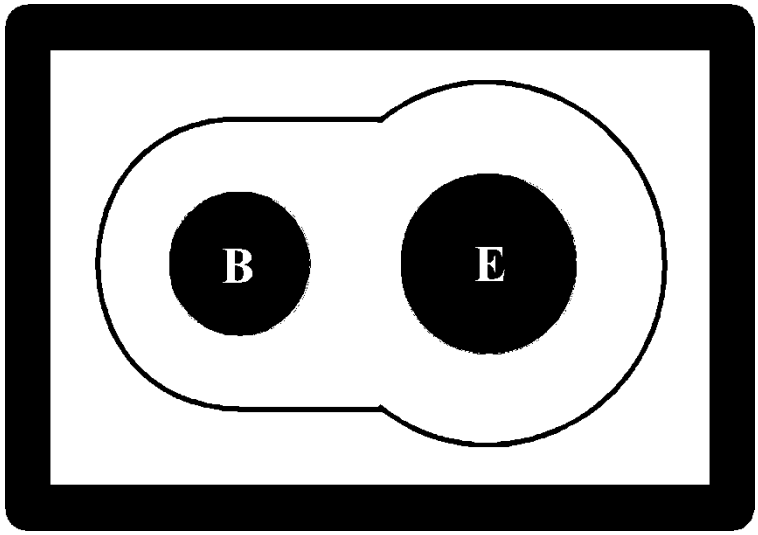


* FIGURE 3. Physical dimensions, surface mount (2N2484UB, UBC, UBN, and UBCN)

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.115	.128	2.92	3.25	
BW	.095	.108	2.41	2.74	
BH	.046	.056	1.17	1.42	UB only, 4
BH	.046	.056	1.17	1.42	UBN only, 5
BH	.055	.069	1.40	1.75	UBC only, 6
BH	.055	.069	1.40	1.75	UBCN only, 7
CL		.128		3.25	
CW		.108		2.74	
LL1	.022	.038	0.56	0.97	3 PLS
LL2	.014		0.356		3 PLS
LS_1	.035	.039	0.89	0.99	
LS_2	.071	.079	1.80	2.01	
LW	.016	.024	0.41	0.61	
r		.008		0.20	6
r1		.012		0.30	8
r2		.022		0.56	UB & UBC only, 8

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Hatched areas on package denote metallized areas.
4. UB only: Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Pad 4 = Shielding connected to the lid.
5. UBN only: Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Isolated lid with 3 pads only.
6. UBC (ceramic lid) only: Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Pad 4 = connected to the lid braze ring.
7. UBCN (ceramic lid) only: Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Isolated lid with 3 pads only.
8. For design reference only.
9. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

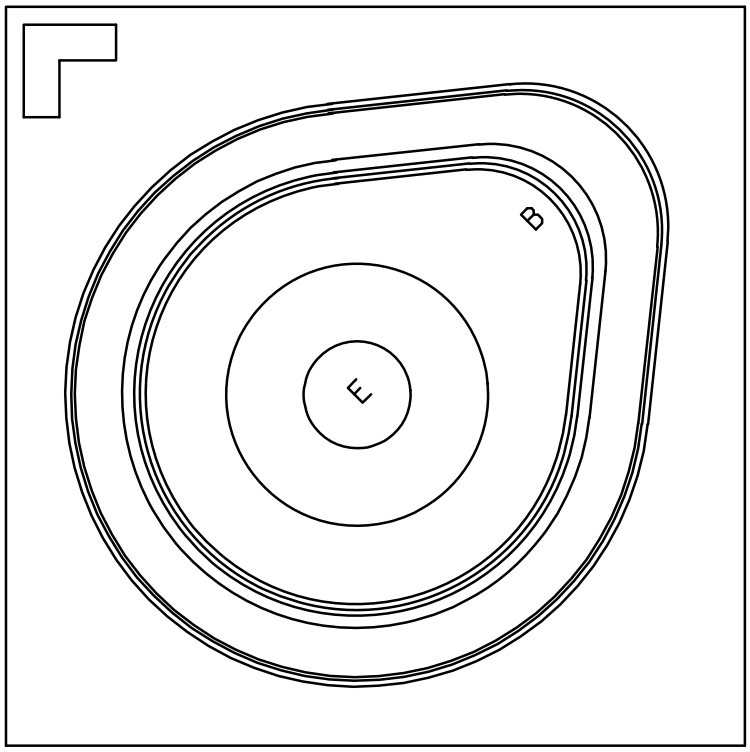
* FIGURE 3. Physical dimensions, surface mount (UB, UBN, UBC and UBCN versions) - Continued.



A- version

NOTES:
1. Die size: .015 inch (0.381 mm) x .019 inch (0.483 mm) ±.001 inch (0.025 mm).
2. Die thickness: .010 inch (0.254 mm) ±.0015 inch (0.038 mm).
3. Top metal: Aluminum 15,000 Å minimum, 18,000 Å nominal.
4. Back metal: Gold 3,500 Å minimum, 5,000 Å nominal.
5. Backside: Collector.
6. Bonding pad: B = .003 inch (0.076 mm), E = .004 inch (0.102 mm) diameter.
7. Millimeter equivalents are given for general information only.

FIGURE 4. Physical dimensions, JANHC and JANKC die, A - version.



B - version

NOTES:
1. Die size: .018 inch (0.457 mm) x .018 inch (0.457 mm).
2. Die thickness: .008 inch (0.203 mm) ±.0016 inch (0.041 mm).
3. Base pad: .0025 inch (0.064 mm) diameter.
4. Emitter pad: .003 inch (0.076 mm) diameter.
5. Back metal: Gold, 6,500 ±1,950 Å.
6. Top metal: Aluminum, 19,500 ±2,500 Å.
7. Back side: Collector.
8. Glassivation: SiO_2, 7,500 ±1,500 Å.
9. Millimeter equivalents are given for general information only.

FIGURE 5. Physical dimensions, JANHC and JANKC die, B - version.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows.

PCB	Printed circuit board
$R_{\theta JA}$	Thermal resistance junction to ambient.
UA, UB, and UBC	Surface mount case outlines (see figures 2, 3, and 4).

* 3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figures 1, 2, 3, 4, and 5. No lead (Pb) shall be used in the construction of the die bonds.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Radiation hardness assurance (RHA). Radiation hardness assurance requirements, PIN designators, and test levels shall be as defined in MIL-PRF-19500.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.7 Electrical test requirements. The electrical test requirements shall be as specified in table I.

* 3.8 Marking. Marking shall be in accordance with MIL-PRF-19500, except for the UB, UBC, UBN, and UBCN suffix packages. Marking on the UB, UBC, UBN, and UBCN packages shall consist of an abbreviated part number, the date code, and the manufacturers symbol or logo. The prefixes JAN, JANTX, JANTXV, and JANS can be abbreviated as J, JX, JV, and JS respectively. The "2N" prefix can also be omitted. The radiation hardened designator M, D, P, L, R, F, G, or H shall immediately precede (or replace) the device “2N” identifier (depending upon degree of abbreviation required).

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and tables I, II, III, and IV).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1. JANHC and JANKC qualification. JANHC and JANKC qualification inspection shall be in accordance with MIL-PRF-19500.

4.2.2 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.2.2.1 Group E thermal response. With extremely small junction devices such as this one, a true thermal impedance cannot be measure, only calculated. While "thermal response" has been substituted for "thermal impedance" herein, the terms, units and procedure as essentially unchanged. Each supplier shall submit a thermal response ($Z_{\theta JX}$) histogram of the entire qualification lot. The histogram data shall be taken prior to the removal of devices that are atypical for thermal response. Thermal response curves (from $Z_{\theta JX}$ test pulse time to $R_{\theta JX}$ minimum steady-state time) of the best device in the qual lot and the worst device in the qual lot (that meets the supplier proposed screening limit), or from the thermal grouping, shall be submitted. The optimal test conditions and proposed initial thermal response screening limit shall be provided in the qualification report. Data indicating how the optimal test conditions were derived for $Z_{\theta JX}$ shall also be submitted. The proposed maximum thermal response $Z_{\theta JX}$ screening limit shall be submitted. The qualifying activity may approve a different $Z_{\theta JX}$ limit for conformance inspection end-point measurements as applicable**.** Equivalent data, procedures, or statistical process control plans may be used for part, or all, of the above requirements. The approved thermal response conditions and limit for $Z_{\theta JX}$ shall be used by the supplier in screening and table I, subgroup 2. The approved thermal resistance conditions for $R_{\theta JX}$ shall be used by the supplier for conformance inspection. For product families with similar thermal characteristics based on the same physical and thermal die, package, and construction combination (thermal grouping), the supplier may use the same thermal response curves.

* 4.3 Screening (JANS, JANTX, and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500)	Measurement	
	JANS level	JANTX and JANTXV levels
(1) 3c	Thermal response, method 3131 of MIL-STD-750. (see 4.3.3)	Thermal response, method 3131 of MIL-STD-750. (see 4.3.3)
9	I_{CBO2}, h_{FE4}	Not applicable
10	48 hours minimum	48 hours minimum
11	I_{CBO2}; h_{FE4}; ΔI_{CBO2} = 100 percent of initial value or 2 nA dc, whichever is greater. Δh_{FE4} = ±15 percent	I_{CBO2} ,h_{FE4}
12	See 4.3.2	See 4.3.2
13	Subgroups 2 and 3 of table I herein; ΔI_{CBO2} = 100 percent of initial value or 2 nA dc, whichever is greater; Δh_{FE4} = ±15 percent	Subgroup 2 of table I herein; ΔI_{CBO2} = 100 percent of initial value or 2 nA dc, whichever is greater; Δh_{FE4} = ±25 percent

* (1) Shall be performed anytime after temperature cycling, screen 3a; JANTX and JANTXV levels do not need to be repeated in screening requirements.

4.3.1 Screening (JANHC and JANKC). Screening for JANHC and JANKC die shall be in accordance with MIL-PRF-19500 "Discrete Semiconductor Die/Chip Lot Acceptance". Burn-in duration for the JANKC level follows JANS requirements; the JANHC follows JANTX requirements.

4.3.2 Power burn-in conditions. Power burn-in conditions are as follows: V_{CB} = 10 to 30 V dc, power shall be applied to achieve T_J = +135°C minimum using a minimum P_D = 75 percent of P_T maximum rated as defined in 1.3. With approval of the qualifying activity and preparing activity, alternate burn-in criteria (hours, bias conditions, T_J, and mounting conditions) may be used for JANTX and JANTXV quality levels. A justification demonstrating equivalence is required. In addition, the manufacturing site's burn-in data and performance history will be essential criteria for burn-in modification approval.

4.3.3 Thermal response. For very small junction devices such as this, the term thermal response shall be used in lieu of thermal impedance although measurements shall be performed the same way as thermal impedance in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{MD} (and V_C where appropriate). Measurement delay time (t_{MD}) = 70 μs max. See group E, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein. If alternate screening is being performed in accordance with MIL-PRF-19500, a sample of screened devices shall be submitted to and pass the requirements of subgroups 1 and 2, of table I herein, inspection only (table E-VIb, group B, subgroup 1 is not required to be performed again if group B has already been satisfied in accordance with 4.4.2).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500 and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-VIa (JANS) of MIL-PRF-19500 and 4.4.2.1. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein. Delta requirements shall be in accordance with table IV herein. See 4.4.2.2 for JAN, JANTX, and JANTXV group B testing. Electrical measurements (end-points) and delta requirements for JAN, JANTX, and JANTXV shall be after each step in 4.4.2.2 and shall be in accordance with table I, subgroup 2 herein. Delta requirements shall be after each step and shall be in accordance with table IV herein.

4.4.2.1 Group B inspection (JANS), table E-VIa of MIL-PRF-19500.

Subgroup	Method	Condition
B4	1037	V_{CB} = 10 V dc, 2,000 cycles, adjust device current, or power, to achieve a minimum ΔT_J of +100°C.
B5	1027	V_{CB} = 10 V dc; $P_D \geq$ 100 percent of maximum rated P_T (see 1.3). (NOTE: If a failure occurs, resubmission shall be at the test conditions of the original sample.) Option 1: 96 hours minimum sample size in accordance with MIL-PRF-19500, table E-VIa, adjust T_A or P_D to achieve T_J = +275°C minimum. Option 2: 216 hours minimum, sample size = 45, c = 0; adjust T_A or P_D to achieve a T_J = +225°C minimum.

4.4.2.2 Group B inspection, (JAN, JANTX, and JANTXV). Separate samples may be used for each step. In the event of a lot failure, the resubmission requirements of MIL-PRF-19500 shall apply. In addition, all catastrophic failures during CI shall be analyzed to the extent possible to identify root cause and corrective action. Whenever a failure is identified as wafer lot or wafer processing related, the entire wafer lot and related devices assembled from the wafer lot shall be rejected unless an appropriate determined corrective action to eliminate the failures mode has been implemented and the devices from the wafer lot are screened to eliminate the failure mode.

Step	Method	Condition
1	1026	Steady-state life: 1,000 hours minimum, V_{CB} = 10 V dc, power shall be applied to achieve T_J = +150°C minimum using a minimum of P_D = 75 percent of maximum rated P_T as defined in 1.3. n = 45 devices, c = 0. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.
2	1048	Blocking life, T_A = +150°C, V_{CB} = 80 percent of rated voltage, 48 hours minimum. n = 45 devices, c = 0.
3	1032	High-temperature life (non-operating), t = 340 hours, T_A = +200°C. n = 22, c = 0.

4.4.2.3 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

a. For JAN, JANTX, and JANTXV, samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot. For JANS, samples shall be selected from each inspection lot. See MIL-PRF-19500.

b. Shall be chosen from an inspection lot that has been submitted to and passed table I, subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (subgroups B4 and B5 for JANS, and group B for JAN, JANTX, and JANTXV) may be pulled prior to the application of final lead finish.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the test and conditions specified for subgroup testing in table E-VII of MIL-PRF-19500, and in 4.4.3.1 (JANS) and 4.4.3.2 (JAN, JANTX, and JANTXV) herein for group C testing. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein. Delta requirements shall be in accordance with table IV herein.

* 4.4.3.1 Group C inspection (JANS), table E-VII of MIL-PRF-19500.

	Subgroup	Method	Condition
*	C2	2036	Test condition E; (not applicable for UA, UB, UBC, UBN, and UBCN devices).
	C5	3131	$R_{\theta JA}$ only, as applicable (see 1.3) and in accordance with thermal impedance curves.
	C6	1026	1,000 hours at V_{CB} = 10 V dc; power shall be applied to achieve T_J = +150°C minimum and a minimum of P_D = 75 percent of maximum rated P_T as defined in 1.3 n = 45, c = 0. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.

* 4.4.3.2 Group C inspection (JAN, JANTX, and JANTXV), table E-VII of MIL-PRF-19500.

Subgroup	Method	Condition
* C2	2036	Test condition E; (not applicable for UA, UB, UBC, UBN, and UBCN devices).
C5	3131	$R_{\theta JA}$ only, as applicable (see 1.3) and in accordance with thermal impedance curves.
C6		Not applicable.

4.4.3.3 Group C sample selection. Samples for subgroups in group C shall be chosen at random from any inspection lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes table I tests herein for conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for C6 life test may be pulled prior to the application of final lead finish. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

* 4.4.4 Group D inspection. Conformance inspection for hardness assured JANS, JANJ, and JANTXV types shall include the group D tests specified in table II herein. These tests shall be performed as required in accordance with MIL-PRF-19500 and method 1019 of MIL-STD-750, for total ionizing dose or method 1017 of MIL-STD-750 for neutron fluence as applicable (see 6.2 herein), except group D, subgroup 2 may be performed separate from other subgroups. Alternate package options may also be substituted for the testing provided there is no adverse effect to the fluence profile.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table III herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein; delta measurements shall be in accordance with the applicable steps of table IV.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

* TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 1 2/						
* Visual and mechanical examination 3/	2071					
Solderability 3/ 4/	2026	n = 15 leads, c = 0				
Resistance to solvents 3/ 4/ 5/	1022	n = 15 devices, c = 0				
Temp cycling 3/ 4/	1051	Test condition C, 25 cycles. n = 22 devices, c = 0				
Hermetic seal 4/ 6/ Fine leak Gross leak	1071	n = 22 devices, c = 0				
Electrical measurements 4/		Table I, subgroup 2				
Bond strength 3/ 4/	2037	Precondition T_A = +250°C at t = 24 hours or T_A = +300°C at t = 2 hours n = 11 wires, c = 0				
Decap internal visual (design verification) 4/	2075	n = 4 devices, c = 0				
Subgroup 2						
Thermal response	3131	See 4.3.3	$Z_{\theta JX}$			°C/W
Collector to emitter breakdown voltage	3011	Bias condition D; I_C = 10 mA dc pulsed (see 4.5.1)	$V_{(BR)CEO}$	60		V dc
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 60 V dc	I_{CBO1}		10	µA dc
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 6 V dc	I_{EBO1}		10	µA dc
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 45 V dc	I_{CBO2}		5	nA dc
Collector to emitter cutoff current	3041	Bias condition D; V_{CE} = 5 V dc	I_{CEO}		2	nA dc
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 5 V dc	I_{EBO2}		2	nA dc
Collector to emitter cutoff current	3041	Bias condition C; V_{CE} = 45 V dc	I_{CES}		5	nA dc
Forward-current transfer ratio	3076	V_{CE} = 5 V dc; I_C = 1 µA dc	h_{FE1}	45		
Forward-current transfer ratio	3076	V_{CE} = 5 V dc; I_C = 10 µA dc	h_{FE2}	200	500	
Forward-current transfer ratio	3076	V_{CE} = 5 V dc; I_C = 100 µA dc	h_{FE3}	225	675	

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - Continued						
Forward-current transfer ratio	3076	V_{CE} = 5 V dc; I_C = 500 μA dc	h_{FE4}	250	800	
Forward-current transfer ratio	3076	V_{CE} = 5 V dc; I_C = 1 mA dc	h_{FE5}	250	800	
Forward-current transfer ratio	3076	V_{CE} = 5 V dc; I_C = 10 mA dc pulsed (see 4.5.1)	h_{FE6}	225	800	
Collector to emitter voltage (saturated)	3071	I_C = 1.0 mA dc; I_B = 100 μA dc	$V_{CE(sat)}$		0.3	V dc
Base emitter voltage (nonsaturated)	3066	Test condition B; V_{CE} = 5 V dc; I_C = 100 μA dc	$V_{BE(ON)}$	0.5	0.7	V dc
Subgroup 3						
High-temperature operation		T_A = +150°C				
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 45 V dc	I_{CBO3}		10	μA dc
Low-temperature operation		T_A = -55°C				
Forward-current transfer ratio	3076	V_{CE} = 5 V dc; I_C = 10 μA dc	h_{FE7}	35		
Subgroup 4						
Magnitude of common emitter small-signal short-circuit forward-current transfer ratio	3306	V_{CE} = 5 V dc; I_C = 50 μA dc; f = 5 MHz	$\|h_{fe}\|1$	3.0		
Magnitude of common emitter small-signal short-circuit forward- current transfer ratio	3306	V_{CE} = 5 V dc; I_C = 500 μA dc; f = 30 MHz	$\|h_{fe}\|2$	2.0	7.0	
Small-signal open-circuit output admittance	3216	V_{CE} = 5 V dc; I_C = 1.0 mA dc; f = 1 kHz	h_{oe}		40	μmhos
Small-signal open-circuit reverse-voltage transfer ratio	3211	V_{CE} = 5 V dc; I_C = 1.0 mA dc; f = 1 kHz	h_{re}		8.0×10^{-4}	
Small-signal short-circuit input impedance	3201	V_{CE} = 5 V dc; I_C = 1 mA dc; f = 1 kHz	h_{ie}	3.5	24	kΩ
Small-signal short-circuit forward current transfer ratio	3206	V_{CE} = 5 V dc; I_C = 1 mA dc; f = 1 kHz	h_{fe}	250	900	
Open circuit output capacitance	3236	V_{CB} = 5 V dc; I_E = 0; 100 kHz ≤ f ≤ 1 MHz	C_{obo}		5.0	pF

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 4 - Continued						
Input capacitance (output open-circuited)	3240	V_{EB} = 0.5 V dc; I_C = 0; 100 kHz ≤ f ≤ 1 MHz	C_{ibo}		6.0	pF
Noise figure	3246	f = 100 Hz; V_{CE} = 5 V dc; I_C = 10 μA dc; R_g = 10 kΩ;	NF1		7.5	dB
Noise figure	3246	f = 1 kHz; V_{CE} = 5 V dc; I_C = 10 μA dc; R_g = 10 kΩ;	NF2		3	dB
Noise figure	3246	f = 10 kHz; V_{CE} = 5 V dc; I_C = 10 μA dc; R_g = 10 kΩ;	NF3		2	dB
Noise figure (wideband)	3246	Noise bandwidth = 10 Hz to 15.7 kHz; V_{CE} = 5 V dc; I_C = 10 μA dc; R_g = 10 kΩ;	NF4		3	dB
Subgroups 5 and 6						
Not applicable						
Subgroup 7						

1/ For sampling plan see MIL-PRF-19500.
2/ For resubmission of failed test in subgroup 1 of table I, double the sample size of the failed test or sequence of tests. A failure in table I, subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.
3/ Separate samples may be used.
4/ Not required for JANS devices.
5/ Not required for laser marked devices.
6/ This hermetic seal test is an end-point to temp-cycling in addition to electrical measurements.

TABLE II. Group D inspection.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 1 4/						
Neutron irradiation	1017	Neutron exposure V_{CES} = 0 V.				
Collector to emitter breakdown voltage	3011	Bias condition D; I_C = 10 mA dc pulsed (see 4.5.1)	$V_{(BR)CEO}$	60		V dc
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 60 V dc	I_{CBO1}		20	µA dc
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 6 V dc	I_{EBO1}		20	µA dc
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 45 V dc	I_{CBO2}		10	nA dc
Collector to emitter cutoff current	3041	Bias condition D; V_{CE} = 5 V dc	I_{CEO}		4	nA dc
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 5 V dc	I_{EBO2}		4	nA dc
Collector to emitter cutoff current	3041	Bias condition C; V_{CE} = 45 V dc	I_{CES}		10	nA dc
Forward-current transfer ratio M through H2N2484	3076	V_{CE} = 5 V dc; I_C = 1.0 µA dc.	[h_{FE1}] 5/	[22.5]		
Forward-current transfer ratio M through H2N2484	3076	V_{CE} = 5 V dc; I_C = 10 µA dc.	[h_{FE2}] 5/	[100]	500	
Forward-current transfer ratio M through H2N2484	3076	V_{CE} = 5 V dc; I_C = 100 µA dc.	[h_{FE3}] 5/	[112.5]	675	
Forward-current transfer ratio M through H2N2484	3076	V_{CE} = 5 V dc; I_C = 500 µA dc.	[h_{FE4}] 5/	[125]	800	
Forward-current transfer ratio M through H2N2484	3076	V_{CE} = 5 V dc; I_C = 1.0 mA dc.	[h_{FE5}] 5/	[125]	800	
Forward-current transfer ratio M through H2N2484	3076	V_{CE} = 5 V dc; I_C = 10 mA dc.	[h_{FE6}] 5/	[112.5]	800	
Collector-emitter saturation voltage	3071	I_C = 1.0 mA dc; I_B = 100 µA dc.	$V_{CE(sat)1}$		.35	V dc
* Base emitter voltage (nonsaturated)	3066	Test condition B; V_{CE} = 5 V dc; I_C = 100 µA dc	$V_{BE(ON)}$	0.5	0.81	V dc

See footnotes at end of table.

TABLE II. Group D inspection - Continued.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 2						
Total dose irradiation	1019	Gamma exposure V_{CES} = 48 V.				
Collector to emitter breakdown voltage	3011	Bias condition D; I_C = 10 mA dc pulsed (see 4.5.1)	$V_{(BR)CEO}$	60		V dc
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 60 V dc	I_{CBO1}		20	µA dc
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 6 V dc	I_{EBO1}		20	µA dc
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 45 V dc	I_{CBO2}		10	nA dc
Collector to emitter cutoff current	3041	Bias condition D; V_{CE} = 5 V dc	I_{CEO}		4	nA dc
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 5 V dc	I_{EBO2}		4	nA dc
Collector to emitter cutoff current	3041	Bias condition C; V_{CE} = 45 V dc	I_{CES}		10	nA dc
Forward-current transfer ratio M through H2N2484	3076	V_{CE} = 5 V dc; I_C = 1.0 µA dc.	[h_{FE1}] 5/	[22.5]		
Forward-current transfer ratio M through H2N2484	3076	V_{CE} = 5 V dc; I_C = 10 µA dc.	[h_{FE2}] 5/	[100]	500	
Forward-current transfer ratio M through H2N2484	3076	V_{CE} = 5 V dc; I_C = 100 µA dc.	[h_{FE3}] 5/	[112.5]	675	
Forward-current transfer ratio M through H2N2484	3076	V_{CE} = 5 V dc; I_C = 500 µA dc.	[h_{FE4}] 5/	[125]	800	
Forward-current transfer ratio M through H2N2484	3076	V_{CE} = 5 V dc; I_C = 1.0 mA dc.	[h_{FE5}] 5/	[125]	800	
Forward-current transfer ratio M through H2N2484	3076	V_{CE} = 5 V dc; I_C = 10 mA dc	[h_{FE6}] 5/	[112.5]	800	
Collector-emitter saturation voltage	3071	I_C = 1 mA dc; I_B = 100 µA.	$V_{CE(sat)1}$		.35	V dc
* Base emitter voltage (nonsaturated)	3066	Test condition B; V_{CE} = 5 V dc; I_C = 100 µA dc	$V_{BE(ON)}$	0.5	0.81	V dc

1/ Tests to be performed on all devices receiving radiation exposure.
2/ For sampling plan, see MIL-PRF-19500.
3/ Electrical characteristics apply to all device types unless otherwise noted.
4/ Subgroup 1 is an optional test and must be specified on the contract when required.
5/ See method 1019 of MIL-STD-750 for how to determine [h_{FE}] by first calculating the delta ($1/h_{FE}$) from the pre- and post-radiation h_{FE}. Notice the [h_{FE}] is not the same as h_{FE} and cannot be measured directly. The [h_{FE}] value can never exceed the pre-radiation minimum h_{FE} that it is based upon.

* TABLE III. Group E inspection (all quality levels) - for qualification or re-qualification only.

Inspection	MIL-STD-750		Qualification
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles.	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I, subgroup 2 and table IV herein.	
Subgroup 2			45 devices, c = 0
Intermittent life	1037	Intermittent operation life: V_{CB} = 10 V dc, 6,000 cycles. Adjust device current, or power, to achieve a minimum ΔT_J of +100°C.	
Electrical measurements		See table I, subgroup 2 and table IV herein.	
Subgroup 4			
Thermal resistance	3131	$R_{\theta JSP(IS)}$ can be calculated but shall be measured once in the same package with a similar die size to confirm calculations.	15 devices, c = 0
Thermal response curves		See MIL-PRF-19500, table E-IX, group E, subgroup 4 and 4.2.2.1 herein.	
Subgroup 5			
Not applicable			
* Subgroup 6			11 devices
Electrostatic discharge (ESD)	1020		
Subgroup 8			45 devices c = 0
Reverse stability	1033	Condition B.	

TABLE IV. Groups B, C, and E delta measurements. 1/ 2/ 3/ 4/

Step	Inspection	MIL-STD-750		Symbol	Limit	Unit
		Method	Conditions			
1	Forward-current transfer ratio	3076	V_{CE} = 5 V dc; I_C = 500 μA dc; pulsed see 4.5.1.	Δh_{FE4} 5/	±25 percent change from initial recorded reading	
2.	Collector to emitter voltage (saturated)	3071	I_C = 1.0 mA dc; I_B = 100 μA dc.	$\Delta V_{CE(sat)}$ 5/	±50 mV dc change from previously measured value.	
3.	Collector to emitter cutoff current	3041	Bias condition C; V_{CE} = 45 V dc.	ΔI_{CES} 5/	100 percent of initial value or 2 nA dc, whichever is greater.	

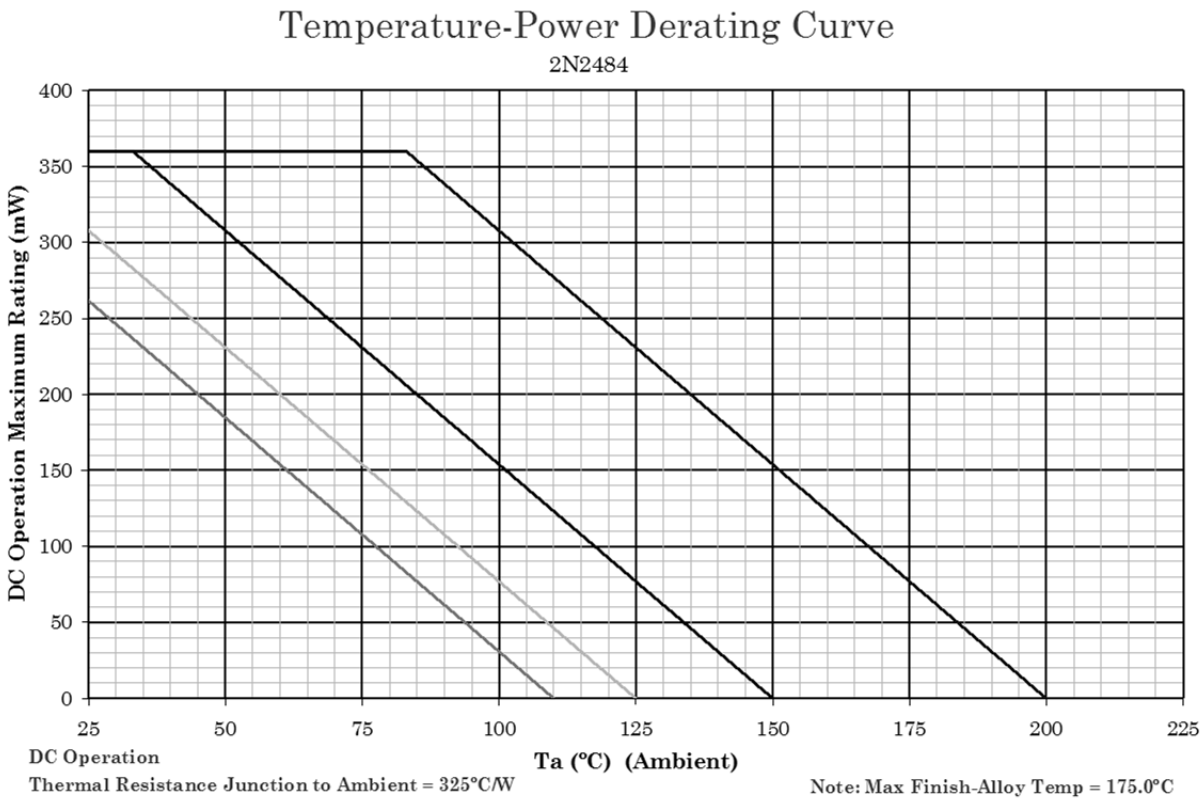
1/ The delta measurements for group B, table E-VIa (JANS) of MIL-PRF-19500 are as follows:
a. Subgroup 4, see table IV herein, step 2.
b. Subgroup 5, see table IV herein, steps 1 and 3.

2/ The delta measurements for 4.4.2.2 herein (group B, JAN, JANTX, and JANTXV) are as follows: All steps of table IV shall be performed after each step in 4.4.2.2 herein.

3/ The delta measurements for group C, table E-VII of MIL-PRF-19500 are as follows: Subgroup 6, herein, steps 1 and 3 for JANS.

4/ The delta measurements for group E, table E-IX of MIL-PRF-19500 are as follows: Subgroups 1 and 2, see table IV herein, all steps.

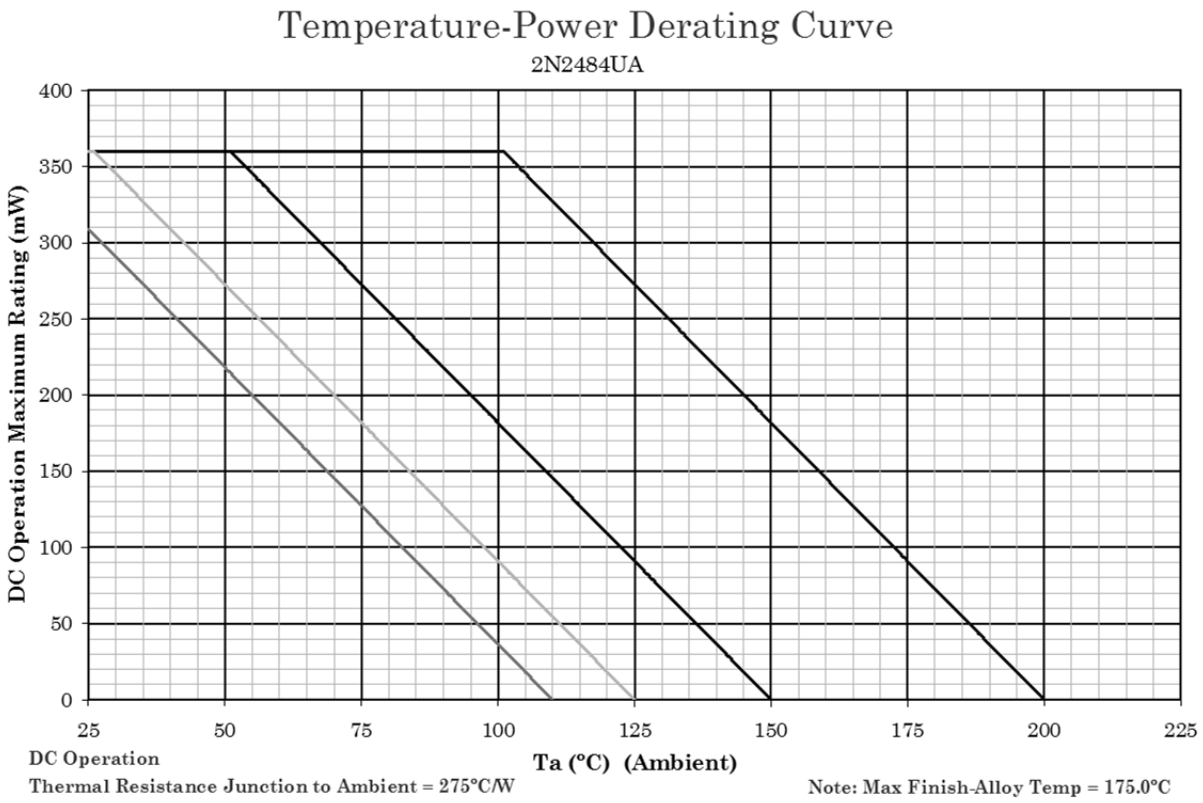
5/ Devices which exceed the table I limits for this test shall not be accepted.



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

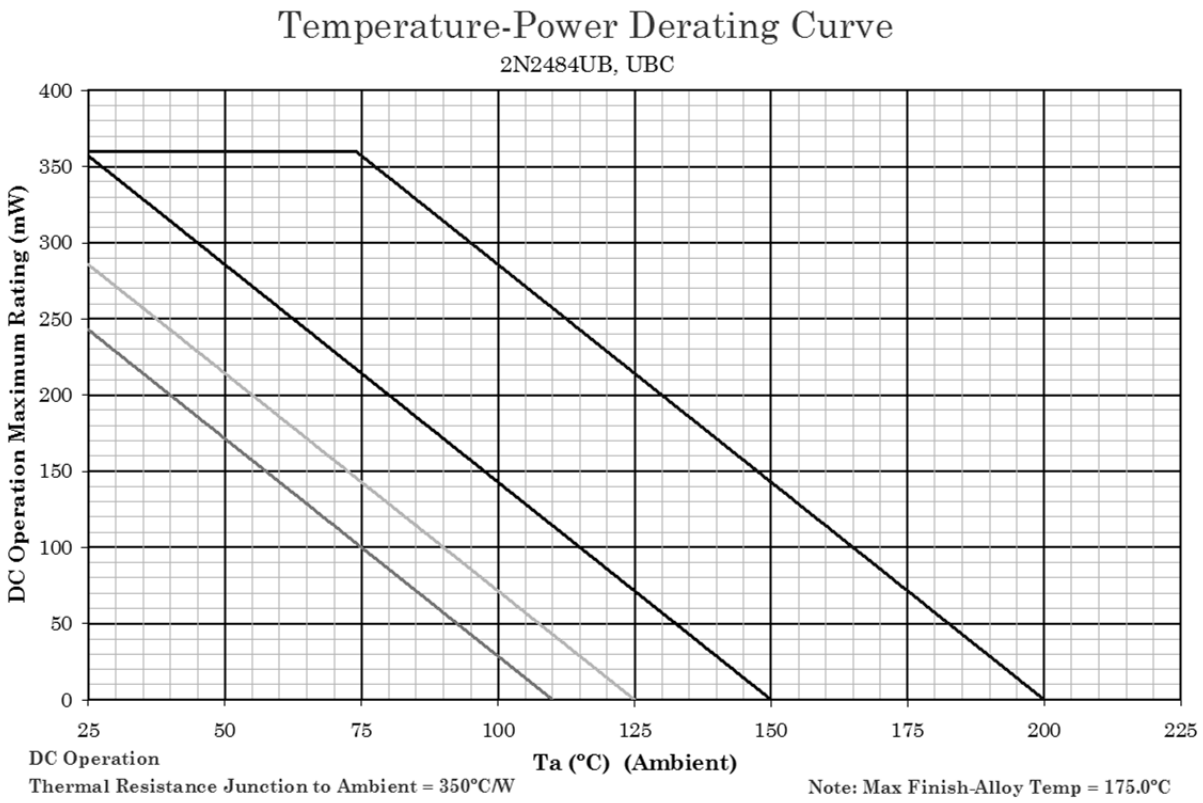
FIGURE 6. Temperature-power derating for 2N2484, (TO-18 package).



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 7. Temperature-power derating for 2N2484UA, (UA package).



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

* FIGURE 8. Temperature-power derating for 2N2484UB (UB, UBC, UBN, and UBCN package).

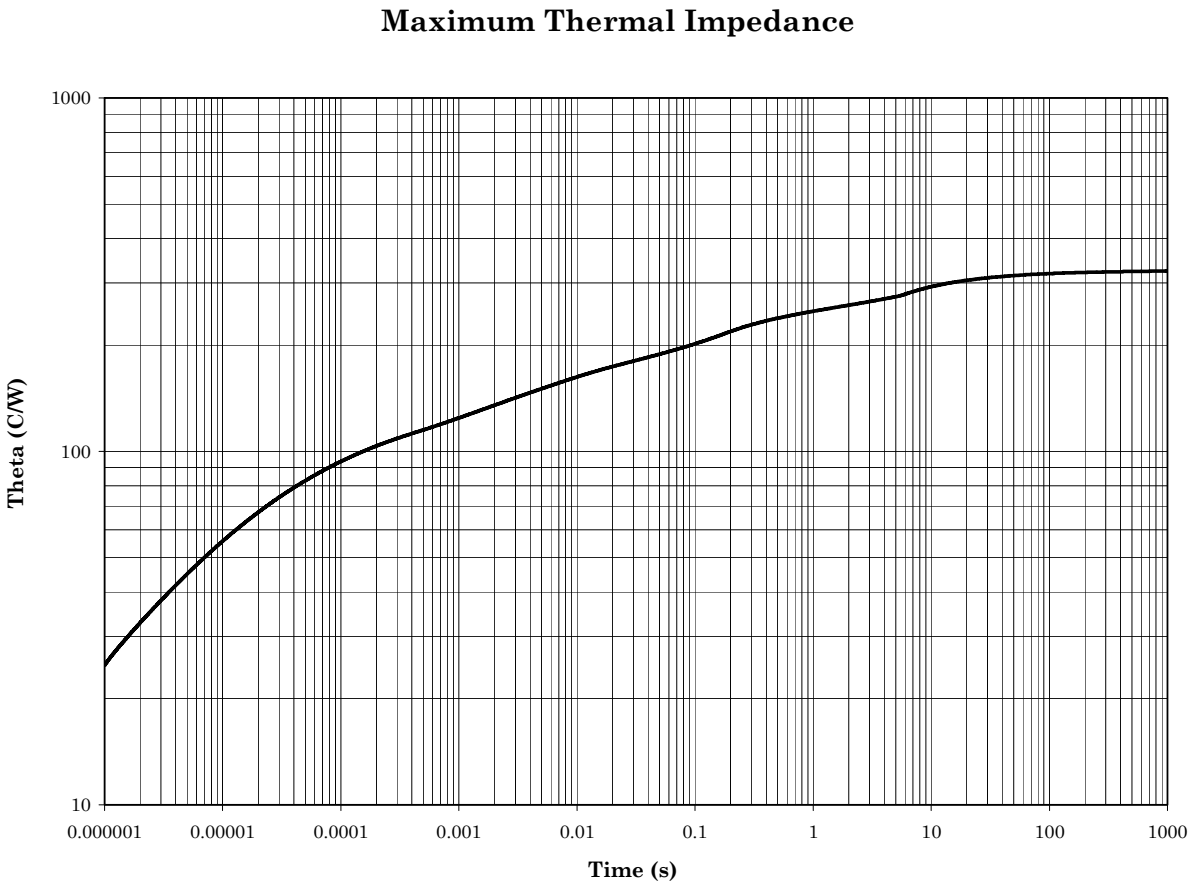


FIGURE 9. Thermal impedance graph ($R_{\theta JA}$) for 2N2484 (TO-18).

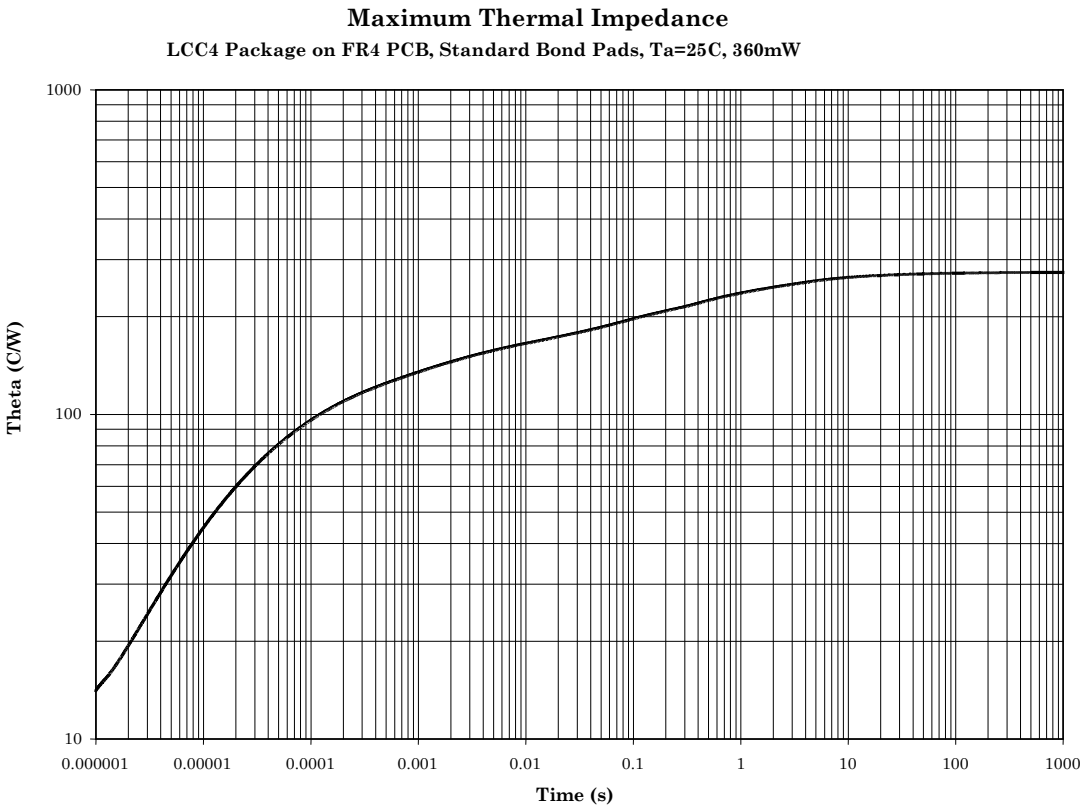


FIGURE 10. Thermal impedance graph ($R_{\theta JA}$) for 2N2484UA (UA).

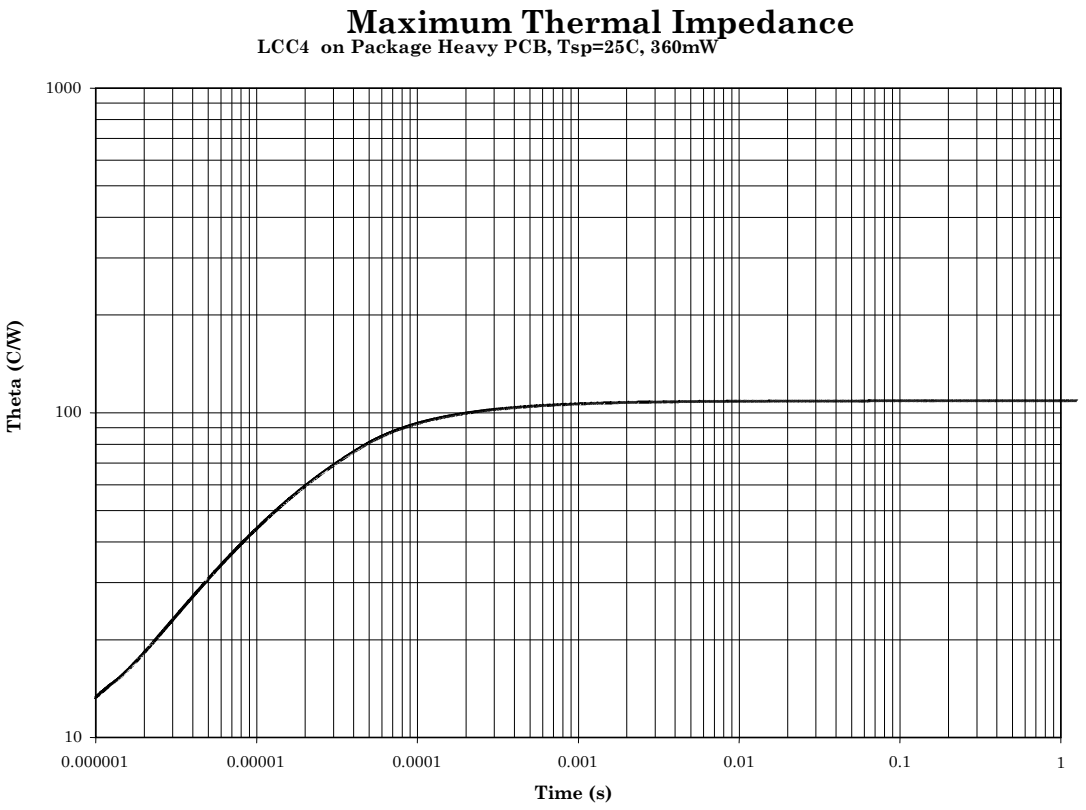
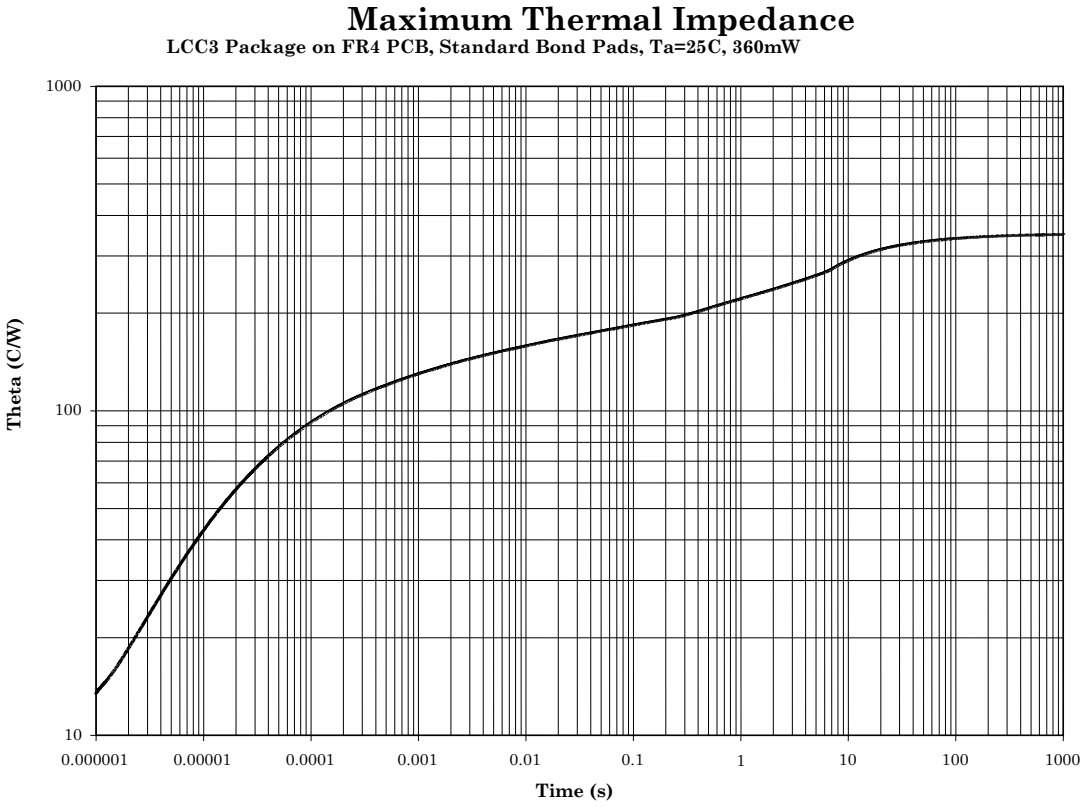
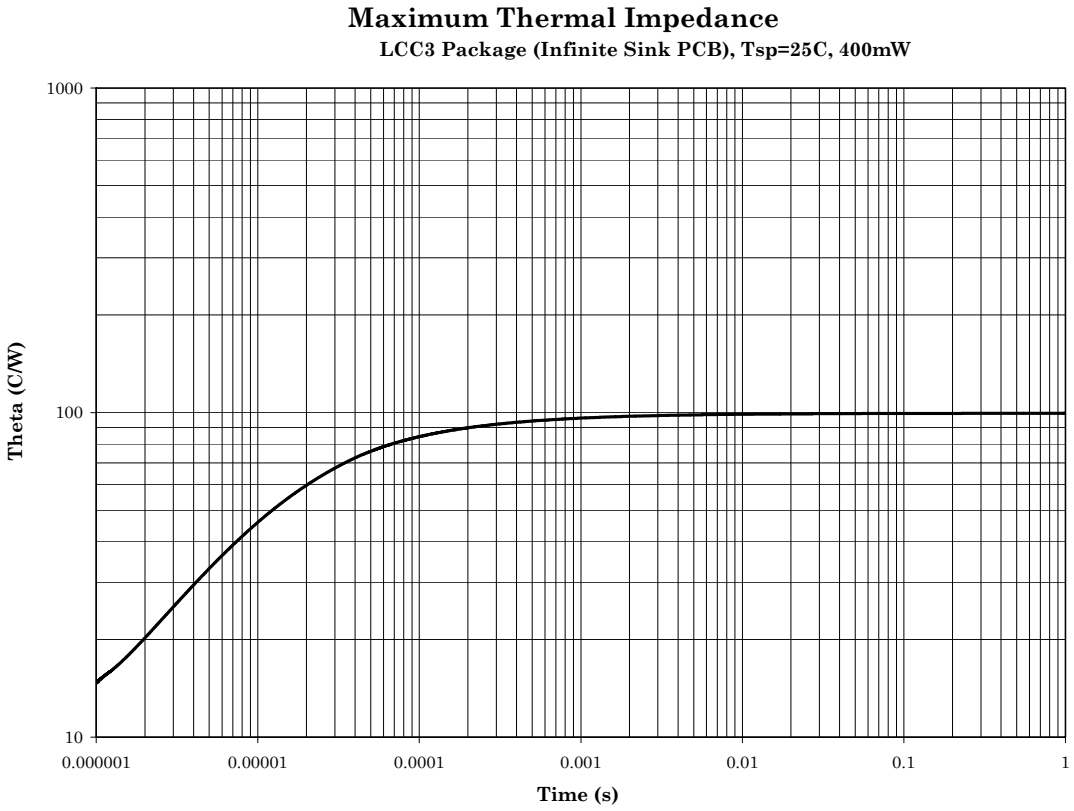


FIGURE 11. Thermal impedance graph ($R_{\theta JSP}$) for 2N2484UA (UA).



* FIGURE 12. Thermal impedance graph ($R_{\theta JA}$) for 2N2484 (UB, UBC, UBN, and UBCN).



* FIGURE 13. Thermal impedance graph ($R_{\theta JSP}$) for 2N2484 (UB, UBC, UBN, and UBCN).

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. Product assurance level and type designator.

e. For acquisition of RHA designed devices, table II, subgroup 1 testing of group D is optional. If subgroup 1 testing is desired, it must be specified in the contract.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil .

6.4 Suppliers of JANHC die. The qualified JANHC suppliers with the applicable letter version (example JANHCA2N2484) will be identified on the QML.

JANHC and JANKC ordering information		
PIN	Manufacturer	
	43611	34156
2N2484	JANHCA2N2484 JANKCA2N2484	JANHCB2N2484 JANKCB2N2484