

MULTIPLE (QUAD) NPN SILICON DUAL IN-LINE AND FLATPACK SWITCHING TRANSISTOR

Qualified per MIL-PRF-19500/559

DEVICES

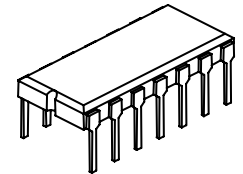
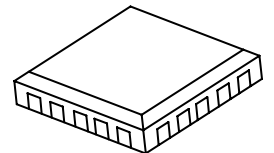
2N6989 2N6989U
2N6990

LEVELS

JAN
JANTX
JANTXV
JANS

ABSOLUTE MAXIMUM RATINGS ($T_C = +25^\circ\text{C}$ unless otherwise noted)

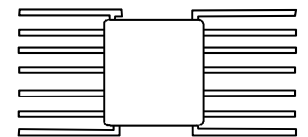
Parameters / Test Conditions	Symbol	Value	Unit
Collector-Emitter Voltage ⁽³⁾	V_{CEO}	50	Vdc
Collector-Base Voltage ⁽³⁾	V_{CBO}	75	Vdc
Emitter-Base Voltage ⁽³⁾	V_{EBO}	6.0	Vdc
Collector Current ⁽³⁾	I_C	800	mAdc
Total Power Dissipation @ $T_A = +25^\circ\text{C}$	2N6989 ⁽²⁾	1.5	W
	2N6989U ⁽²⁾	1.0	
	2N6990 ⁽²⁾	1.0	
Operating & Storage Junction Temperature Range	T_{op}, T_{stg}	-65 to +200	$^\circ\text{C}$


TO-116 – 2N6989

**20 PIN LEADLESS
 2N6989U**
Note:

- Maximum voltage between transistors shall be $\geq 500\text{Vdc}$.
- For derating, see figures 6, 7, 8 and 9. Ratings apply to total package.
- For thermal impedance curves, see figures 10, 11, 12 and 13.
- Ratings apply to each transistor in the array.

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$, unless otherwise noted)

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage $I_C = 10\text{mAdc}$	$V_{(BR)CEO}$	50		Vdc
Collector-Base Cutoff Current $V_{CB} = 60\text{Vdc}$ $V_{CB} = 75\text{Vdc}$ $V_{CB} = 60\text{Vdc}, T_A = +150^\circ\text{C}$	I_{CBO}		10	ηAdc
			10	μAdc
			10	μAdc
Emitter-Base Cutoff Current $V_{EB} = 4.0\text{Vdc}$ $V_{EB} = 6.0\text{Vdc}$	I_{EBO}		10	μAdc
			10	ηAdc


**14 PIN FLAT PACK
 2N6990**

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$, unless otherwise noted)

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
ON CHARACTERISTICS ⁽⁴⁾				
Forward-Current Transfer Ratio $I_C = 0.1\text{mA}_{dc}$, $V_{CE} = 10\text{V}_{dc}$ $I_C = 1.0\text{mA}_{dc}$, $V_{CE} = 10\text{V}_{dc}$ $I_C = 10\text{mA}_{dc}$, $V_{CE} = 10\text{V}_{dc}$ $I_C = 150\text{mA}_{dc}$, $V_{CE} = 10\text{V}_{dc}$ $I_C = 500\text{mA}_{dc}$, $V_{CE} = 10\text{V}_{dc}$ $I_C = 10\text{mA}_{dc}$, $V_{CE} = 10\text{V}_{dc}$, $T_A = -55^\circ\text{C}$	h_{FE}	50 75 100 100 30 35	325 300	
Collector-Emitter Saturation Voltage $I_C = 150\text{mA}_{dc}$, $I_B = 15\text{mA}_{dc}$ $I_C = 500\text{mA}_{dc}$, $I_B = 50\text{mA}_{dc}$	$V_{CE(sat)}$		0.3 1.0	Vdc
Base-Emitter Saturation Voltage $I_C = 150\text{mA}_{dc}$, $I_B = 15\text{mA}_{dc}$ $I_C = 500\text{mA}_{dc}$, $I_B = 50\text{mA}_{dc}$	$V_{BE(sat)}$	0.6	1.2 2.0	Vdc

DYNAMIC CHARACTERISTICS

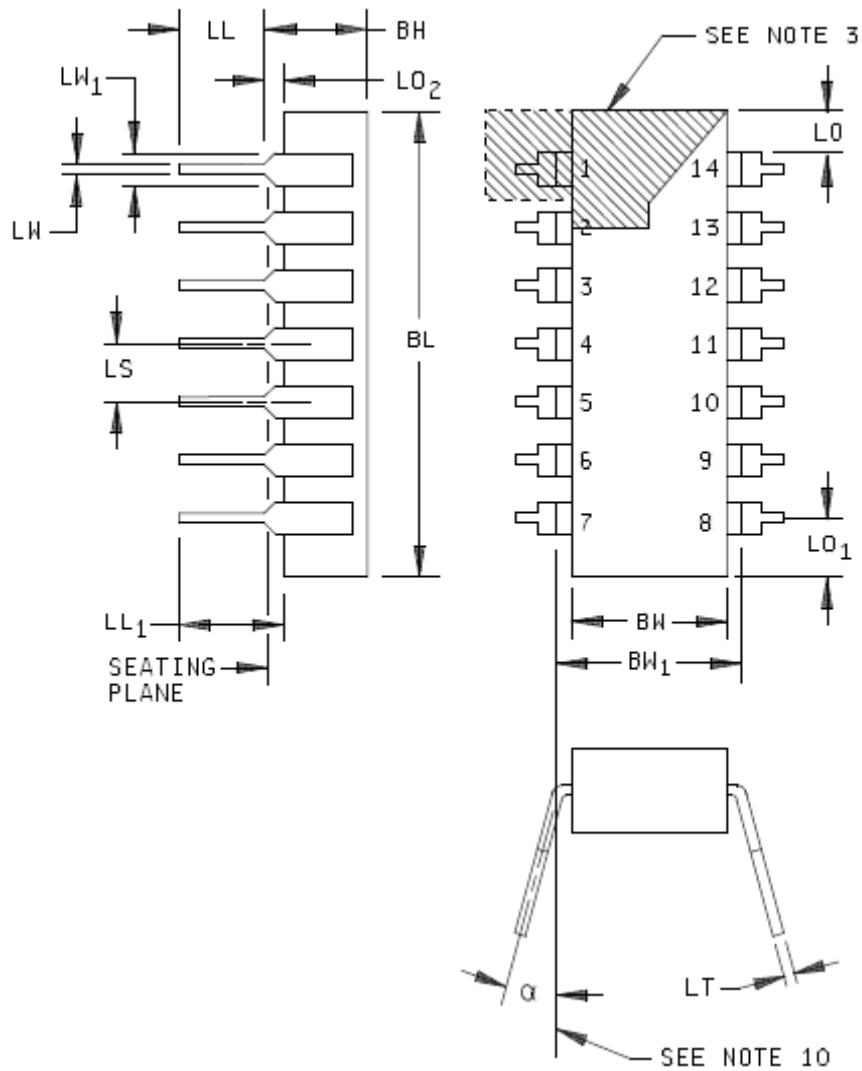
Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Magnitude of Small-Signal Short-Circuit Forward Current Transfer Ratio $I_C = 20\text{mA}_{dc}$, $V_{CE} = 10\text{V}_{dc}$, $f = 100\text{MHz}$	$ h_{fe} $	2.5	8.0	
Forward current Transfer Ratio $I_C = 1.0\text{mA}_{dc}$, $V_{CE} = 10\text{V}_{dc}$, $f = 1.0\text{kHz}$	h_{fe}	50		
Output Capacitance $V_{CB} = 10\text{V}_{dc}$, $I_E = 0$, $100\text{kHz} \leq f \leq 1.0\text{MHz}$	C_{obo}		8.0	pF
Input Capacitance $V_{EB} = 0.5\text{V}_{dc}$, $I_E = 0$, $100\text{kHz} \leq f \leq 1.0\text{MHz}$	C_{ibo}		25	pF

SWITCHING CHARACTERISTICS

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Turn-On Time SEE FIGURE 14 / MIL-PRF-19500/559	t_{on}		35	ηs
Turn-Off Time SEE FIGURE 15 / MIL-PRF-19500/559	t_{off}		300	ηs

(4) Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2.0\%$.

PACKAGE DIMENSIONS



Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
BH		.200		5.08	
LW	.014	.023	0.36	0.58	10
LW ₁	.030	.070	0.76	1.78	4, 10
LT	.008	.015	0.20	0.38	10
BL		.785		19.94	6
BW	.220	.310	5.59	7.87	6
BW ₁	.290	.320	7.37	8.13	9

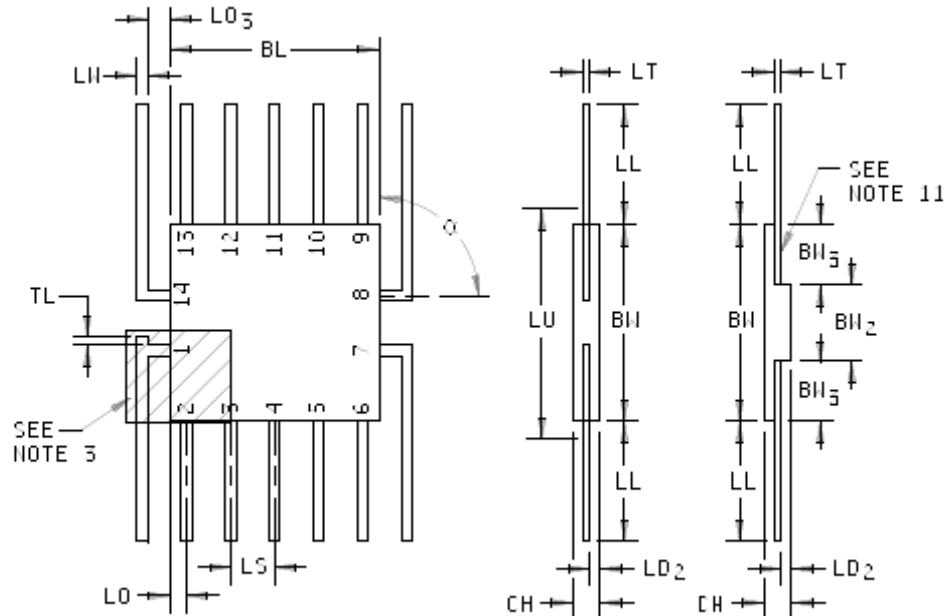
Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
LS	.100 BSC		2.54 BSC		7, 11
LL	.125	.200	3.18	5.08	
LL ₁	.150		3.81		
LO	.005		0.13		8
LO ₁		.098		2.49	8
LO ₂	.015	.060	0.38	1.52	5
α	0°	15°	0°	15°	

NOTES:

- 1 Dimension are in inches.
- 2 Millimeters are given for general information only.
- 3 Index area: A notch or pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
- 4 The minimum limit for dimension LW₁ may be .023 inch (0.58 mm) for leads number 1, 7, 8 and 14 only.
- 5 Dimension LO₂ shall be measured from the seating plane to the base plane.
- 6 This dimension allows for off-center lid, meniscus, and glass overrun.
- 7 The basic pin spacing is .100 inch (2.54 mm) between centerlines. Each pin centerline shall be located within ±.010 inch (0.25 mm) of its exact longitudinal position relative to pins 1 and 14.
- 8 Applies to all four corners (leads number 1, 7, 8 and 14).
- 9 Lead center when α is 0 degrees. BW₁ shall be measured at the centerline of the leads.
- 10 All leads.
- 11 Twelve spaces.
- 12 No organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
- 13 In accordance with ASME Y14.5M, diameters are equivalent to ϕ x symbology.

FIGURE 1. Physical Dimension and Configuration for type 2N6989

PACKAGE DIMENSIONS



Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CH	.030	.115	0.76	2.92	
LW	.010	.019	0.25	0.48	7
TL	.008	.015	0.20	0.38	12
BL		.280		7.11	5
BW	.240	.260	6.10	6.60	
LU		.290		7.37	5
BW ₂	.125		3.18		

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
BW ₃	.030		0.76		
LS	.050 BSC		1.27 BSC		6, 8
LT	.003	.006	0.076	0.152	7
LL	.250	.370	6.35	9.40	
LD ₂	.005	.040	0.13	1.02	4
LO	.005		0.13		9, 10
LO ₃	.004				13
α	30°	90°	30°	90°	14

NOTES:

- 1 Dimension are in inches.
- 2 Millimeters are given for general information only.
- 3 Index area: A notch or pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternatively, a tab (dine TL) may be used to identify pin one.
- 4 Dimension LD_2 shall be measured at the point of exit of the lead from the body.
- 5 This dimension allows for off-center lid, meniscus, and glass overrun.
- 6 The basic pin spacing is .050 inch (1.27 mm) between centerlines. Each pin centerline shall be located within $\pm .005$ inch (0.13 mm) of its exact longitudinal position relative to pins 1 and 14.
- 7 All leads: Increase maximum limit by .003 inch (0.08 mm) measured at the center of the flat when the lead finish is solder.
- 8 Twelve spaces.
- 9 Applies to all four corners (leads number 2, 6, 9 and 13).
- 10 Dimension LO may be .000 inch (0.00 mm) if leads number 2, 6, 9, and 13) bend toward the cavity of the package within one lead width from the point of entry of the lead into the body or if the leads are brazed to the metalized ceramic body.
- 11 No organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
- 12 Optional, see note 1. If a pin one identification mark is used in addition to this tab, the minimum limit of dimension TL does not apply.
- 13 Applies to leads number 1, 7, 8, and 14.
- 14 Lead configuration is optional within dimension BW except dimensions LW and LT apply.
- 15 In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
- 16 Pins 1, 7, 8, and 14 are collectors.
- 17 Pin 2, 6, 9, and 13 are bases.
- 18 Pin 3, 5, 10, and 12 are emitters.
- 19 Pins 4 and 11 are no contacts.

FIGURE 2. Physical dimensions for type 2N6990

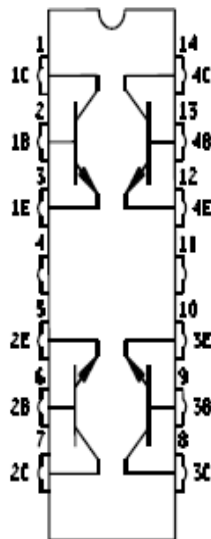


FIGURE 3. Schematic and terminal connections for types 2N6989 & 2N6990