6 Lake Street, Lawrence, MA 01841
1-800-446-1158 / (978) 620-2600 / Fax: (978) 689-0803
Website: http: //www.microsemi.com

TECHNICAL DATA SHEET

RADIATION HARDENED
NPN SILICON SWITCHING TRANSISTOR
Qualified per MIL-PRF-19500/255

DEVICES

2N2221A	**2N2222A**
2N2221AL	**2N2222AL**
2N2221AUA	**2N2222AUA**
2N2221AUB	**2N2222AUB**
2N2221AUBC	**2N2222AUBC**

LEVELS

JANSM – 3K Rads (Si)
JANSD – 10K Rads (Si)
JANSP – 30K Rads (Si)
JANSL – 50K Rads (Si)
JANSR – 100K Rads (Si)
JANSF – 300K Rads (Si)
JANSG – 500K Rads (Si)
JANSH – 1MEG Rads (Si)

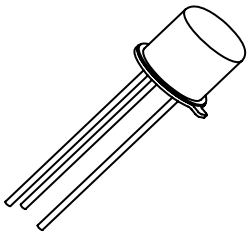
ABSOLUTE MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

Parameters / Test Conditions	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector-Base Voltage	V_{CBO}	75	Vdc
Emitter-Base Voltage	V_{EBO}	6.0	Vdc
Collector Current	I_C	800	mAdc
Total Power Dissipation @ T_A = +25°C 2N2221A, L / 2N2222A, L 2N2221AUA / 2N2222AUA 2N2221AUB, UBC / 2N2222AUB, UBC	P_T	 0.5 0.65 0.50	W
Operating & Storage Junction Temperature Range	T_{op}, T_{stg}	-65 to +200	°C

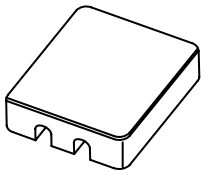
THERMAL CHARACTERISTICS

Parameters / Test Conditions	Symbol	Max.	Unit
Thermal Resistance, Junction-to-Ambient 2N2221A, L / 2N2222A, L 2N2221AUA / 2N2222AUA 2N2221AUB, UBC / 2N2222AUB, UBC	$R_{\theta JA}$	 325 210 325	°C/W

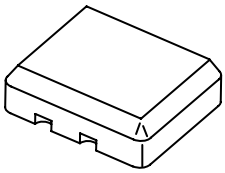
1. Derate linearly 3.08 mW/°C above T_A > +37.5°C
2. Derate linearly 4.76 mW/°C above T_A > +63.5°C



TO-18 (TO-206AA)
2N2221A, 2N2222A



4 PIN
2N2221AUA, 2N2222AUA



3 PIN
2N2221AUB, 2N2222AUB
2N2221AUBC, 2N2222AUBC
(UBC = Ceramic Lid Version)

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ELECTRICAL CHARACTERISTICS *(T_A = +25°C, unless otherwise noted)*

Parameters / Test Conditions		Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage I_C = 10mAdc		$V_{(BR)CEO}$	50		Vdc
Collector-Base Cutoff Current V_{CB} = 75Vdc V_{CB} = 60Vdc		I_{CBO}		10 10	µAdc ηAdc
Emitter-Base Cutoff Current V_{EB} = 6.0Vdc V_{EB} = 4.0Vdc		I_{EBO}		10 10	µAdc ηAdc
Collector-Emitter Cutoff Current V_{CE} = 50Vdc		I_{CES}		50	ηAdc
ON CHARACTERISTICS [3]					
Forward-Current Transfer Ratio					
I_C = 0.1mAdc, V_{CE} = 10Vdc	2N2221A, L, UA, UB, UBC 2N2222A, L, UA, UB, UBC		30 50		
I_C = 1.0mAdc, V_{CE} = 10Vdc	2N2221A, L, UA, UB, UBC 2N2222A, L, UA, UB, UBC		35 75	150 325	
I_C = 10mAdc, V_{CE} = 10Vdc	2N2221A, L, UA, UB, UBC 2N2222A, L, UA, UB, UBC	h_{FE}	40 100		
I_C = 150mAdc, V_{CE} = 10Vdc	2N2221A, L, UA, UB, UBC 2N2222A, L, UA, UB, UBC		40 100	120 300	
I_C = 500mAdc, V_{CE} = 10Vdc	2N2221A, L, UA, UB, UBC 2N2222A, L, UA, UB, UBC		20 30		
Collector-Emitter Saturation Voltage I_C = 150mAdc, I_B = 15mAdc I_C = 500mAdc, I_B = 50mAdc		$V_{CE(sat)}$		0.3 1.0	Vdc
Base-Emitter Voltage I_C = 150mAdc, I_B = 15mAdc I_C = 500mAdc, I_B = 50mAdc		$V_{BE(sat)}$	0.6	1.2 2.0	Vdc

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DYNAMIC CHARACTERISTICS

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Small-Signal Short-Circuit Forward Current Transfer Ratio I_C = 1.0mAdc, V_{CE} = 10Vdc, f = 1.0kHz 2N2221A, L, UA, UB, UBC 2N2222A, L, UA, UB, UBC	h_{fe}	30 50		
Magnitude of Small–Signal Short-Circuit Forward Current Transfer Ratio I_C = 20mAdc, V_{CE} = 20Vdc, f = 100MHz	$\|h_{fe}\|$	2.5		
Output Capacitance V_{CB} = 10Vdc, I_E = 0, 100kHz ≤ f ≤ 1.0MHz	C_{obo}		8.0	pF
Input Capacitance V_{EB} = 0.5Vdc, I_C = 0, 100kHz ≤ f ≤ 1.0MHz	C_{ibo}		25	pF

SWITCHING CHARACTERISTICS

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Turn-On Time See figure 8 of MIL-PRF-19500/255	t_{on}		35	ηs
Turn-Off Time See Figure 9 of MIL-PRF-19500/255	t_{off}		300	ηs

(3) Pulse Test: Pulse Width = 300μs, Duty Cycle ≤ 2.0%.

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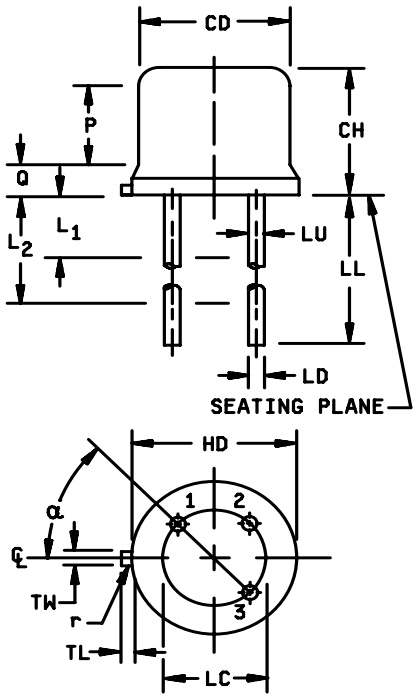
PACKAGE DIMENSIONS



NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Beyond r (radius) maximum, TL shall be held for a minimum length of .011 inch (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC.
7. Dimension LU applies between L_1 and L_2. Dimension LD applies between L_2 and LL minimum. Diameter is uncontrolled in L_1 and beyond LL minimum.
8. All three leads.
9. The collector shall be internally connected to the case.
10. Dimension r (radius) applies to both inside corners of tab.
11. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
12. Lead 1 = emitter, lead 2 = base, lead 3 = collector.
13. For L suffix devices, dimension LL = 1.5 inches (38.10 mm) min. and 1.75 inches (44.45 mm) max.

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.178	.195	4.52	4.95	
CH	.170	.210	4.32	5.33	
HD	.209	.230	5.31	5.84	
LC	.100 TP		2.54 TP		6
LD	.016	.021	0.41	0.53	7,8
LL	.500	.750	12.70	19.05	7,8,13
LU	.016	.019	0.41	0.48	7,8
L_1		.050		1.27	7,8
L_2	.250		6.35		7,8
P	.100		2.54		
Q		.030		0.76	5
TL	.028	.048	0.71	1.22	3,4
TW	.036	.046	0.91	1.17	3
r		.010		0.25	10
α	45° TP		45° TP		6
1, 2, 9, 11, 12, 13					

FIGURE 1. Physical dimensions (similar to TO-18).

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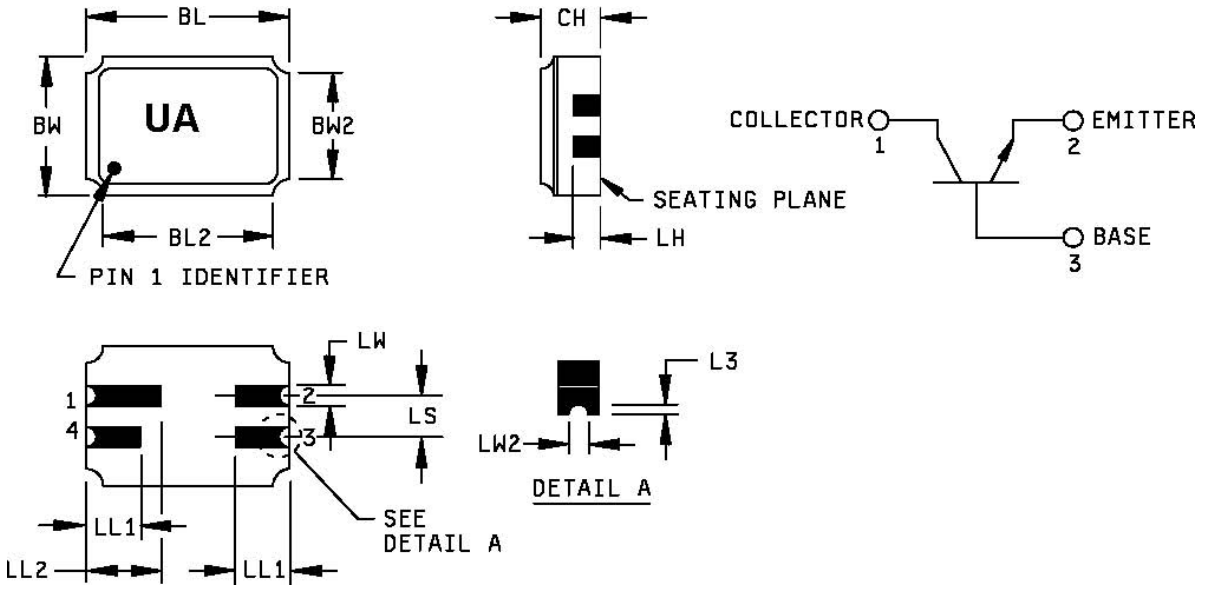

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Dimension CH controls the overall package thickness. When a window lid is used, dimension CH must increase by a minimum of .010 inch (0.254 mm) and a maximum of .040 inch (1.020 mm).
4. The corner shape (square, notch, radius) may vary at the manufacturer's option, from that shown on the drawing.
5. Dimensions LW2 minimum and L3 minimum and the appropriate castellation length define an unobstructed three-dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on the bottom two layers, optional on the top ceramic layer.) Dimension LW2 maximum and L3 maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.
6. The co-planarity deviation of all terminal contact points, as defined by the device seating plane, shall not exceed .006 inch (0.15mm) for solder dipped leadless chip carriers.
7. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.215	.225	5.46	5.71	
BL2		.225		5.71	
BW	.145	.155	3.68	3.93	
BW2		.155		3.93	
CH	.061	.075	1.55	1.90	3
L3	.003	.007	0.08	0.18	5
LH	.029	.042	0.74	1.07	
LL1	.032	.048	0.81	1.22	
LL2	.072	.088	1.83	2.23	
LS	.045	.055	1.14	1.39	
LW	.022	.028	0.56	0.71	
LW2	.006	.022	0.15	0.56	5

Pin no.	1	2	3	4
Transistor	Collector	Emitter	Base	N/C

FIGURE 2. Physical dimensions, surface mount (UA version).

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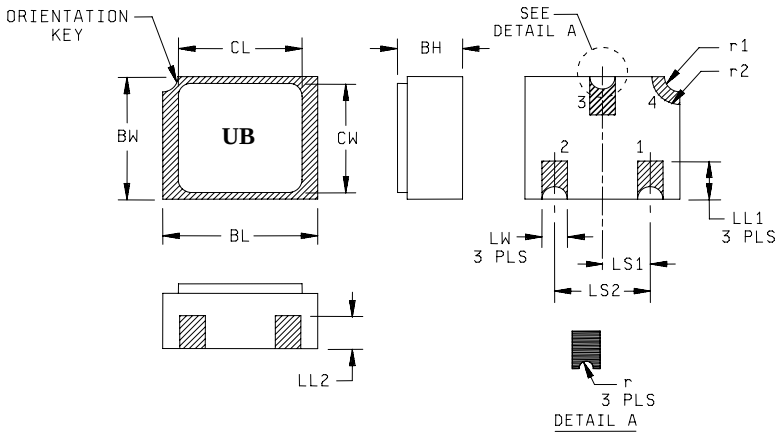

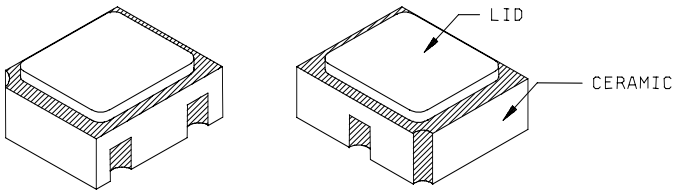

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BH	.046	.056	1.17	1.42	
BL	.115	.128	2.92	3.25	
BW	.085	.108	2.16	2.74	
CL		.128		3.25	
CW		.108		2.74	
LL1	.022	.038	0.56	0.96	
LL2	.017	.035	0.43	0.89	

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
LS_1	.036	.040	0.91	1.02	
LS_2	.071	.079	1.81	2.01	
LW	.016	.024	0.41	0.61	
r		.008		.203	
r_1		.012		.305	
r_2		.022		.559	

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Hatched areas on package denote metalized areas.
4. Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Pad 4 = Shielding connected to the lid.
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 3. Physical dimensions, surface mount (UB version)