The documentation and process conversion measures necessary to comply with this document shall be completed by 2 January 2014.

INCH-POUND

MIL-PRF-19500/368M
2 October 2013
SUPERSEDING
MIL-PRF-19500/368L
20 November 2010

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, TRANSISTOR, NPN, SILICON, LOW-POWER
TYPES: 2N3439, 2N3439L, 2N3439UA, 2N3439U4, 2N3440, 2N3440L, 2N3440UA, AND 2N3440U4, JAN, JANTX, JANTXV, JANS, JANHCB, JANKCB, JANHCC, JANKCC JANSM, JANSD, JANSP, JANSL, JANSR, JANSF, JANSG, JANSH, JANKCBM, JANKCBD, JANKCBP, JANKCBL, JANKCBR, JANKCBF, JANKCBG, AND JANKCBH

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for NPN, silicon, low-power, high voltage transistors. Four levels of product assurance are provided for each encapsulated device types as specified in MIL-PRF-19500, and two levels of product assurance for each unencapsulated device type die. RHA level designators “M”, “D”, “P“, “L”, “R”, “F”, “G”, and “H” are appended to the device prefix to identify devices, which have passed RHA requirements.

1.2 Physical dimensions. See figure 1 (similar to TO-5 and TO-39), figure 2 (JANHCB and JANKCB (B versions)), figure 3 (2N3439UA and 2N3440UA surface mount versions), figure 4 (2N3439U4 and 2N3440U4 versions), and figure 5 (JANHCC and JANKCC (C versions)).

1.3 Maximum ratings. Unless otherwise specified, T_A = +25°C.

Types	P_T (1) T_A = +25°C	P_T (2) T_C = +25°C	P_T (2) T_{SP} = +25°C	$R_{\theta JA}$ (3)	$R_{\theta JC}$ (3)	$R_{\theta JSP}$ (3)	V_{CBO}	V_{EBO}	V_{CEO}	I_C	T_{STG} and T_J
	W	W	W	°C/W	°C/W	°C/W	V dc	V dc	V dc	A dc	°C
2N3439	0.8	5.0	N/A	175	30	N/A	450	7	350	1.0	-65 to +200
2N3439L	0.8	5.0	N/A	175	30	N/A	450	7	350	1.0	
2N3439UA	0.8	N/A	2.0	175	N/A	70	450	7	350	1.0	
2N3439U4	0.8	5	N/A	175	8	N/A	450	7	350	1.0	
2N3440	0.8	5.0	N/A	175	30	N/A	300	7	250	1.0	
2N3440L	0.8	5.0	N/A	175	30	N/A	300	7	250	1.0	
2N3440UA	0.8	N/A	2.0	175	N/A	70	300	7	250	1.0	
2N3440U4	0.8	5	N/A	175	8	N/A	300	7	250	1.0	

(1) For derating, see figure 6.
(2) For derating, see figures 7, 8, and 9.
(3) For thermal impedance curves see figures 10, 11, 12, and 13.

* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil .

1.4 Primary electrical characteristics. Unless otherwise specified T_A = +25°C.

	h_{FE2} (1) V_{CE} = 10 V dc I_C = 2 mA dc	h_{FE1} (1) V_{CE} = 10 V dc I_C = 20 mA dc	$\lvert h_{fe} \rvert$ V_{CE} = 10 V dc I_C = 10 mA dc f = 5 MHz	C_{obo} V_{CB} = 10 V dc I_E = 0 100 kHz ≤ f ≤ 1 MHz	$V_{BE(sat)}$ (1) I_C = 50 mA dc I_B = 4 mA dc	$V_{CE(sat)}$ I_C = 50 mA dc I_B = 4 mA dc
				pF	V dc	V dc
Min	30	40	3			
Max		160	15	10	1.3	0.5

(1) Pulsed, (see 4.5.1).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

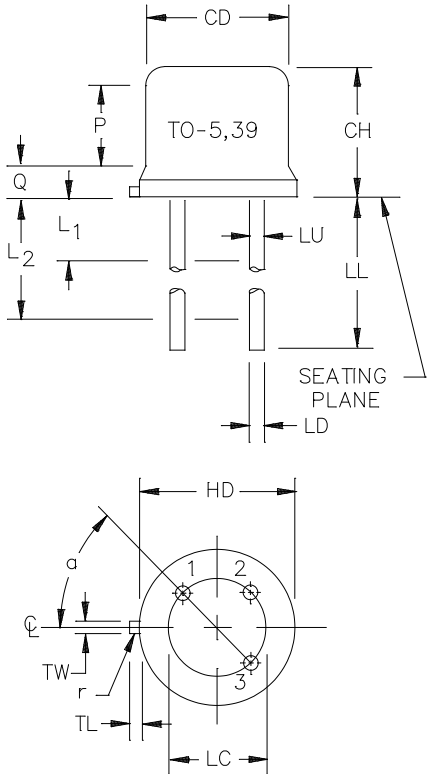
DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at http://quicksearch.dla.mil or https://assist.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

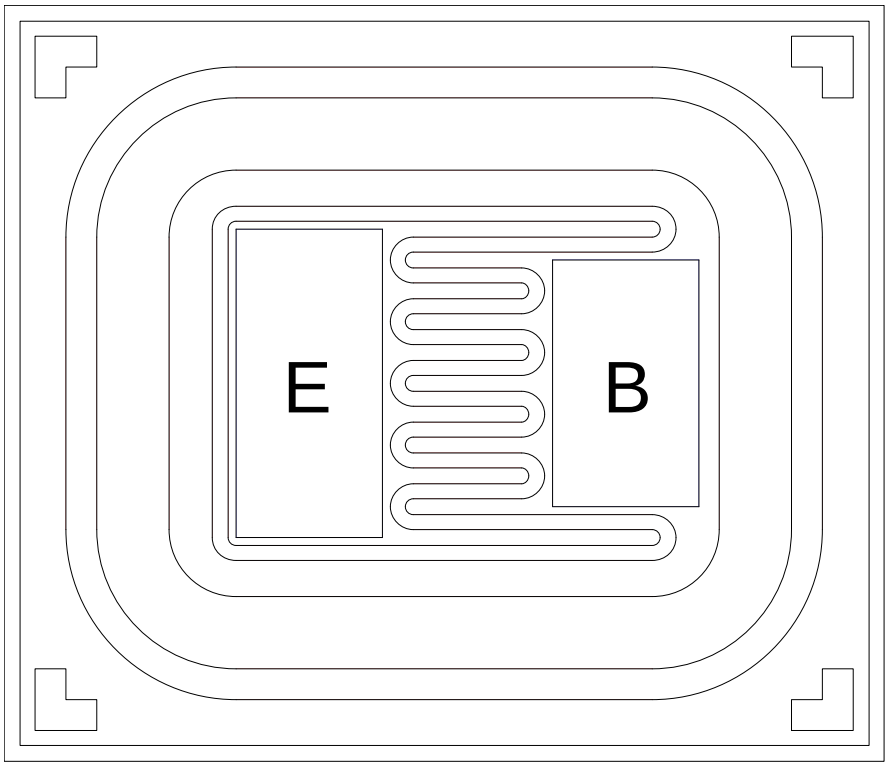
Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	6
CH	.240	.260	6.10	6.60	
HD	.335	.370	8.51	9.40	
LC	.200 TP		5.08 TP		7
LD	.016	.019	0.41	0.48	8,9
LL	See note 14				
LU	.016	.019	0.41	0.48	8,9
L_1		.050		1.27	8,9
L_2	.250		6.35		8,9
P	.100		2.54		7
Q		.030		0.76	5
TL	.029	.045	0.74	1.14	3,4
TW	.028	.034	0.71	0.86	3
r		.010		0.25	10
α	45° TP		45° TP		7



NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Beyond r (radius) maximum, TW shall be held for a minimum length of .011 (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. CD shall not vary more than .010 inch (0.25 mm) in zone P. This zone is controlled for automatic handling.
7. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC. The device may be measured by direct methods or by gauging procedure.
8. Dimension LU applies between L_1 and L_2. Dimension LD applies between L_2 and LL minimum. Diameter is uncontrolled in and beyond LL minimum.
9. All three leads.
10. The collector shall be internally connected to the case.
11. Dimension r (radius) applies to both inside corners of tab.
12. In accordance with ASME Y14.5M, diameters are equivalent to Φx symbology.
13. Lead 1 = emitter, lead 2 = base, lead 3 = collector.
14. For transistor types 2N3439L and 2N3440L (T0-5), dimension LL = 1.5 inches (38.10 mm) min. and 1.75 inches (44.45 mm) max. For transistor types 2N3439 and 2N3440 (T0-39), dimension LL = .5 inch (12.70 mm) min. and .750 inch (19.05 mm) max.

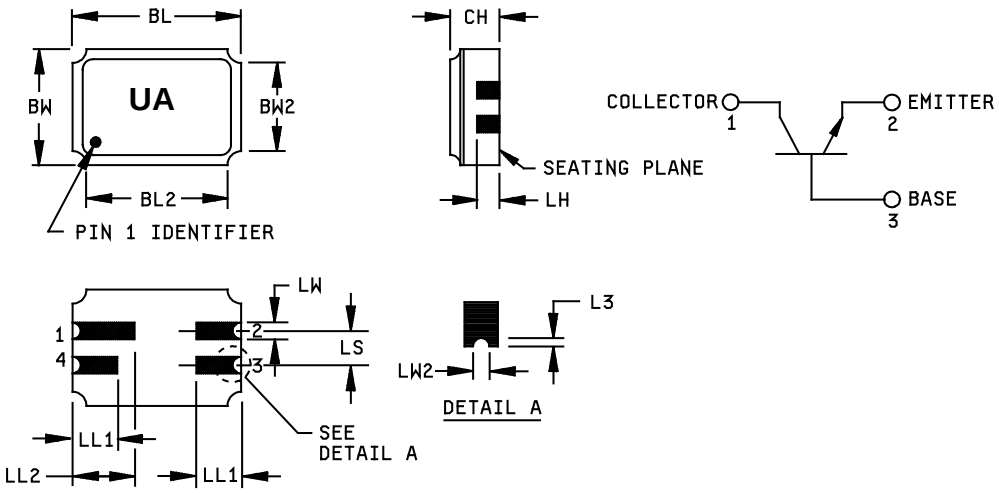
FIGURE 1. Physical dimensions (similar to TO-5 and TO-39).



1.	Chip size.....	.049 x .057 inch ±.002 inch (1.24 mm x 1.45 mm ±0.05 mm).
2.	Chip thickness.....	.010 ± .0015 inch nominal (0.254 mm ±0.038 mm).
3.	Top metal.....	Aluminum 15,000Å minimum, 18,000Å nominal
4.	Back metal.....	A. Al/Ti/Ni/Ag 12kÅ/3kÅ/7kÅ/7kÅminimum,15kÅ/ 5kÅ/10kÅ/10kÅ nominal. B. Gold 3,500Å minimum, 5,000Å nominal.
5.	Backside.....	Collector.
6.	Bonding pad.....	B = .005 x .008 inch (0.127 mm x 0.203 mm). E = .010 x .007 inch (0.254 mm x 0.178 mm).

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 2. Physical dimensions JANHCB and JANKCB (die) B versions.

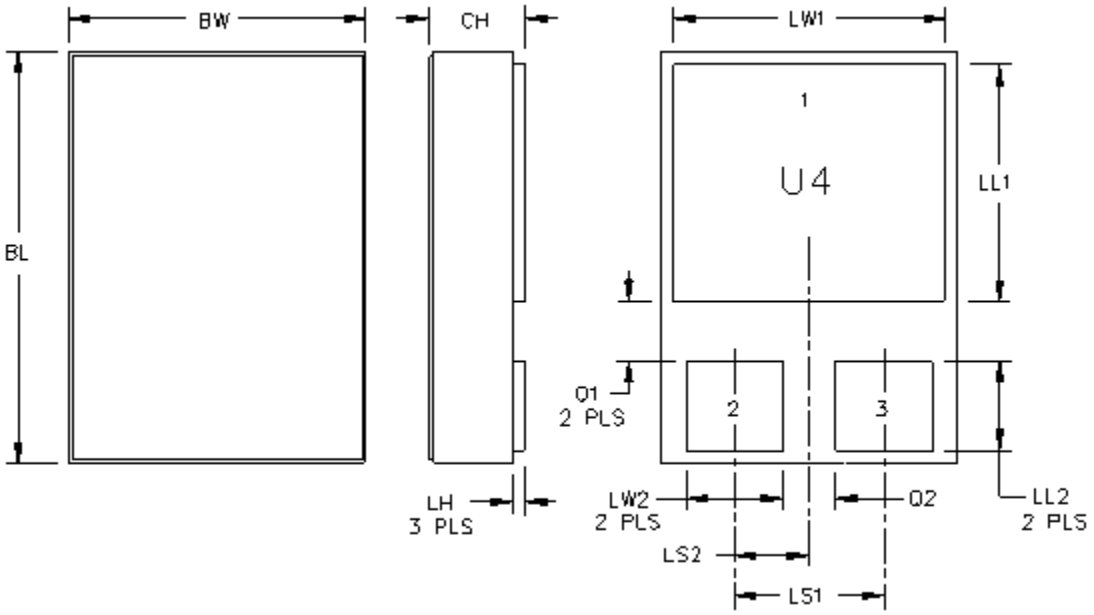


Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.215	.225	5.46	5.71	
BL2		.225		5.71	
BW	.145	.155	3.68	3.93	
BW2		.155		3.93	
CH	.061	.075	1.55	1.90	3
L3	.003		0.08		5
LH	.029	.042	0.74	1.07	
LL1	.032	.048	0.81	1.22	
LL2	.072	.088	1.83	2.23	
LS	.045	.055	1.14	1.39	
LW	.022	.028	0.56	0.71	
LW2	.006	.022	0.15	0.56	5

Pin no.	1	2	3	4
Transistor	Collector	Emitter	Base	N/C

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Dimension "CH" controls the overall package thickness. When a window lid is used, dimension "CH" must increase by a minimum of .010 inch (0.254 mm) and a maximum of .040 inch (1.020 mm).
4. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
* 5. Dimensions " LW2" minimum and "L3" minimum and the appropriate castellation length define an unobstructed three-dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on bottom two layers, optional on top ceramic layer.) Dimension " LW2" maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.
6. The coplanarity deviation of all terminal contact points, as defined by the device seating plane, shall not exceed .006 inch (0.15mm) for solder dipped leadless chip carriers.
7. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

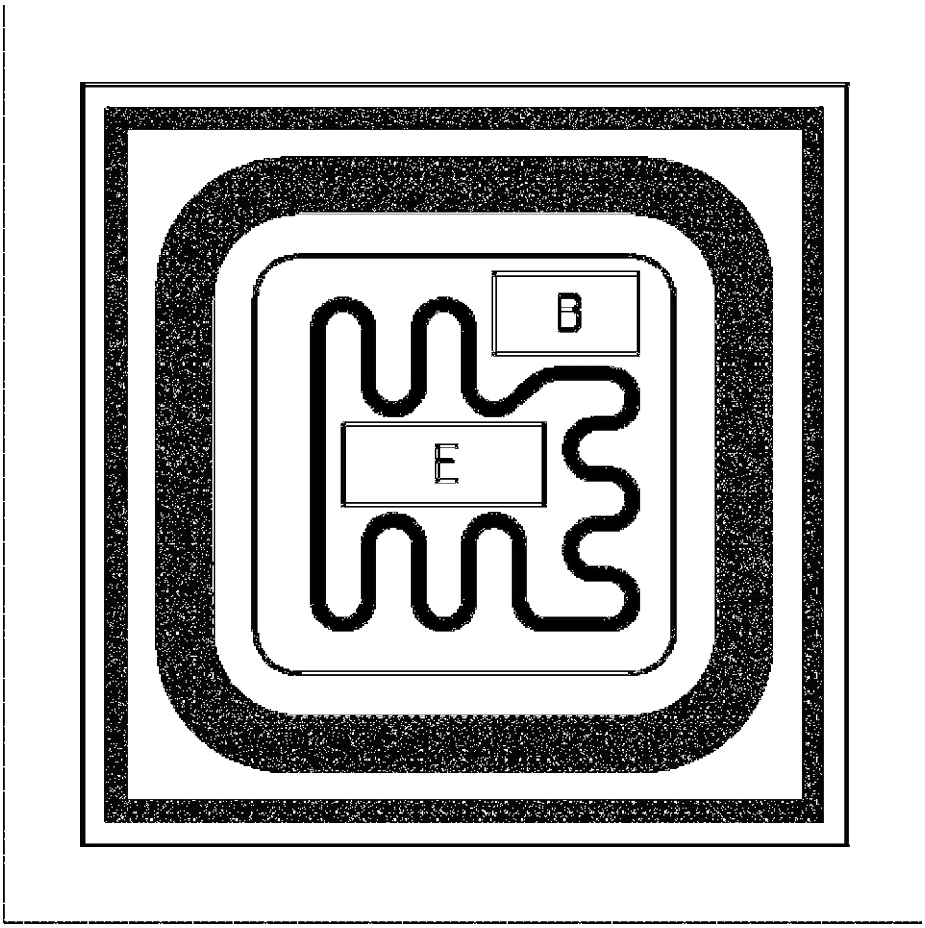
* FIGURE 3. Physical dimensions, surface mount (2N3439UA, 2N3440UA) version.



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.215	.225	5.46	5.72
BW	.145	.155	3.68	3.94
CH	.049	.075	1.24	1.91
LH		.020		0.51
LW1	.135	.145	3.43	3.68
LW2	.047	.057	1.19	1.45
LL1	.085	.125	2.16	3.17
LL2	.045	.075	1.14	1.90
LS1	.070	.095	1.78	2.41
LS2	.035	.048	0.89	1.21
Q1	.030	.070	0.76	1.78
Q2	.020	.035	0.51	0.89
1	Collector			
2	Base			
3	Emitter			

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Terminal 1 is collector.
4. Terminal 2 is base.
5. Terminal 3 is emitter.
6. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 4. Physical dimensions, surface mount (2N3439U4, 2N3440U4) version (U4).



Chip size ..... 0.045 x 0.045 inch ±0.002 inch (1.143 x 1.143 mm ±0.051mm)
Chip thickness..... 0.008 ±0.0005 inch (0.203 ±0.0127mm)
Top metal ..... Aluminum 17,500 Å minimum; 20,000 Å nominal
Back metal ..... Gold 5,000 Å minimum; 6,500 Å nominal
Backside ..... Collector Bonding pads..... B= 0.008 x 0.005 inch (0.203 x 0.127mm)
E= 0.011 x 0.005 inch (0.279 x 0.127mm)

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 5. Physical dimensions JANHCC and JANKCC (die) C versions.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

$R_{\theta JA}$	Thermal resistance junction to ambient.
$R_{\theta JC}$	Thermal resistance junction to case.
$R_{\theta JSP}$	Thermal resistance junction to solder pads.
UA	Surface mount case outlines (see figure 3).
TRB	Technical review board.
T_{SP}	Temperature of solder pads.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500 and on figure 1 (similar to TO- 5 and TO-39), figure 2 (JANHCB and JANKCB (B versions)), figure 3 (2N3439UA and 2N3440UA surface mount, figure 4 (2N3439U4 and 2N3440U4)), and figure 5 (JANHCC and JANKCC (C versions)).

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Radiation hardness assurance (RHA). Radiation hardness assurance requirements, PIN designators, and test levels shall be as defined in MIL-PRF-19500.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.7 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table I herein.

3.8 Marking. Marking shall be in accordance with MIL-PRF-19500. At the option of the manufacturer, marking may be omitted from the body, but shall be retained on the initial container. The radiation hardened designator M, D, P, L, R, F, G, or H shall immediately precede (or replace) the device “2N” identifier (depending upon degree of abbreviation required).

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and tables I, II, and III).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and table III herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.3 Screening (JANS, JANTXV, and JANTX levels only). Screening shall be in accordance with MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500)	Measurement	
	JANS level	JANTX and JANTXV levels
(1) 3c	Thermal impedance, method 3131 of MIL-STD-750 (see 4.3.3)	Thermal impedance, method 3131 of MIL-STD-750 (see 4.3.3)
9	I_{CBO1} and h_{FE1}	Not applicable
10	48 hours minimum	48 hours minimum
11	I_{CBO1}; h_{FE1}; ΔI_{CB01} = 100 percent of initial value or 0.5 μA dc, whichever is greater; Δh_{FE1} = ±15 percent of initial value.	I_{CBO1} and h_{FE1}
12	See 4.3.2	See 4.3.2
13	Subgroups 2 and 3 of table I herein; ΔI_{CB01} = 100 percent of initial value or 200 nA dc, whichever is greater; Δh_{FE1} = ±15 percent of initial value.	Subgroup 2 of table I herein; ΔI_{CB01} = 100 percent of initial value or 200 nA dc, whichever is greater; Δh_{FE1} = ±15 percent of initial value.

* (1) Thermal impedance, see 4.3.3. Shall be performed anytime after temperature cycling, screen 3a; TX and TXV levels do not need to be repeated in screening requirements.

4.3.1 Screening (JANHC and JANKC). Screening of JANHC and JANKC die shall be in accordance with MIL-PRF-19500. As a minimum, die shall be 100 percent probed to ensure the assembled chips will meet the requirements of table I, subgroup 2.

4.3.2 Power burn-in conditions. Power burn-in conditions are as follows: V_{CB} = 10 - 30 V dc. Power shall be applied to achieve T_J = +135°C minimum using a minimum P_D = 75 percent of P_T maximum rated as defined in 1.3. With approval of the qualifying activity and preparing activity, alternate burn-in criteria (hours, bias conditions, T_J, and mounting conditions) may be used for JANTX and JANTXV quality levels. A justification demonstrating equivalence is required. In addition, the manufacturing site's burn-in data and performance history will be essential criteria for burn-in modification approval.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{MD} (and V_C where appropriate). See table III, subgroup 4 and figures 10, 11, 12, and 13 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein. If alternate screening is being performed in accordance with MIL-PRF-19500, a sample of screened devices shall be submitted to and pass the requirements of group A1 and A2 inspection only (table E-VIb, group B, subgroup 1 is not required to be performed again if group B has already been satisfied in accordance with 4.4.2).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500 and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in E-VIa (JANS) of 4.4.2.1 herein. Electrical measurements (end-points) requirements shall be in accordance with table I, subgroup 2 herein. See 4.4.2.2 for JAN, JANTX, and JANTXV group B testing. Electrical measurements (end-points) requirements shall be in accordance with table I, subgroup 2 herein.

4.4.2.1 Group B inspection, table E-VIa (JANS) of MIL-PRF-19500.

Subgroup	Method	Condition
B4	1037	V_{CB} = 10 V dc, 2,000 cycles.
B5	1027	V_{CB} = 10 V dc; $P_D \geq$ 100 percent of maximum rated P_T (see 1.3). (NOTE: If a failure occurs, resubmission shall be at the test conditions of the original sample.) Option 1: 96 hrs minimum, sample size in accordance with table VIa of MIL-PRF-19500, adjust T_A or P_D to achieve T_J = +275°C minimum. Option 2: 216 hrs minimum, sample size = 45, c = 0; adjust T_A or P_D to achieve T_J = +225°C minimum.
B6	3131	$R_{\theta JA}$ for TO-5 and TO-39, $R_{\theta JC}$ for U4 only (see 1.3 and 4.3.3).

4.4.2.2 Group B inspection, (JAN, JANTX, and JANTXV). Separate samples may be used for each step. In the event of a group B failure, the resubmission requirements of MIL-PRF-19500 shall apply. In addition, all catastrophic failures during CI shall be analyzed to the extent possible to identify root cause and corrective action. Whenever a failure is identified as wafer lot or wafer processing related, the entire wafer lot and related devices assembled from the wafer lot shall be rejected unless an appropriate determined corrective action to eliminate the failure mode has been implemented and the devices from the wafer lot are screened to eliminate the failure mode.

Step	Method	Condition
1	1026	Steady-state life: 1,000 hours, V_{CB} = 10 dc, power shall be applied to achieve T_J = +150°C minimum using a minimum of P_D = 75 percent of maximum rated P_T as defined in 1.3. n = 45 devices, c = 0. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.
2	1048	Blocking life, T_A = +150°C, V_{CB} = 80 percent of rated voltage, 48 hours minimum. n = 45 devices, c = 0.
3	1032	High-temperature life (non-operating), t = 340 hours, T_A = +200°C. n = 22, c = 0.

4.4.2.3 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

a. For JAN, JANTX, and JANTXV, samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot. For JANS, samples shall be selected from each inspection lot. See MIL-PRF-19500.

b. Shall be chosen from an inspection lot that has been submitted to and passed table I, subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (subgroups B4 and B5 for JANS, and group B for JAN, JANTX, and JANTXV) may be pulled prior to the application of final lead finish.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-VII of MIL-PRF-19500, and in 4.4.3.1 (JANS) and 4.4.3.2 (JAN, JANTX, and JANTXV) herein for group C testing. Electrical measurements (end-points) requirements shall be in accordance with table I and subgroup 2 herein.

4.4.3.1 Group C inspection, table E-VII (JANS) of MIL-PRF-19500.

Subgroup	Method	Condition
C2	2036	Test condition E, except the UA and U4 packages.
C5	3131	$R_{\theta JA}$ for TO-5 and TO-39, $R_{\theta JC}$ for U4 only, as applicable (see 1.3 and see 4.3.3) and in accordance with thermal impedance curves.
C6	1026	1,000 hours at V_{CB} = 10 V dc; power shall be applied to achieve T_J = +150°C minimum and a minimum of P_D = 75 percent of maximum rated P_T as defined in 1.3. n = 45 devices, c = 0. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.

4.4.3.2 Group C inspection, table E-VII (JAN, JANTX, and JANTXV) of MIL-PRF-19500.

Subgroup	Method	Condition
C2	2036	Except the UA and U4 packages.
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see 1.3 and 4.3.3) and in accordance with thermal impedance curves.
C6		Not applicable.

4.4.3.3 Group C sample selection. Samples for subgroups in group C shall be chosen at random from any lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes table I tests for conformance inspection. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

4.4.4 Group D inspection. Conformance inspection for hardness assured JANS, JANTX, and JANTXV types shall include the group D tests specified in table II herein. These tests shall be performed as required in accordance with MIL-PRF-19500 and method 1019 of MIL-STD-750, for total ionizing dose or method 1017 of MIL-STD-750 for neutron fluence as applicable (see 6.2 herein), except group D, subgroup 2 may be performed separate from other subgroups. Group D inspection may also be performed ahead of the screening lot using die selected in accordance with MIL-PRF-19500 and related documents. Alternate package options may also be substituted for the testing provided there is no adverse effect to the fluence profile.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in appendix E, table E-IX of MIL-PRF-19500 and as specified in table III herein. Electrical measurements (end-points) shall be in accordance with table I, group A, subgroup 2 herein

4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
		Conditions		Min	Max	
Subgroup 1 2/						
Visual and mechanical 3/ examination	2071	n = 45 devices, c = 0				
Solderability 3/ 4/	2026	n = 15 leads, c = 0				
Resistance to 3/ 4/ 5/ solvent	1022	n = 15 devices, c = 0				
Temp cycling 3/ 4/	1051	Test condition C, 25 cycles. n = 22 devices, c = 0				
Hermetic seal 4/	1071	n = 22 devices, c = 0				
Fine leak Gross leak						
Electrical measurements 4/		Table I, subgroup 2				
Bond strength 3/ 4/	2037	Precondition T_A = +250°C at t = 24 hrs or T_A = +300°C at t = 2 hrs, n = 11 wires, c = 0				
Decap internal visual (design verification) 4/	2075	n = 4 devices, c = 0				
Subgroup 2						
Thermal impedance 6/	3131	See 4.3.3	$Z_{\theta JX}$			°C/W
Emitter to base cutoff current	3061	Bias condition D, V_{EB} = 7 V dc	I_{EBO1}		10	µA dc
Collector to emitter cutoff	3041	Bias condition D	I_{CEO}			
2N3439, 2N3439L, 2N3439UA, 2N3439U4		V_{CE} = 300 V dc			2	µA dc
2N3440, 2N3440L, 2N3440UA, 2N3440U4		V_{CE} = 200 V dc			2	µA dc
Collector to emitter cutoff current	3041	Bias condition A, V_{BE} = -1.5 V dc	I_{CEX}			
2N3439, 2N3439L, 2N3439UA, 2N3439U4		V_{CE} = 450 V dc			5	µA dc
2N3440, 2N3440L, 2N3440UA, 2N3440U4		V_{CE} = 300 V dc			5	µA dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

	Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
		Method	Conditions		Min	Max	
	Subgroup 2 - Continued						
	Collector to base cutoff current	3036	Bias condition D	I_{CBO1}			
	2N3439, 2N3439L, 2N3439UA, 2N3439U4		V_{CB} = 360 V dc			2	µA dc
	2N3440, 2N3440L, 2N3440UA, 2N3440U4		V_{CB} = 250 V dc			2	µA dc
	Collector to base cutoff current	3036	Bias condition D	I_{CBO2}			
	2N3439, 2N3439L, 2N3439UA, 2N3439U4		V_{CB} = 450 V dc			5	µA dc
	2N3440, 2N3440L, 2N3440UA, 2N3440U4		V_{CB} = 300 V dc			5	µA dc
*	Base emitter voltage (nonsaturated)	3066	Test condition B, pulsed (see 4.5.1), I_C = 50 mA dc, I_B = 4 mA dc	$V_{BE(sat)}$		1.3	V dc
	Collector to emitter voltage (saturated)	3071	Pulsed (see 4.5.1), I_C = 50 mA dc, I_B = 4 mA dc	$V_{CE(sat)}$		0.5	V dc
	Forward-current transfer ratio	3076	Pulsed (see 4.5.1), V_{CE} = 10 V dc, I_C = 20 mA	h_{FE1}	40	160	
	Forward-current transfer ratio	3076	Pulsed (see 4.5.1), V_{CE} = 10 V dc, I_C = 2 mA	h_{FE2}	30		
	Forward-current transfer ratio	3076	Pulsed (see 4.5.1), V_{CE} = 10 V dc, I_C = 0.2 mA	h_{FE3}	10		
	Subgroup 3						
	High temperature operation:		T_A = +150°C				
	Collector to emitter cutoff current	3036	Bias condition D	I_{CB03}			
	2N3439, 2N3439L, 2N3439UA, 2N3439U4		V_{CB} = 360 V dc			6	µA dc
	2N3440, 2N3440L, 2N3440UA, 2N3440U4		V_{CB} = 250 V dc			6	µA dc
	Low temperature operation:		T_A = -55°C				
	Forward-current transfer ratio	3076	V_{CE} = 10 V dc, I_C = 20 mA dc, pulsed (see 4.5.1)	h_{FE4}	15		

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 4						
Pulse response:	3251	Test condition A				
Turn-on time		V_{CC} = 200 V dc, I_C = 20 mA dc, I_{B1} = 2 mA dc, see figure 14	t_{on}		1	µs
Turn-off time		V_{CC} = 200 V dc, I_C = 20 mA dc, I_{B1} = -I_{B2} = 2 mA dc, see figure 14	t_{off}		10	µs
Magnitude of common- emitter small-signal short-circuit forward-current transfer ratio	3306	V_{CE} = 10 V dc, I_C = 10 mA dc, f = 5 MHz	$\|h_{fe}\|$	3	15	
Open capacitance input open circuited	3236	V_{CB} = 10 V dc, I_E = 0, 100 kHz ≤ f ≤ 1 MHz	C_{obo}		10	pF
Small-signal short- circuit forward-current transfer ratio	3206	V_{CE} = 10 V dc, I_C = 5 mA, f = 1 kHz	h_{fe}	25		
Input capacitance (output open circuited)	3240	V_{CB} = 5 V dc, I_E = 0, 100 kHz ≤ f ≤ 1 MHz	C_{ibo}		75	pF
Subgroup 5						
Safe operating area (continuous dc)	3051	(See figure 15) T_C = +25°C, 1 cycle, t = 1.0 s.				
Test 1		V_{CE} = 5 V dc, I_C = 1 A dc				
Test 2						
Only 2N3439, 2N3439L, 2N3439UA		V_{CE} = 350 V dc, I_C = 14 mA dc				

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 5 - Continued						
Test 3						
Only 2N3440, 2N3440L, 2N3440UA		V_{CE} = 250 V dc, I_C = 20 mA dc				
Electrical measurements		See table I, subgroup 2 herein.				
* Breakdown voltage, collector to emitter	3011	I_C = 10 mA, R_{BB1} = 470 ohms V_{BB1} = 6 V, f = 30 to 60 Hz	$V_{BR(CEO)}$			V dc
2N3439, 2N3439L, 2N3439UA				350		
2N3440, 2N3440L, 2N3440UA				250		

1/ For sampling plan, see MIL-PRF-19500.
2/ For resubmission of failed test in subgroup 1 of table I, double the sample size of the failed test or sequence of tests. A failure in table I, subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.
3/ Separate samples may be used.
4/ Not required for JANS.
5/ Not required for laser marked devices.
6/ This test required for the following end-point measurements only: See 4.3.3 and figures 10, 11, 12, and 13.
Group B, subgroups 3, 4, and 5.
Group B, step 1.
Group C, subgroups 2 and 6.
Group E, subgroups 1 and 2.

TABLE II. Group D inspection.

	Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Limit		Unit
		Method	Conditions		Min	Max	
	Subgroup 1 4/						
	Neutron irradiation	1017	Neutron exposure V_{CES} = 0 V				
	Emitter to base cutoff current	3061	Bias condition D, V_{EB} = 7 V dc	I_{EBO1}		20	µA dc
	Collector to emitter cutoff	3041	Bias condition D	I_{CEO}			
	2N3439, 2N3439L, 2N3439UA, 2N3439U4		V_{CE} = 300 V dc			4	µA dc
	2N3440, 2N3440L, 2N3440UA, 2N3440U4		V_{CE} = 200 V dc			4	µA dc
	Collector to emitter cutoff current	3041	Bias condition A, V_{BE} = -1.5 V dc	I_{CEX}			
	2N3439, 2N3439L, 2N3439UA, 2N3439U4		V_{CE} = 450 V dc			10	µA dc
	2N3440, 2N3440L, 2N3440UA, 2N3440U4		V_{CE} = 300 V dc			10	µA dc
	Collector to base cutoff current	3036	Bias condition D	I_{CBO1}			
	2N3439, 2N3439L, 2N3439UA, 2N3439U4		V_{CB} = 360 V dc			4	µA dc
	2N3440, 2N3440L, 2N3440UA, 2N3440U4		V_{CB} = 250 V dc			4	µA dc
	Collector to base cutoff current	3036	Bias condition D	I_{CBO2}			
	2N3439, 2N3439L, 2N3439UA, 2N3439U4		V_{CB} = 450 V dc			10	µA dc
	2N3440, 2N3440L, 2N3440UA, 2N3440U4		V_{CB} = 300 V dc			10	µA dc
*	Base emitter voltage (nonsaturated)	3066	Test condition B, pulsed (see 4.5.1), I_C = 50 mA dc, I_B = 4 mA dc	$V_{BE(sat)}$		1.5	V dc
	Collector to emitter voltage (saturated)	3071	Pulsed (see 4.5.1), I_C = 50 mA dc, I_B = 4 mA dc	$V_{CE(sat)}$		0.56	V dc
	Forward-current transfer ratio	3076	Pulsed (see 4.5.1), V_{CE} = 10 V dc, I_C = 20 mA	h_{FE1} 5/	[20]	160	
	Forward-current transfer ratio	3076	Pulsed (see 4.5.1), V_{CE} = 10 V dc, I_C = 2 mA	h_{FE2} 5/	[15]		
	Forward-current transfer ratio	3076	Pulsed (see 4.5.1), V_{CE} = 10 V dc, I_C = 0.2 mA	h_{FE3} 5/	[5]		

See footnotes at end of table.

TABLE II. Group D inspection -Continued.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 2						
Total dose irradiation	1019	Gamma exposure				
2N3439 2N3440		V_{CES} = 280 V V_{CES} = 200 V				
Emitter to base cutoff current	3061	Bias condition D, V_{EB} = 7 V dc	I_{EBO1}		20	µA dc
Collector to emitter cutoff	3041	Bias condition D	I_{CEO}			
2N3439, 2N3439L, 2N3439UA, 2N3439U4		V_{CE} = 300 V dc			4	µA dc
2N3440, 2N3440L, 2N3440UA, 2N3440U4		V_{CE} = 200 V dc			4	µA dc
Collector to emitter cutoff current	3041	Bias condition A, V_{BE} = -1.5 V dc	I_{CEX}			
2N3439, 2N3439L, 2N3439UA, 2N3439U4		V_{CE} = 450 V dc			10	µA dc
2N3440, 2N3440L, 2N3440UA, 2N3440U4		V_{CE} = 300 V dc			10	µA dc
Collector to base cutoff current	3036	Bias condition D	I_{CBO1}			
2N3439, 2N3439L, 2N3439UA, 2N3439U4		V_{CB} = 360 V dc			4	µA dc
2N3440, 2N3440L, 2N3440UA, 2N3440U4		V_{CB} = 250 V dc			4	µA dc
Collector to base cutoff current	3036	Bias condition D	I_{CBO2}			
2N3439, 2N3439L, 2N3439UA, 2N3439U4		V_{CB} = 450 V dc			10	µA dc
2N3440, 2N3440L, 2N3440UA, 2N3440U4		V_{CB} = 300 V dc			10	µA dc
* Base emitter voltage (nonsaturated)	3066	Test condition B, pulsed (see 4.5.1), I_C = 50 mA dc, I_B = 4 mA dc	$V_{BE(sat)}$		1.5	V dc
Collector to emitter voltage (saturated)	3071	Pulsed (see 4.5.1), I_C = 50 mA dc, I_B = 4 mA dc	$V_{CE(sat)}$		0.56	V dc

See footnotes at end of table.

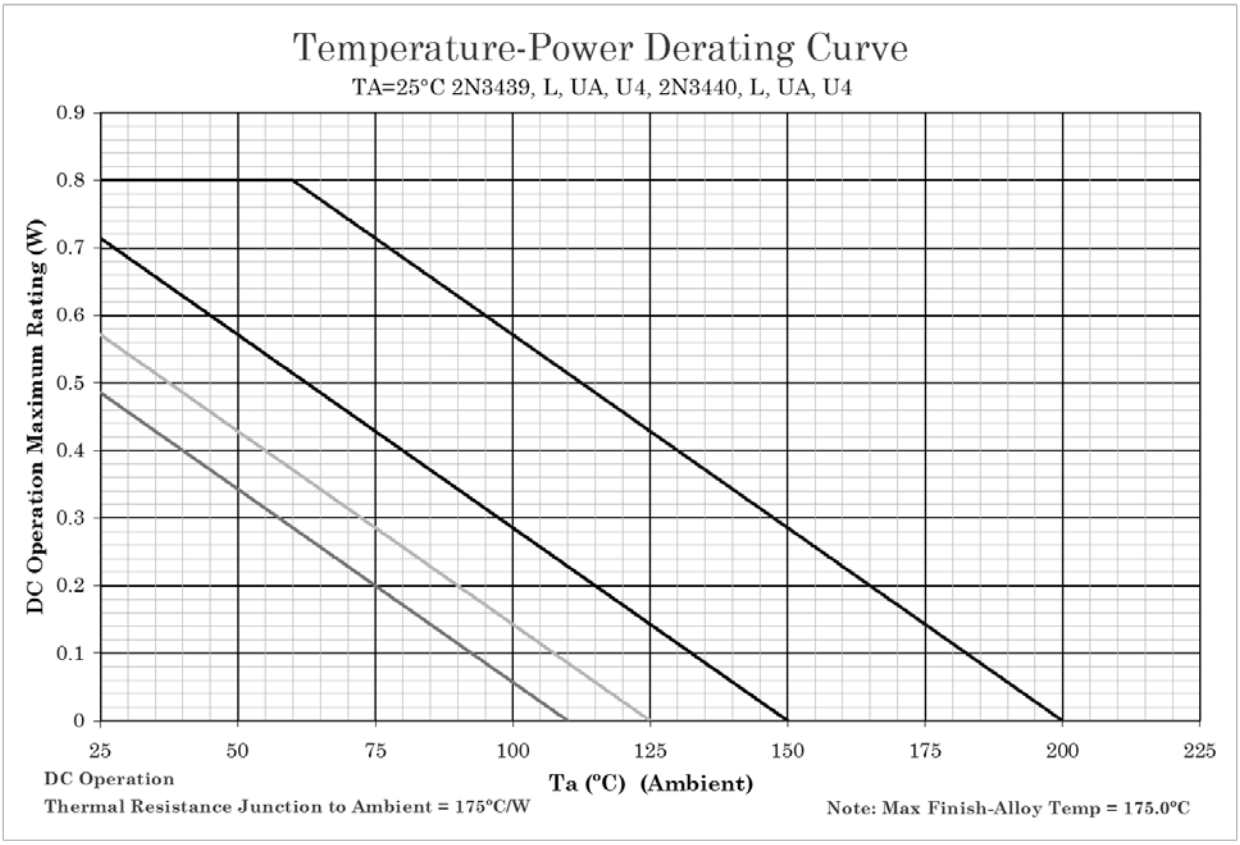
TABLE II. Group D inspection. - Continued.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - Continued.						
Forward-current transfer ratio	3076	Pulsed (see 4.5.1), V_{CE} = 10 V dc, I_C = 20 mA	[h_{FE1}] 5/	[20]	160	
Forward-current transfer ratio	3076	Pulsed (see 4.5.1), V_{CE} = 10 V dc, I_C = 2 mA	[h_{FE2}] 5/	[15]		
Forward-current transfer ratio	3076	Pulsed (see 4.5.1), V_{CE} = 10 V dc, I_C = 0.2 mA	[h_{FE3}] 5/	[5]		

1/ Tests to be performed on all devices receiving radiation exposure.
2/ For sampling plan, see MIL-PRF-19500.
3/ Electrical characteristics apply to device types unless otherwise noted.
4/ Subgroup 1 is an optional test and must be specified on the contract when required.
5/ See method 1019 of MIL-STD-750 for how to determine [h_{FE}] by first calculating the delta ($1/h_{FE}$) from the pre- and post-radiation h_{FE}. Notice the [h_{FE}] is not the same as h_{FE} and cannot be measured directly. The [h_{FE}] value can never exceed the pre-radiation minimum h_{FE} that it is based upon.

* TABLE III. Group E inspection (all quality levels) - for qualification only or re-qualification only.

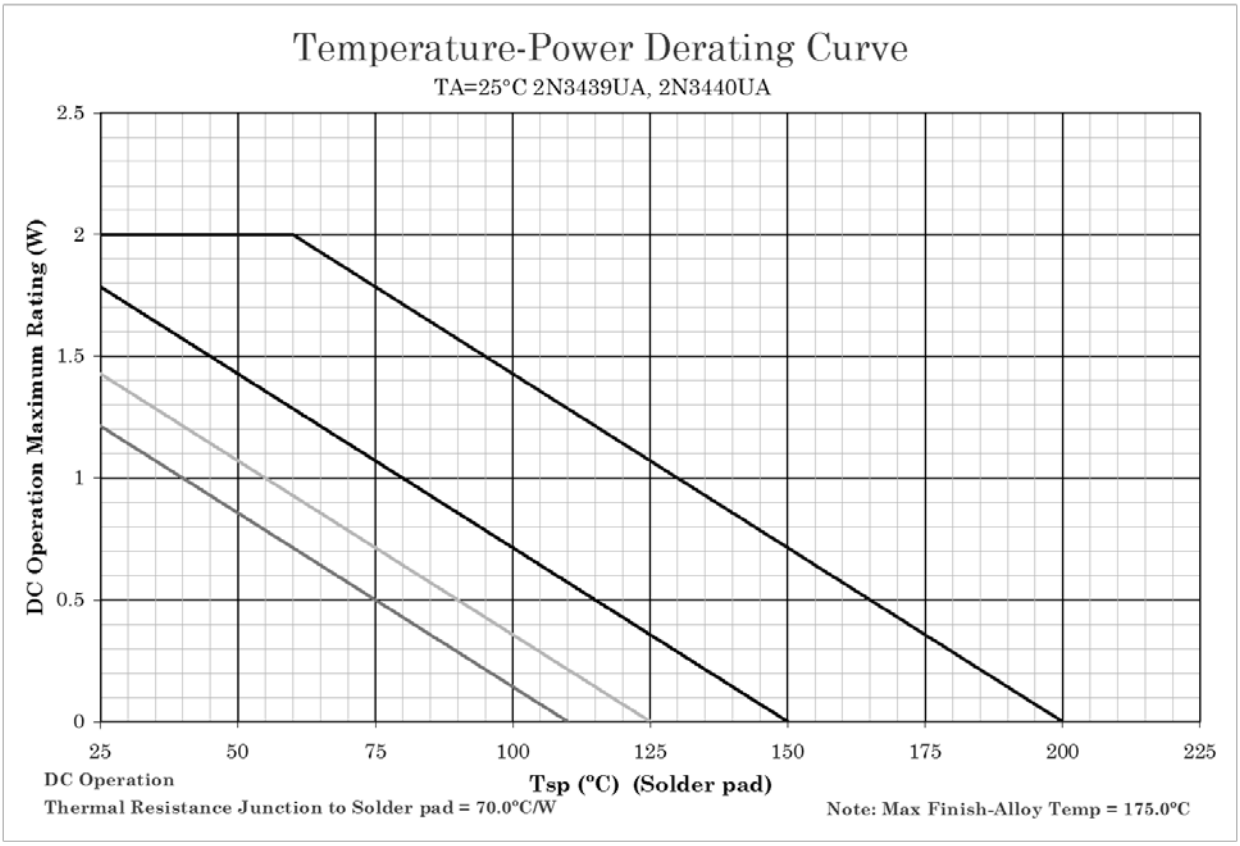
Inspection	MIL-STD-750		Qualification
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles.	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I, subgroup 2.	
Subgroup 2			45 devices c = 0
Intermittent life	1037	Intermittent operation life: $V_{CB} \geq 10$ V dc, 6,000 cycles.	
Electrical measurements		See table I, subgroup 2.	
Subgroup 4			
Thermal resistance	3131	$R_{\theta JSP}$ can be calculated but shall be measured once in the same package with a similar die size to confirm calculations (may apply to multiple specification sheets).	15 devices, c = 0
* Thermal impedance curves		See MIL-PRF-19500.	
Subgroup 5			15 devices, c = 0
Barometric pressure (reduced)	1001	Normal mounting pressure = 8 mm Hg, ±2 mm Hg for 60 s (minimum).	
Electrical measurements		See table I, subgroup 2.	
Subgroups 6			
* ESD (electrostatic discharge)	1020		
Subgroup 8			45 devices c = 0
Reverse stability	1033	Condition A for devices ≥ 400 V, condition B for devices < 400 V.	



NOTES:

1. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq$, 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

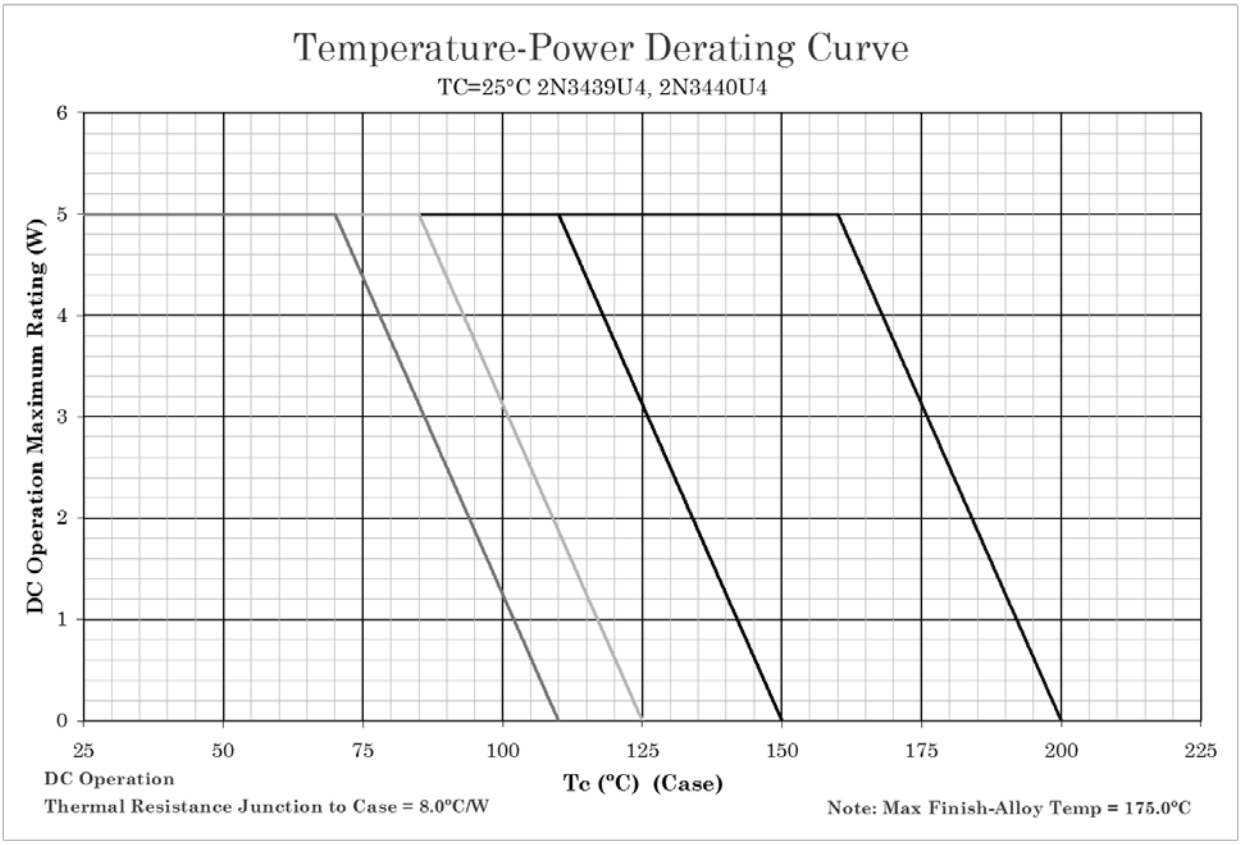
FIGURE 6. Temperature-power derating for all types $R_{\theta JA}$ (TO-5, TO-39, UA, and U4).



NOTES:

1. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

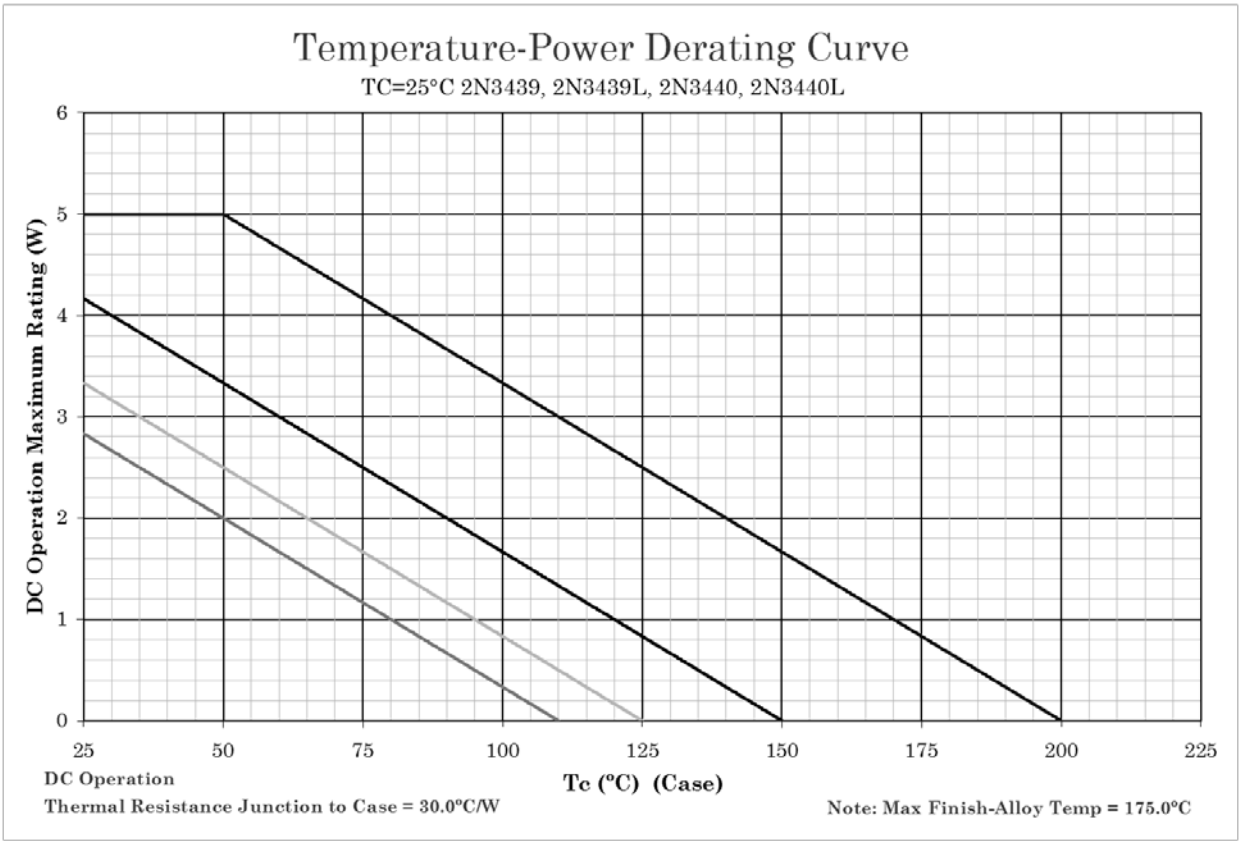
FIGURE 7. Temperature-power derating for 2N3439UA and 2N3440UA.



NOTES:

1. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

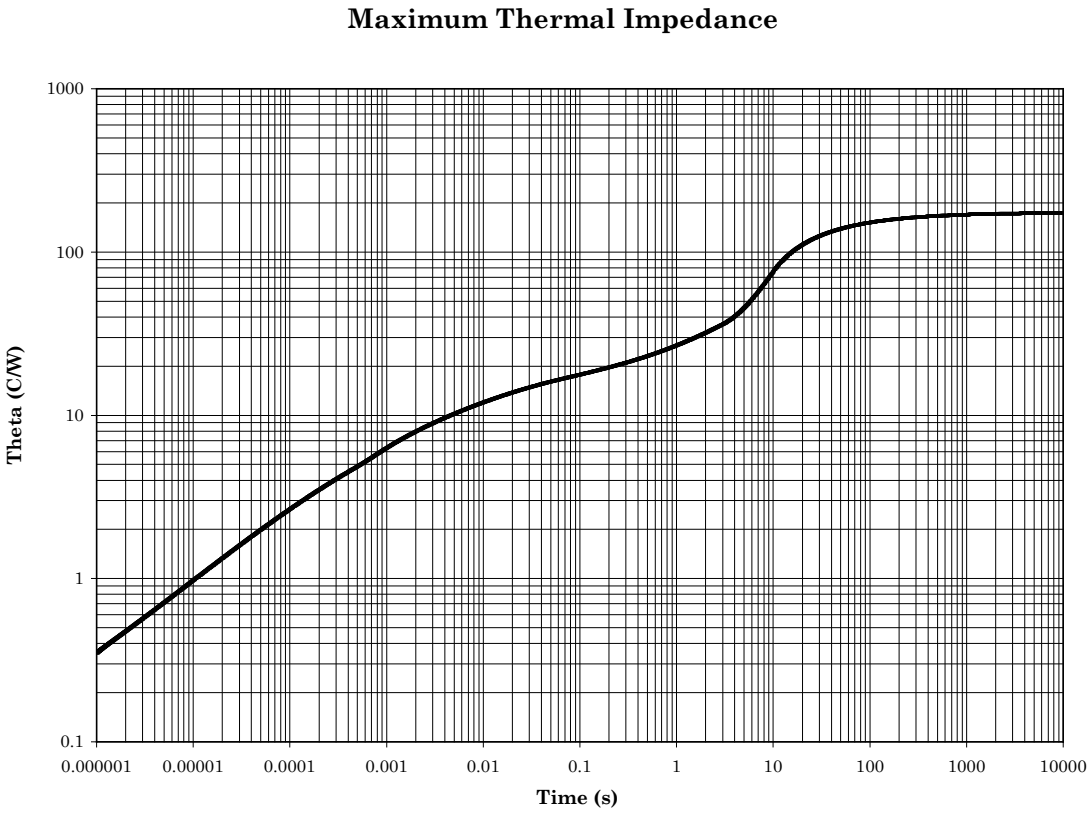
FIGURE 8. Temperature-power derating for 2N3439U4 and 2N3440U4.



NOTES:

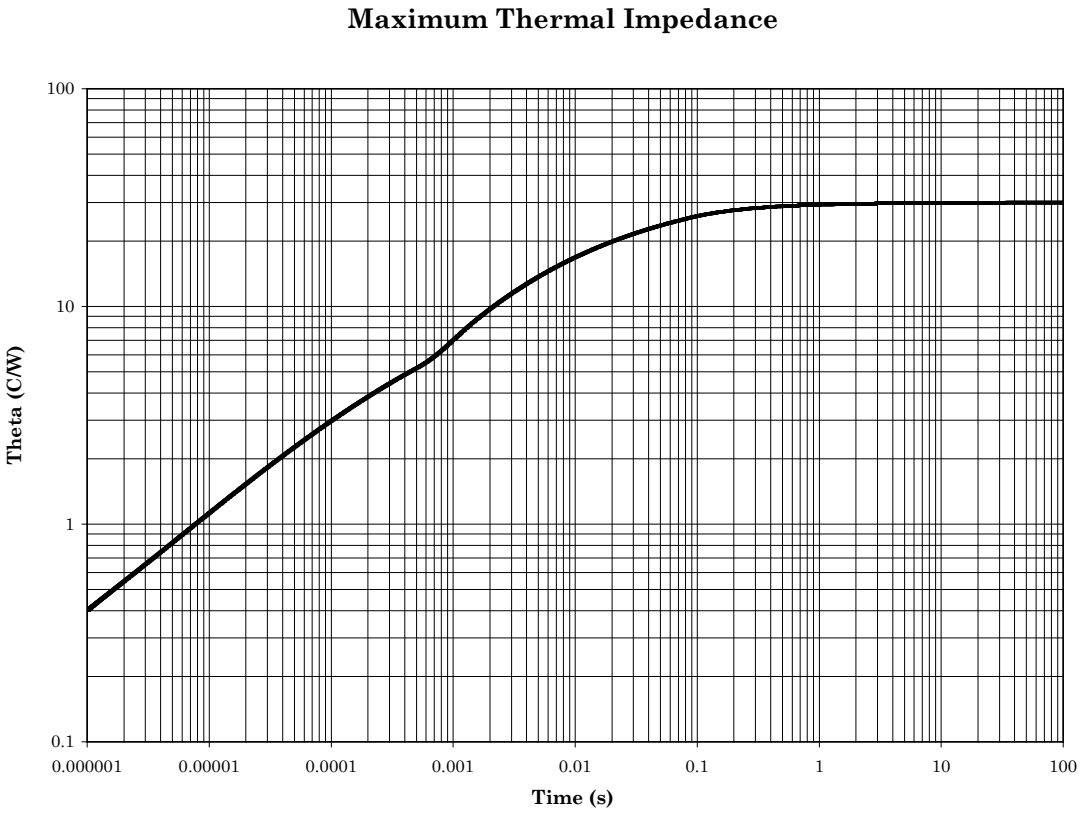
1. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 9. Temperature-power derating for 2N3439, 2N3439L, 2N3440, and 2N3440L.



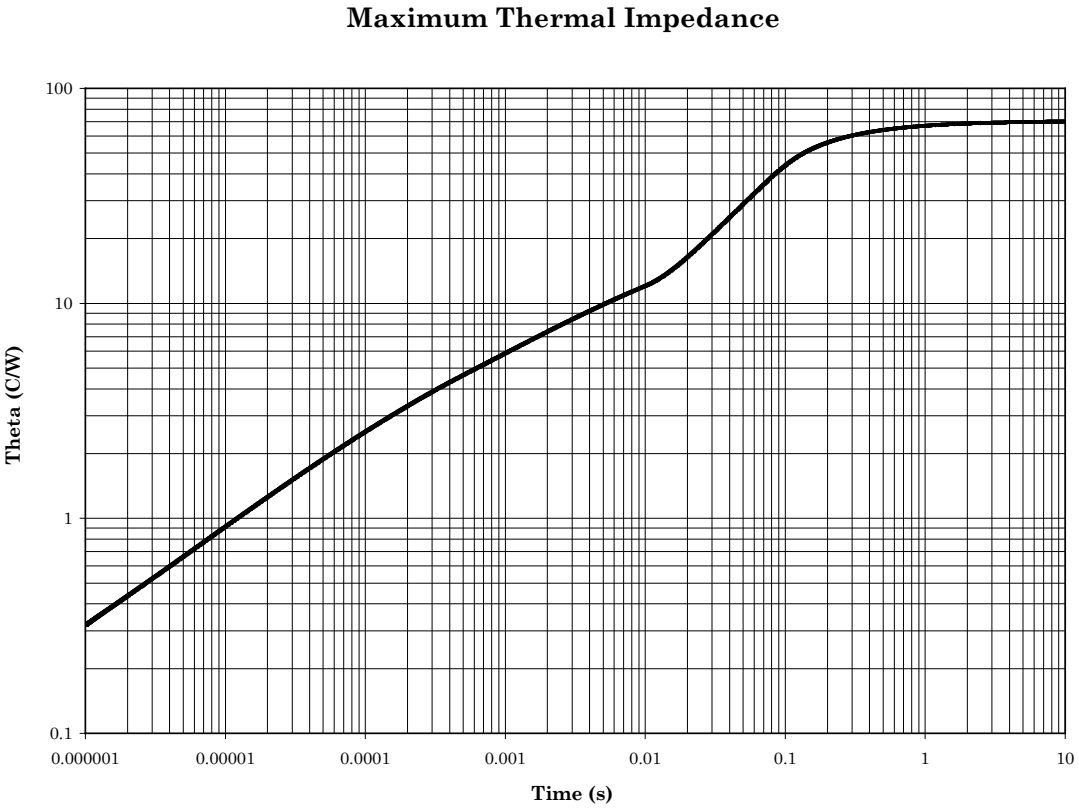
T_A = +25°C, P_T = 0.8W, thermal resistance $R_{\theta JA}$ = 175°C/W.

FIGURE 10. Thermal impedance graph ($R_{\theta JA}$) for 2N3439, 2N3439L, 2N3440, and 2N3440L (TO-5, TO-39, U4, and UA).



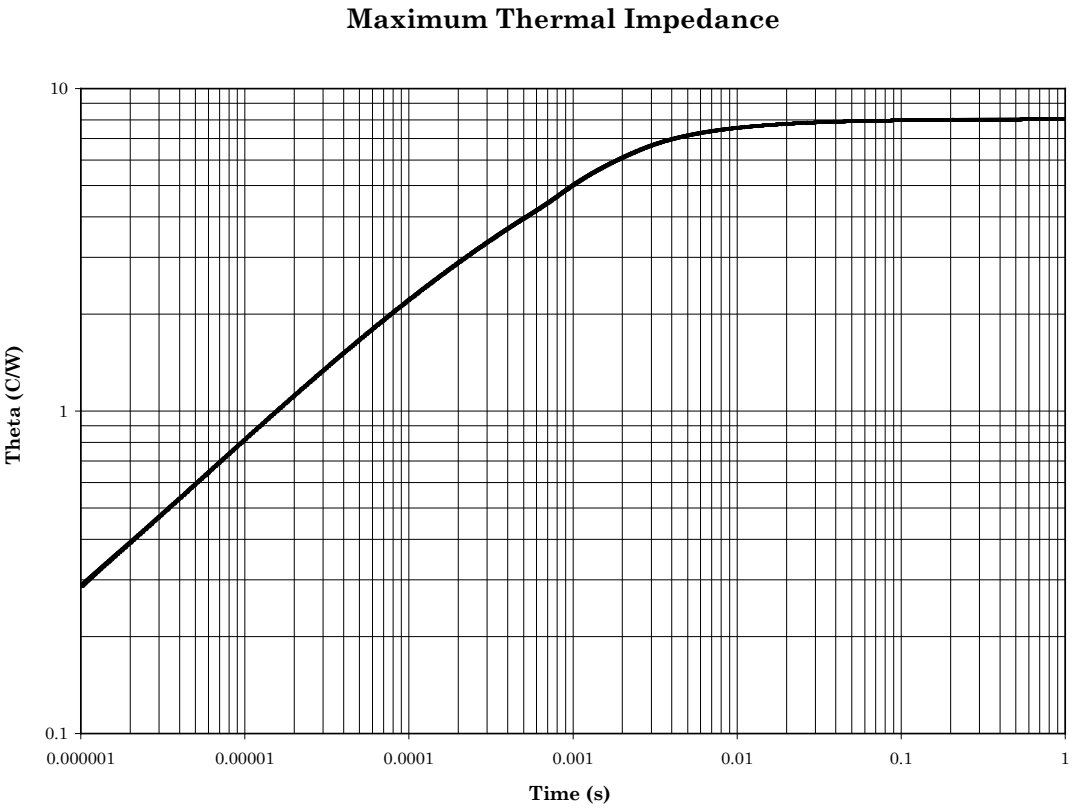
T_C = +25°C, P_T = 5.0W, thermal resistance $R_{\theta JC}$ = 30°C/W, steel.

FIGURE 11. Thermal impedance graph ($R_{\theta JC}$) for 2N3439, 2N3439L, 2N3440, and 2N3440L (TO-5 and TO-39).



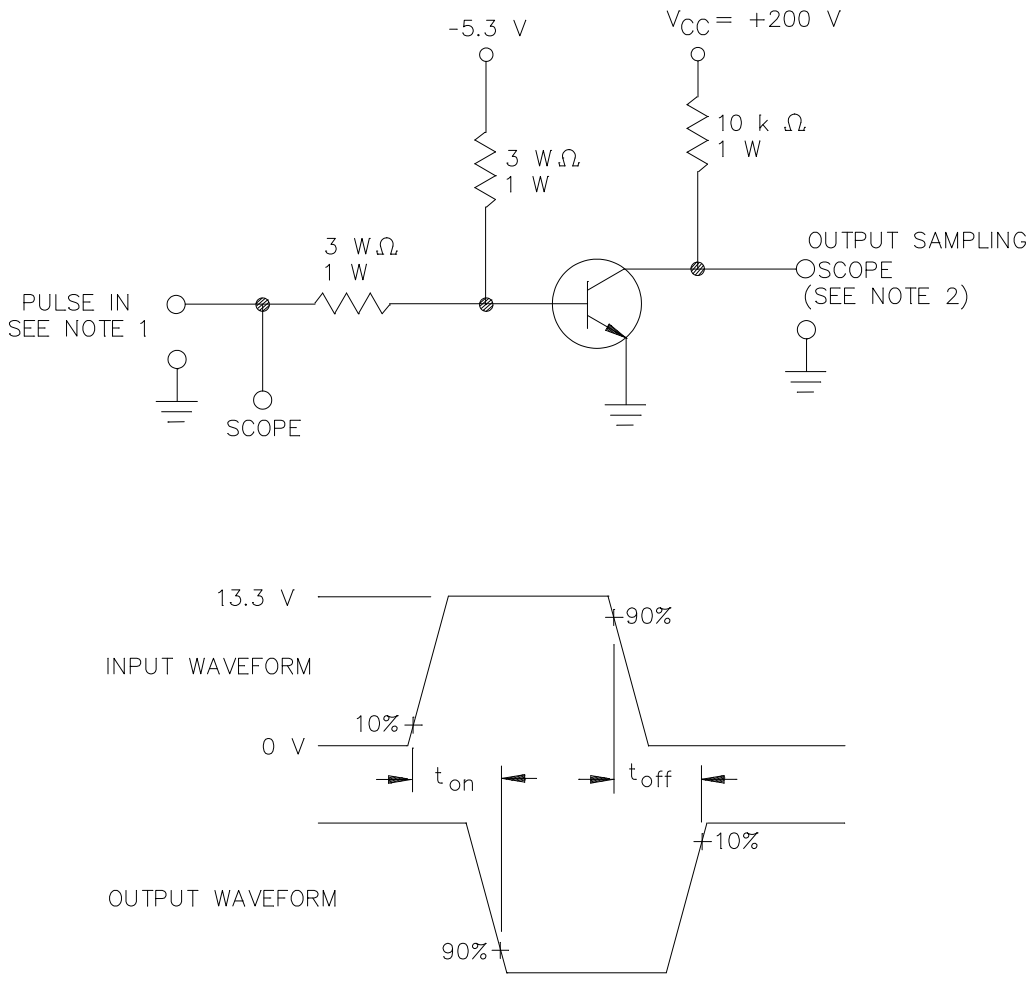
T_C = +25°C, thermal resistance $R_{\theta JSP}$ = 70°C/W, Pdiss = 2W.

FIGURE 12. Thermal impedance graph ($R_{\theta JSP}$) for 2N3439UA and 2N3440UA.



Solder mounted to copper heatsink at T_C = +25C. Thermal resistance $R_{\theta JC}$ = 8.0 C/W

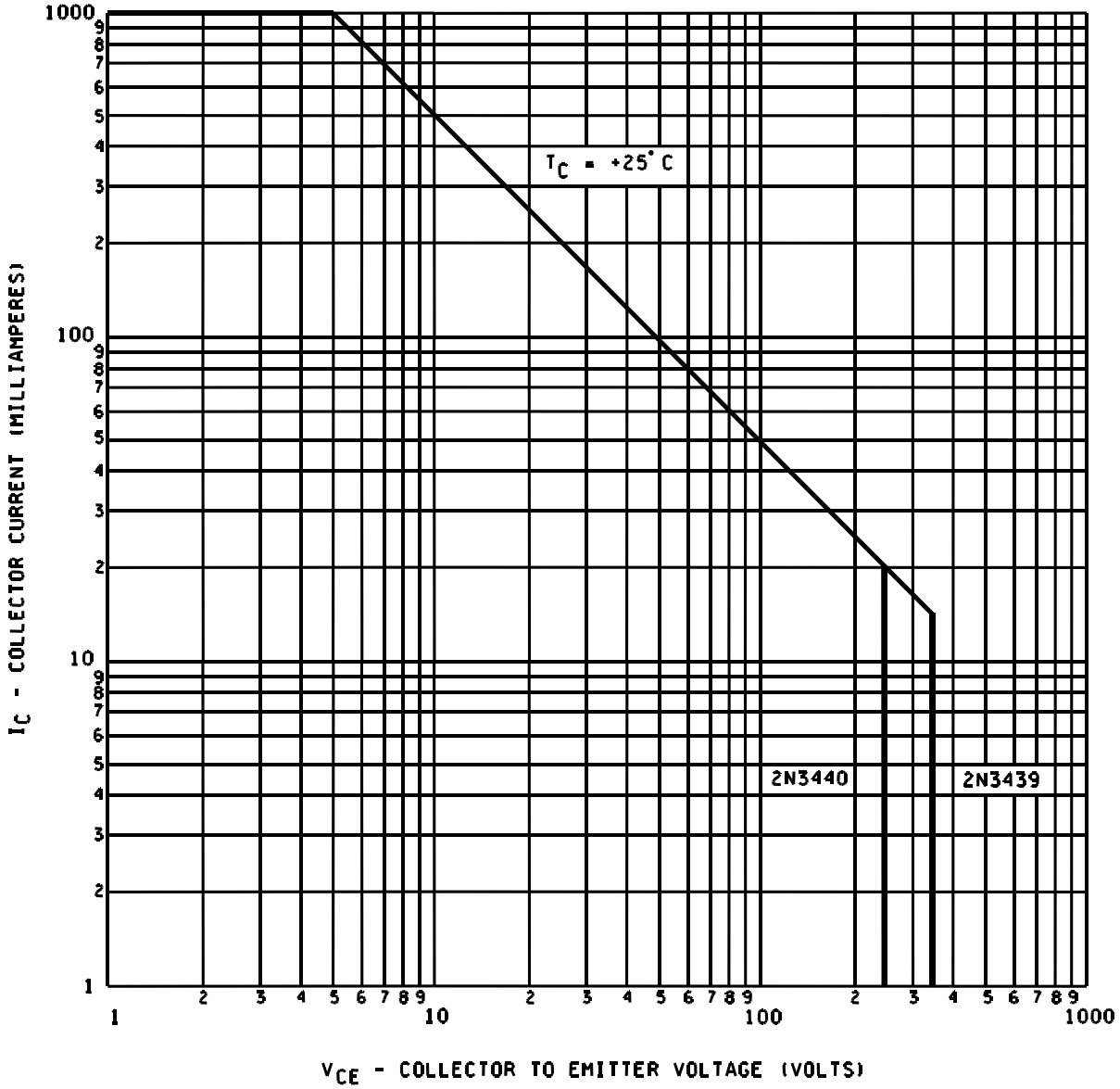
FIGURE 13. Thermal impedance graph ($R_{\theta JC}$) for 2N3439U4, and 2N3440U4 (U4).



NOTES:

1. The rise time (t_r) and fall time (t_f) of applied pulse shall be ≤ 20 ns, duty cycle ≤ 2 percent, generator source impedance shall be 50 ohms, pulse width = 20 μs.
2. Output sampling oscilloscope: Z_{IN} ≥ 100 kΩ, C_{IN} ≤ 50 pF, and rise time ≤ 1.0 μs.

FIGURE 14. Pulse response test circuit.



NOTE: Also applies to the corresponding "L" and "UA" suffix devices.

FIGURE 15. Maximum safe operating graph (continuous dc).

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. Product assurance level and type designator.

e. For acquisition of RHA designed devices, table II, subgroup 1 testing of group D is optional. If subgroup 1 testing is desired, it must be specified in the contract.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil .

6.4 Suppliers of JANHC and JANKC die. The qualified JANHC and JANKC suppliers with the applicable letter version (example JANHCA2N3439) will be identified on the QML.

Die ordering information		
PIN	Manufacturer	
	43611	34156
2N3439	JANHCB2N3439 JANKCB2N3439	JANHCC2N3439 JANKCC2N3439
2N3440	JANHCB2N3440 JANKCB2N3440	JANHCC2N3440 JANKCC2N3440