JN517x

IEEE802.15.4 Wireless Microcontroller

Rev. 3.0 — 7 November 2017 Product data sheet

1. General description

The JN517x series is a range of ultra low power, high performance wireless microcontrollers suitable for ZigBee applications to facilitate the development of Smart Home and Smart Lighting applications. It features a high-performance and low-power ARM Cortex-M3 processor with debug with programmable clock speeds. The JN517x devices are available in JN5174, JN5178 and JN5179 variants, respectively having 160 kB, 256 kB and 512 kB of embedded Flash memory as well as 32 kB of RAM and 4 kB of EEPROM. The embedded Flash can support “Over-The-Air” code download of software stacks. Radio transmit power is configurable up to +10 dBm output. The very-low receive operating current (down to 12.7 mA and with a 0.6 μA sleep timer mode) gives excellent battery life allowing operation direct from a coin cell. The JN517x also includes a 2.4 GHz “IEEE802.15.4 compliant” transceiver and a comprehensive mix of analog and digital peripherals.

The JN517x is ideal for battery-operated applications supported through the comprehensive power-saving modes available in the device. The on-chip peripherals, which include a fail-safe I^2C-bus, SPI-bus ports (both master and slave), and a six-channel analog-digital converter with internal temperature sensor support a wide range of applications directly without extra hardware.

2. Features and benefits

2.1 Benefits

- Very low current solution for long battery life: over 10 years
- Very low receive current for low standby power of receiver always on nodes
- Integrated power amplifier for long range and robust communication
- Large embedded Flash memory to enable Over-The-Air (OTA) firmware updates without external Flash memory
- Single chip device to run communication stack and application
- Supports multiple network stacks
- Peripherals customized for lighting applications
- System BOM is low in component count and cost
- Flexible sensor interfacing
- Package
  - 6 × 6 mm HVQFN40, 0.5 mm pitch
  - lead-free and RoHS compliant
- Temperature range: −40 °C to +125 °C

2.2 Radio features

- 2.4 GHz IEEE802.15.4 compliant Ref. 1
- Receive current 14.8 mA, in low-power receive mode 12.7 mA
- Receiver sensitivity −96 dBm
- Configurable transmit power, for reduced current consumption, for example:
  - 10 dBm, 22.5 mA
  - 8.5 dBm, 19.6 mA
  - 3 dBm, 14 mA
- Radio link budget 106 dB
- Maximum input level of +10 dBm
- Compensation for temperature drift of crystal oscillator frequency
- 2.0 V to 3.6 V battery operation
- Antenna diversity (Auto RX)
- Integrated ultra-low-power sleep oscillator (0.6 μA)
- 100 nA deep sleep current with wake-up from external event
- 128-bit AES security processor
- MAC accelerator with packet formatting, CRCs, address check, auto-acks, timers

2.3 Microcontroller features

- ARM Cortex-M3 CPU with debug support
- JN5174: 160 kB/32 kB/4 kB (Flash/RAM/EEPROM)
- JN5178: 256 kB/32 kB/4 kB (Flash/RAM/EEPROM)
- JN5179: 512 kB/32 kB/4 kB (Flash/RAM/EEPROM)
- OTA firmware upgrade capability
- 32 MHz clock selectable down to 1 MHz for low-power operation
- Dual PAN ID support
- Fail-safe I^2C-bus interface. operates as either master or slave
- 8 Timers (6 × PWM and 2 timer/counters)
- 2 low-power sleep counters
- 2 × UART, one with flow control
- SPI-bus master and slave port, 2 simultaneous selects
- Variable instruction width for high coding efficiency
- Multi-stage instruction pipeline
- Data EEPROM with guaranteed 100 k write operations
- Supply voltage monitor with 8 programmable thresholds
- Battery voltage and temperature sensors
- 6-input 10-bit ADC
- Analog comparator
- Digital monitor for ADC
- Watchdog timer and POR
- Low-power modes controller
- Up to 18 Digital IO (DIO) and 2 digital outputs pins

3. Applications

- Robust and secure low-power wireless applications
- ZigBee 3.0
- Commercial Building and Home Automation
- Smart Lighting networks
- Internet of Things (IoT)
- Toys and gaming peripherals
- Energy harvesting, for example self-powered light switch

4. Overview

The JN517x is an IEEE802.15.4 wireless microcontroller that provides a fully integrated solution for applications using the IEEE802.15.4 standard in the 2.4 GHz to 2.5 GHz ISM frequency band, including ZigBee PRO.

Applications that transfer data wirelessly tend to be more complex than wired ones. Wireless protocols make stringent demands on frequencies, data formats, timing of data transfers, security and other issues. Application development must consider the requirements of the wireless network in addition to the product functionality and user interfaces. To minimize this complexity, NXP provides a series of software libraries and interfaces that control the transceiver and peripherals of the JN517x. These libraries and interfaces remove the need for the developer to understand wireless protocols and greatly simplifies the programming complexities of power modes, interrupts and hardware functionality.

In view of the above, it is not necessary to provide the register details of the JN517x in the data sheet.

The device includes a wireless transceiver, ARM Cortex-M3 CPU, “on-chip memory” and an extensive range of peripherals.

4.1 Wireless transceiver

The wireless transceiver comprises a 2.45 GHz radio, a modem, a baseband controller and a security coprocessor. In addition, the radio also provides an output to control transmit-receive switching of external devices such as power amplifiers allowing applications that require increased transmit power to be realized very easily. Section 15.1 describes a complete reference design including Printed-Circuit Board (PCB) design and Bill Of Materials (BOM).

The security coprocessor provides hardware-based 128-bit AES-CCM modes as specified by the IEEE802.15.4 2006 standard. Specifically this includes encryption and authentication covered by the MIC-32/-64/-128, ENC and ENC-MIC-32/-64/-128 modes of operation.

The transceiver elements (radio, modem and baseband) work together to provide IEEE802.15.4 (2006) MAC and PHY functionality under the control of a protocol stack. The transmitter is equipped with a power amplifier with 3 options for transmit power (major steps, fine steps and attenuator) see Figure 51. Applications incorporating IEEE802.15.4 functionality can be developed rapidly by combining user-developed application software

with a protocol stack library.

4.2 CPU and memory

An ARM Cortex-M3 CPU allows software to be run on-chip, its processing power being shared between the IEEE802.15.4 MAC protocol, other higher layer protocols and the user application. The JN517x has a unified memory architecture, where code memory, data memory, peripheral devices and IO ports are organized within the same linear address space. The device contains 160 kB or 256 kB or 512 kB of Flash and 32 kB of RAM and 4 kB EEPROM.

4.3 Peripherals

The following peripherals are available on chip:

- Master SPI-bus port with 2 simultaneous select outputs
- Slave SPI-bus port
- 2 UARTs: one capable of hardware flow control (4-wire, includes RTS/CTS) and the other a 2-wire (RX/TX).
- 2 programmable timer/counters which support Pulse Width Modulation (PWM) and capture/compare, plus 6 PWM timers which support PWM and Timer modes only.
- 2 programmable sleep timers and a system tick timer
- 2-wire serial interface (compatible with SMbus and I^2C-bus) supporting master and slave operation. Fail-safe open-drain IOs for I^2C-bus.
- 18 digital IO lines (multiplexed with peripherals such as timers, SPI-bus and UARTs)
- 2 digital outputs (multiplexed with SPI-bus port)
- 10-bit, Analog-to-Digital Converter with 6 input channels. Autonomous multi-channel sampling.
- Programmable analog comparator
- Digital comparator/monitor linked to ADC
- Internal temperature sensor and battery monitor
- 2 low-power pulse counters
- Random number generator
- Watchdog Timer and Supply Voltage Monitor (SVM)
- Debug support using serial-wire or 4-pin JTAG interface
- Debug trace port with up to 4 data lines.
- Transmit and receive antenna diversity with automatic receive switching based on received energy detection

User applications access the peripherals using the Integrated Peripherals API. For further details, refer to the JN517x Integrated Peripherals API User Guide, JN-UG-3118 on the Wireless Connectivity area of the NXP web site Ref. 2. This allows applications to use a tested and easily understood view of the peripherals allowing rapid system development.

5. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
JN517x[1]	HVQFN40	Plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 × 6 × 0.85 mm	SOT618-8

[1] x = 4: Flash = 160 kB.
x = 8: Flash = 256 kB.
x = 9: Flash = 512 kB.

For further details, refer to the Wireless Connectivity area of the NXP web site Ref. 2.

6. Block diagram

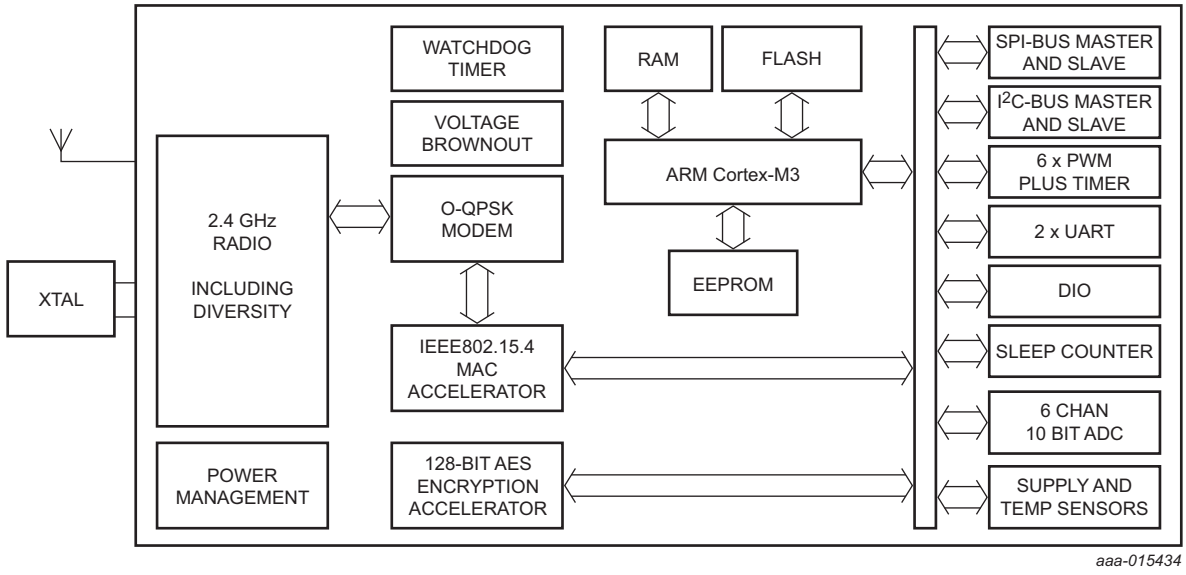
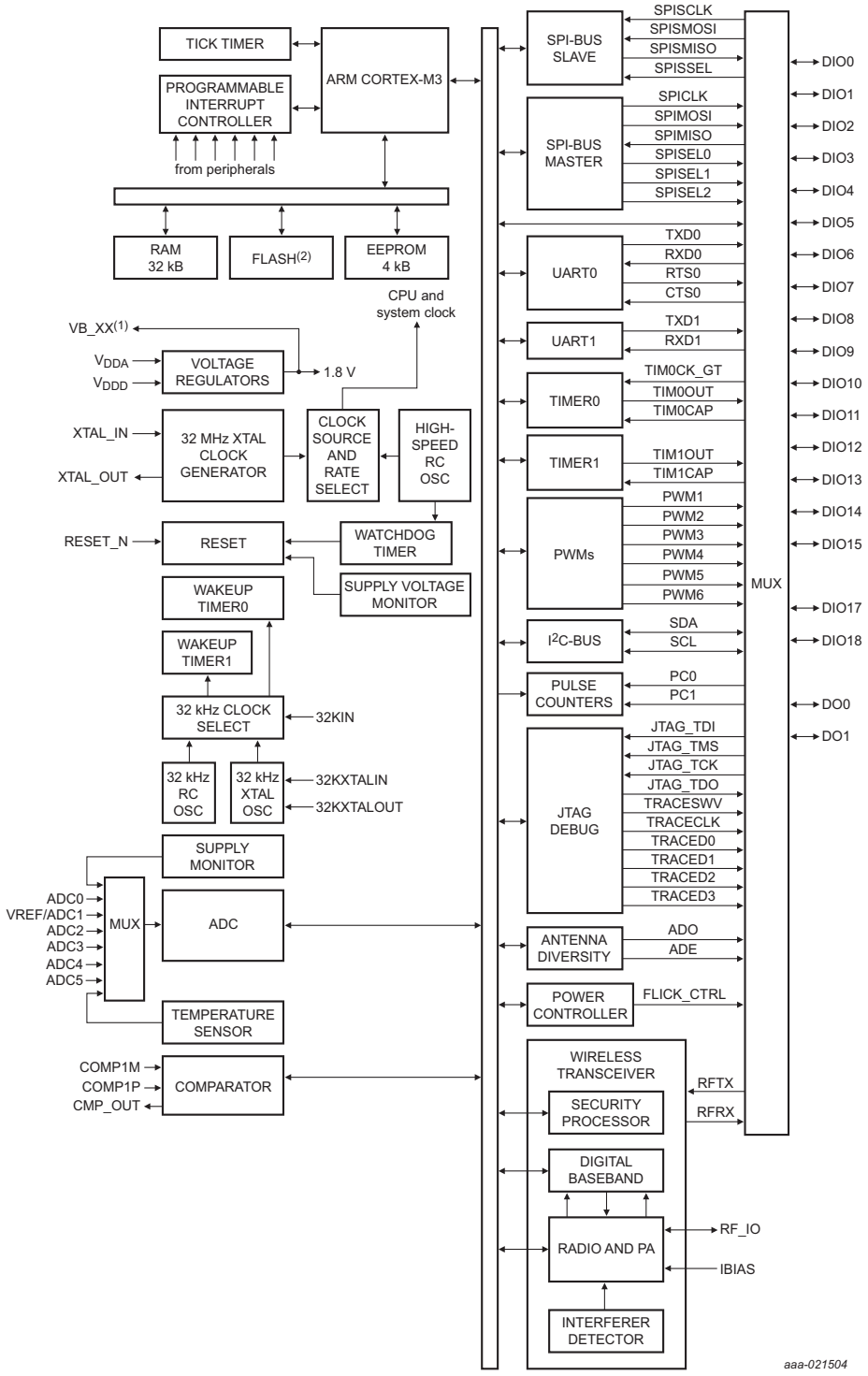


Fig 1. Block diagram

7. Functional diagram



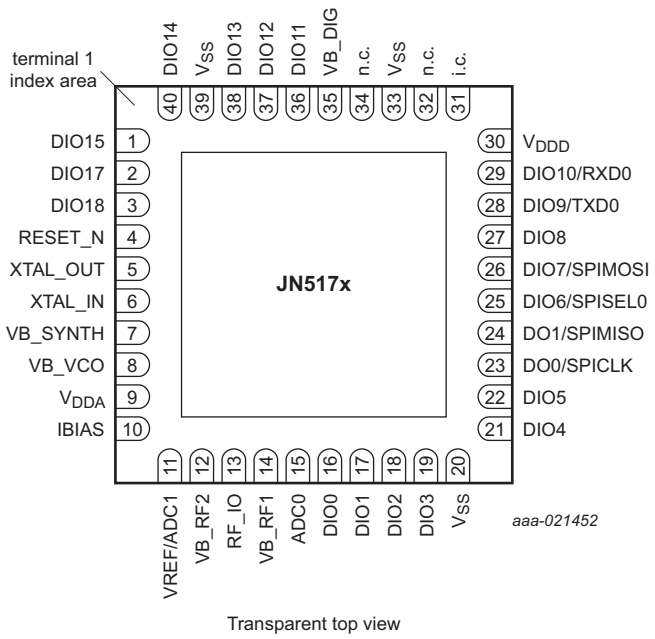
(1) With XX = SYNTH or VCO or RF2 or RF1 or DIG.

(2) JN5174: 160 kB, JN5178: 256 kB and JN5179: 512 kB.

Fig 2. Functional block diagram

8. Pinning information

8.1 Pinning



Transparent top view

Refer to Section 15.1 for important applications information regarding the connection of the paddle to the PCB.

Fig 3. Pin configuration

8.2 Pin description

Table 2. Pin description

Symbol	Pin	Type[1]	Default at reset/ during boot	Default internal pull-up/pull-down	Description
DIO15	1	IO	DIO15 (I)	pull-down	**DIO15 —** digital input/output 15
					PWM6 — PWM6 output
					JTAG_TDO — JTAG TDO data output
					SPIMOSI — SPI-bus master data output
					SPISEL1 — SPI-bus master select output 1
					TIM0CK_GT — Timer0 - clock gate input
					TRACESWV — ARM trace Serial Wire Viewer output
					SPISSEL — SPI-bus slave select input
DIO17	2	IO	at reset: DIO17 (I); during boot: SWCK (I)	pull-up	**DIO17 —** digital input/output 17
					JTAG_TCK — JTAG TCK input
					SWCK — Serial Wire Debugger Clock input
					SPISEL0 — SPI-bus master select output 0
					TIM1CAP — Timer1 capture input
					COMP1P — comparator plus input
					SPISMISO — SPI-bus slave data output
DIO18	3	IO	DIO18 (I)	pull-up	**DIO18 —** digital input/output 18
					JTAG_TMS — JTAG TMS input
					SWD — Serial Wire Debugger input
					SPIMISO — SPI-bus master data input
					TIM1OUT — Timer1 output
					COMP1M — comparator minus input
					SPISCLK — SPI-bus slave clock input
RESET_N	4	I		pull-up	**RESET_N —** reset input
XTAL_OUT	5	O		pull-up	**XTAL_OUT —** system crystal oscillator
XTAL_IN	6	I		pull-up	**XTAL_IN —** system crystal oscillator
VB_SYNTH	7	P			**VB_SYNTH —** regulated supply voltage
VB_VCO	8	P			**VB_VCO —** regulated supply voltage
V_{DDA}	9	P			**V_{DDA} —** analog supply voltage
IBIAS	10	I			**IBIAS —** bias current control
VREF/ADC1	11	I			**VREF —** analog peripheral reference voltage
					ADC1 — ADC input 1
VB_RF2	12	P; 1.8 V			**VB_RF2 —** regulated supply voltage
RF_IO	13	IO			**RF_IO —** RF antenna
VB_RF1	14	P; 1.8 V			**VB_RF1 —** regulated supply voltage
ADC0	15	I			**ADC0 —** ADC input 0

Table 2. Pin description *…continued*

Symbol	Pin	Type[1]	Default at reset/ during boot	Default internal pull-up/pull-down	Description
DIO0	16	IO	DIO0 (I)	pull-up	**DIO0 —** digital input/output 0
					ADC4 — ADC input 4
					SPISEL0 — SPI-bus master select output 0
					RFRX — radio receiver control output
					FLICK_CTRL — flicker control output
					ADO — antenna diversity odd output
DIO1	17	IO	DIO1 (I)	pull-up	**DIO1 —** digital input/output 1
					ADC3 — ADC input 3
					RFTX — radio transmitter control input
					PC0 — pulse counter 0 input
					ADE — antenna diversity even output
DIO2	18	IO	DIO2 (I)	pull-up	**DIO2 —** digital input/output 2
					ADC5 — ADC input 5
					SDA — I^2C-bus master/slave SDA input/output (push-pull output)
					RXD1 — UART 1 receive data input
					TIM0CAP — Timer0 capture input
					RFRX — radios receiver control output
DIO3	19	IO	DIO3 (I)	pull-down	**DIO3 —** digital input/output 3
					ADC2 — ADC input 2
					PWM4 — PWM4 output
					SCL — I^2C-bus master/slave SCL input/output (push-pull output)
					TXD1 — UART 1 transmit data output
					TIM0OUT — Timer0 output
					RFTX — radio transmit control input
					FLICK_CTRL — flicker control output
V_{SS}	20	G			**V_{SS} —** ground
DIO4	21	IO (open-drain)	DIO4 (I)	pull-up	**DIO4 —** digital input/output 4
					SCL — I^2C-bus master/slave SCL input/output (open-drain)
					RXD0 — UART 0 receive data input
					TIM0CK_GT — Timer0 clock/gate input
					ADO — antenna diversity odd output

Table 2. Pin description *…continued*

Symbol	Pin	Type[1]	Default at reset/ during boot	Default internal pull-up/pull-down	Description
DIO5	22	IO (open-drain)	DIO5 (I)	pull-up	**DIO5 —** digital input/output 5
					SDA — I²C-bus master/slave SDA input/output (open-drain)
					TXD0 — UART 0 transmit data output
					PC1 — pulse counter 1 input
					TIM0CAP — Timer0 capture input
					ADE — antenna diversity even output
DO0[2]	23	O	SPICLK (O)	pull-up	**DO0 —** digital output 0
					SPICLK — SPI-bus master clock output
					ADE — antenna diversity even output
DO1[3]	24	IO	SPIMISO (I)	pull-up	**DO1 —** digital output 1
					SPIMISO — SPI-bus master data input
					SPISMISO — SPI-bus slave data output
					ADO — antenna diversity odd output
DIO6[4]	25	IO	SPISEL0 (O)	pull-up	**DIO6 —** digital input/output 6
					SPISEL0 — SPI-bus master select output 0
					CTS0 — UART 0 clear to send input
					RXD1 — UART 1 receive data input
					JTAG_TCK — JTAG TCK input
					SWCK — Serial Wire Debugger Clock input
					SPISCLK — SPI-bus slave clock input
					TIM1CAP — Timer1 capture input
DIO7[5]	26	IO	SPIMOSI (O)	pull-down	**DIO7 —** digital input/output 7
					SPIMOSI — SPI-bus master data output
					JTAG_TDI — JTAG TDI data input
					SPISEL2 — SPI-bus master select output 2
					SPISSEL — SPI-bus slave select input
					CMP_OUT — comparator output
					32KIN — 32 kHz External clock input
					32KXTALOUT — 32 kHz clock output
DIO8	27	IO	DIO8 (I)	pull-down	**DIO8 —** digital input/output 8
					PWM5 — PWM5 output
					TIM0OUT — Timer0 output
					TRACECLK — trace clock output
					32KXTALIN — 32 kHz clock input

Table 2. Pin description *…continued*

Symbol	Pin	Type[1]	Default at reset/ during boot	Default internal pull-up/pull-down	Description
DIO9	28	IO	JTAG_TDO (O)/ TXD0 (O)	pull-up	**DIO9 —** digital input/output 9
					JTAG_TDO — JTAG TDO data output
					TXD0 — UART 0 transmit data output
					TRACESWV — ARM trace serial wire viewer output
DIO10	29	IO	JTAG_TDI (I)/ RXD0 (I)	pull-up	**DIO10 —** digital input/output 10
					JTAG_TDI — JTAG TDI data input
					RXD0 — UART 0 receive data input
V_{DDD}	30	P			**V_{DDD} —** digital supply voltage
i.c.	31	-			internally connected
n.c.	32	-			not connected
V_{SS}	33	G			**V_{SS} —** ground
n.c.	34	-			not connected
VB_DIG	35	P; 1.8 V			**VB_DIG —** regulated supply voltage
DIO11	36	IO	SWD (I)	pull-up	**DIO11 —** digital input/output 11
					JTAG_TMS — JTAG TMS input
					SWD — serial wire debugger input
					RTS0 — UART 0 request to send output
					TXD1 — UART 1 transmit data output
					SPICLK — SPI-bus master clock output
					SPISMOSI — SPI-bus slave data input
					TIM1OUT — Timer1 output
					TRACED0 — ARM trace data0 output
DIO12	37	IO	DIO12 (I)	pull-down	**DIO12 —** digital input/output 12
					PWM1 — PWM1 output
					TXD0 — UART 0 transmit data output
					TRACED3 — ARM trace data3 output
DIO13	38	IO	DIO13 (I)	pull-down	**DIO13 —** digital input/output 13
					PWM2 — PWM2 output
					RXD0 — UART 0 receive data input
					PC0 — pulse counter 0 input
					TRACED2 — ARM trace data2 output
V_{SS}	39	G			**V_{SS} —** ground
DIO14	40	IO	DIO14 (I)	pull-down	**DIO14 —** digital input/output 14
					PWM3 — PWM3 output
					PC1 — pulse counter 1 input
					CMP_OUT — comparator output
					TRACED1 — ARM trace data1 output
					SPISMOSI — SPI-bus slave data input
V_{SSA}	-	G	-	-	**V_{SSA} —** Exposed die paddle

[1] P = power supply; G = ground; I = input, O = output; IO = input/output.

[2] JTAG programming mode: must be left floating high during reset to avoid entering JTAG programming mode.

[3] UART programming mode: leave pin floating high during reset to avoid entering UART programming mode or hold it low to program.

[4] Specific precautions have to be followed for UART flow control: CTS0 is not usable in the same time with SPISEL0.

[5] Specific precautions have to be followed if external 32 kHz crystal is used. SPI-bus Flash can not be used in the same time than external 32 kHz crystal.

8.2.1 Power supplies

The V_{DDA} and V_{DDD} pins are decoupled with a 100 nF ceramic capacitor. V_{DDA} is the power supply to the analog circuitry; it should be decoupled to ground. V_{DDD} is the power supply for the digital circuitry; and should also be decoupled to ground. In addition, a common 10 μF tantalum capacitor is required to filter out low frequencies noise on the power supply pins. Decoupling pins for the internal 1.8 V regulators are provided which each requires a100 nF capacitor located as close to the device as practical. VB_SYNTH and VB_DIG require only a 100 nF capacitor. VB_RF1 and VB_RF2 should be connected together as close to the device as practical, and require one 100 nF capacitor and one 47 pF capacitor. The pin VB_VCO requires a 10 nF capacitor. Refer to Figure 55 for the schematic diagram.

V_{SSA} and V_{SS} are the ground pins.

Users are strongly discouraged from connecting their own circuits to the 1.8 V regulated supply pins, as the regulators have been optimized to supply only enough current for the internal circuits.

Rising V_{DD} voltage at power-up has to be done within 100 ms with a minimum I_{DD} current of 20 mA to avoid any start up issue.

8.2.2 Reset

RESET_N is an active low reset input pin that is connected to an internal pull-up resistor see Table 19. It may be pulled low by an external circuit. Refer to Section 9.5.2 for more details.

8.2.3 32 MHz oscillator

A crystal is connected between XTAL_IN and XTAL_OUT to form the reference oscillator, which drives the system clock. A capacitor to analog ground is required on each of these pins. Refer to Section 9.4.1 for more details. The 32 MHz reference frequency is divided down to 16 MHz and this is used as the system clock throughout the device.

8.2.4 Radio

The radio is a single ended design, requiring only a capacitor and just 2 inductors to match a 50 Ω microstrip line to the RF_IO pin. In addition, extra-components are added on the line for filtering purpose.

An external resistor (43 kΩ) is required between IBIAS and analog ground (paddle) to set various bias currents and references within the radio.

8.2.5 Analog peripherals

The ADC requires a reference voltage to use as part of its operation. It can use either an internal reference voltage or an external reference connected to VREF. This voltage is referenced to analog ground and the performance of the analog peripherals is dependent on the quality of this reference.

There are 6 ADC inputs and a pair of comparator inputs. ADC0 has a designated input pin but ADC1 uses the same pin as VREF, invalidating its use as an ADC pin when an external reference voltage is required. The remaining 4 ADC channels are shared with the digital IOs DIO0, DIO1, DIO2 and DIO3. When these 4 ADC channels are selected, the corresponding DIOs must be configured as inputs with their pull-ups disabled. Similarly, the comparator shares pins 2 and 3 with DIO17 and DIO18, so when the comparator is selected these pins must be configured as inputs with their pull-ups disabled. The analog IO pins on the JN517x can have signals applied up to 0.3 V higher than V_{DDA}. A schematic view of the analog IO cell is shown in Figure 4. Figure 5 demonstrates a special case, where a digital IO pin doubles as an input to analog devices. This applies to ADC2, ADC3, ADC4, ADC5, COMP1P and COMP1M.

In reset, sleep and deep sleep, the analog peripherals are all OFF. In sleep, the comparator may optionally be used as a wake-up source.

On platform with higher power (e.g. light Bulb, Smart Plug), unused ADC and comparator inputs should not be left unconnected, but connected to analog ground.

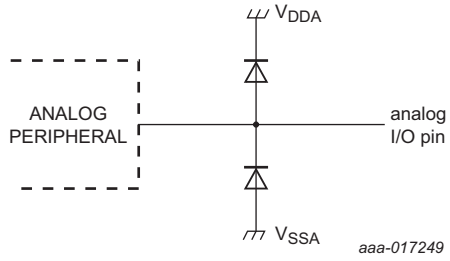


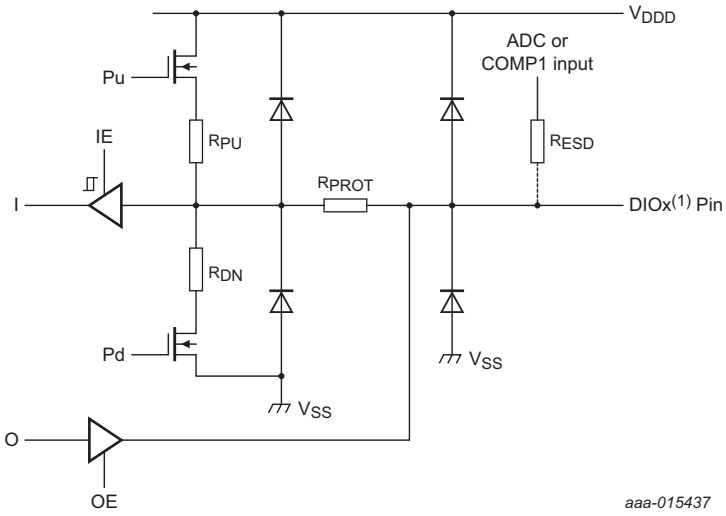
Fig 4. Analog IO cell

8.2.6 Digital Input Output (DIO)

When used in their primary function, all DIO pins are bidirectional and are connected to weak internal pull-up or pull-down resistors (50 kΩ nominal) that can be disabled. When used in their secondary function (selected when the appropriate peripheral block is enabled through software library calls), their direction is fixed by the function. The pull-up or pull-down resistor is enabled or disabled independently of the function and direction; the default state from reset is enabled.

A schematic view of the DIO cell is in Figure 5. The dotted lines through resistor R_{ESD} represent a path that exists only on DIO0, DIO1, DIO2, DIO3, DIO17 and DIO18 which are also inputs to the ADC (ADC2, ADC3, ADC4, ADC5) and comparator (COMP1P, COMP1M) respectively. To use these DIO pins for their analog functions, the DIO must be set as an input with its pull-up resistor, R_{PU}, disabled.

The DIO4 and DIO5 are different from other DIOs, as these have DIO and I^2C-bus mode. In I^2C-bus mode, DIO4 and DIO5 are true open-drain with “in-built” glitch filter enabled. A schematic view of DIO4 and DIO5 cells is shown in Figure 6.



(1) With x = 0, 1, 2, 3, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 17 or 18.

Fig 5. DIO (other than DIO4 and DIO5) pin equivalent schematic

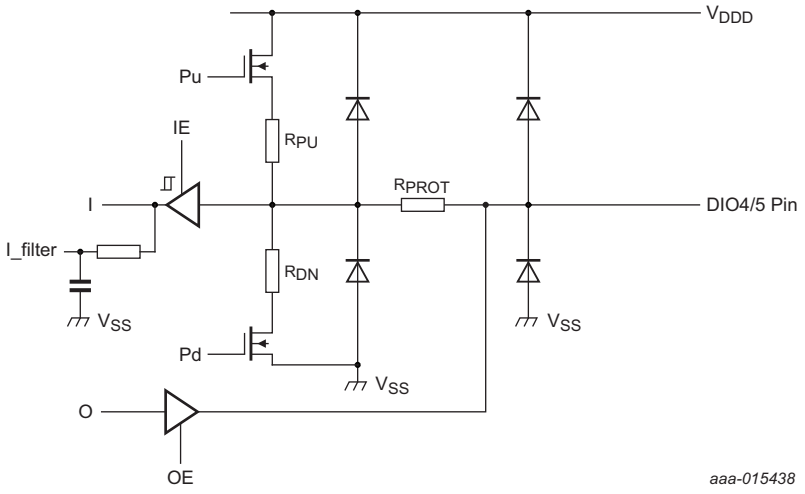


Fig 6. DIO4 and DIO5 pin equivalent schematic

In reset, the digital peripherals are all OFF and the DIO pins are set as high-impedance inputs. During sleep and deep sleep, the DIO pins retain both their input/output state and output level that was set as sleep commences. If the DIO pins were enabled as inputs and the interrupts were enabled, then these pins may be used to wake up the JN517x from sleep or deep sleep.

9. Functional description

9.1 CPU

The ARM Cortex-M3 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption. The ARM Cortex-M3 offers many new features, including a Thumb-2 instruction set, low interrupt latency, hardware divide, interruptible/continuable multiple load and store instructions, automatic state save and restore for interrupts, tightly integrated interrupt controller with wake-up interrupt controller, and multiple core buses capable of simultaneous accesses.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM Cortex-M3 includes three AHB-Lite buses: the system bus, the I-CODE bus, and the D-CODE bus. The I-CODE and D-CODE core buses are faster than the system bus and are used similarly to TCM interfaces: one bus dedicated for instruction fetch (I-CODE) and one bus for data access (D-CODE). The use of 2 core buses allows for simultaneous operations if concurrent operations target different devices.

The JN517x uses a multi-layer AHB matrix to connect the ARM Cortex-M3 buses and other bus masters to peripherals in a flexible manner that optimizes performance by allowing peripherals that are on different slaves ports of the matrix to be accessed simultaneously by different bus masters.

The ARM Cortex-M3 processor is described in detail in the Cortex-M3 Technical Reference Manual that can be found on the official ARM website.

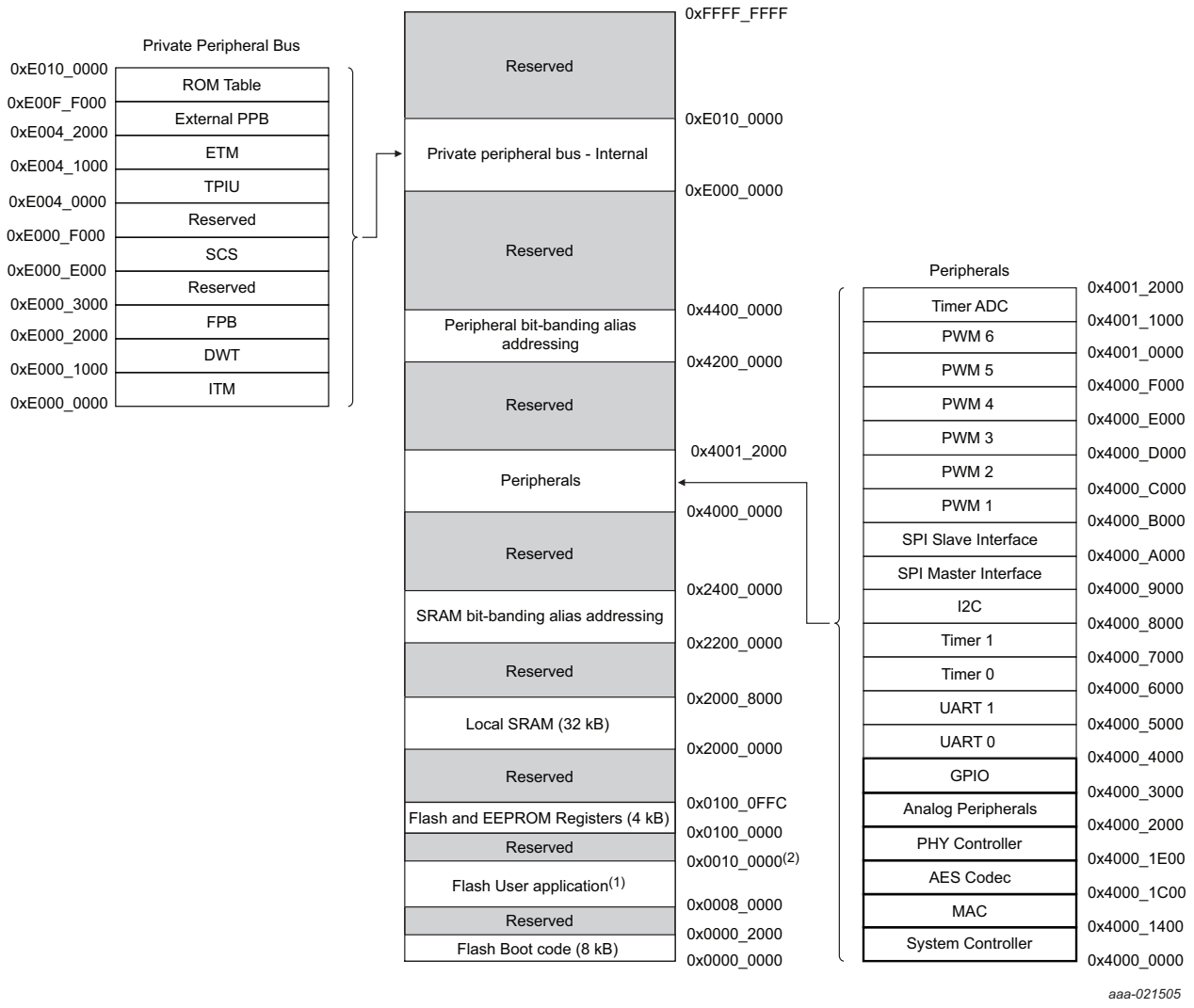
To improve power consumption a number of power-saving modes are implemented in the JN517x, described more fully in Section 10. One of these modes is the CPU doze mode; under software control, the processor can be shut down and on receiving an interrupt it will wake up to service the request. Additionally, it is possible under software control, to set the speed of the CPU to 1 MHz, 2 MHz, 4 MHz, 8 MHz, 16 MHz or 32 MHz. This feature can be used to trade off processing power against current consumption.

9.2 Emulation and debugging

Debug and trace functions are integrated into the ARM Cortex-M3. Serial wire debug and trace functions are supported in addition to a standard JTAG debug and parallel trace functions. The ARM Cortex-M3 is configured to support up to 8 breakpoints and 4 watch points.

9.3 Memory organization

This section describes the different memories found within the JN517x. The device contains Flash, RAM, and EEPROM memory, the wireless transceiver and peripherals registers all within the same linear address space.



(1) JN5174: 160 kB, JN5178: 256 kB and JN5179: 512 kB.

(2) JN5174: 0x000A_8000, JN5178: 0x000C_0000 and JN5179: 0x0010_0000.

Fig 7. JN517x memory map

9.3.1 Flash

The embedded Flash consists of 2 parts: an 8 kB region used for holding boot code, and a 160 kB or 256 kB or 512 kB region used for application code. The sector size of the application code is always 32 kB, for any size of Flash memory. The guaranteed endurance of the memory is 10,000 write cycles with typical endurance of 100,000 cycles, while the data retention is guaranteed for at least 10 years. The boot code region is pre-programmed by NXP on supplied parts, and contains code to handle reset, interrupts and other events (see section Section 9.6). It also contains a Flash Programming Interface to allow interaction with the PC-based Flash Programming Utility which allows user code compiled using the supplied SDK to be programmed into the application space. The memory can be erased by a single or multiple sectors and written to in units of 256 bytes, known as pagewords. For further information, refer to Flash Programmer User Guide JN-UG-3099 on the Wireless Connectivity area of the NXP web site Ref. 2.

9.3.2 RAM

The JN517x devices contain 32 kB of high-speed RAM. It is primarily used to hold the CPU Stack together with program variables and data. If necessary, the CPU can execute code contained within the RAM (although it would normally just execute code directly from the embedded Flash). Software can control the power supply to the RAM allowing the contents to be maintained during a sleep period when other parts of the device are unpowered, allowing a quicker resumption of processing once woken.

9.3.3 OTP configuration memory

The JN517x contains a quantity of One Time Programmable (OTP) memory as part of the embedded Flash (Index Sector). This can be used to securely hold such things as a user 64-bit MAC address and a 128-bit AES security key. By default the 64-bit MAC address is pre-programmed by NXP on supplied parts; however the pre-programmed value can be overridden by customers providing their own MAC addresses. The user MAC address and other data can be written to the OTP memory using the Flash programmer. Details on how to obtain and install MAC addresses can be found in the dedicated Application Note. In addition, 128 bits are available for customer use for storage of configuration or other information.

For further information on how to program and use this facility, refer to Flash Programmer User Guide JN-UG-3099 on the Wireless Connectivity area of the NXP web site Ref. 2.

9.3.4 EEPROM

The JN517x contains 4 kB of EEPROM. The guaranteed endurance of the memory is 100 000 write cycles with typical endurance of 1 million cycles, while the data retention is guaranteed for at least 10 years. EEPROM endurance can be extended using the Persistent Data Manager software which wear levels the EEPROM as data is written to it. This is supplied in the NXP ZigBee SDK.

This non-volatile memory is primarily used to hold persistent data generated from such things as the Network Stack software component (for example network topology, routing tables). As the EEPROM holds its contents through sleep and reset events, this means more stable operation and faster recovery is possible after outages.

The memory can be erased by a single or multiple pages of 64 bytes. It can be written to in single or multiple bytes up to 64 bytes. For further details, refer to the JN517x Integrated Peripherals API User Guide JN-UG-3118 on the Wireless Connectivity area of the NXP web site Ref. 2.

9.3.5 External memory

An optional external serial non-volatile memory (for instance Flash or EEPROM) with a SPI-bus interface may be used to provide additional storage for program code, such as a new code image or further data for the device when external power is removed. The memory can be connected to the SPI-bus master interface using select line SPISEL0 (see Figure 8 for details).

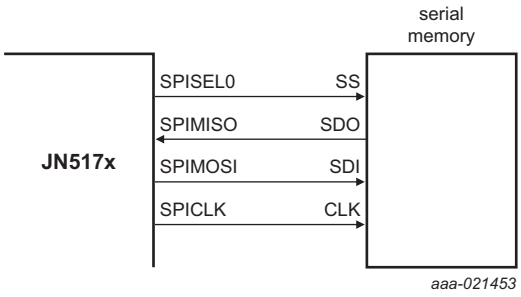


Fig 8. Connecting external serial memory

The contents of the external serial memory may be encrypted. The AES security processor combined with a user programmable 128-bit encryption key is used to encrypt the contents of the external memory. The encryption key is stored in the Flash memory index section. When bootloading program code from external serial memory, the JN517x automatically accesses the encryption key to execute the decryption process, which is transparent to the user, user program code does not need to handle any part of the decryption process; it is transparent. For more details, including the how the program code encrypts data for the external memory, refer to Application Note Boot loader Operation JN-AN-1003 on the Wireless Connectivity area of the NXP web site Ref. 2.

Remark: SPI-bus Flash can not be used in the same time than external 32 kHz crystal.

9.3.6 Peripherals

All peripherals have their registers mapped into the memory space. Applications have access to the peripherals through the software libraries that present a high-level view of the peripheral's functions through a series of dedicated software routines. These routines provide both a tested method for using the peripherals and allow bug-free application code to be developed more rapidly. For details, see JN517x Integrated Peripherals API User Guide JN-UG-3118 on the Wireless Connectivity area of the NXP web site Ref. 2.

9.4 System clocks

Two system clocks are used to drive the on-chip subsystems of the JN517x. The wake-up timers are driven from a low frequency clock (notionally 32 kHz). All other subsystems (transceiver, processor, memory and digital and analog peripherals) are driven by a high-speed clock (notionally 32 MHz), or a divided-down version of it.

The high-speed clock is either generated by the accurate crystal-controlled oscillator (32 MHz) or the less accurate high-speed RC oscillator (27 MHz to 32 MHz calibrated). The low-speed clock is either generated by the less accurate RC oscillator (centered on 32 kHz) or can be supplied externally.

9.4.1 High-speed (32 MHz) system clock

The selected high-speed system clock is used directly by the radio subsystem, whereas a divided-by-two version is used by the remainder of the transceiver and the digital and analog peripherals. The direct or divided down version of the clock is used to drive the processor and memories (32 MHz, 16 MHz, 8 MHz, 4 MHz, 2 MHz or 1 MHz).

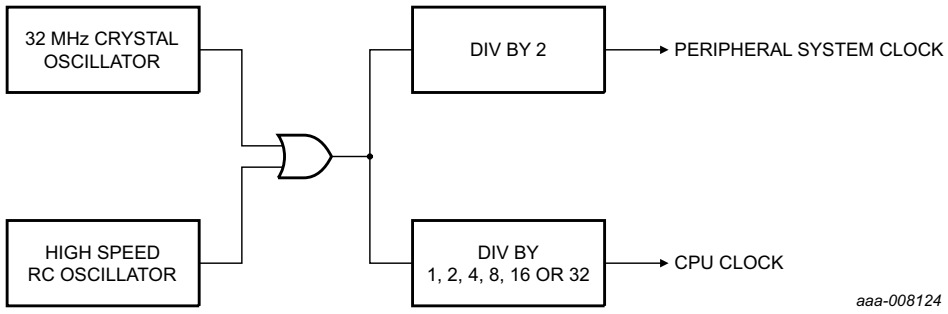


Fig 9. System and CPU clocks

Crystal oscillators are generally slow to start. Hence to provide a fast start-up following a sleep cycle or reset, the fast RC oscillator is always used as the initial source for the high-speed system clock. The oscillator starts very quickly and will run at 25 MHz to 32 MHz (uncalibrated) or 32 MHz ±5 % (calibrated). Although this means that the system clock will be running at an undefined frequency (slightly slower or faster than nominal), this does not prevent the CPU and memory subsystems operating normally, so the program code can execute. However, it is not possible to use the radio or UARTs, as even after calibration (initiated by the user software calling an API function) there is still a ±5 % tolerance in the clock rate over voltage and temperature. Other digital peripherals can be used (eg SPI-bus master/slave), but care must be taken if using Timers due to the clock frequency inaccuracy.

Further details of the high-speed RC oscillator can be found in Section 14.3.9

On wake-up from sleep, the JN517x uses the fast RC oscillator. It can then either:

- Automatically switch over to use the 32 MHz clock source when it has started up
- Continue to use the fast RC oscillator until software triggers the switch-over to the 32 MHz clock source, for example when the radio is required
- Continue to use the RC oscillator until the device goes back into one of the sleep modes

The use of the fast RC Oscillator at wake-up means that there is no need to wait for the 32 MHz crystal oscillator to stabilize.

9.4.1.1 32 MHz crystal oscillator

The JN517x contains the necessary on chip components to build a 32 MHz reference oscillator with the addition of an external crystal resonator and 2 tuning capacitors. The schematics of these components are shown in Figure 10. The 2 capacitors, C1 and C2, should typically be 12 pF and use a COG dielectric. Due to the small size of these capacitors, it is important to keep the traces to the external components as short as possible. The on-chip transconductance amplifier is compensated for temperature variation, and is self-biasing by means of the internal resistor R1. This oscillator provides the frequency reference for the radio and therefore the reference PCB layout and BOM must be carefully followed. Refer to Section 14.3.11 for development support with the crystal oscillator circuit. The oscillator includes a function which flags when the amplitude of oscillation has reached a satisfactory level for full operation, and this is checked before the source of the high-speed system clock is changed to the 32 MHz crystal oscillator.

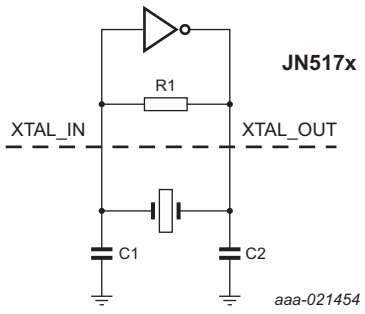


Fig 10. 32 MHz crystal oscillator connections

For operation over the extended temperature range, 85 °C to 125 °C, special care is required; this is because the temperature characteristics of crystal resonators are generally in excess of ±40 ppm frequency tolerance defined by the IEEE802.15.4 standard. The oscillator cell contains additional circuitry to compensate for the poor performance of the crystal resonators above 100 °C. Full details, including the software API function, can be found in the Temperature Dependent Operating Guidelines JN-AN-1186 on the Wireless Connectivity area of the NXP web site Ref. 2.

9.4.1.2 High-speed RC oscillator

An on-chip high-speed RC oscillator is provided in addition to the 32 MHz crystal oscillator for 2 purposes, to allow a fast start-up from reset or sleep and to provide a lower current alternative to the crystal oscillator for non-timing critical applications. By default the oscillator will run at 27 MHz typically with a wide tolerance. It can be calibrated, using a software API function, which will result in a nominal frequency of 32 MHz with a ±1.6 % tolerance at 3 V and 25 °C. However, it should be noted that over the full operating range of voltage and temperature this will increase to ±5%. The calibration information is retained through speed cycles and when the oscillator is disabled, so typically the calibration function only needs to be called once. No external components are required for this oscillator. The electrical specification of the oscillator can be found in Section 14.3.9.

9.4.2 Low-speed (32 kHz) system clock

The 32 kHz system clock is used for timing the length of a sleep period (see Section 10. The clock can be selected from one of 2 sources through the application software:

- 32 kHz RC oscillator
- 32 kHz external clock
- 32 kHz crystal oscillator

Upon a chip reset or power-up, the JN517x defaults to using the internal 32 kHz RC oscillator. If another clock source is selected, then, it will remain in use for all 32 kHz timing until a chip reset is performed.

9.4.2.1 32 kHz RC oscillator

The internal 32 kHz RC oscillator requires no external components. The internal timing components of the oscillator have a wide tolerance due to manufacturing process variation and so the oscillator runs nominally at 32 kHz −20.7 %/+52.6 %. To make this useful as a timing source for accurate wake-up from sleep, a frequency calibration factor derived from the more accurate 16 MHz peripheral system clock may be applied. The

calibration factor is derived through software, details can be found in Section 9.10.3.1. Software must check that the 32 kHz RC oscillator is running before using it. The oscillator has a default current consumption of around 0.5 μA. Optionally, this can be reduced to 0.375 μA, however, the calibrated accuracy and temperature coefficient will be worse as a consequence. For detailed electrical specifications, see Section 14.3.9.

9.4.2.2 32 kHz External clock

An externally supplied 32 kHz reference clock on the 32KIN input (DIO7) may be provided to the JN517x. This would allow the 32 kHz system clock to be sourced from a very stable external oscillator module, allowing more accurate sleep cycle timings compared to the internal RC oscillator. SPI-bus Flash can not be used in the same time than external 32 kHz crystal.

9.4.2.3 32 kHz crystal oscillator

In order to obtain more accurate sleep periods, the JN517x contains the necessary on-chip components to build a 32 kHz oscillator with the addition of an external 32.768 kHz crystal and two tuning capacitors. The crystal should be connected between 32KXTALIN and 32KXTALOUT (DIO8 and DIO7), with two equal capacitors to ground, one on each pin. Due to the small size of the capacitors, it is important to keep the traces to the external components as short as possible.

The electrical specification of the oscillator can be found in Section 14.3.10. The oscillator cell is flexible and can operate with a range of commonly available 32.768 kHz crystals with load capacitances from 6 pF to 12.5 pF. However, the maximum ESR of the crystal and the supply current are both functions of the actual crystal used.

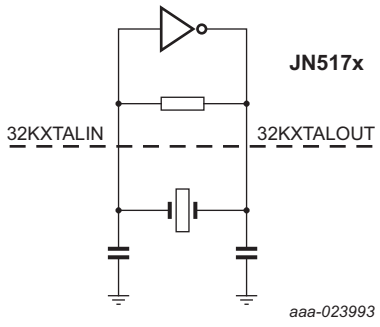


Fig 11. 32 kHz crystal oscillator connections

9.5 Reset

A system reset initializes the device to a pre-defined state and forces the CPU to start program execution from the reset vector. The reset process that the JN517x goes through is as follows.

When power is first applied (on V_{DDA} and V_{DDD} supply pins) or when the external reset is released, the high-speed RC oscillator and 32 MHz crystal oscillator are activated. After a short wait period (approximately 13 μs) while the high-speed RC starts up, and so long as the supply voltage satisfies the default SVM threshold (2.0 V + 0.045 V hysteresis), the internal 1.8 V regulators are turned on to power the processor and peripheral logic. The regulators are allowed to stabilize (about 15 μs) followed by a further wait (approximately

150 μs) to allow the Flash and EEPROM bandgaps to stabilize and allow their initialization, including reading the user SVM threshold from the Flash. This is applied to the SVM, and after a brief pause (approximately 2.5 μs) the SVM is checked again. If the supply is above the new SVM threshold, the CPU and peripheral logic is released from reset and the CPU starts to run code beginning at the reset vector. This runs the bootloader code contained within the Flash, which looks for a valid application to run, first from the internal Flash and then from any connected external serial memory over the SPI-bus master interface. Once found, required variables are initialized in RAM before the application is called at its AppColdStart entry point. For more details on the bootloader, refer to Application Note Boot loader Operation JN-AN-1003 on the Wireless Connectivity area of the NXP web site Ref. 2.

The JN517x has 5 sources of reset:

- Internal Power-On Reset/Brown-Out Reset (BOR)
- External reset
- Software reset
- Watchdog timer
- Supply voltage detect

Remark: When the device exits a reset condition, device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, then the device must be held in reset until the operating conditions are met (see Section 14.3.1).

9.5.1 Internal Power-On Reset/Brown-out Reset (BOR)

For most applications, the Internal POR is capable of generating the required reset signal. When power is applied to the device, the power-on reset circuit monitors the rise of the V_{DD} (V_{DDA} and V_{DDD}) supply. When the V_{DD} reaches the specified threshold, the reset signal is generated. This signal is held internally until the power supply and oscillator stabilization time has elapsed, when the internal reset signal is then removed and the CPU is allowed to run.

The BOR circuit has the ability to reject spikes on the V_{DD} rail to avoid false triggering of the reset module. Typically for a negative going square pulse of duration 1 μs, the voltage must fall to 1.2 V before a reset is generated. Similarly for a triangular wave pulse of 10 μs width, the voltage must fall to 1.3 V before causing a reset. The exact characteristics are complex and these are only examples. See Figure 47 for more details on BOR and SVM characteristics.

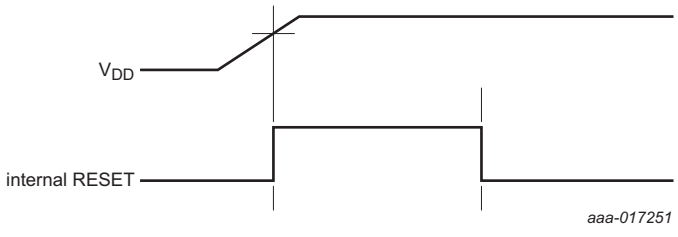


Fig 12. Internal Power-On Reset

When the supply drops below the POR 'falling' threshold, it will retrigger the reset. On platform with higher power (e.g. light bulb, smart plug) it is recommended to use this external circuit to avoid unexpected reset due to spurs.

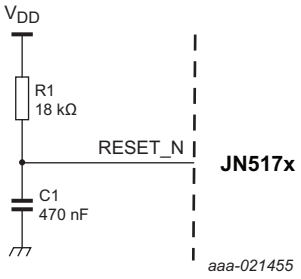


Fig 13. External reset generation

9.5.2 External reset

An external reset is generated by a low level on the RESET_N pin. Reset pulses longer than the minimum pulse width will generate a reset during active or sleep modes. Shorter pulses are not guaranteed to generate a reset. The JN517x is held in reset while the RESET_N pin is low. When the applied signal reaches the reset threshold voltage (V_{rst}) on its positive edge, the internal reset process starts.

The JN517x has an internal pull-up resistor (see Table 19) connect to the RESET_N pin. The pin is an input for an external reset only. By holding the RESET_N pin low, the JN517x is held in reset, resulting in a typical current of 6 μA.

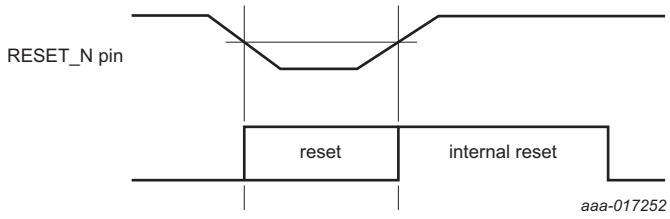


Fig 14. External reset

9.5.3 Software reset

A system reset can be triggered at any time through software control, causing a full chip reset and invalidating the RAM contents. For example, this can be executed within a user's application upon detection of a system failure.

9.5.4 Supply Voltage Monitor

An internal SVM is used to monitor the supply voltage to the JN517x; this can be used while the device is awake or is in CPU doze mode. Dips in the supply voltage below a variable threshold can be detected and can be used to cause the JN517x to perform a chip reset. Equally, dips in the supply voltage can be detected and used to cause an interrupt to the processor, when the voltage either drops below the threshold or rises above it.

The supply voltage detect is enabled by default from power-up and can extend the reset during power-up. This will keep the CPU in reset until the voltage exceeds the SVM threshold voltage. The threshold voltage is configurable to 1.95 V, 2.0 V, 2.1 V, 2.2 V, 2.3 V, 2.4 V, 2.7 V and 3.0 V and is controllable by software. From power-up, the threshold is set by a setting within the Flash and the default chip configuration is for the 2.0 V threshold. It is expected that the threshold is set to the minimum needed by the system. See Figure 47 for more details on BOR and SVM characteristics.

9.5.5 Watchdog timer

A watchdog timer is provided to guard against software lockups. It operates by counting cycles of the high-speed RC system clock. A pre-scaler is provided to allow the expiry period to be set between typically 8 ms and 16.4 s (dependent on high-speed RC accuracy: +30 %, −15 %). Failure to restart the watchdog timer within the pre-configured timer period will cause a chip reset to be performed. A status bit is set if the watchdog was triggered so that the software can differentiate watchdog initiated resets from other resets, and can perform any required recovery once it restarts. Optionally, the watchdog can cause an exception rather than a reset, this preserves the state of the memory and is useful for debugging.

After power-up, reset, start from deep sleep or start from sleep, the watchdog is always enabled with the largest time-out period and will commence counting as if it had just been restarted. Under software control, the watchdog can be disabled. If it is enabled, the user must regularly restart the watchdog timer to stop it from expiring and causing a reset. The watchdog runs continuously, even during doze, however the watchdog does not operate during sleep or deep sleep, or when the hardware debugger has taken control of the CPU. It will recommence automatically if enabled once the debugger unstalls the CPU.

9.6 Nested Vector Interrupt controller (NVIC)

The NVIC is an integral part of the Cortex-M3. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late-arriving interrupts. The main features of the interrupt controller are:

- Controls the system exceptions and peripheral interrupts
- Supports 20 vectored interrupts
- 16 programmable interrupt priority levels

Interrupts can be used to wake the JN517x from sleep or deep sleep. The peripherals, baseband controller, security coprocessor and NVIC are powered down during sleep or deep sleep but the DIO interrupts and optionally the pulse counters, wake-up timers and analog comparator interrupts remain powered to bring the JN517x out of sleep.

The Cortex-M3 incorporates a mechanism that allows remapping the interrupt vector table to alternate locations in the memory map. This is controlled via the Vector Table Offset Register (VTOR) contained in the Cortex-M3. The NVIC is described in detail in the Cortex-M3 Technical Reference Manual that can be found on official ARM website.

9.6.1 Interrupts sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Table 3 lists the interrupt sources for each peripheral function. Exception numbers relate to where entries are stored in the exception vector table. Interrupt numbers are used in some other contexts, such as software interrupts.

Table 3. Interrupt sources

Interrupt ID	Exception number	Vector offset (h)	Function
0	16	0x40	PWM1
1	17	0x44	PWM2
2	18	0x48	PWM3
3	19	0x4C	PWM4
4	20	0x50	PWM5
5	21	0x54	PWM6
6	22	0x58	system controller
7	23	0x5C	MAC
8	24	0x60	AES codec
9	25	0x64	PHY controller
10	26	0x68	UART0
11	27	0x6C	UART1
12	28	0x70	SPI-bus slave
13	29	0x74	SPI-bus master
14	30	0x78	I^2C-bus master/slave
15	31	0x7C	Timer0
16	32	0x80	Timer1
17	33	0x84	timer ADC
18	34	0x88	analog peripheral
19	35	0x8C	watchdog interrupt

9.7 Wireless transceiver

The wireless transceiver comprises a 2.45 GHz radio, modem, a baseband processor, a security coprocessor and PHY controller. These blocks, with protocol software provided as a library, implement an IEEE802.15.4 standards-based wireless transceiver that transmits and receives data OTA in the unlicensed 2.4 GHz band.

9.7.1 Radio

Figure 15 shows the single-ended radio architecture.

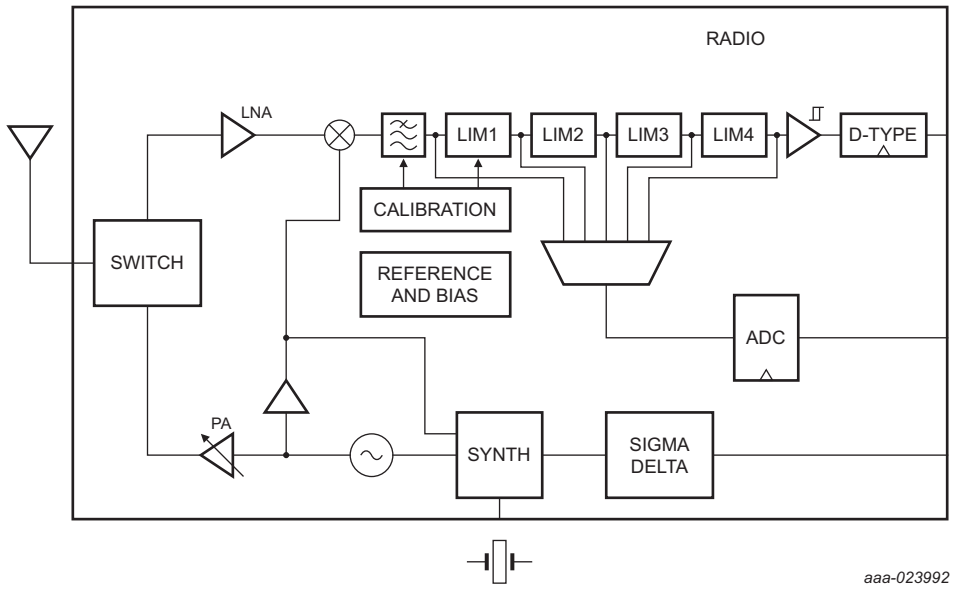


Fig 15. Radio architecture

The radio comprises a low-IF receive path and a direct modulation transmit path, which converge at the TX/RX switch. The switch connects to the external single ended matching network, which consists of two inductors and a capacitor; this arrangement creates a 50 Ω port and removes the need for a balun. A 50 Ω single-ended antenna can be connected directly to this port.

The 32 MHz crystal oscillator feeds a divider, which provides the frequency synthesizer with a reference frequency. The synthesizer contains programmable feedback dividers, phase detector, charge pump and internal Voltage Controlled Oscillator (VCO). The VCO has no external components, and includes calibration circuitry to compensate for differences in internal component values due to process and temperature variations. The VCO is controlled by a Phase-Locked Loop (PLL) that has an internal loop filter. A programmable charge pump is also used to tune the loop characteristic.

The receiver chain starts with the low noise amplifier/mixer combination whose outputs are passed to a low pass filter, which provides the channel definition. The signal is then passed to a series of amplifier blocks forming a limiting strip. The signal is converted to a digital signal before being passed to the Modem. The gain control for the RX path is derived in the Automatic Gain Control (AGC) block within the Modem, which samples the signal level at various points down the RX chain. To improve the performance and reduce current consumption, automatic calibration is applied to various blocks in the RX path.

In the transmit direction, the digital stream from the Modem is passed to a digital sigma-delta modulator which controls the feedback dividers in the synthesizer (dual point modulation). The VCO frequency now tracks the applied modulation. The 2.4 GHz signal from the VCO is then passed to the RF Power Amplifier (PA), whose power control can be selected from one of three settings. The output of the PA drives the antenna via the RX/TX switch

The JN517x radio when enabled is automatically calibrated for optimum performance. In operating environments with a significant variation in temperature (e.g. greater than 20 °C) due to diurnal or ambient temperature variation, it is recommended to recalibrate the radio to maintain performance. Recalibration is only required on devices that never sleep. Devices which sleep or deep sleep are automatically recalibrated when they wake. A dedicated Application Note, Temperature Dependent Operating Guidelines JN-AN-1186 on the Wireless Connectivity area of the NXP web site Ref. 2, describes this in detail and includes a software API function which can be used to test the temperature using the on-chip temperature sensor and trigger a recalibration if there has been a significant temperature change since the previous calibration.

9.7.1.1 Radio external components

In order to realize the full performance of the radio, the reference PCB layout and BOM must be followed very closely (see Section 15.1).

The radio is powered from a number of internal 1.8 V regulators fed from the analog supply V_{DDA}, in order to provide good noise isolation between the digital logic of the JN517x and the analog blocks. These regulators are also controlled by the baseband controller and protocol software to minimize power consumption. Decoupling for internal regulators is required as described in Section 8.2.1.

For single-ended antennas or connectors, a balun is not required, however a matching network is needed.

The RF matching network requires 3 external components and the IBIAS pin requires one external component as shown in Figure 55. These components are critical and should be placed close to the JN517x pins and analog ground as defined in Table 34. Specifically, the output of the network comprising L2, C1 and L1 is designed to present an accurate match to a 50 Ω resistive network as well as provide a DC path to the final output stage or antenna. Users wishing to match to other active devices such as amplifiers should design their networks to match to 50 Ω at the output of L1.

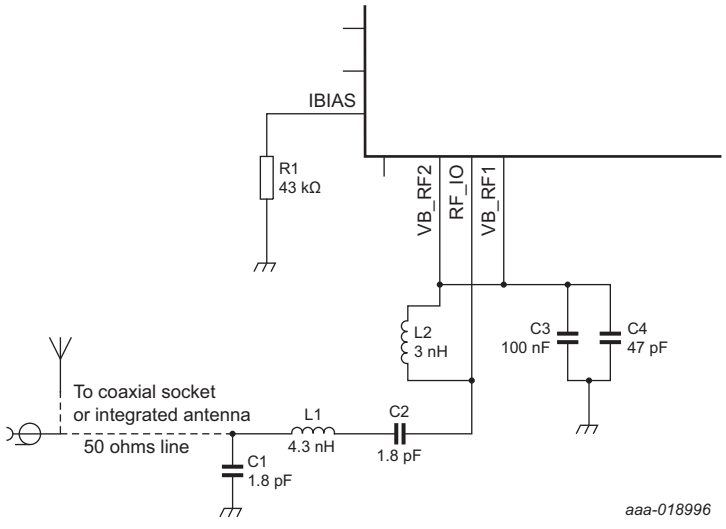


Fig 16. External radio components

9.7.1.2 Antenna diversity

Support is provided for antenna diversity, which is a technique that maximizes the performance of an antenna system. It allows the radio to switch between two antennas that have very low correlation between their received signals. Typically, this is achieved by spacing two antennae around 0.25 wavelengths apart or by using 2 orthogonal polarizations. So, if a packet is transmitted and no acknowledgement is received, the radio system can switch to the other antenna for the retry, with a different probability of success.

Additionally antenna diversity can be enabled while in receive mode waiting for a packet. The JN517x measures the received energy in the relevant radio channel every 40 μs and the measured energy level is compared with a pre-set energy threshold, which can be set by the application program. The JN517x device will automatically switch the antenna if the measurement is below this threshold, except if waiting for an acknowledgement from a previous transmission or in the process of receiving a packet, where it will wait until this has finished. Also, it will not switch if a preamble symbol having a signal quality above a minimum specified threshold has not been detected in the last 40 μs.

Both modes can be used at once and use the same ADO (SELA) and ADE (SELB) outputs to control the external switch.

The JN517x provides an output (ADO) on one of DIO0, DIO4 and DO1 that is asserted on odd-numbered retries and optionally its complement (ADE) on one of DIO1, DIO5 and DO0, that can be used to control an antenna switch; this enables antenna diversity to be implemented easily (see Figure 17 and Figure 18).

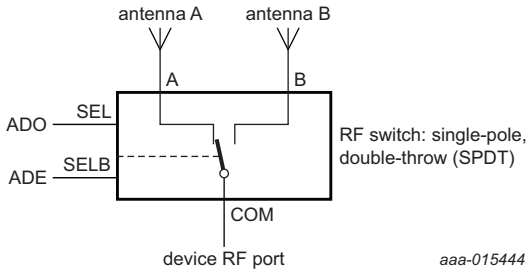


Fig 17. Simple antenna diversity implementation using external RF switch

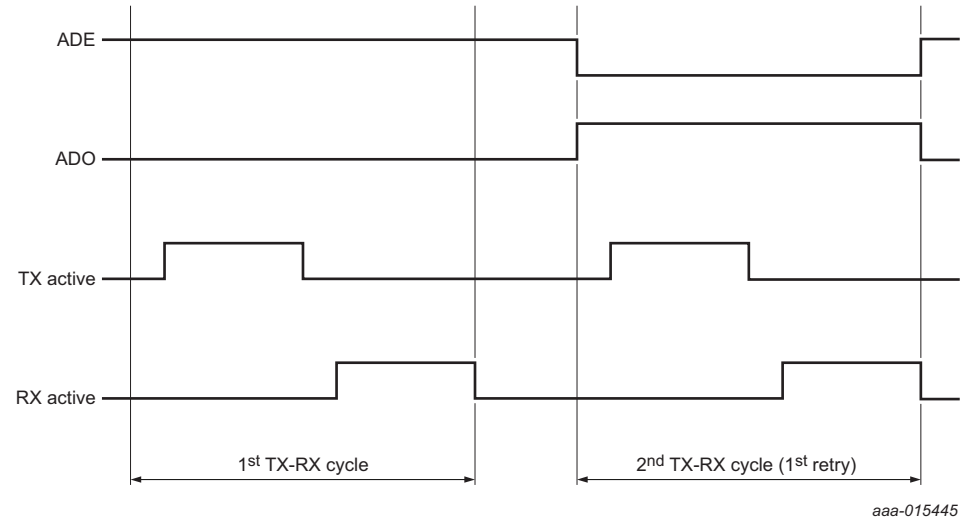


Fig 18. Antenna diversity ADO signal for TX with acknowledgement

If two DIO pins cannot be spared, one of the signals (ADE or ADO) from the JN517x can be used and its complement can be generated using an inverter on the PCB.

9.7.2 Modem

The modem performs all the necessary modulation and spreading functions required for digital transmission and reception of data at 250 kbits/s in the 2.4 GHz radio frequency band in compliance with the IEEE802.15.4 standard.

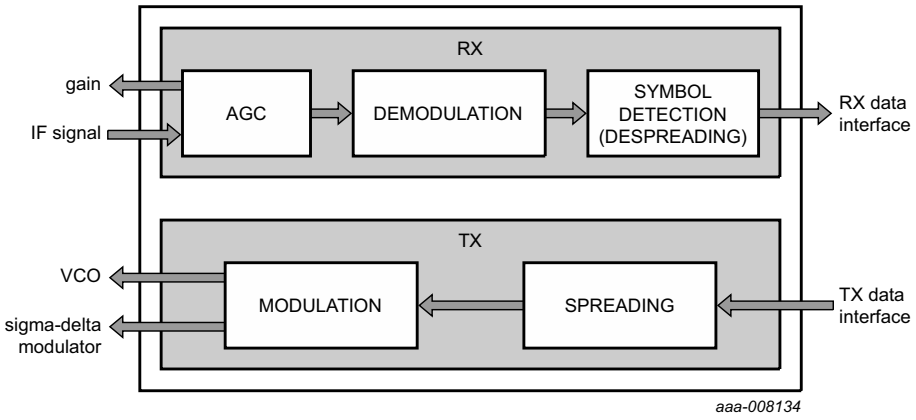


Fig 19. Modem architecture

Features provided to support network channel selection algorithms include Energy Detection (ED), Link Quality Indication (LQI) and fully programmable Clear Channel Assessment (CCA).

The modem provides a digital Receive Signal Strength Indication (RSSI) that facilitates the implementation of the IEEE802.15.4 ED and LQI functions.

The ED and LQI are both related to received power in the same way, as shown in Figure 20. LQI is associated with a received packet, whereas ED is an indication of signal power on-air at a particular moment.

The CCA capability of the modem supports all modes of operation defined in the IEEE802.15.4 standard, namely Energy above ED threshold, Carrier Sense and Carrier Sense and/or energy above ED threshold.

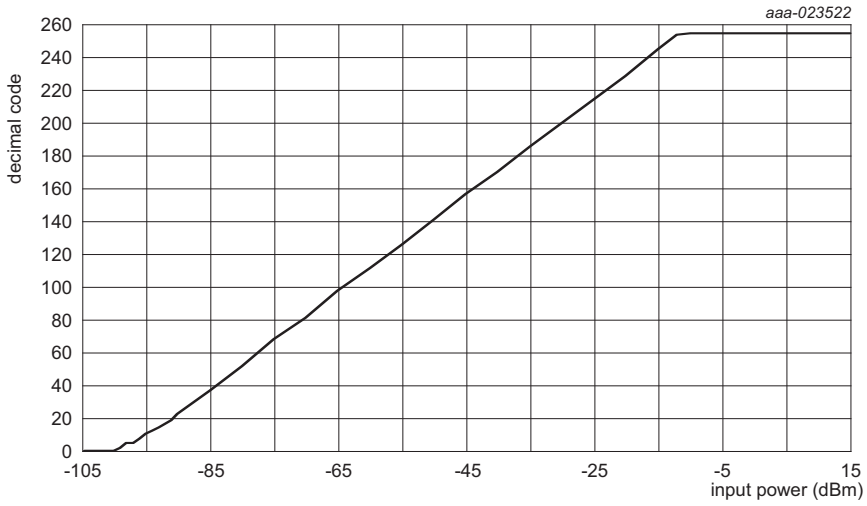


Fig 20. Energy detect value versus receive power level

9.7.3 Baseband processor

The baseband processor provides all time-critical functions of the IEEE802.15.4 MAC layer. Dedicated hardware guarantees air interface timing is precise. The MAC layer hardware/software partitioning enables software to implement the sequencing of events required by the protocol and to schedule timed events with millisecond resolution and the hardware to implement specific events with microsecond timing resolution. The protocol software layer performs the higher-layer aspects of the protocol, sending management and data messages between End Device and Co-ordinator nodes, using the services provided by the baseband processor.

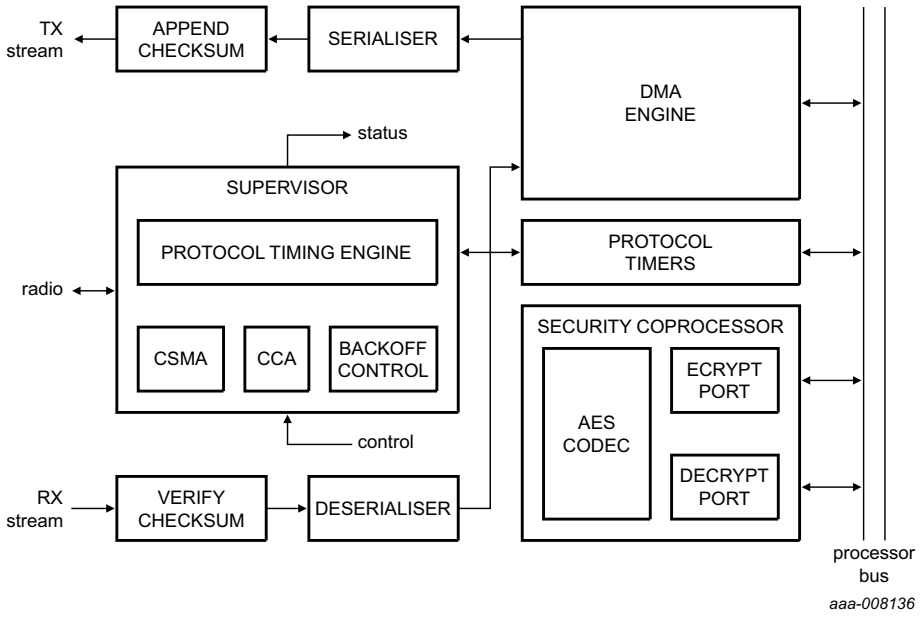


Fig 21. Baseband processor

9.7.3.1 Transmit

A transmission is performed by software writing the data to be transferred into the TX frame buffer in RAM, together with parameters such as the destination address and the number of retries allowed, as well as programming one of the protocol timers to indicate the time at which the frame is to be sent. This time will be determined by the software tracking the higher-layer aspects of the protocol such as superframe timing and slot boundaries. Once the packet is prepared and the protocol timer set, the supervisor block controls the transmission. When the scheduled time arrives, the supervisor controls the sequencing of the radio and modem to perform the type of transmission required, fetching the packet data directly from RAM. It can perform all the algorithms required by IEEE802.15.4 such as CSMA/CA without processor intervention, including retries and random back-offs.

When the transmission begins, the header of the frame is constructed from the parameters programmed by the software and sent with the frame data through the serializer to the modem. At the same time, the radio is prepared for transmission. During the passage of the bitstream to the modem, it passes through a CRC checksum generator that calculates the checksum on-the-fly, and appends it to the end of the frame.

9.7.3.2 Reception

During reception, the radio is set to receive on a particular channel. On receipt of data from the modem, the frame is directed into the receive frame buffer in RAM where both header and frame data can be read by the protocol software. An interrupt may be provided on receipt of the frame. An additional interrupt may be provided after the transmission of an acknowledgement frame in response to the received frame, if an acknowledgement frame has been requested and the auto acknowledge mechanism is enabled, see Section 9.7.3.3. As the frame data is being received from the modem, it is passed through a checksum generator; at the end of the reception the checksum result is

compared with the checksum at the end of the message to ensure that the data has been received correctly. During reception, the modem determines the Link Quality, which is made available at the end of the reception as part of the requirements of IEEE802.15.4.

9.7.3.3 Auto acknowledge

Part of the protocol allows for transmitted frames to be acknowledged by the destination sending an acknowledge packet within a very short window after the transmitted frame has been received. The JN517x baseband processor can automatically construct and send the acknowledgement packet without processor intervention and hence avoid the protocol software being involved in time-critical processing within the acknowledge sequence. The JN517x baseband processor can also request an acknowledge for packets being transmitted and handle the reception of acknowledged packets without processor intervention.

9.7.3.4 Security

The transmission and reception of secured frames using the AES algorithm is handled by the security coprocessor and the stack software. The application software must provide the appropriate encrypt/decrypt keys for the transmission or reception. On transmission, the key can be programmed at the same time as the rest of the frame data and set-up information.

9.7.4 Security coprocessor

The security coprocessor is available to the application software to perform encryption/decryption operations. A hardware implementation of the encryption engine significantly speeds up the processing of the encrypted packets over a pure software implementation. The AES library for the JN517x provides operations that utilize the encryption engine in the device and allow the contents of memory buffers to be transformed. Information such as the type of security operation to be performed and the encrypt/decrypt key to be used must also be provided.

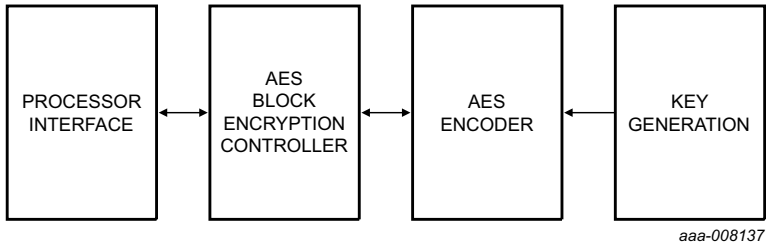


Fig 22. Security coprocessor architecture

9.8 Digital Input Output

There are 18 Digital IO (DIO) pins which when used as general-purpose pins can be configured as either an input or an output, with each having a selectable internal pull-up or pull-down resistor. In addition, there are 2 Digital Output (DO) pins.

Most DIO pins are shared with the digital and analog peripherals of the device. When a peripheral is enabled, it takes control over the device pins allocated to it. However, note that most peripherals have two alternative pin allocations to alleviate clashes between uses, and many peripherals can disable the use of specific pins if not required. Refer to

Section 8.2 and the individual peripheral descriptions for full details of the available pinout arrangements.

Following a reset (and while the RESET_N input is held low), all peripherals are forced off and the DIO pins are configured as inputs with their default internal pull-up or pull-down resistor connected. When a peripheral is not enabled, the DIO pins associated with it can be used as digital inputs or outputs. Each pin can be controlled individually by setting the direction and then reading or writing to the pin.

The individual pull-up or pull-down resistors, R_{PU} or R_{DN}, can also be enabled or disabled as needed and the setting is held through sleep or deep sleep cycles. The pull-up or pull-down resistors are generally configured once after reset depending on the external components and functionality. For instance, outputs should generally have the pull-up or pull-down resistor disconnected. An input that is always driven should also have the pull-up or pull-down resistor disconnected.

When configured as an input each pin can be used to generate an interrupt upon a change of state (selectable transition either from low to high or high to low); the interrupt can be enabled or disabled. When the device is sleeping, these interrupts become events that can be used to wake up the device. Equally the status of the interrupt may be read. See Section 10 for further details on sleep and wake-up.

The state of all DIO pins can be read, irrespective of whether the DIO is configured as an input or an output.

Throughout a sleep or deep sleep cycle, the direction of the DIO, and the state of the outputs, is held. This is based on the contents of the GPIO Data/Direction registers and the effect of any enabled peripherals at the point of entering sleep or deep sleep. Following a wake-up these directions and output values are maintained under control of the GPIO data/direction registers. Any peripherals enabled before the sleep or deep sleep cycle are not automatically re-enabled, this must be done through software after the wake-up.

For example, if DIO0 is configured to be SPISEL0 then it becomes an output. The output value is controlled by the SPI-bus functional block. If the device then enters a sleep or deep sleep cycle, the DIO will remain an output and hold the value being output when entering sleep or deep sleep. After wake-up, the DIO will still be an output with the same value but controlled from the GPIO Data/Direction registers. It can be altered with the software functions that adjust the DIO, or the application may reconfigure it to be SPISEL0.

Unused DIO pins are recommended to be set as inputs with the pull-up enabled.

2 DIO pins can optionally be used to provide control signals for RF circuitry (e.g. switches and PA) in high-power range extenders. DIO1/DIO3/RFTX is asserted when the radio is in the transmit state and similarly, DIO0/DIO2/RFRX is asserted when the radio is in the receiver state.

9.9 Serial Peripheral Interface-bus (SPI-bus)

9.9.1 SPI-bus master

The SPI-bus allows high-speed synchronous data transfer between the JN517x and peripheral devices. The JN517x operates as a master on the SPI-bus and all other devices connected to the SPI-bus are expected to be slave devices under the control of the JN517x CPU. The SPI-bus includes the following features:

- Full-duplex, three-wire synchronous data transfer
- Programmable bit rates (up to 16 Mbit/s)
- Programmable transaction size up to 32-bits
- Standard SPI-bus modes 0, 1, 2 and 3
- Manual or automatic slave select generation (up to 2 simultaneous slaves)
- Supports external data in little endian as well as big endian format
- Maskable “transaction complete” interrupt
- LSB First or MSB First Data Transfer
- Supports delayed read edges

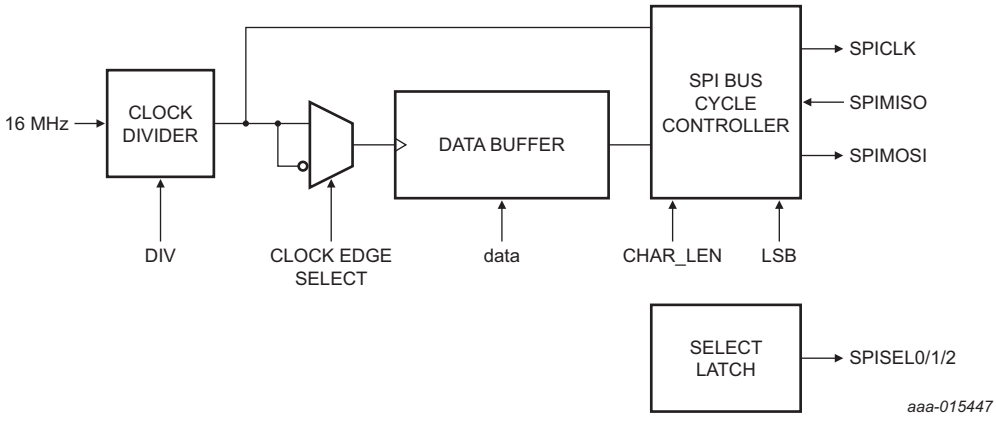


Fig 23. SPI-bus block diagram

The SPI-bus employs a simple shift-register data transfer scheme. Data is clocked out of and into the active devices in a first-in, first-out fashion allowing SPI-bus devices to transmit and receive data simultaneously. Master-Out-Slave-In or Master-In-Slave-Out data transfer is relative to the clock signal SPICLK generated by the JN517x.

The JN517x provides 3 slave selects, SPISEL0 to SPISEL2 to allow 2 simultaneous SPI-bus peripherals on the bus. The Table 4 details which DIO is used for the SPISEL signals depending upon the software configuration.

Table 4. SPI-bus master I/O

Signal	DIO assignment	
	Standard pins	Alternative pins
SPISEL0	DIO6	DIO0, DIO17
SPISEL1	DIO15	-
SPISEL2	-	DIO7
SPICLK	DO0	DIO11
SPIMISO	DO1	DIO18
SPIMOSI	DIO7	DIO15

The interface can transfer from 1 bit to 32 bits without software intervention and can keep the slave select lines asserted between transfers when required, to enable longer transfers to be performed.

When the device reset is active, all the SPI-bus master pins are configured as inputs with their pull-up resistors active. The pins stay in this state until the SPI-bus master block is enabled, or the pins are configured for some other use.

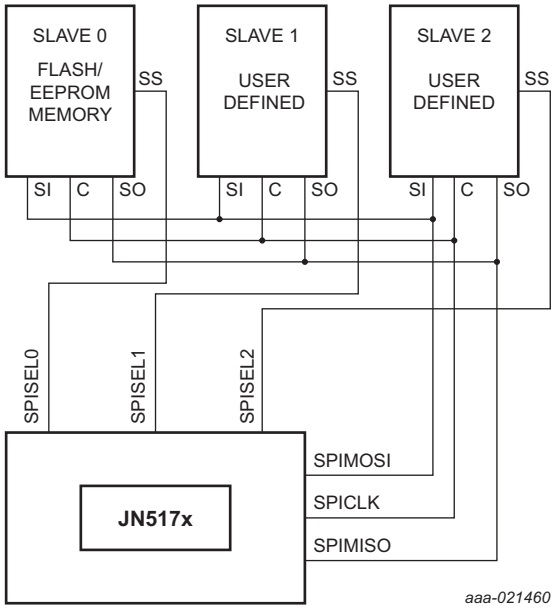


Fig 24. Typical JN517x SPI-bus peripheral connection

The data transfer rate on the SPI-bus is determined by the SPICLK signal. The JN517x supports transfers at data rates from 16 MHz to 125 kHz selected by a clock divider. Both SPICLK clock phase and polarity are configurable. The clock phase determines which edge of SPICLK is used by the JN517x to present new data on the SPIMOSI line; the opposite edge will be used to read data from the SPIMISO line. The interface should be configured appropriately for the SPI-bus slave being accessed.

Table 5. SPI-bus configurations

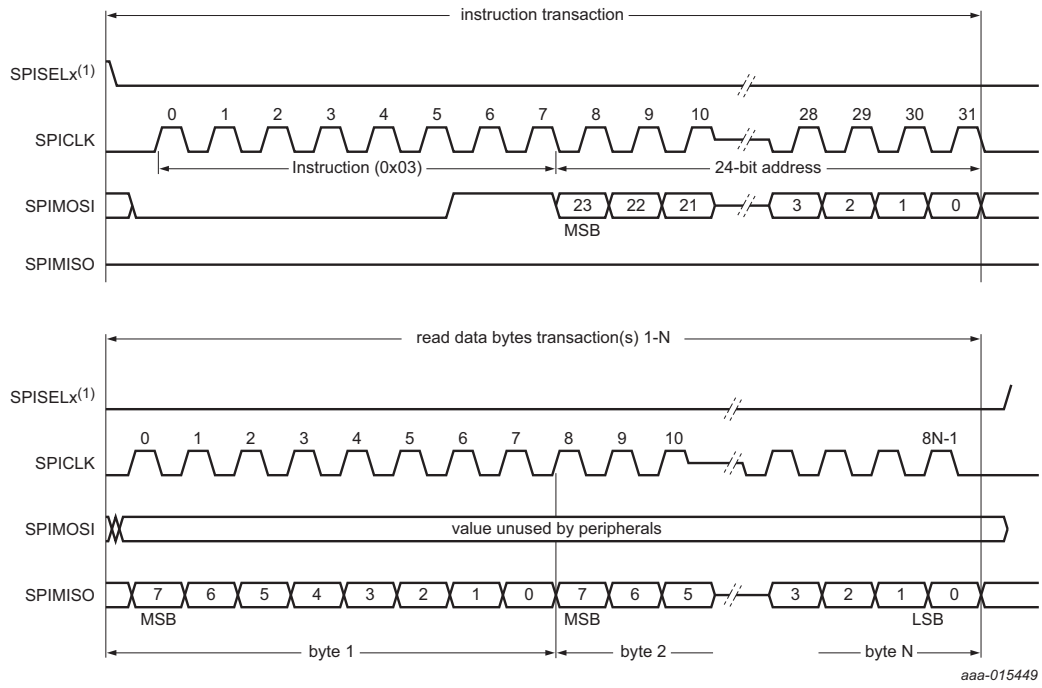
SPICLK		Mode	Description
Polarity (CPOL)	Phase (CPHA)		
0	0	0	SPICLK is low when idle - the first edge is positive. Valid data is output on SPIMOSI before the first clock and changes every negative edge. SPIMISO is sampled every positive edge.
0	1	1	SPICLK is low when idle – the first edge is positive. Valid data is output on SPIMOSI every positive edge. SPIMISO is sampled every negative edge.
1	0	2	SPICLK is high when idle – the first edge is negative. Valid data is output on SPIMOSI before the first clock edge and is changed every positive edge. SPIMISO is sampled every negative edge.
1	1	3	SPICLK is high when idle – the first edge is negative. Valid data is output on SPIMOSI every negative edge. SPIMISO is sampled every positive edge.

If more than one SPISEL line is to be used in a system, they must be used in numerical order starting from SPISEL0. A SPISEL line can be automatically de-asserted between transactions if required, or it may stay asserted over a number of transactions. For devices such as memories where a large amount of data can be received by the master by continually providing SPICLK transitions, the ability for the select line to stay asserted is an advantage since it keeps the slave enabled over the whole of the transfer.

A transaction commences with the SPI-bus being set to the correct configuration, and then the slave device is selected. Upon commencement of transmission, (1 to 32 bits) data is placed in the FIFO data buffer and clocked out, at the same time generating the corresponding SPICLK transitions. Since the transfer is full-duplex, the same number of data bits is being received from the slave as it transmits. The data that is received during this transmission can be read (1 to 32 bits). If the master simply needs to provide a number of SPICLK transitions to allow data to be sent from a slave, it should perform transmit using dummy data. An interrupt can be generated when the transaction has completed or alternatively the interface can be polled.

If a slave device wishes to signal the JN517x indicating that it has data to provide, it may be connected to one of the DIO pins that can be enabled as an interrupt.

Figure 25 shows a complex SPI-bus transfer, reading data from a Flash device that can be achieved using the SPI-bus master interface. The slave select line must stay low for many separate SPI-bus accesses, and therefore manual slave select mode must be used. The required slave select can then be asserted (active low) at the start of the transfer. A sequence of 8-bit and 32-bit transfers can be used to issue the command and address to the Flash device and then to read data back. Finally, the slave select can be deselected to end the transaction.



(1) With x = 0 or 1 or 2.

Fig 25. Example SPI-bus waveforms: reading from Flash device using mode 0

9.9.2 SPI-bus slave

The SPI-bus slave interface allows high-speed synchronous data transfer between the JN517x and a peripheral device. The JN517x operates as a slave on the SPI-bus and an external device, connected to the SPI-bus operates as the master. The pins are different from the SPI-bus master interface and are shown in the Table 6.

Table 6. SPI-bus slave I/O

Signal	DIO assignment	
	Standard pins	Alternative pins
SPISCLK	DIO6	DIO18
SPISMISO	DO1	DIO17
SPISMOSI	DIO11	DIO14
SPISSEL	DIO7	DIO15

The SPI-bus employs a simple shift-register data transfer scheme, with SPISSEL acting as the active low select control. Data is clocked out of and into the active devices in a first-in, first-out fashion allowing SPI-bus devices to transmit and receive data simultaneously. Master-Out-Slave-In or Master-In-Slave-Out data transfer is relative to the clock signal SPISCLK generated by the external master.

The SPI-bus slave includes the following features:

- Full-duplex synchronous data transfer
- Supports external clock up to 8 MHz

- Supports 8-bit transfers (MSB or LSB first configurable), with SPISSEL deselected between each transfer
- Internal FIFO up to 255 bytes for transmit and receive
- Standard SPI-bus mode 0, data is sampled on positive clock edge
- Maskable interrupts for receive FIFO not empty, transmit FIFO empty, receive FIFO fill level above threshold, transmit FIFO below threshold, transmit FIFO overflow, receive FIFO underflow, transmit FIFO underflow, receive time-out
- Programmable receive time-out period allows an interrupt to be generated to prompt the receive FIFO to be read if no further data arrives within the time-out period

9.10 Timers

9.10.1 Peripheral timer/counters

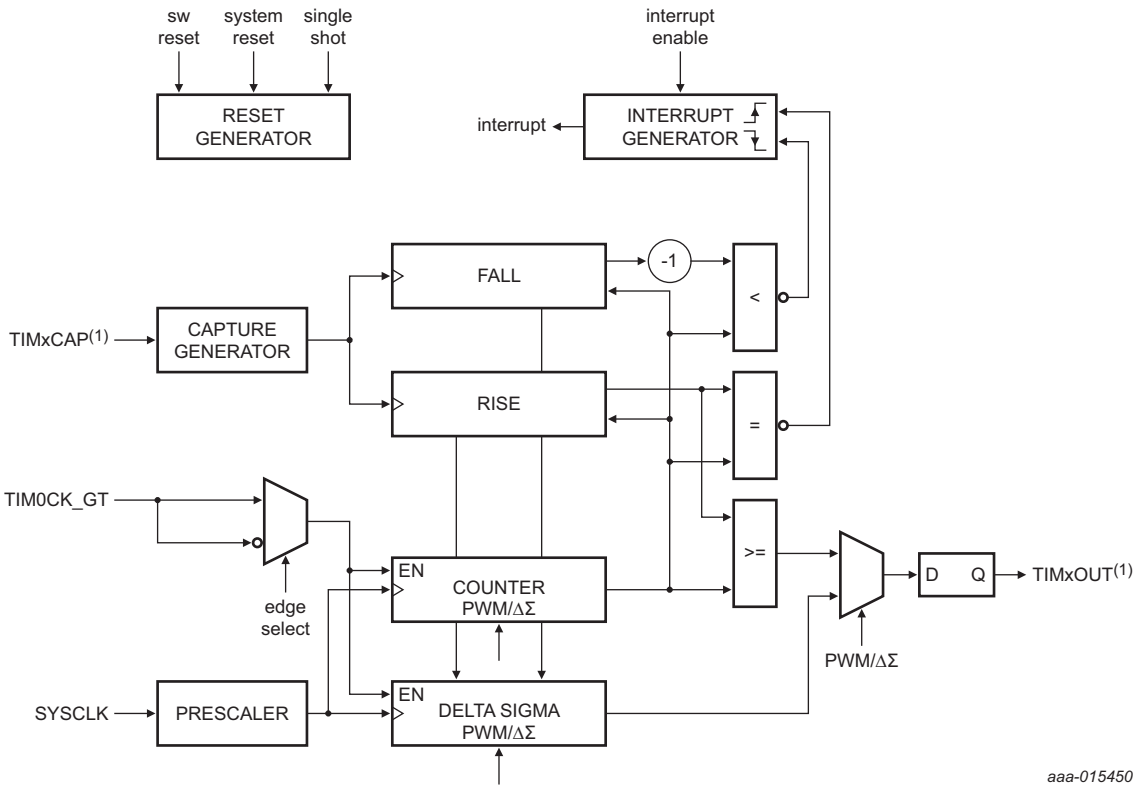
2 general-purpose timer/counter units, Timer0 and Timer1, are available and can be configured to operate in one of five possible modes:

1. Timer: can generate interrupts from rise and fall counts. Can be gated by external signal
2. Counter: counts number of transitions of an external event signal. Can use low-high, high-low or both transitions PWM/Single pulse: outputs a repeating Pulse Width Modulation signal or a single pulse. Can set period and mark-space ratio
3. Capture: measures times between transitions of an applied signal
4. Delta-Sigma: Return-To-Zero (RTZ) and Non-Return-to-Zero (NRZ) modes

The Timer functionality is as follows:

- Clocked from internal system clock (16 MHz or 32 MHz)
- 5-bit prescaler, divides system clock by $2^{prescale}$ as the clock to the timer (prescaler range is 0 to 16)
- 17-bit counter, 17-bit Rise and Fall (period) registers
- Timer: can generate interrupts OFF Rise and Fall counts. Can be gated by external signal
- Counter: counts number of transitions on external event signal. Can use low-high, high-low or both transitions
- PWM/Single pulse: outputs repeating Pulse Width Modulation signal or a single pulse. Can set period and mark-space ratio
- Capture: measures times between transitions of an applied signal
- Delta-Sigma: Return-To-Zero (RTZ) and Non-Return-to-Zero (NRZ) modes
- Timer usage of external IO can be controlled on a pin by pin basis

6 further timers are also available that support the same functionality but have no counter or capture mode. These are referred to as PWM timers. Additionally, it is not possible to gate these four timers with an external signal.



(1) With x = 0 or 1.

Fig 26. Timer unit block diagram

The clock source for the Timer0/Timer1 unit is fed from the system clock, selected as 16 MHz or 32 MHz. This clock passes to a 5-bit prescaler where a value of 0 leaves the clock unmodified and other values divide it by $2^{\text{prescale value}}$. For example, a prescale value of 2 applied to the 16 MHz system clock source results in a timer clock of 4 MHz.

The counter is optionally gated by a signal on the clock/gate input (TIM0CK_GT). If the gate function is selected, then the counter is frozen when the clock/gate input is high.

An interrupt can be generated whenever the counter is equal to the value in either of the High or Low registers.

The Analog Peripheral Timer is dedicated for timing the analog peripherals, e.g. ADC and comparator. APT inputs and outputs do not come to device pins.

Table 7 details which DIO is used for Timer0 and the PWM depending upon the configuration.

Table 7. Timer and PWM I/O

Signal	DIO assignment	
	Standard pins	Alternative pins
TIM0CK_GT	DIO4	DIO15
TIM0CAP	DIO2	DIO5
TIM0OUT	DIO3	DIO8

Table 7. Timer and PWM I/O *...continued*

Signal	DIO assignment	
	Standard pins	Alternative pins
TIM1CAP	DIO6	DIO17
TIM1OUT	DIO11	DIO18
PWM1	DIO12	-
PWM2	DIO13	-
PWM3	DIO14	-
PWM4	DIO3	-
PWM5	DIO8	-
PWM6	DIO15	-

When operating in timer mode, it is not necessary to use any of the DIO pins, allowing the standard DIO functionality to be available to the application.

9.10.1.1 Pulse Width Modulation mode

Pulse Width Modulation (PWM) mode, as used by PWM timers 1, 2, 3, 4, 5 and 6 and optionally by Timer0/Timer1, allows the user to specify an overall cycle time and pulse length within the cycle. The pulse can be generated either as a single shot or as a train of pulses with a repetition rate determined by the cycle time.

In this mode, the cycle time and low periods of the PWM output signal can be set by the values of two independent 17-bit registers (Fall and Rise). The counter-increments and its output are compared to the 17-bit Rise and Fall registers. When the counter is equal to the Rise register, the PWM output is set to high; when the counter reaches the Fall value, the output returns to low. In continuous mode, when the counter reaches the Fall value, it will reset and the cycle repeats. If either the cycle time or low periods are changed while in continuous mode, the new values are not used until a full cycle has completed. The PWM waveform is available on PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, TIM0OUT or TIM1OUTwhen the output driver is enabled. The clock source used for pulse width modulation could be 16 MHz or 32 MHz clock.

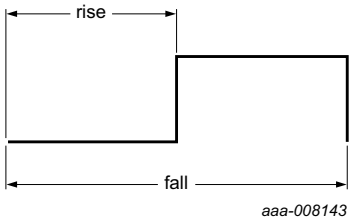
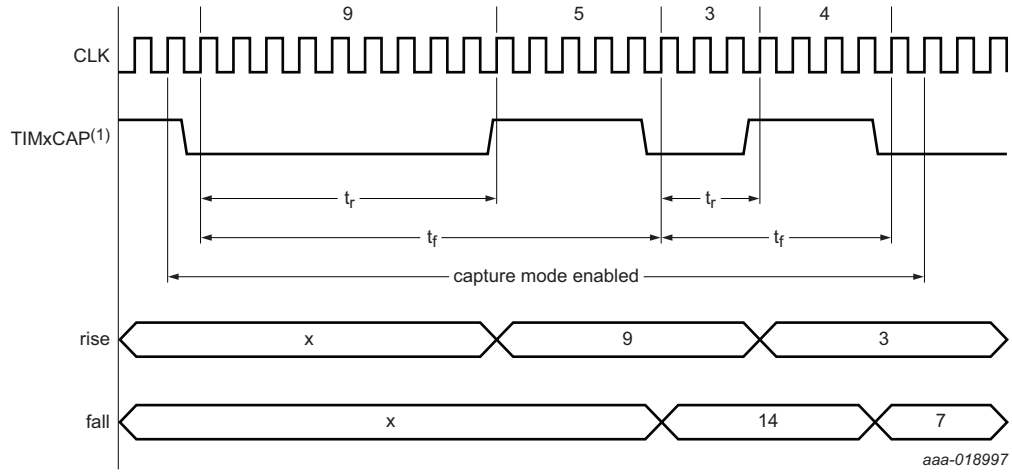


Fig 27. PWM output timings

9.10.1.2 Capture mode

The capture mode can be used to measure the time between transitions of a signal applied to the capture input (TIM0CAP or TIM1CAP). When the capture is started, on the next low-to-high transition of the captured signal, the count value is stored in the rise register, and on the following high-to-low transition, the counter-value is stored in the fall register. The pulse width is the difference in counts in the two registers multiplied by the period of the prescaled clock. Upon reading the capture registers, the counter is stopped.

The values in the high and low registers will be updated whenever there is a corresponding transition on the capture input, and the value stored will be relative to when the mode was started. Therefore, if multiple pulses are seen on capture input before the counter is stopped only the last pulse width will be stored.



(1) With x = 0 or 1.

Fig 28. Capture mode

9.10.1.3 Counter/timer mode

The counter/timer can be used to generate interrupts, based on the timers or event counting, for software to use. When used as a timer the clock source is taken from the system clock, prescaled if required. The timer period is programmed into the fall register and the Fall register match interrupt enabled. The timer is started as either a single-shot or a repeating timer, and generates an interrupt when the counter reaches the Fall register value.

When used to count external events on TIM0CK_GT, the clock source is selected from the input pin and the number of events programmed into the Fall register. The Fall register match interrupt is enabled and the counter started, usually in single shot mode. An interrupt is generated when the programmed number of transitions is seen on the input pin. The transitions counted can configure to be rising, falling or both rising and falling edges. This feature is available only for Timer0.

Edges on the event signal must be at least 100 ns apart, that is pulses must be wider than 100 ns.

9.10.1.4 Delta-sigma mode

A separate delta-sigma mode is available, allowing a low speed delta-sigma DAC to be implemented with up to 17-bit resolution. This requires that a resistor-capacitor network is placed between the output DIO pin and digital ground. A stream of pulses with digital voltage levels is generated which is integrated by the RC network to give an analog voltage. A conversion time is defined in terms of a number of clock cycles. The width of the pulses generated is the period of a clock cycle. The number of pulses output in the cycle, together with the integrator RC values, will determine the resulting analog voltage. For example, generating approximately half the number of pulses that make up a complete conversion period will produce a voltage on the RC output of V_{DD}, provided the

RC time constant is chosen correctly. During a conversion, the pulses will be pseudo-randomly dispersed throughout the cycle in order to produce a steady voltage on the output of the RC network.

The output signal is asserted for the number of clock periods defined in the high register, with the total period being 2^{17} cycles. For the same value in the high register, the pattern of pulses on subsequent cycles is different, due to the pseudo-random distribution.

The delta-sigma converter output can operate in a Return-To-Zero (RTZ) or a Non-Return-to-Zero (NRZ) mode. The NRZ mode allows several pulses to be output next to each other. The RTZ mode ensures that each pulse is separated from the next by at least one period. This improves linearity if the rise and fall times of the output are different to one another. Essentially, the output signal is low on every other output clock period, and the conversion cycle time is twice the NRZ cycle time, that is 2^{18} clocks. The integrated output will only reach half V_{DDD} in RTZ mode, since even at full scale only half the cycle contains pulses. Figure 29 and Figure 30 illustrate the difference between RTZ and NRZ for the same programmed number of pulses.

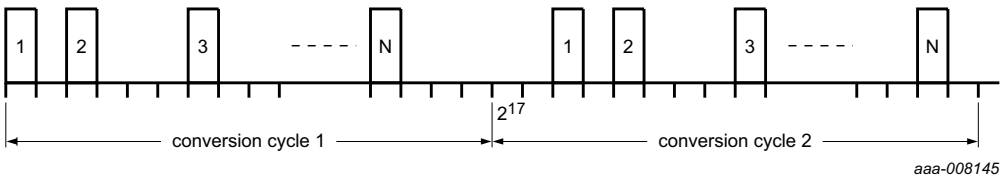


Fig 29. Return-To-Zero mode in operation

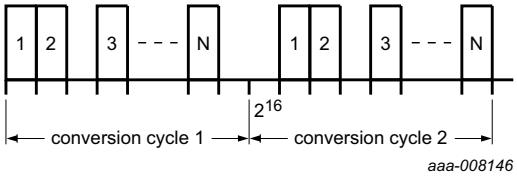


Fig 30. Non-Return-to-Zero mode

9.10.1.5 Example timer/counter application

Figure 31 shows an application of the JN517x timers to provide closed loop speed control. PWM1 is configured in PWM mode to provide a variable mark-space ratio switching waveform to the gate of the NFET. This in turn controls the power in the DC motor.

Timer0 is configured to count the rising edge events on the CLK/GATE pin over a constant period. This converts the tacho pulse stream output into a count proportional to the motor speed. This value is then used by the application software executing the control algorithm.

If necessary for other functionality, then the unused IO associated with the timers could be used as general-purpose DIO.

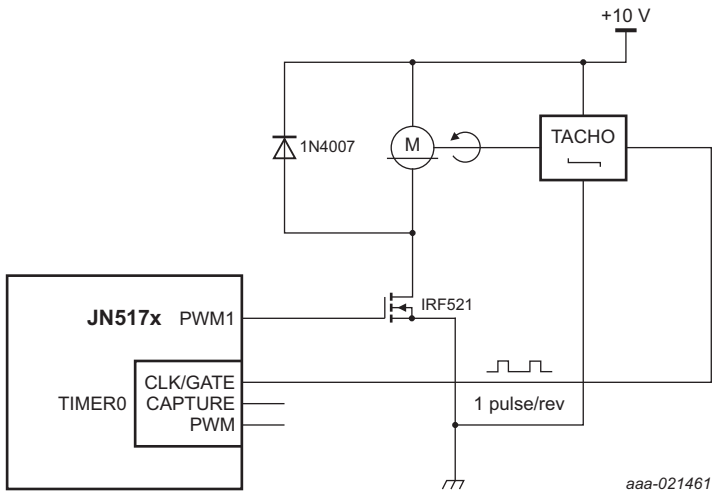


Fig 31. Closed loop PWM speed control using JN517x timers

9.10.2 ARM cortex-M3 system tick timer

The JN517x has a system tick timer (SysTick) which is a part of the Cortex-M3. SysTick, that provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. A system can use this counter in several different ways, including:

- As an RTOS tick timer that fires at a programmable rate, for example 100 Hz, and invokes a SysTick routine each time it fires
- As a high-speed alarm timer using the main processor clock
- As a variable-rate alarm or signal timer. The available duration range depends on the reference clock used and the dynamic range of the counter
- As a simple counter. Software can use this to measure time to completion and time used

For further details, refer to JN-UG-3118 Integrated Peripherals API User Guide JN-UG-3118 on the Wireless Connectivity area of the NXP web site Ref. 2.

In the JN517x, this timer can be clocked from the CPU clock or from a 32 kHz clock. The 32 kHz source can be either high-speed RC oscillator or 32 MHz crystal clock, suitably divided down. When the high-speed RC oscillator is used as the clock source, the SysTick clock may not be accurate 32 kHz.

9.10.3 Wake-up timers

Two 41-bit wake-up timers are available in the JN517x driven from the 32 kHz internal clock. They may run during sleep periods when most of the rest of the device is powered down, to time sleep periods or other long period timings that may be required by the application. The wake-up timers do not run during deep sleep and may optionally be disabled in sleep mode through software control. When a wake-up timer expires, it typically generates an interrupt; if the device is asleep then the interrupt may be used as an event to end the sleep period. See Section 10 for further details on how they are used during sleep periods. Features include:

- 41-bit down counter
- Optionally runs during sleep periods
- Clocked by 32 kHz system clock; either 32 kHz RC oscillator or 32 kHz clock input

A wake-up timer consists of a 41-bit down counter clocked from the selected 32 kHz clock. An interrupt or wake-up event can be generated when the counter reaches zero. On reaching zero, the counter will continue to count down until stopped, which allows the latency in responding to the interrupt to be measured. If an interrupt or wake-up event is required, the timer interrupt should be enabled before loading the count value for the period. Once the count value is loaded and counter started, the counter begins to count down; the counter can be stopped at any time through software control. The counter will remain at the value it contained when the timer was stopped and no interrupt will be generated. The status of the timers can be read to indicate if the timers are running and/or have expired; this is useful when the timer interrupts are masked. This operation will reset any expired status flags.

9.10.3.1 32 kHz RC oscillator calibration

The 32 kHz RC oscillator that can be used to time sleep periods is designed to require very little power to operate and be self-contained, requiring no external timing components and hence is lower cost. As a consequence of using on-chip resistors and capacitors, the inherent absolute accuracy and temperature coefficient is lower than that of a crystal oscillator, but once calibrated the accuracy approaches that of a crystal oscillator. Sleep time periods should be as close to the desired time as possible in order to allow the device to wake up in time for important events, for example beacon transmissions in the IEEE802.15.4 protocol. If the sleep time is accurate, the device can be programmed to wake up very close to the calculated time of the event and so keep current consumption to a minimum. If the sleep time is less accurate, it will be necessary to wake up earlier in order to be certain the event will be captured. If the device wakes earlier, it will be awake for longer and so reduce battery life. The oscillator has a default current consumption of around 0.5 μA, which can optionally be reduced to 0.375 μA, in order to improve battery life. However, the calibrated accuracy and temperature coefficient will be worse as a consequence. For detailed electrical specifications, see Section 14.3.9.

In order to allow sleep time periods to be as close to the desired length as possible, the true frequency of the RC oscillator needs to be determined to better than the initial 30 % accuracy. The calibration factor can then be used to calculate the true number of nominal 32 kHz periods needed to make up a particular sleep time. A calibration reference counter, clocked from the 16 MHz peripheral system clock, is provided to allow comparisons to be made between the 32 kHz RC clock and the 16 MHz clock when the JN517x is awake and running from the 32 MHz crystal.

Wake-up Timer0 counts for a set number of 32 kHz clock periods during which time the reference counter runs. When the wake-up timer reaches zero the reference counter is stopped, allowing software to read the number of 16 MHz clock ticks generated during the time represented by the number of 32 kHz ticks programmed in the wake-up timer. The true period of the 32 kHz clock can thus be determined and used when programming a wake-up timer to achieve a better accuracy and hence more accurate sleep periods.

For an RC oscillator running at exactly 32000 Hz, the value returned by the calibration procedure should be 10000, for a calibration period of twenty 32000 Hz clock periods. If the oscillator is running faster than 32000 Hz the count will be less than 10000, if running

slower the value will be higher. For a calibration count of 9000, indicating that the RC oscillator period is running at approximately 35 kHz, to time for a period of 2 seconds the timer should be loaded with 71,111 ((10000/9000) × (32000 × 2)) rather than 64000.

9.11 Pulse counters

Two 16-bit counters are provided that can increment during all modes of operation (including sleep). The first, PC0, increments from pulses received on DIO1 or DIO13. The other pulse counter, PC1 operates from DIO5 or DIO14 depending upon the configuration. This is enabled under software control. The pulses can be de-bounced using the 32 kHz clock to guard against false counting on slow or noisy edges. Increments occur from a configurable rising or falling edge on the respective DIO input.

Each counter has an associated 16-bit reference that is loaded by the user. An interrupt (and wake-up event if asleep) may be generated when a counter reaches its pre-configured reference value. The 2 counters may optionally be cascaded together to provide a single 32-bit counter, linked to any of the four DIOs. The counters do not saturate at 65535, but naturally roll-over to 0. Additionally, the pulse counting continues when the reference value is reached without software interaction so that pulses are not missed even if there is a long delay before an interrupt is serviced or during the wake-up process.

The system can work with signals up to 100 kHz, with no debounce, or from 5.3 kHz to 1.7 kHz with debounce. When using debounce the 32 kHz clock must be active, so for minimum sleep currents the debounce mode should not be used.

9.12 Serial communications

The JN517x has two Universal Asynchronous Receiver/Transmitter (UART) serial communication interfaces. These provide similar operating features to the industry standard 16550A device operating in FIFO mode. The interfaces perform serial-to-parallel conversion on incoming serial data and parallel-to-serial conversion on outgoing data from the CPU to external devices. In both directions, a configurable FIFO buffer (with a default depth of 16-byte) allows the CPU to read and write multiple characters on each transaction. This means that the CPU is freed from handling data on a character-by-character basis, with the associated high processor overhead. The UARTs have the following features:

- Emulates behavior of industry standard NS16450 and NS16550A UARTs
- Configurable transmit and receive FIFO buffers (with default depths of 16 bytes for each), with direct access to fill levels of each. Adds/deletes standard start, stop and parity bits to/from the serial data
- Independently controlled transmit, receive, status and data sent interrupts
- Optional modem flow control signals CTS and RTS on UART0
- Fully programmable data formats: baud rate, start, stop and parity settings
- False start-bit detection, parity, framing and FIFO overrun error detect and break indication
- Internal diagnostic capabilities: loopback controls for communications link fault isolation
- Flow control by software or automatically by hardware

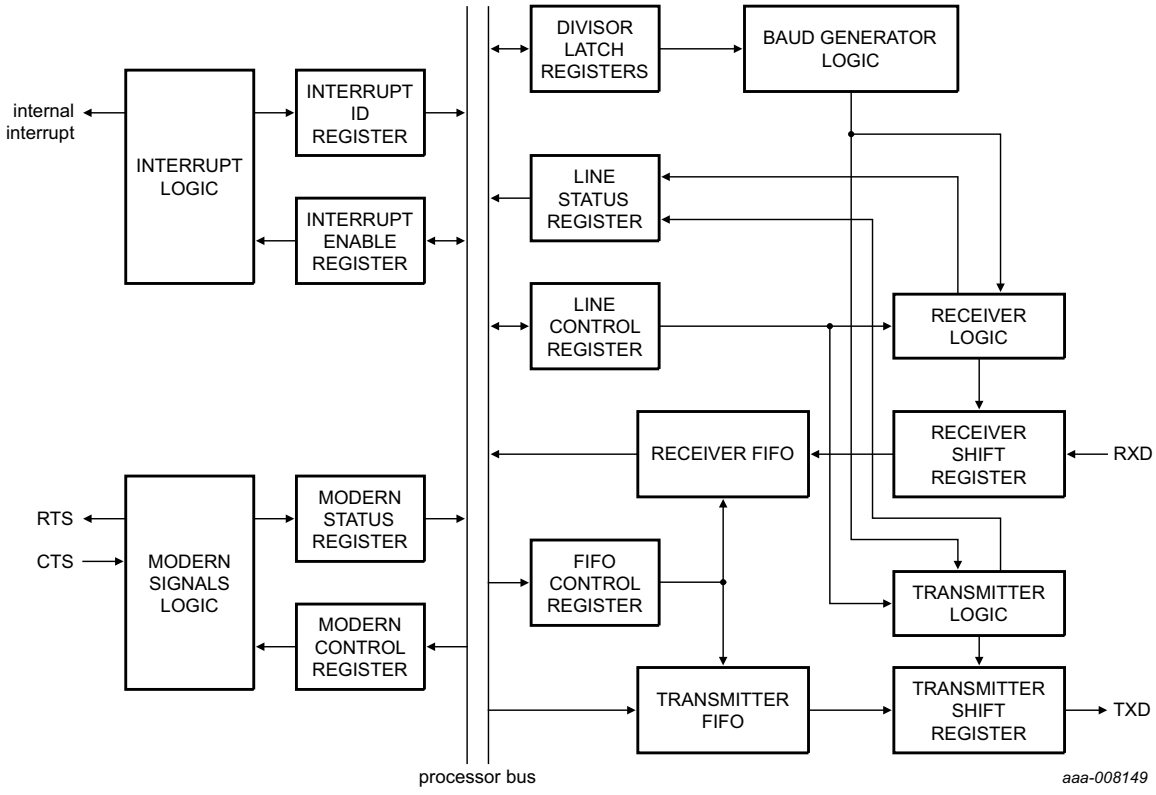


Fig 32. UART block diagram

The serial interfaces contain programmable fields that can be used to set number of data bits (5, 6, 7 or 8), even, odd, set-at-1, set-at-0 or no-parity detection and generation of single or multiple stop bit (for 5-bit data, multiple is 1.5 stop bits; for 6 data bits or 7 data bits or 8 data bits, multiple is 2 bits).

The baud rate is programmable up to 1 Mbits/s and standard 4.8 kbits/s, 9.6 kbits/s, 19.2 kbits/s, 38.4 kbits/s.

For applications requiring hardware flow control, UART0 provides two control signals: Clear-To-Send (CTS) and Request-To-Send (RTS). CTS is an indication sent by an external device to the UART that it is ready to receive data. RTS is an indication sent by the UART to the external device that it is ready to receive data. RTS is controlled from software activities, while the value of CTS can be read. Monitoring and control of CTS and RTS are software activity, normally performed as part of interrupt processing. The signals do not control parts of the UART hardware, but simply indicate to software the state of the UART external interfaces. Alternatively, the automatic flow control mode can be used, in which the hardware controls the value of the generated RTS (negated if the receive FIFO fill level is greater than a programmable threshold of 8 bytes, 11 bytes, 13 bytes or 15 bytes), and only transmits data when the incoming CTS is asserted.

Software can read characters, one byte at a time, from the receive FIFO and can also write to the transmit FIFO, one byte at a time. The transmit and receive FIFOs can be cleared and reset independently of each other. The status of the transmit FIFO can be checked to see if it is empty and if there is a character being transmitted. The status of the receive FIFO can also be checked, indicating if a condition such as parity error, framing

error or break indication has occurred. It also shows if an overrun error has occurred (receive buffer full and another character arrives) and if there is data held in the receive FIFO.

UART0 and UART1 can both be configured to use standard or alternative DIO lines, as shown in Table 8. Additionally, UART0 can be configured to be used in 2-wire mode (where CTS0 and RTS0 are not configured), and UART1 can be configured in 1-wire mode (where RXD1 is not configured). These freed up DIO pins can then be used for other purposes.

Table 8. UART I/O

Signal	DIO assignment	
	Standard pins	Alternative pins
CTS0	DIO6	-
RTS0	DIO11	-
RXD0	DIO4	DIO10, DIO13
TXD0	DIO5	DIO9, DIO12
RXD1	DIO2	DIO6
TXD1	DIO3	DIO11

Remark: With the automatic flow control threshold set to 15, the hardware flow control within the UART's block negates RTS when the receive FIFO is about to become full. In some instances, it has been observed that remote devices that are transmitting data do not respond quickly enough to the de-asserted RTS and continue to transmit data. In these instances, the data will be lost in a receive FIFO overflow

9.12.1 Interrupts

Interrupt generation can be controlled for the UART's block and is divided into four categories:

- Received Data Available: set when data in the RX FIFO queue reaches a particular level (the trigger level can be configured as 1, 4, 8 or 14) or if no character has been received for 4-character times.
- Transmit FIFO Empty: set when the last character from the TX FIFO is read and starts to be transmitted
- Receiver Line Status: set when one of the following occurs
  a. Parity Error - the character at the head of the receive FIFO has been received with a parity error
  b. Overrun Error - the RX FIFO is full and another character has been received at the receiver shift register
  c. Framing Error - the character at the head of the receive FIFO does not have a valid stop bit
  d. Break Interrupt – occurs when the RXD line has been held low for an entire character
- Modem Status: generated when the CTS (Clear To Send) input control line changes.

9.12.2 UART application

The following example shows the UART0 connected to a 9-pin connector compatible with a PC. As the JN517x device pins do not provide the RS232 line voltage, a level shifter is used.

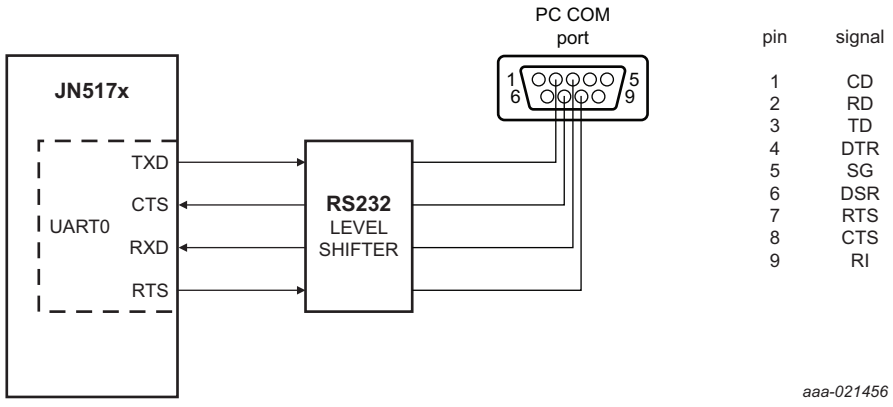


Fig 33. JN517x serial communication link

9.13 JTAG test interface

The JN517x includes a JTAG interface for the purposes of software debugging when used in conjunction with the LCPXpresso for NXP development environment.

For further details, refer to SDK Installation and User Guide JN-UG-3109 on the Wireless Connectivity area of the NXP web site Ref. 2.

The JTAG interface does not support boundary scan testing. It is recommended that the JN517x is not connected as part of the board scan chain.

9.14 2-wire serial interface (I^2C-bus)

The JN517x includes industry standard I^2C-bus 2-wire synchronous Serial Interface operates as a Master (MSIF) or Slave (SSIF) that provides a simple and efficient method of data exchange between devices. The system uses a serial data line (SDA) and a serial clock line (SCL) to perform bidirectional data transfers and includes the following features:

Common to both master and slave:

- Compatible with both I^2C-bus standard
- Support for 7 and 10-bit addressing modes
- Pulse suppression on signal inputs (60 ns guaranteed, 125 ns typical)
- True open-drain support on one set of DIOs
- Receive and transmit FIFO of depth of 8
- Bus monitor mode
- Fail-safe operation on DIO4 and DIO5

Master only:

- Multi-master operation
- Software programmable clock frequency
- Supports Slave clock stretching
- Software programmable acknowledge bit
- Interrupt or polling driven data-transfers

Slave only:

- Read data flow control using clock stretching
- Read data preloaded or provided as required

The serial interface is accessed, depending upon the configuration, through DIO4 and DIO5 which have true open-drain mode or DIO2 and DIO3. This is enabled under software control. The following table details which DIO is used for the Serial Interface depending upon the configuration.

Table 9. 2-wire serial interface I/O

Signal	DIO assignment	
	Standard pins	Alternative pins
SCL	DIO4	DIO3
SDA	DIO5	DIO2

9.14.1 Connecting devices

The clock and data lines, SCL and SDA, are alternate functions of DIO4 and DIO5 respectively. The serial interface function of these pins is selected when the interface is enabled. They are both bidirectional lines, connected internally to the positive supply voltage via weak (50 kΩ) programmable pull-up resistors. However, it is recommended that external 4.7 kΩ pull-ups be used for reliable operation at high bus speeds, as shown in Figure 34. When the bus is free, both lines are HIGH. The output stages of devices connected to the bus must have an open-drain or open-collector in order to perform the wired-AND function. The number of devices connected to the bus is solely dependent on the bus capacitance limit of 400 pF.

DIO4 and DIO5 support fail-safe operation of the I^2C-bus system bus, i.e., if the V_{DD} supply is removed from the JN517x then rest of I^2C-bus at system level is not affected. However when alternate pins DIO2 and DIO3 are used as the I^2C-bus interface the fail-safe operation is not guaranteed as these DIOs do not have true open-drain output stages.

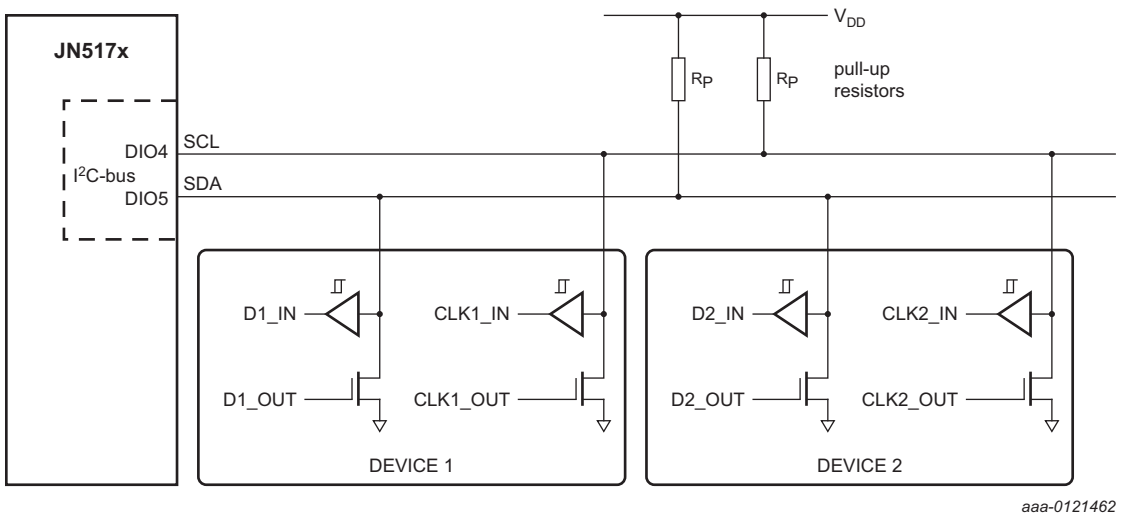


Fig 34. Connection details

9.14.2 Clock stretching

Slave devices can use clock stretching to slow down the read transfer bit rate. After the master has driven SCL low, the slave can drive SCL low for the required period and then release it. If the slave's SCL low period is greater than the master's low period the resulting SCL bus signal low period is stretched thus inserting wait states, see Section 9.14.4 for further details.

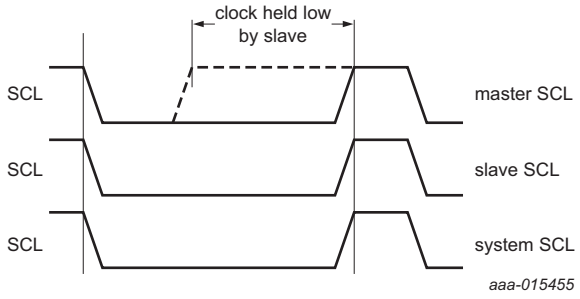


Fig 35. Clock stretching

9.14.3 Master interface

When operating as a master, it provides the clock signal and a separately programmable SCL low and high period to determine the clock rate and shape, allowing operation up to 400 kbit/s.Data transfer is controlled from the processor bus interface by populating the TX FIFO or managing the RX FIFO, with the I²C-bus controller taking care of when start, stop, read, write and acknowledge control should be generated. To use the master device as a receiver, one just needs to fill the TX_FIFO with a start condition and a valid slave address (LSB = 1: read operation), and then with as many dummy bytes (i.e. any byte) as the number of bytes requested from the slave device. A 'stop' must always be issued together with a dummy byte in the TX_FIFO to indicate the slave no longer needs to send data. The data received on the master side is stored in the RX_FIFO.

Regardless of the direction of the communication in master mode the first thing that must be done is to set the I²C-bus clock frequency, by programming both the Clock_Divisor_High and Clock_Divisor_Low registers.

Then the programming depends on the function required for the device:

9.14.3.1 Master transmitter

1. The user has to write the TX_FIFO register with a slave address byte (with the LSB set to 0 = write operation) and a start command bit, so that an I²C-bus transfer can be initiated. The data bytes to be sent must then be loaded into the TX_FIFO register (start and stop commands bits should be cleared to '0'). The matching slave device will acknowledge the slave address and then each data byte so that the transaction can continue.
2. If the TX_FIFO is empty, the master will automatically stretch the clock of the previous byte (after acknowledge) until a new byte is written to the TX_FIFO as can be seen in Figure 36. This stretching after acknowledge is the case for the address + R/W byte (first) as well as for all data bytes that follow.

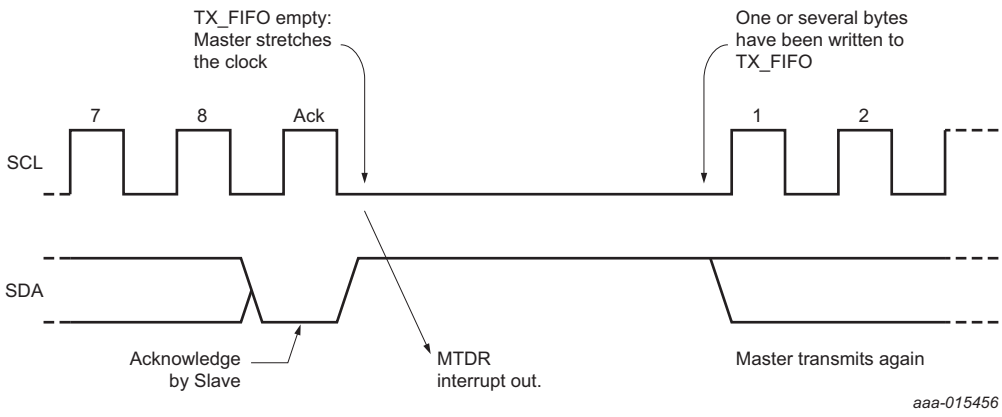


Fig 36. TX_FIFO in the middle of a transaction

3. With the LAST data byte to be sent the user must set the stop bit to generate a STOP condition and the slave should acknowledge the byte. For a RESTART to be issued both start and stop bits should remain cleared at this point.
4. If a STOP has been produced, a new transaction can be initiated by jumping back to step 1 of the master receiver or transmitter mode. Otherwise for the RESTART case, the start bit has to be programmed together with the slave address of the next transaction (start bit set).

The next action will be step 2 of the master receiver or Transmitter mode, depending on the slave address direction bit. Table 10 is an example of master transmitter writing data to TX_FIFO.

Table 10. I²C-bus TX_FIFO master transmitter writing data example

Instruction code	Description
0x148	master issues a START + slave address 24h (write operation)
0x025	data bytes 25h", 13h will be sent to the slave" interrupt
0x013	-

Table 10. I²C-bus TX_FIFO master transmitter writing data example *…continued*

Instruction code	Description
0x1DC	master issues a RESTART + slave address 6Eh (write)
0x001	data bytes 01h, AAh will be sent to the slave
0x2AA	master issues a STOP

9.14.3.2 Master receiver

1. The user has to write the TX_FIFO register with a slave address byte (with the LSB set to 1 = read operation) and a start command bit, so that an I²C-bus transfer can be initiated. The slave will acknowledge if it recognizes its address, and start transmitting data.
2. For each data byte requested by the master, a dummy byte (i.e. the value of the data byte can be anything from 0x00 to 0xFF) must be loaded into the TX_FIFO, so that the master acknowledges the data bytes it receives. Please note that the acknowledge bit is generated automatically; no specific programming is required for it. The received (acknowledged) data bytes will be stored in the RX_FIFO (address 0x000), from where they can be fetched by the bus system interface. If the RX_FIFO happens to be full (interrupt RX_FIFO_FULL) in the middle of a transaction, the master will automatically stretch the clock before the acknowledge of the last byte that is stored, until some room is made in the RX_FIFO, refer to Figure 37. The data is actually written into the RX_FIFO on the 8th clock cycle, so it can be read by software even if the clock is currently stretched in the Ack cycle (9th clock) due to RX_FIFO_Full.

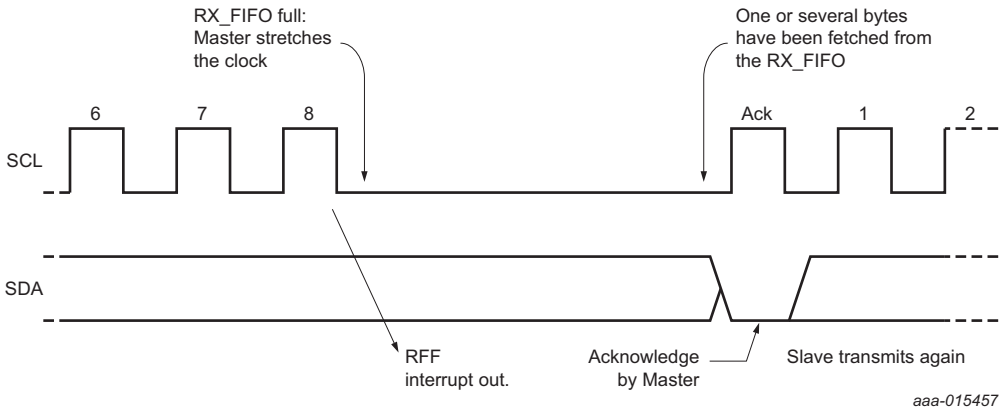


Fig 37. RX_FIFO full in the middle of a transaction

3. When the LAST data byte has to be received, the user must set the stop bit with the last dummy byte to generate a STOP condition. In this case, the master will NOT Acknowledge the byte, so that the slave releases the data line and the STOP can be issued by the master

   If the TX_FIFO is empty, the master will automatically stretch the clock. If the TX_FIFO becomes empty, the clock will be stretched after the acknowledgement has been sent. This behavior is identical to the master transmitter as shown in Figure 36. However when the TX_FIFO is empty after sending a dummy byte (in order to receive a byte from the slave) the clock will be stretched between the 8th cycle and the Ack cycle, until at least one new byte is written to the TX_FIFO. This is shown in

Figure 38.

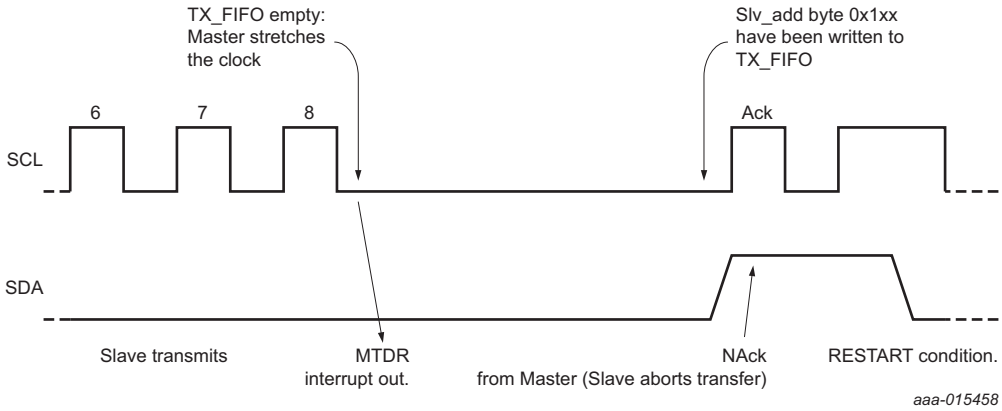


Fig 38. TX_FIFO empty just before RESTART condition in master slave case

The master transmitter has to stretch the clock between the 8th and the 9th pulse when TX_FIFO is empty, since it does not know whether it should send a NAck (next byte that is programmed contains a restart) or an Ack (next byte is a normal dummy data byte). Although the clock is stretched in the Ack cycle until the next dummy byte is written into the TX_FIFO, the current data can already be read from the RX_FIFO, since the data is written into the RX_FIFO on the 8th clock pulse. This implies that data can be read from a slave on a byte by byte basis even when the TX_FIFO is empty.

4. If a STOP has been produced, a new transaction can be initiated by jumping back to step 1 of the master receiver or transmitter mode. Otherwise for the RESTART case, the start bit has to be programmed together with the slave address of the next transaction. The previous byte will then not be acknowledged and the restart produced. The next action will be then step 2 of the master receiver or transmitter mode, depending on the slave address direction bit. When the master loses arbitration, the data already received in the RX_FIFO is invalid. To prevent new slave I2C-bus data from being written into the RX_FIFO while it still contains this invalid data, the RX_FIFO_block signal is set (bit 10 of I2C_Status register). When the RX_FIFO is accessed as a slave receiver after it has lost arbitration (as a master) and the RX_FIFO was not cleared (emptied) the clock will be stretched, until the RX_FIFO has been emptied. See Section 9.14.4.1 for more information.

Table 11. I2C-bus RX_FIFO master receiver reading data example

Instruction code	Description
0x149	master issues a START + slave address 24h (read operation)
0x0xx	the presence of the 3 dummy bytes indicates that the master expects 3 data bytes from the slave
0x0xx	-
0x2xx	master issues a STOP

9.14.4 Slave interface

When operating as a slave, the first thing that needs to be done is to set the addressing mode (either 10-bit or 7-bit).

As soon as the slave sees a start condition on the bus, it will read the first byte (if 7-bit slave address mode selected) or the first 2 bytes (if 10-bit slave address mode selected). If the address received matches the address programmed into the slave by the user, it will acknowledge the slave address, and enter respectively the Receiver or the Transmitter mode, according to the slave address first byte LSB, respectively 0 or 1.

9.14.4.1 Slave receiver

All the received bytes are stored in the RX_FIFO and all bytes are acknowledged. The slave cannot generate a NAck.

Remark: the generation of the acknowledge is automatic and no extra programming is required.

If the RX_FIFO happens to be full (interrupt RX_FIFO_FULL) in the middle of a transaction, the slave will automatically stretch the clock after the acknowledge of the last byte stored, until some room is made in the RX_FIFO as shown in Figure 39.

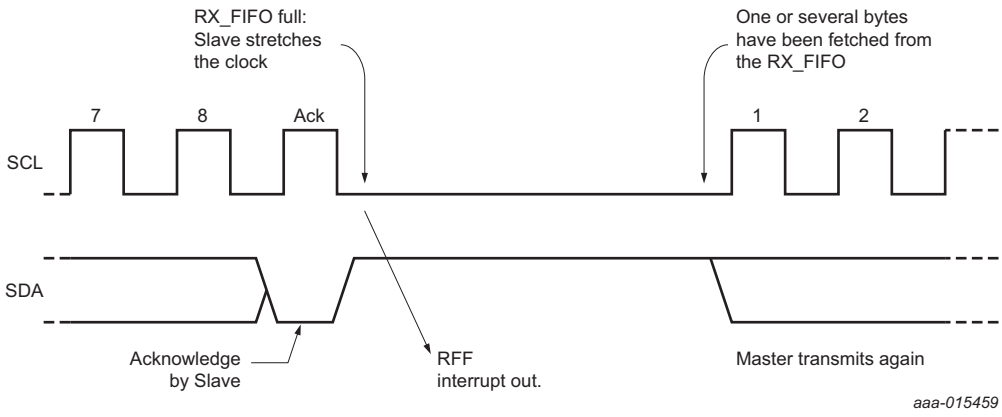


Fig 39. Slave receiver: RX_FIFO in middle of a transaction

The transaction is aborted only when a STOP or a RESTART is detected on the bus.

After the slave has been addressed in receiver mode, the RX_FIFO must be emptied before the device is addressed again after a STOP or RESTART. This will be notified externally via interrupt SRSD (Int_Status register bit 4), set when the slave receiver sees a STOP or a RESTART on the bus. The RX_FIFO is then automatically blocked (I2C_Status register bit 10 set) and must be emptied (read), before clearing the interrupt. Only then can the slave be involved in a new transfer. If the slave is addressed again in receiver mode and the RX_FIFO is not empty, the slave will stretch the clock after acknowledging its address, until the RX_FIFO is completely emptied. This mechanism is present to prevent multiple messages from being entered into the RX_FIFO, since the slave cannot differentiate 2 distinct messages - START and STOP information is not stored.

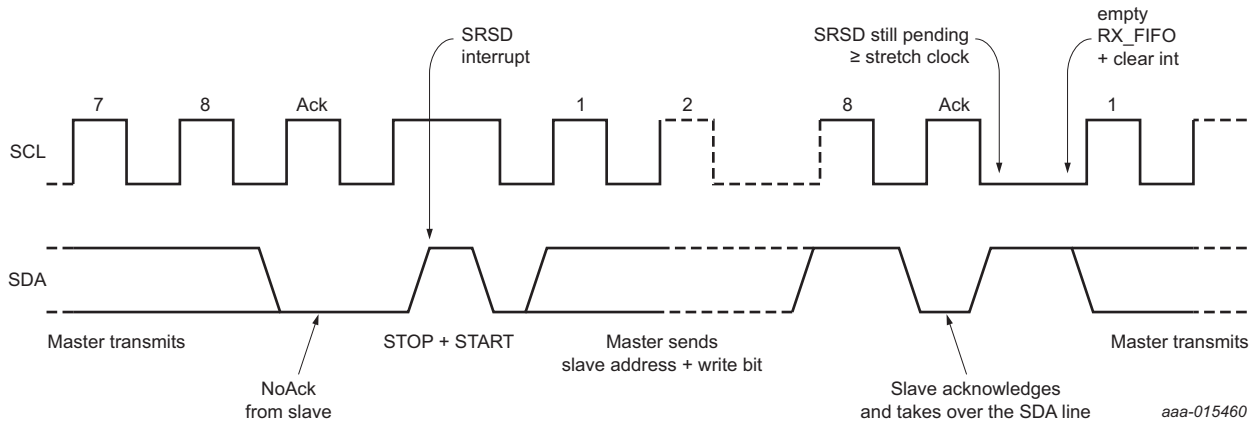


Fig 40. Example of use of the SRSD interrupt (STOP case)

9.14.4.2 Slave transmitter

The slave transmitter data must be written to the TXS_FIFO. Each data byte must be acknowledged by the master to continue the transaction.

If the TXS_FIFO is empty (interrupt STDR -Int_Status register bit 8- set), the slave will automatically stretch the clock of the previous byte (after acknowledge) until some new byte is loaded in the TXS_FIFO. See Figure 41.

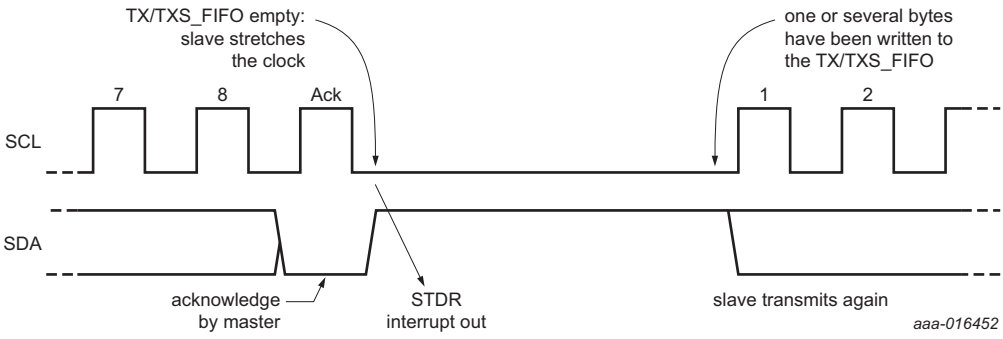


Fig 41. TXS_FIFO empty in the middle of a transaction

A transaction is aborted only when the master does not acknowledge a data byte, after which the slave releases the data line. A STOP or a RESTART is then issued by the master.

After the slave has been addressed in transmitter mode, the TXS_FIFO must be emptied before the device is addressed again. This is notified externally via interrupt STSD (Int_Status register bit 3), set when the slave transmitter sees a STOP or a RESTART on the bus. The TXS_FIFO is then automatically blocked (I2C_Status register bit 11 set) and must be flushed by software before clearing the interrupt. This blocking mechanism is used to prevent unwanted data from remaining in the TXS_FIFO after the STOP or RESTART on the bus. If the slave is addressed again in transmitter mode and the TXS_FIFO has not been flushed, the slave will stretch the clock after acknowledging its address, until the TXS_FIFO is flushed and filled up again with correct new data.

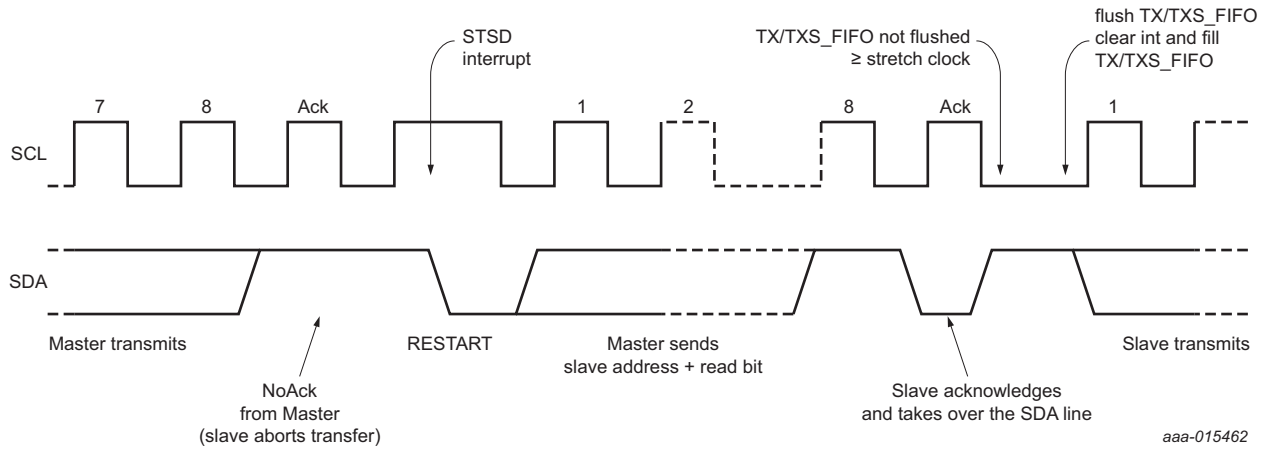


Fig 42. Example of use of the STSD interrupt (RESTART case)

9.14.5 Particular cases on I²C-bus

9.14.5.1 I²C-bus error

In a protocol violation on the I²C-bus, i.e., an unexpected START or STOP in the middle of a transfer, the I²C-bus Error interrupt is set. On detection of an unexpected stop condition, the device goes to the IDLE state and releases SDA and SCL. In case of an unexpected restart condition, the device releases SDA and SCL checks whether it is addressed as a slave.

9.14.5.2 Arbitration lost

When arbitration loss occurs, the Transmitter Arbitration Failure interrupt (TAF: bit 1 of the Int_Status register) is automatically set. This means that the data bytes stored in the TX_FIFO and the RX_FIFO are not valid, since the transfer was interrupted. The TX_FIFO must be flushed (I2C_Control register bit 3) before clearing the interrupt. On detection of an arbitration loss, the master will immediately release the I²C-bus (IDLE state).

Likewise, the data in the RX_FIFO is invalid and must be read by the system to empty the RX_FIFO. Until this is done, access to the RX_FIFO from I²C-bus is blocked by clock stretching as described in Section 9.14.3.

9.14.5.3 NAck from slave receiver

If a master transmitter receives a NAck from the addressed slave, the master will automatically generate a STOP and break off the transfer. The user must manually flush the TX_FIFO before clearing the interrupt.

Software can add data to the TX_FIFO, since there is no blocking from the system bus, however this data must be flushed again later to start normal master operation again.

9.15 Random number generator

A random number generator is provided which creates a 16-bit random number each time it is invoked. Consecutive calls can be made to build up any length of random number. Each call takes approximately 0.25 ms to complete. Alternatively, continuous generation

mode can be used where a new number is generated approximately every 0.25 ms. In either mode of operation, an interrupt can be generated to indicate when the number is available, or a status bit can be polled.

The random bits are generated by sampling the state of the 32 MHz clock every 32 kHz system clock edge. As these clocks are asynchronous to each other, each sampled bit is unpredictable and hence random.

9.16 Analog peripherals

The JN517x contains a number of analog peripherals allowing the direct connection of a wide range of external sensors and switches.

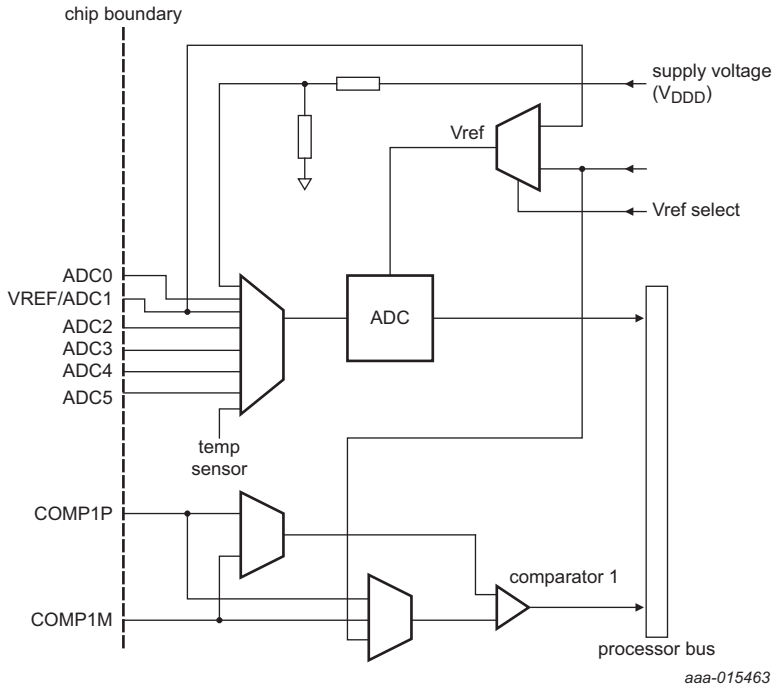


Fig 43. Analog peripherals

In order to provide good isolation from digital noise, the analog peripherals and radio are powered by the radio regulator, which is supplied from the analog supply V_{DDA} and referenced to analog ground V_{SSA}.

A reference signal V_{ref} for the ADC can be selected between an internal band gap reference or an external voltage reference supplied to the VREF pin. ADC input 1 cannot be used if an external reference is required, as this uses the same pin as VREF. The ADC4, ADC3, ADC5 and ADC2 use the same pins as DIO0, DIO1, DIO2 and DIO3 respectively. These pins can only be used for the ADC if they are not required for any of their alternative functions. Similarly, the comparator inputs are shared with DIO17 and DIO18. If used for their analog functions, these DIOs must be put into a passive state by setting them to Inputs with their pull-ups disabled.

The ADC is clocked from a common clock source derived from the 16 MHz clock

9.16.1 Analog to Digital Converter

The 10-bit ADC uses a successive approximation design to perform high accuracy conversions as typically required in wireless sensor network applications. It has eight multiplexed single-ended input channels: six available externally, one connected to an internal temperature sensor, and one connected to an internal supply monitoring circuit.

9.16.1.1 Operation

The input range of the ADC can be set between 40 mV to either the reference voltage or twice the reference voltage. The reference can be either taken from the internal voltage reference or from the external voltage applied to the VREF pin. For example, an external reference of 1.2 V supplied to VREF may be used to set the ADC range between 40 mV and 2.4 V.

Table 12. ADC maximum input range

VREF	Gain setting	Maximum input range	Supply voltage range (V_{DD})
1.2 V	0	1.2 V	2.2 V to 3.6 V
1.6 V	0	1.6 V	2.2 V to 3.6 V
1.2 V	1	2.4 V	2.6 V to 3.6 V
1.6 V	1	3.2 V	3.4 V to 3.6 V

The input clock to the ADC is 16 MHz and can be divided down to 2 MHz, 1 MHz, 500 kHz and 250 kHz. During an ADC conversion, the selected input channel is sampled for a fixed period and then held. This sampling period is defined as a number of ADC clock periods and can be programmed to 2, 4, 6 or 8. The conversion rate is ((3 × sample period) + 13) clock periods. For example, for 500 kHz conversion with sample period of 2 will be (3 × 2) + 13 = 19 clock periods, 38 μs or 26.32 kHz. The ADC can be operated in either a single conversion mode or alternatively a new conversion can be started as soon as the previous one has completed, to give continuous conversions.

If the source resistance of the input voltage is 1 kΩ or less, then the default sampling time of 2 clock periods should be used. The input to the ADC can be modeled as a resistor of 5 kΩ (typ.) and 10 kΩ (max.) to represent the on-resistance of the switches and the sampling capacitor 8 pF. The sampling time required can then be calculated, by adding the sensor source resistance to the switch resistance, multiplying by the capacitance giving a time constant. Assuming normal exponential RC charging, the number of time constants required to give an acceptable error can be calculated, seven time constants gives an error of 0.091 %, so for 10-bit accuracy, seven time constants should be the target. For a source with zero resistance, seven time constants are 640 ns, hence the smallest sampling window of 2 clock periods can be used.

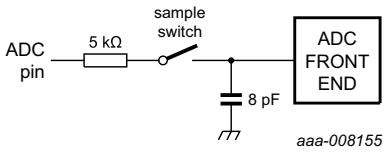


Fig 44. ADC input equivalent circuit

The ADC sampling period, input range and mode (single shot or continuous) are controlled through software.

When the ADC conversion is complete, an interrupt is generated. Alternatively the conversion status can be polled. When operating in continuous mode, it is recommended that the interrupt is used to signal the end of a conversion, since conversion times may range from 9.5 μs to 148 μs. Polling over this period would be wasteful of processor bandwidth.

To facilitate averaging of the ADC value, which is a common practice in microcontrollers, a dedicated accumulator has been added, the user can define the accumulation to occur over 2, 4, 8 or 16 samples. The end of conversion interrupt can be modified to occur at the end of the chosen accumulation period, alternatively polling can still be used. Software can then be used to apply the appropriate rounding and shifting to generate the average value, as well as setting up the accumulation function.

For detailed electrical specifications, see Section 14.3.7.

9.16.1.2 Supply monitor

The internal supply monitor allows the voltage on the analog supply pin V_{DDA} to be measured. This is achieved with a potential divider that reduces the voltage by a factor of 0.666, allowing it to fall inside the input range of the ADC when set with an input range twice the internal voltage reference. The resistor chain that performs the voltage reduction is disabled until the measurement is made to avoid a continuous drain on the supply.

9.16.1.3 Temperature sensor

The on-chip temperature sensor can be used either to provide an absolute measure of the device temperature or to detect changes in the ambient temperature. In common with most on-chip temperature sensors, it is not trimmed and so the absolute accuracy variation is large; the user may wish to calibrate the sensor prior to use. The sensor forces a constant current through a forward biased diode to provide a voltage output proportional to the chip die temperature which can then be measured using the ADC. The measured voltage has a linear relationship to temperature as described in Section 14.3.13.

Because this sensor is on-chip, any measurements taken must account for the thermal time constants. For example, if the device just came out of sleep or deep sleep mode the user application should wait until the temperature has stabilized before taking a measurement.

9.16.1.4 ADC sample buffer mode

In this mode, the ADC operates with a Direct Memory Access (DMA) engine as follows:

- ADC sampling is triggered at a configurable rate using dedicated Timer ADC
- ADC samples are automatically stored in a buffer located in RAM using a DMA mechanism
- ADC inputs may be multiplexed between different analog sources

The 10-bit ADC data samples are transferred into the buffer in RAM as 16-bit words. The maximum number of 16-bit words that may allocated in RAM for ADC sample storage is 2047.

The buffer may be configured to automatically wrap around to the start when full. Interrupts may be configured to indicate when the buffer is half-full, full and has overflowed.

The CPU may perform other tasks while the data transfer and storage is being managed independently by the DMA engine - the CPU only needs to configure the ADC sample buffer mode and deal with the stored samples in the buffer when an interrupt occurs.

ADC sample buffer mode allows up to 8 analog inputs to be multiplexed in combination. These inputs comprise 6 external inputs (ADC0 to 5, corresponding to IO pins), an on-chip temperature sensor and an internal voltage monitor. Samples from all the selected inputs will be produced on each timer trigger and stored in consecutive RAM locations.

9.16.2 Comparator

The JN517x contains one analog comparator, COMP1, that is designed to have true rail-to-rail inputs and operate over the full voltage range of the analog supply V_{DDA}. The hysteresis level can be set to a nominal value of 0 mV, 10 mV, 20 mV or 40 mV. The source of the negative input signal for the comparator can be set to the internal voltage reference, the negative external pin (COMP1M, which uses the same pin as DIO18) or the positive external pin (COMP1P, on the same pin as DIO17). The source of the positive input signal can be COMP1P or COMP1M. DIO17 and DIO18 cannot be used if the external comparator inputs are needed. The comparator output is routed to an internal register and can be polled, or can be used to generate interrupts. The comparator can be disabled to reduce power consumption. DIO17 and DIO18 should be set to inputs with pull-ups disabled, when using the comparator.

The comparator also has a low-power mode where the response time of the comparator is slower than the normal mode, but the current required is greatly reduced. These figures are specified in Section 14.3.8. It is the only mode that may be used during sleep, where a transition of the comparator output will wake the device. The wake-up action and the configuration for which edge of the comparator output is active are controlled through software. In sleep mode, the negative input signal source must be configured to be driven from the external pins.

9.16.3 Digital monitor for ADC output

The JN517x contains one digital monitor function at the output of the ADC. The digital monitor can be configured to compare the ADC output against programmable upper threshold (DC_UT) and lower threshold (DC_LT) and raise an interrupt on enabled trigger conditions. The output of the monitor can also be brought out on DIO7. There are four trigger conditions which can be selected:

- Less than: TRUE when ADC_VAL < DC_LT
- More than: TRUE when ADC_VAL > DC_UT
- Inside range: TRUE when DC_LT ≤ ADC_VAL ≤ DC_UT
- Outside range: TRUE when (ADC_VAL < DC_LT) OR (ADC_VAL > DC_UT)

10. Power management and sleep modes

10.1 Operating modes

After the main supply source is selected, 3 operating modes are provided in the JN517x that enable the system power consumption to be controlled carefully to maximize battery life.

- Active processing mode
- Sleep mode
- Deep sleep mode

The variation in power consumption of the 3 modes is a result of having a series of power domains within the chip that may be selectively powered ON or OFF.

10.1.1 Power domains

The JN517x has the following power domains:

- V_{DD} supply domain: supplies the wake-up timers and controller, DIO blocks, Comparator, SVM and BOR together with the Fast RC, 32 kHz RC and crystal oscillator. This domain is driven from the external supply (battery) and is always powered. The wake-up timers and controller, and the 32 kHz RC and crystal oscillator may be powered ON or OFF in sleep mode through software control.
- Digital logic domain: supplies the digital peripherals, CPU, Flash when in active processing mode, baseband controller, modem and encryption processor. It is powered OFF during sleep or deep sleep mode.
- RAM domain: supplies the RAM when in active processing mode. Also supplies the RAM during sleep mode to retain the memory contents. It may be powered ON or OFF for sleep mode through software control.
- Radio domain: supplies the radio interface, ADCs and temperature sensor. It is powered during transmit and receive and when the analog peripherals are enabled. It is controlled by the baseband processor and is powered OFF during sleep or deep sleep mode.

The current consumption figures for the different modes of operation of the device is given in Section 14.1.

10.2 Active processing mode

Active processing mode in the JN517x is where all of the application processing takes place. By default, the CPU will execute at the selected clock speed executing application firmware. All of the peripherals are available to the application, as are options to actively enable or disable them to control power consumption; see specific peripheral sections for details.

While in active processing mode there is the option to doze the CPU but keep the rest of the chip active; this is particularly useful for radio transmit and receive operations, where the CPU operation is not required therefore saving power.

10.2.1 CPU doze

While in doze mode, CPU operation is stopped but the chip remains powered and the digital peripherals continue to run. Doze mode is entered through software and is terminated by any interrupt request. Once the interrupt service routine has been executed, normal program execution resumes. Doze mode uses more power than sleep and deep sleep modes but requires less time to restart and can therefore be used as a low-power alternative to an idle loop.

While in CPU doze, the CPU is not drawing current, therefore the total device current is reduced.

10.3 Sleep mode

The JN517x enters sleep mode through software control. In this mode most of the internal chip functions are shut down to save power, however the state of DIO pins are retained, including the output values and pull-up enables, and this therefore preserves any interface to the outside world.

When entering into sleep mode, there is an option to retain the RAM contents throughout the sleep period. If the wake-up timers are not to be used for a wake-up event and the application does not require them to run continually, then power can be saved by switching off the 32 kHz oscillator if selected as the 32 kHz system clock through software control. The oscillator is restarted when a wake-up event occurs.

Whilst in sleep mode, one of 4 possible events can cause a wake-up to occur: transitions on DIO inputs, expiry of wake-up timers, pulse counters maturing or comparator events. If any of these events occur, and the relevant interrupt is enabled, then an interrupt is generated that will cause a wake-up from sleep. It is possible for multiple wake-up sources to trigger an event at the same instant and only one of them will be accountable for the wake-up period. It is therefore necessary in software to remove all other pending wake-up events prior to requesting entry back into sleep mode; otherwise, the device will reawaken immediately.

When wake-up occurs, a similar sequence of events to the reset process described in Section 9.5.1 happens, including the checking of the supply voltage by the Supply Voltage Monitor (Section 9.5.4). The high-speed RC oscillator is started up, once stable the power to the CPU sub-system is enabled and the reset is removed. Software determines that this is a reset from sleep and so commences with the wake-up process. If RAM contents were held through sleep, wake-up is quicker as the software does not have to initialize RAM contents meaning the application can recommence more quickly. See Section 14.3.5 for wake-up timings.

10.3.1 Wake-up timer event

The JN517x contains two 41-bit wake-up timers that are counters clocked from the 32 kHz oscillator, and can be programmed to generate a wake-up event. Following a wake-up event, the timers continue to run. These timers are described in Section 9.10.3.

Timer events can be generated from both of the timers; one is intended for use by the 802.15.4 protocol, the other being available for use by the application running on the CPU. These timers are available to run at any time, even during sleep mode.

10.3.2 DIO event

Any DIO pin when used as an input has the capability, by detecting a transition, to generate a wake-up event. Once this feature has been enabled, the type of transition can be specified (rising or falling edge). Even when groups of DIO lines are configured as alternative functions such as the UARTs or Timers, any input line in the group can still be used to provide a wake-up event. This means that an external device communicating over the UART can wake up a sleeping device by asserting its RTS signal pin (which is the CTS input of the JN517x).

10.3.3 Comparator event

The comparator can generate a wake-up interrupt when a change in the relative levels of the positive and negative inputs occurs. The ability to wake up when continuously monitoring analog signals is useful in ultra-low power applications. For example, the JN517x can remain in sleep mode until the voltage drops below a threshold and then be woken up to deal with the alarm condition; the comparator has a low current mode to facilitate this.

10.3.4 Pulse counter

The JN517x contains two 16-bit pulse counters that can be programmed to generate a wake-up event. Following the wake-up event the counters will continue to operate and therefore no pulse will be missed during the wake-up process. These counters are described in Section 9.11.To minimize sleep current it is possible to disable the 32 kHz RC oscillator and still use the pulse counters to cause a wake-up event, provided debounce mode is not required.

10.4 Deep sleep mode

Deep sleep mode gives the lowest power consumption. All switchable power domains are off and most functions in the V_{DD} supply power domain are stopped, including the 32 kHz RC oscillator. However, the Brown-Out Reset remains active as well as all the DIO cells. This mode can be exited by a hardware reset on the RESET_N pin, or an enabled DIO wake-up event.

10.5 Flicker control

FLICK_CTRL feature is dedicated to lighting application in a bulb. It allows either to do a OR or NOR function from RFRX and RFTX to be outputted on one of DIO. Aim of this feature is to compensate the variation of current of the IC depending of the mode (RX/TX) when using Lighting application.

11. Limiting values

Table 13. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDA}	analog supply voltage		–0.3	+3.6	V
V_{DDD}	digital supply voltage		–0.3	+3.6	V
$V_{DD(regd)}$	regulated supply voltage	on pins VB_xx [1]	–0.3	+1.98	V
V_{XTAL_OUT}	voltage on pin XTAL_OUT	[1]	–0.3	VB_xx + 0.3	V
V_{XTAL_IN}	voltage on pin XTAL_IN	[1]	–0.3	VB_xx + 0.3	V
V_{RF_IO}	voltage on pin RF_IO	[1]	–0.3	VB_xx + 0.3	V
V_{VREF}	voltage on pin VREF		–0.3	V_{DDA} + 0.3	V
V_{ADCx}	voltage on pin ADCX	[2]	–0.3	V_{DDA} + 0.3	V
V_{IBIAS}	voltage on pin IBIAS		–0.3	V_{DDA} + 0.3	V
$V_{IO(dig)}$	digital input/output voltage	on pins DIOx [3]	–0.3	V_{DDD} + 0.3	V

Table 13. Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
T_{stg}	storage temperature		–40	+150	°C
V_{ESD}	electrostatic discharge voltage	HBM [4]	-	2000	V
		CDM [5]	-	1000	V

[1] With xxx = SYNTH or VCO or RF2 or RF1 or DIG.

[2] With x = 0 or 1.

[3] With x = 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 17 or 18.

[4] Testing for HBM discharge is performed as specified in JEDEC Standard JS-001.

[5] Testing for CDM discharge is performed as specified in JEDEC Standard JESD22-C101.

12. Recommended operating conditions

Table 14. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDA}	analog supply voltage	[1]	2	3.6	V
V_{DDD}	digital supply voltage		2	3.6	V
T_{amb}	ambient temperature	standard range	–40	+125	°C

[1] To reach the maximum TX power, 2.8 V is the minimum.

13. Thermal characteristics

Table 15. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		-	29.9	-	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		-	19	-	K/W
$T_{j(max)}$	maximum junction temperature		-	-	130	°C

14. Characteristics

14.1 DC current

Table 16. Active processing

V_{DD} = 2 V to 3.6 V; T_{amb} = −40 °C to +125 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	supply current	CPU in doze mode; analog and digital [1]				
		with radio in receive mode; maximum input level at 10 dBm; high-performance mode	-	14.8	-	mA
		with radio in receive mode; maximum input level at −2 dBm; low-power mode	-	12.7	-	mA
		with radio in transmit mode 10 dBm [2]	-	22.5	-	mA
		with radio in transmit mode 8.5 dBm [2]	-	19.6	-	mA
		with radio in transmit mode 3 dBm	-	14	-	mA
		without radio	-	2	-	mA
		CPU processing at: [3]				
		32 MHz	-	2.62	-	mA
		16 MHz	-	1.54	-	mA
		8 MHz	-	0.89	-	mA
		4 MHz	-	0.49	-	mA
		2 MHz	-	0.28	-	mA
		1 MHz	-	0.15	-	mA
$I_{DD(ADC)}$	ADC supply current	[4] [5]	-	390	-	µA
$I_{DD(comp)}$	comparator supply current	[5]				
		operating mode	-	70	-	µA
		low-power mode	-	0.62	-	µA
$I_{DD(UART)}$	UART supply current	per UART [5]	-	60	-	µA
$I_{DD(tmr)}$	timer supply current	per timer [5]	-	54	-	µA
$I_{DD(sintf)}$	serial interface supply current	SPI-bus supply current [5]	-	40	-	µA

[1] Doze mode = CPU is not clocked.

[2] To reach the maximum TX power, 2.8 V is the minimum.

[3] Digital consumption only. When in CPU doze, the current related to CPU speed is not consumed. This value should be added to the CPU in doze mode supply current value.

[4] Temperature sensor and battery measurements require ADC.

[5] These numbers should be added to I_{DD} if the feature is being used.

Table 17. Sleep mode

V_{DD} = 2 V to 3.6 V; T_{amb} = −40 °C to +125 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(IO)}$	I/O supply current	analog and digital supply current; with IO and 1 × RC oscillator timer wake-up; T_{amb} = 25 °C [1]	-	0.61	-	µA
$I_{DD(xtal)}$	crystal oscillator supply current	for 32 kHz internal RC oscillator [1]				
		HIGH current	-	0.76	-	µA
		LOW current	-	0.40	-	µA
$I_{ret(RAM)}$	RAM retention current	T_{amb} = 25 °C [2]	-	0.6	-	µA
$I_{DD(comp)}$	comparator supply current	low-power mode [1][2][3]	-	0.62	-	µA

[1] Waiting on IO event.

[2] RAM and comparator supply currents should be added to $I_{DD(IO)}$ if the feature is being used.

[3] Reduced response time.

Table 18. Deep sleep mode

V_{DD} = 2 V to 3.6 V; T_{amb} = −40 °C to +125 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	supply current	analog and digital supply current; deep sleep mode; measured at 25 °C [1]	-	100	-	nA

[1] Waiting on chip RESET or IO event.

14.2 IO characteristics

Table 19. IO characteristics

V_{DD} = 2 V to 3.6 V; T_{amb} = −40 °C to +125 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{pu(int)(DIO)}$	internal pull-up resistance on pins DIOx[1]		40	50	60	kΩ
$R_{pu(int)(RESET\_N)}$	internal pull-up resistance on pin RESET_N	V_{DD} = 3.6 V	300	425	550	kΩ
		V_{DD} = 3.0 V	400	500	700	kΩ
		V_{DD} = 2.2 V	650	830	1100	kΩ
		V_{DD} = 2.0 V	750	950	1350	kΩ
Digital voltages						
IO						
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{IL}	LOW-level input voltage		−0.3	-	$0.27V_{DD}$	V
$V_{hys(i)}$	input hysteresis voltage		200	310	400	mV
Output on pins DIOx[1]						
V_{OH}	HIGH-level output voltage	6.8 mA load	V_{DD} − 0.4	-	V_{DD}	V
V_{OL}	LOW-level output voltage	6.8 mA load	0	-	0.4	V

Table 19. IO characteristics *...continued*

V_{DD} = 2 V to 3.6 V; T_{amb} = −40 °C to +125 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Currents						
I_{LIL}	LOW-level input leakage current	V_{DD} = 3.6 V; T_{amb} = 25 °C	-	2	-	nA
I_{LIH}	HIGH-level input leakage current	V_{DD} = 3.6 V; T_{amb} = 25 °C	-	2	-	nA

[1] With x = 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 17 or 18.

14.3 AC characteristics

14.3.1 Reset and Supply Voltage Monitor

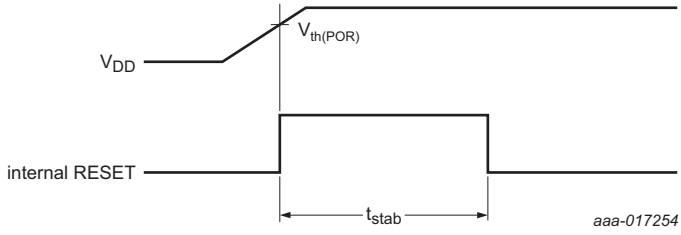


Fig 45. Internal Power-On Reset without showing Brown-Out

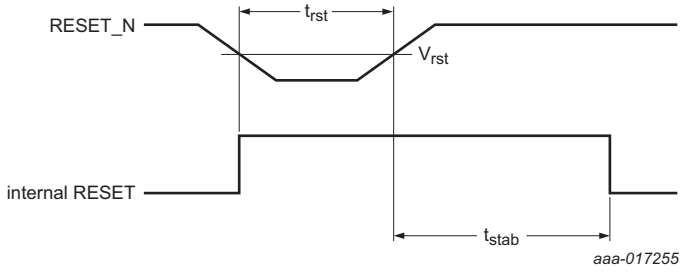


Fig 46. Externally applied reset

Table 20. Externally applied reset

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{rst}	reset time	external reset pulse width to initiate reset sequence [1]	1	-	-	µs
V_{rst}	reset voltage	external threshold voltage [2]	$0.7V_{DD}$	-	-	V
$V_{th(POR)}$	power-on reset threshold voltage	rise time > 10 ms				
		rising	-	1.44	-	V
		falling	-	1.41	-	V
α_{spike}	spike rejection	depth of pulse to trigger reset				
		1 µs square wave	-	1.2	-	V
		10 µs triangular wave	-	1.3	-	V
t_{stab}	stabilization time	reset [3]	-	180	-	µs
I_{DD}	supply current	chip current when held in reset	-	6	-	µA

Table 20. Externally applied reset *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{rst(bo)}$	brownout reset current		-	80	-	nA
V_{th}	threshold voltage	supply threshold voltage monitor; configurable in eight levels				
			1.86	1.94	2.00	V
			1.92	2.00	2.06	V
			2.02	2.10	2.16	V
			2.11	2.20	2.27	V
			2.21	2.30	2.37	V
			2.30	2.40	2.47	V
			2.59	2.70	2.78	V
			2.88	3.00	3.09	V
V_{hys}	hysteresis voltage	supply voltage monitor; corresponding to the eight threshold levels				
			-	37	-	mV
			-	38	-	mV
			-	45	-	mV
			-	52	-	mV
			-	58	-	mV
			-	65	-	mV
			-	82	-	mV
			-	100	-	mV

[1] Assumes internal pull-up resistor value of 100 kΩ worst case and ≈5 pF external capacitance.

[2] Minimum voltage to avoid being reset.

[3] Time from release of reset to start of executing of bootloader code from internal Flash. An extra 15 µs is incurred if the BOR circuit has been activated (e.g. if the supply voltage has been ramped up from 0 V).

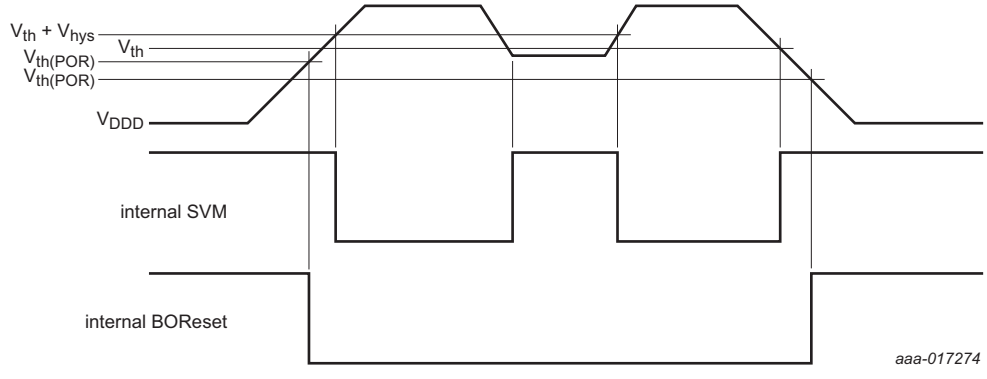
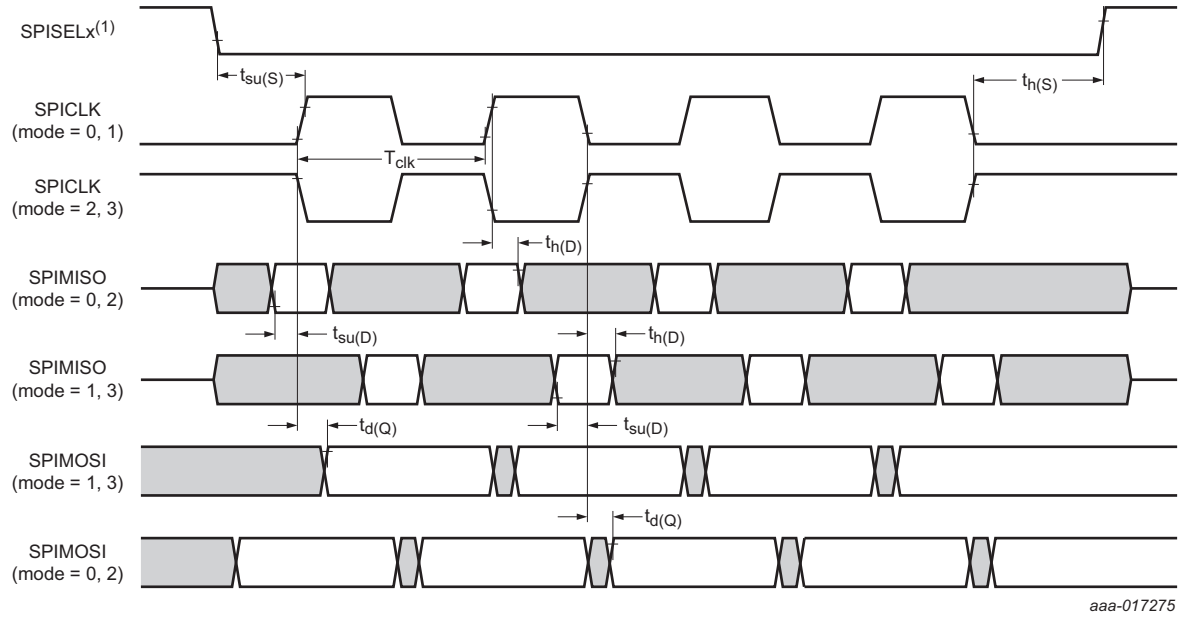


Fig 47. Brown-Out Reset followed by Supply Voltage Monitor trigger

14.3.2 SPI-bus master timing



(1) With x = 0, 1 or 2.

Fig 48. SPI-bus master timing

Table 21. SPI-bus master timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{clk}	clock period		62.5	-	-	ns
$t_{su(D)}$	data input set-up time	for SPI-bus clock on pin 23 DO0				
		3.3 V	16.7	-	-	ns
		2.8 V	18.2	-	-	ns
		2.0 V	21	-	-	ns
		for SPI-bus clock on pin 36 DIO11				
		3.3 V	20.2	-	-	ns
		2.8 V	23.3	-	-	ns
		2.0 V	25.3	-	-	ns
$t_{h(D)}$	data input hold time		0	-	-	ns
$t_{d(Q)}$	data output delay time	on SPIMOSI	-	-	15	ns
$t_{su(S)}$	chip select set-up time		60	-	-	ns
$t_{h(S)}$	chip select hold time	SPICLK = 16 MHz	30	-	-	ns
		SPICLK < 16 MHz; mode = 0 or 2	0	-	-	ns
		SPICLK < 16 MHz; mode = 1 or 3	60	-	-	ns

14.3.3 SPI-bus slave timing

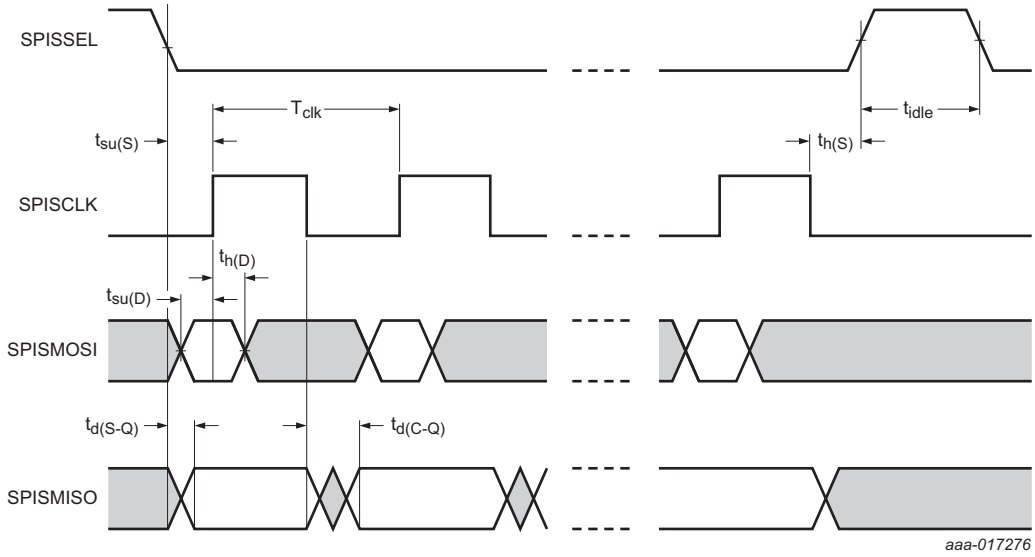


Fig 49. SPI-bus slave timing

Table 22. SPI-bus slave timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{clk}	clock period		125	-	-	ns
t_{idle}	idle time		125	-	-	ns
$t_{su(D)}$	data input set-up time		10	-	-	ns
$t_{h(D)}$	data input hold time		10	-	-	ns
$t_{d(C-Q)}$	clock to data output delay time	SPISCLK falling edge to SPISMISO output delay time	-	-	30	ns
$t_{d(S-Q)}$	chip select to data output delay time	SPISSEL falling edge to SPISMISO output delay time	-	-	30	ns
$t_{su(S)}$	chip select set-up time	SPISSEL falling edge to SPISCLK rising edge delay time	30	-	-	ns
$t_{h(S)}$	chip select hold time	SPISCLK falling edge to SPISSEL rising edge delay time	30	-	-	ns

14.3.4 I²C-bus interface

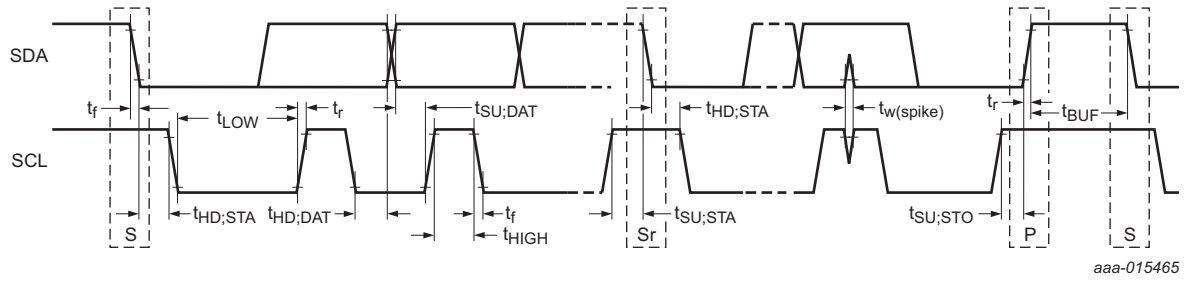


Fig 50. I²C-bus interface timing

Table 23. I²C-bus interface

Symbol	Parameter	Conditions	Standard mode		Fast mode		Unit
			Min	Max	Min	Max	
f_{clk}	clock frequency	SCL; DIO4; pin 21	0	100	0	400	kHz
$t_{HD;STA}$	hold time (repeated) START condition	[1]	4	-	0.6	-	µs
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock		4	-	0.6	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	µs
$t_{SU;DAT}$	data set-up time	data setup time SDA	0.25	-	0.1	-	µs
$t_{HD;DAT}$	data hold time	data hold time SDA	0[2]	-	0[2]	-	µs
t_r	rise time	rise time SDA and SCL [3]	-	1000	20 + 0.1 Cb	300	ns
t_f	fall time	fall time SDA and SCL [3]	-	300	20 + 0.1 Cb	300	ns
$t_{SU;STO}$	set-up time for STOP condition		4	-	0.6	-	µs
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	µs
$t_{w(spike)}$	spike pulse width	pulse width of spikes that will be suppressed by input filters	-	60	-	60	ns
C_b	capacitive load for each bus line		-	400	-	400	pF
V_{nL}	noise margin at the LOW level	noise margin at the LOW level for each connected device (including hysteresis)	$0.1V_{DD}$	-	$0.1V_{DD}$	-	V
V_{nH}	noise margin at the HIGH level	noise margin at the HIGH level for each connected device (including hysteresis)	$0.2V_{DD}$	-	$0.2V_{DD}$	-	V

[1] After this period, the first clock pulse is generated.

[2] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH(min)}$ of the CLK signal) to bridge the undefined region of the falling edge of CLK.

[3] Following the I²C-bus specifications.

14.3.5 Wake-up timings

Table 24. Wake-up timings

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{startup}$	start-up time	CPU start up time; time for crystal to stabilize ready to run CPU; reached oscillator amplitude threshold. Default bias current	-	0.87	-	ms
		radio start-up time; time for crystal to stabilize ready for radio activity	-	1.10	-	ms
		from reset RESET_N pin, BOR or SVM	-	310	-	µs
t_{wake}	wake-up time	from deep sleep mode or sleep mode without RAM retention	-	300	-	µs
		from sleep mode with RAM retention	-	210	-	µs
		from CPU Doze mode	-	7	-	µs

14.3.6 Band gap reference

Table 25. Band gap reference

V_{DD} = 2 V to 3.6 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DDA(bg)}$	band gap analog supply voltage		1.198	1.235	1.260	V

14.3.7 Analog to Digital Converters

Table 26. Analog to Digital Converters

V_{DD} = 3 V; V_{ref} = 1.2 V; T_{amb} = -40 °C to +125 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_i	input voltage	switchable [1]	0.04	-	$2V_{ref}$	V
V_{ref}	reference voltage	internal [2]	-	-	-	V
		external; allowable range into VREF pin	-	1.2	-	V
I_{ADCx}	current on pins ADCx[3]		-	400	-	µA
INL	integral non-linearity	T_{amb} = –40 °C to +85 °C	-	±1.6	-	LSB
		T_{amb} = –40 °C to +125 °C	-	±1.8	-	LSB
DNL	differential non-linearity		-	±0.5	-	LSB
E_O	offset error	0 to V_{ref} range	-	–10	-	mV
		0 to 2 × V_{ref} range	-	–20	-	mV
E_G	gain error	0 to V_{ref} range	-	–10	-	mV
		0 to 2 × V_{ref} range	-	–20	-	mV
$f_{clk(int)}$	internal clock frequency	16 MHz input clock [4]				
		÷ 16	-	1	-	MHz
		÷ 32	-	0.5	-	MHz
		÷ 64	-	0.25	-	MHz
t_{conv}	conversion time	programmable	9.5	-	148	µs
$C_{i(a)}$	analog input capacitance	in series with 5 kΩ resistor	-	8	-	pF

[1] See Section 9.16.1.1.

[2] See Section 14.3.6.

[3] With x = 1, 2, 3, 4, 5 or 6.

[4] Number of internal clock periods to sample input (programmable at 2, 4, 6 or 8).

14.3.8 Comparator

Table 27. Comparator

V_{DD} = 2 V to 3.6 V; T_{amb} = −40 °C to +125 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{resp}	response time	operating mode [1]	-	90	-	ns
		low-power mode [2]	-	2.2	-	ns
$t_{res(tot)}$	total response time	operating mode; including delay to interrupt controller [3]	-	130	-	ns
V_{hys}	hysteresis voltage	programmable in 3 steps	-	10	-	mV
			-	20	-	mV
			-	40	-	mV
V_{ref}	reference voltage	[4]	-	-	-	V
$V_{I(cm)}$	common-mode input voltage		0	-	V_{DD}	V
I_I	input current	operating mode	-	73	-	µA
		low-power mode	-	0.8	-	µA

[1] ±250 mV overdrive; 10 pF load.

[2] ±250 mV overdrive; no digital delay.

[3] Digital delay can be up to a maximum of two 16 MHz clock periods.

[4] See Section 14.3.6.

14.3.9 32 kHz RC oscillator

Table 28. 32 kHz RC oscillator

V_{DD} = 2 V to 3.6 V; T_{amb} = −40°C to +125°C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Δf_{xtal}	crystal frequency accuracy	32 kHz clock uncalibrated accuracy; without temperature and voltage variation [1]	32 − 21%	32	32 + 53%	kHz
		calibration done in operating mode; calibrated 32 kHz accuracy; for a 1 s sleep period calibrating over 20 x 32 kHz clocks periods	-	±300	-	ppm
		calibration done in low-power mode; calibrated 32 kHz accuracy; for a 1 s sleep period calibrating over 20 x 32 kHz clocks periods	-	±600	-	ppm

[1] Measured at 3 V and 25 °C.

14.3.10 32 kHz crystal oscillator

Table 29. 32 kHz crystal oscillator

V_{DD} = 2 V to 3.6 V; T_{amb} = −40°C to +125°C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(xtal)}$	crystal oscillator supply current	of cell and counter-logic [1]	-	0.6	-	µA
$t_{startup}$	start-up time	[2]	-	0.6	-	s

[1] This is sensitive to the ESR of the crystal, V_{DD} and total capacitance at each pin.

[2] Assuming crystal with ESR of less than 40 Ω, C_L = 9 pF and external capacitances = 15 pF (V_{DD} / 2 mV(p-p).

When external 32 kHz oscillator is used, external capacitances of 15 pF are implemented. Total external capacitance needs to be 2 × C_L, allowing for stray capacitance from chip, package and PCB (C_L = 9 pF).

14.3.11 32 MHz crystal oscillator

Table 30. 32 MHz crystal oscillator

V_{DD} = 2 V to 3.6 V; T_{amb} = −40°C to +125°C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(xtal)}$	crystal oscillator supply current	of cell and counter-logic [1]	-	275	-	µA
$t_{startup}$	start-up time	[2]	-	0.87	-	ms

[1] Excluding band gap ref.

[2] Assuming crystal with ESR of less than 40 Ω, C_L = 9 pF and external capacitances = 12 pF (V_{DD} / 2 mV(p-p).

When external 32 MHz oscillator is used, external capacitances of 12 pF are implemented. Total external capacitance needs to be 2 × C_L, allowing for stray capacitance from chip, package and PCB (C_L = 9 pF).

14.3.12 High-speed RC oscillator

Table 31. High-speed RC oscillator

V_{DD} = 2 V to 3.6 V; T_{amb} = −40°C to +125°C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(xtal)}$	crystal oscillator supply current	of cell	-	145	-	µA
f_{osc}	oscillator frequency	uncalibrated	26.1 − 16%	26.1	26.1 + 18%	MHz
		calibrated	32.1 − 4%	32.1	32.1 + 5%	MHz
$t_{startup}$	start-up time		-	2.4	-	µs

14.3.13 Temperature sensor

Table 32. Temperature sensor

V_{DD} = 2 V to 3.6 V; T_{amb} = −40°C to +125°C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{sen}	sensor temperature		−40	-	+125	°C
G_{sen}	sensor gain		-	−1.66	-	mV/°C
ΔT_{sen}	sensor temperature accuracy		-	±7	-	°C
V_o	output voltage	[1]	540	-	840	mV
V_{sen}	sensor voltage	at V_{DD} = 3.0 V and T_{amb} = 25 °C	-	720	-	mV

[1] Includes absolute variation due to manufacturing and temperature.

14.3.14 Non-volatile memory

Table 33. Non-volatile memory

V_{DD} = 2 V to 3.6 V; T_{amb} = −40°C to +125°C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{endu}	endurance	Flash; program/erase [1]	10	100	-	kCycle
		EEPROM; program/erase [2]	100	1000	-	kCycle
t_{er}	erase time	Flash; one sector	-	100	-	ms
t_{prog}	programming time	Flash; per page of 256 bytes	-	1.0	-	ms
t_{er}	erase time	EEPROM; one 64-byte page	-	1.8	-	ms
t_{prog}	programming time	EEPROM; between 1 byte and 64 bytes	-	1.1	-	ms
t_{ret}	retention time	powered; Flash and EEPROM	10	-	-	year

[1] See Section 9.3.2.

[2] See Section 9.3.4.

14.3.15 Radio transceiver

This JN517x meets all the requirements of the IEEE802.15.4 standard over 2.0 V to 3.6 V and offers the improved RF characteristics shown in Table 34. All RF characteristics are measured single ended.

This part also meets the following regulatory body approvals, when used with NXP's Module Reference Designs. Compliant with *FCC part 15 rules, IC Canada and ETSI ETS 300-328*, refer to the JN517x Module Reference Design package on the Wireless Connectivity area of the NXP web site Ref. 2.

The PCB schematic and layout rules detailed in Section 15 must be followed. Failure to do so will likely result in the JN517x failing to meet the performance specification detailed herein and worst case may result in device not functioning in the end application.

Table 34. RF port characteristics

Single-ended; Impedance = 50 Ω[1]; V_{DD} = 2 V to 3.6 V; T_{amb} = −40°C to +125°C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{range}	frequency range		2.4	-	2.485	GHz
V_{ESD}	electrostatic discharge voltage	pin 13	-	-	-	
		HBM	-	2	-	kV
		CDM	-	500	-	V

[1] With external matching inductors and assuming PCB layout as inSection 15.1.1.

Table 35. Radio transceiver characteristics: +25 °C

V_{DD} = 2 V to 3.6 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Receiver						
S_{RX}	receiver sensitivity	nominal for 1 % PER, as per 802.15.4	-	−96	−93.5	dBm

Table 35. Radio transceiver characteristics: +25 °C *…continued*

V_{DD} = 2 V to 3.6 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{i(RX)(max)}$	maximum receiver input power	1 % PER, measured as sensitivity; supply current at 14.8 mA; high-performance mode	-	10	-	dBm
		1 % PER, measured as sensitivity; supply current at 12.7 mA; low-power mode	-	−2	-	dBm
α_{ch}	channel rejection	1 % PER, with wanted signal 3 dB, above sensitivity as per 802.15.4				
		modulated interferer[1][2]				
		−1 channel	-	19	-	dBc
		+1 channel	-	34	-	dBc
		−2 channel	-	40	-	dBc
		+2 channel	-	44	-	dBc
		co-channel	-	−7	-	dBc
		CW interferer[1][2]				
		−1 channel	-	25	-	dBc
		+1 channel	-	50	-	dBc
		−2 channel	-	57	-	dBc
		+2 channel	-	60	-	dBc
α_{ib}	in-band rejection	1 % PER with wanted signal 3 dB above sensitivity; 2.4 GHz to 2.4835 GHz; modulated interferers at 3 channel separation [1]	-	43	-	dBc
α_{oob}	out-of-band rejection	1 % PER with wanted signal 3 dB above sensitivity [1]				
		all frequencies except wanted/2 which is 8 dB lower	-	45	-	dBc
		3G frequency at 2.1 GHz	-	−5	-	dBm
		LTE frequency at 2.5 GHz	-	−18	-	dBm
$P_{sp(RX)}$	receiver spurious power	measured conducted into 50 Ω				
		30 MHz to 1 GHz	-	-	−70	dBm
		1 GHz to 12 GHz	-	-	−70	dBm
$P_{L(lo)}$	local oscillator leakage power		-	-	−55	dBm
IMP	intermodulation protection	1 % PER at with wanted signal 3 dB above sensitivity; modulated interferers at 3 and 6 channel separation [1]	-	46	-	dB
$\Delta\alpha_{RSSI}$	RSSI variation	−95 dBm to −10 dBm; available through JN517x Integrated Peripherals API	−4	-	+4	dB
Transmitter						
P_o	output power	PA = 5 and Att. 2.5 dB OFF [3]	-	10	-	dBm
$P_{o(cr)}$	control range output power	in 6 major steps and then 4 fine steps [4]	-	−42	-	dB

Table 35. Radio transceiver characteristics: +25 °C *…continued*

V_{DD} = 2 V to 3.6 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{sp(TX)}$	transmitter spurious power	measured conducted into 50 Ω				
		30 MHz to 1 GHz	-	-	–65	dBm
		1 GHz to 12.5 GHz (harmonic H2)	-	-	–36	dBm
		exceptions				
		1.8 GHz to 1.9 GHz	-	-	–65	dBm
		5.15 GHz to 5.3 GHz	-	-	–65	dBm
EVM	error vector magnitude	at maximum output power	-	8	-	%
EVM_{offset}	error vector magnitude offset	at maximum output power	-	3	4.5	%
PSD	power spectral density	relative density at greater than 3.5 MHz offset [5]	-	–38	–20	dBc
		absolute density at greater than 3.5 MHz offset [5]	-	–32	-	dBm

[1] Blocker rejection is defined as the value, when 1 % PER is seen with the wanted signal 3 dB above sensitivity, as per IEE802.15.4.

[2] Channels 11, 17, 24 low/high values reversed.

[3] To reach the maximum TX power, 2.8 V is the minimum on V_{DDA}.

[4] Up to an extra 2.5 dB of attenuation is available if required.

[5] See IEEE802.15.4.

Table 36. Radio transceiver characteristics: –40 °C

V_{DD} = 2 V to 3.6 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Receiver						
S_{RX}	receiver sensitivity	nominal for 1 % PER, as per 802.15.4	-	–96.5	-	dBm
$P_{i(RX)(max)}$	maximum receiver input power	1 % PER, measured as sensitivity; supply current at 14.8 mA; high-performance mode	-	10	-	dBm
		1 % PER, measured as sensitivity; supply current at 12.7 mA; low-power mode	-	–2	-	dBm
α_{ch}	channel rejection	1 % PER, with wanted signal 3 dB, above sensitivity as per 802.15.4				
		modulated interferer[1][2]				
		–1 channel	-	19	-	dBc
		+1 channel	-	34	-	dBc
		–2 channel	-	40	-	dBc
		+2 channel	-	44	-	dBc
		co-channel	-	–7	-	dBc
α_{ib}	in-band rejection	1 % PER with wanted signal 3 dB above sensitivity; 2.4 GHz to 2.4835 GHz; modulated interferers at 3 channel separation [1]	-	43	-	dBc
α_{oob}	out-of-band rejection	1 % PER with wanted signal 3 dB above sensitivity; all frequencies except wanted/2 which is 8 dB lower [1]	-	45	-	dBc

Table 36. Radio transceiver characteristics: –40 °C *…continued*

V_{DD} = 2 V to 3.6 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{sp(RX)}$	receiver spurious power	measured conducted into 50 Ω				
		30 MHz to 1 GHz	-	-	–70	dBm
		1 GHz to 12 GHz	-	-	–70	dBm
$P_{L(lo)}$	local oscillator leakage power		-	-	–54	dBm
IMP	intermodulation protection	1 % PER at with wanted signal 3 dB above sensitivity; modulated interferers at 3 and 6 channel separation [1]	-	45	-	dB
$\Delta\alpha_{RSSI}$	RSSI variation	–95 dBm to –10 dBm; available through JN517x Integrated Peripherals API	-	±4	-	dB
Transmitter						
P_o	output power	PA = 5 and Att. 2.5 dB OFF [3]	-	10	-	dBm
$P_{o(cr)}$	control range output power	in 6 major steps and then 4 fine steps [4]	-	–42	-	dB
$P_{sp(TX)}$	transmitter spurious power	measured conducted into 50 Ω				
		30 MHz to 1 GHz	-	-	–65	dBm
		1 GHz to 12.5 GHz (harmonic H2)	-	-	–36	dBm
		exceptions				
		1.8 GHz to 1.9 GHz	-	-	–65	dBm
		5.15 GHz to 5.3 GHz	-	-	–65	dBm
EVM	error vector magnitude	at maximum output power	-	8	-	%
EVM_{offset}	error vector magnitude offset	at maximum output power	-	3	-	%
PSD	power spectral density	relative density at greater than 3.5 MHz offset [5]	-	–38	-	dBc
		absolute density at greater than 3.5 MHz offset [5]	-	–32	-	dBm

[1] Blocker rejection is defined as the value, when 1 % PER is seen with the wanted signal 3 dB above sensitivity, as per IEE802.15.4.

[2] Channels 11, 17, 24 low/high values reversed.

[3] To reach the maximum TX power, 2.8 V is the minimum on V_{DDA}.

[4] Up to an extra 2.5 dB of attenuation is available if required.

[5] See IEEE802.15.4.

Table 37. Radio transceiver characteristics: +125 °C

V_{DD} = 2 V to 3.6 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Receiver						
S_{RX}	receiver sensitivity	nominal for 1 % PER, as per 802.15.4	-	–94	-	dBm
$P_{i(RX)(max)}$	maximum receiver input power	1 % PER, measured as sensitivity; supply current at 14.8 mA; high-performance mode	-	5	-	dBm
		1 % PER, measured as sensitivity; supply current at 12.7 mA; low-power mode	-	–10	-	dBm

Table 37. Radio transceiver characteristics: +125 °C *…continued*

V_{DD} = 2 V to 3.6 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
α_{ch}	channel rejection	1 % PER, with wanted signal 3 dB, above sensitivity as per 802.15.4				
		modulated interferer[1][2]				
		–1 channel	-	18	-	dBc
		+1 channel	-	31	-	dBc
		–2 channel	-	38	-	dBc
		+2 channel	-	42	-	dBc
		co-channel	-	–7	-	dBc
α_{ib}	in-band rejection	1 % PER with wanted signal 3 dB above sensitivity; 2.4 GHz to 2.4835 GHz; modulated interferers at 3 channel separation [1]	-	41	-	dBc
α_{oob}	out-of-band rejection	1 % PER with wanted signal 3 dB above sensitivity; all frequencies except wanted/2 which is 8 dB lower [1]	-	42	-	dBc
$P_{sp(RX)}$	receiver spurious power	measured conducted into 50 Ω				
		30 MHz to 1 GHz	-	-	–70	dBm
		1 GHz to 12 GHz	-	-	–70	dBm
$P_{L(lo)}$	local oscillator leakage power		-	-	–56	dBm
IMP	intermodulation protection	1 % PER at with wanted signal 3 dB above sensitivity; modulated interferers at 3 and 6 channel separation [1]	-	45	-	dB
$\Delta\alpha_{RSSI}$	RSSI variation	–95 dBm to –10 dBm; available through JN517x Integrated Peripherals API	-	±4	-	dB
Transmitter						
P_o	output power	PA = 5 and Att. 2.5 dB OFF [3]	-	10	-	dBm
$P_{o(cr)}$	control range output power	in 6 major steps and then 4 fine steps [4]	-	–42	-	dB
$P_{sp(TX)}$	transmitter spurious power	measured conducted into 50 Ω				
		30 MHz to 1 GHz	-	-	–65	dBm
		1 GHz to 12.5 GHz (harmonic H2)	-	-	–36	dBm
		exceptions				
		1.8 GHz to 1.9 GHz	-	-	–65	dBm
		5.15 GHz to 5.3 GHz	-	-	–65	dBm
EVM	error vector magnitude	at maximum output power	-	8	-	%
EVM_{offset}	error vector magnitude offset	at maximum output power	-	3	-	%
PSD	power spectral density	relative density at greater than 3.5 MHz offset [5]	-	–38	-	dBc
		absolute density at greater than 3.5 MHz offset [5]	-	–32	-	dBm

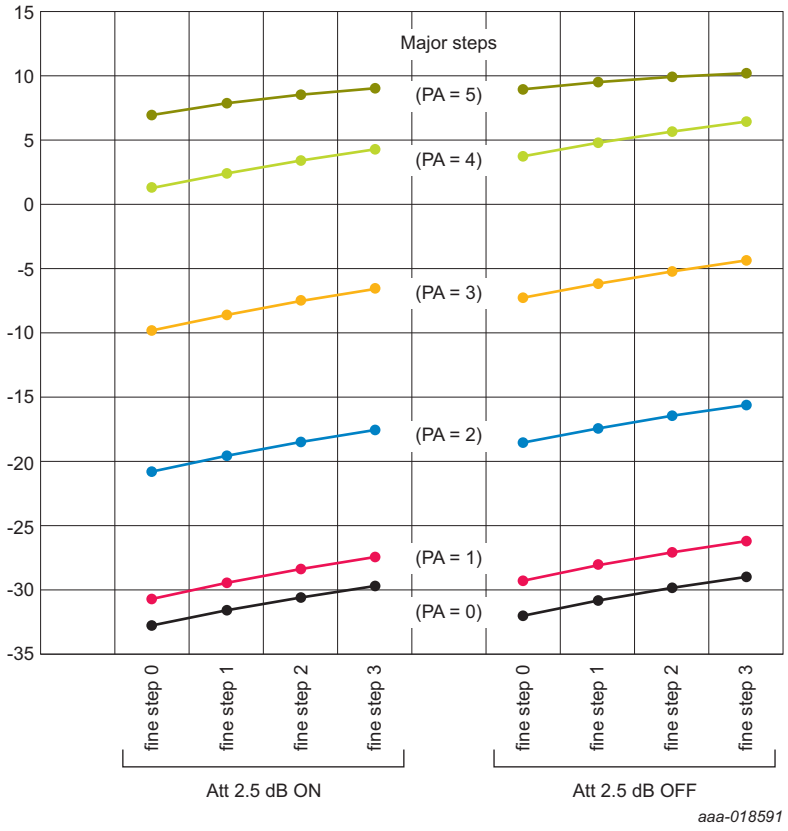
[1] Blocker rejection is defined as the value, when 1 % PER is seen with the wanted signal 3 dB above sensitivity, as per IEE802.15.4.

[2] Channels 11, 17, 24 low/high values reversed.

[3] To reach the maximum TX power, 2.8 V is the minimum on V_{DDA}.

[4] Up to an extra 2.5 dB of attenuation is available if required.

[5] See IEEE802.15.4.



At V_{DD} = 3 V and T_{amb} = 25 °C on channel 17. In complete temperature range and over all channels, min and max values equal nominal value ± 1 dB.

Fig 51. Typical control range output power

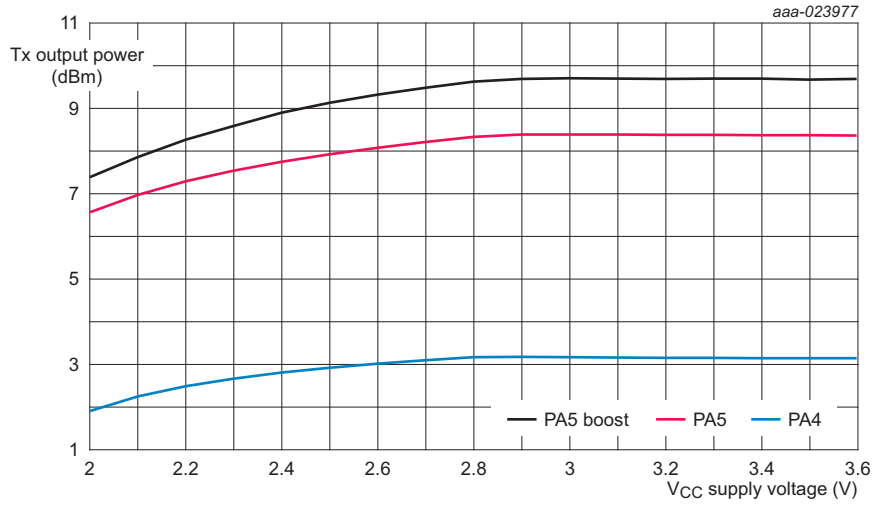


Fig 52. Typical transmit output power versus voltage

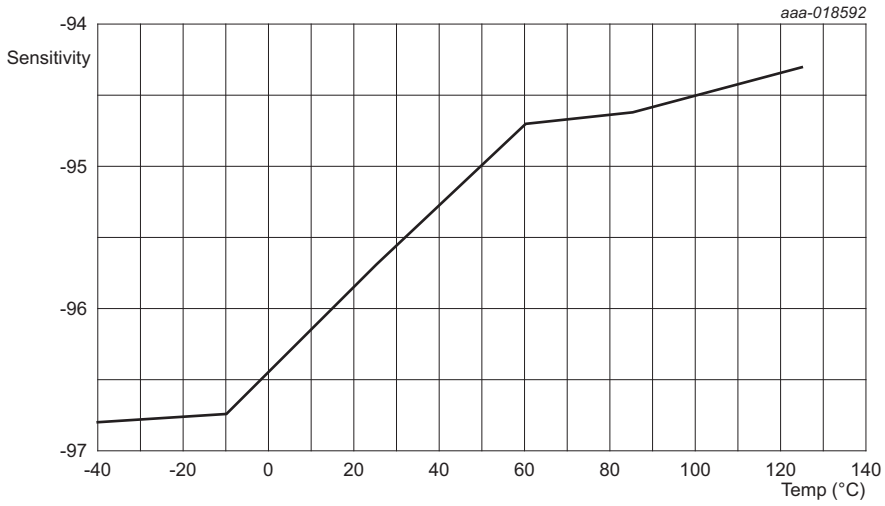


Fig 53. Typical receiver sensitivity versus temperature

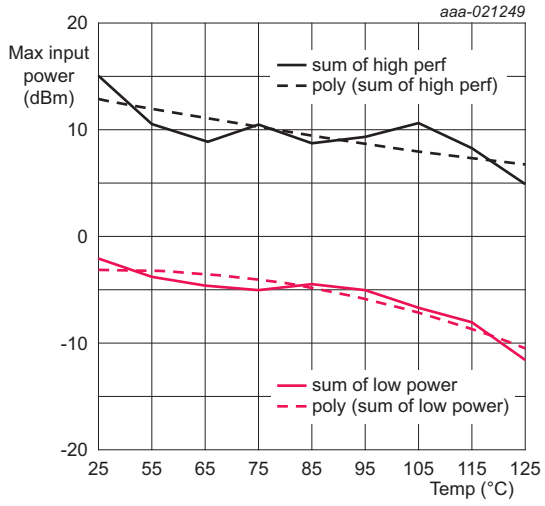


Fig 54. Maximum input level

15. Application information

15.1 JN517x module reference designs

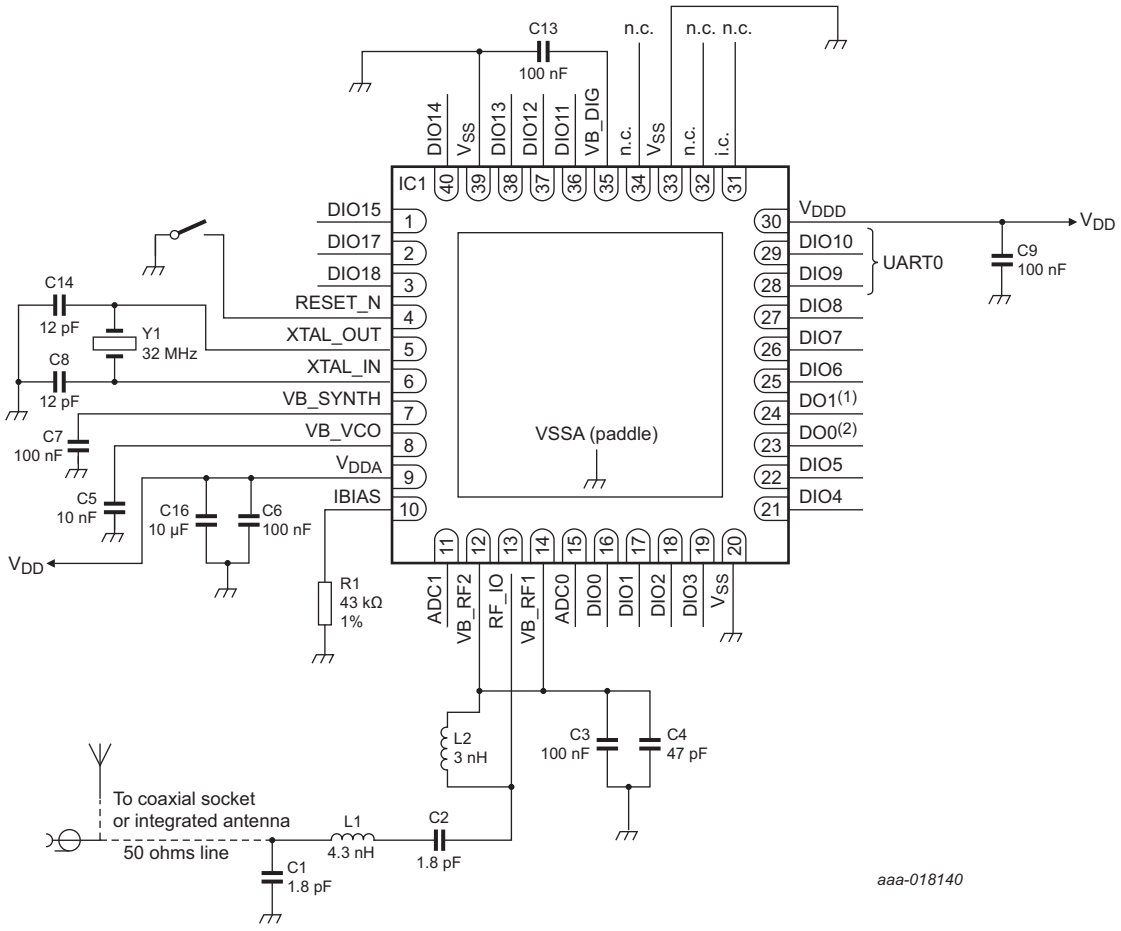
For customers wishing to integrate the JN517x device directly into their system, NXP provides a range of Module Reference Designs.

To ensure the correct performance, it is strongly recommended that where possible the design details provided by the reference designs, are used in their exact form for all end designs, this includes component values, pad dimensions, track layouts etc. In order to minimize all risks, it is recommended that the entire layout of the appropriate reference module, if possible, be replicated in the end design.

For full details, contact technical support.

15.1.1 Schematic diagrams

Schematic diagrams of the JN517x reference module is shown in Figure 55.



In that configuration, an external low ohmic supply voltage shall be delivered to V_{DDA} and V_{DDD} pins. V_{DDA} and V_{DDD} voltages shall be minimum 2.0 V and maximum 3.6 V, the supply source shall be connected directly to the device pins without any serial resistor.

To ease the layout implementation and improve the GND plane pins 31,32 and 34 can be connected to GND.

(1) The JN517x will enter UART programming mode if SPIMISO (DO1) pin 24 is low after RESET.

(2) The JN517x will enter JTAG programming mode if SPICLK (DO0) pin 23 is low after RESET.

Fig 55. JN517x module reference design using low voltage supply

Table 38. Components

Component	Function	Value		Remarks
C1	RF matching capacitor	1 pF		COG type
C2	AC coupling	1.8 pF	[1]	COG type
C3	VB RF decoupling	100 nF		locate less than 5 mm from IC1 pin 12 and IC1 pin 14
C4	VB RF decoupling	47 pF		locate less than 5 mm from IC1 pin 12 and IC1 pin 14
C5	VB VCO decoupling	10 nF		locate less than 5 mm from IC1 pin 8
C6	analog power decoupling	100 nF		locate less than 5 mm from IC1 pin 9
C7	VB synth decoupling	100 nF		locate less than 5 mm from IC1 pin 7
C8	crystal load capacitance	12 pF ± 5 % COG		adjacent to pin 6 and Y1 pin 3
C9	digital power decoupling	100 nF		adjacent to IC1 pin 30

Table 38. Components *…continued*

Component	Function	Value		Remarks
C13	VB Dig decoupling	100 nF		locate less than 5 mm from IC1 pin 35
C14	crystal load capacitance	12 pF ± 5 % COG		adjacent to pin 5 and Y1 pin 1
C16	power source decoupling	10 μF		
L1	RF matching inductor	4.3 nH	[1]	Murata LQP15MN4N3B02 can be used up to 85 °C; Murata LQG15MN4N3B02 can be used up to 125 °C
L2	load inductor	3 nH	[1]	Murata LQP15MN3N0B02 can be used up to 85 °C; Murata LQG15MN3N0B02 can be used up to 125 °C
R1	IBIAS resistor	43 kΩ 1%		
Y1	crystal	32 MHz; C_L = 9 pF		AEL X32M000000S039 or NDK NX3225SA EXS00A-CS08207 or NX2016SA 32 MHz EXS00A-CS07977 or Murata XR16GD32M000KYQ01R0 (2016) or Epson Toyocom X1E000021016700

[1] Must be copied directly from the reference design.

The paddle should be connected directly to ground. Any pads that require connection to ground should do so by connecting directly to the paddle.

15.1.2 Application diagram with Pi filter

Extra pi filter is recommended on RF path to insure a successful FCC certification regarding H2 spurs. This is the implemented solution for the NXP modules available on the market.

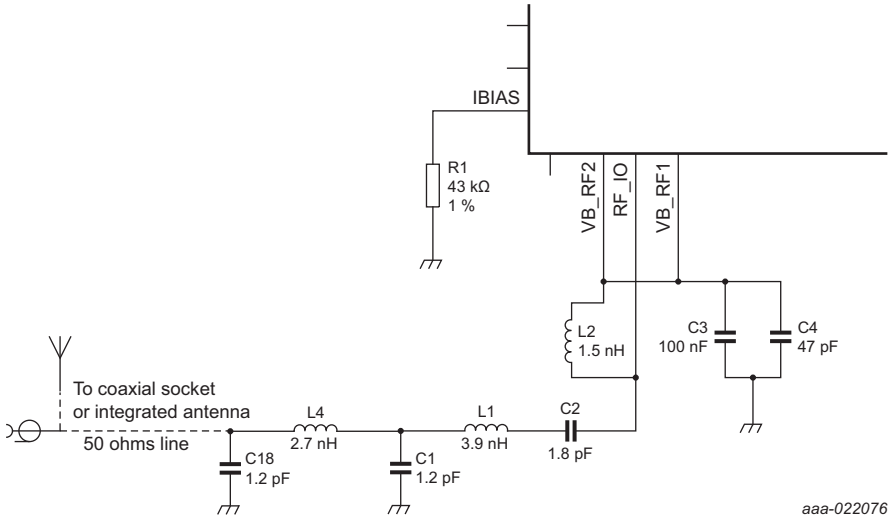


Fig 56. Application diagram with Pi filter

Table 39. Components

Component	Function	Value		Remarks
C1	RF matching capacitor	1.2 pF	[1]	COG type
C2	AC coupling	1.8 pF	[1]	COG type
C3	VB RF decoupling	100 nF		locate less than 5 mm from U1 pin 12 and U1 pin 14

Table 39. Components *…continued*

Component	Function	Value		Remarks
C4	VB RF decoupling	47 pF		locate less than 5 mm from U1 pin 12 and U1 pin 14
C18	RF filtering capacitor	1.2 pF		COG type
L1	RF matching inductor	3.9 nH	[1]	MuRata LQP15MN3N9B02 can be used up to 85 °C; MuRata LQG15MN3N9B02 can be used up to 125 °C
L2	load inductor	1.5 nH	[1]	MuRata LQP15MN1N5B02 can be used up to 85 °C; MuRata LQG15MN1N5B02 can be used up to 125 °C
L4	filtering inductor	2.7 nH	[1]	MuRata LQP15MN2N7B02 can be used up to 85 °C; MuRata LQG15MN2N7B02 can be used up to 125 °C
R1	IBIAS resistor	43 kΩ 1%		

[1] Must be copied directly from the reference design.

15.1.3 PCB design and reflow profile

PCB and land pattern designs are key to the reliability of any electronic circuit design.

The Institute for Interconnecting and Packaging Electronic Circuits (IPC) defines a number of standards for electronic devices. One of these is the "Surface Mount Design and Land Pattern Standard" IPC-SM-782 commonly referred to as “IPC782". This specification defines the physical packaging characteristics and land patterns for a range of surface-mounted devices. IPC782 is also a useful reference document for general surface mount design techniques, containing sections on design requirements, reliability and testability. NXP strongly recommends that this be referred to when designing the PCB.

NXP also provides an Application Note *AN10366, “HVQFN application information”*, which describes the reflow soldering process, refer also to Section 18.

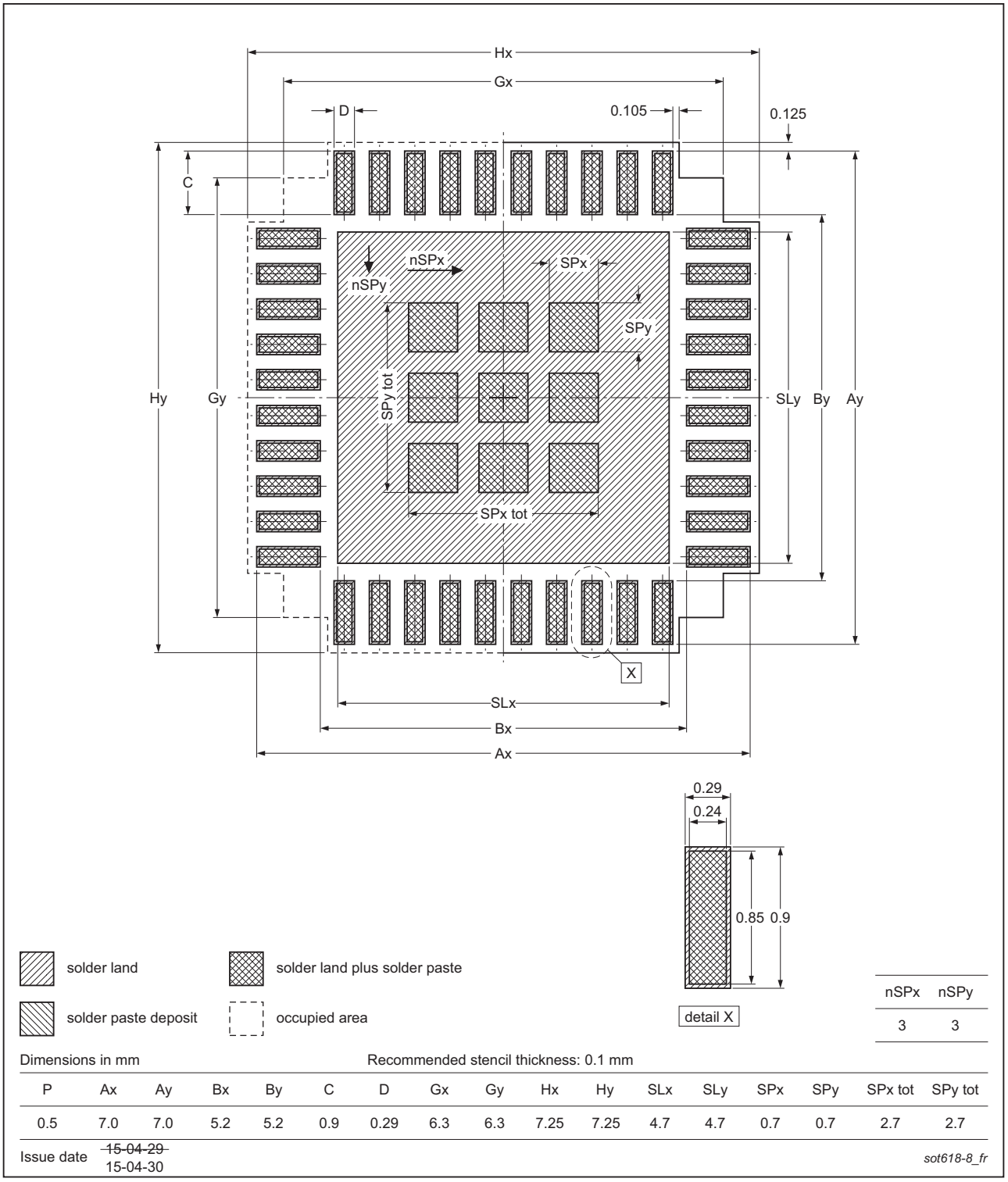
15.1.4 Moisture sensitivity level (MSL)

If there is moisture trapped inside a package, and the package is exposed to a reflow temperature profile, the moisture may turn into steam, which expands rapidly. This may cause damage to the inside of the package (delamination), and it may result in a cracked semiconductor package body (the popcorn effect). A package’s MSL depends on the package characteristics and on the temperature it is exposed to during reflow soldering, refer also to Section 18.

Depending on the damage after this test, an MSL of 1 (not sensitive to moisture) to 6 (very sensitive to moisture) is attached to the semiconductor package.

16. Footprint information for reflow soldering

Footprint information for reflow soldering of HVQFN40 package **SOT618-8**



nSPx	nSPy
3	3

Dimensions in mm — Recommended stencil thickness: 0.1 mm

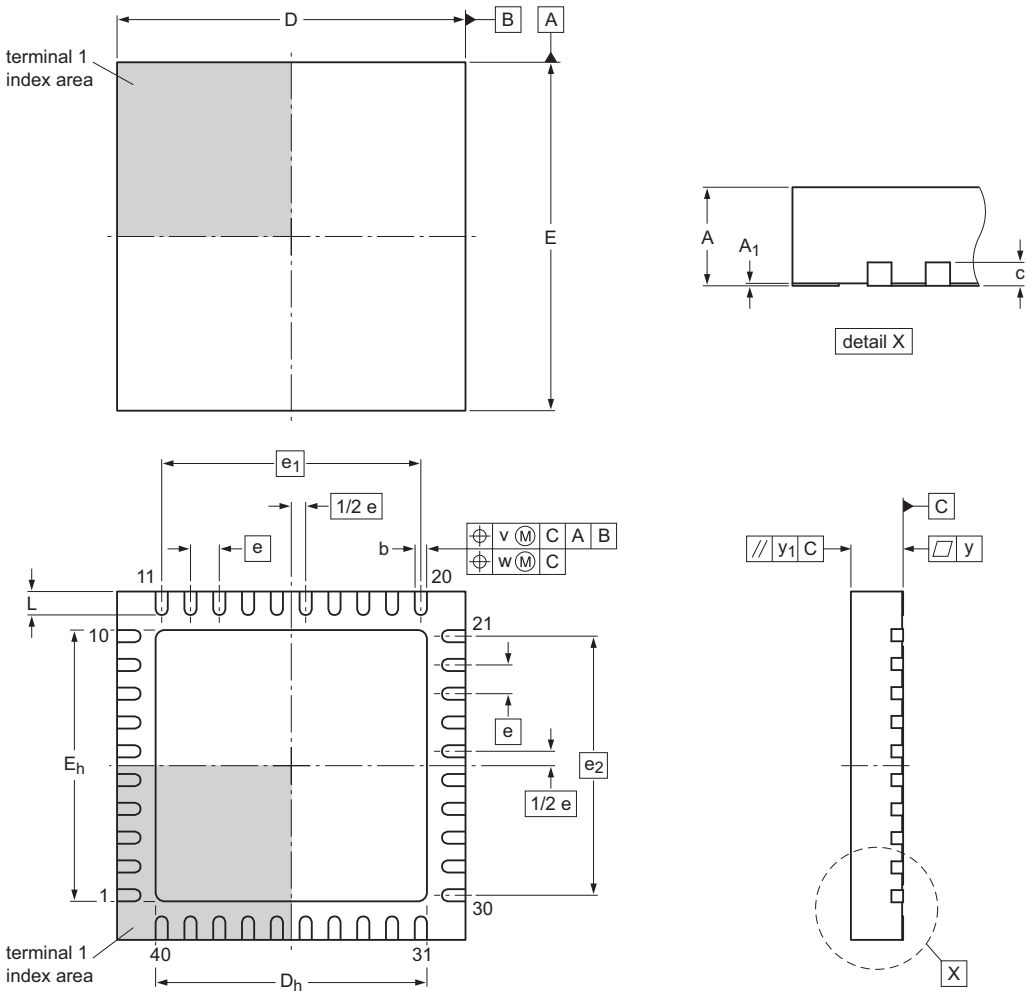
P	Ax	Ay	Bx	By	C	D	Gx	Gy	Hx	Hy	SLx	SLy	SPx	SPy	SPx tot	SPy tot
0.5	7.0	7.0	5.2	5.2	0.9	0.29	6.3	6.3	7.25	7.25	4.7	4.7	0.7	0.7	2.7	2.7

Issue date ~~15-04-29~~ 15-04-30 *sot618-8_fr*

Fig 57. Reflow soldering information for the HVQFN40 package

17. Package outline

HVQFN40: plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 x 6 x 0.85 mm **SOT618-8**



Dimensions

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
	max	1.00	0.05	0.30		6.1	4.85	6.1	4.85				0.5				
mm	nom	0.85	0.02	0.21	0.2	6.0	4.70	6.0	4.70	0.5	4.5	4.5	0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		5.9	4.55	5.9	4.55				0.3				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot618-8_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT618-8		MO-220	- - -			~~13-11-19~~ 14-01-16

Fig 58. Package outline SOT618-8 HVQFN40

18. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

18.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

18.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

18.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

18.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 59) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 40 and 41

Table 40. SnPb eutectic process (from J-STD-020D)

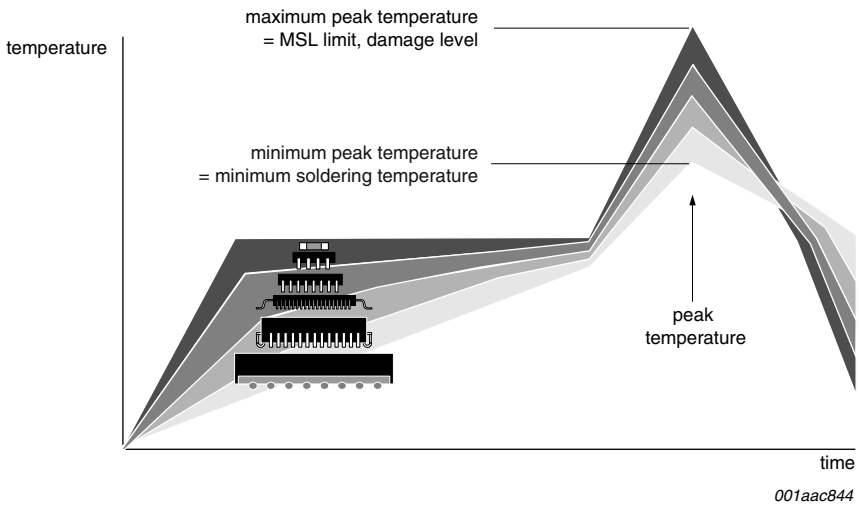
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 41. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 59.



MSL: Moisture Sensitivity Level

Fig 59. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

19. Abbreviations

Table 42. Abbreviations

Acronym	Description
ADC	Analog to Digital Converter
ADE	Antenna diversity Even
ADO	Antenna diversity Odd
AES	Advanced Encryption Standard
AGC	Automatic Gain Control
API	Application Program Interface
APT	Analog Peripheral Timer
BOM	Bill Of Material
BOR	Brown-Out Reset
CCA	Clear Channel Assessment
CCM	Counter with CBC-MAC
CDM	Charged Device Model
CLK	CLocK
CPU	Central Processing Unit
CRC	Cyclic redundancy Check
CSMA/CA	Carrier Sense Multiple Access with Collision Avoidance
CTS	Clear-To-Send
CW	Continuous Wave
DC	Direct current
DIO	Digital Input Output
DMA	Direct memory Access
DO	Digital Output
ED	Energy Detection
EEPROM	Electrically-Erasable Programmable Read Only Memory
ESR	Equivalent Series Resistance
FIFO	First In First Out
GP	General Purpose
GPIO	General Purpose Input Output
HBM	Human Body Model
HS	High Speed
HVQFN	Heatsink Very-thin Quad Flat No-Leads
ID	IDentification
IF	Intermediate frequency
IO	Input Output
IoT	Internet of Things
IPC	Interconnecting and Packaging Electronic Circuits
JTAG	Joint Test Action Group
LNA	Low Noise Amplifier
LQI	Link Quality Indication

Table 42. Abbreviations *...continued*

Acronym	Description
LSB	Low Significant Bit
MAC	Media Access Control
MSB	Most Significant Bit
MSIF	Master Serial InterFace
MSL	Moisture sensitivity level
NACK	Not ACKnowledge
NFET	Negative Field Effect Transistor
NRZ	Non-Return-to-Zero
NVIC	Nested Vector Interrupt Controller
OOK	On-Off Key
OTA	Over-The-Air
OTP	One Time Programmable
PA	Power Amplifier
PAN	Personal Area Network
PCB	Printed-Circuit Board
PDM	Persistent Data Manager
PHY	PHYsical
PLL	Phase-Locked Loop
POR	Power-On Reset
PPF	Palladium Pre Plated
PWM	Pulse Width Modulation
RAM	Random Access Memory
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
RSSI	Receive Signal Strength Indication
RTS	Request-To-Send
RTOS	Real-Time Operating System
RTZ	Return-To-Zero
RX	Received
SCL	Serial CLock
SDA	Serial DatA
SDK	Software Developer's Kit
SMbus	System Management bus
SMDs	Surface Mount Devices
SPDT	Single-Pole Double-Throw
SPI-bus	Serial Peripheral Interface -bus
STSD	Slave Transmitter Stop Detect
SSIF	Slave Serial InterFace
SVM	Supply Voltage Monitor
SYNTH	SYNTHesizer
SysTick	System Tick timer

Table 42. Abbreviations *…continued*

Acronym	Description
TAF	Transmitter Arbitration Failure
TCM	Tightly-Coupled Memory
TX	Transmit
UART	Universal Asynchronous Receiver Transmitter
VCO	Voltage Controlled Oscillator
VTOR	Vector Table Offset Register

20. References

[1] **IEEE Std 802.15.4-2011 IEEE Standard for Information Technology Part 15.4 —** Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs).

[2] **Wireless Connectivity —** http://www.nxp.com/products/wireless-connectivity:WIRELESS-CONNECTIVITY

21. Revision history

Table 43. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
JN517x v3.0	20171107	Product data sheet	-	JN517x v2.0
JN517x v2.0	20161108	Product data sheet	-	JN517x v1.0
JN517x v1.0	20160805	Product data sheet	-	-

22. Legal information

22.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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