The documentation and process conversion measures necessary to comply with this document shall be completed by 12 December 2013.

INCH-POUND

MIL-PRF-19500/448F
12 September 2013
SUPERSEDING
MIL-PRF-19500/448E
18 October 2011

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, TRANSISTOR, PNP, SILICON, LOW-POWER,
TYPE 2N4405, 2N4405UA, and 2N4405UB,
JAN AND JANTX

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for PNP, silicon, low-power transistors. Two levels of product assurance are provided for each device type as specified in MIL-PRF-19500.

1.2 Physical dimensions. See figure 1 (similar to TO-39), figure 2 (UA), and figure 3 (UB).

1.3 Maximum ratings T_A = +25°C unless otherwise stated.

Types	P_T (1) T_C = +25°C	P_T (1) T_A = +25°C	P_T (1) $T_{SP(IS)}$ = +25°C	P_T (1) $T_{SP(AM)}$ = +25°C	$R_{\theta JC}$ (2)	$R_{\theta JA}$ (2)	$R_{\theta JSP(IS)}$ (2)	$R_{\theta JSP(AM)}$ (2)
	W	W	W	W	°C/W	°C/W	°C/W	°C/W
2N4405	5.0	1.0	N/A	N/A	35	175	N/A	N/A
2N4405UA	N/A	N/A	1.0	4	N/A	N/A	110	40
2N4405UB	N/A	N/A	1.0	N/A	N/A	N/A	90	N/A

Types	V_{CBO}	V_{CEO}	V_{EBO}	I_C	T_{STG} and T_J
	V dc	V dc	V dc	A dc	°C
2N4405	80	80	5	0.5	-65 to +200
2N4405UA	80	80	5	0.5	-65 to +200
2N4405UB	80	80	5	0.5	-65 to +200

(1) See figures 4, 5, 6, 7, and 8.
(2) For thermal impedance, see figures 9, 10, 11, 12, and 13.

* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil .

1.4 Primary electrical characteristics T_A = +25°C unless otherwise stated.

Limit	h_{FE1} (1)	h_{FE3} (1)	$V_{BE(SAT)2}$ (1)	$V_{CE(SAT)3}$ (1)	C_{obo}	$\|h_{fe}\|$
	V_{CE} = 5 V dc I_C = 100 µA dc	V_{CE} = 5 V dc I_C = 150 mA dc	I_C = 500 mA dc I_B = 50 mA dc	I_C = 500 mA dc I_B = 50 mA dc	V_{CB} = 10 V dc I_E = 0 mA dc 100 kHz ≤ f ≤1 MHz	V_{CE} = 20 V dc I_C = 50 mA dc f = 100 MHz
			V dc	V dc	pF	
Min	75	100	0.85			2.0
Max		300	1.20	0.5	20	6.0

(1) Pulsed (see 4.5.1).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

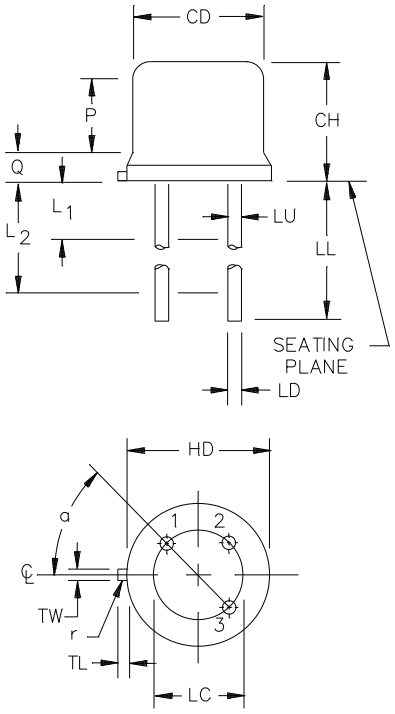
DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at http://quicksearch.dla.mil or https://assist.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

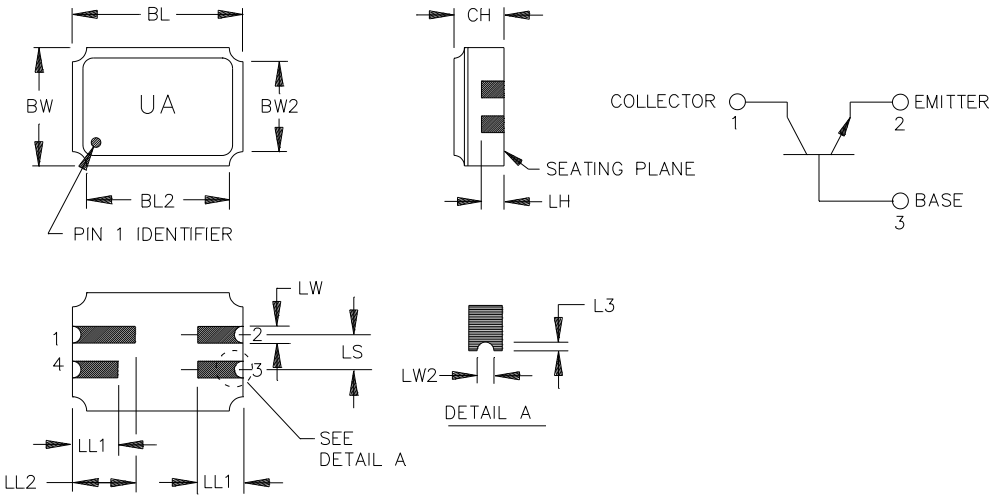
2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min.	Max.	Min.	Max.	
CD	.305	.335	7.75	8.51	
CH	.24	.26	6.1	6.6	
HD	.335	.37	8.51	9.4	
LC	.200 TP		5.08 TP		4
LD	.016	.021	.41	.53	2, 5
LL	.500	.750	12.70	19.05	5
LU	.016	.019	.41	.48	3, 5
L1		.050		1.27	
L2	.250		6.35		
P	.100		2.54		
Q		.040		1.02	
r		.007		.18	
TL	.029	.045	.74	1.14	
TW	.028	.034	.71	.86	
α	45° TP		45° TP		



NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Measured in the zone beyond .250 (6.35) from the seating plane.
4. Measured in the zone .050 (1.27 mm) and .250 (6.35) from the seating plane.
5. Measured from the maximum diameter of the actual case.
6. All three leads.
7. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
8. Lead 1 is the emitter, lead 2 is the base, and lead 3 is the collector, which is electrically connected to the case.

FIGURE 1. Physical dimensions for 2N4405 (similar to TO-39).



Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.215	.225	5.46	5.71	
BL2		.225		5.71	
BW	.145	.155	3.68	3.93	
BW2		.155		3.93	
CH	.061	.075	1.55	1.90	3
L3	.003		0.08		5
LH	.029	.042	0.74	1.07	
LL1	.032	.048	0.81	1.22	
LL2	.072	.088	1.83	2.23	
LS	.045	.055	1.14	1.39	
LW	.022	.028	0.56	0.71	
LW2	.006	.022	0.15	0.56	5

Pin no.	1	2	3	4
Transistor	Collector	Emitter	Base	N/C

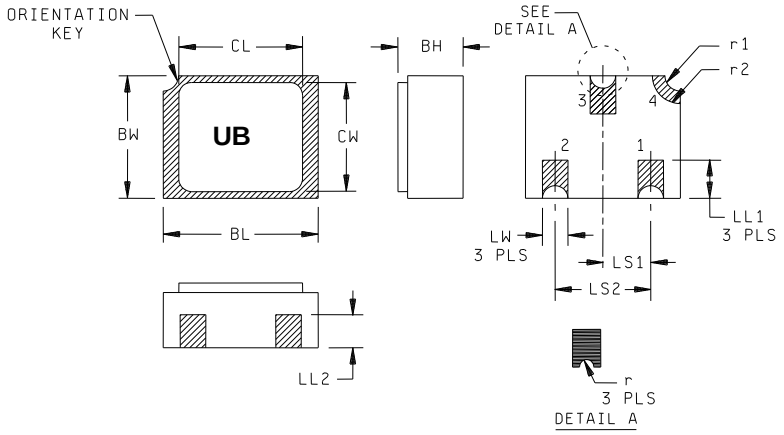
NOTES:

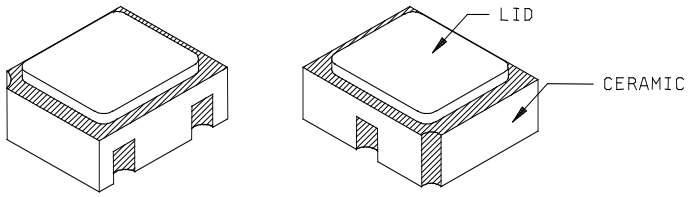
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Dimension "CH" controls the overall package thickness. When a window lid is used, dimension "CH" must increase by a minimum of .010 inch (0.254 mm) and a maximum of .040 inch (1.020 mm).
4. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.

* 5. Dimensions "LW2" minimum and "L3" minimum and the appropriate castellation length define an unobstructed three-dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on bottom two layers, optional on top ceramic layer.) Dimension "LW2" maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.

6. The coplanarity deviation of all terminal contact points, as defined by the device seating plane, shall not exceed .006 inch (0.15mm) for solder dipped leadless chip carriers.
7. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

* FIGURE 2. Physical dimensions, surface mount (UA version).





Ltr.	Dimensions				Note	Ltr.	Dimensions				Note
	Inches		Millimeters				Inches		Millimeters		
	Min	Max	Min	Max			Min	Max	Min	Max	
BH	.046	.056	1.17	1.42		LS1	.035	.040	0.89	1.02	
BL	.115	.128	2.92	3.25		LS2	.071	.079	1.80	2.01	
BW	.085	.108	2.16	2.74		LW	.016	.024	0.41	0.61	
CL		.128		3.25		r		.008		0.20	
CW		.108		2.74		r1		.012		0.31	
LL1	.022	.038	0.56	0.96		r2		.022		0.56	
LL2	.017	.035	0.43	0.89							

NOTES:

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Hatched areas on package denote metallized areas.
4. Lid material: Kovar.
5. Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Pad 4 = Shielding connected to the lid.
6. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 3. Physical dimensions, surface mount (UB version).

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

PCB	Printed circuit board
$R_{\theta JA}$	Thermal resistance junction to ambient.
$R_{\theta JC}$	Thermal resistance junction to case.
$R_{\theta JSP(AM)}$	Thermal resistance junction to solder pads (adhesive mount to PCB).
$R_{\theta JSP(IS)}$	Thermal resistance junction to solder pads (infinite sink mount to PCB).

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figure 1 (similar to TO-39), figure 2 (UA), and figure 3 (UB).

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.6 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.7 Marking. Marking shall be in accordance with MIL-PRF-19500. At the option of the manufacturer, marking may be omitted from the body, but shall be retained on the initial container.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4, and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.3 Screening JANTX level. Screening shall be in accordance with table IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500)	Measurement
	JANTX level only
(1) 3c	Method 3131of MIL-STD-750, thermal impedance. See 4.3.2.
9	Not applicable
11	h_{FE2} and I_{CBO2}
12	See 4.3.1
13	Subgroup 2 of table I herein, ΔI_{CBO2} = 100 percent of initial value or 10 nA dc, whichever is greater; Δh_{FE2} = ±20 percent of initial value.

(1) Shall be performed anytime after temperature cycling, screen 3a; and does not need to be repeated in screening requirements.

4.3.1 Power burn-in conditions. Power burn-in conditions are as follows: V_{CB} = 10 - 30 Vdc. Power shall be applied to achieve T_J =+135°C minimum and a minimum P_D = 75 percent of P_T maximum rated as defined in 1.3.

4.3.2 Thermal impedance ($Z_{\theta JX}$ measurements). The $Z_{\theta JX}$ measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{MD}, (and V_C where appropriate). The $Z_{\theta JX}$ limit used in screen 3c of 4.3 and subgroup 2 of table I shall comply with the thermal impedance graph in figures 9, 10, 11, 12, and 13 (less than or equal to the curve value at the same t_H time) and shall be less than the process determined statistical maximum limit as outlined in method 3131.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein. Group A inspection shall be performed on each sublot.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500 and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the tests and conditions specified in 4.4.2.1 for JAN and JANTX group B testing. Electrical measurements (end-points) and delta requirements for JAN and JANTX shall be after each step in 4.4.2.1 and shall be in accordance with table I, group A, subgroup 2. Delta measurements shall be in accordance with table III herein as specified in the notes for table III.

4.4.2.1 Group B inspection, (JAN and JANTX). Separate samples may be used for each step. In the event of a group B failure, the manufacturer may pull a new sample at double size from either the failed assembly lot or from another assembly lot from the same wafer lot. If the new "assembly lot" option is exercised, the failed assembly lot shall be scrapped.

Step	Method	Condition
1	1026	Steady-state life: 1,000 hours minimum, V_{CB} = 10 V dc, power shall be applied to achieve T_J = +150°C minimum using a minimum of P_D = 75 percent of maximum rated P_T as defined in 1.3. n = 45 devices, c = 0. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.
2	1048	Blocking life: T_A = 150°C, V_{CB} = 80 percent rated voltage, 48 hours minimum. n = 45, c = 0.
3	1032	High-temperature life (non-operating), t = 340 hours, T_A = +200°C. n = 22, c = 0.

4.4.2.2 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

a. For JAN and JANTX, samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot. See MIL-PRF-19500.

b. Shall be chosen from an inspection lot that has been submitted to and passed table I, subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (group B for JAN and JANTX) may be pulled prior to the application of final lead finish.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500. Electrical measurements (end-points) and delta requirements shall be in accordance with the applicable steps of table III herein.

	Subgroup	Method	Condition
*	C2	2036	Test condition E, not applicable for UA and UB devices.
	C5	3131	$R_{\theta JA}$ only.
	C6		Not applicable.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified herein. Electrical measurements (end-points) and delta measurements shall be in accordance with the applicable steps of table III and table I, subgroup 2 herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 1 2/						
Visual and mechanical examination	2071					
Solderability 3/ 4/	2026	n = 15 leads, c = 0				
Resistance to solvents 3/ 4/	1022	n = 15 devices, c = 0				
Temp cycling 3/ 4/	1051	Test condition C, 25 cycles. n = 22 devices, c = 0				
Hermetic seal 4/ Fine leak Gross leak	1071	n = 22 devices, c = 0				
Electrical measurements 4/		Table I, subgroup 2				
Bond strength 3/ 4/	2037	Precondition T_A = +250°C at t = 24 hours or T_A = +300°C at t = 2 hours, n = 11 wires, c = 0				
Decap internal visual (design verification) 4/	2075	n = 4 devices, c = 0				
Subgroup 2						
Thermal impedance	3131	See 4.3.2.	$Z_{\theta JX}$			°C/W
Breakdown voltage, collector to emitter	3011	Bias condition D, I_C = 10 mA dc pulsed (see 4.5.1)	$V_{(BR)CEO}$	80		V dc
Collector to base cutoff current	3036	Bias condition D, V_{CB} = 80 V dc	I_{CBO1}		10	µA dc
Collector to base cutoff current	3036	Bias condition D, V_{CB} = 60 V dc	I_{CBO2}		25	nA dc
Emitter to base breakdown voltage	3061	Bias condition D, V_{EB} = 5.0 V dc	I_{EBO1}		10	µA dc
Emitter to base cutoff current	3061	Bias condition D, V_{EB} = 3.0 V dc	I_{EBO2}		25	nA dc
Forward-current transfer ratio	3076	V_{CE} = 5 V dc; I_C = 0.1 mA dc; pulsed (see 4.5.1)	h_{FE1}	75		
Forward-current transfer ratio	3076	V_{CE} = 5 V dc; I_C = 10 mA dc; pulsed (see 4.5.1)	h_{FE2}	100		

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - Continued						
Forward-current transfer ratio	3076	V_{CE} = 5 V dc; I_C = 150 mA dc, pulsed (see 4.5.1)	h_{FE3}	100	300	
Forward-current transfer ratio	3076	V_{CE} = 5 V dc; I_C = 500 mA dc; pulsed (see 4.5.1)	h_{FE4}	50		
Collector-emitter saturated voltage	3071	I_C = 10 mA dc; I_B = 1.0 mA dc; pulsed (see 4.5.1)	$V_{CE(SAT)1}$		0.15	V dc
Collector-emitter saturated voltage	3071	I_C = 150 mA dc; I_B = 15 mA dc; pulsed (see 4.5.1)	$V_{CE(SAT)2}$		0.20	V dc
Collector-emitter saturated voltage	3071	I_C = 500 mA dc; I_B = 50 mA dc; pulsed (see 4.5.1)	$V_{CE(SAT)3}$		0.50	V dc
Base-emitter non-saturated	3066	Test condition B; V_{CE} = 5 V dc; I_C = 150 mA dc; pulsed (see 4.5.1)	V_{BE}		0.90	V dc
Base-emitter saturated voltage	3066	Test condition A; I_C = 10 mA dc; I_B = 1 mA dc; pulsed (see 4.5.1)	$V_{BE(SAT)1}$		0.80	V dc
Base-emitter saturated voltage	3066	Test condition A; I_C = 500 mA dc; I_B = 50 mA dc; pulsed (see 4.5.1)	$V_{BE(SAT)2}$	0.85	1.20	V dc
Subgroup 3						
High-temperature operation		T_A = +150°C				
Collector to base cutoff current	3036	Bias condition D, V_{CB} = 60 V dc	I_{CBO3}		25	µA dc
Low-temperature operation		T_A = -55°C				
Forward-current transfer ratio	3076	V_{CE} = 5 V dc; I_C = 150 mA dc pulsed (see 4.5.1)	h_{FE5}	40		

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 4						
Delay time		V_{CC} = 31.9 V dc; $V_{BE(OFF)}$ = 0.8 V dc; I_C = 500 mA dc; I_{B1} = 50 mA dc; (see figure 14)	t_d		15	ns
Rise time		V_{CC} = 31.9 V dc; $V_{BE(OFF)}$ = 0.8 V dc; I_C = 500 mA dc; I_{B1} = 50 mA dc; (see figure 14)	t_r		25	ns
Storage time		V_{CC} = 31.9 V dc; I_C = 500 mA dc; I_{B1} = I_{B2} = 50 mA dc; (see figure 14)	t_s		175	ns
Fall time		V_{CC} = 31.9 V dc; I_C = 500 mA dc; I_{B1} = I_{B2} = 50 mA dc; (see figure 14)	t_f		50	ns
Magnitude of common emitter, small- signal short-circuit forward current transfer ratio	3306	V_{CE} = 20 V dc; I_C = 50 mA dc; f = 100 MHz	$\|h_{FE}\|$	2.0	6	
Noise figure	3246	V_{CE} = 10 V dc; I_C = 1 mA dc; f = 1 kHz; R_s = 100 ohms	NF		3.5	dB
Open circuit output capacitance	3236	V_{CB} = 10 V dc; I_E = 0 mA dc 100 kHz ≤ f ≤ 1 MHz	C_{obo}		20	pF
Subgroup 5						
Safe operating area (continuous dc)	3051	T_C = +25°C; V_{CE} = 10 V dc; I_C = 0.5 A dc; t = 1 s; 1 cycle				
Electrical measurements		See table I, subgroup 2				

1/ For sampling plan, see MIL-PRF-19500.
2/ For resubmission of failed subgroup 1, double the sample size of the failed test or sequence of tests. A failure in table I, subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.
3/ Separate samples may be used.
4/ Not required for laser marked devices.

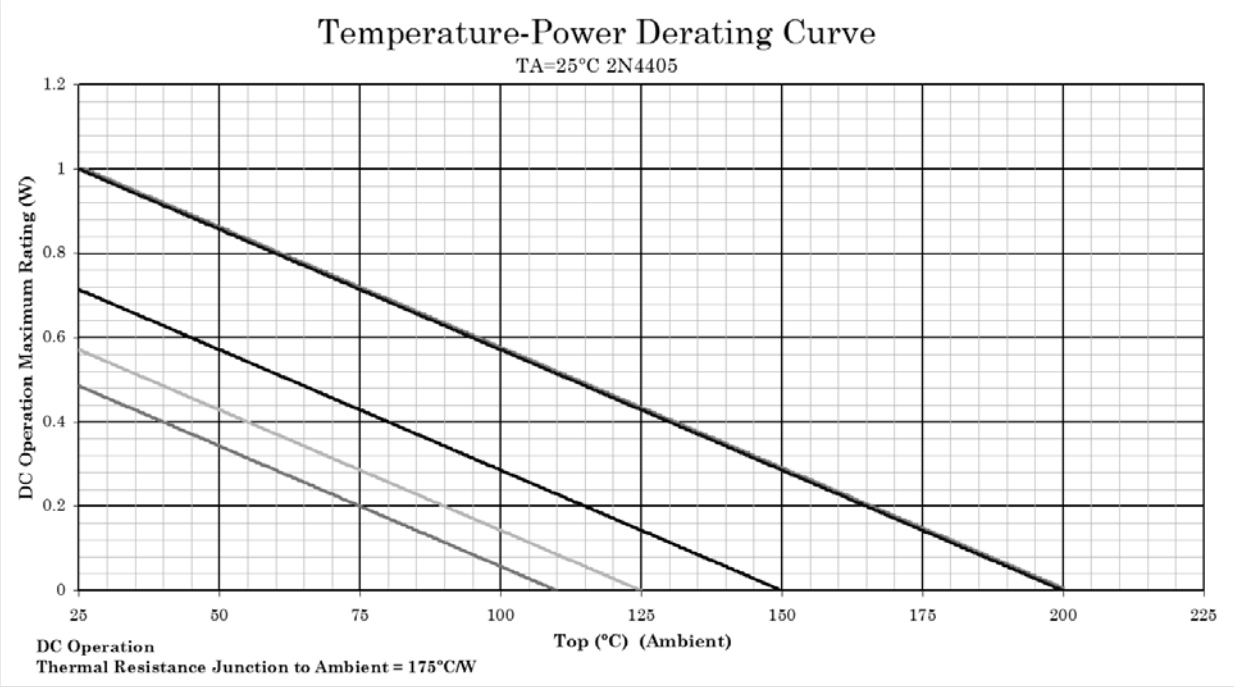
TABLE II. Group E inspection (all quality levels) - for qualification and requalification only.

Inspection	MIL-STD-750		Qualification
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table 1, subgroup 2 and table III herein.	
Subgroup 2			45 devices c = 0
Intermittent life	1037	V_{CB} = 10 V dc, 6,000 cycles	
Electrical measurements		See table 1, subgroup 2 and table III herein.	
Subgroup 4			
Thermal resistance	3131	$R_{\theta JSP(IS)}$ can be calculated but shall be measured once in the same package with a similar die size to confirm calculations (may apply to specification sheets). $R_{\theta JSP(AM)}$ need be calculated only.	15 devices, c = 0
Thermal impedance curves		See MIL-PRF-19500, table E-IX, group E, subgroup 4.	
Subgroup 5			
Not applicable			
Subgroup 6			
ESD	1020		
Subgroup 8			
Reverse stability	1033	Condition B < 400 V	45 devices c = 0

TABLE III. Delta measurements. 1/

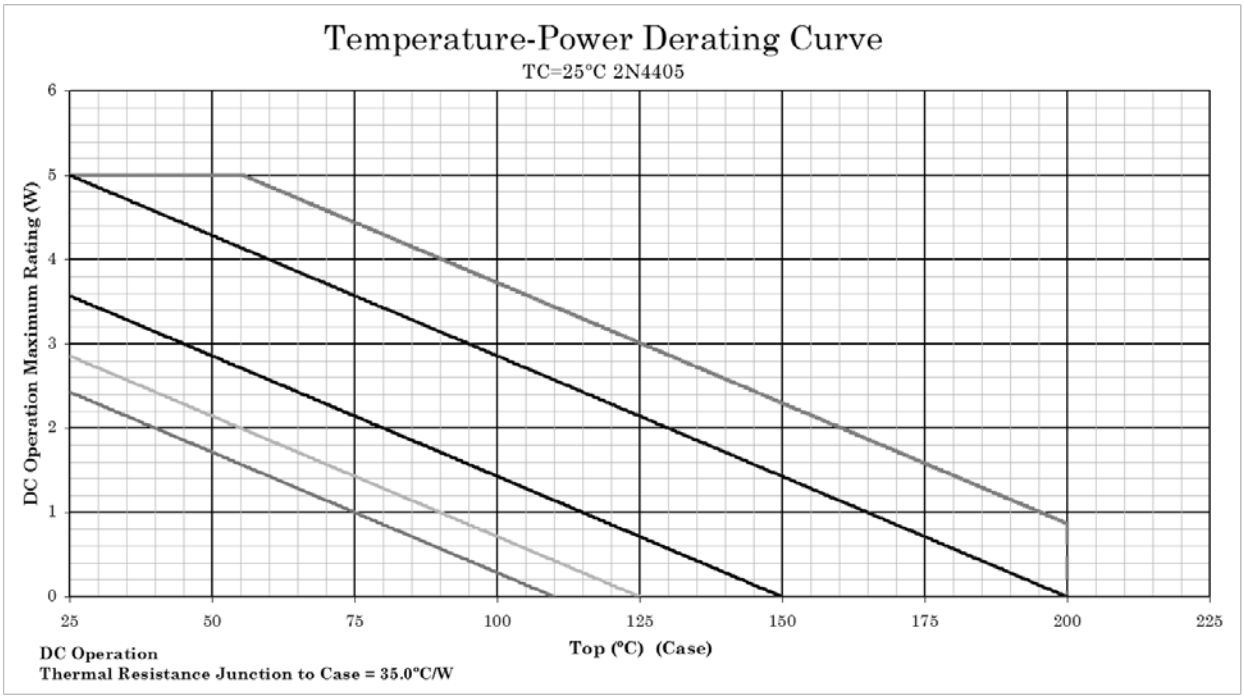
Step	Inspection	MIL-STD-750		Symbol	Limits		Unit
		Method	Conditions		Min	Max	
1	Forward-current transfer ratio	3076	V_{CE} = 5.0 V dc; I_C = 10 mA dc; pulsed (see 4.5.1)	Δh_{FE2}	±20 percent change		

1/ The delta measurements for 4.4.2.1 are as follows: Table III, step 1, to be performed after each step in group B.



NOTES:
1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curves chosen at T_J ≤ 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

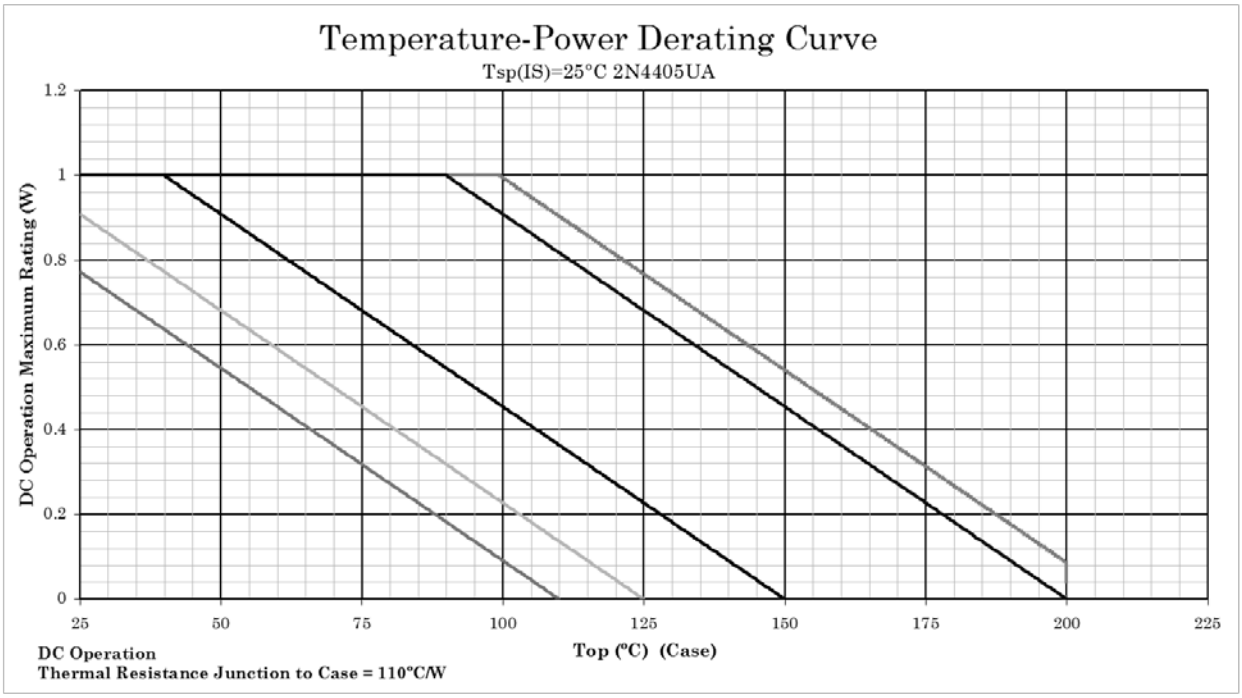
FIGURE 4. Derating for 2N4405 $R_{\theta JA}$ (TO-39).



NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

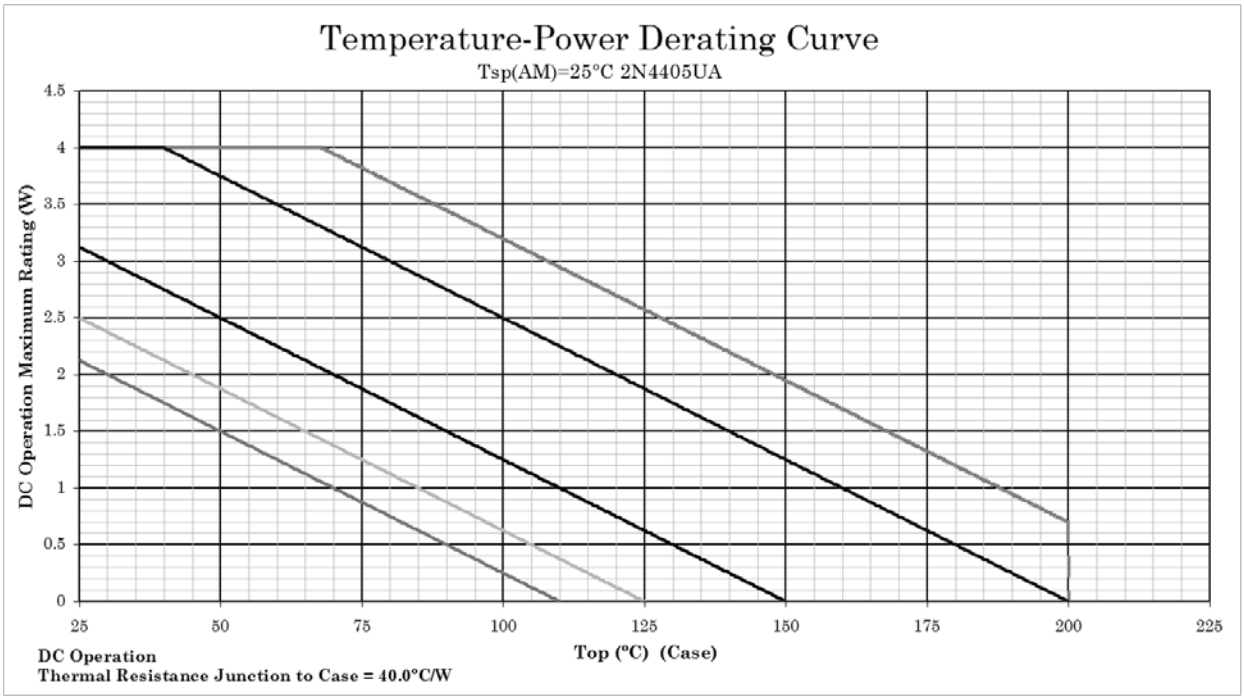
FIGURE 5. Derating for 2N4405 $R_{\theta JC}$ (TO-39).



NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

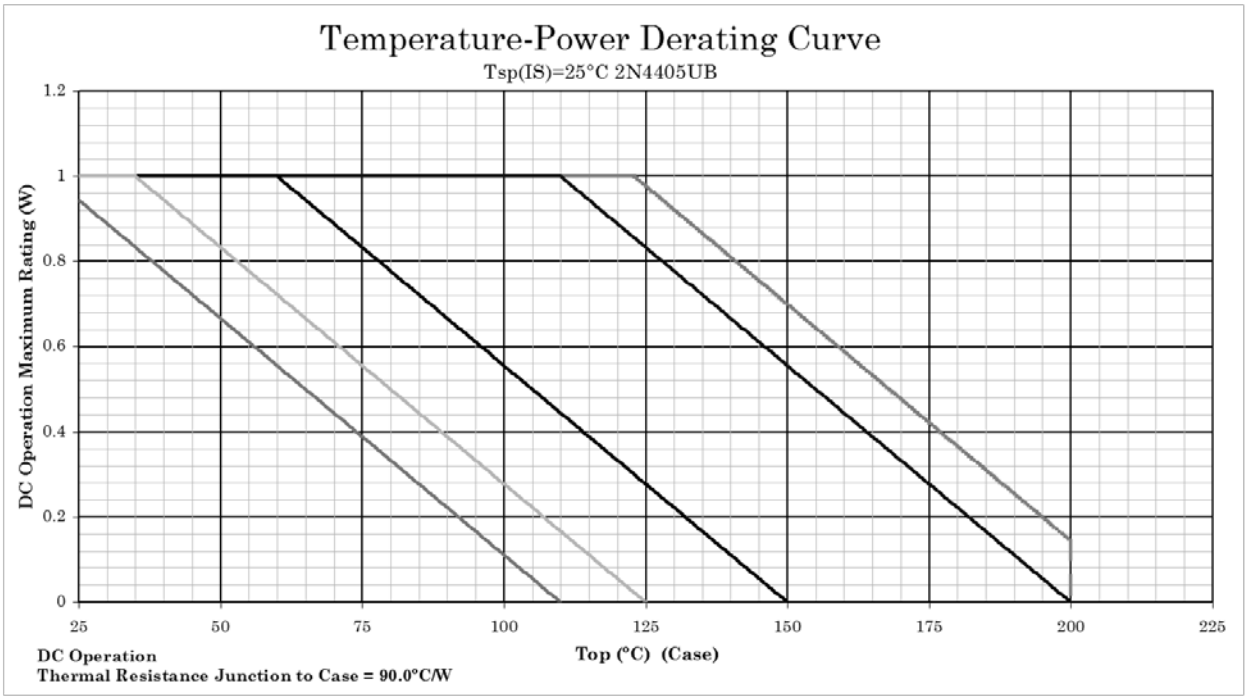
FIGURE 6. Derating for 2N4405UA, $R_{\theta JSP(IS)}$ (UA) Kovar.



NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

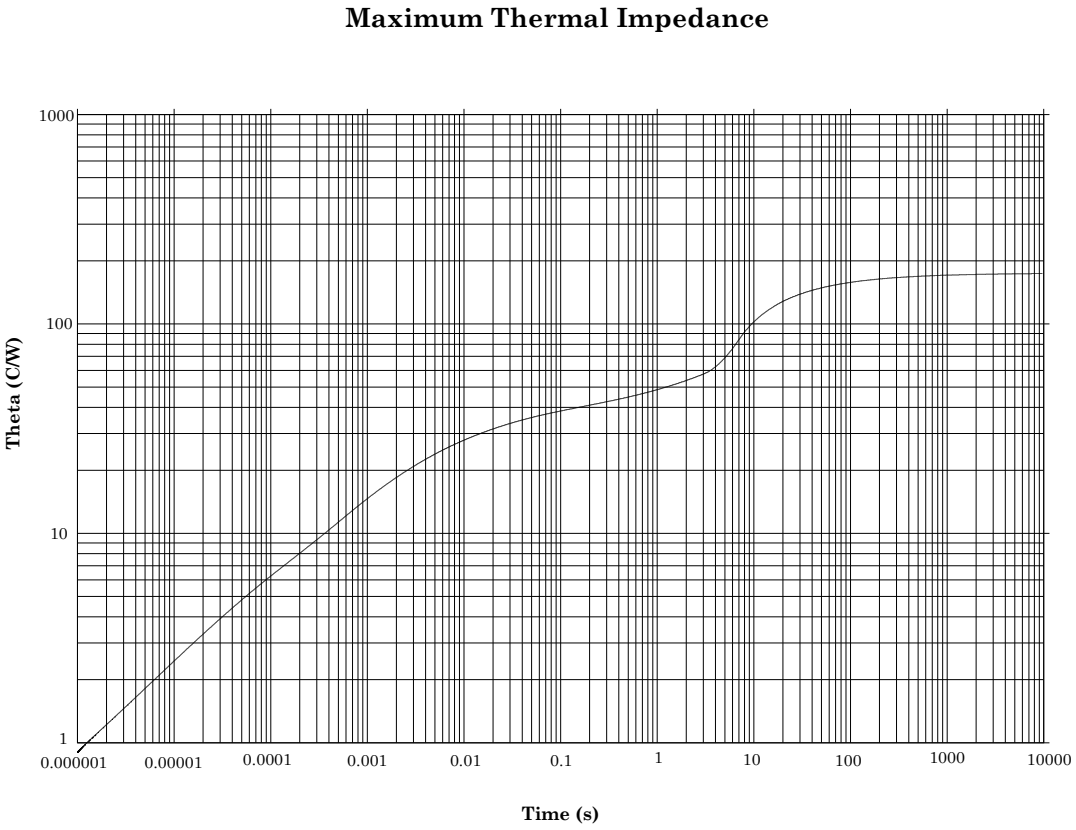
FIGURE 7. Derating for 2N4405UA, $R_{\theta JSP(AM)}$ (UA) Kovar.



NOTES:

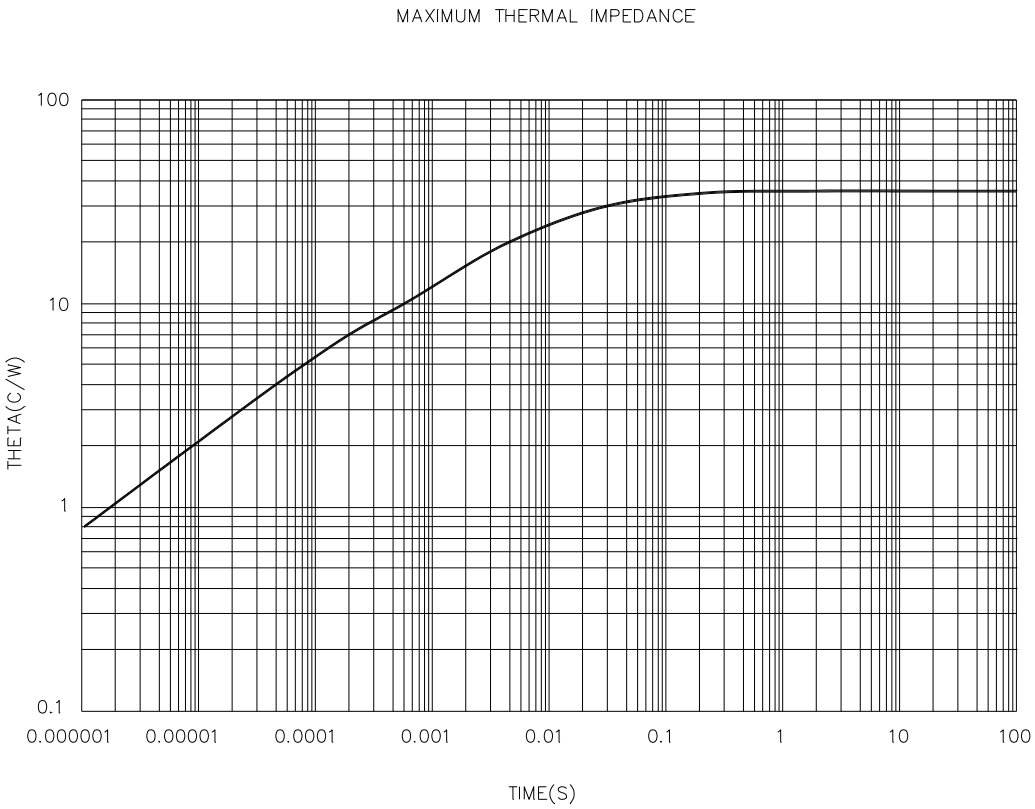
1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 8. Derating for 2N4405UB, $R_{\theta JSP(IS)}$ (UB) Kovar.



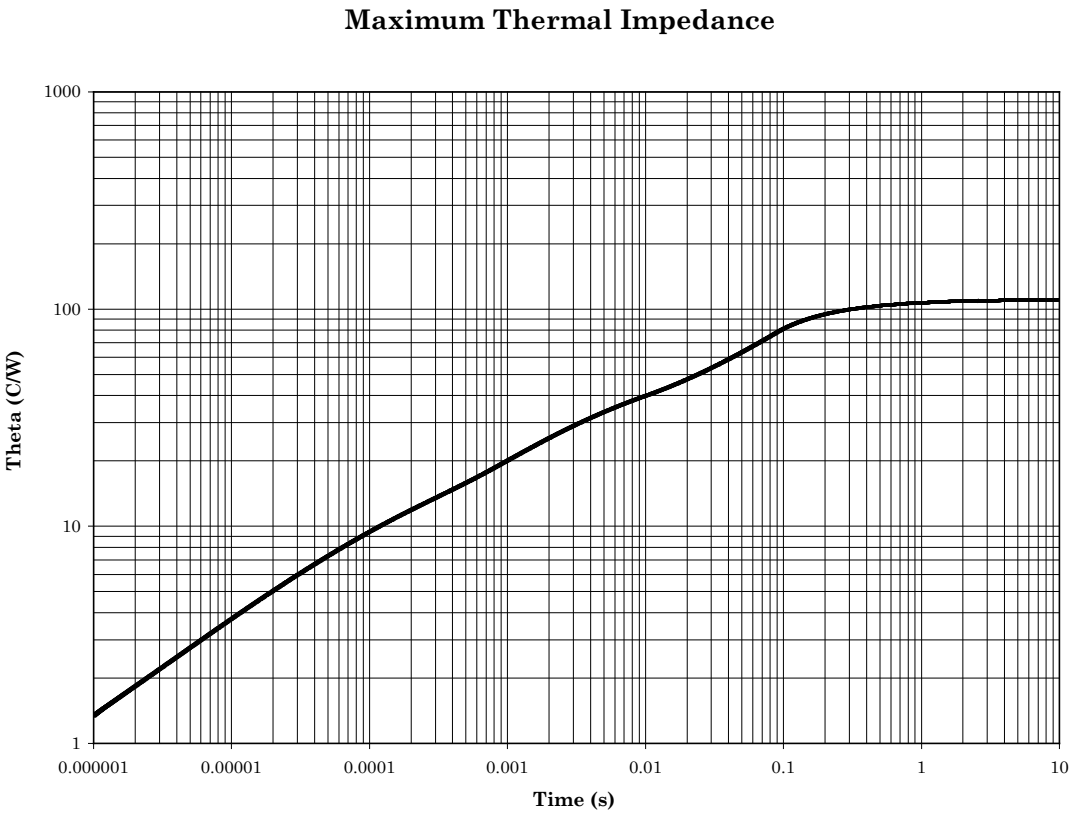
Ambient free air cooled T_A = +25°C, 800mW, thermal resistance $R_{\theta JA}$ = 175°C/W

FIGURE 9. Thermal impedance graph ($R_{\theta JA}$) for 2N4405 (TO-39).



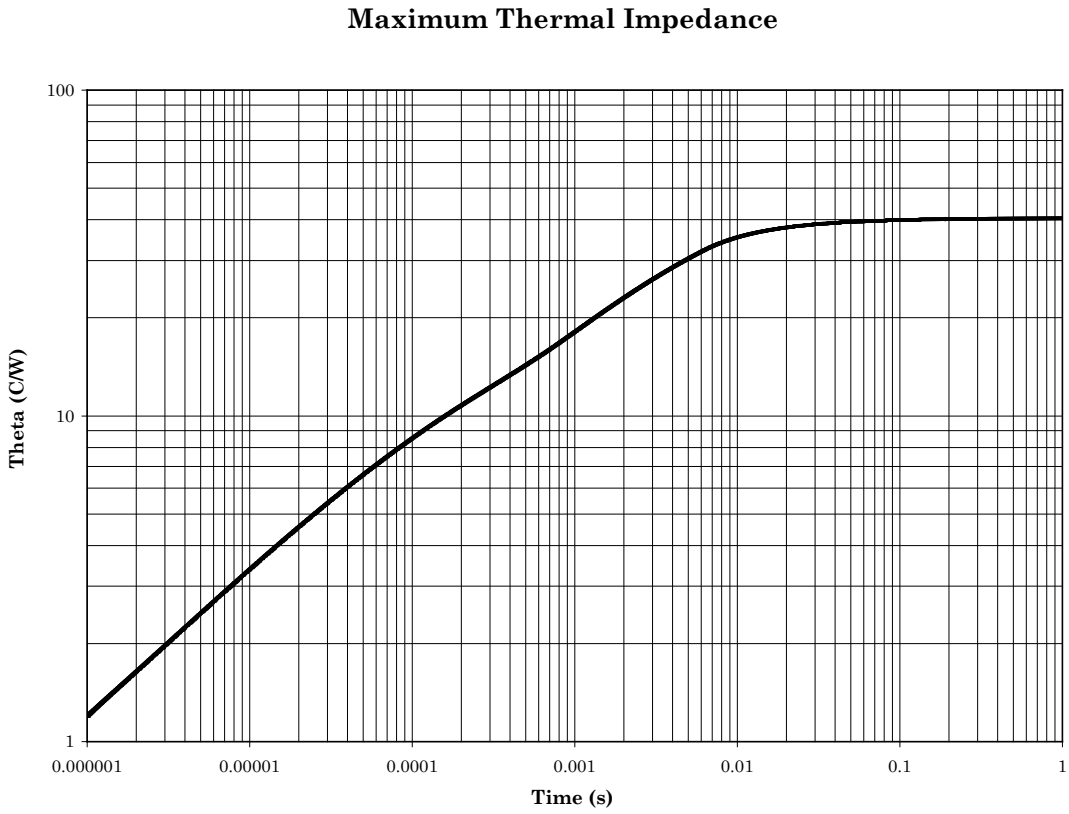
Ambient case mounted T_C = +25°C, thermal resistance $R_{\theta JC}$ = 35C°/W.

FIGURE 10. Thermal impedance graph ($R_{\theta JC}$) for 2N4405 (TO-39).



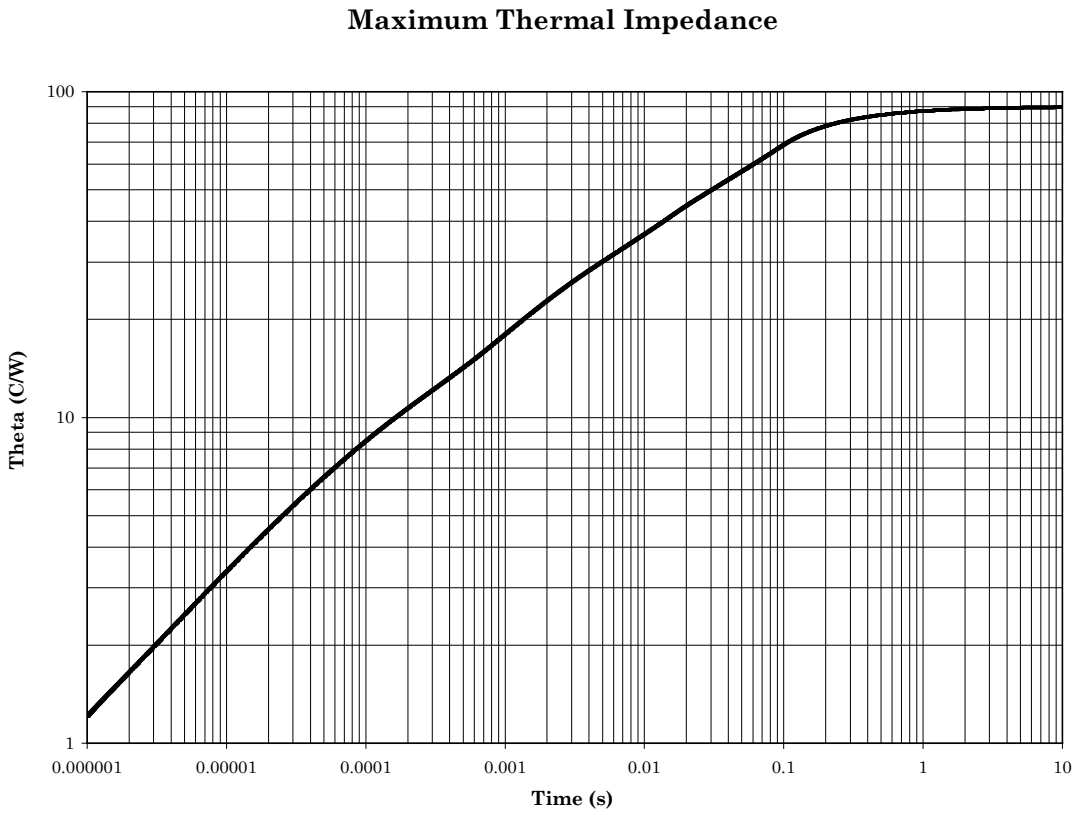
Solder mounted to heavy copper clad PCB at T_{SP} = +25°C, thermal resistance $R_{\theta JSP(IS)}$ = 110°C/W.

FIGURE 11. Thermal impedance graph ($R_{\theta JSP(IS)}$) for 2N4405UA.



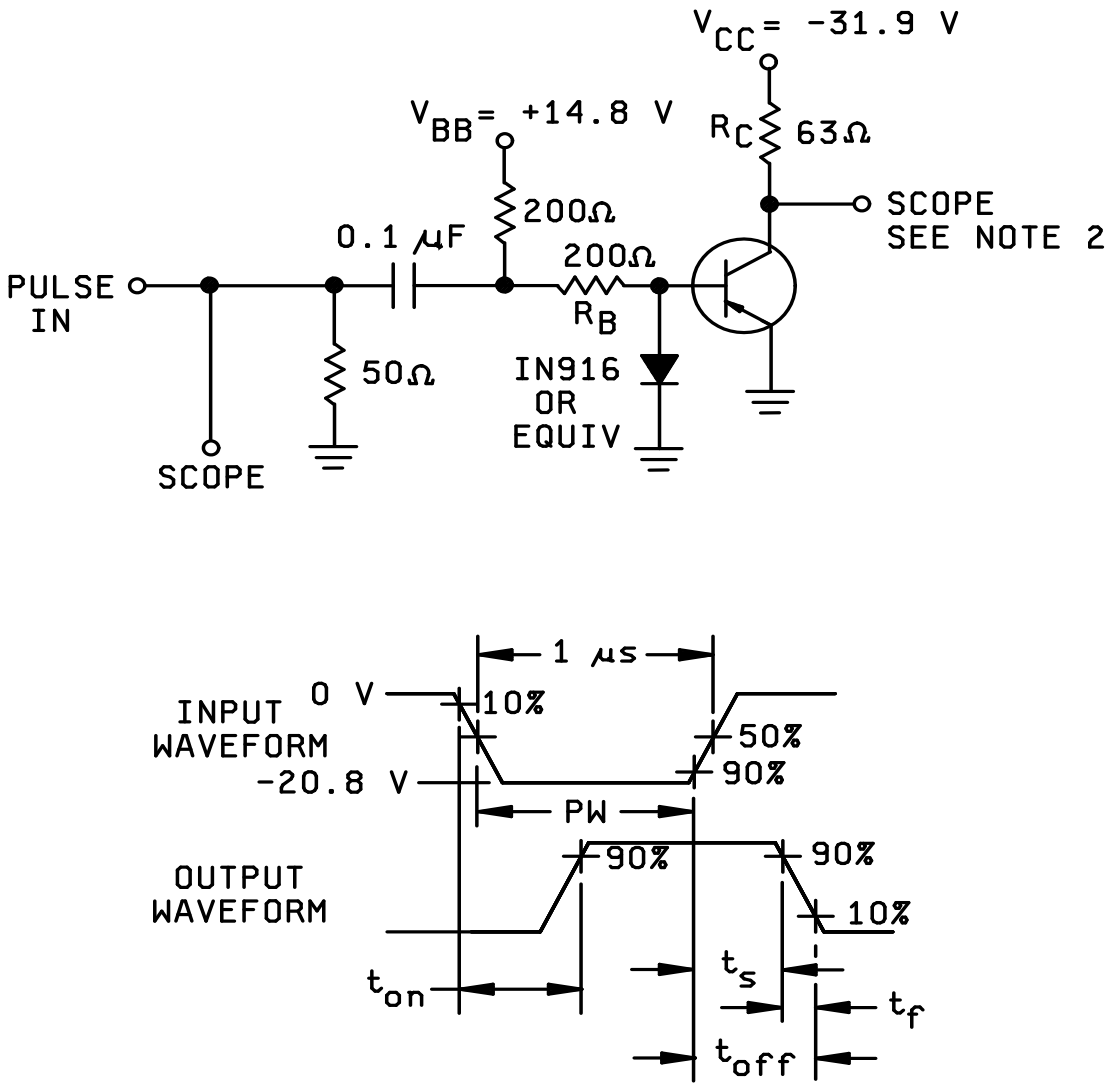
Solder mounted to heavy copper clad PCB at T_{SP} = +25°C, thermal resistance $R_{\theta JSP(AM)}$ = 40°C/W.

FIGURE 12. Thermal impedance graph ($R_{\theta JSP(AM)}$) for 2N4405UA.



Solder mounted to heavy copper clad PCB at T_{SP} = +25°C, thermal resistance $R_{\theta JSP(IS)}$ = 90°C/W.

FIGURE 13. Thermal impedance graph ($R_{\theta JSP(IS)}$) for 2N4405UB.



NOTES:

1. The rise time (t_r) of the applied pulse shall be ≤ 2.0 ns; duty cycle ≤ 2 percent; generator source impedance shall be 50 ohms.
2. Output sampling oscilloscope: $Z_{in} \geq 100\ k\Omega$; $C_{in} \leq 12$ pF; rise time ≤ 0.2 ns.
3. To obtain data for curves, voltage levels are approximately as shown, R_B and R_C are varied.

FIGURE 14. Pulse response test circuit.