The documentation and process conversion measures necessary to comply with this document shall be completed by 5 December 2013.

INCH-POUND

MIL-PRF-19500/393L
5 September 2013
SUPERSEDING
MIL-PRF-19500/393K
3 February 2012

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, TRANSISTOR, NPN, SILICON POWER,
TYPES 2N3418, 2N3418S, 2N3418U4, 2N3419, 2N3419S, 2N3419U4, 2N3420, 2N3420S, 2N3420U4, 2N3421, 2N3421S, AND 2N3421U4, JAN, JANTX, JANTXV, JANS, JANSM, JANSD, JANSP, JANSL, JANSR, JANSF, JANSG, JANSH, JANHCC, JANKCC, JANKCCM, JANKCCD, JANKCCP, JANKCCL, JANKCCR, JANKCCF, JANKCCG, AND JANKCCH

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1. Scope. This specification covers the performance requirements for NPN, silicon, transistors for use in medium power switching applications. Four levels of product assurance are provided for each device type, and two levels of product assurance for die (element evaluation) are provided, as specified in MIL-PRF-19500. RHA level designators “M”, “D”, “P“, “L”, “R”, “F”, “G”, and “H” are appended to the device prefix to identify devices, which have passed RHA requirements.

1.2. Physical dimensions. See figure 1 (similar to TO-5 for long leaded devices and TO-39 for short leaded devices), figure 2 for JANHC and JANKC (die), and figure 3 (2N3418U4 through 2N3421U4) dimensions.

1.3 Maximum ratings, unless otherwise specified T_A = +25°C.

Type	P_T T_A = +25°C (1)	P_T T_C = +100°C (1)	V_{CBO}	V_{CEO}	V_{EBO}	I_C	I_C (2)	T_{STG} and T_J	$R_{\theta JA}$ (3)	$R_{\theta JC}$ (3)
	W	W	V dc	V dc	V dc	A dc	A dc	°C	°C/W	°C/W
2N3418, 2N3418S	1.0	5	85	60	8	3	5	-65 to	175	18
2N3418U4	1.0	15	85	60	8	3	5	+200	175	4.5
2N3419, 2N3419S	1.0	5	125	80	8	3	5	-65 to	175	18
2N3419U4	1.0	15	125	80	8	3	5	+200	175	4.5
2N3420, 2N3420S	1.0	5	85	60	8	3	5	-65 to	175	18
2N3420U4	1.0	15	85	60	8	3	5	+200	175	4.5
2N3421, 2N3421S	1.0	5	125	80	8	3	5	-65 to	175	18
2N3421U4	1.0	15	125	80	8	3	5	+200	175	4.5

(1) For derating, see figure 4 through figure 6.
(2) This value applies for $t_p \leq 1$ ms, duty cycle ≤ 50 percent.
(3) For thermal impedance curves see figures 7, 8, and 9.

* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil.

1.4. Primary electrical characteristics at T_A = +25°C.

Limits	h_{FE2} (1)		h_{FE4} (1)		$V_{CE(sat)}$ (1)	$V_{BE(sat)}$ (1)	$\|h_{fe}\|$	C_{obo}
	V_{CE} = 2 V dc I_C = 1 A dc		V_{CE} = 5 V dc I_C = 5 A dc		I_C = 1 A dc I_B = 0.1 A dc	I_C = 1 A dc I_B = 0.1 A dc	V_{CE} = 10 V dc I_C = 0.1 A dc f = 20 MHz	V_{CB} = 10 V dc I_E = 0 100 kHz ≤ f ≤ 1 MHz
	2N3418 2N3418S 2N3418U4 2N3419 2N3419S 2N3419U4	2N3420 2N3420S 2N3420U4 2N3421 2N3421S 2N3421U4	2N3418 2N3418S 2N3418U4 2N3419 2N3419S 2N3419U4	2N3420 2N3420S 2N3420U4 2N3421 2N3421S 2N3421U4				
					V dc	V dc		pF
Min	20	40	10	15		0.6	1.3	
Max	60	120			0.25	1.2	8	150

(1) Pulsed (see 4.5.1).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

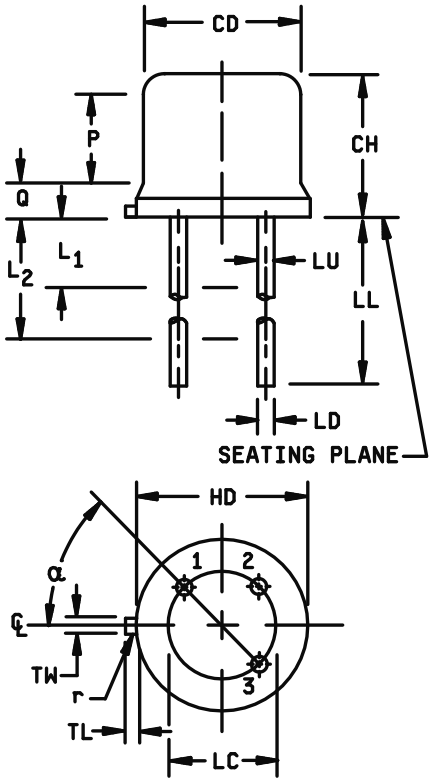
DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at http://quicksearch.dla.mil or https://assist.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

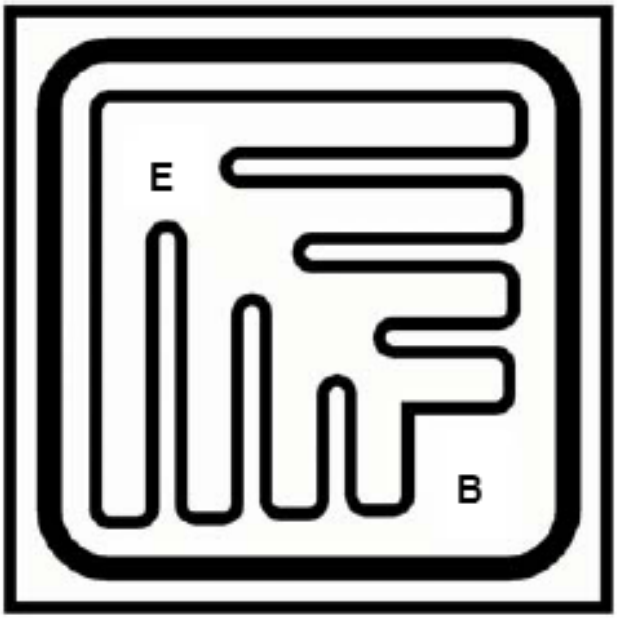
2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	
CH	.240	.260	6.10	6.60	
HD	.335	.370	8.51	9.40	
LC	.200 TP		5.08 TP		6
LD	.016	.021	0.41	0.53	
LL	.500	.750	12.7	19.05	7
LU	See notes 7, 13, 14				
L_1		.050		1.27	7
L_2	.250		6.35		7
P	.100		2.54		5
Q		.040		1.02	4
TL	.029	.045	0.74	1.14	3,10
TW	.028	.034	0.71	.86	9,10
r		.010		0.25	11
α	45° TP		45° TP		6



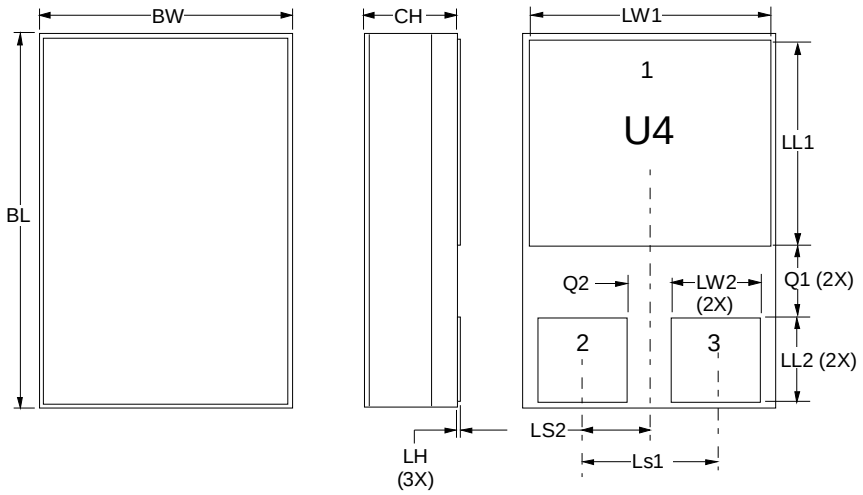
NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Symbol TL is measured from HD maximum.
4. Details of outline in this zone are optional.
5. Symbol CD shall not vary more than .010 inch (0.25 mm) in zone P. This zone is controlled for automatic handling.
6. Leads at gauge plane .054 inch (1.37 mm) +.001 inch (0.03 mm) -.000 inch (0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of TP relative to tab. Device may be measured by direct methods or by gauge.
7. Symbol LU applies between L_1 and L_2. Dimension LD applies between L_2 and LL minimum. Diameter is uncontrolled in L_1 and beyond LL minimum.
8. Lead number 3 is electrically connected to case.
9. Beyond r maximum, TW shall be held for a minimum length of .021 inch (0.53 mm).
10. Lead number 4 omitted on this variation.
11. Symbol r applied to both inside corners of tab.
12. For transistor types 2N3418S, 2N3419S, 2N3420S, 2N3421S, LL is .500 (12.70 mm) minimum and .750 (19.05 mm) maximum.
13. For transistor types 2N3418, 2N3419, 2N3420, 2N3421, LL is 1.500 (38.10 mm) minimum, and 1.750 (44.45 mm) maximum.
14. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
15. Lead 1 is emitter, lead 2 is base, and lead 3 is collector.

FIGURE 1. Physical dimensions.



1. Chip size: .075 x .075 inch ±.002 inches (1.905 x 1.905 mm ±0.051 mm).
2. Chip thickness: .014 ±.003 inch nominal (0.356 ±0.0762 mm).
3. Top metal: Aluminum 110,000 Å minimum, 125,000 Å nominal.
4. Back metal: Al/Ti/Ni/Au 10,000 Å minimum, 12,500 Å nominal.
5. Backside: Collector.
6. Bonding pad: B = .014 x .014 inch (0.3556 x 0.3556 mm), E = .014 x .014 inch (0.3556 x 0.3556 mm).
* 7. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 2. JANHCC and JANKCC-version die dimensions.



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.215	.225	5.46	5.72
BW	.145	.155	3.68	3.94
CH	.049	.075	1.24	1.91
LH		.020		0.51
LW1	.135	.145	3.43	3.68
LW2	.047	.057	1.19	1.45
LL1	.085	.125	2.16	3.17
LL2	.045	.075	1.14	1.91
LS1	.070	.095	1.78	2.41
LS2	.035	.048	0.890	1.21
Q1	.030	.070	0.76	1.78
Q2	.020	.035	0.510	0.890
Term 1	Collector			
Term 2	Base			
Term 3	Emitter			

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
* 3. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 3. Physical dimensions and configuration (U4).

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

$R_{\theta JA}$	Thermal resistance junction to ambient.
$R_{\theta JC}$	Thermal resistance junction to case.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figure 1, (similar to TO-5 and TO-39), figure 2 (die), and figure 3 (surface mount) herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Radiation hardness assurance (RHA). Radiation hardness assurance requirements, PIN designators, and test levels shall be as defined in MIL-PRF-19500.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.7 Marking. Marking shall be in accordance with MIL-PRF-19500. The radiation hardened designator M, D, P, L, R, F, G, or H shall immediately precede (or replace) the device “2N” identifier (depending upon degree of abbreviation required).

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and, tables I, II, and III).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.2.2 JANHC and JANKC qualification. JANHC and JANKC qualification inspection shall be in accordance with MIL-PRF-19500.

4.3 Screening (JANS, JANTX, and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500)	Measurement	
	JANS level	JANTX and JANTXV levels
(1) 3c	Thermal impedance (see 4.3.3)	Thermal impedance (see 4.3.3)
9	I_{CEX1} and h_{FE2}	I_{CEX1}
11	I_{CEX1}; h_{FE2}; ΔI_{CEX1} = 100 percent or 50 nA dc, whichever is greater; Δh_{FE2} = +15, -10 percent change of initial value.	I_{CEX1} and h_{FE2}; ΔI_{CEX1} = 100 percent or 100 nA dc, whichever is greater.
12	See 4.3.1	See 4.3.1
13	Subgroups 2 and 3 of table I herein; ΔI_{CEX1} = 100 percent or 50 nA dc, whichever is greater; Δh_{FE2} = +15, -10 percent of initial value.	Subgroup 2 of table I herein; ΔI_{CEX1} = 100 percent or 100 nA dc, whichever is greater; Δh_{FE2} = +20, -10 percent of initial value.

(1) Shall be performed anytime after temperature cycling, screen 3a; JANTX and JANTXV levels do not need to be repeated in screening requirements.

4.3.1 Power burn-in conditions. Power burn-in conditions are as follows: V_{CB} = 10 - 30 V dc. Power shall be applied to achieve T_J = +175°C minimum and a minimum P_D = 75 percent of P_T maximum rated as defined in 1.3.

4.3.2 Screening JANHC or JANKC. Screening of die shall be in accordance with MIL-PRF-19500.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{SW} (V_C and V_H where appropriate). Measurement delay time (t_{MD}) = 70 μs max. See table III, group E, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500 and table I herein. Electrical measurements (end-points) shall be in accordance with the applicable inspections of table I, subgroup 2 herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VIa (JANS) of MIL-PRF-19500 and 4.4.2.1. Electrical measurements (end-points) shall be in accordance with group A, subgroup 2. See 4.4.2.2 for JAN, JANTX, and JANTXV group B testing. Electrical measurements (end-points) for JAN, JANTX, and JANTXV shall be after each step in 4.4.2.2 and shall be in accordance with table I, subgroup 2 herein.

* 4.4.2.1 Group B inspection, table E-VIa (JANS) of MIL-PRF-19500.

Subgroup	Method	Condition
B3	2037	Test condition D. All internal wires for each device shall be pulled separately.
B4	1037	V_{CE} = 5 V dc, 2,000 cycles, adjust device current, or power, to achieve a minimum ΔT_J of +100°C.
B5	1027	V_{CE} = 5 V dc, P_T adjusted to achieve T_J and time required in MIL-PRF-19500.

4.4.2.2 Group B inspection, (JAN, JANTX, and JANTXV). Separate samples may be used for each step. In the event of a lot failure, the resubmission requirements of MIL-PRF-19500 shall apply. In addition, all catastrophic failures during CI shall be analyzed to the extent possible to identify root cause and corrective action. Whenever a failure is identified as wafer lot and wafer processing related, the entire wafer lot and related devices assembled from the wafer lot shall be rejected unless an appropriate determined corrective action to eliminate the failures mode has been implemented and the devices from the wafer lot are screened to eliminate the failure mode.

Step	Method	Condition
1	1026	Steady-state life: 1,000 hours minimum, V_{CB} = 10 V dc, power shall be applied to achieve T_J = +150°C minimum using a minimum of P_D = 75 percent of maximum rated P_T as defined in 1.3. n = 45 devices, c = 0. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.
2	1048	Blocking life, T_A = +150°C, V_{CB} = 80 percent of rated voltage, 48 hours minimum. n = 45 devices, c = 0.
3	1032	High-temperature life (non-operating), t = 340 hours, T_A = +200°C. n = 22, c = 0.

4.4.2.3 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

a. For JAN, JANTX, and JANTXV samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot. For JANS, samples shall be selected from each inspection lot. See MIL-PRF-19500.

b. Shall be chosen from an inspection lot that has been submitted to and passed table I, subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (subgroups B4 and B5 for JANS, and group B for JAN, JANTX, and JANTXV) may be pulled prior to the application of final lead finish.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.4.3.1 Group C inspection, table E-VII of MIL-PRF-19500.

Subgroup	Method	Condition
C2	2036	Test condition E, not applicable for U4.
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see 1.3) and in accordance with thermal impedance curves.
C6	1026	T_A = +25 ±5°C; T_J = +150°C minimum. (Not applicable to JAN, JANTX, and JANTXV). V_{CB} = 40 V dc for types 2N3418, 2N3418S, 2N3418U4, 2N3420, 2N3420S, and 2N3420U4. V_{CB} = 60 V dc for types 2N3419, 2N3419S, 2N3419U4, 2N3421, 2N3421S, and 2N3421U4.

4.4.3.2 Group C sample selection. Samples for subgroups in group C shall be chosen at random from any inspection lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes table I tests for conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for C6 life test may be pulled prior to the application of final lead finish. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

* 4.4.4 Group D inspection. Conformance inspection for hardness assured JANS and JANTXV types shall include the group D tests specified in table II herein. These tests shall be performed as required in accordance with MIL-PRF-19500 and method 1019 of MIL-STD-750, for total ionizing dose or method 1017 of MIL-STD-750 for neutron fluence as applicable (see 6.2 herein), except group D, subgroup 2 may be performed separate from other subgroups. Alternate package options may also be substituted for the testing provided there is no adverse effect to the fluence profile.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in appendix E, table E-IX of MIL-PRF-19500 and as specified in table III herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

TABLE I. Group A inspection.

	Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
		Method	Conditions		Min	Max	
	Subgroup 1 2/						
	Visual and mechanical examination 3/	2071					
	Solderability 3/ 4/	2026	n = 15 leads, c = 0				
	Resistance to solvents 3/ 4/ 5/	1022	n = 15 devices, c = 0				
	Temp cycling 3/ 4/	1051	Test condition C, 25 cycles. n = 22 devices, c = 0				
	Hermetic seal 4/ Fine leak Gross leak	1071	n = 22 devices, c = 0				
	Electrical measurements 4/		Table I, subgroup 2				
	Bond strength 3/ 4/	2037	Precondition T_A = +250°C at t = 24 hrs or T_A = +300°C at t = 2 hrs n = 11 wires, c = 0				
	Subgroup 2						
*	Thermal impedance	3131	See 4.3.3	$Z_{\theta JX}$			°C/W
	Breakdown voltage collector to emitter	3011	Bias condition D; I_C = 50 mA dc, I_B = 0, pulsed (see 4.5.1)	$V_{(BR)CEO}$			
	2N3418, 2N3418S 2N3420, 2N3420S 2N3418U4, 2N3420U4				60		V dc
	2N3419, 2N3419S 2N3421, 2N3421S 2N3419U4, 2N3421U4				80		V dc
	Collector to emitter cutoff current	3041	Bias condition A; V_{BE} = -0.5 V dc	I_{CEX1}			
	2N3418, 2N3418S 2N3420, 2N3420S 2N3418U4, 2N3420U4		V_{CE} = 80 V dc			0.3	µA dc
	2N3419, 2N3419S 2N3421, 2N3421S 2N3419U4, 2N3421U4		V_{CE} = 120 V dc			0.3	µA dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - Continued						
Collector to emitter cutoff current	3041	Bias condition D; $I_B = 0$	I_{CEO}			
2N3418, 2N3418S 2N3420, 2N3420S 2N3418U4, 2N3420U4		V_{CE} = 45 V dc			5.0	μA dc
2N3419, 2N3419S 2N3421, 2N3421S 2N3419U4, 2N3421U4		V_{CE} = 60 V dc			5.0	μA dc
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 6 V dc, $I_C = 0$	I_{EBO1}		0.5	μA dc
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 8 V dc, $I_C = 0$	I_{EBO2}		10	μA dc
Forward current transfer ratio	3076	V_{CE} = 2 V dc; I_C = 100 mA dc, pulsed (see 4.5.1)	h_{FE1}			
2N3418, 2N3418S 2N3418U4, 2N3419, 2N3419S, 2N3419U4				20		
2N3420, 2N3420S, 2N3420U4, 2N3421, 2N3421S, 2N3421U4				40		
Forward current transfer ratio	3076	V_{CE} = 2 V dc; I_C = 1.0 A dc, pulsed (see 4.5.1)	h_{FE2}			
2N3418, 2N3418S, 2N3418U4, 2N3419, 2N3419S, 2N3419U4				20	60	
2N3420, 2N3420S, 2N3420U4, 2N3421, 2N3421S, 2N3421U4				40	120	
Forward current transfer ratio	3076	V_{CE} = 2 V dc; I_C = 2 A dc, pulsed (see 4.5.1)	h_{FE3}			
2N3418, 2N3418S, 2N3418U4, 2N3419, 2N3419S, 2N3419U4				15		
2N3420, 2N3420S, 2N3420U4, 2N3421, 2N3421S, 2N3421U4				30		

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - Continued						
Forward current transfer ratio 2N3418, 2N3418S, 2N3418U4, 2N3419, 2N3419S, 2N3419U4 2N3420, 2N3420S, 2N3420U4, 2N3421, 2N3421S, 2N3421U4	3076	V_{CE} = 5 V dc; I_C = 5 A dc, pulsed (see 4.5.1)	h_{FE4}	 10 15		
Base-emitter voltage (saturated)	3066	Test condition A; I_C = 1.0 A dc, I_B = 0.1 A dc, pulsed (see 4.5.1)	$V_{BE(sat)1}$ 6/	0.6	1.2	V dc
Base-emitter voltage (saturated)	3066	Test condition A; I_C = 2.0 A dc, I_B = 0.2 A dc, pulsed (see 4.5.1)	$V_{BE(sat)2}$ 6/	0.7	1.4	V dc
Saturation voltage and resistance (collector-emitter)	3071	I_C = 1.0 A dc, I_B = 0.1 A dc, pulsed (see 4.5.1)	$V_{CE(sat)1}$ 6/		0.25	V dc
Saturation voltage and resistance (collector-emitter)	3071	I_C = 2.0 A dc, I_B = 0.2 A dc, pulsed (see 4.5.1)	$V_{CE(sat)2}$ 6/		0.5	V dc
Subgroup 3						
High-temperature operation:		T_A = +150°C				
Collector to emitter cutoff current	3041	Bias condition A; V_{BE} = -0.5 V dc	I_{CEX2}			
2N3418, 2N3418S 2N3420, 2N3420S 2N3418U4, 2N3420U4		V_{CE} = 80 V dc			16	µA dc
2N3419, 2N3419S 2N3421, 2N3421S 2N3419U4, 2N3421U4		V_{CE} = 120 V dc			16	µA dc
Low-temperature operation:		T_A = -55°C				
Forward current transfer ratio	3076	V_{CE} = 2 V dc, I_C = 1 A dc pulsed (see 4.5.1)	h_{FE5}	10		
Subgroup 4						
Small-signal short-circuit forward-current transfer ratio magnitude of common emitter	3306	V_{CE} = 10 V dc; I_C = 0.1 A dc; f = 20 MHz	$\|h_{fe}\|$	1.3	8	

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 4 - Continued						
Open-circuit output capacitance	3236	V_{CB} = 10 V dc, I_E = 0 , 100 kHz ≤ f ≤ 1 MHz	C_{obo}		150	pF
Switching time		I_C = 1.0 A dc, $I_{B(1)}$ = 100 mA dc, $I_{B(2)}$ = -100 mA dc $V_{BE(off)}$ = -3.7 V dc, R_L = 20 Ω, see figure 10	t_r t_d t_s t_f t_{off}		0.22 0.08 1.10 0.20 1.20	µs µs µs µs µs
Subgroup 5						
Safe operating area (continuous dc)	3051	T_C = +100°C, t ≥ 1 s, 1 cycle, see figure 11				
Test 1		I_C = 3 A dc, V_{CE} = 5 V dc				
Test 2		I_C = 0.4 A dc, V_{CE} = 37 V dc				
Test 3						
2N3418, 2N3418S 2N3418U4, 2N3420, 2N3420S, 2N3420U4		I_C = 0.185 A dc, V_{CE} = 60 V dc				
2N3419, 2N3419S 2N3419U4, 2N3421, 2N3421S, 2N3421U4		I_C = 0.12 A dc, V_{CE} = 80 V dc				
Safe operating area (clamped switching)	3053	T_A = +25°C, I_B = 0.5 A dc, I_C = 3.0 A dc, see figure 12				
Electrical measurements		See subgroup 2 herein				
Subgroup 6 and 7						
Not applicable						

1/ For sampling plan see MIL-PRF-19500.
2/ For resubmission of failed subgroup 1, double the sample size of the failed test or sequence of tests. A failure in table I, subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.
3/ Separate samples may be used.
4/ Not required for JANS devices.
5/ Not required for laser marked devices.
6/ Measured at a point on the leads no further than .125 inch (3.18 mm) from the case.

TABLE II. Group D inspection.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 1 4/						
Neutron irradiation	1017	Neutron exposure V_{CES} = 0 V				
Breakdown voltage collector to emitter	3011	Bias condition D; I_C = 50 mA dc, I_B = 0, pulsed (see 4.5.1)	$V_{(BR)CEO}$			
2N3418, 2N3418S 2N3420, 2N3420S 2N3418U4, 2N3420U4				60		V dc
2N3419, 2N3419S 2N3421, 2N3421S 2N3419U4, 2N3421U4				80		V dc
Collector to emitter cutoff current	3041	Bias condition A; V_{BE} = -0.5 V dc	I_{CEX1}			
2N3418, 2N3418S 2N3420, 2N3420S 2N3418U4, 2N3420U4		V_{CE} = 80 V dc			0.6	µA dc
2N3419, 2N3419S 2N3421, 2N3421S 2N3419U4, 2N3421U4		V_{CE} = 120 V dc			0.6	µA dc
Collector to emitter cutoff current	3041	Bias condition D; I_B = 0	I_{CEO}			
2N3418, 2N3418S 2N3420, 2N3420S 2N3418U4, 2N3420U4		V_{CE} = 45 V dc			10	µA dc
2N3419, 2N3419S 2N3421, 2N3421S 2N3419U4, 2N3421U4		V_{CE} = 60 V dc			10	µA dc
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 6 V dc, I_C = 0	I_{EBO1}		1.0	µA dc
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 8 V dc, I_C = 0	I_{EBO2}		20	µA dc
Forward current transfer ratio	3076	V_{CE} = 2 V dc; I_C = 100 mA dc, pulsed (see 4.5.1)	[h_{FE1}] 5/			
2N3418, 2N3418S 2N3418U4, 2N3419, 2N3419S, 2N3419U4				[10]		
2N3420, 2N3420S, 2N3420U4, 2N3421, 2N3421S, 2N3421U4				[20]		

See footnotes at end of table.

TABLE II. Group D inspection - Continued.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 1 4/ - Continued						
Forward current transfer ratio 2N3418, 2N3418S, 2N3418U4, 2N3419, 2N3419S, 2N3419U4 2N3420, 2N3420S, 2N3420U4, 2N3421, 2N3421S, 2N3421U4	3076	V_{CE} = 2 V dc; I_C = 1.0 A dc, pulsed (see 4.5.1)	[h_{FE2}] 5/	[10] [20]	60 120	
Forward current transfer ratio 2N3418, 2N3418S, 2N3418U4, 2N3419, 2N3419S, 2N3419U4 2N3420, 2N3420S, 2N3420U4, 2N3421, 2N3421S, 2N3421U4	3076	V_{CE} = 2 V dc; I_C = 2 A dc, pulsed (see 4.5.1)	[h_{FE3}] 5/	[7.5] [15]		
Forward current transfer ratio 2N3418, 2N3418S, 2N3418U4, 2N3419, 2N3419S, 2N3419U4 2N3420, 2N3420S, 2N3420U4, 2N3421, 2N3421S, 2N3421U4	3076	V_{CE} = 5 V dc; I_C = 5 A dc, pulsed (see 4.5.1)	[h_{FE4}] 5/	[5} [7.5]		
Base-emitter voltage (saturated)	3066	Test condition A; I_C = 1.0 A dc, I_B = 0.1 A dc, pulsed (see 4.5.1)	$V_{BE(sat)1}$ 6/	0.69	1.38	V dc
Base-emitter voltage (saturated)	3066	Test condition A; I_C = 2.0 A dc, I_B = 0.2 A dc, pulsed (see 4.5.1)	$V_{BE(sat)2}$ 6/	0.81	1.61	V dc
Saturation voltage and resistance (collector-emitter)	3071	I_C = 1.0 A dc, I_B = 0.1 A dc, pulsed (see 4.5.1)	$V_{CE(sat)1}$ 6/		0.29	V dc
Saturation voltage and resistance (collector-emitter)	3071	I_C = 2.0 A dc, I_B = 0.2 A dc, pulsed (see 4.5.1)	$V_{CE(sat)2}$ 6/		0.58	V dc

See footnotes at end of table.

TABLE II. Group D inspection - Continued.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 2						
Total dose irradiation	1019	Gamma exposure				
2N3418, 2N3418S		V_{CES} = 48 V				
2N3420, 2N3420S		V_{CES} = 48 V				
2N3418U4, 2N3420U4		V_{CES} = 48 V				
2N3419, 2N3419S		V_{CES} = 64 V				
2N3421, 2N3421S		V_{CES} = 64 V				
2N3419U4, 2N3421U4		V_{CES} = 64 V				
Breakdown voltage collector to emitter	3011	Bias condition D; I_C = 50 mA dc, I_B = 0, pulsed (see 4.5.1)	$V_{(BR)CEO}$			
2N3418, 2N3418S				60		V dc
2N3420, 2N3420S						
2N3418U4, 2N3420U4						
2N3419, 2N3419S				80		V dc
2N3421, 2N3421S						
2N3419U4, 2N3421U4						
Collector to emitter cutoff current	3041	Bias condition A; V_{BE} = -0.5 V dc	I_{CEX1}			
2N3418, 2N3418S		V_{CE} = 80 V dc			0.6	µA dc
2N3420, 2N3420S						
2N3418U4, 2N3420U4						
2N3419, 2N3419S		V_{CE} = 120 V dc			0.6	µA dc
2N3421, 2N3421S						
2N3419U4, 2N3421U4						
Collector to emitter cutoff current	3041	Bias condition D; I_B = 0	I_{CEO}			
2N3418, 2N3418S		V_{CE} = 45 V dc			10	µA dc
2N3420, 2N3420S						
2N3418U4, 2N3420U4						
2N3419, 2N3419S		V_{CE} = 60 V dc			10	µA dc
2N3421, 2N3421S						
2N3419U4, 2N3421U4						
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 6 V dc, I_C = 0	I_{EBO1}		1.0	µA dc
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 8 V dc, I_C = 0	I_{EBO2}		20	µA dc

See footnotes at end of table.

TABLE II. Group D inspection - Continued.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - Continued						
Forward current transfer ratio 2N3418, 2N3418S 2N3418U4, 2N3419, 2N3419S, 2N3419U4 2N3420, 2N3420S, 2N3420U4, 2N3421, 2N3421S, 2N3421U4	3076	V_{CE} = 2 V dc; I_C = 100 mA dc, pulsed (see 4.5.1)	[h_{FE1}] 5/	[10] [20]		
Forward current transfer ratio 2N3418, 2N3418S, 2N3418U4, 2N3419, 2N3419S, 2N3419U4 2N3420, 2N3420S, 2N3420U4, 2N3421, 2N3421S, 2N3421U4	3076	V_{CE} = 2 V dc; I_C = 1.0 A dc, pulsed (see 4.5.1)	[h_{FE2}] 5/	[10] [20]	60 120	
Forward current transfer ratio 2N3418, 2N3418S, 2N3418U4, 2N3419, 2N3419S, 2N3419U4 2N3420, 2N3420S, 2N3420U4, 2N3421, 2N3421S, 2N3421U4	3076	V_{CE} = 2 V dc; I_C = 2 A dc, pulsed (see 4.5.1)	[h_{FE3}] 5/	[7.5] [15]		
Forward current transfer ratio 2N3418, 2N3418S, 2N3418U4, 2N3419, 2N3419S, 2N3419U4 2N3420, 2N3420S, 2N3420U4, 2N3421, 2N3421S, 2N3421U4	3076	V_{CE} = 5 V dc; I_C = 5 A dc, pulsed (see 4.5.1)	[h_{FE4}] 5/	[5} [7.5]		
Base-emitter voltage (saturated)	3066	Test condition A; I_C = 1.0 A dc, I_B = 0.1 A dc, pulsed (see 4.5.1)	$V_{BE(sat)1}$ 6/	0.69	1.38	V dc
Base-emitter voltage (saturated)	3066	Test condition A; I_C = 2.0 A dc, I_B = 0.2 A dc, pulsed (see 4.5.1)	$V_{BE(sat)2}$ 6/	0.81	1.61	V dc

See footnotes at end of table.

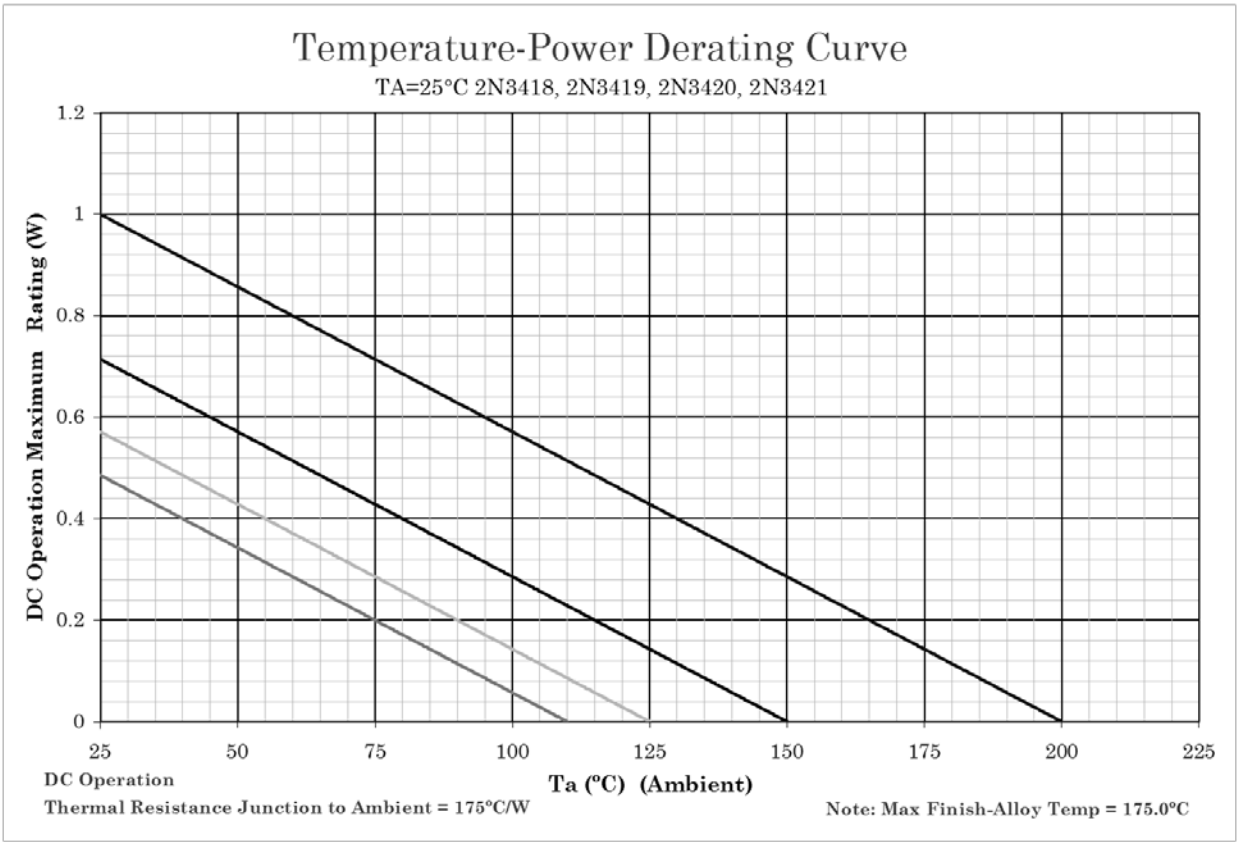
TABLE II. Group D inspection - Continued.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - Continued						
Saturation voltage and resistance (collector-emitter)	3071	I_C = 1.0 A dc, I_B = 0.1 A dc, pulsed (see 4.5.1)	$V_{CE(sat)1}$ 6/		0.29	V dc
Saturation voltage and resistance (collector-emitter)	3071	I_C = 2.0 A dc, I_B = 0.2 A dc, pulsed (see 4.5.1)	$V_{CE(sat)2}$ 6/		0.58	V dc

1/ Tests to be performed on all devices receiving radiation exposure.
2/ For sampling plan, see MIL-PRF-19500.
3/ Electrical characteristics apply to the corresponding U4 suffix versions unless otherwise noted.
4/ See 6.2.g herein.
5/ See method 1019 of MIL-STD-750 for how to determine [h_{FE}] by first calculating the delta ($1/h_{FE}$) from the pre- and Post-radiation h_{FE}. Notice the [h_{FE}] is not the same as h_{FE} and cannot be measured directly. The [h_{FE}] value can never exceed the pre-radiation minimum h_{FE} that it is based upon.
6/ Measured at a point on the leads no more than .125 inch (3.18 mm) from the case.

* TABLE III. Group E inspection (all quality levels) - for qualification and re-qualification only.

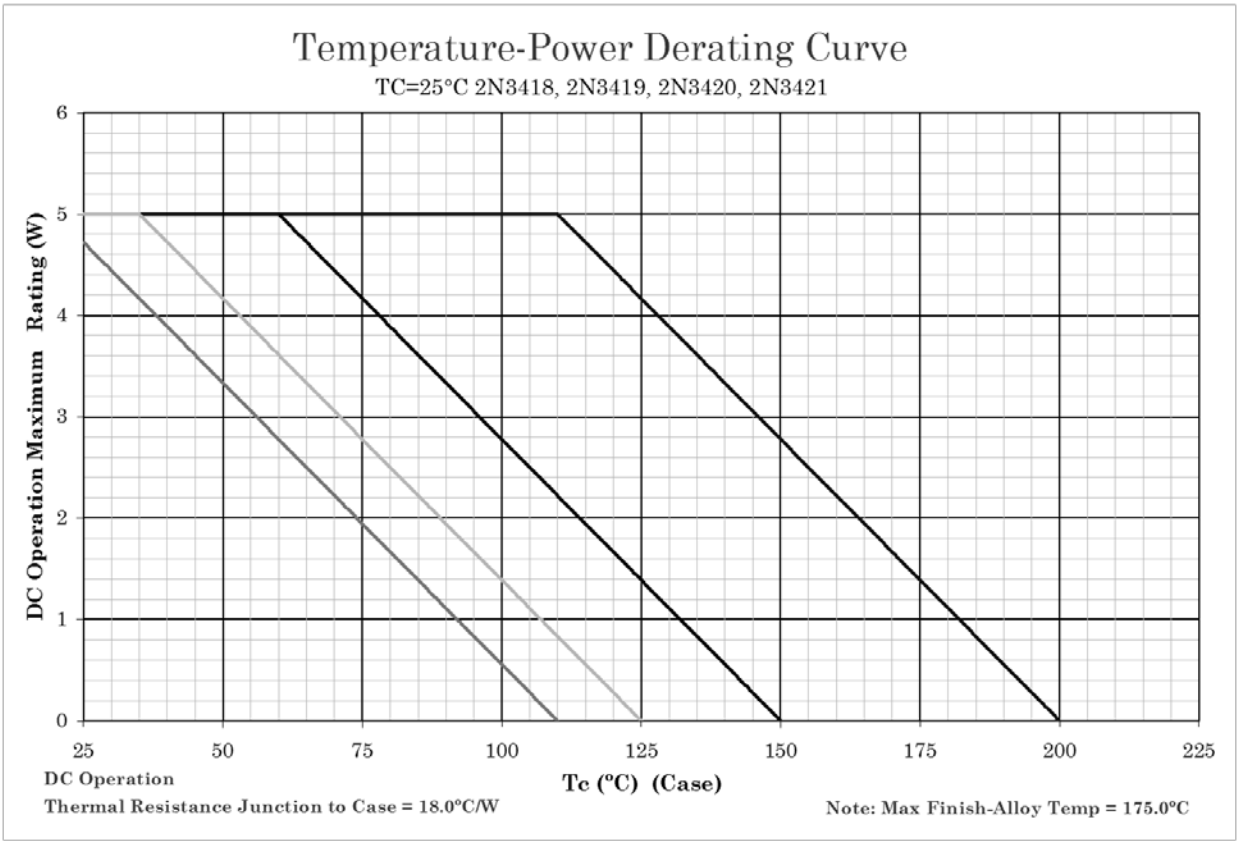
Inspection	MIL-STD-750		Qualification
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles	
Hermetic seal Fine leak Gross leak	1071		
Electrical measurements		See table I, subgroup 2.	
Subgroup 2			45 devices c = 0
Intermittent life	1037	Intermittent operation life: V_{CB} = 10 V dc, 6,000 cycles. Adjust device current, or power, to achieve a minimum ΔT_J of +100°C.	
Electrical measurements		See table I, subgroup 2.	
Subgroup 4			
Thermal impedance curves		See MIL-PRF-19500, table E-IX, group E, subgroup 4.	
Subgroup 5			
Not applicable			
* Subgroup 6			
ESD	1020		
Subgroup 8			45 devices c = 0
Reverse stability	1033	Condition B.	



NOTES:

1. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

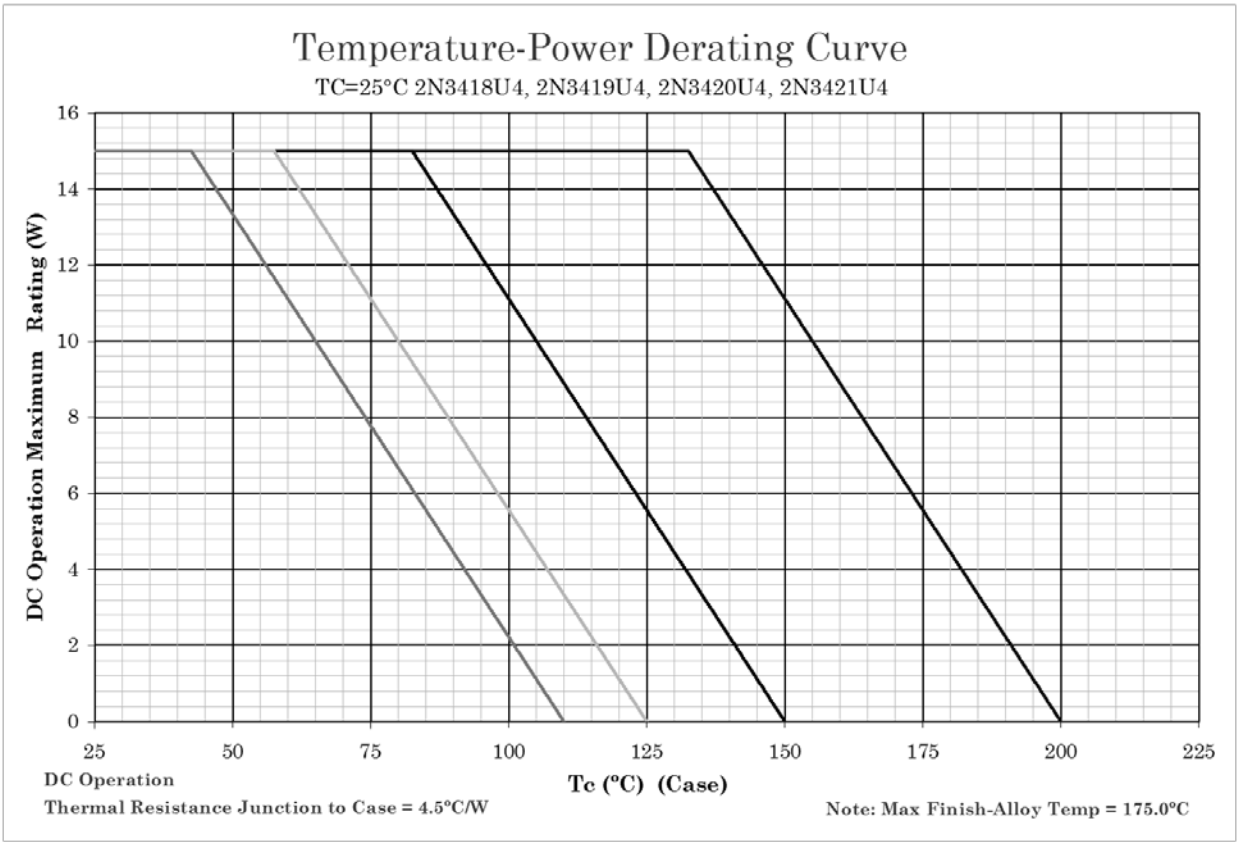
FIGURE 4. Derating for 2N3418, 2N3418S, 2N3419, 2N3419S, 2N3420, 2N3420S, 2N3421, and 2N3421S ($R_{\theta JA}$) leads .375 inch (9.53 mm) PCB (TO-5 and TO-39).



NOTES:

1. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

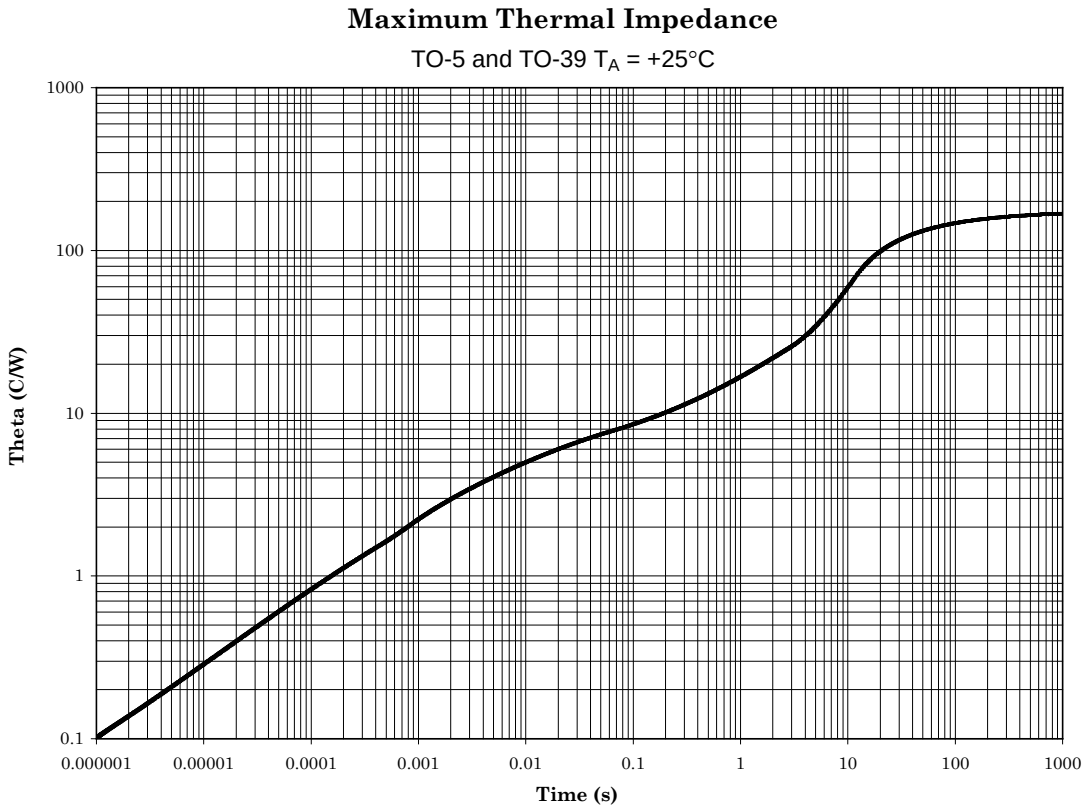
FIGURE 5. Derating for 2N3418, 2N3418S, 2N3419, 2N3419S, 2N3420, 2N3420S, 2N3421, and 2N3421S ($R_{\theta JC}$) (TO-5 and TO-39).



NOTES:

1. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 6. Derating for 2N3418U4, 2N3419U4, 2N3420U4, and 2N3421U4 ($R_{\theta JC}$) (U4).

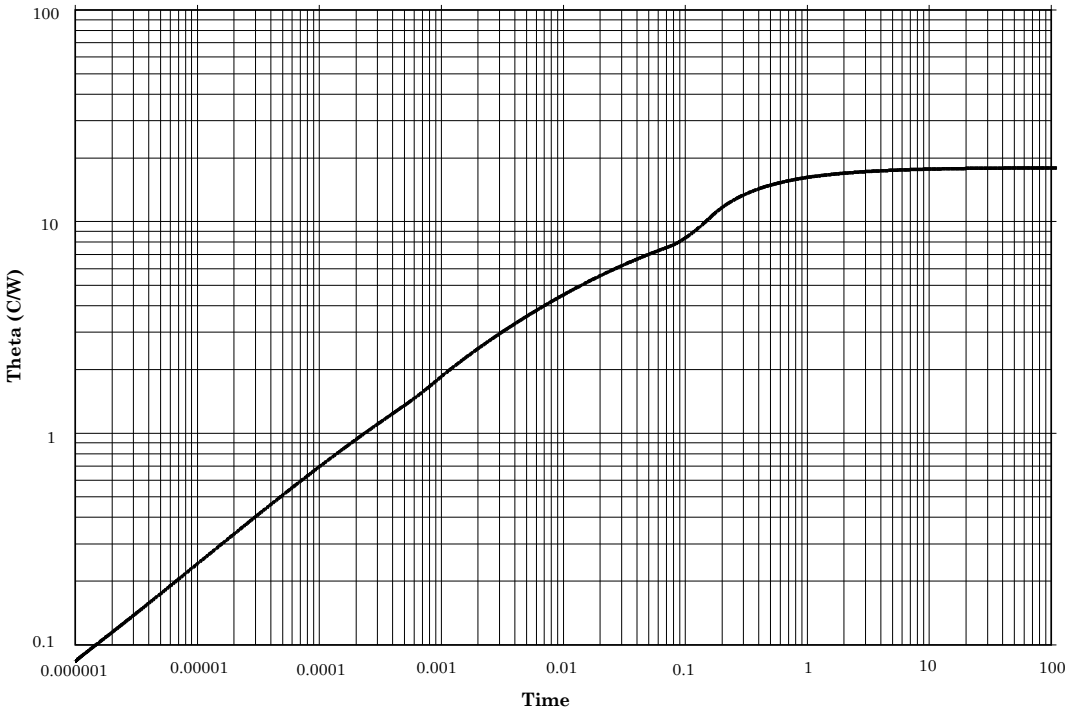


T_A = +25°C, P_{diss} = 1.0 W, Thermal Resistance $R_{\theta JA}$ = 175°C/W

FIGURE 7. Thermal impedance graph ($R_{\theta JA}$) for 2N3418, 2N3418S, 2N3419, 2N3419S, 2N3420, 2N3420S, 2N3421, and 2N3421S leads .375 inch PCB (TO-5 and TO-39).

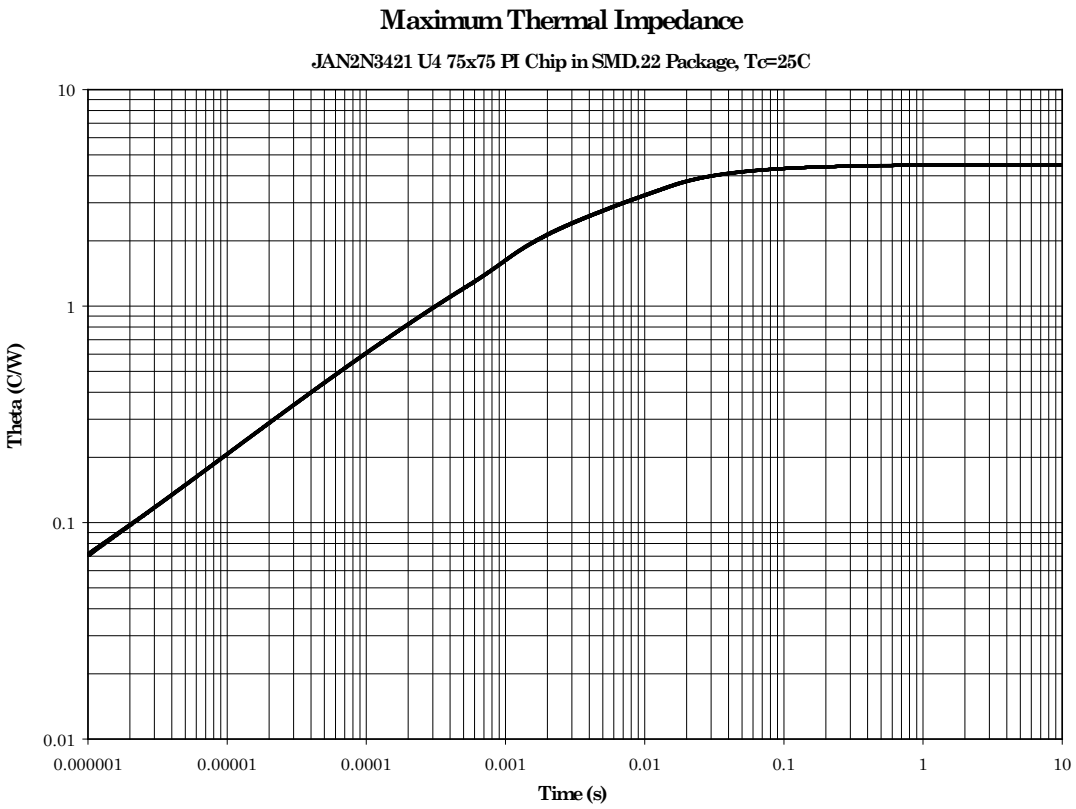
Maximum Thermal

TO-5 and TO-39 T_c = +25°C



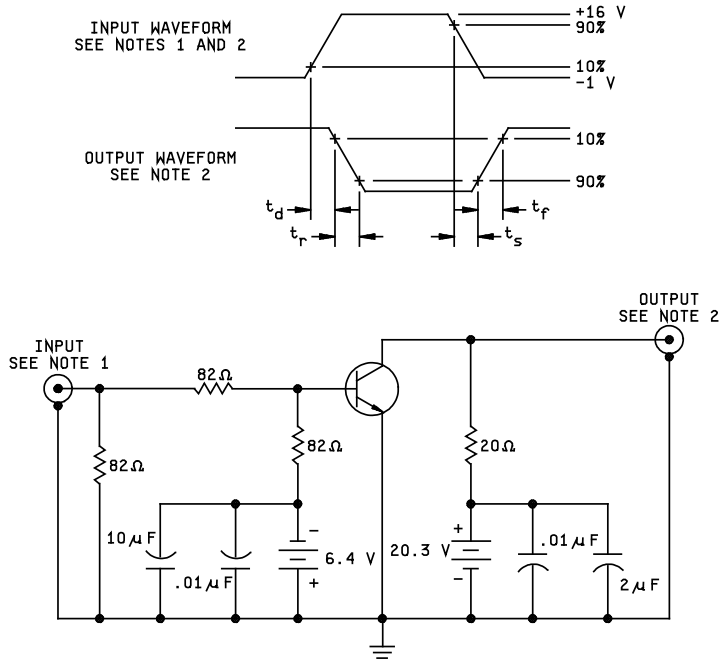
T_c = +25°C, Thermal Resistance $R_{\theta JC}$ = 18°C/W

FIGURE 8. Thermal impedance graph ($R_{\theta JC}$) for 2N3418, 2N3418S, 2N3419, 2N3419S, 2N3420, 2N3420S, 2N3421, and 2N3421S (TO-5 and TO-39).



T_c = +25°C, Thermal Resistance $R_{\theta JC}$ = 4.5°C/W, $R_{\theta JX}$ =3.25°C/W at 10ms

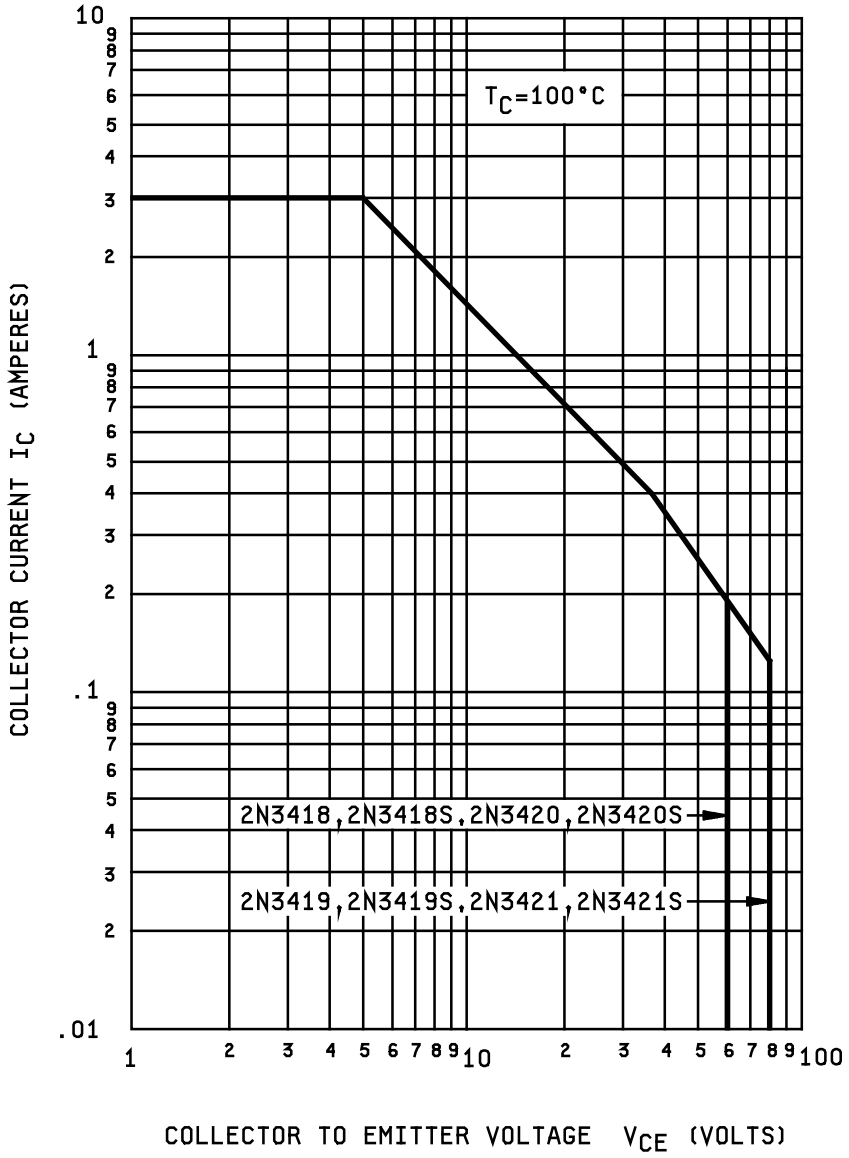
FIGURE 9. Thermal impedance graph ($R_{\theta JC}$) for 2N3418U4, 2N3419U4, 2N3420U4 and 2N3421U4 PCB (U4).



NOTES:

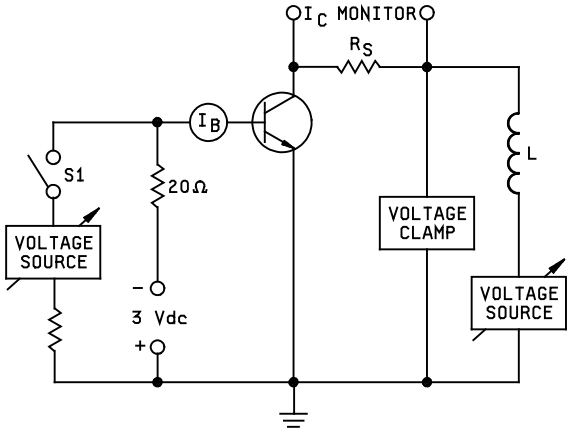
1. The input waveform is supplied by a pulse generator with the following characteristics: $t_r \leq 15$ ns, $t_f \leq 15$ ns, $Z_{OUT} = 50\ \Omega$, PW = 2 μs, duty cycle ≤ 2 percent.
2. Output waveforms are monitored by an oscilloscope with the following characteristics: $t_r \leq 15$ ns, $R_{in} \geq 10\ M\Omega$, $C_{in} \leq 11.5$ pF.
3. Resistors shall be noninductive types.
4. The dc power supplies may require additional by-passing in order to minimize ringing.

FIGURE 10. Pulse response test circuit.



NOTES:
1. The 2N3418U4 and 2N3420U4 devices follow the 2N3418 devices.
2. The 2N3419U4 and 2N3421U4 devices follow the 2N3419 devices.

FIGURE 11. Maximum safe operating region.



NOTES:

Voltage clamp: 2N3418, 2N2418S, 2N3418U4, 2N3420, 2N3420S, and 2N3420U4 = 85 V dc.
2N3419, 2N3419S, 2N3419U4, 2N3421, 2N3421S, and 2N3421U4 = 125 V dc.

$R_S \leq 1.0\ \Omega$ (noninductive), L = 40 mH

Procedure:

1. With switch S_1 closed, set the specified test conditions.
2. Open S_1.
3. Perform specified end-point tests.

FIGURE 12. Clamped inductive sweep test circuit diagram.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. Product assurance level and type designator.

e. For acquisition of RHA designed devices, table II, subgroup 1 testing of group D is optional. If subgroup 1 testing is desired, it must be specified in the contract.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil .