NXP Semiconductors
Technical Data

Document Number: MC35XS3400
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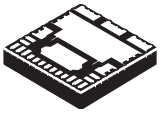
Quad high-side switch (quad 35 mOhm)

35XS3400

HIGH-SIDE SWITCH



FK SUFFIX (PB-FREE)
98ARL10596D
24-PIN PQFN

The 35XS3400 is one in a family of devices designed for low-voltage automotive lighting applications. Its four low $R_{DS(on)}$ MOSFETs (quad 35 mOhm) can control four separate 28 W bulbs, and/or LEDs.

Programming, control and diagnostics are accomplished using a 16-bit SPI interface. Its output with selectable slew rate improves electromagnetic compatibility (EMC) behavior. Additionally, each output has its own parallel input or SPI control for pulse-width modulation (PWM) control. The 35XS3400 allows the user to program via the SPI the fault current trip levels and duration of acceptable lamp inrush. The device has Fail-safe mode to provide functionality of the outputs in case of MCU damage. This device is powered by SMARTMOS technology.

Features

- Four protected 35 mΩ high-side switches (at 25 °C)
- Operating voltage range of 6.0 V to 20 V with standby current < 5.0 μA, extended mode from 4.0 V to 28 V
- 8.0 MHz 16-bit 3.3 V and 5.0 V SPI control and status reporting with daisy chain capability
- PWM module using external clock or calibratable internal oscillator with programmable outputs delay management
- Smart overcurrent shutdown, severe short-circuit, overtemperature protection with time limited autoretry, and Fail-safe mode in case of MCU damage
- Output OFF or ON openload detection compliant to bulbs or LEDs and short to battery detection
- Analog current feedback with selectable ratio and board temperature feedback

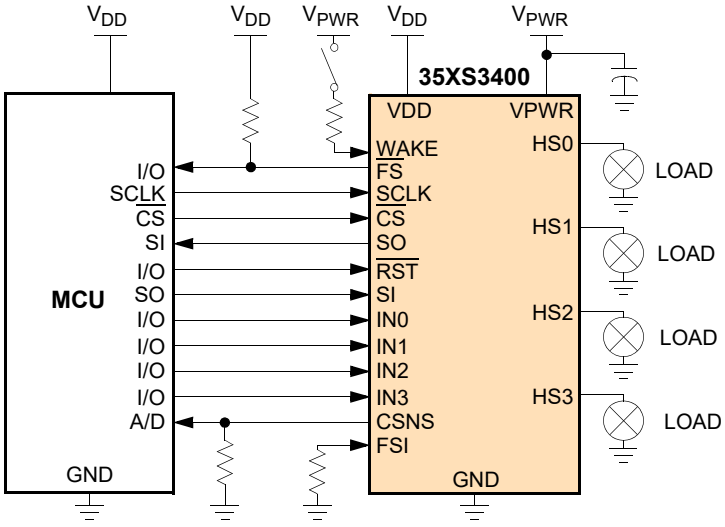


Figure 1. 35XS3400 simplified application diagram

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1 Orderable parts

This section describes the part numbers available to be purchased along with their differences. Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to http://www.nxp.com and perform a part number search for the following device numbers.

Table 1. Orderable part variations

Part number [1]	Temperature (T_A)	Package
MC35XS3400CHFK	-40 °C to 125 °C	24-pin PQFN
MC35XS3400DHFK		

Notes
1. To order parts in tape and reel, add the R2 suffix to the part number.

2 Device variations

Table 2. Device variations

Characteristic	Symbol	Min	Typ	Max	Unit
Wake input clamp voltage, $I_{CL(WAKE)}$ < 2.5 mA • 35XS3400CHFK • 35XS3400DHFK	$V_{CL(WAKE)}$	 18 20	 25 27	 32 35	V
Fault detection blanking time • 35XS3400CHFK • 35XS3400DHFK	t_{FAULT}	 - -	 5.0 5.0	 20 10	µs
Output shutdown delay time • 35XS3400CHFK • 35XS3400DHFK	t_{DETECT}	 - -	 7.0 7.0	 30 20	µs
Openload detection time in OFF state [2] • 35XS3400CHFK and 35XS3400DHFK	t_{OLOFF}	170	212	270	µs
Peak Package Reflow Temperature During Reflow[3], [4]	T_{PPRT}	Note 4			°C

Notes
2. Guaranteed by design.
3. Pin soldering temperature limit is for 40 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
4. NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to www.nxp.com, search by part number (remove prefixes/suffixes) and enter the core ID to view all orderable parts, and review parametrics.

3 Internal block diagram

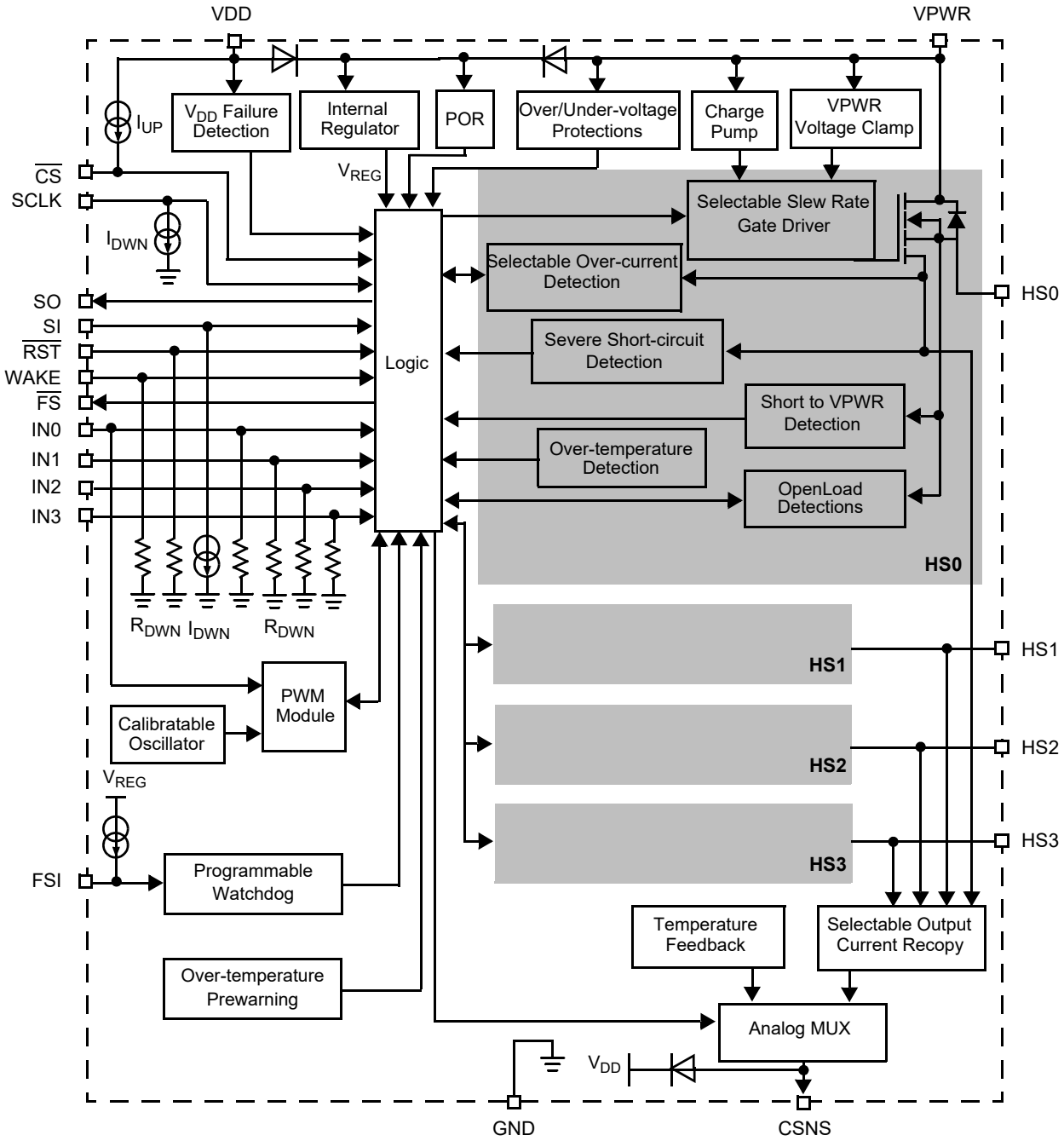


Figure 2. 35XS3400 simplified internal block diagram

4 Pin connections

Transparent Top View of Package

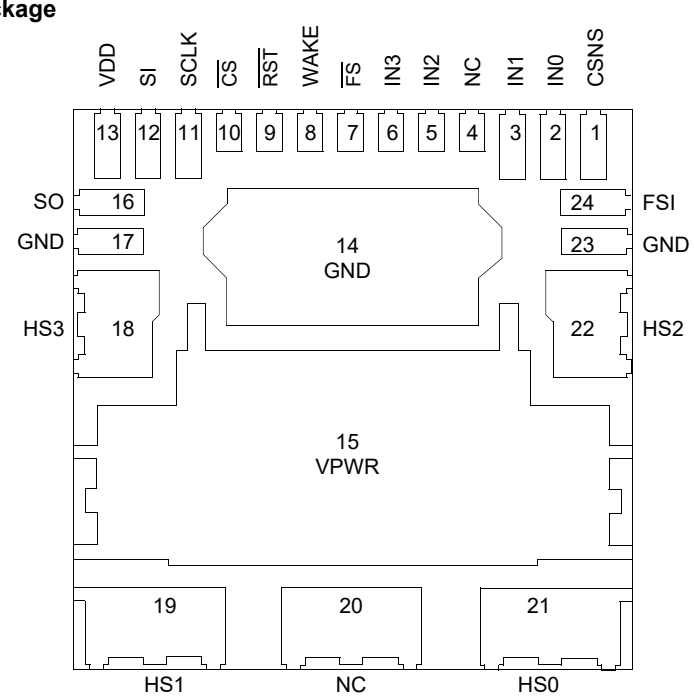


Figure 3. 35XS3400 pin connections

Table 3. 35XS3400 pin definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 20.

Pin number	Pin name	Pin function	Formal name	Definition
1	CSNS	Output	Output current monitoring	This pin reports an analog value proportional to the designated HS[0:3] output current or the temperature of the GND flag (pin 14). It is used externally to generate a ground-referenced voltage for the microcontroller (MCU). Current recopy and temperature feedback is SPI programmable.
2 3 5 6	IN0 IN1 IN2 IN3	Input	Direct inputs	Each direct input controls the device mode. The IN[0:3] high-side input pins are used to directly control HS0:HS3 high-side output pins. The PWM frequency can be generated from IN0 pin to PWM module in case the external clock is set.
7	$\overline{FS}$	Output	Fault status (active low)	This pin is an open drain configured output requiring an external pull-up resistor to V_{DD} for fault reporting.
8	WAKE	Input	Wake	This input pin controls the device mode.
9	$\overline{RST}$	Input	Reset	This input pin is used to initialize the device configuration and fault registers, as well as place the device in a low-current Sleep mode.
10	$\overline{CS}$	Input	Chip Select (active low)	This input pin is connected to a chip select output of a master microcontroller (MCU).
11	SCLK	Input	Serial clock	This input pin is connected to the MCU providing the required bit shift clock for SPI communication.
12	SI	Input	Serial input	This pin is a command data input pin connected to the SPI serial data output of the MCU or to the SO pin of the previous device of a daisy-chain of devices.
13	VDD	Power	Digital drain voltage	This pin is an external voltage input pin used to supply power interfaces to the SPI bus.

Table 3. 35XS3400 pin definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 20.

Pin number	Pin name	Pin function	Formal name	Definition
14, 17, 23	GND	Ground	Ground	These pins, internally shorted, are the ground for the logic and analog circuitry of the device. These ground pins must be also shorted in the board.
15	VPWR	Power	Positive power supply	This pin connects to the positive power supply and is the source of operational power for the device.
16	SO	Output	Serial output	This output pin is connected to the SPI serial data input pin of the MCU or to the SI pin of the next device of a daisy-chain of devices.
18 19 21 22	HS3 HS1 HS0 HS2	Output	High-side outputs	Protected 35 mΩ high-side power output pins to the load.
4, 20	NC	N/A	No connect	These pins may not be connected.
24	FSI	Input	Fail-safe input	This input enables the watchdog timeout feature.

5 Electrical characteristics

5.1 Maximum ratings

Table 4. Maximum ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
V_{PWR} supply voltage range • Load dump at 25 °C (400 ms) • Maximum operating voltage • Reverse battery at 25 °C (2.0 min.)	$V_{PWR(SS)}$	41 28 -18	V
V_{DD} supply voltage range	V_{DD}	-0.3 to 5.5	V
Input/output voltage	(8)	-0.3 to V_{DD}+0.3	V
WAKE input clamp current	$I_{CL(WAKE)}$	2.5	mA
CSNS input clamp current	$I_{CL(CSNS)}$	2.5	mA
HS [0:3] voltage • Positive • Negative	$V_{HS[0:3]}$	41 -16	V
Output current(5)	$I_{HS[0:3]}$	6	A
Output clamp energy using single-pulse method(6)	$E_{CL[0:3]}$	35	mJ
ESD voltage(7) • Human Body Model (HBM) for HS[0:3], VPWR and GND • Human Body Model (HBM) for other pins • Charge Device Model (CDM) Corner pins (1, 13, 19, 21) All other pins (2-12, 14-18, 20, 22-24)	V_{ESD1} V_{ESD2} V_{ESD3} V_{ESD4}	±8000 ±2000 ±750 ±500	V
THERMAL RATINGS			
Operating temperature • Ambient • Junction	T_A T_J	-40 to 125 -40 to 150	°C
Storage Temperature	T_{STG}	-55 to 150	°C
THERMAL RESISTANCE			
Thermal resistance(9) • Junction to Case • Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	<1.0 30	°C/W
Peak Package Reflow Temperature During Reflow(10), (11)	T_{PPRT}	Note 11	°C

Notes

5. Continuous high-side output current rating so long as maximum junction temperature is not exceeded. Calculation of maximum output current using package thermal resistance is required.
6. Active clamp energy using single-pulse method (L = 2.0 mH, R_L = 0 Ω, V_{PWR} = 14 V, T_J = 150 °C initial).
7. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), the Machine Model (MM) (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω), and the Charge Device Model (CDM), Robotic (C_{ZAP} = 4.0 pF).
8. Input / Output pins are: IN[0:3], $\overline{RST}$, FSI, CSNS, SI, SCLK, $\overline{CS}$, SO, $\overline{FS}$
9. Device mounted on a 2s2p test board per JEDEC JESD51-2. 15 °C/W of $R_{\theta JA}$ can be reached in a real application case (4 layers board).
10. Pin soldering temperature limit is for 40 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
11. NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to www.nxp.com, search by part number (remove prefixes/suffixes) and enter the core ID to view all orderable parts, and review parametrics.

5.2 Static electrical characteristics

Table 5. Static electrical characteristics

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUTS					
Battery supply voltage range • Fully operational • Extended mode[12]	V_{PWR}	 6.0 4.0	 – –	 20 28	V
Battery clamp voltage[13]	$V_{PWR(CLAMP)}$	41	47	53	V
V_{PWR} operating supply current • Outputs commanded ON, HS[0:3] open, IN[0:3] > V_{IH}	$I_{PWR(ON)}$	–	6.5	20	mA
V_{PWR} supply current • Outputs commanded OFF, OFF openload detection disabled, HS[0:3] shorted to the ground with V_{DD}= 5.5 V WAKE > V_{IH} or $\overline{RST}$ > V_{IH} and IN[0:3] < V_{IL}	$I_{PWR(SBY)}$	–	6.0	8.0	mA
Sleep state supply current V_{PWR} = 12 V, $\overline{RST}$ = WAKE = IN[0:3] < V_{IL}, HS[0:3] shorted to the ground • T_A = 25 °C • T_A = 85 °C	$I_{PWR(SLEEP)}$	 – –	 1.0 –	 5.0 30	µA
V_{DD} supply voltage	$V_{DD(ON)}$	3.0	–	5.5	V
V_{DD} supply current at V_{DD} = 5.5 V • No SPI communication • 8.0 MHz SPI communication[14]	$I_{DD(ON)}$	– –	1.6 5.0	2.2 –	mA
V_{DD} sleep state current at V_{DD} = 5.5 V	$I_{DD(SLEEP)}$	–	–	5.0	µA
Overvoltage shutdown threshold	$V_{PWR(OV)}$	28	32	36	V
Overvoltage shutdown hysteresis	$V_{PWR(OVHYS)}$	0.2	0.8	1.5	V
Undervoltage shutdown threshold[15]	$V_{PWR(UV)}$	3.3	3.9	4.3	V
V_{PWR} and V_{DD} power on reset threshold	$V_{SUPPLY(POR)}$	0.5	–	0.9	$V_{PWR(UV)}$
V_{DD} supply failure threshold (for V_{PWR} > $V_{PWR(UV)}$)	$V_{DD(FAIL)}$	2.2	2.5	2.8	V
Recovery undervoltage threshold	$V_{PWR(UV)\_UP}$	3.4	4.1	4.5	V
OUTPUTS HS0 TO HS3					
Output Drain-to-Source ON resistance (I_{HS} = 2.0 A, T_A = 25 °C) • V_{PWR} = 4.0 V • V_{PWR} = 6.0 V • V_{PWR} = 10 V • V_{PWR} = 13 V	$R_{DS(ON)\_25}$	 – – – –	 – – – –	 100 55 35 35	mΩ

Notes

12. In extended mode, the functionality is guaranteed but not the electrical parameters. From 4.0 to 6.0 V voltage range, the device is only protected with the thermal shutdown detection.
13. Measured with the outputs open.
14. Typical value guaranteed per design.
15. Output will automatically recover with time limited autoretry to instructed state when V_{PWR} voltage is restored to normal as long as the V_{PWR} degradation level did not go below the under-voltage power-ON reset threshold. This applies to all internal device logic that is supplied by V_{PWR} and assumes that the external V_{DD} supply is within specification.

Table 5. Static electrical characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUTS HS0 TO HS3 (continued)					
Output Drain-to-Source ON resistance (I_{HS} = 2.0 A, T_A = 150 °C) • V_{PWR} = 4.5 V • V_{PWR} = 6.0 V • V_{PWR} = 10 V • V_{PWR} = 13 V	$R_{DS(ON)\_150}$	 – – – –	 – – – –	 170 94 66 66	mΩ
Output Source-to-Drain ON resistance (I_{HS} = -2.0 A, V_{PWR} = -18 V)(16) • T_A = 25 °C • T_A = 150 °C	$R_{SD(ON)}$	 – –	 – –	 52.5 70	mΩ
Maximum severe short-circuit impedance detection(17)	R_{SHORT}	70	160	200	mΩ
Output overcurrent detection levels (6.0 V ≤ $V_{HS[0:3]}$ ≤ 20 V)	OCHI1_0 OCHI2_0 OC1_0 OC2_0 OC3_0 OC4_0 OCLO4_0 OCLO3_0 OCLO2_0 OCLO1_0	39.5 25.2 22 18.9 15.7 12.6 9.4 6.3 5.0 3.2	47 30 26.2 22.5 18.7 15 11.2 7.5 6.0 4.0	54.5 34.8 30.4 26.1 21.7 17.4 13.0 8.7 7.0 4.8	A
C_{SR0} current recopy accuracy with one calibration point (6.0 V ≤ $V_{HS[0:3]}$ ≤ 20 V)(19) • Output current 2.0 A	$C_{SR0\_0\_ACC(CAL)}$	 -5.0	 –	 5.0	%
Current sense ratio (6.0 V ≤ $_{HS[0:3]}$ ≤ 20 V, CSNS ≤ 5.0 V)(18) • CSNS_ratio bit = 0 • CSNS_ratio bit = 1	C_{SR0_0} C_{SR1_0}	– –	1/4300 1/25800	– –	–
Current sense ratio (C_{SR0}) accuracy (6.0 V ≤ $V_{HS[0:3]}$ ≤ 20 V) • Output current 6.75 A 2.5 A 1.5 A 0.75 A	$C_{SR0\_0\_ACC}$	 -12 -13 -16 -20	 – – – –	 12 13 16 20	%

Notes

16. Source-Drain ON resistance (Reverse Drain-to-Source ON resistance) with negative polarity V_{PWR}.
17. Short-circuit impedance calculated from HS[0:3] to GND pins. Value guaranteed per design.
18. Current sense ratio = I_{CSNS} / $I_{HS[0:3]}$.
19. Based on statistical analysis, it is not production tested.

Table 5. Static electrical characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUTS HS0 TO HS3 (continued)					
C_{SR0} current recopy temperature drift (6.0 V ≤ $V_{HS[0:3]}$ ≤ 20 V)[20] • Output Current 2.0 A	$\Delta(C_{SR0\_0})/\Delta(T)$			0.04	%/°C
Current sense ratio (C_{SR1}) accuracy (6.0 V ≤ $V_{HS[0:3]}$ ≤ 20 V) • Output current 6.25 A 39.5 A	$C_{SR1\_0\_ACC}$	 -17 -12	 – –	 +17 +12	%
Current sense clamp voltage • CSNS Open; $I_{HS[0:3]}$ = 2.0 A with C_{SR0} ratio	$V_{CL(CSNS)}$	V_{DD}+0.25	–	V_{DD}+1.0	V
OFF openload detection source current[21]	$I_{OLD(OFF)}$	30	–	100	µA
OFF openload fault detection voltage threshold	$V_{OLD(THRES)}$	2.0	3.0	4.0	V
ON openload fault detection current threshold	$I_{OLD(ON)}$	100	300	600	mA
ON openload fault detection current threshold with LED $V_{HS[0:3]}$ = V_{PWR} - 0.75 V	$I_{OLD(ON\_LED)}$	2.5	5.0	10	mA
Output short to V_{PWR} detection voltage threshold Output programmed OFF	$V_{OSD(THRES)}$	V_{PWR}-1.2	V_{PWR}-0.8	V_{PWR}-0.4	V
Output negative clamp voltage • 0.5 A ≤ $I_{HS[0:3]}$ ≤ 5.0 A, output programmed OFF	V_{CL}	-22	–	-16	V
Output overtemperature shutdown for 4.5 V < VPWR < 28 V	T_{SD}	155	175	195	°C

Notes

20. Based on statistical data: delta(C_{SR0})/delta(T)={(measured I_{CSNS} at T_1 - measured I_{CSNS} at T_2) / measured I_{CSNS} at room} / {T_1-T_2}. No production tested.
21. Output OFF openload detection current is the current required to flow through the load for the purpose of detecting the existence of an openload condition when the specific output is commanded OFF. Pull-up current is measured for V_{HS}=$V_{OLD(THRES)}$

Table 5. Static electrical characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CONTROL INTERFACE					
Input logic high voltage[22]	V_{IH}	2.0	–	V_{DD}+0.3	V
Input logic low voltage[22]	V_{IL}	-0.3	–	0.8	V
Input logic pull-down current (SCLK, SI)[25]	I_{DWN}	5.0	–	20	µA
Input logic pull-up current ($\overline{CS}$)[26]	I_{UP}	5.0	–	20	µA
SO, $\overline{FS}$ Tri-state capacitance[23]	C_{SO}	–	–	20	pF
Input logic pull-down resistor ($\overline{RST}$, WAKE and IN[0:3])	R_{DWN}	125	250	500	kΩ
Input capacitance[23]	C_{IN}	–	4.0	12	pF
Wake input clamp voltage[24], $I_{CL(WAKE)}$ < 2.5 mA • 35XS3400CHFK • 35XS3400DHFK	$V_{CL(WAKE)}$	 18 20	 25 27	 32 35	V
Wake input forward voltage • $I_{CL(WAKE)}$ = -2.5 mA	$V_{F(WAKE)}$	-2.0	–	-0.3	V
SO high state output voltage • I_{OH} = 1.0 mA	V_{SOH}	V_{DD}-0.4	–	–	V
SO and $\overline{FS}$ low-state output voltage • I_{OL} = -1.0 mA	V_{SOL}	–	–	0.4	V
SO, CSNS and $\overline{FS}$ tri-state leakage current • $\overline{CS}$ = V_{IH} and 0 V ≤ V_{SO} ≤ V_{DD}, or $\overline{FS}$ = 5.5 V, or CSNS=0.0 V	$I_{SO(LEAK)}$	-2.0	0	2.0	µA
FSI external pull-down resistance[27] • Watchdog disabled • Watchdog enabled	RFS	 10	0 Infinite	1.0 –	kΩ

Notes

22. Upper and lower logic threshold voltage range applies to SI, $\overline{CS}$, SCLK, $\overline{RST}$, IN[0:3] and WAKE input signals. The WAKE and $\overline{RST}$ signals may be supplied by a derived voltage referenced to V_{PWR}.
23. Input capacitance of SI, $\overline{CS}$, SCLK, $\overline{RST}$, IN[0:3] and WAKE. This parameter is guaranteed by process monitoring but is not production tested.
24. The current must be limited by a series resistance when using voltages > 7.0 V.
25. Pull-down current is with V_{SI} ≥ 1.0 V and V_{SCLK} ≥ 1.0 V.
26. Pull-up current is with $V_{\overline{CS}}$ ≤ 2.0 V. $\overline{CS}$ has an active internal pull-up to V_{DD}.
27. In Fail-safe HS[0:3] depends respectively on ON[0:3]. FSI has an active internal pull-up to V_{REG} ~ 3.0 V.

5.3 Dynamic electrical characteristics

Table 6. Dynamic electrical characteristics

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT TIMING HS0 TO HS3					
Output rising medium slew rate (medium speed slew rate / SR[1:0]=00)[28] • V_{PWR} = 14 V	SR_{R_00}	0.2	0.4	0.8	V/µs
Output rising slow slew rate (low speed slew rate / SR[1:0]=01)[28] • V_{PWR} = 14 V	SR_{R_01}	0.1	0.2	0.4	V/µs
Output falling fast slew rate (high speed slew rate / SR[1:0]=10)[28] • V_{PWR} = 14 V	SR_{R_10}	0.4	0.8	1.6	V/µs
Output falling medium slew rate (medium speed slew rate / SR[1:0]=00)[28] • V_{PWR} = 14 V	SR_{F_00}	0.2	0.4	0.8	V/µs
Output falling slow slew rate (low speed slew rate / SR[1:0]=01)[28] • V_{PWR} = 14 V	SR_{F_01}	0.1	0.2	0.4	V/µs
Output rising fast slew rate (high speed slew rate / SR[1:0]=10)[28] • V_{PWR} = 14 V	SR_{F_10}	0.4	0.8	1.6	V/µs
Output turn-on delay time[29] • V_{PWR} = 14 V for medium speed slew rate (SR[1:0]=00)	$t_{DLY(ON)}$	35	60	85	µs
Output turn-off delay time[30] • V_{PWR} = 14 V for medium speed slew rate (SR[1:0]=00)	$t_{DLY(OFF)}$	35	60	85	µs
Driver output matching slew rate (SR_R /SR_F) V_{PWR} = 14 V @ 25 °C and for medium speed slew rate (SR[1:0]=00)	ΔSR	0.8	1.0	1.2	
Driver output matching time ($t_{DLY(ON)}$ - $t_{DLY(OFF)}$) V_{PWR} = 14 V, f_{PWM} = 240 Hz, PWM duty-cycle = 50%, @ 25 °C for medium speed slew rate (SR[1:0]=00)	Δt_{RF}	-25	0	25	µs

Notes

28. Rise and fall slew rates measured across a 5.0 Ω resistive load at high-side output = 30 % to 70 % (see Figure 4, page 17).
29. Turn-on delay time measured from rising edge of any signal (IN[0:3] and $\overline{CS}$) that would turn the output ON to $V_{HS[0:3]}$ = V_{PWR} / 2 with R_L = 5.0 Ω resistive load.
30. Turn-off delay time measured from falling edge of any signal (IN[0:3] and $\overline{CS}$) that would turn the output OFF to $V_{HS[0:3]}$ =V_{PWR} / 2 with R_L = 5.0 Ω resistive load.

Table 6. Dynamic electrical characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT TIMING HS0 TO HS3 (continued)					
Fault detection blanking time[31] • 35XS3400CHFK • 35XS3400DHFK	t_{FAULT}	- -	5.0 5.0	20 10	µs
Output shutdown delay time[32] • 35XS3400CHFK • 35XS3400DHFK	t_{DETECT}	- -	7.0 7.0	30 20	µs
$\overline{CS}$ to CSNS valid time[33]	t_{CNSVAL}	–	70	100	µs
Watchdog timeout[34]	t_{WDTO}	217	310	400	ms
ON openload fault cyclic detection period with LED • Internal clock (PWM_en bit = 1 & CLOCK_Set = 1) • External clock (PWM_en bit = 1 & CLOCK_Set = 0)	T_{OLLED}	6.4 -	8.3 PWM period	12 -	ms

Notes

31. Time necessary to report the fault to $\overline{FS}$ pin.
32. Time necessary to switch-off the output in case of OT or OC or SC or UV fault detection (from negative edge of $\overline{FS}$ pin to HS voltage = 50 % of V_{PWR}
33. Time necessary for the CSNS to be with ±5 % of the targeted value.
34. For FSI open, the watchdog timeout delay measured from the rising edge of RST, to HS[0,2] output state depend on the corresponding input command.

Table 6. Dynamic electrical characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Output overcurrent time step					ms
OC[1:0]=00 (slow by default)	t_{OC1_00}	3.4	5.0	6.6	
	t_{OC2_00}	1.0	1.72	2.0	
	t_{OC3_00}	1.4	2.0	2.6	
	t_{OC4_00}	2.0	3.0	4.0	
	t_{OC5_00}	3.4	5.0	6.74	
	t_{OC6_00}	8.4	12.2	16	
	t_{OC7_00}	31.2	44.6	48	
OC[1:0]=01 (fast)	t_{OC1_01}	1.72	2.48	3.22	
	t_{OC2_01}	0.56	0.8	1.04	
	t_{OC3_01}	0.72	1.04	1.36	
	t_{OC4_01}	1.02	1.58	1.92	
	t_{OC5_01}	1.56	2.24	2.92	
	t_{OC6_01}	4.28	6.12	7.96	
	t_{OC7_01}	15.4	22.2	29	
OC[1:0]=10 (medium)	t_{OC1_10}	6.8	9.8	12.8	
	t_{OC2_10}	2.2	3.2	4.2	
	t_{OC3_10}	2.8	4.2	5.6	
	t_{OC4_10}	4.0	5.8	7.6	
	t_{OC5_10}	6.8	9.8	12.8	
	t_{OC6_10}	17	24.4	31.8	
	t_{OC7_10}	6.24	89.2	116	
OC[1:0]=11 (very slow)	t_{OC1_11}	13.7	19.6	25.5	
	t_{OC2_11}	4.5	6.4	8.3	
	t_{OC3_11}	5.9	8.4	10.9	
	t_{OC4_11}	8.1	11.6	15.1	
	t_{OC5_11}	13.7	19.6	25.5	
	t_{OC6_11}	34.2	48.8	63.4	
	t_{OC7_11}	124.9	178.4	231.9	

Table 6. Dynamic electrical characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Bulb cooling time step					ms
CB[1:0]=00 or 11 (medium)	t_{BC1_00}	582	834	1084	
	t_{BC2_00}	312	448	584	
	t_{BC3_00}	356	510	664	
	t_{BC4_00}	416	596	776	
	t_{BC5_00}	502	718	934	
	t_{BC6_00}	628	898	1168	
CB[1:0]=01 (fast)	t_{BC1_01}	296	418	544	
	t_{BC2_01}	156	224	292	
	t_{BC3_01}	176	254	332	
	t_{BC4_01}	202	290	378	
	t_{BC5_01}	256	360	468	
	t_{BC6_01}	452	648	884	
CB[1:0]=10 (slow)	t_{BC1_10}	1166	1668	2170	
	t_{BC2_10}	624	894	1164	
	t_{BC3_10}	714	1022	1310	
	t_{BC4_10}	834	1192	1552	
	t_{BC5_10}	1002	1434	1866	
	t_{BC6_10}	1256	1796	2340	
PWM MODULE TIMING					
Input PWM clock range on IN0	f_{IN0}	7.68	–	30.72	kHz
Input PWM clock low frequency detection range on IN0[35]	$f_{IN0(LOW)}$	1.0	2.0	4.0	kHz
Input PWM clock high frequency detection range on IN0[35]	$f_{IN0(HIGH)}$	100	200	400	kHz
Output PWM frequency range	f_{PWM}	–	–	1.0	kHz
Output PWM frequency accuracy using calibrated oscillator	$A_{FPWM(CAL)}$	-10	–	+10	%
Default output PWM frequency using internal oscillator	$f_{PWM(0)}$	84	120	156	Hz
$\overline{CS}$ calibration low minimum time detection range	$t_{CSB(MIN)}$	14	20	26	µs
$\overline{CS}$ calibration low maximum time detection range	$t_{CSB(MAX)}$	140	200	260	µs
Output PWM duty-cycle range for f_{PWM} = 400 Hz[36]	R_{PWM_400}	10	–	98	%
Output PWM duty-cycle range for f_{PWM} = 200 Hz[36]	R_{PWM_200}	5.0	–	98	%
Output PWM duty-cycle range for f_{PWM} = 1.0 kHz for high speed slew rate[36]	R_{PWM_1k}	6.0	–	94	%
INPUT TIMING					
Direct input toggle timeout	t_{IN}	175	250	325	ms
AUTORETRY TIMING					
Autoretry period	t_{AUTO}	105	150	195	ms

Notes

35. Clock fail detector available for PWM_en bit is set to logic [1] and CLOCK_sel is set to logic [0].
36. The PWM ratio is measured at V_{HS} = 50 % of V_{PWR} and for the default SR value. It is possible to put the device fully-on (PWM duty-cycle 100 %) and fully-off (duty-cycle 0 %). For values outside this range, a calibration is needed between the PWM duty-cycle programming and the PWM on the output with R_L = 5.0 Ω resistive load.

Table 6. Dynamic electrical characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
TEMPERATURE ON THE GND FLAG					
Thermal prewarning detection[37]	T_{OTWAR}	110	125	140	°C
Analog temperature feedback at T_A = 25 °C with R_{CSNS} = 2.5 kΩ	T_{FEED}	1.15	1.20	1.25	V
Analog temperature feedback derating with R_{CSNS} = 2.5 kΩ[38]	DT_{FEED}	-3.5	-3.7	-3.9	mV/°C
SPI INTERFACE CHARACTERISTICS[37]					
Maximum frequency of SPI operation	f_{SPI}	–	–	8.0	MHz
Required low state duration for $\overline{RST}$[39]	$t_{W\overline{RST}}$	10	–	–	µs
Rising edge of $\overline{CS}$ to falling edge of $\overline{CS}$ (required setup time)[40]	$t_{\overline{CS}}$	–	–	1.0	µs
Rising edge of $\overline{RST}$ to falling edge of $\overline{CS}$ (required setup time)[40]	t_{ENBL}	–	–	5.0	µs
Falling edge of $\overline{CS}$ to rising edge of SCLK (required setup time)[40]	t_{LEAD}	–	–	500	ns
Required high state duration of SCLK (required setup time)[40]	t_{WSCLKh}	–	–	50	ns
Required low state duration of SCLK (required setup time)[40]	t_{WSCLKl}	–	–	50	ns
Falling edge of SCLK to rising edge of $\overline{CS}$ (required setup time)[40]	t_{LAG}	–	–	60	ns
SI to falling edge of SCLK (required setup time)[41]	$t_{SI(SU)}$	–	–	37	ns
Falling edge of SCLK to SI (required setup time)[41]	$t_{SI(HOLD)}$	–	–	49	ns
SO rise time • C_L = 80 pF	t_{RSO}	–	–	13	ns
SO fall time • C_L = 80 pF	t_{FSO}	–	–	13	ns
SI, $\overline{CS}$, SCLK, incoming signal rise time[41]	t_{RSI}	–	–	13	ns
SI, $\overline{CS}$, SCLK, incoming signal fall time[41]	t_{FSI}	–	–	13	ns
Time from rising edge of SCLK to SO low logic level[42]	$t_{SO(EN)}$	–	–	60	ns
Time from rising edge of SCLK to SO high logic level[43]	$t_{SO(DIS)}$	–	–	60	ns

Notes

37. Parameters guaranteed by design.
38. Value guaranteed per statistical analysis
39. $\overline{RST}$ low duration measured with outputs enabled and going to OFF or disabled condition.
40. Maximum setup time required for the 35XS3400 is the minimum guaranteed time needed from the microcontroller.
41. Rise and fall time of incoming SI, $\overline{CS}$, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
42. Time required for output status data to be available for use at SO. 1.0 kΩ on pull-up on $\overline{CS}$.
43. Time required for output status data to be terminated at SO. 1.0 kΩ on pull-up on $\overline{CS}$.

5.4 TIming diagrams

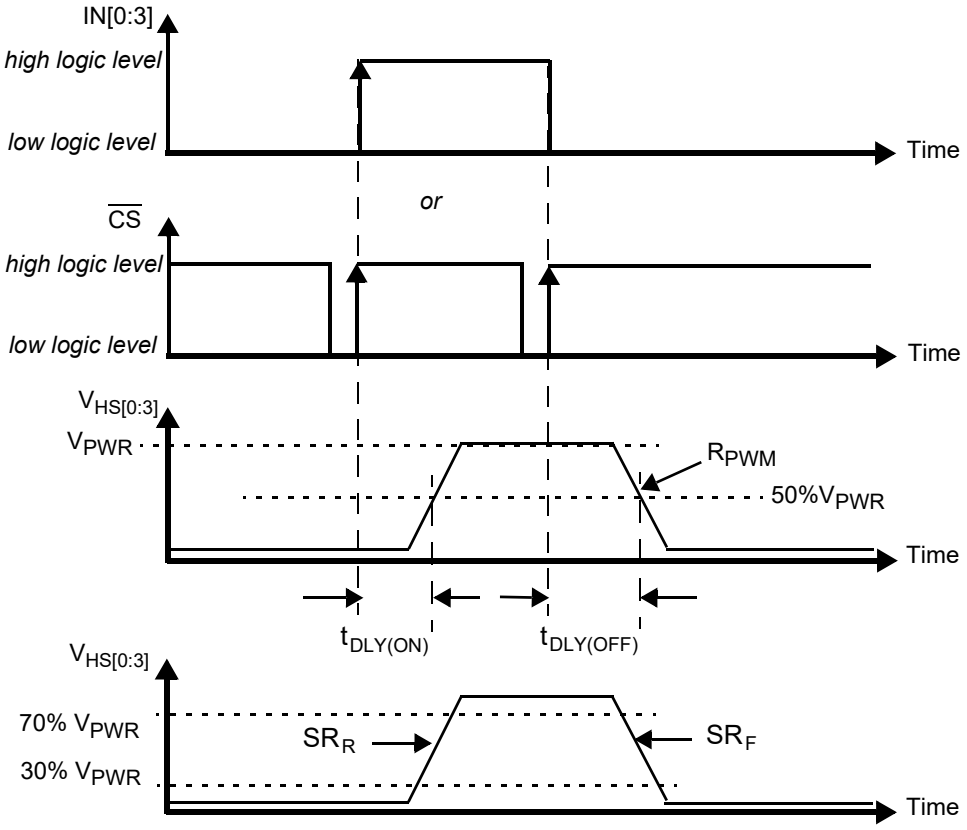


Figure 4. Output slew rate and time delays

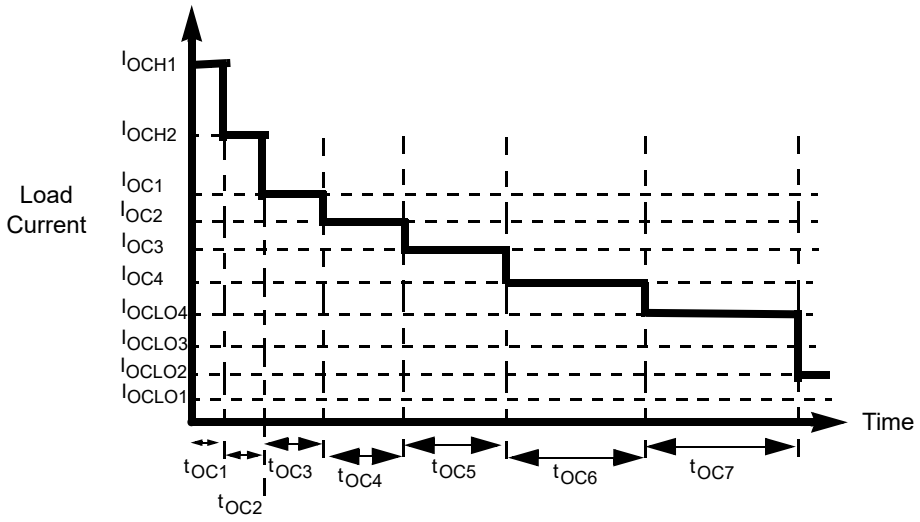


Figure 5. Overcurrent shutdown protection

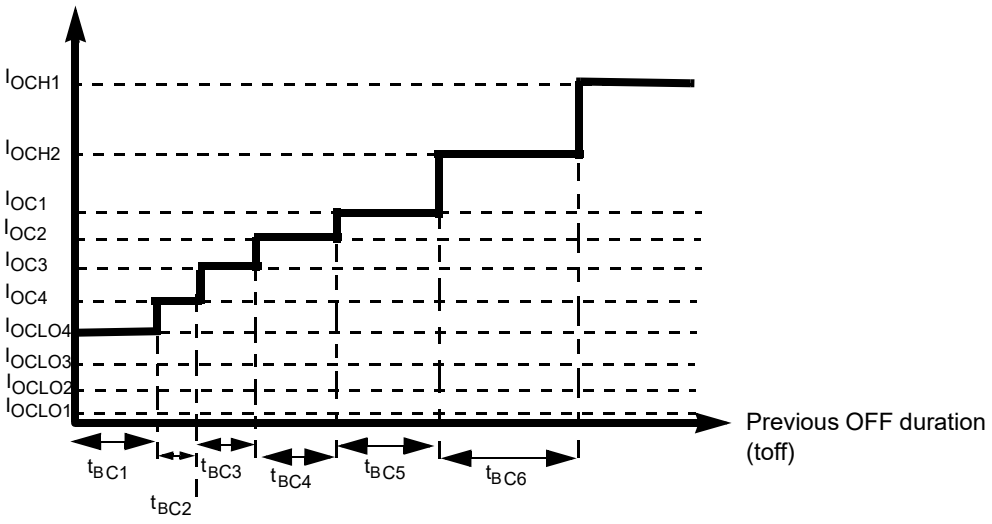


Figure 6. Bulb cooling management

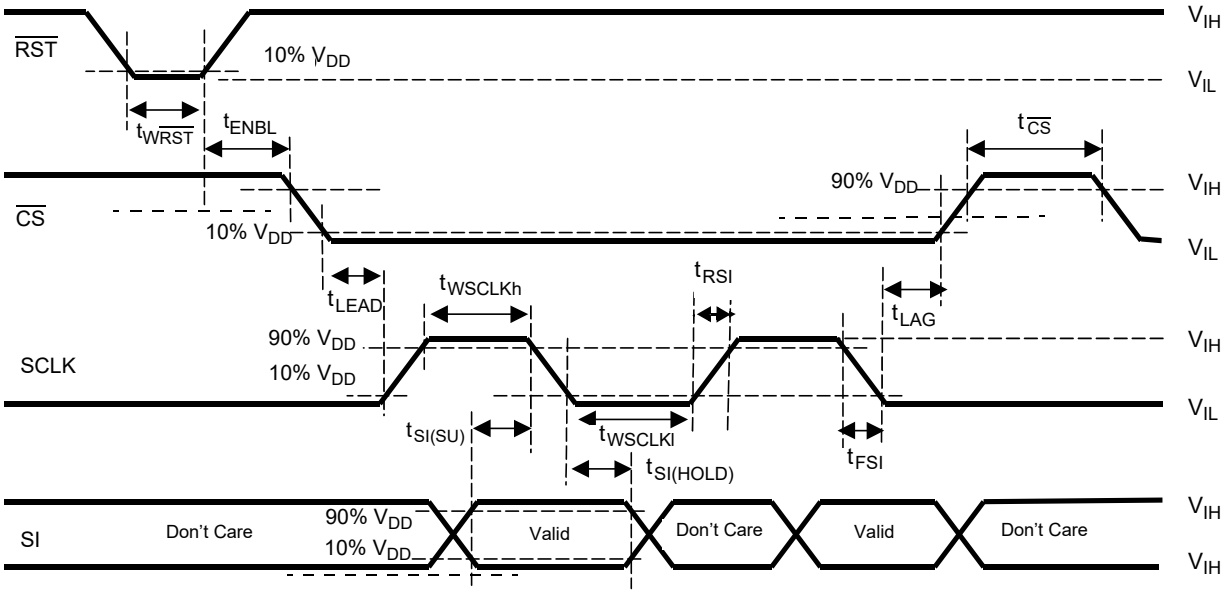


Figure 7. Input timing switching characteristics

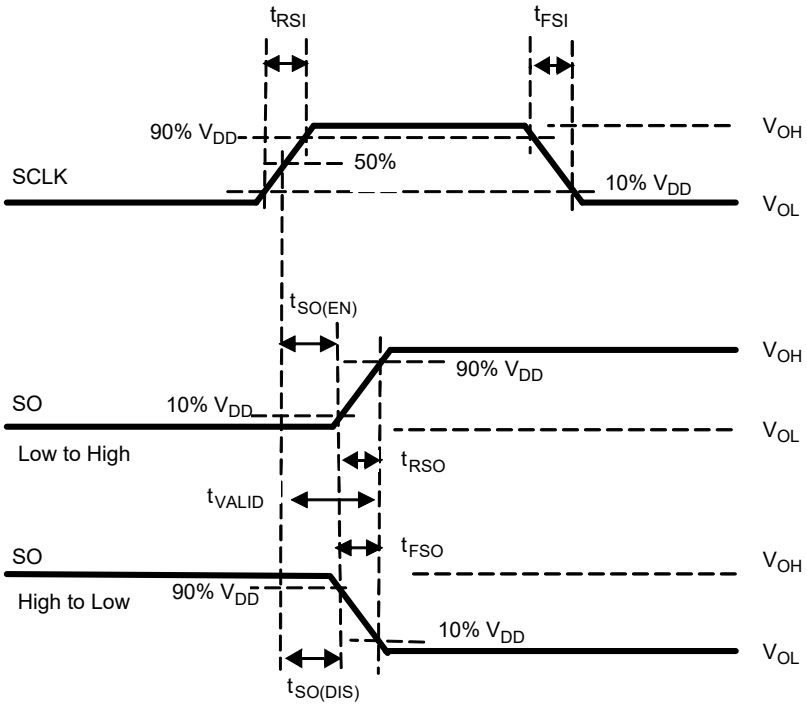


Figure 8. SCLK waveform and valid SO data delay time

6 Functional description

6.1 Introduction

The 35XS3400 is one in a family of devices designed for low-voltage automotive lighting applications. Its four low $R_{DS(on)}$ MOSFETs (quad 35 mΩ) can control four separate 28 W bulbs.

Programming, control and diagnostics are accomplished using a 16-bit SPI interface. Its output with selectable slew-rate improves electromagnetic compatibility (EMC) behavior. Additionally, each output has its own parallel input or SPI control for pulse-width modulation (PWM) control if desired. The 35XS3400 allows the user to program via the SPI the fault current trip levels and duration of acceptable lamp inrush. The device has Fail-safe mode to provide functionality of the outputs in case of MCU damage.

6.2 Functional pin description

6.2.1 Output current monitoring (CSNS)

The Current Sense pin provides a current proportional to the designated HS0:HS3 output or a voltage proportional to the temperature on the GND flag. That current is fed into a ground-referenced resistor (4.7 kΩ typical) and its voltage is monitored by an MCU's A/D. The output type is selected via the SPI. This pin can be tri-stated through the SPI.

6.2.2 Direct inputs (IN0, IN1, IN2, IN3)

Each IN input wakes the device. The IN0:IN3 high-side input pins are also used to directly control HS0:HS3 high-side output pins. If the outputs are controlled by the PWM module, the external PWM clock is applied to IN0 pin. These pins are to be driven with CMOS levels, and they have a passive internal pull-down, R_{DWN}.

6.2.3 Fault status ($\overline{FS}$)

This pin is an open drain configured output requiring an external pull-up resistor to V_{DD} for fault reporting. If a device fault condition is detected, this pin is active LOW. Specific device diagnostics and faults are reported via the SPI SO pin.

6.2.4 Wake

The wake input wakes the device. An internal clamp protects this pin from high damaging voltages with a series resistor (10 kΩ typ). This input has a passive internal pull-down, R_{DWN}.

6.2.5 Reset ($\overline{RST}$)

The reset input wakes the device. This is used to initialize the device configuration and fault registers, as well as place the device in a low-current Sleep mode. The pin also starts the watchdog timer when transitioning from logic [0] to logic [1]. This pin has a passive internal pull-down, R_{DWN}.

6.2.6 Chip select ($\overline{CS}$)

The $\overline{CS}$ pin enables communication with the master microcontroller (MCU). When this pin is in a logic [0] state, the device is capable of transferring information to, and receiving information from, the MCU. The 35XS3400 latches in data from the input shift registers to the addressed registers on the rising edge of $\overline{CS}$. The device transfers status information from the power output to the Shift register on the falling edge of $\overline{CS}$. The SO output driver is enabled when $\overline{CS}$ is logic [0]. $\overline{CS}$ should transition from a logic [1] to a logic [0] state only when SCLK is a logic [0]. $\overline{CS}$ has an active internal pull-up from V_{DD}, I_{UP}.

6.2.7 Serial clock (SCLK)

The SCLK pin clocks the internal shift registers of the 35XS3400 device. The serial input (SI) pin accepts data into the input shift register on the falling edge of the SCLK signal while the serial output (SO) pin shifts data information out of the SO line driver on the rising edge of the SCLK signal. It is important the SCLK pin be in a logic low state whenever $\overline{CS}$ makes any transition. For this reason, it is recommended the SCLK pin be in a logic [0] whenever the device is not accessed ($\overline{CS}$ logic [1] state). SCLK has an active internal pull-down. When $\overline{CS}$ is logic [1], signals at the SCLK and SI pins are ignored and SO is tri-stated (high-impedance) (see Figure 10, page 23). SCLK input has an active internal pull-down, I_{DWN}.

6.2.8 Serial input (SI)

This is a serial interface (SI) command data input pin. Each SI bit is read on the falling edge of SCLK. A 16-bit stream of serial data is required on the SI pin, starting with D15 (MSB) to D0 (LSB). The internal registers of the 35XS3400 are configured and controlled using a 5-bit addressing scheme described in Table 11, page 33. Register addressing and configuration are described in Table 12, page 33. SI input has an active internal pull-down, I_{DWN}.

6.2.9 Digital drain voltage (VDD)

This pin is an external voltage input pin used to supply power to the SPI circuit. In the event V_{DD} is lost (V_{DD} Failure), the device goes to Fail-safe mode.

6.2.10 Ground (GND)

These pins are the ground for the device.

6.2.11 Positive power supply (VPWR)

This pin connects to the positive power supply and is the source of operational power for the device. The VPWR contact is the backside surface mount tab of the package.

6.2.12 Serial output (SO)

The SO data pin is a tri-stateable output from the shift register. The SO pin remains in a high-impedance state until the $\overline{CS}$ pin is put into a logic [0] state. The SO data is capable of reporting the status of the output, the device configuration, the state of the key inputs, etc. The SO pin changes state on the rising edge of SCLK and reads out on the falling edge of SCLK. SO reporting descriptions are provided in Table 24, page 38.

6.2.13 High-side outputs (HS3, HS1, HS0, HS2)

Protected 35 mΩ high-side power outputs to the load.

6.2.14 Fail-safe input (FSI)

This pin incorporates an active internal pull-up current source from internal supply (V_{REG}). This enables the watchdog timeout feature.

When the FSI pin is opened, the watchdog circuit is enabled. After a watchdog timeout occurs, the output states depends on IN[0:3].

When the FSI pin is connected to GND, the watchdog circuit is disabled. The output states depends on IN[0:3] in case of V_{DD} failure condition, in case V_{DD} failure detection is activated (VDD_FAIL_en bit sets to logic [1]).

6.3 Functional internal block description

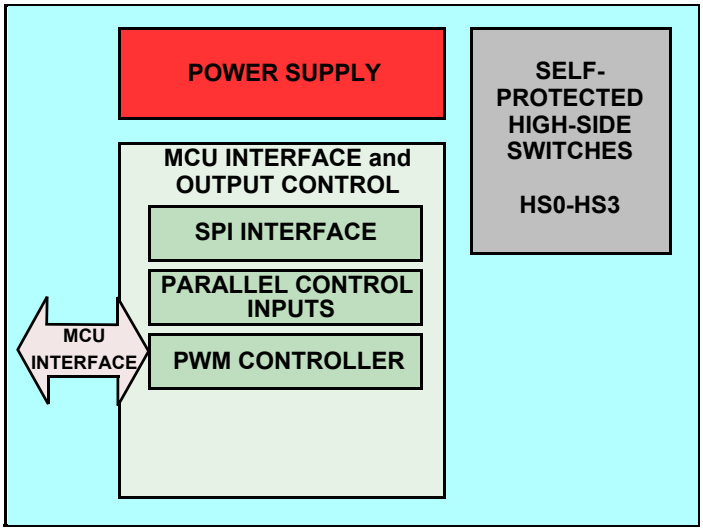


Figure 9. Functional block diagram

6.3.1 Power supply

The 35XS3400 is designed to operate from 4.0 to 28 V on the VPWR pin. Characteristics are provided from 6.0 to 20 V for the device. The VPWR pin supplies power to internal regulator, analog, and logic circuit blocks. The VDD supply is used for Serial Peripheral Interface (SPI) communication in order to configure and diagnose the device. This IC architecture provides a low quiescent current Sleep mode. Applying V_{PWR} and V_{DD} to the device will place the device in the Normal mode. The device will transit to Fail-safe mode in case of failures on the SPI or/and on the V_{DD} voltage.

6.3.2 High-side switches: HS0 – HS3

These pins are the high-side outputs controlling automotive lamps located for the rear of vehicle, such as 28 W bulbs and LED modules. 55 W/65 W lamps can be driven for two outputs shorted together. Those N-channel MOSFETs with 35 mΩ $R_{DS(on)}$ are self-protected and present extended diagnostics in order to detect bulb outage and short-circuit fault condition. The HS output is actively clamped during turn off of inductive loads and inductive battery line.

When driving DC motor or solenoid loads demanding multiple switching, an external recirculation device must be used to maintain the device in its safe operating area.

6.3.3 MCU interface and output control

In Normal mode, each bulb is controlled directly from the MCU through SPI. A pulse width modulation control module allows improvement of lamp lifetime with bulb power regulation (PWM frequency range from 100 to 400 Hz) and addressing the dimming application (day running light). An analog feedback output provides a current proportional to the load current or the temperature of the board. The SPI is used to configure and to read the diagnostic status (faults) of high-side outputs. The reported fault conditions are: OpenLoad, short-circuit to battery, short-circuit to ground (overcurrent and severe short-circuit), thermal shutdown, and under/overvoltage. Due to accurate and configurable overcurrent detection circuitry and wire-harness optimization, the vehicle is lighter.

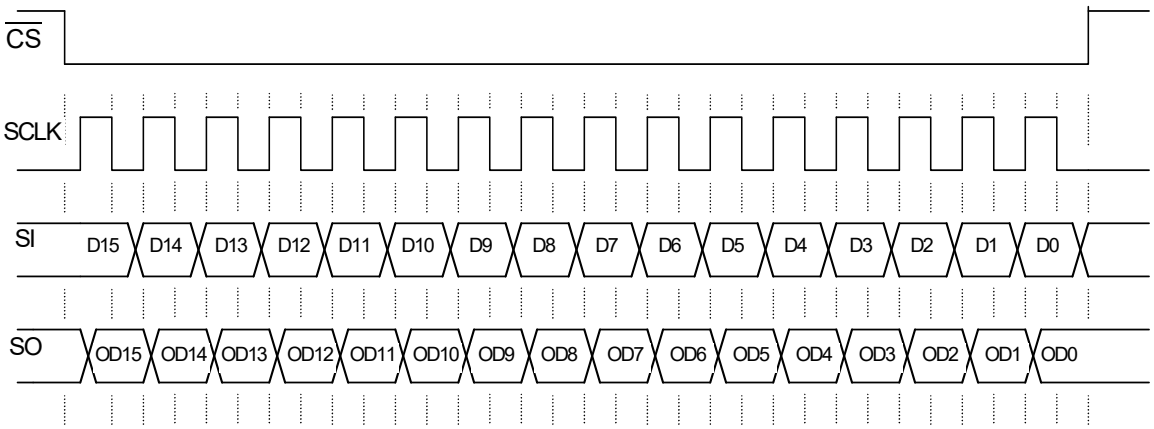
In Fail-safe mode, each lamp is controlled with dedicated parallel input pins. The device is configured in default mode.

7 Functional device operation

7.1 SPI protocol description

The SPI interface has a full duplex, three-wire synchronous data transfer with four I/O lines associated with it: Serial Input (SI), Serial Output (SO), Serial Clock (SCLK), and Chip Select ($\overline{CS}$).

The SI/SO pins of the 35XS3400 follow a first-in first-out (D15 to D0) protocol, with both input and output words transferring the most significant bit (MSB) first. All inputs are compatible with 5.0 V or 3.3 V CMOS logic levels.



Notes 1. $\overline{RST}$ is a logic [1] state during the above operation.
2. D15:D0 relate to the most recent ordered entry of data into the device.
3. OD15:OD0 relate to the first 16 bits of ordered fault and status data out of the device.

Figure 10. Single 16-bit word SPI communication

7.2 Operational modes

The 35XS3400 has four operating modes: Sleep, Normal, Fail-safe and Fault. Table 7 and Figure 12 summarize details contained in succeeding paragraphs.

The Figure 11 describes an internal signal called IN_ON[x] depending on IN[x] input.

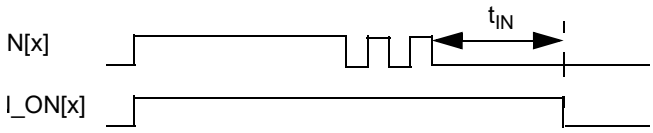


Figure 11. IN_ON[x] internal signal

The 35XS3400 transits to operating modes according to the following signals:

- wake-up = $\overline{RST}$ or WAKE or IN_ON[0] or IN_ON[1] or IN_ON[2] or IN_ON[3],
- fail = (V_{DD} Failure and VDD_FAIL_en) or (Watchdog time-out and FSI input not shorted to ground),
- fault = OC[0:3] or $\overline{OT[0:3]}$ or SC[0:3] or UV
  (UV) or (OV and $\overline{OV}$_dis).

Table 7. 35XS3400 operating modes

Mode	wake-up	fail	fault	Comments
Sleep	0	x	x	Device is in Sleep mode. All outputs are OFF.
Normal	1	0	0	Device is currently in Normal mode. Watchdog is active if enabled.
Fail-safe	1	1	0	Device is currently in Fail-safe mode due to watchdog timeout or V_{DD} Failure conditions. The output states depend on the corresponding input in case FSI is open.
Fault	1	X	1	Device is currently in Fault mode. The faulted output(s) is (are) OFF. The safe autoretry circuitry is active to turn-on again the output(s).

x = Don’t care.

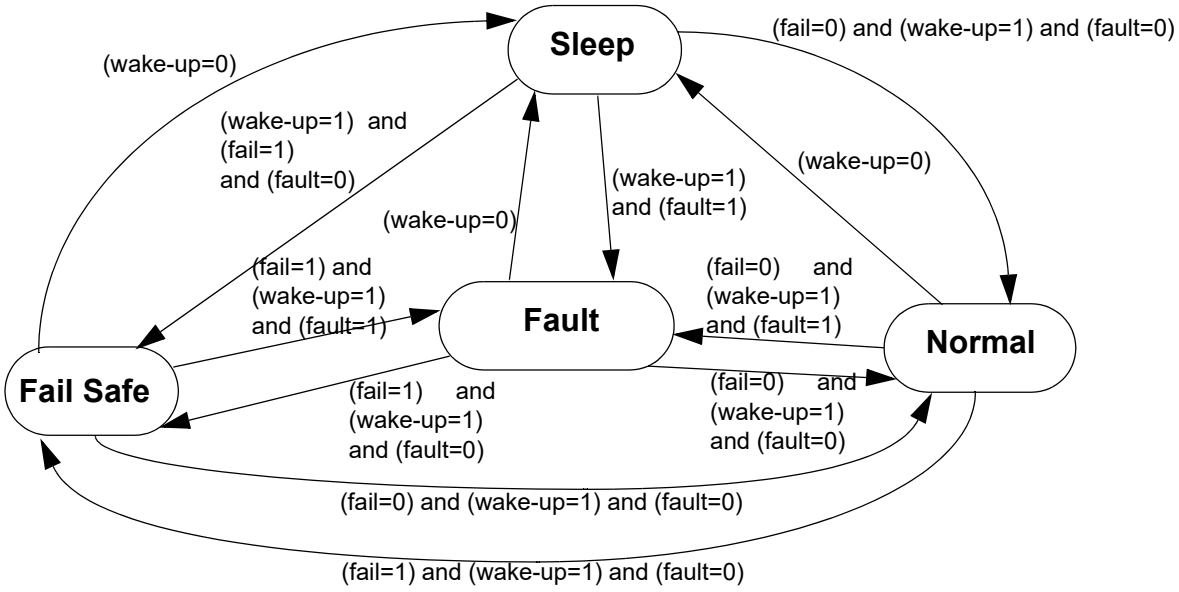


Figure 12. Operating modes

7.2.1 Sleep mode

The 35XS3400 is in Sleep mode when:

- V_{PWR} and V_{DD} are within the normal voltage range,
- wake-up = 0,
- fail = X,
- fault = X.

This is the Default mode of the device after first applying battery voltage (VPWR) prior to any I/O transitions. This is also the state of the device when the WAKE and $\overline{RST}$ and IN_ON[0:3] are logic [0]. In the Sleep mode, the output and all unused internal circuitry, such as the internal regulator, are off to minimize draw current. In addition, all SPI-configurable features of the device are as if set to logic [0].

7.2.2 Normal mode

The 35XS3400 is in Normal mode when:

- V_{PWR} and V_{DD} are within the normal voltage range,
- wake-up = 1,
- fail = 0,
- fault = 0.

In this mode, the NM bit is set to lfault_contrologic [1] and the outputs HS[0:3] are under control, as defined by hson signal:

hson[x] = (((IN[x] and $\overline{\text{DIR\_dis}}$[x]) or On bit[x]) and $\overline{\text{PWM\_en}}$) or (On bit [x] and Duty_cycle[x] and PWM_en).

In this mode and also in Fail-safe, the fault condition reset depends on fault_control signal, as defined below:

fault_control[x] = ((IN_ON[x] and $\overline{\text{DIR\_dis}}$[x]) and $\overline{\text{PWM\_en}}$) or (On bit [x]).

7.2.2.1 Programmable PWM module

The outputs HS[0:3] are controlled by the programmable PWM module if PWM_en and On bits are set to logic [1].

The clock frequency from IN0 input pin or from internal clock is the factor 2^7 (128) of the output PWM frequency (CLOCK_sel bit). The outputs HS[0:3] can be controlled in the range of 5% to 98% with a resolution of 7 bits of duty-cycle (Table 8). The state of other IN pin is ignored.

Table 8. Output PWM resolution

On bit	Duty-cycle	Output state
0	**X**	**OFF**
1	0000000	PWM (1/128 duty-cycle)
1	0000001	PWM (2/128 duty-cycle)
1	0000010	PWM (3/128 duty-cycle)
1	n	PWM ((n+1)/128 duty-cycle)
1	1111111	fully ON

The timing includes seven programmable PWM switching delay (number of PWM clock rising edges) to improve overall EMC behavior of the light module (Table 9).

Table 9. Output PWM switching delay

Delay bits	Output delay
000	no delay
001	16 PWM clock periods
010	32 PWM clock periods
011	48 PWM clock periods
100	64 PWM clock periods
101	80 PWM clock periods
110	96 PWM clock periods
111	112 PWM clock periods

The clock frequency from IN0 is permanently monitored in order to report a clock failure in case of the frequency is out a specified frequency range (from $f_{IN0(LOW)}$ to $f_{IN0(HIGH)}$). In case of clock failure, no PWM feature is provided, the On bit defines the outputs state and the CLOCK_fail bit reports [1].

7.2.2.2 Calibratable internal clock

The internal clock can vary as much as +/-30 percent corresponding to typical $f_{PWM(0)}$ output switching period.

Using the existing SPI inputs and the precision timing reference already available to the MCU, the 35XS3400 allows clock period setting within ±10 percent of accuracy. Calibrating the internal clock is initiated by defined word to CALR register. The calibration pulse is provided by the MCU. The pulse is sent on the $\overline{CS}$ pin after the SPI word is launched. At the moment, the $\overline{CS}$ pin transitions from logic [1] to [0] until from logic [0] to [1] determine the period of internal clock with a multiplicative factor of 128.

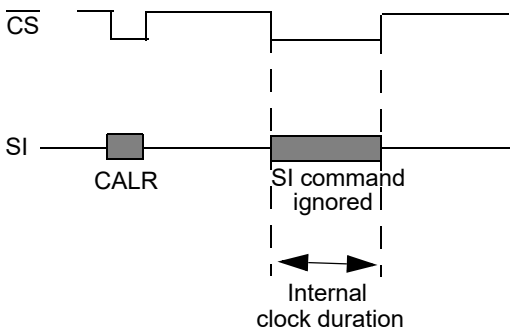


Figure 13. Internal clock calibration diagram

In case of negative $\overline{CS}$ pulse is outside a predefined time range (from $t_{CSB(MIN)}$ to $t_{CSB(MAX)}$), the calibration event will be ignored and the internal clock will be unaltered or reset to default value ($f_{PWM(0)}$) if this was not calibrated before.

The calibratable clock is used, instead of the clock from IN0 input, when CLOCK_sel is set to [1].

7.2.3 Fail-safe mode

The 35XS3400 is in Fail-safe mode when:

- V_{PWR} is within the normal voltage range,
- wake-up = 1,
- fail = 1,
- fault = 0.

7.2.3.1 Watchdog

If the FSI input is not grounded, the watchdog timeout detection is active when either the WAKE or IN_ON[0:3] or $\overline{RST}$ input pin transitions from logic [0] to logic [1]. The WAKE input is capable of being pulled up to VPWR with a series of limiting resistance limiting the internal clamp current according to the specification.

The watchdog timeout is a multiple of an internal oscillator. As long as the WD bit (D15) of an incoming SPI message is toggled within the minimum watchdog timeout period (WDTO), the device will operate normally.

7.2.3.2 Fail-safe conditions

If an internal watchdog time-out occurs before the WD bit for FSI open (Table 10) or in case of V_{DD} failure condition (V_{DD}< $V_{DD(FAIL)}$)) for VDD_FAIL_en bit is set to logic [1], the device will revert to a Fail-safe mode until the WD bit is written to logic [1] (see fail-safe to normal mode transition paragraph) and V_{DD} is within the normal voltage range.

Table 10. SPI watchdog activation

Typical RFSI (Ω)	Watchdog
0 (shorted to ground)	Disabled
(open)	Enabled

During the Fail-safe mode, the outputs will depend on the corresponding input. The SPI register content is reset to their default value (except POR bit) and fault protections are fully operational.

The Fail-safe mode can be detected by monitoring the NM bit is set to [0].

7.2.4 Normal and Fail-safe mode transitions

7.2.4.1 Transition Fail-safe to Normal mode

To leave the Fail-safe mode, V_{DD} must be in nominal voltage and the microcontroller has to send a SPI command with WDIN bit set to logic [1]; the other bits are not considered. The previous latched faults are reset by the transition into Normal mode (autoretry included).

Moreover, the device can be brought out of the Fail-safe mode due to watchdog timeout issue by forcing the FSI pin to logic [0].

7.2.4.2 Transition Normal to Fail-safe mode

To leave the Normal mode, a Fail-safe condition must occurred (fail=1). The previous latched faults are reset by the transition into Fail-safe mode (autoretry included).

7.2.5 Fault mode

The 35XS3400 is in Fault mode when:

- V_{PWR} and V_{DD} are within the normal voltage range,
- wake-up = 1,
- fail = X,
- fault=1.

This device indicates the faults below as they occur by driving the $\overline{FS}$ pin to logic [0] for $\overline{RST}$ input is pulled up:

- Overtemperature fault,
- Overcurrent fault,
- Severe short-circuit fault,
- Output(s) shorted to VPWR fault in OFF state,
- Openload fault in OFF state,
- Overvoltage fault (enabled by default),
- Undervoltage fault.

The $\overline{FS}$ pin will automatically return to logic [1] when the fault condition is removed, except for overcurrent, severe short-circuit, overtemperature and undervoltage which will be reset by a new turn-on command (each fault_control signal to be toggled).

Fault information is retained in the SPI fault register and is available (and reset) via the SO pin during the first valid SPI communication.

The openload fault in ON state is only reported through SPI register without effect on the corresponding output state (HS[x]) and the $\overline{FS}$ pin.

7.2.6 Start-up sequence

The 35XS3400 enters in Normal mode after start-up if following sequence is provided:

- VPWR and VDD power supplies must be above their under-voltage thresholds,
- generate wake-up event (wake-up=1) from 0 to 1 on RSTB. The device switches to Normal mode with SPI register content is reset (as defined in Table 12 and Table 24). All features of 35XS3400 will be available after 50µs typical and all SPI registers are set to default values (set to logic [0]). The UV fault is reported in the SPI status registers.

And, in case of the PWM module is used (PWM_en bit is set to logic [1]) with an external reference clock:

- apply PWM clock on IN0 input pin after maximum 200 µs (min. 50 µs).

If the correct start-up sequence is not provided, the PWM function is not guaranteed.

7.3 Protection and diagnostic features

7.3.1 Protections

7.3.1.1 Overtemperature fault

The 35XS3400 incorporates overtemperature detection and shutdown circuitry for each output structure.

Two cases need to be considered when the output temperature is higher than T_{SD}:

- If the output command is ON: the corresponding output is latched OFF. $\overline{FS}$ will be also latched to logic [0]. To delatch the fault and be able to turn ON again the outputs, the failure condition must disappear and the autoretry circuitry must be active or the corresponding output must be commanded OFF and then ON (toggling fault_control signal of corresponding output) or $V_{SUPPLY(POR)}$ condition if V_{DD} = 0.
- If the output command is OFF: $\overline{FS}$ will go to logic [0] until the corresponding output temperature will be below T_{SD}.

For both cases, the fault register OT[0:3] bit into the status register will be set to [1]. The fault bits will be cleared in the status register after a SPI read command.

7.3.1.2 Overcurrent fault

The 35XS3400 incorporates output shutdown in order to protect each output structure against resistive short-circuit condition. This protection is composed by eight predefined current levels (time dependent) to fit 28 W bulb profiles.

In the first turn-on, the lamp filament is cold and the current will be huge. fault_control signal transition from logic [0] to [1] or an autoretry define this event. In this case, the overcurrent protection will be fitted to inrush current, as shown in Figure 5. This overcurrent protection is programmable: OC[1:0] bits select overcurrent slope speed and OCHI1 current step can be removed in case the OCHI bit is set to [1].

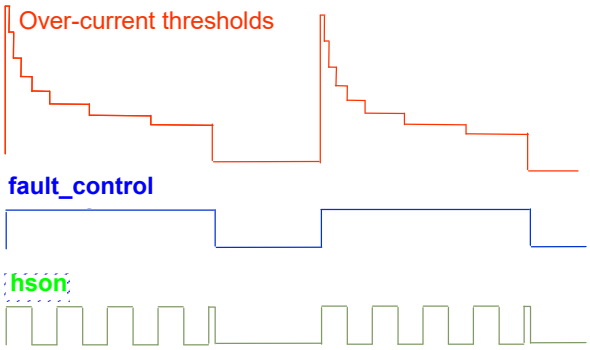


Figure 14. Overcurrent detection profile

In steady state, the wire harness will be protected by OCLO2 current level by default. Three other DC overcurrent levels are available: OCLO1 or OCLO3 or OCLO4 based on the state of the OCLO[1,0] bits.

If the load current level ever reaches the overcurrent detection level, the corresponding output will latch the output OFF and $\overline{FS}$ will be also latched to logic [0]. To delatch the fault and be able to turn ON again the corresponding output, the failure condition

must disappear and the autoretry circuitry must be active or the corresponding output must be commanded OFF and then ON (toggling fault_control signal of corresponding output) or $V_{SUPPLY(POR)}$ condition if V_{DD} = 0.

The SPI fault report (OC[0:3] bits) is removed after a read operation.

In Normal mode using the internal PWM module, the 35XS3400 also incorporates a cooling bulb filament management, if the OC_mode is set to logic [1]. In this case, the 1st step of multi-step overcurrent protection will depend to the previous OFF duration, as illustrated in Figure 6. The following figure illustrates the current level will be used in function to the duration of previous OFF state (toff). The slope of cooling bulb emulator is configurable with OCOFFCB[1:0] bits.

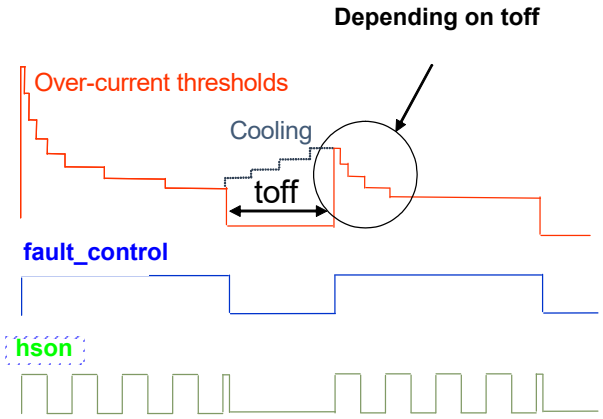


Figure 15. Bulb cooling principle

7.3.1.3 Severe short-circuit fault

The 35XS3400 provides output shutdown in order to protect each output in case of severe short-circuit during of the output switching.

If the short-circuit impedance is below R_{SHORT}, the device will latch the output OFF, $\overline{FS}$ will go to logic [0] and the fault register SC[0:3] bit will be set to [1]. To delatch the fault and be able to turn ON again the outputs, the failure condition must disappear and the corresponding output must be commanded OFF, and then ON (toggling fault_control signal of corresponding output) or $V_{SUPPLY(POR)}$ condition, if V_{DD} = 0.

The SPI fault report (SC[0:3] bits) is removed after a read operation.

7.3.1.4 Overvoltage fault (enabled by default)

By default, the overvoltage protection is enabled. The 35XS3400 shuts down all outputs and $\overline{FS}$ will go to logic [0] during an overvoltage fault condition on the VPWR pin ($V_{PWR} \geq V_{PWR(OV)}$). The outputs remain in the OFF state until the overvoltage condition is removed ($V_{PWR} \leq V_{PWR(OV)} - V_{PWR(OVHYS)}$). When experiencing this fault, the OVF fault bit is set to logic [1] and cleared after either a valid SPI read.

The overvoltage protection can be disabled through SPI (OV_dis bit is disabled set to logic [1]). The fault register reflects any overvoltage condition ($V_{PWR} \geq V_{PWR(OV)}$). This overvoltage diagnosis, as a warning, is removed after a read operation, if the fault condition disappears. The HS[0:3] outputs are not commanded in $R_{DS(ON)}$ above the OV threshold.

In Fail-safe mode, the overvoltage activation depends on the $\overline{RST}$ logic state; enable for $\overline{RST}$ = 1 and disable for $\overline{RST}$ = 0. The device is still protected with overtemperature protection in case the overvoltage feature is disabled.

7.3.1.5 Undervoltage fault

The output(s) will latch off at some battery voltage below $VPWR_{(UV)}$. As long as the V_{DD} level stays within the normal specified range, the internal logic states within the device will remain (configuration and reporting).

In the case where battery voltage drops below the undervoltage threshold ($V_{PWR} \leq V_{PWR(UV)}$), the outputs will turn off, $\overline{FS}$ will go to logic [0], and the fault register UV bit will be set to [1].

Two cases need to be considered when the battery level recovers ($V_{PWR} > V_{PWR(UV)\_UP}$):

- If the output command is OFF, $\overline{FS}$ will go to logic [1], but the UV bit will remain set to 1 until the next read operation (warning report).
- If the output command is ON, $\overline{FS}$ will remain at logic [0]. To delatch the fault and be able to turn ON again the outputs, the failure condition must disappear and the autoretry circuitry must be active or the corresponding output must be commanded OFF and then ON (toggling fault_control signal of corresponding output) or $V_{SUPPLY(POR)}$ condition if V_{DD} = 0.

In **extended mode**, the output is protected by overtemperature shutdown circuitry. All previous latched faults, occurred when VPWR was within the normal voltage range, are guaranteed if VDD is within the operational voltage range or until $V_{SUPPLY(POR)}$ if VDD = 0. Any new OT fault is detected (VDD failure included) and reported through SPI above $VPWR_{(UV)}$. The output state is not changed as long as the VPWR voltage does not drop any lower than 3.5 V typical.

All latched faults (overtemperature, over-current, severe short-circuit, over and undervoltage) are reset if:

- $V_{DD} \leq V_{DD(FAIL)}$ with V_{PWR} in nominal voltage range,
- V_{DD} and V_{PWR} supplies is below $V_{SUPPLY(POR)}$ voltage value.

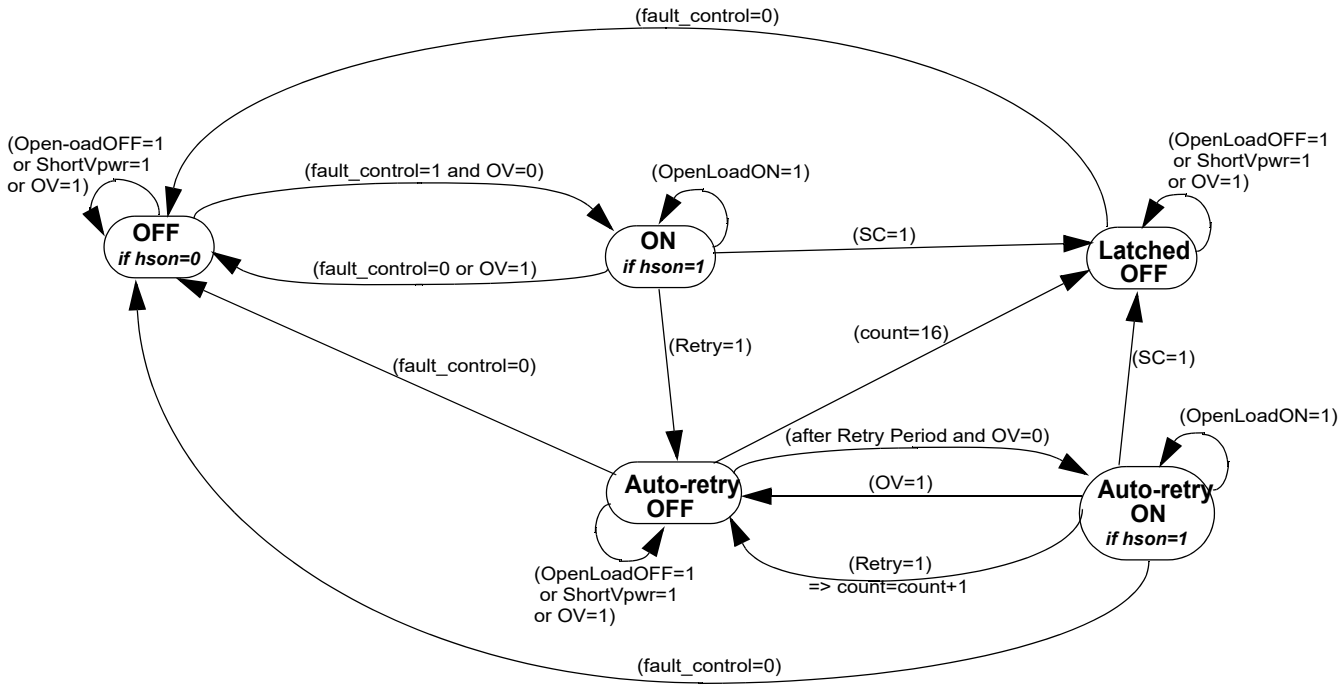


Figure 16. Autoretry state machine

7.3.2 Autoretry

The autoretry circuitry is used to reactivate the output(s) automatically in case of overcurrent or overtemperature or undervoltage failure conditions to provide a high availability of the load.

Autoretry feature is available in Fault mode. It is activated in case of internal retry signal is set to logic [1]:

retry[x] = OC[x] or OT[x] or UV.

The feature retries to switch-on the output(s) after one autoretry period (t_{AUTO}) with a limitation in term of number of occurrence (16 for each output). The counter of retry occurrences is reset in case of Fail-safe to Normal or Normal to Fail-safe mode transitions. At each autoretry, the overcurrent detection will be set to default values in order to sustain the inrush current.

The Figure 16 describes the autoretry state machine.

7.3.3 Diagnostic

7.3.3.1 Output shorted to VPWR fault

The 35XS3400 incorporates output shorted to VPWR detection circuitry in OFF state. Output shorted to VPWR fault is detected if output voltage is higher than $V_{OSD(THRES)}$ and reported as a fault condition when the output is disabled (OFF). The output shorted to VPWR fault is latched into the status register after the internal gate voltage is pulled low enough to turn OFF the output. The OS[0:3] and OL_OFF[0:3] fault bits are set in the status register and $\overline{FS}$ pin reports in real time the fault. If the output shorted to VPWR fault is removed, the status register will be cleared after reading the register.

The open output shorted to VPWR protection can be disabled through SPI (OS_DIS[0:3] bit).

7.3.3.2 Openload faults

The 35XS3400 incorporates three dedicated openload detection circuitries on the output to detect in OFF and in ON state.

7.3.3.3 Openload detection on OFF state

The OFF output openload fault is detected when the output voltage is higher than $V_{OLD(THRES)}$ pulled up with internal current source ($I_{OLD(OFF)}$) and reported as a fault condition when the output is disabled (OFF). The OFF Output OpenLoad fault is latched into the status register or when the internal gate voltage is pulled low enough to turn OFF the output. The OL_OFF[0:3] fault bit is set in the status register. If the OpenLoad fault is removed ($\overline{FS}$ output pin goes to high), the status register will be cleared after reading the register.

The OFF output OpenLoad protection can be disabled through SPI (OLOFF_DIS[0:3] bit).

7.3.3.4 Openload detection in ON state

The ON output openload current thresholds can be chosen by SPI to detect a standard bulbs or LEDs (OLLED[0:3] bit set to logic [1]). In cases where the load current drops below the defined current threshold, the OLON bit will be set to a logic [1], the output will stay ON and $\overline{FS}$ will not be disturbed.

7.3.3.5 Openload detection in ON state for LED

Openload for LEDs only (OLLED[0:3] set to logic [1]) is detected periodically each t_{OLLED} (fully-on, D[7:0]=FF). To detect OLLED in fully-on state, the output must be ON at least t_{OLLED} and PWM module must be enabled (PWM_en = 1 in GCR register).

To delatch the diagnosis, the condition should be removed and SPI read operation is needed (OL_ON[0:3] bit). The ON output openload protection can be disabled through SPI (OLON_DIS[0:3] bit).

7.3.4 Analog current recopy and temperature feedback

The CSNS pin is an analog output reporting a current proportional to the designed output current or a voltage proportional to the temperature of the GND flag (pin #14). The routing is SPI programmable (TEMP_en, CSNS_en, CSNS_s[1,0] and CSNS_ratio_s bits).

In case the current recopy is active, the CSNS output delivers current only during ON time of the output switch without overshoot. The maximum current is 2.0 mA typical. The typical value of external CSNS resistor connected to the ground is 4.7 kΩ.

The current recopy is not active in Fail-safe mode.

7.3.5 Temperature prewarning detection

In Normal mode, the 35XS3400 provides a temperature prewarning reported via SPI in case of the temperature of the GND flag is higher than T_{OTWAR}. This diagnosis (OTW bit set to [1]) is latched in the SPI DIAGR0 register. To delatch, a read SPI command is needed.

7.3.6 Active clamp on VPWR

The device provides an active gate clamp circuit in order to limit the maximum transient V_{PWR} voltage at $VPWR_{(CLAMP)}$. In case of overload on an output, the corresponding output is turned off, which leads to a high-voltage at VPWR with an inductive VPWR line. When VPWR voltage exceeds $VPWR_{(CLAMP)}$ threshold, the turn-off on the corresponding output is deactivated and all HS[0:3] outputs are switched ON automatically to demagnetize the inductive Battery line.

For a long battery line between the battery and the device (> 20 meters), the smart high-side switch output may exceed the energy capability, in case of a short-circuit. It is recommended to implement a voltage transient suppressor to drain the battery line energy.

7.3.7 Reverse battery on VPWR

The output survives the application of reverse voltage as low as -18 V. Under these conditions, the ON resistance of the output is 2 times higher than typical ohmic value in forward mode. No additional passive components are required except on V_{DD} current path.

7.3.8 Ground disconnect protection

In the event the 35XS3400 ground is disconnected from load ground, the device protects itself and safely turns OFF the output regardless of the state of the output at the time of disconnection (maximum VPWR=16 V). A 10 kΩ resistor needs to be added between the MCU and each digital input pin in order to ensure that the device turns off in case of ground disconnect and to prevent this pin from exceeding maximum ratings.

7.3.9 Loss of supply lines

7.3.9.1 Loss of V_{DD}

If the external V_{DD} supply is disconnected (or not within specification: $V_{DD}<V_{DD(FAIL))}$ with VDD_FAIL_en bit is set to logic [1]), all SPI register content is reset.

The outputs can still be driven by the direct inputs IN[0:3] if V_{PWR} is within specified voltage range. The 35XS3400 uses the battery input to power the output MOSFET related current sense circuitry and any other internal logic providing Fail-safe device operation with no V_{DD} supplied. In this state, the overtemperature, overcurrent, severe short-circuit, short to VPWR and OFF openload circuitry are fully operational with default values corresponding to all SPI bits are set to logic [0]. No current is conducted from VPWR to V_{DD}.

7.3.9.2 Loss of V_{PWR}

If the external VPWR supply is disconnected (or not within specification), the SPI configuration, reporting, and daisy chain features are provided for $\overline{RST}$ is set to logic [1] under V_{DD} in nominal conditions. This fault condition can be diagnosed with a UV fault in the SPI STATS_s registers. The SPI pull-up and pull-down current sources are not operational. The previous device configuration is maintained. No current is conducted from VDD to VPWR.

7.3.9.3 Loss of V_{PWR} and V_{DD}

If the external VPWR and VDD supplies are disconnected (or not within specification: (VDD and VPWR) < $V_{SUPPLY(POR)}$), all SPI register contents are reset with default values corresponding to all SPI bits are set to logic [0] and all latched faults are also reset.

7.3.10 EMC performances

All following tests are performed on NXP evaluation board in accordance with the typical application schematic.

The device is protected in case of positive and negative transients on the VPWR line (per ISO 7637-2).

The 35XS3400 successfully meets the Class 5 of the CISPR25 emission standard and 200 V/m or BCI 200 mA injection level for immunity tests.

7.4 Logic commands and registers

7.4.1 Serial input communication

SPI communication is accomplished using 16-bit messages. A message is transmitted by the MCU starting with the MSB D15 and ending with the LSB, D0 (Table 11). Each incoming command message on the SI pin can be interpreted using the following bit assignments: the MSB, D15, is the watchdog bit (WDIN). In some cases, output selection is done with bits D14:D13. The next three bits, D12:D10, are used to select the command register. The remaining nine bits, D8:D0, are used to configure and control the outputs and their protection features.

Multiple messages can be transmitted in succession to accommodate those applications where daisy-chaining is desirable, or to confirm transmitted data, as long as the messages are all multiples of 16 bits. Any attempt made to latch in a message that is not 16 bits will be ignored.

The 35XS3400 has defined registers, which are used to configure the device and to control the state of the outputs. Table 12 summarizes the SI registers.

Table 11. SI message bit assignment

Bit sig	SI msg bit	Message bit description
MSB	D15	Watchdog in: toggled to satisfy watchdog requirements.
	D14:D13	Register address bits used in some cases for output selection (Table 12).
	D12:D10	Register address bits.
	D9	Not used (set to logic [0]).
LSB	D8:D0	Used to configure the inputs, outputs, and the device protection features and SO status content.

Table 12. Serial input address and configuration bit map

SI Register	SI Data															
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
STATR_s	WDIN	X	X	0	0	0	0	0	0	0	0	SOA4	SOA3	SOA2	SOA1	SOA0
PWMR_s	WDIN	A_1	A_0	0	0	1	0	0	ON_s	PWM6_s	PWM5_s	PWM4_s	PWM3_s	PWM2_s	PWM1_s	PWM0_s
CONFR0_s	WDIN	A_1	A_0	0	1	0	0	0	0	0	DIR_dis_s	SR1_s	SR0_s	DELAY2_s	DELAY1_s	DELAY0_s
CONFR1_s	WDIN	A_1	A_0	0	1	1	0	0	0	Retry_ unlimited_s	Retry_dis_s	OS_dis_s	OLON_dis_s	OLOFF_dis_s	OLLED_en_s	CSNS_ratio_s
OCR_s	WDIN	A_1	A_0	1	0	0	0	0	BC1_s	BC0_s	OC1_s	OC0_s	OCHI_s	OCLO1_s	OCLCO0_s	OC_mode_s
GCR	WDIN	0	0	1	0	1	0	VDD_FAIL_en	PWM_en	CLOCK_sel	TEMP_en	CSNS_en	CSNS1	CSNS0	X	OV_dis
CALR	WDIN	0	0	1	1	1	0	1	0	0	0	1	1	0	1	1
Register state after RST=0 or $V_{DD(FAIL)}$ or $V_{SUPPLY(POR)}$ condition	0	0	0	X	X	X	0	0	0	0	0	0	0	0	0	0

x=Don't care.
s=Output selection with the bits A_1A_0 as defined in Table 13.

7.4.2 Device register addressing

The following section describes the possible register addresses (D[14:10]) and their impact on device operation.

7.4.2.1 Address XX000—Status register (STATR_S)

The STATR register is used to read the device status and the various configuration register contents without disrupting the device operation or the register contents. The register bits D[4:0] determine the content of the first sixteen bits of SO data. In addition to the device status, this feature provides the ability to read the content of the PWMR_s, CONFR0_s, CONFR1_s, OCR_s, GCR and CALR registers (see Serial output communication (device status return data).

7.4.2.2 Address $A_1A_0$001—Output PWM control register (PWMR_S)

The PWMR_s register allows the MCU to control the state of corresponding output through the SPI. Each output “s” is independently selected for configuration based on the state of the D14:D13 bits (Table 13).

Table 13. Output selection

A_1 (D14)	A_0 (D13)	HS selection
0	0	HS0 (default)
0	1	HS1
1	0	HS2
1	1	HS3

Bit D7 sets the output state. A logic [1] enables the corresponding output switch and a logic [0] turns it OFF (if IN input is also pulled down). Bits D6:D0 set the output PWM duty-cycle to one of 128 levels for PWM_en is set to logic [1], as shown Table 8.

7.4.2.3 Address $A_1A_0$010—Output configuration register (CONFR0_S)

The CONFR0_s register allows the MCU to configure corresponding output switching through the SPI. Each output “s” is independently selected for configuration based on the state of the D14:D13 bits (Table 13).

For the selected output, a logic [0] on bit D5 (DIR_DIS_s) will enable the output for direct control. A logic [1] on bit D5 will disable the output from direct control (in this case, the output is only controlled by On bit).

D4:D3 bits (SR1_s and SR0_s) are used to select the high or medium or low speed slew rate for the selected output, the default value [00] corresponds to the medium speed slew rate (Table 14).

Table 14. Slew rate speed selection

SR1_s (D4)	SR0_s (D3)	Slew rate speed
0	0	medium (default)
0	1	low
1	0	high
1	1	Not used

Incoming message bits D2:D0 reflect the desired output that will be delayed of predefined PWM clock rising edges number, as shown Table 9 (only available for PWM_en bit is set to logic [1]).

7.4.2.4 Address $A_1A_0$011—Output configuration register (CONFR1_S)

The CONFR1_s register allows the MCU to configure corresponding output fault management through the SPI. Each output “s” is independently selected for configuration based on the state of the D14:D13 bits (Table 13).

A logic [1] on bit D6 (RETRY_unlimited_s) disables the autoretry counter for the selected output, the default value [0] corresponds to enable autoretry feature with time limitation.

A logic [1] on bit D5 (RETRY_dis_s) disables the autoretry for the selected output, the default value [0] corresponds to enable this feature.

A logic [1] on bit D4 (OS_dis_s) disables the output hard shorted to VPWR protection for the selected output, the default value [0] corresponds to enable this feature.

A logic [1] on bit D3 (OLON_dis_s) disables the ON output openload detection for the selected output, the default value [0] corresponds to enable this feature (Table 15).

A logic [1] on bit D2 (OLOFF_dis_s) disables the OFF output openload detection for the selected output, the default value [0] corresponds to enable this feature.

A logic [1] on bit D1 (OLLED_en_s) enables the ON output openload detection for LEDs for the selected output, the default value [0] corresponds to ON output openload detection is set for bulbs (Table 15).

Table 15. ON openload selection

OLON_dis_s (D3)	OLLED_en_s (D1)	ON openload detection
0	0	enable with bulb threshold (default)

Table 15. ON openload selection

0	1	enable with LED threshold
1	X	disable

A logic [1] on bit D0 (CSNS_ratio_s) selects the high ratio on the CSNS pin for the corresponding output. The default value [0] is the low ratio (Table 16).

Table 16. Current sense ratio selection

CSNS_high_s (D0)	Current sense ratio
0	CRS0 (default)
1	CRS1

7.4.2.5 Address A_1A_0100—Output overcurrent register (OCR)

The OCR_s register allows the MCU to configure corresponding output overcurrent protection through the SPI. Each output “s” is independently selected for configuration based on the state of the D14:D13 bits (Table 13).

D[7:6] bits allow to MCU to programmable bulb cooling curve and D[5:4] bits inrush curve for selected output, as shown Table 17 and Table 18.

Table 17. Cooling and inrush curve selection

BC1_s (D7)	BC0_s (D6)	Profile curves speed
0	0	medium (default)
0	1	slow
1	0	fast
1	1	medium

Table 18. Inrush curve selection

OC1_s (D5)	OC0_s (D4)	Profile curves speed
0	0	slow (default)
0	1	fast
1	0	medium
1	1	very slow

A logic [1] on bit D3 (OCHI_s bit) the OCHI1 level is replaced by OCHI2 during t_{OC1}, as shown Figure 17.

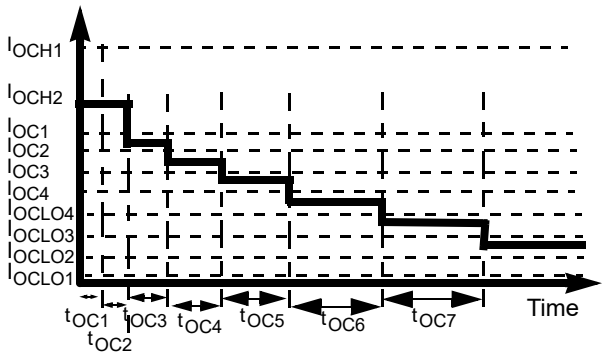


Figure 17. Overcurrent profile with OCHI bit set to ‘1’

The wire harness is protected by one of four possible current levels in steady state, as defined in Table 19.

Table 19. Output steady state selection

OCLO1 (D2)	OCLO0 (D1)	Steady state current
0	0	OCLO2 (default)
0	1	OCLO3
1	0	OCLO4
1	1	OCLO1

Bit D0 (OC_mode_sel) allows to select the overcurrent mode, as described Table 20.

Table 20. Overcurrent mode selection

OC_mode_s (D0)	Overcurrent mode
0	only inrush current management (default)
1	inrush current and bulb cooling management

7.4.2.6 Address 00101—Global configuration register (GCR)

The GCR register allows the MCU to configure the device through the SPI.

Bit D8 allows the MCU to enable or disable the V_{DD} failure detector. A logic [1] on VDD_FAIL_en bit allows transitioning to Fail-safe mode for $V_{DD} < V_{DD(FAIL)}$.

Bit D7 allows the MCU to enable or disable the PWM module. A logic [1] on PWM_en bit allows control of the outputs HS[0:3] with PWMR register (the direct input states are ignored).

Bit D6 (CLOCK_sel) allows to select the clock used as reference by PWM module, as described in the following Table 21.

Table 21. PWM module selection

PWM_en (D7)	CLOCK_sel (D6)	PWM module
0	X	PWM module disabled (default)
1	0	PWM module enabled with external clock from IN0
1	1	PWM module enabled with internal calibrated clock

Bits D5:D4 allow the MCU to select one of two analog feedback on CSNS output pin, as shown in Table 22.

Table 22. CSNS reporting selection

TEMP_en (D5)	CSNS_en (D4)	CSNS reporting
0	0	CSNS tri-stated (default)
X	1	current recopy of selected output (D3:2] bits)
1	0	temperature on GND flag

Table 23. Output current recopy selection

CSNS1 (D3)	CSNS0 (D2)	CSNS reporting
0	0	HS0 (default)
0	1	HS1
1	0	HS2
1	1	HS3

The GCR register disables the overvoltage protection (D0). When this bits is [0], the overvoltage is enabled (default value).

7.4.2.7 Address 00111—Calibration register (CALR)

The CALR register allows the MCU to calibrate internal clock, as explained in Figure 16.

7.4.3 Serial output communication (device status return data)

When the $\overline{CS}$ pin is pulled low, the output register is loaded. Meanwhile, the data is clocked out MSB- (OD15-) first as the new message data is clocked into the SI pin. The first sixteen bits of data clocking out of the SO, and following a $\overline{CS}$ transition, is dependent upon the previously written SPI word.

Any bits clocked out of the Serial Output (SO) pin after the first 16 bits will be representative of the initial message bits clocked into the SI pin since the $\overline{CS}$ pin first transitioned to a logic [0]. This feature is useful for daisy-chaining devices as well as message verification.

A valid message length is determined following a $\overline{CS}$ transition of [0] to [1]. If there is a valid message length, the data is latched into the appropriate registers. A valid message length is a multiple of 16 bits. At this time, the SO pin is tri-stated and the fault status register is now able to accept new fault status information.

SO data will represent information ranging from fault status to register contents, user selected by writing to the STATR bits OD4, OD3, OD2, OD1, and OD0. The value of the previous bits SOA4 and SOA3 will determine which output the SO information applies to for the registers which are output specific; viz., Fault, PWMR, CONFR0, CONFR1, and OCR registers.

Note that the SO data will continue to reflect the information for each output (depending on the previous SOA4, SOA3 state) that was selected during the most recent STATR write until changed with an updated STATR write.

The output status register correctly reflects the status of the STATR-selected register data at the time that the $\overline{CS}$ is pulled to a logic [0] during SPI communication, and/or for the period of time since the last valid SPI communication, with the following exception:

- The previous SPI communication was determined to be invalid. In this case, the status will be reported as though the invalid SPI communication never occurred.
- The VPWR voltage is below 4.0 V, the status must be ignored by the MCU.

7.4.4 Serial output bit assignment

The 16 bits of serial output data depend on the previous serial input message, as explained in the following paragraphs. Table 24, summarizes SO returned data for bits OD15:OD0.

- Bit OD15 is the MSB; it reflects the state of the Watchdog bit from the previously clocked-in message.
- Bits OD14:OD10 reflect the state of the bits SOA4:SOA0 from the previously clocked in message.
- Bit OD9 is set to logic [1] in Normal mode (NM).
- The contents of bits OD8:OD0 depend on bits D4:D0 from the most recent STATR command SOA4:SOA0 as explained in the paragraphs following Table 24.

Table 24. Serial output bit map description

	Previous STATR					**SO returned data**														
	SOA4	**SOA3**	**SOA2**	**SOA1**	**SOA0**	**OD15**	**OD14**	**OD13**	**OD12**	**OD11**	**OD10**	**OD9**	**OD8**	**OD7**	**OD6**	**OD5**	**OD4**	**OD3**	**OD2**	**OD1**	**OD0**
STATR_s	A_1	A_0	0	0	0	WDIN	SOA4	SOA3	SOA2	SOA1	SOA0	NM	POR	UV	OV	OLON_s	OLOFF_s	OS_s	OT_s	SC_s	OC_s
PWMR_s	A_1	A_0	0	0	1	WDIN	SOA4	SOA3	SOA2	SOA1	SOA0	NM	0	ON_s	PWM6_s	PWM5_s	PWM4_s	PWM3_s	PWM2_s	PWM1_s	PWM0_s
CONFR0_s	A_1	A_0	0	1	0	WDIN	SOA4	SOA3	SOA2	SOA1	SOA0	NM	X	X	X	DIR_dis_s	SR1_s	SR0_s	DELAY2_s	DELAY1_s	DELAY0_s
CONFR1_s	A_1	A_0	0	1	1	WDIN	SOA4	SOA3	SOA2	SOA1	SOA0	NM	X	X	Retry_unlimited_s	Retry_dis_s	OS_dis_s	OLON_dis_s	OLOFF_dis_s	OLLED_en_s	CSNS_ratio_s
OCR_s	A_1	A_0	1	0	0	WDIN	SOA4	SOA3	SOA2	SOA1	SOA0	NM	X	BC1_s	BC0_s	OC1_s	OC0_s	OCHI_s	OCLO1_s	OCLO0_s	OC_mode_s
GCR	0	0	1	0	1	WDIN	SOA4	SOA3	SOA2	SOA1	SOA0	NM	VDD_FAIL_en	PWM_en	CLOCK_sel	TEMP_en	CSNS_en	CSNS1	CSNS0	X	OV_dis
DIAGR0	0	0	1	1	1	WDIN	SOA4	SOA3	SOA2	SOA1	SOA0	NM	X	X	X	X	X	X	CLOCK_fail	CAL_fail	OTW
DIAGR1	0	1	1	1	1	WDIN	SOA4	SOA3	SOA2	SOA1	SOA0	NM	X	X	X	X	IN3	IN2	IN1	IN0	WD_en
DIAGR2	1	0	1	1	1	WDIN	SOA4	SOA3	SOA2	SOA1	SOA0	NM	X	X	X	X	X	x	1	X	X
Register state after RST=0 or $V_{DD(FAIL)}$ or $V_{SUPPLY(POR)}$ condition	N/A	N/A	N/A	N/A	N/A	0	0	0	0	0	0	0	X	0	0	0	0	0	0	0	0

s = Output selection with the bits A_1A_0 as defined in Table 13

7.4.4.1 Previous address SOA4:SOA0=$A_1A_0$000 (STATR_S)

The returned data OD8 reports logic [1] in case of previous power-on reset condition ($V_{SUPPLY(POR)}$). This bit is only reset by a read operation.

Bits OD7:OD0 reflect the current state of the Fault register (FLTR) corresponding to the output previously selected with the bits SOA4:SOA3 = A_1A_0 (Table 24).

- OC_s: overcurrent fault detection for a selected output,
- SC_s: severe short-circuit fault detection for a selected output,
- OS_s: output shorted to VPWR fault detection for a selected output,
- OLOFF_s: openload in OFF state fault detection for a selected output,
- OLON_s: openload in ON state fault detection (depending on current level threshold: bulb or LED) for a selected output,
- OV: overvoltage fault detection,
- UV: undervoltage fault detection
- POR: power on reset detection.

The $\overline{FS}$ pin reports all faults. For latched faults, this pin is reset by a new Switch OFF command (toggling fault_control signal).

7.4.4.2 Previous Address SOA4:SOA0=$A_1A_0$001 (PWMR_S)

The returned data contains the programmed values in the PWMR register for the output selected with A_1A_0.

7.4.4.3 Previous Address SOA4:SOA0=$A_1A_0$010 (CONFR0_S)

The returned data contains the programmed values in the CONFR0 register for the output selected with A_1A_0.

7.4.4.4 Previous Address SOA4:SOA0=$A_1A_0$011 (CONFR1_S)

The returned data contains the programmed values in the CONFR1 register for the output selected with A_1A_0.

7.4.4.5 Previous Address SOA4:SOA0=$A_1A_0$100 (OCR_S)

The returned data contains the programmed values in the OCR register for the output selected with A_1A_0.

7.4.4.6 Previous Address SOA4:SOA0=00101 (GCR)

The returned data contains the programmed values in the GCR register.

7.4.4.7 Previous Address SOA4:SOA0=00111 (DIAGR0)

The returned data OD2 reports logic [1] in case of PWM clock on IN0 pin is out of specified frequency range.

The returned data OD1 reports logic [1] in case of calibration failure.

The returned data OD0 reports logic [1] in case of overtemperature prewarning (temperature of GND flag is above T_{OTWAR}).

7.4.4.8 Previous Address SOA4:SOA0=01111 (DIAGR1)

The returned data OD4: OD1 report in real time the state of the direct input IN[3:0].

The OD0 indicates if the watchdog is enabled (set to logic [1]) or not (set to logic [0]). OD4:OD1 report the output state in case of Fail-safe state due to watchdog time-out as explained in the following Table 25.

Table 25. Watchdog activation report

WD_en (OD0)	SPI watchdog
0	disabled
1	enabled

7.4.4.9 Previous address SOA4:SOA0=10111 (DIAGR2)

The returned data is the product ID. Bits OD2:OD0 are set to 1XX for protected quad 35 mΩ high-side switches.

7.4.5 Default device configuration

The default device configuration is explained below:

- HS output is commanded by corresponding IN input or ON bit through SPI. The medium slew rate is used,
- HS output is fully protected by the severe short-circuit protection, the undervoltage, and the overtemperature protection. The autoretry feature is enabled,
- Openload in ON and OFF state and HS shorted to VPWR detections are available,
- No current recopy and no analog temperature feedback active,
- Overvoltage protection is enabled,
- SO reporting fault status from HS0,
- VDD failure detection is disabled.

8 Typical applications

The following figure shows a typical automotive lighting application (only one vehicle corner) using an external PWM clock from the main MCU. A redundancy circuitry has been implemented to substitute light control (from MCU to watchdog) in case of a Fail-safe condition.

It is recommended to locate a 22 nF decoupling capacitor to the module connector.

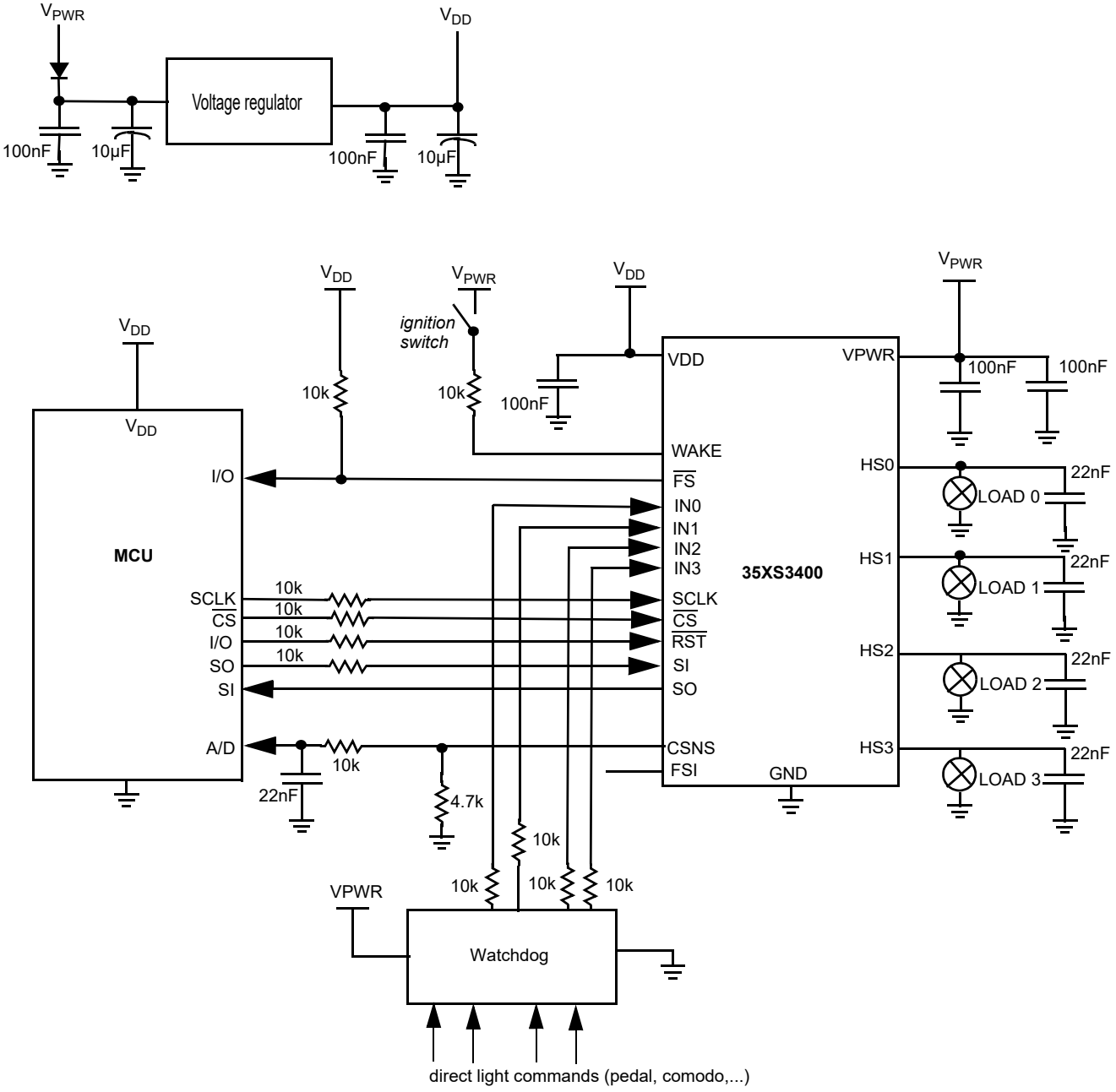


Figure 18. Typical application schematic

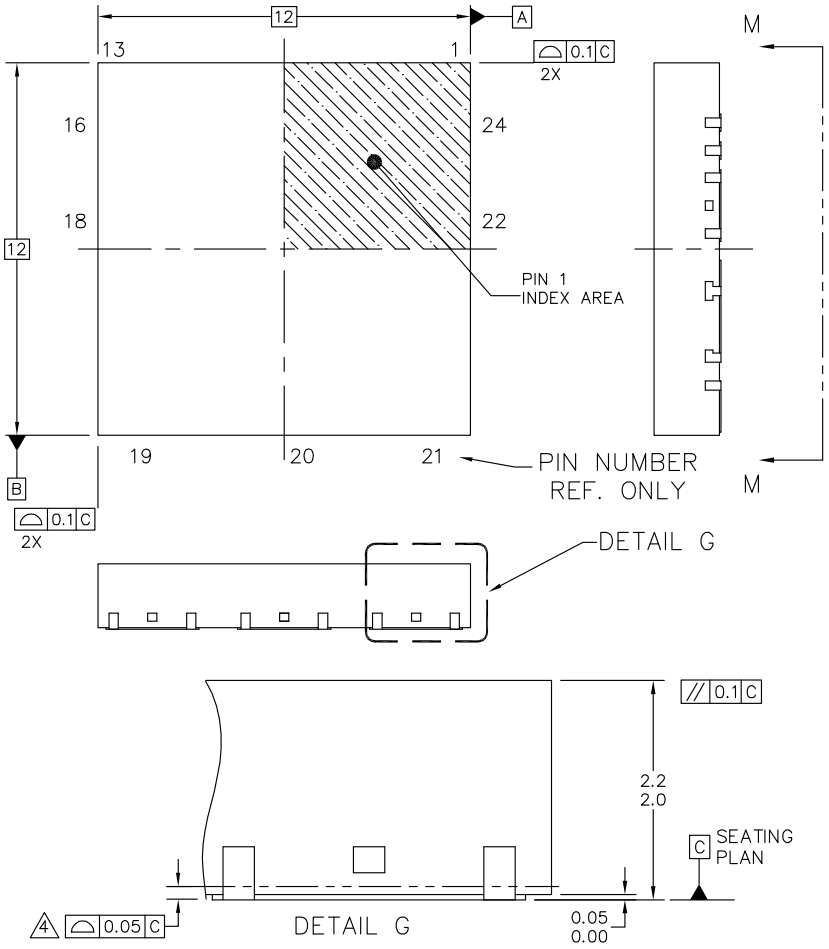
9 Packaging

9.1 Soldering information

The 35XS3400 is packaged in a surface mount power package intended to be soldered directly on the printed circuit board. The AN2467 application note provides guidelines for printed circuit board design and assembly.

9.2 Package dimensions

For the most current package revision, visit **www.nxp.com** and perform a keyword search using the 98ARL10596D listed below. Dimensions shown are provided for reference ONLY.



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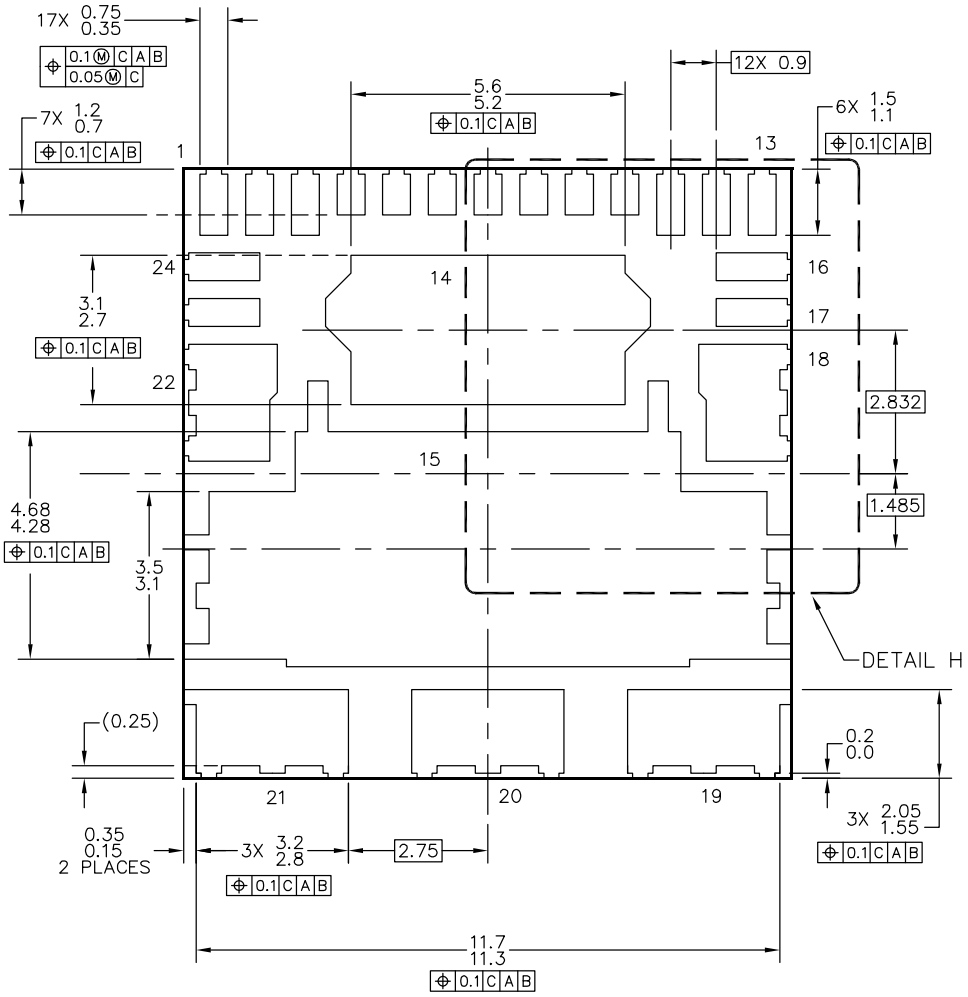
TITLE: POWER QUAD FLAT NON-LEADED PACKAGE (PWR QFN) 24 TERMINAL, 0.9 PITCH(12X12X2.1)	DOCUMENT NO: 98ARL10596D	REV: D
	CASE NUMBER: 1593-04	14 FEB 2008
	STANDARD: NON-JEDEC	

FK SUFFIX
24-PIN PQFN
NONLEADED PACKAGE
98ARL10596D
ISSUE D

35XS3400



VIEW M–M

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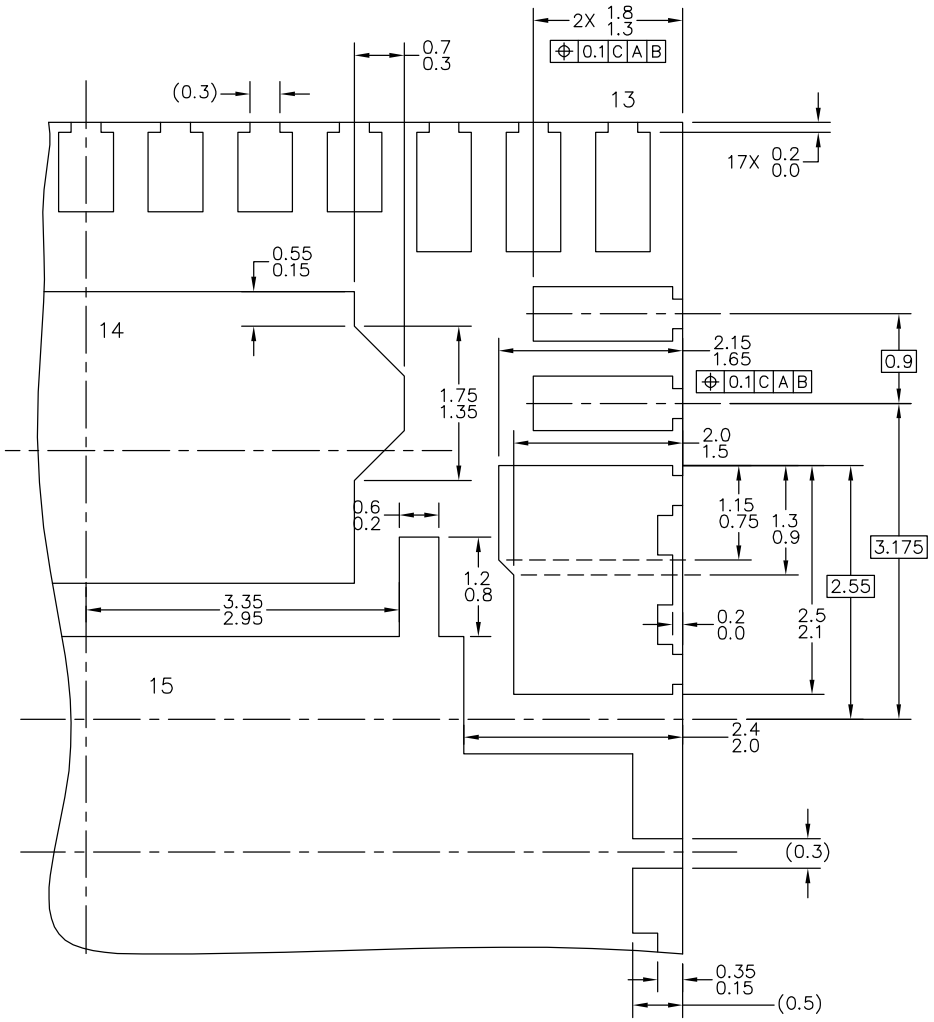
TITLE: POWER QUAD FLAT NON–LEADED PACKAGE (PWR QFN) 24 TERMINAL, 0.9 PITCH(12X12X2.1)	DOCUMENT NO: 98ARL10596D	REV: D
	CASE NUMBER: 1593–04	14 FEB 2008
	STANDARD: NON–JEDEC	

FK SUFFIX
24-PIN PQFN
NONLEADED PACKAGE
98ARL10596D
ISSUE D



DETAIL H

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TITLE: POWER QUAD FLAT NON–LEADED PACKAGE (PWR QFN) 24 TERMINAL, 0.9 PITCH(12X12X2.1)	DOCUMENT NO: 98ARL10596D	REV: D
	CASE NUMBER: 1593–04	14 FEB 2008
	STANDARD: NON–JEDEC	

FK SUFFIX
24-PIN PQFN
NONLEADED PACKAGE
98ARL10596D
ISSUE D

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFP–N.
4. COPLANARITY APPLIES TO LEADS AND CORNER LEADS.
5. MINIMUM METAL GAP IS GUARANTEED TO BE 0.25MM.

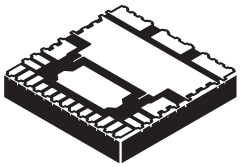
MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: POWER QUAD FLAT NON–LEADED PACKAGE (PWR QFN) 24 TERMINAL, 0.9 PITCH(12X12X2.1)	DOCUMENT NO: 98ARL10596D	REV: D
	CASE NUMBER: 1593–04	14 FEB 2008
	STANDARD: NON–JEDEC	

FK SUFFIX
24-PIN PQFN
NONLEADED PACKAGE
98ARL10596D
ISSUE D

10 Additional documentation

35XS3400

24-PIN PQFN



FK SUFFIX (PB-FREE)
98ARL10596D
24-PIN PQFN (12 x 12)

Note: For package dimensions, see 98ARL10596D.

10.1 Thermal addendum (Rev 2.0)

10.1.1 Introduction

This thermal addendum is provided as a supplement to the 35XS3400 technical data sheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application and packaging information is provided in the data sheet.

10.1.2 Package and thermal considerations

This 35XS3400 is a dual die package. There are two heat sources in the package independently heating with P_1 and P_2. This results in two junction temperatures, T_{J1} and T_{J2}, and a thermal resistance matrix with $R_{\theta JAmn}$.

For m, n = 1, $R_{\theta JA11}$ is the thermal resistance from Junction 1 to the reference temperature while only heat source 1 is heating with P_1.

For m = 1, n = 2, $R_{\theta JA12}$ is the thermal resistance from Junction 1 to the reference temperature while heat source 2 is heating with P_2. This applies to $R_{\theta J21}$ and $R_{\theta J22}$, respectively.

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} R_{\theta JA11} & R_{\theta JA12} \\ R_{\theta JA21} & R_{\theta JA22} \end{bmatrix} \cdot \begin{Bmatrix} P_1 \\ P_2 \end{Bmatrix}$$

The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment. Stated values were obtained by measurement and simulation according to the standards listed below.

10.1.3 Standards

Table 26. Thermal performance comparison

Thermal resistance	1 = Power chip, 2 = Logic chip [°C/W]		
	m **= 1,** ***n*** **= 1**	***m*** **= 1,** ***n*** **= 2** ***m*** **= 2,** ***n*** **= 1**	***m*** **= 2,** ***n*** **= 2**
$R_{\theta JAmn}$ (1)(2)	27.35	18.40	35.25
$R_{\theta JBmn}$ (2)(3)	14.53	6.64	23.69
$R_{\theta JAmn}$ (1)(4)	47.63	37.21	53.61
$R_{\theta JCmn}$ (5)	1.48	0.00	0.95

Notes:
1. Per JEDEC JESD51-2 at natural convection, still air condition.
2. 2s2p thermal test board per JEDEC JESD51-7 and JESD51-5.
3. Per JEDEC JESD51-8, with the board temperature on the center trace near the power outputs.
4. Single layer thermal test board per JEDEC JESD51-3 and JESD51-5.
5. Thermal resistance between the die junction and the exposed pad, “infinite” heat sink attached to exposed pad.

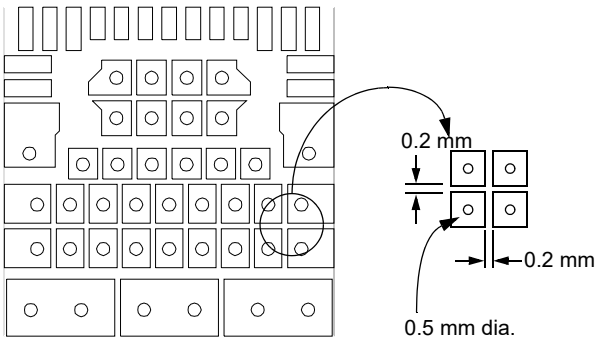


Figure 19. Detail of copper traces under device with thermal vias

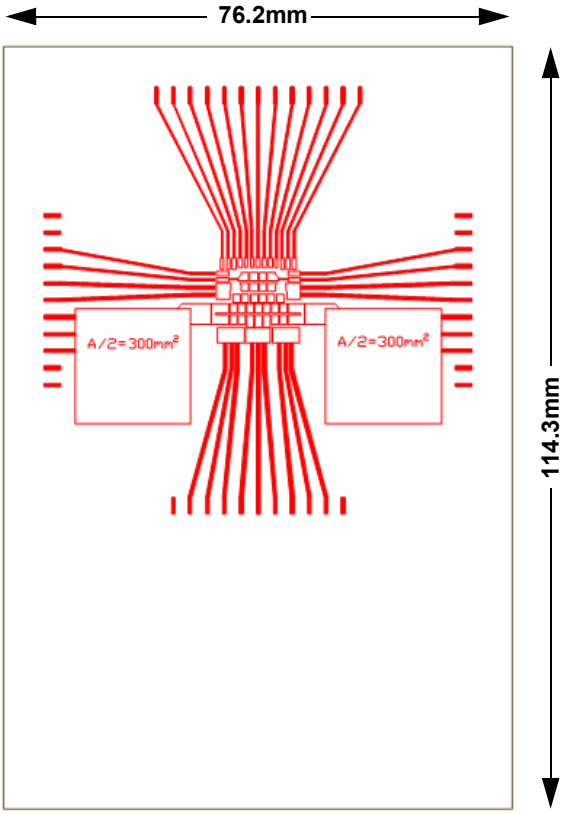


Figure 20. 1s JEDEC thermal test board layout

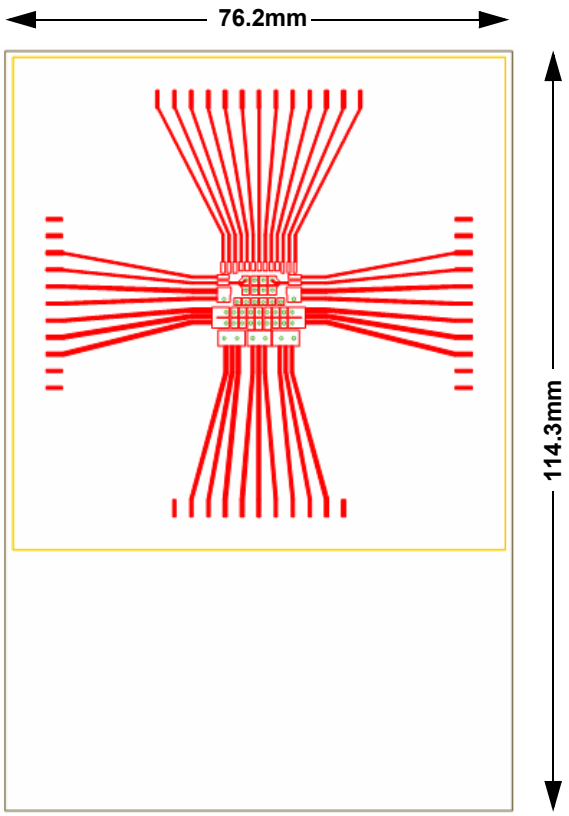
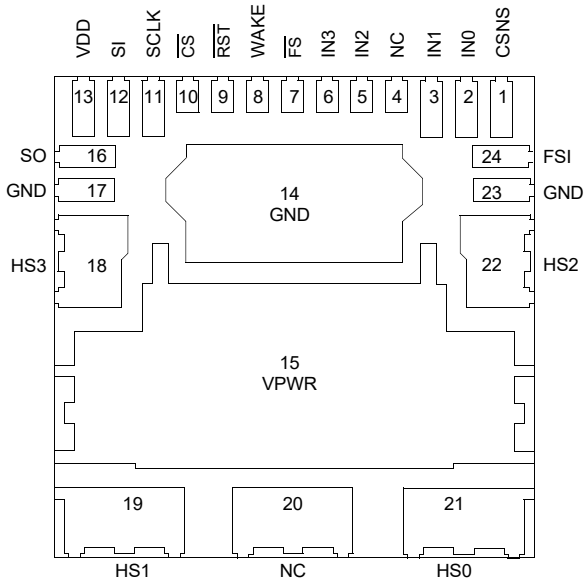


Figure 21. 2s2p JEDEC thermal test board
(Red - top layer, Yellow - two buried layers)

Transparent Top View



MC35XS3400 Pin Connections
24 Pin PQFN (12 x 12)
0.9mm Pitch
12.0mm x 12.0mm Body

Figure 22. Pin connections

10.1.4 Device on thermal test board

Material:	Single layer printed circuit board FR4, 1.6 mm thickness Cu traces, 0.07 mm thickness Cu buried traces thickness 0.035 mm
Outline:	76.2 mm x 114.3 mm board area, including edge connector for thermal testing, 74 mm x 74 mm buried layers area
Area **A**:	Cu heat-spreading areas on board surface
Ambient conditions:	Natural convection, still air

Table 27. Thermal resistance performance

Thermal resistance	Area A (mm^2)	1 = Power chip, 2 = Logic chip (°C/W)		
		m **= 1,** ***n*** **= 1**	***m*** **= 1,** ***n*** **= 2** ***m*** **= 2,** ***n*** **= 1**	***m*** **= 2,** ***n*** **= 2**
$R_{\theta JAmn}$	0	47.63	37.21	53.61
	150	42.82	33.14	51.06
	300	41.23	31.84	50.36
	450	40.07	30.90	49.26
	600	39.24	30.14	48.57

$R_{\theta JA}$ is the thermal resistance between die junction and ambient air.
This device is a dual die package. Index *m* indicates the die that is heated. Index *n* refers to the number of the die where the junction temperature is sensed.

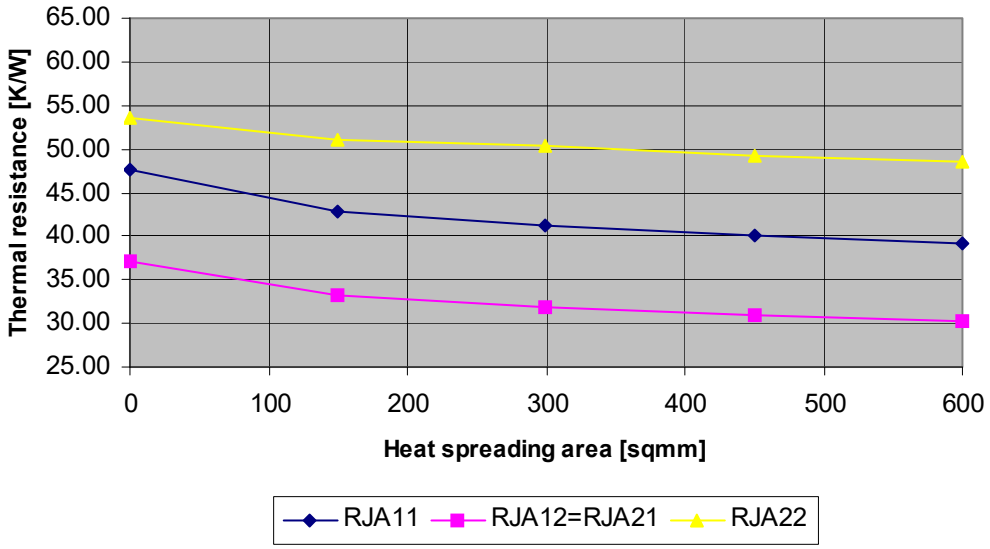


Figure 23. Steady state thermal resistance in dependence on heat spreading area; 1s JEDEC thermal test board with spreading areas

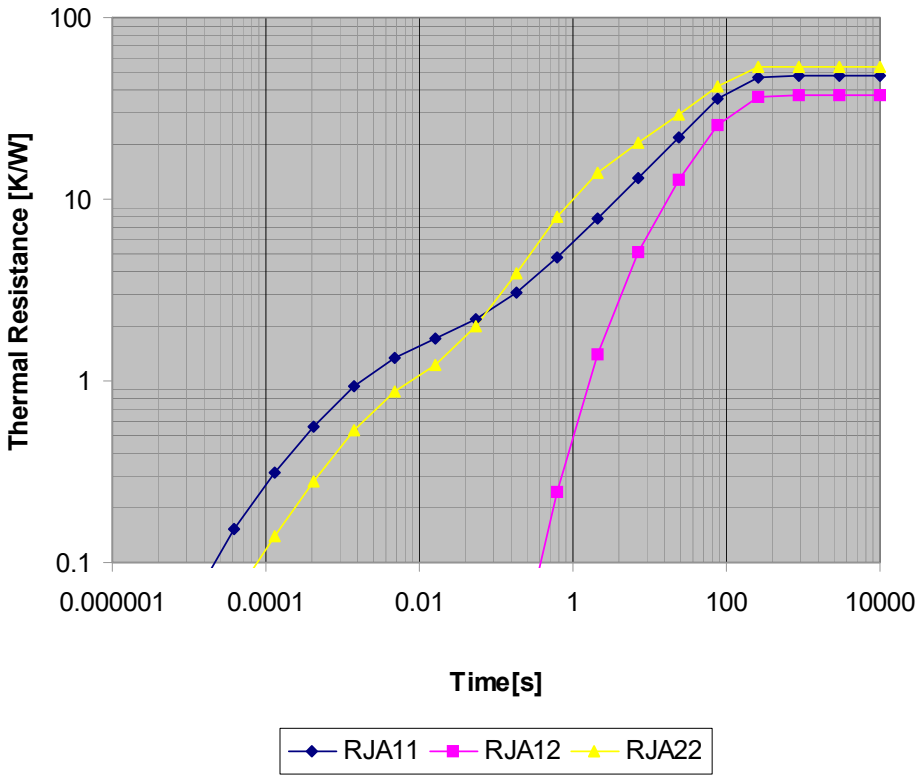


Figure 24. Transient thermal 1W step response; device on 1s JEDEC standard thermal test board with heat spreading areas 600 Sq. mm

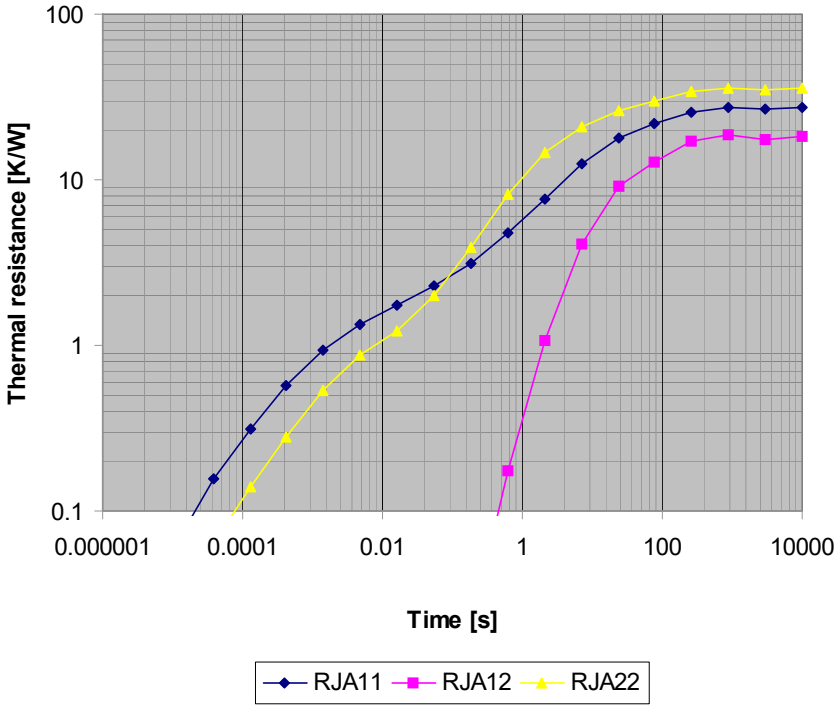


Figure 25. Transient thermal 1W step response; device on 2s2p JEDEC standard thermal test board

11 Revision history

Revision	Date	Description of changes
4.0	9/2008	• Initial release
5.0	10/2008	• Changed Maximum rating for *Output Source-to-Drain ON Resistance* in Static Electrical Characteristics Table on page 7. • Added explanation for recovering to Sleep Mode on page 22.
6.0	7/2009	• Added MC35XS3400DPNA part number. The “D” version has different soldering limits.
7.0	10/2009	• Corrected minor formatting • Separated definitions for the 35XS3400C and 35XS3400D in the Static and Dynamic Tables
8.0	1/2011	• Table 24, Serial output bit map description: (DIAGR2 register): OD1=X (instead of 0) and OD0=X (instead of 0) • 7.4.4.9Previous address SOA4:SOA0=10111 (DIAGR2) 40: bits OD2:OD0 are set to 1XX (instead of 100) for protected.
9.0	05/2012	• Updated part number MC35XS3400DPNA to MC35XS3400DHFK and MC35XS3400CPNA to MC35XS3400CHFK. • Updated the pin soldering temperature limit from 10 seconds to 40 seconds (Note (3) and (10)). • Updated Freescale form and style.
10	8/2013	• Corrected Address A1A0011—Output configuration register (CONFR1_S). Changed from “the default value [0] corresponds to enable auto-retry feature **without** time limitation” to “the default value [0] corresponds to enable auto-retry feature **with** time limitation”.

11	8/2018	• Updated as per CIN 201808007I
		  • Corrected T_{OLLED} values in Table 6, Dynamic electrical characteristics
		  • Updated Openload detection in ON state for LED (added clarification for the usage of openload LED function and changed D[6:0]=7F to D[7:0]=FF)