UM11854 KITPF5030SKTEVM programming board Rev. 1 — 9 March 2023

User manual

Document information

Information	Content
Keywords	PF5030, KITPF5030SKTEVM, KL25Z, I ² C, spf-53091
Abstract	The KITPF5030SKTEVM provides flexibility to explore all the features of the device and make measurements on the main part of the application.



Revision history

Rev	Date	Description
v.1	20230309	Initial release

Important notice

NXP provides the enclosed product(s) under the following conditions:

This evaluation kit is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This evaluation board may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. This evaluation board is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

The goods provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end product incorporating the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. In order to minimize risks associated with the customers applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact NXP sales and technical support services.

1 Introduction

The KITPF5030SKTEVM board user manual is intended for the engineers involved in the evaluation, design, implementation, and validation of PF5030 Configurable Power Management IC.

The KITPF5030SKTEVM enables development on PF5030 family of devices. The kit can be connected to the NXP GUI software, which allows the user to explore registers, try OTP configurations, and burn the part.

The devices can be placed and removed easily from the board using the socket. This board supports the PF5030 family of devices. The delivered board consists of a soldered device with empty OTP content in order to leave the opportunity to the user to burn the OTP configuration. The board contains a superset device PPF5030BMDA0ES, allowing tests on all the PF5030 derivatives. Each device OTP can be burned twice, which provides flexibility.

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2 Finding resources and information on the NXP website

NXP Semiconductors provides online resources for this evaluation board and its supported devices on <u>http://www.nxp.com</u>.

The information page for KITPF5030SKTEVM board is available at <u>http://www.nxp.com/KITPF5030SKTEVM</u>. The information page provides overview information, documentation, software and tools, parametric data, ordering information and a Getting Started tab. The Getting Started tab provides quick-reference information applicable to using the KITPF5030SKTEVM board, including the downloadable assets referenced in this document.

The information page for "NXP GUI for Automotive PMIC Families" is at <u>http://www.nxp.com/NXP GUI for</u> <u>Automotive PMIC Families</u>. The information page provides overview information, documentation, downloads, and development tools.

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3 Getting ready

Working with the KITPF5030SKTEVM requires the kit contents, additional hardware, and a Windows PC workstation with installed software.

3.1 Kit contents

- · Assembled and tested KITPF5030SKTEVM connected to a FRDM-KL25Z in an anti-static bag
- 2 ft or 3 ft USB-STD A to USB-B-mini cable
- 1x Pluggable terminal block, two positions, straight, 3.81 mm pitch
- 3x Pluggable terminal block, three positions, straight, 3.81 mm pitch
- · Jumpers mounted on board
- Quick Start Guide

3.2 Additional hardware

In addition to the kit contents, the following hardware is necessary or beneficial when working with this kit.

• One or two power supplies with a range from 3.3 V to 5.0 V, and a current limit set initially to 1.0 A

3.3 Windows PC workstation

This evaluation board requires a Windows PC workstation. Meeting these minimum specifications should produce great results when working with this evaluation board.

• USB-enabled computer with Windows 7 or Windows 10

3.4 Software

Installing software is necessary to work with this evaluation board. All listed software is available on the evaluation boards information page.

- http://www.nxp.com/KITPF5030SKTEVM
- NXP GUI for automotive PMIC families latest version

4 Getting to know the hardware

The KITPF5030SKTEVM provides flexibility to explore all the features of the device and make measurements on the main part of the application. In combination with the FRDM-KL25Z MCU board, the NXP GUI software allows access to the registers in read and write mode. All regulators are accessible through connectors. DC-DC switching nodes and other nonuser signals are mapped on test points. Digital signals (I²C, RSTB) are accessible through connectors. Pin PWRON has a switch to control them. A supply switch is available to power on or off the device.

The main purpose of this kit is to burn the OTP configuration. The main purpose of this kit is to evaluate PF5030 in automotive applications. The device always starts loading the fused configuration (OTP) (that may be blank) to the mirror registers, then the user can override the mirrors using Emulation mode. The device can be programmed/fused two times. This board is able to fuse the OTP without any extra tools or board. In Emulation mode, as long as the power is supplied, the board configuration stays valid. However, the main and fail-safe configurations are lost when the device restarts or goes into deep fail-safe (DEEP-FS) state, because OTP is reloaded and overwrite the mirrors content.

Note: Due to the socket, this kit is not optimized for performance measurement or current higher than 1.0 A.

4.1 Kit overview

The KITPF5030SKTEVM is a hardware evaluation tool that allows OTP burning. Due to the socket, PF5030 part can be configured without the need to solder it. Devices can be programmed two times. The KITPF5030SKTEVM is a hardware evaluation tool that allows performance test. PF5030 can be evaluated with this board because it is populated with a superset part. The PPF5030BMDA0ES part soldered on the board can be fused twice.

An Emulation mode is possible to test as many configurations as needed. From USB voltage, an external DC-DC provides VDDIO_SEL voltage with a choice of 1.8 V, 3.3 V (default), or 5.0 V. Furthermore, another external DC-DC generates the OTP programming voltage (7.95 V) without any need for an external power supply.

4.2 KITPF5030SKTEVM features

- VIN power supply connector (1x or 2x 3.3 V to 5.0 V)
- BUCK1 and BUCK2: 0.7 V to 1.5 V up to 1.0 A (socket limit)
- BUCK3: 1.0 V to 3.3 V up to 1.0 A (socket limit)
- LDO1 and LDO2: 1.5 V to 5.0 V
- PWRON switch
- FS0B external safety pin
- Embedded USB connection for easy connection to software NXP GUI (access to I²C bus, IOs, RSTB, FS0B, INTB, debug, AMUX_OUT, regulators, register access, OTP emulation, and OTP programming)
- · LEDs that indicate signals and regulator status
- · Support OTP fuse capabilities
- Voltage monitoring jumper setting

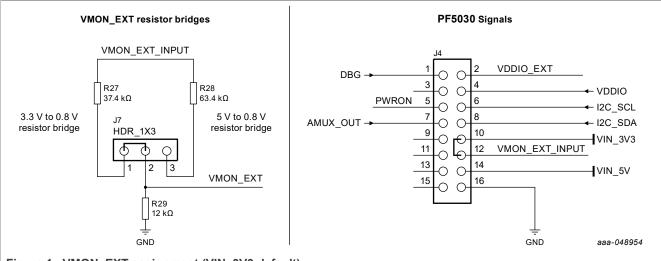
4.3 Schematic, board layout, and bill of materials

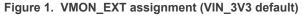
The schematic, board layout, and bill of materials for the KITPF5030SKTEVM board are available at <u>http://www.nxp.com/KITPF5030SKTEVM</u>.

4.3.1 VMON board configuration

The VMON configuration is highly dependent on the use case. This kit is delivered with a default configuration.

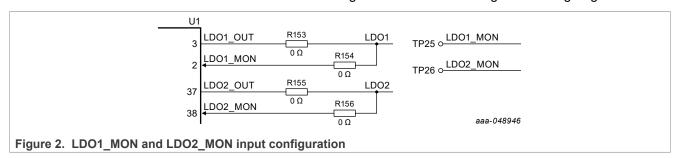
The user can assign VMON_EXT differently to address the use case using J4 and J7 connectors shown in <u>Figure 1</u>. J7 is used to select the VMON_EXT (VMON0) external resistor divider to monitor 3.3 V or 5.0 V. J4 is used to connect the VMON_EXT external resistor divider input VMON_EXT_INPUT to an external voltage, VIN_3V3, or VIN_5V. By default, VMON_EXT is monitoring VIN_3V3.





By default, BUCK2_FB (VMON2) is connected to BUCK2 though R162. However, When BUCK2 is disabled or used in multiphase with BUCK1, BUCK2_FB can be connected to an external voltage. R162 must be removed in this case and the internal DAC must be configured to the voltage monitoring target.

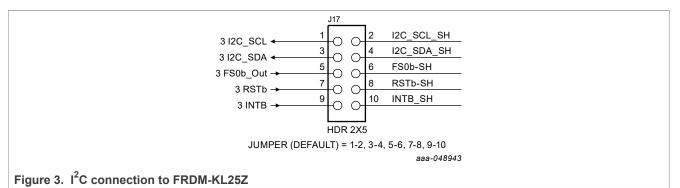
By default, LDO1_MON (VMON4) and LDO2_MON (VMON5) pins are tied to LDO1 and LDO2, respectively. LDO1_MON and LDO2_MON can be used to monitor an external voltage using test points TP25 (LDO1_MON) and TP26 (LDO2_MON), then R154 and/or R156 must be removed. Figure 2 shows the corresponding part of the schematic. The internal resistors dividers can be configured to select the voltage monitoring target.



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4.3.2 I²C

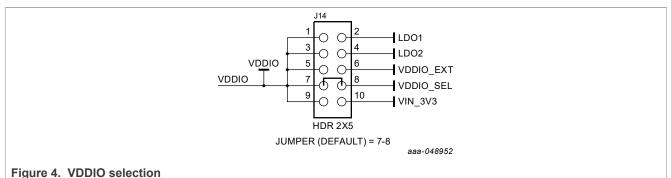
The I²C bus is connected to KL25Z MCU to communicate with NXP GUI. Another MCU can be connected to the I²C bus on J4 connector, but J17 1-2 and 3-4 must be removed to disconnect the FRDM-KL25Z MCU (see Figure 3). In addition to this change, make sure that the VDDIO voltage domain and ground are the same on MCU side and KITPF5030SKTEVM side.



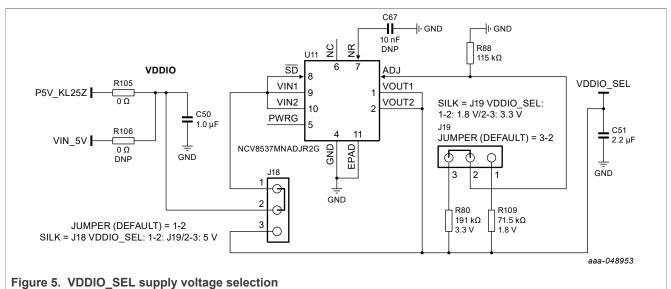
4.3.3 VDDIO

The VDDIO pin is powered through VDDIO net and is used to supply internal buffers and I²C communication.

The selection of VDDIO is made using J14 connector as shown in <u>Figure 4</u>. By default, an external LDO is provided to feed VDDIO through the VDDIO_SEL net.



The I²C is compatible with 1.8 V, 3.3 V, and 5.0 V, therefore VDDIO_SEL voltage is configurable between 1.8 V, 3.3 V, or 5.0 V using J18 and J19 connectors (3.3 V by default) shown in <u>Figure 5</u>.



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4.4 Kit featured components

Figure 6 identifies important components and Table 1 provides details.

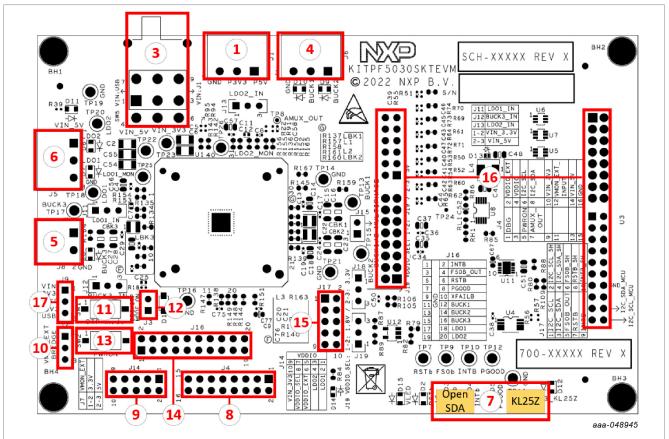


Figure 6. Evaluation board featured components location

Table 1	Evaluation	board	featured	components	location
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Number	Description		
1	VIN_5V and VIN_3V3 power supply input		
3	VIN three position switch		
	Left position: VIN from USB		
	Middle position: board not supplied		
	Right position: VIN from J1		
4	BUCK1/2 regulators output		
5	BUCK3 regulator output		
6	LDO1/2 regulators output		
7	USB connectors (OpenSDA for MCU flash; KL25Z for NXP GUI control)		
8	Debug connectivity. Access to PF5030 signals		
9	VDDIO selection		
10	VMON_EXT resistor bridge configuration (choice between monitoring 3.3 V or 5.0 V)		
11	OTP mode switch		
12	DBG pin to ground if unplugged		

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Number	Description	
13	PWRON pin switch	
14	Signal debug connector	
15	FRDM-KL25Z board signals connection	
16	FRDM-KL25Z board connectors	
17	VLED supply configuration	

Table 1. Evaluation board featured components location...continued

4.4.1 Connectors

Figure 7 shows the location of connectors on the board.

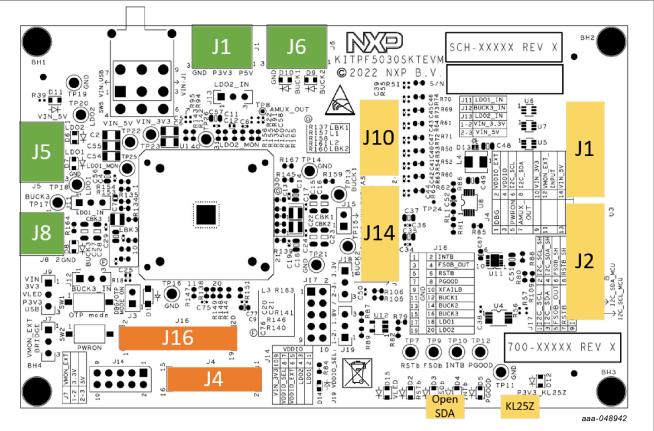


Figure 7. Evaluation board connectors location

4.4.1.1 VIN connector (J1)

Table 2. VIN_5V and VIN_3V3 connector (J1)

Schematic label	Signal name	Description
J1-1	VIN_5V	5 V voltage supply input
J1-2	VIN_3V3	3.3 V voltage supply input
J1-3	GND	Ground

4.4.1.2 Output power supply connectors

Table 3. LDO1/2 connector (J5)

Schematic label	Signal name	Description
J5-1	LDO2	LDO2 regulator output
J5-2	LDO1	LDO1 regulator output
J5-3	GND	Ground

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Table 4. BUCK1/2 connector (J6)

Schematic label	Signal name	Description
J6-1	BUCK2	BUCK2 regulator output
J6-2	BUCK1	BUCK1 regulator output
J6-3	GND	Ground

Table 5. BUCK3 connector (J8)

Schematic label	Signal name	Description
J8-1	BUCK3	BUCK3 regulator output
J8-2	GND	Ground

4.4.1.3 Debug connector (J4)

Fable 6. Debug connector (J4)			
Schematic label	Signal name	Description	
J4-1	n.c.	Not connected	
J4-2	VDDIO_EXT	External VDDIO voltage supply	
J4-3	INTB	Interrupt output pin (active low)	
J4-4	n.c.	Not connected	
J4-5	PWRON	PWRON input pin	
J4-6	I2C_SCL	I ² C serial clock	
J4-7	AMUX_OUT	Analog multiplexer output	
J4-8	I2C_SDA	I ² C serial data	
J4-9	n.c.	Not connected	
J4-10	VIN_3V3	VIN_3V3 voltage supply	
J4-11	n.c.	Not connected	
J4-12	VMON_EXT_INPUT	VMON_EXT voltage divider input	
J4-13	n.c.	Not connected	
J4-14	VIN_5V	VIN_5V voltage supply	
J4-15	n.c.	Not connected	
J4-16	GND	Ground	

4.4.1.4 Voltage monitoring connector (J16)

Table 7. Voltage monitoring connector (J16)

Schematic label	Signal name	Description
J16-1	GND	Ground
J16-2	INTB	Interrupt output pin (active low-logic level)
J16-3	GND	Ground
J16-4	FS0B_out	Fail-safe pin (active low-logic level)

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Schematic label	Signal name	Description
J16-5	GND	Ground
J16-6	RSTB	Reset input / output pin (active low-logic level)
J16-7	GND	Ground
J16-8	PGOOD	Power good output pin
J16-9	GND	Ground
J16-10	XFAILB	Power synchronization input/output with NXP low voltage PMIC
J16-11	GND	Ground
J16-12	BUCK1	BUCK1 regulator output
J16-13	GND	Ground
J16-14	BUCK2	BUCK2 regulator output
J16-15	GND	Ground
J16-16	BUCK3	BUCK3 regulator output
J16-17	GND	Ground
J16-18	LDO1	LDO1 regulator output
J16-19	GND	Ground
J16-20	LDO2	LDO2 regulator output

Table 7. Voltage monitoring connector (J16)...continued

4.4.1.5 FRDM-KL25Z board connectors

Table 8. FRDM-KL25Z safety output connector (J1)

Schematic label	Signal name	Description
J1-1 to J1-9	n.c.	Not connected
J1-6	INTB_MCU	Interruption (active low-logic level)
J1-7	n.c.	Not connected
J1-8	RSTB_MCU	Reset (active low-logic level)
J1-9 to J1-11	n.c.	Not connected
J1-12	FS0b_MCU	Fail-safe (active low-logic level)
J1-13 to J1-16	n.c.	Not connected

Table 9. FRDM-KL25Z I²C connector (J2)

Schematic label	Signal name	Description
J2-1 to J2-13	n.c.	Not connected
J2-14	GND	Ground
J2-15 to J2-17	n.c.	Not connected
J2-18	I2C_SDA_MCU	I ² C serial data line
J2-19	n.c.	Not connected
J2-20	I2C_SCL_MCU	I ² C serial clock line

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Schematic label	Signal name	Description
J10-1	BUCK2_ADC	BUCK2 regulator output to KL25Z ADC
J10-2	DBG_ADC	DBG pin voltage to KL25Z ADC
J10-3	BUCK1_ADC	BUCK1 regulator output to KL25Z ADC
J10-4	AMUX_ADC	AMUX pin to KL25Z ADC
J10-5	BUCK3_ADC	BUCK3 regulator output to KL25Z ADC
J10-6	LDO1_ADC	LDO1 regulator output to KL25Z ADC
J10-7	n.c.	Not connected
J10-8	LDO2_ADC	LDO2 regulator output to KL25Z ADC
J10-9	n.c.	Not connected
J10-10	VIN_ADC	VIN pin voltage to KL25Z ADC
J10-11	n.c.	Not connected
J10-12	VDDIO_ADC	VDDIO pin voltage to KL25Z ADC

Table 10. FRDM-KL25Z ADC connector (J10)

Table 11. FRDM-KL25Z supply connector (J14)

Schematic label	Signal name	Description
J14-1 to J14-3	n.c.	Not connected
J14-4	P3V3_KL25Z	3.3 V generated from KL25Z
J14-5 to J14-7	n.c.	Not connected
J14-8	P3V3_KL25Z	3.3 V generated from KL25Z
J14-9	n.c.	Not connected
J14-10	P5V_KL25Z	5.0 V generated from USB
J14-11	n.c.	Not connected
J14-12	GND	Ground
J14-13	n.c.	Not connected
J14-14	GND	Ground
J14-15	n.c.	Not connected
J14-16	n.c.	Not connected

Table 12. FRDM-KL25Z USB connectors

Schematic label	Signal name	Description
KL25Z	NA	USB connector used to communicate with the PF5030 part
OpenSDA	NA	USB connector used to flash the KL25Z MCU

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4.4.2 Test points

Figure 8 shows test points that provide access to various signals to and from the boards.

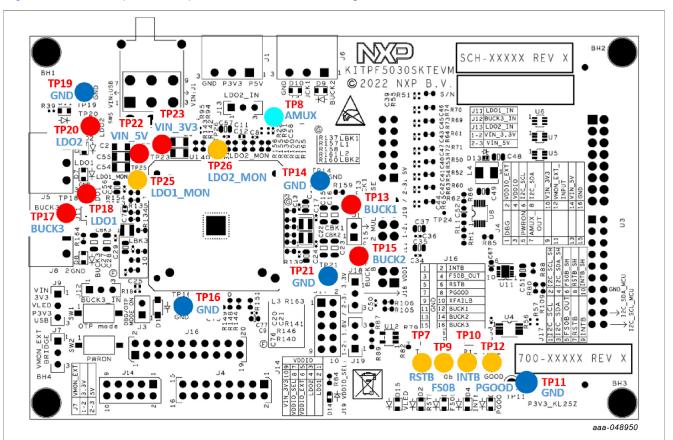


Figure 8. Evaluation board test points

Table 13.	Evaluation	board	test	points	description
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Signal name	Description
RSTB	Reset pin (active low)
AMUX	Analog multiplexer output
FS0B	Fail-safe pin (active low)
INTB	Interruption pin (active low)
PGOOD	Power good pin (active high)
BUCK1	BUCK1 regulator output
BUCK2	BUCK2 regulator output
BUCK3	BUCK3 regulator output
LDO1	LDO1 regulator output
LDO2	LDO2 regulator output
VIN_5V	VIN pin voltage
VIN_3V3	BUCK1/2_IN pin voltage
LDO1_MON	LDO1_MON pin voltage
LDO2_MON	LDO2_MON IN pin voltage
GND	Ground
	RSTB AMUX FS0B INTB PGOOD BUCK1 BUCK2 BUCK3 LD01 LD02 VIN_5V VIN_3V3 LD01_MON LD02_MON

4.4.3 Jumpers

Figure 9 shows jumper locations for board configuration.

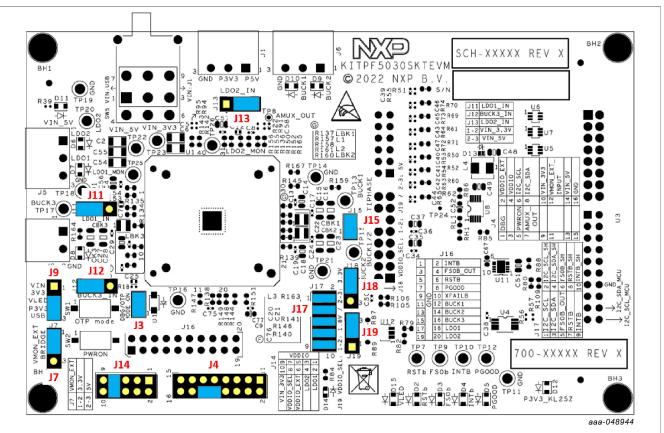


Figure 9	Evaluation board	iumners loca	ation (with de	fault nosition)
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Name	Function	Pin number	Description
J3	Apply voltage to DBG pin	1–2	Either 4.5 V (DBG mode) or 7.95 V (OTP mode). See SW1 position
J4	VMON_EXT input	10-12	VIN_3V3
	selection	12-14	VIN_5V
J7	VLED selection	1-2	VIN_3V3
		2-3	P3V3_KL25Z
J 9	VMON_EXT resistor	1–2	Monitors 3.3 V
	bridge selection	2-3	Monitors 5.0 V
J11	LDO1 input	1-2	LDO1_IN tied to VIN_3V3
		2-3	LDO1_IN tied to VIN_5V
J12	BUCK3 input	1-2	BUCK3_IN tied to VIN_3V3
		2-3	BUCK3_IN tied to VIN_5V
J13	LDO2 input	1-2	LDO2_IN tied to VIN_3V3
		2-3	LDO2_IN tied to VIN_5V

Table 14. E	Evaluation	board	jumpers	description
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Name	Function	Pin number	Description
J14	VDDIO input	1-2	VDDIO tied to LDO1
		3-4	VDDIO tied to LDO2
		5-6	VDDIO tied to VDDIO_EXT
		7-8	VDDIO tied to VDDIO_SEL
		9-10	VDDIO tied to VIN_3V3
J15	BUCK1/2 multiphase	1-2	BUCK2 tied to BUCK1
J17	I ² C and safety IOs	1-2	I ² C SCL
	connection to FRDM- KL25Z	3-4	I ² C SDA
		5-6	FS0B_out
		7-8	RSTB
		9-10	INTB
J18	VDDIO_SEL selection A	1-2	See J19
		2-3	VDDIO_SEL voltage @ 5.0 V
J19	VDDIO_SEL selection B	1-2	VDDIO_SEL voltage @ 1.8 V
		2-3	VDDIO_SEL voltage @ 3.3 V

Table 14. Evaluation board jumpers description...continued

4.4.4 LED signaling

Figure 10 shows the LEDs provided as visual output devices for the evaluation board:

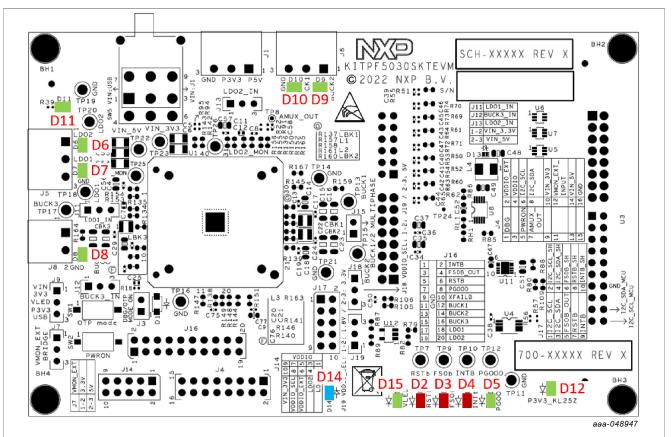


Figure 10. Evaluation board LED signaling location

Label	Name	Color	Description
D2	RSTB	Red	RSTB asserted (low-logic level)
D3	FS0B	Red	FS0B asserted (low-logic level)
D4	INTB	Red	INTB asserted (low-logic level)
D5	PGOOD	Green	PGOOD released
D6	LDO2	Green	LDO2 ON
D7	LDO1	Green	LDO1 ON
D8	BUCK3	Green	BUCK3 ON
D9	BUCK2	Green	BUCK2 ON
D10	BUCK1	Green	BUCK1 ON
D11	VIN_5V	Green	VIN_5V ON
D12	P3V3_KL25Z	Green	P3V3_KL25Z ON
D14	DBG ≥ 7.85 V	Blue	DBG pin voltage ≥ 7.85 V (OTP programming)
D15	VLED	Green	VLED ON

Table 15	Evoluction	board I ED	aignaling	description
Table 15.	Evaluation	board LED	signaling	description

4.4.5 Switches

Figure 11 and Figure 12 show switches locations for board operation.

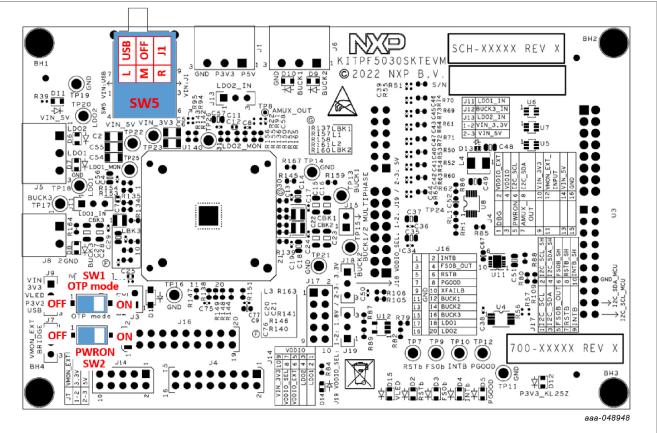


Figure 11. Switches location top

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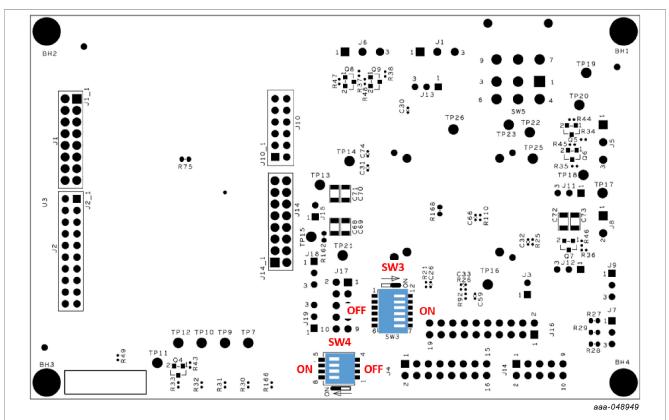


Figure 12. Switches location bottom

Table 16. SW1 description

Position	Function	Description
RIGHT	OTP mode ON	PF5030 OTP can be emulated and programmed when J3 populated
LEFT	OTP mode OFF	PF5030 OTP cannot be emulated and programmed

Table 17. SW2 description

Position	Function	Description
RIGHT	PWRON pin high	PF5030 can power up
LEFT	PWRON pin low	PF5030 cannot power up

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Table 18. SW3 description

Switch number	Line	LED	Description
1	VIN_5V	D11	
2	BUCK1	D10	
3	BUCK2	D9	Each LED is connected through an independent switch. Disconnecting them allows more accurate efficiency measurement.
4	BUCK3	D8	The switches also disconnect the FRDM-KL25Z ADC inputs.
5	LDO1	D7	
6	LDO2	D6	

Table 19. SW4 description

Switch number	Line	LED	Description
1	PGOOD	D5	Each LED is connected through an independent switch.
2	INTB	D4	Disconnecting them allows more accurate efficiency measurement.
3	FS0B	D3	The switches also disconnect the level shifters to the FRDM-KL25Z
4	RSTB	D2	inputs.

Table 20. SW5 description

Position	Function	Description
RIGHT	VIN ON	PF5030 supplied from USB
MIDDLE	VIN OFF	PF5030 not supplied
LEFT	VIN ON	PF5030 supplied from J1

5 Installing and configuring software and tools

The programming/evaluation boards are always delivered with the GUI firmware already flashed. If MCU firmware is already flashed, ignore this section. If it is specified that firmware must be updated or it is malfunctioning, follow these instructions.

5.1 Flashing or updating the FRDM-KL25Z GUI firmware

If bootloader is already loaded in the FRDM-KL25Z board, steps 1-3 are not required. Start from step 4.

1. Disable the Storage Service and Windows Search: Run Services, double click, and stop them as shown in <u>Figure 13</u>.

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ces (Local)	Services (Local)						Services (Local)	Services (Local)					
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		Shell Hardware Detection	Provides no	Running	Automatic	Loc			Windows Push Notification	This service	Running	Automatic	Loc
	Description:	Smart Card	Manages ac	Running	Automatic (T	Loc		Description:	🖓 Windows Remote Manage	Windows R		Manual	Net
	Provides enabling services for storage settings and external storage	Smart Card Device Enumera	Creates soft		Manual (Trig	Loc		Provides content indexing, property caching, and search results for files, e-	Windows Search	Provides co	Running	Automatic (D	. Loc
	expansion	Smart Card Removal Policy	Allows the s		Manual	Loc		mail, and other content.	S Windows Time	Maintains d	Running	Manual (Trig	Loc
		SMS Agent Host	Provides ch	Running	Automatic (D	Loc			Windows Update	Enables the	Running	Manual (Trig	Los
		SNMP Trap	Receives tra		Manual	Loc			WinHTTP Web Proxy Auto	WinHTTP i	Running	Automatic	Lo
		Snow Inventory Client	This is the S	Running	Automatic	Loc			Wired AutoConfig	The Wired	Running	Automatic	Loc
		Software Protection	Enables the	Running	Automatic (D	Net			WLAN AutoConfig	The WLANS	Running	Automatic	Loc
		Spot Verifier	Verifies pote		Manual (Trig	Loc			Sector WMI Performance Adapter	Provides pe		Manual	Loc
		SSDP Discovery	Discovers n		Disabled	Loc			Sector Contens	This service		Manual	Lo
		State Repository Service	Provides re	Running	Manual	Loc			Q Workstation	Creates and	Running	Automatic	Ne
		Still Image Acquisition Events			Manual	Loc			WWAN AutoConfig	This service		Manual	Lo
			Provides en	Running	Manual (Trig	Loc				This service		Manual	Loc
			Optimizes t		Manual	Loc			Abox Game Monitoring	This service		Manual (Trig	Loc
			Maintains a	Running	Automatic	Loc			A Xbox Live Auth Manager	Provides au		Manual	Loc
		Symantec Endpoint Protecti		Running	Automatic	Loc			Abox Live Game Save	This service		Manual (Trig	
			Checks that		Manual	Loc			Xbox Live Networking Service	This service		Manual	Loc
		Sync Host_15c8b4	This service	Running	Automatic (D	Loc Y			<			_	>
	Extended Standard	•				<u> </u>		Extended Standard					
-													_

Figure 13. Services configuration

- 2. Press the RST push button and connect the USB cable to the SDA port on the FRDM-KL25Z board.
 A new "bootloader" device appears on the left pane of the file explorer
- 3. Drag and drop the file "MSD-DEBUG-FRDM-KL25Z_Pemicro_v118.SDA" to the bootloader drive Ensure that there is enough time for the firmware to be saved in the bootloader
- 4. Disconnect the USB cable, then reconnect it to the SDA port **WITHOUT** pressing the RST push button
 - This time, FRDM_KL25Z device appears on the left pane of the file explorer as in Figure 14.

	 ▲ Computer ▷ ▲ Local Disk (C:) ▷ □ Local Disk (D:) ▷ □ Local Disk (E:) 	
Figure 14. FRDM-KL25Z in left pane	FRDM-KL25Z (G:) aaa-044227	

5. Locate the file "nxp-gui-fw-frdmkl25z-usb_hid-device_<version>.bin" from the package. Drag and drop this file into the FRDM_KL25Z device.

Ensure that there is enough time for the firmware to be saved.

6. Freedom board firmware is successfully loaded. Disconnect the USB-cable and reconnect it to the KL25Z USB port.

5.2 Installing NXP GUI software package

To install the "NXP GUI for Automotive PMIC Families" or obtain the NXP GUI package, unzip an open "1 - NXP_GUI_Setup" folder as shown in Figure 15.

Name	e	Status	Date modified	Туре	Size
0	- Documentation	\odot	6/8/2020 10:57 AM	File folder	
<mark></mark> 1	- NXP_GUI_Setup	g	6/8/2020 5:26 PM	File folder	
2	- KL25Z_FW	\odot	6/4/2020 1:42 PM	File folder	
L L	ICENSE.txt	\odot	6/4/2020 11:14 AM	Text Document	3 KB
					aaa-044228
Figure 15. NXP_GU	JI_Setup folder				

Then double click on the "NXP_GUI-version-Setup.exe" shown in Figure 16 and follow the instructions.

Name	Status	Date modified	Туре	Size
궁 NXP_GUI-3.1.45-Setup.exe	S	6/6/2020 6:55 PM	Application	64,336 KB
				aaa-044229
Figure 16. NXP_GUI_version_Setup.exe				

To install the application on Windows PC, proceed with the pop-up windows shown in Figure 17 and Figure 18.

Welcome	e to NXP_GUI 3.1.45 Setup	License Agreement Please review the license terms before installing NXP_GUI 3.1.45.
3.1.45. It is recommer before startin	e you through the installation of NXP_GUI nded that you close all other applications g Setup. This will make it possible to update m files without having to reboot your	Press Page Down to see the rest of the agreement. /* Copyright 2019 TESSOLVE * All rights reserved.
Click Next to c	ontinue.	 Redistribution and use in source and binary forms, with or without modification, are permitted provided that the following conditions are met: Redistributions of source code must retain the above copyright notice, this list of conditions and the following disclaimer. If you accept the terms of the agreement, click I Agree to continue. You must accept the agreement to install NXP_GUI 3.1.45.
	Next > Cancel	Nullsoft Install System v3.05

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Choose Components Choose which features of NXP_	GUI 3.1.45 you want to install.			Choose Install Location Choose the folder in which to instal NXP_GUI 3, 1, 45.	(
Check the components you war install. Click Next to continue.	nt to install and uncheck the com	oonents you don't want	: to	Setup will install NXP_GUI 3.1.45 in the following folder. To install in a dif Browse and select another folder. Click Install to start the installation.	ferent folder, dick
Select components to install:	MainSection Optional	Description Position your mouse over a component to see its description.		Destination Folder	Browse
Space required: 164.4 MB				Space required: 164.4 MB Space available: 26.9 GB	
ullsoft Install System v3.05				Nullsoft Install System v3.05	
	< Back	Next > Ca	ancel	< Back Insta	all Cancel

Figure 18. NXP GUI setup 2/2

Select the options shown in <u>Figure 19</u> before completing the installation of the setup:

- Run NXP_GUI
- Show Readme

WXP_GUI 3.1.45 Setup	Completing NXP_GUI 3.1.45 Setup	
	NXP_GUI 3.1.45 has been installed on your computer. Click Finish to close Setup.	
	Run NXP_GUI 3.1.45 Show Readme	
	< Back Finish Cancel	
	aaa-044232	
9. NXP GUI setup completion		

Select Finish to complete the installation.

When installation is finished, you can search the application on the Windows search bar as "NXPGUI". Click to launch.

Figure

6 Using PF5030 NXP GUI

To follow the steps in this section, ensure that the board is connected using the appropriate hardware configuration.

Always use the latest version of the NXP GUI.

6.1 Starting the PF5030 NXP GUI

When your kit is ready and the NXP GUI is installed, click to launch the GUI from your Windows search bar. When the kit selection window appears, as shown in Figure 20, select PF5030.

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Figure 20. Kit selection window

To avoid the kit selection window on every launch, you can check the box "Use this configuration and do not ask again". The window shown in <u>Figure 21</u> opens.

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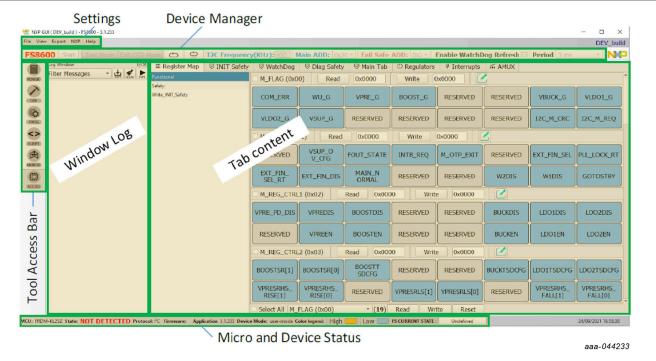


Figure 21. NXP GUI framework

You are now using the PF5030 GUI interface. It can be divided in several parts:

- Settings: Import or export files, configure framework.
- Device Manager: Start communication with device. Enter or exit test mode. I²C communication settings.
- Tool Access Bar: Quick access to the PF5030 evaluation tools and features.
- Window Log: Microcontroller and device communication events.
- Tab Content: Content of each tool or tab. There can be more tabs, boxes, or windows.
- **Micro and Device Status:** Indicates if the computer USB is connected to the kit. Displays firmware and GUI version. Displays the current state of the fail-safe state machine. Click Display button to refresh.

Note: The tool access bar shows the GUI tools in the sequence that they must be used. The first step is to verify device POWER dissipation and then configure the OTP. When the power is verified and OTP is done, the device can be programmed or emulated with a SCRIPT. MIRROR registers can be read/modified to a configuration validation. To verify states and configure safety reactions, the Access tab allows registers handling.

6.2 Power tab

The POWER tool allows the calculation of power management power dissipation.

User must start by setting or importing an OTP configuration to preset all regulators, then entering the current consumption of each rail.

As PF5030 can be supplied by more than one voltage rail, two input supply rails can be set on "INPUT PARAMETERS" group. Once the voltages are set, each regulator must be associated to one of those rails. The voltages set are used to calculate the power dissipation. The calculated absorbed input currents are assigned to the associated rail.

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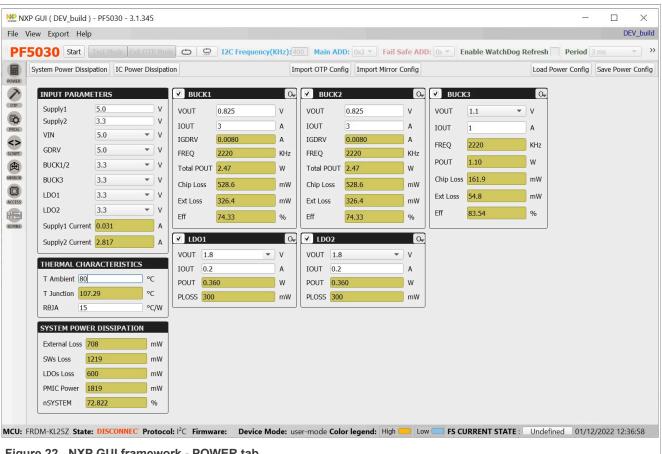


Figure 22. NXP GUI framework - POWER tab

Each regulator can be enabled / disabled by clicking on the upper left corner check box.

Additional options are available on the menu on the upper right corner of each regulation, such as:

- Operation mode: Single or multiphase, regulator or load switch
- **Component selection**: input / output capacitors, inductor and DCR. DCR is automatically changed based on inductor value and can be reedited
- · Advanced parameters: detailed losses summary
- Efficiency chart: regulator losses / output current plot at current junction temperature
- · Power chart: regulator losses partition

6.3 OTP tab

The OTP tool allows the configuration of OTP registers and generates scripts for OTP emulation or OTP programming. These scripts program parameters that the main state machine and the fail-safe state machine control.

At the right side, fill **Customer Details** and **Program Details** sub-windows. Set **Device Core ID** and **Device Type** for device pre-configuration.

The OTP tool includes the following tabs:

- System Configuration
- Switching and LDO Regulators
- Functional Safety

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These tabs are used to define the entire PF5030 OTP configuration.

When the OTP configuration is defined, TBB/OTP scripts can be generated using the Export menu. Generate a TBB file for emulation and an OTP file for OTP programming.

It is possible to save a configuration to use or modify it later. To export the OTP configuration, click "Save Config". To import a configuration initially saved from the OTP tool or the Mirrors tab, click the Import button.

6.3.1 System configuration tab

The system configuration tab has several sections, divided into two groups. The first group is related to OTP configuration itself:

- System Configuration: I²C addresses, VIN threshold, program ID, fault retry management, regulator assignment
- Clock and Synchronization: Clock modulation, XFAILB synchronization
- VMON OV Deep Fail-safe Reaction: configures device reaction when OV event is detected.
- **Power Sequence Configuration**: This box is used to define the power sequence of the device and device reaction when TSD happens. If the configuration is modified, the power-up sequence graph is updated automatically.

Figure 23 shows an OTP configuration example.

	System Configuration			Clock and Synchronisation		1			Power Sequence Con			1		
IZCDEVADDR	0.20	• 0000	CLK_DIV1	2.22 MHz	10	Regulator	Sequence	EN	Phase Delay	Cloc	k Soft start	TSE	Behavior	r ,
12CDEVID	0/21	▼ 0000	CLK_DTV2	455 KHz	100	VPRE	OFF dy 250 µs	*	Not delayed	♥ CLK2	▼ 2 mV/µs	•		
BAT_SC_EN	Enabled	▼ 1	MOD_EN	Disable clock modulation	0	Boost	Slot 0	- V	Delayed by 1 Clock Cycle	▼ CLK1	-	Shutdow	+ DFS	*
TBAT_SC_CFG	1 ms	v 0	MOD_CONF	Triangular modulation -	0	Buck	Slot 1	- V	Delayed by 2 Clock Cycles	▼ CLK1	 10.41 mV/μs 	* Shutdow	+ DFS	
NoMCU	Application with MCU	v 0	PLL_SEL	Disabled	0	LDO1	Slot 2	*				Shutdow	+ DFS	*
VSUPCEG	Automotive application(3.3V < VPRE < 4.5V)	v 0	FOUT_SLOT_EN	FOUT slot assignment disabled	0	LDO2	Slot 3	*				Shutdow	+ DFS	
PWRDWN_DFS	Transition to DFS with power down sequence	▼ 1	FOUTS	Do not drive FOUT low	1111			t Time	Power-Up Last Slot		down First Slot			-
AUTORETRY_EN	Enabled	▼ 1	XFAIL8_CFG	No synchronization	00	Slo	t Config 1 ms			ower down st		-		
AUTORETRY_INFINITE	Endless	▼ 1	XFAILBS	Do not wait for XFAILB release	1111									
VMON0_REG_ASSIGN	External regulator (No action if OV)	• 000	XFAILB_PWD_CFG	No Power down	0									
	External regulator (No action if OV)	▼ 000												
VMON1_REG_ASSIGN														
	External regulator (No action if OV)	▼ 000												

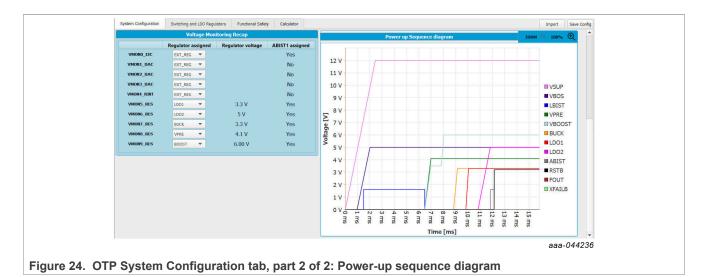
Figure 23. OTP System Configuration Tab, part 1 of 2: OTP configuration

The second group is related to VMON board connection and startup sequence diagram:

- Voltage monitoring recap for power-up sequence diagram drawing: This box is NOT related to the OTP configuration. It allows the definition of an assignment between the VMONx and the regulators to plot the power-up sequence graph. It does not configure any registers. It is only used as information. It is saved as comment on the configuration script.
- Power-up sequence diagram: This diagram reflects the power-up sequence of the PF5030 depending on the OTP configuration. To plot the associated configuration, it uses the "Voltage Monitoring Recap". The powerup sequence timing may not be 100 % accurate. If shown, the RSTB, the FOUT, and the XFAILB voltages are different from 3.3 V to differentiate between the different curves.

Figure 24 shows a voltage monitoring recap connection and the resulting power-up sequence diagram.

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6.3.2 Switching and LDO regulators tab

The switching and LDO Regulators tab shown in Figure 25 has several sections:

- Block diagram: Summarizes the output voltage and startup slot of each regulator
- SMPSs configuration: Switching Mode Power Supplies configuration.
- LDOs configuration: Linear dropout regulators configuration

Block Diagram	VPRE Configuration	BOOST Configuration	BUCK Configuration	LDO1 Configuration	LDO2 Configuration
FSSG3 ASL-0 VRE	VPRETON 60 ns 01 VPREV 4.1 V • 01111 VPRESC 52 mV/µs • 000101 VPRELIN 100 mV 11 VPRESC 80 ns 00 VPRESRIS PU/PD/900 mA 11 VPRESRIS PU/PD/130 mA 00	$\begin{array}{c c c c c c c c c c c c c c c c c c c $	$\begin{array}{c c c c c c c c c c c c c c c c c c c $	LDOIV 3.3 V • 1011 LDO1_SW_EN Disabled • 0	LDO2V 5V 11 LDO2ILIM 150 mA 1

Figure 25. OTP SMPS and LDO regulators Configuration tab

6.3.3 Functional safety tab

The functional safety tab shown in Figure 26 has several sections:

- System Safety Configuration: Watchdog, RSTB, PGOOD, safety path, SVS clamp
- **Voltage Monitoring**: Define the voltage monitoring configuration. Some protections have been implemented to avoid OTP configuration issue.

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	System Safety Configuration							Voltage Mo	n itoring				
RRMON_EN	Disabled	~ 0		EN	Voltage		UV TH	OV TH	UV Debound	e OV Debour	ce PGOOD Ctrl	ABIST1 Assi	gnment
CCU_EN	Disabled	- 0	VMON0_I2C	V	3.3 V	*	90.0% *	110.0% *	25 µs 🔹	25 µs	 Assigned 	 Assigned 	*
WD_DIS	Watchdog monitoring enabled	~ 0	VMON1_DAC		1.4 V	*	90.0% -	110.0% -	25 µs 🔹	25 µs	 Not assigned 	 Not assign 	ned 🔹
WD_SELECTION	Challenger watchdog	* 1	VMON2_DAC		0.7 V	*	90.0% *	110.0% *	25 µs 🔹	25 µs	 Not assigned 	 Not assign 	ned *
LT_RECOVERY_EN	Disabled	- 0	VMON3_DAC		0.7 V	-	90.0% *	110.0% -	25 µs 🔹	25 µs	 Not assigned 	 Not assign 	ned 🔹
RSTB_8s_DIS	Counter enabled	- 0	VMON4_RINT		1.8 V	*	90.0% *	110.0% *	25 µs 🔹	25 µs	 Not assigned 	 Not assign 	ned 🔹
RSTB DLY	No delay	- 0	VMON5_RES	V	0.8 V		90.0% -	110.0% -	25 µs 🔹	25 µs	 Assigned 	 Assigned 	*
STB2PGOOD	Fault asserting RSTb won't asser	t PGOOD - 0	VMON6_RES	V	0.8 V		90.0% -	110.0% -	25 µs 🔹	25 µs	 Assigned 	 Assigned 	-
MON123 SVS CLAMP	9	• 00000	VMON7_RES	~	0.8 V		90.0% -	110.0% -	25 µs 🔹	25 µs	 Assigned 	 Assigned 	-
1101125_5V5_CEAH	10 303	00000	VMON8_RES	~	0.8 V		90.0% *	110.0% -	25 µs 🔹	25 µs	 Assigned 	 Assigned 	*
			VMON9_RES	V	0.8 V		90.0% *	110.0% -	25 µs 🔹	25 µs	 Assigned 	 Assigned 	*

Figure 26. OTP Functional Safety tab

6.4 Establishing the connection between the NXP GUI and the hardware

The device manager allows the connection of the PF5030 development board with the NXP GUI.

Before plugging the KL25Z USB port to the computer, the MCU is in a "NOT DETECTED" state.

MCU: FRDM-KL25Z State: NOT DETECTED	Protocol: I ² C Firmware:	Application 3.1.140 Device Mode: user-mode
		aaa-0442:

After plugging in the USB, the MCU state changes to "DISCONNECTED." If the state does not change, press the RST button on the freedom board.

At this state, the communication with the MCU can be started.

MCU: FRDM-KL25Z State: CONNECTED Protocol: I²C Firmware: 0.3 Application 3.1.140 Device Mode: user-mode aaa-044255

The MCU state changes to "CONNECTED" and the firmware version is displayed.

To start the communication with the PF5030, click the "Start" button. The GUI is able to identify the device address to establish the communication.



When the communication has started successfully, the PF5030 (device name) switches to green.

FS8600	Stop	Test Mode	Exit OTP Mode	G	C	I2C Frequency(KHz): 400	Main ADD:	0x20 -	Fail Safe ADD:	0x2 *
									aaa	-044258

When the device starts with the DBG pin voltage at 7.95 V (EVB OTP mode LED on), the state machine stops at the Main/FS OTP MODE state.

The current mode can be read using the refresh button and loop refresh button highlighted in red. Clicking refresh reads the state one time. Clicking the loop refresh latches and reads the state periodically until a new click deactivates it.

When the "Exit OTP mode" button is green, the device is in OTP mode. When in OTP mode, device I²C register addresses are the default values 0x20 for main and 0x21 for fail-safe. An "Exit OTP mode" button click sends

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commands to the main state and the fail-safe state machine to exit OTP mode and initiate device start-up. The addresses are automatically updated to keep device communication.



Test mode can be enabled and disabled by clicking the Test Mode button when DBG pin voltage is 7.95 V (EVB OTP mode LED on). When the button is green, Test mode is activated. The button state can also be refreshed by clicking the arrow loop buttons.

▼ Fail Safe ADD: 0x2 ▼	Main ADD: 0x20 -	I2C Frequency(KHz): 400	Ð	Exit OTP Mode	Test Mode	Stop	FS8600
aaa-044260				_			

Figure 27. GUI and device in test mode

The current device mode (user / test) is shown on the device status bar.

Test mode can be entered when device is not in OTP mode.

When in OTP mode, the device is necessarily in Debug mode.

6.5 OTP mode and device programming

Device enters OTP mode when the DBG pin voltage is set to 7.95 V before start-up. The OTP mode consists of a device state machine stop at Main/FS OTP MODE states. When in Main/FS OTP mode states, the I²C addresses are 0x20 for main and 0x21 for fail-safe. The Main/FS OTP mode states are left when one of these conditions is met:

- Imposing DBG pin voltage inferior to 5.5 V
- Sending Main/FS OTP mode exit command through I²C
- Clicking NXP GUI button "Exit OTP Mode"

The NXP GUI is able to identify these addresses automatically from the device.

Then, the device addresses are set based on the mirror registers values. User can only change these addresses in the mirror register in Test mode.

6.5.1 Device programming

The Device Programming tab shown in <u>Figure 28</u> allows OTP device programming using a file initially generated by the OTP tool. This tab is only available when **Test mode** is active.

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Device Programming Conf Select TBB/OTP File Bro File Name Not Select Status Not Ready Program Reset	wse ed		OTP Mode FS OTP Mode Exit FS OTP Mode RT Main OTP Mode Exit Main OTP Mode RT Read Write
	Fuse E	lox Status	
Main Programming Status BUSY ERROR ONE_ERR TWO_ERR MAX_PGM_EXCEED VRR_CHECK_TRIES PGM_FAIL_WP BOOT_ERROR VRR_ERROR BOOT_DONE	Main Sector Flags Sector 1 Flags CRC Image: CRC BOOT Enable(BE) Image: CRC Sector 1 bis Flags CRC Image: CRC BOOT Enable(BE) Image: CRC Write Protected(WP) Image: CRC Write Protected(WP) Image: CRC MTP Image: CRC Image: CRC Image: CRC BOOT Enable(BE) Image: CRC Write Protected(WP) Image: CRC MTP Image: CRC	FailSafe Programming S BUSY ERROR ONE_ERR TWO_ERR MAX_PGM_EXCEED VRR_CHECK_TRIES PGM_FAIL_WP BOOT_ERROR VRR_ERROR BOOT_DONE	FailSafe Sector Flags Sector 1 Flags CRC Image: CRC BOOT Enable(BE) Image: CRC Write Protected(WP) Image: CRC Sector 1bis Flags CRC CRC Image: CRC BOOT Enable(BE) Image: CRC Write Protected(WP) Image: CRC Write Protected(WP) Image: CRC MTP Image: CRC BOOT Enable(BE) Image: CRC Write Protected(WP) Image: CRC MTP Image: CRC MTP Image: CRC MTP Image: CRC MTP Image: CRC
		Read	
			aaa-044261

To set up the hardware before OTP burning, see <u>Section 7.3</u> configure put device in OTP mode, then follow the steps:

- Start the device in **OTP mode**.
- Enter Test mode.
- Browse and load the script file you want to burn (OTP or TBB type).
- The program button is available.
- Click Program.

Before programming, the GUI verifies if the DBG pin voltage is 7.95 V.

If the DBG pin voltage is less than 7.95 V, a pop-up window is shown requiring to turn on the 7.95 V. The blue LED on the board indicates that an 7.95 V voltage is available on the DBG pin. At the end of the first OTP programming, the MTP index = 1, WP, BE, and CRC flags are orange.

The Main/Fail-safe sector flags provide the OTP fuse status, as shown in <u>Table 21</u>. It helps to determine how many times the part was burned.

 Table 21. OTP burning flag status

OTP burning step	Sector	BE	WP	CRC	MTP index
mirrors empty, OTP not burned	1	blue	blue	blue	orange
	1bis	blue	blue	blue	blue
mirrors filled, OTP not burned	1	blue	blue	orange	orange
	1bis	blue	blue	orange	blue
OTP burned once	1	orange	orange	orange	orange
OTP burned twice	1bis	orange	orange	orange	orange

The example shown in Figure 28 corresponds to the OTP not burned, mirrors empty line in Table 21.

To check if a valid OTP configuration is already burned, switch off the supply and then on again. Start the device by clicking the "Exit OTP Mode" button. The device starts with the OTP configuration.

6.6 User mode controls

The device operation is called **User mode** when the Main/FS state machines are not in OTP MODE state and not in Test Mode. In this mode, the main/fail-safe addresses come from mirror registers / fused OTP.

When using the EVB, the voltages on device pins can be verified in ACCESS > AMUX > ADC Measurements (see <u>Section 6.6.3.9</u>).

6.6.1 Working with the script editor

The register and OTP emulation can be configured with the script editor shown in <u>Figure 29</u>. The script editor is useful for trying various OTP configurations in OTP mode.

Filter Messages	Device FS8600		Script Commands Window		Script Resu	Its Window
 Sent and Received Commands 		Command Script Editor	Script	Text Editor		Script Results
			Managen	nent Commands		
				La ?		
	and the first of the second se	1 222 Denies Mader Lat. made Cales Inco	et High 🛑 Low 🛑 FS CURRE	NT STATE: OTP_MODE		24/09/2021 16:

Figure 29. Script editor

The main subareas of this panel are:

- Command Script Editor: Builds commands to be sent to the device.
- Script Text Editor: Sends a sequence of register configurations from a text file or from a command edited directly in this area.
- Script Results: Displays result status of each command sent to the device.
- Sent and Received Commands: Displays a summary of commands sent and received from the device.
- Management Commands: Used for scripts.

6.6.1.1 Command script editor

Using the script editor, you can execute any command either directly or from a file. It is also possible to save and modify a script. Using the brush symbol, it is possible to clean windows if necessary.

All commands must follow a specific syntax. The Help menu describes the commands available in the script editor and the syntax to be used.

Figure <u>30</u> shows an example of building a command from the panel.

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Instrumentation Ist parameters 2nd parameters 3rd parameters 4th parameters Sth parameters SET_REG Device Reg. set Reg. name / Reg. address Reg. value - - GET_REG Device Reg. set Reg. name / Reg. address - - - SET_DPIN_PinName Device Dig. pin value - - - - GET_DPIN_PinName Device - - - - - - GET_APIN_PinName Device -	This help page describes commands List of commands SET_REG : sets value of a selected	d register.	or and their format.			
Interview Ist parameters Interview Interview<	READ_REG : reads value of a select SET_DPIN_PinName : sets value GET_DPIN_PinName : gets value GET_APIN_PinName : gets value	cted register. of a selected digital pin. of a selected digital pin. of a selected analog pin.	Returned value is in mV. Jevice.			
Commands 1st parameter 2nd parameter 3rd parameter 4th parameter 5th parameter SET_REG Device Reg. set Reg. name / Reg. address Reg. value - GET_REG Device Reg. set Reg. name / Reg. address - - SET_DPIN_PinName Device Dig. pin value - - - GET_APIN_PinName Device . - - - GET_APIN_PinName Device - - - - GET_APIN_PinName Device - - - - Device - - - - - CetT_APIN_PinName Device - - - - Device device mode address in device address in device address registers which have similar function. Reg. address: register address in device device mode address registers which have similar function. Reg. address: register address in device dotabatelet. Op. pin value: wold on device dotabatelet. Op. pin value: wold on device mode. - Reg. address: register address in device dotadatelet. O	Command format					
SET_REG Device Reg. set Reg. name / Reg. address Reg. value - GET_REG Device Reg. set Reg. name / Reg. address - - - GET_REG Device Reg. set Reg. name / Reg. address - - - SET_DPIN_PinName Device Dig. pin value - - - - GET_APIN_PinName Device - - - - - - GET_APIN_PinName Device - <t< th=""><th>The following table describes comm</th><th>and parameters. All param</th><th>aters are mandatory.</th><th></th><th></th><th></th></t<>	The following table describes comm	and parameters. All param	aters are mandatory.			
GET_REG Device Reg. set Reg. name / Reg. address - - SET_DPIN_PinName Device Dig. pin value - - - GET_DPIN_PinName Device Dig. pin value - - - GET_APIN_PinName Device - - - - GET_APIN_PinName Device - - - - GET_APIN_PinName Device - - - - Description of command parameters mentioned in the table above: Device: - - - Device: device name (alias used in application). Reg. set: register set name. Register adeaeanse. Textpoint to x prefx) format. Reg. address: You y	Commands	1st parameter	2nd parameter	3rd parameter	4th parameter	5th parameter
SET_DPIN_PinName Device Dig. pin value - - - GET_DPIN_PinName Device - - - - - GET_DPIN_PinName Device - - - - - GET_APIN_PinName Device - - - - - GET_APIN_PinName Device - - - - - Description of command parameters mentioned in the table above: Device device name (also used in application). - - - - Description of command parameters mentioned in the table above: Device device name (also used in application). - Device device databatet. <th>SET_REG</th> <th>Device</th> <th>Reg. set</th> <th>Reg. name / Reg. address</th> <th>Reg. value</th> <td>~</td>	SET_REG	Device	Reg. set	Reg. name / Reg. address	Reg. value	~
GET_DPJIH_PinName Device - - - - GET_APIN_PinName Device - - - - - GET_APIN_PinName Device - - - - - - Description of command parameters mentioned in the table above: - - - - - - - Descreptor of command parameters mentioned in the table above: - <th>GET_REG</th> <th>Device</th> <th>Reg. set</th> <th></th> <th>÷</th> <td>E.</td>	GET_REG	Device	Reg. set		÷	E.
GET_APJIH_PinName Device - - - - GET_APJIH_PinName Device - - - - - Description of command parameters mentioned in the table above: Device: device name (alias used in application). Reg. set: register sets allows to associate registers which have similar function. Reg. address:register address in dectand or hexadecmal (with 0x prefix) format. Reg. address:register address in dectand or hexadecmal (with 0x prefix) format. Reg. address:register address in dectand or hexadecmal (with 0x prefix) format. Reg. address:register address in dectand or hexadecmal (with 0x prefix) format. Win name: name of digital or noted of address at address in dectand or hexadecmal (with 0x prefix) format. Reg. address:register address in dectand or hexadecmal (with 0x prefix) format. Win name: name of digital or noted of address are bow and high . Hexague: negister address are bow and high . Message: an exage to be digital prix Allowed strings are low and high . Hexague: negister address are bow and high . Wessage: an exage to be digital prix Allowed strings are low and high . Hexague: negister address ad	SET_DPIN_PinName	Device	Dig. pin value	-	÷	H.
Description of command parameters mentioned in the table above: Devices device name (alias used in application), Reg. set: register sets and in application), Reg. anter: register name. Register sets allows to associate registers which have similar function. Reg. address: register address in decimal or hexadecimal (with 0x prefix) format. Reg. address: register address in decimal or hexadecimal (with 0x prefix) format. Reg. address: register address in decimal or hexadecimal (with 0x prefix) format. Reg. address: register value in decimal or hexadecimal (with 0x prefix) format. Reg. address: register value of digital or analog pin as defined in device datasheet. Dip, pin value: value of digital pin, Allowed strings are low and high'. Meessage: a message to be displayed in a dialog. It cannot contain ': character, which is used as delimiter of parameters. Mode: name of a device mode. Script example Note that name of registers, register sets, devices and pins depends on particular device. // Sets the 'M_FLAG' register in the 'functional' register set. SET_REGISPS8001:functional:M_FLAG:W000 // Sets value of the 'FS08_MCU' (digital pin (low/high). GET_DFINFS8001:functional:M_FLAG // Cets value of her 'FS08_MCU' (digital pin (low/high). GET_DFINFS8001:Finctional:M_FLAG:WCU' // Cets value of her 'M_MLAG' caladop pin.	GET_DPIN_PinName	Device	÷	-	ь.	
Device: device name (alias used in application). Reg. set: register set name. Register sets allows to associate registers which have similar function. Reg. anate: register anae. additional or hexadecimal (with 0x prefix) format. Reg. value: register value in decimal or hexadecimal (with 0x prefix) format. Reg. value: register value of digital or analog pin as defined in device datasheet. Dig, pin value: value: of digital or analog pin as defined in device datasheet. Dig, pin value: value: of digital or analog pin as defined in device datasheet. Dig, pin value: value: of digital or analog pin as defined on device datasheet. Dig, pin value: value: of digital or analog pin as defined on device datasheet. Dig, pin value: value: of digital or analog pin as defined on device datasheet. Dig, pin value: value: of digital or analog pin as defined on device datasheet. Script example Note that name of registers, register sets, devices and pins depends on particular device. // Sets the 'M_FLAG' register in the 'functional' register set to value 0x00. SET_ESGF3S8001:functional:M_FLAG: Value: // Sets value of Hew T_FLAG register in the 'functional' register set. GET_ESGF3S8001:functional:M_FLAG (digital pin (digital pin (low/high). GET_DFINF3S8001:Finctional:M_FLAG (digital pin (low/high)	GET_APIN_PinName	Device		~	-	a.
	Device: device name (alias used in Reg. set: register set name. Regis Reg. name: register name and defi Reg. address: register address in Big. pin value: value of digital pri Message: a message to be display Mode: name of a device mode. Script example: Note that name of registers, register // Sets the 'M.F.AG' register in the SET_REG-FSBO01fnrotfonal M.F.IAG' register // Gets value of the 'M.F.IAG' Register in the GET_REG-FSBO01fnrotfonal M.F.IAG' Register // Gets value of the 'M.F.IAG' Register in the	application). ter sets allows to association idential attasheet. .decimal or hexadecimal (with 0) g pin as defined in device a defined in device a dialog. It cannot co er sets, devices and pins d .functional' register set to .ge:0x00 ter in the 'functional' regist 46 bit functional' regist 46 bi	e registers which have similar ith 0x prefix) format. (prefix) format. datasheet. and 'high'. ontain ': character, which is epends on particular device. value 0x00.	used as delimiter of parameters.		

6.6.1.2 Management commands

Some commands are used for formatting the scripts. Figure 31 shows the description of each button.

	NN LOOP Loop Image: State of the state o
	aaa-044265
Figure 31. Script editor commands	
• Run: Runs the script once.	

- Loop: Runs the script continuously in a loop.
- Save: Save the script that is present in the script command window in text file.
- **Open**: Open a saved script from the desired location.
- ATE: Saves the script in ATE format.
- Clear: Clears the script command window.
- Script Editor Help Window: Describes the commands available in script editor and their formats.

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6.6.1.3 Script generator

The script editor allows the user to save script sequence files, as shown in <u>Figure 32</u>. However, a script sequence file is already saved as an example in the script generator. This script is used to release FS0B when the PF5030 is using simple watchdog.

Device FS8600	Script Commands Window	Script Results Window
Device PS8600 Allas PS8600 Digital Pins Analog Pins Registers Mode Control Generator Generator Generator: FS08_RELEASE_SIMPLE_WATCHDO Script Generator	Script Commands Window SET_REG:FS8600:SAFETY:FS_WD_WINDOW_DUR:0x0208 SET_REG:FS8600:SAFETY:FS_WD_ANSWER:0x5A82 SET_REG:FS8600:SAFETY:FS_RD_ANSWER:0x5A82 SET_REG:FS8600:SAFETY:FS_RELEASE_FS08:0x8245	Script Results Window OK : Write Register : FS_WD_WINDOW_DUR : 0xd04 OK : Write Register : FS_WD_NNUR : 0x5ab2 OK : Write Register : FS_WD_ANSWER : 0x5ab2 OK : Write Register : FS_STATES : 0x4000 OK : Write Register : FS_RELEASE_FS0B : 0xb2a5
		± ±
mare: 0.13 Application 3.1.233 Device Mode: test-mode Calor		호 · · · · · · · · · · · · · · · · · · ·

Figure 32. Script generator

6.6.2 Mirrors tab

Test mode must be applied to enable the Mirrors tab. This tab is divided in main and fail-safe mirrors registers, shown in <u>Figure 33</u> and <u>Figure 34</u>, respectively.

The "Read All" / "Write All" buttons can be used to read/write all the mirror registers. The mirrors configuration content can be exported and imported in the OTP tool as OTP configuration to generate TBB/OTP script files.

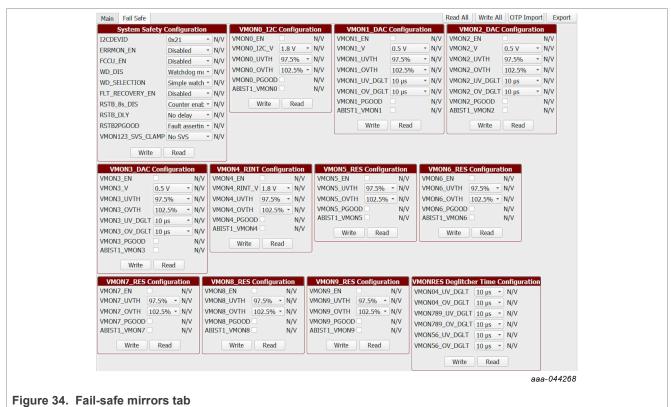
NXP Semiconductors

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	nfiguration		Synchronisation		nce Configuration		Configuration	
I2CDEVADDR	0x20 • N/V	_	2.85 MHz • N/V		0.5 ms • N/V	VPRETON	25 ns	N/\
BAT_SW_EN	Disabled • N/V	CLK_DIV2	2.5 MHz • N/V	BOOSTS	Slot 0 • N/V	VPREV	3.3 V -	N/\
TBAT_SW_CFG	1 ms * N/V	MOD_EN	Disable clock * N/V	BUCKS	Slot 0 • N/V	VPRESSRAMP	1 mV/µs 👻	N/\
VSUPCFG	Automotive a * N/V	MOD_CONF	Triangular m 👻 N/V	LDO1S	Slot 0 • N/V	VPRESC	21 mV/µs 🔹	N/\
PWRDWN_DFS	Transition to • N/V	PLL_SEL	Disabled - N/V	LDO2S	Slot 0 - N/V	VPREILIM	50 mV -	N/\
AUTORETRY_EN	Disabled • N/V	FOUT_SLOT_EN	FOUT slot as: • N/V	PWRUP_LASTS	Power up enc * N/V	VPRETOFF	80 ns	N/\
AUTORETRY_INFINITE	E 15 times • N/V	FOUTS	Drive FOUT I - N/V	PWRDWN_FIRSTS	Power down * N/V	VPRESRLS	PU/PD/130 n *	N/\
VMON0_REG_ASSIGN			No synchroni * N/V	Write	Read	VPRESRHS	PU/PD/130 n *	Ξ.
VMON1_REG_ASSIGN			Do not wait f * N/V			VPRE_CLK_SEL		N/\
VMON4_REG_ASSIGN			FG No Power do * N/V			VPRE_PH	Not delayed -	
DEVICE_ID	0x00 • N/V	Write	e Read			VPRE_OFF_DLY	OFF dly 250 *	N/\
Write	Read			J		Write	Read	
		J						_
BOOST Confi BOOSTEN Di		BUCK Con		LDO1 Config		LDO2 Conf	-	1.0.4
	isabled - N/V B	UCKEN	Disabled 🔹 N/V 🛛 LI	DO1V 1.5		JZV 1	1.1 V - I	V/V
			N/N/ 11	DOL CHU EN DI	LL L NAV LD			101
BOOSTV 5.							400 mA - 1	
BOOSTV 5. BOOSTTONTIME 50	Dins N/V B	UCKV 1	I V - N/V C	DO1_SW_EN Dis ONF_TSD_LDO1 Reg		D2ILIM 4 NF_TSD_LDO2 R		
BOOSTV 5. BOOSTTONTIME 50 BOOSTSC 35	D ns N/V B 58 mV/µs ▼ N/V B	UCKV 1 UCK_CLK_SEL	L V - N/V C CLK1 - N/V					
BOOSTV 5. BOOSTTONTIME 50 BOOSTSC 35 BOOSTRCOMP 75	0 ns N/V B 58 mV/μs • N/V B 50 kΩ • N/V B	UCKV 1 UCK_CLK_SEL C UCK_PH N	L V - N/V C CLK1 - N/V Not delayed - N/V	ONF_TSD_LDO1 Reg	gulator sht • N/V CC	NF_TSD_LDO2	Regulator sht - 1	
BOOSTV5.BOOSTTONTIME50BOOSTSC35BOOSTRCOMP75BOOSTCCMP12	D ns N/V Bi 58 mV/μs N/V Bi 50 kΩ N/V Bi 25 pF N/V Bi	UCKV 1 UCK_CLK_SEL C UCK_PH N UCK_CTRL_RC 6	I V ~ N/V C LK1 ~ N/V C Not delayed ~ N/V C 55KΩ ~ N/V C	ONF_TSD_LDO1 Reg	gulator sht • N/V CC	NF_TSD_LDO2	Regulator sht - 1	
BOOSTV5.BOOSTTONTIME50BOOSTSC35BOOSTRCOMP75BOOSTCCOMP12BOOSTLLIM2	D ns N/V B 58 mV/μs N/V B 50 kΩ N/V B 25 pF N/V B A N/V B	UCKV 1 UCK_CLK_SEL 0 UCK_PH 1 UCK_CTRL_RC 6 UCK_CTRL_GM 4	L V - N/V LK1 - N/V Not delayed - N/V 55KΩ - N/V 18 μS - N/V	ONF_TSD_LDO1 Reg	gulator sht • N/V CC	NF_TSD_LDO2	Regulator sht - 1	
BOOSTV 5. BOOSTTONTIME 50 BOOSTSC 33 BOOSTSCOMP 72 BOOSTCCOMP 12 BOOSTILIM 2 BOOSTSR 50	D ns N/V B 58 mV/μs N/V B 50 kΩ N/V B 25 pF N/V B A N/V B 0 V/μs N/V B	UCKV 1 UCK_CLK_SEL 0 UCK_PH 1 UCK_CTRL_RC 0 UCK_CTRL_GM 4 UCKILIM 2	L V • N/V C LK1 • N/V N/V C Vot delayed • N/V N/V K 55KΩ • N/V N/V K 18 μS • N/V N/V N/V	ONF_TSD_LDO1 Reg	gulator sht • N/V CC	NF_TSD_LDO2	Regulator sht - 1	
BOOSTV 5. BOOSTTONTIME 50 BOOSTSC 35 BOOSTCOMP 75 BOOSTCOMP 12 BOOSTLM 2 BOOSTSR 50 BOOST_CLK_SEL C	D ns N/V B 58 mV/μs N/V B 50 kΩ N/V B 25 pF N/V B 0 V/μs N/V B 0 V/μs N/V B LK1 N/V D	UCKV 1 UCK_CLK_SEL C UCK_PH M UCK_CTRL_RC C UCK_CTRL_GM 4 UCKILIM 2 WS_BUCK 1	L V N/V C LK1 N/V N/V C Not delayed N/V N/V N/V 3555Ω N/V N/V N/V 18 µS N/V N/V N/V 0.1 A N/V N/V N/V	ONF_TSD_LDO1 Reg	gulator sht • N/V CC	NF_TSD_LDO2	Regulator sht - 1	
BOOSTV 5. BOOSTCONTIME 50 BOOSTSC 35 BOOSTRCOMP 75 BOOSTRCMP 12 BOOSTRUM 2 BOOSTR 50 BOOSTSC 10 BOOSTSC 10 BOOSTSC 10 BOOSTSC 10	D ns N/V B 58 mV/μs N/V B 50 kΩ N/V B 25 pF N/V B 0 V/μs N/V B 0 V/μs N/V B LK1 N/V C	UCKV 1 UCK_CLK_SEL C UCK_PH M UCK_CTRL_RC C UCK_CTRL_GM 4 UCKILIM 2 WS_BUCK 1	L V • N/V C LK1 • N/V N/V C Vot delayed • N/V N/V K 55KΩ • N/V N/V K 18 μS • N/V N/V N/V	ONF_TSD_LDO1 Reg	gulator sht • N/V CC	NF_TSD_LDO2	Regulator sht - 1	
BOOSTV 5. BOOSTSC 35 BOOSTSC 35 BOOSTCOMP 75 BOOSTCOMP 12 BOOSTLIM 2 BOOSTSR 55 BOOST_CLK_SEL C	D ns N/V B 58 mV/μs N/V B 50 kΩ N/V B 25 pF N/V B 0 V/μs N/V B 0 V/μs N/V B LK1 N/V C	UCKV 1 UCK_CLK_SEL C UCK_PH M UCK_CTRL_RC C UCK_CTRL_GM 4 UCKILIM 2 WS_BUCK 1	L V N/V C LK1 N/V N/V C Not delayed N/V N/V N/V 3555Ω N/V N/V N/V 18 µS N/V N/V N/V 0.1 A N/V N/V N/V	ONF_TSD_LDO1 Reg	gulator sht • N/V CC	NF_TSD_LDO2	Regulator sht - 1	

Figure 33. Main mirrors tab



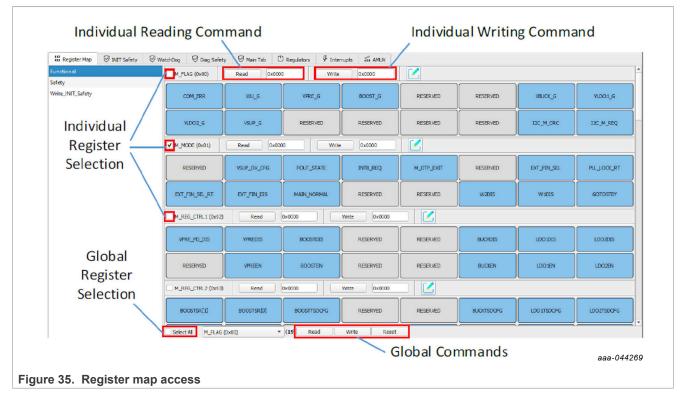
•

6.6.3 Access tab

6.6.3.1 Register map

All PF5030 I²C registers can be accessed in write and read mode using this tab shown in <u>Figure 35</u>. These registers are divided into three sections:

- **Functional**: Main functional I²C registers (diagnostics, configuration, and controls)
- **Safety**: Safety I²C registers (diagnostics and configuration)
- Write INIT safety: Safety registers that can be written only during initialization phase (INIT_FS state).



To read the values of a register, click the **READ** button. The value is read from the device and is displayed on a label near the **READ** button. It is also displayed in the log window.

To write the bit values individually, click the desired bit. The corresponding bit button color changes. The value is updated in the log window. Click the WRITE button to write the register. To write the values through a text box near the **WRITE** button, enter the appropriate write value. Then click the **WRITE** button to write the register.

When registers have been selected, global commands can also be used:

- WRITE: Writes data to all the selected register at once.
- READ: Reads data back from the selected register at once.
- **RESET**: Resets all the input text boxes to 0x00. Write bits are set to 0. Change register bit buttons are set to the default setting.

The value can also be written by selecting the Edit option near the **WRITE** button. Bits and corresponding values are displayed in a pop window as shown in <u>Figure 36</u>. Select the options of all write bits, close the input dialog box, and click the **WRITE** button. Selected input combinations are written to the register.

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RESERVED	VSUP_OV_CF	G FOUT_STATE	INTB_REQ	M_OTP_E	т	RESERVED	EXT_FIN_SEL	PLL_LOCK_RT
EXT_FIN_ SEL_RT	EXT_FIN_DIS	MAIN_N ORMAL	RESERVED	RESERV		W2DI5	W1DI5	GOTOSTBY
NP M	I_MODE (0x01) Bit-M	1ap Dialog			7			×
Set	Value (Edital	ble)		Register C	Conte	nt		
FOUT INTB M_O' EXT_ EXT_ W2D W1D	T_STATE: [B_REQ:] DTP_EXIT:] _FIN_sel:] _FIN_DIS:] DIS:] DIS:]	0V min - 32V type Drive FOUT pin low : to Assertion to action to action to affect vake up enabled vake up enabled bevice remains in cu	state • • • • • • • • • • • • • • • • • • •	FOUT_STA	TE: RT: EL_R1	Drive FOUT PLL not lock F: Internal doc	k oscillator is selec e NOT in Normal bled	tted



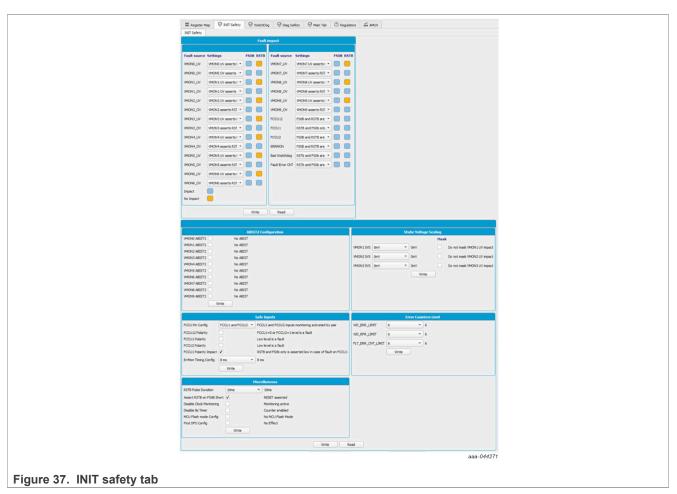
Writing an INIT_FS register automatically updates the corresponding NOT register.

6.6.3.2 INIT Safety tab

This tab allows the initialization phase (INIT_FS state) configuration, that must be done before the first good watchdog refresh until the 2 seconds timeout limit.

In this tab, safety features can be configured, such as the safety output reaction when voltage monitoring fault is detected, watchdog refresh counter, fault error counter, as shown in <u>Figure 37</u>. The Analog Built-In Self-Test 2 ABIST2 (used for voltage monitoring assigned to external regulator), the VMON1 Static Voltage Scaling, counters limit, and other INIT_FS registers are also configurable from this tab. See the PF5030 data sheet for a complete description of these registers.

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To ease the configuration, Read and Write All buttons are implemented.

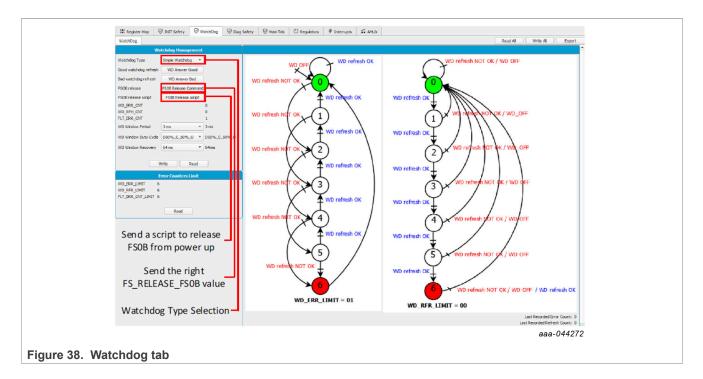
6.6.3.3 Watchdog tab

The watchdog tab gathers all the registers and configurations having an impact on the watchdog, except "Watchdog Type". The watchdog error and refresh counters are displayed depending on the limit configuration. Watchdog answers can be generated and sent to the device depending on the watchdog type. The watchdog type configured in the OTP must be manually selected in the drop-down list to explore the watchdog features. If the user is not aware of the type of watchdog configured in the OTP, it can be found in Mirrors tab.

The "FS0B Release Command" calculates and sends the right secure 16-bit word to release FS0B.

A simplified way to release FS0B after power-up is to select the right type of watchdog configured in the OTP and then click the "FS0B Release script" button. This action sends the right sequence to close the initialization sequence, sets the error counter back to 0, and then releases FS0B, shown in Figure 38.

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6.6.3.4 Diagnostic Safety tab

The diagnostic safety tab shown in Figure 39 makes it possible to know the safety status of the device. The safety function events, like voltage monitoring flags, analog and logical BIST status, and safety pins are automatically reported in this tab. The PF5030 can also get out of OTP or Debug mode using this tab.

Safe IO	Diag. Safety	OV/UV Status	Status and States	General Flags
Report PCOOD Change No failure Report PCOD Devent No Power GOOD Report PCOD Devent No external RESET STB drag No external RESET STB drag No reset STB drag No failure STB revect Bor failure STB revect No reset STB revect Bor failure STB revect No failure STB revect Bor failure STB revect Bor failure STB revect Bor failure STB revect Bor failure STO enne High FSOB drag No failure StOB request Bor failure Stob INIT fail-sofe Read	PCCU12 Error No Error PCCU12 Error RT No Error PCCU1 Error RT No Error PCCU1 Error RT No Error PCCU2 Error RT No Error PFMOn Advowledge ErrMon Status ErrMon Status Good WD Refresh WD Tming Good WD Refresh PS 12C CRC Status No Error F3 12C Access Status No Error Write Read	WICH0_JIV No Indervoltage WICH1_UV No Indervoltage WICH1_UV No Unervoltage WICH1_UV No Unervoltage WICH1_UV No Unervoltage WICH1_UV No Unervoltage WICH1_UV No Undervoltage WICH2_UV No Undervoltage WICH2_UV No Undervoltage WICH3_UV No Undervoltage WICH4_UV No Undervoltage WICH4_UV No Undervoltage WICH5_UV No Undervoltage <t< th=""><th>ABISTI Status Pess ADISTI Status Pess UBIST Status Pess FS Test Mode Activation Status Active FS Debug Mode Ext FS Debug Mode RT No debug FS OTP Mode Ext FS OTP Mode Ext FS OTP Mode RT No debug Fail Safe Machine State FS 13 Write Read</th><th>PS 12C Communication Error Active Watchdog Reflexit Error No debug Voltage Monitoring Error Dx00 OTP 81C compution No corruption No corruption No corruption Write Read</th></t<>	ABISTI Status Pess ADISTI Status Pess UBIST Status Pess FS Test Mode Activation Status Active FS Debug Mode Ext FS Debug Mode RT No debug FS OTP Mode Ext FS OTP Mode Ext FS OTP Mode RT No debug Fail Safe Machine State FS 13 Write Read	PS 12C Communication Error Active Watchdog Reflexit Error No debug Voltage Monitoring Error Dx00 OTP 81C compution No corruption No corruption No corruption Write Read

6.6.3.5 Main tab

UM11854

Main configuration is possible from the main tab shown in Figure 40. The clock management box allows the configuration of the clock modulation. A regulator can be assigned to a voltage monitoring using the VMON assignment box, leading to a shutdown if OV occurs on the associated regulator.

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The PF5030 can enter STANDBY/LPOFF state using the "Go to Standby" command, setting the bit GOTO STBY = 1.

	lock Management			Miscellaneous	VMO	N Assignment	
Clock Frequency Tuning 0 External FIN Deable External FIN Select RT External FIN Select RT FIN Divides Select Divides OUT MUS Select High m FOUT Olock Select CK 14 FOUT Phase Delay No deli	Internal clock or by 1 v Divider by 1 PLL not locked pedance (HI High impedance elected C K 1 selected	lation scillator is selected	BAT Fail VSLP OV Weet: Deable Wake: Deable Wake2 RT Wake2 Deable Wake2 RT XFALLB RT Main 12C RCS Status Main 12C Access Status INTB Assertion Request	Battery Disconceton (POR cocurs) Bottery Disconceton (POR cocurs) S0V min - 32V type - 34V max wake up enabled WARE: Is high wake up enabled WARE: Is low level XFALE: Is low level No error No error Write Reed	VMON1 External Regulator VMON2 External Regulator VMON2 External Regulator VMON3 External Regulator VMON4 External Regulator VMON6 External Regulator VMON6 External Regulator VMON7 External Regulator	External Regulator (No action if OV) External Regulator (No action if OV) External Regulator (No action if OV)	
Battery			eral Flags	Device State		Power Sequence	
	/ driver command sensed high / pad sensed high AT_SC_CFG Read	Wake Up Event VSJP Event VPRE Event VBOOST Event Buck Event LDO1 Event LDO2 Event	Ition Error No Failure Wake event Event occurred Event occurred No Event No Event No Event No Event No Event	Resume from DFS due to TSD Event Does not resume fro Resume from DFS Does not resume fro	te FOI im STRY im STRY due to XFAILB im deep fail-sofe due to TSD	ILD Glot <u>Do not assert durin</u> <u>O</u> o not ass JIF Glot <u>Do not drive during</u> <u>O</u> o not dri JIF State <u>Drive FOU</u> <u>Write</u> Read	

6.6.3.6 Regulators tab

The regulator tab shown in Figure 41 is used to configure the PF5030 SMPS or LDO. Regulators can be enabled or disabled on registers using I²C commands, and the state / status of each regulators is also shown.

Each regulator has its own thermal shutdown (TSD) protection. After a TSD, the regulator is automatically reenabled when the temperature returns to the normal operation range. Nevertheless, an additional configuration, by regulator, is available to make device transition to deep fail-safe (DEEP-FS) state in case of TSD and consequently shut down all regulators. In a practical perspective, it means that TSD on regulators supplying MCU rails can be configured to make a transition to DEEP-FS while regulators supplying external loads wont.

Voltage R	legulators	Regulators Control
VPRE PRE HS Raing SR PU/PC/120mA * PU/PC/130mA PRE HS Paling SR PU/PC/120mA * PU/PC/130mA PRE LS SR PU/PC/900mA * PU/PC/900mA PRE Pull Down Disable no effect write	VBODST Behavior in case of TSD Regulator shutdown + Regulator shutdown + State machine it ansitton to Standby mode VBODST LS SR 500 V/Ls Write 500 V/Ls	VPRE Finable in Normal Mode VPRE Disable in Normal Mode Boost Einable in Normal Mode Boost Stable in Normal Mode Boost Stable in Normal Mode Buck Einable in Normal Mode Buck State Buck State
BUCK ehavior in case of TSD Regulator shutdowr V Regulator shutdown + State machine transition to Standby mode Write	LDO1 Behavor in case of TSD Regulator shutdown V Regulator shutdown + State machine transition to Standby mode Write	LD01Enable in Normal Mode LD01Disable in Normal Mode LD01State LD02Chable in Normal Mode LD02DStable in Normal Mode LD02DState
ehavior in case of TSD Regulator shutdown * Regulator shutdown + State machine transition to Standby mode Write Write Write	Read	Write Read

Figure 41. Regulators tab

6.6.3.7 Main interrupts tab

The main interrupts tab shown in <u>Figure 42</u> allows the monitoring of the regulators, the wake inputs, and the communication events or status. It allows the reading, writing, and polling of overvoltage/undervoltage, overtemperature, and overcurrent flags.

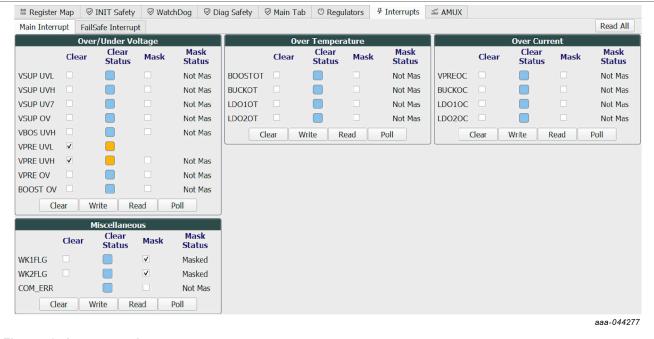


Figure 42. Interrupts tab

Different commands can be used to manage the interrupts:

- Clear: Interrupt flags latched and selected are cleared
- Write: Masks an interruption when the mask is selected
- · Read: Gives the status of all interrupts
- Poll: Reads interrupts values in a loop

Additionally, Clear All / Read All buttons are available to control all interrupts on one click.

6.6.3.8 Fail-safe interrupts tab

The fail-safe interrupts tab shown in <u>Figure 43</u> allows the monitoring of the overvoltage/undervoltage fail-safe monitoring status and the watchdog. It allows the reading, writing, and polling of overvoltage/undervoltage flags.

Main Interrupt		afe Interrupt			-									Read All
	U	nder Voltag	e			0\	ver Voltag	e		Safety Interrupts				
(Clear	Clear Status	Mask	Mask Status		Clear	Clear Status	Mask	Mask Status		Clear	Clear Status	Mask	Mask Statu
VMON0 UV				Not Mas	VMON0 OV				Not Mas	FCCU1				Not Ma
VMON1 UV				Not Mas	VMON1 OV				Not Mas	FCCU2				Not Ma
VMON2 UV				Not Mas	VMON2 OV				Not Mas	FCCU12				
VMON3 UV				Not Mas	VMON3 OV				Not Mas	ERRMON				Not Ma
VMON4 UV				Not Mas	VMON4 OV				Not Mas	BAD_WD_DATA				
VMON5 UV				Not Mas	VMON5 OV				Not Mas	BAD_WD_TIMING				
VMON6 UV				Not Mas	VMON6 OV				Not Mas	Clear	Write	Read	Poll	
VMON7 UV				Not Mas	VMON7 OV				Not Mas					
VMON8 UV				Not Mas	VMON8 OV				Not Mas					
VMON9 UV				Not Mas	VMON9 OV				Not Mas					
Clear	W	rite Rea	d 🔤 I	Poll	Cle	ar Wri	te Re	ad	Poll					
-													aa	a-0442

The same set of commands is used as the set to manage the interrupts as main interrupts.

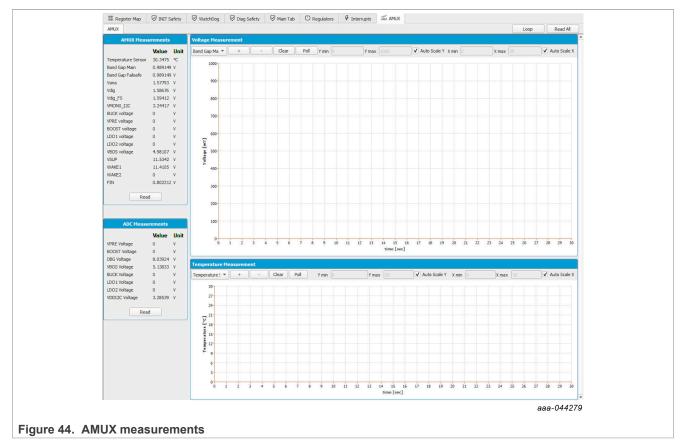
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6.6.3.9 AMUX

The AMUX tab shown in <u>Figure 44</u> allows the selection of an AMUX pin channel and gets its current value by using the exclusive KL25Z AMUX ADC channel. You can do a single read or display various channels dynamically on the voltage or temperature graph. The displayed values already apply the divider and temperature formulas.

The input / output voltage rails are also monitored independently using additional the KL25Z ADC channels.

To use the dynamic graph, select the channel then click the "+" button to add to the graph. To start polling, click the "Poll" button. Click the "Poll" button again to stop measurements.



7 Using an evaluation board

Before starting the process, consult the development board scheme and user manual to configure the required use case.

Learn about OTP before operating with the device. The device has a high level of flexibility due to the parameter configuration available in the OTP. It impacts the functionality of the device. It is key to understand how OTP parameters can be programmed, the interaction with mirror registers, and the PF5030 device.

The OTP-related operations can only be performed in test mode (emulation) and OTP mode (programming, test mode is enabled automatically). When using emulation, the device loses the configuration when the power supply is switched off, when the device enters deep fail-safe (DEEP-FS) state, or when it goes standby.

7.1 OTP and mirrors registers

The device incorporates two OTP blocks. One is for the main section, the other for the fail-safe section. During configuration, each of them uses dedicated sectors.

Each block is divided in two sectors, S1 and S1bis respectively, so the device can be fused two times. The OTP configuration scheme is shown in <u>Figure 45</u> (same implementation for main and fail-safe).

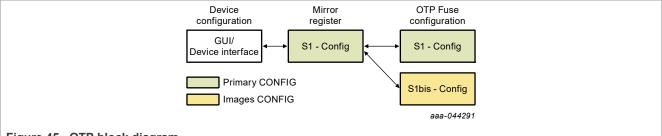


Figure 45. OTP block diagram

At device starts-up, the content of the valid (last programmed) sector is loaded into mirror registers. The mirror register content is accessible from the NXP GUI, using specific I²C commands. The NXP GUI manages the mirror configuration, which facilitates access. The mirror register content handling is called "OTP emulation".

To burn the OTP configuration, the mirror register content must be loaded with the desired content. Then a command must be sent to burn the mirror content to the next available OTP sector. The first sector to be burned is S1, the second S1bis. The NXP GUI automatically manages the next sector to be burned. It is not possible to revert to the previous sector. When the user reaches the sector S1bis, there is no other possibility for burn. However, the emulation is still available.

7.2 Device modes

There are several modes that describe device operation.

There are three modes to run the device:

- User mode: Only user-related registers can be accessed and handled.
- **OTP mode**: OTP fuse content loaded to mirror registers. OTP programming / emulation (mirror registers handling) possible.
- Test mode: OTP programming and mirror registers handling (emulation) granted.

There are two modes to run the device related to the fail-safe state machine:

- Normal mode: Watchdog windowing and initialization (INIT_FS state) timeout depend on OTP configuration.
- Debug mode: Watchdog windowing disabled, no initialization timeout, fail-safe safety reactions disabled.

Debug and OTP modes are enabled by applying voltage on DBG pin during startup and/or restart.

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OTP mode activation implies in Debug mode activation.

Debug and OTP modes can be disabled with an I^2C command.

Test mode can be enabled at any moment with an I²C command when the voltage is applied on DBG pin.

7.3 Configuring the hardware for start-up

<u>Figure 46</u> presents a typical hardware configuration incorporating the development board, power supply and, Windows PC workstation.

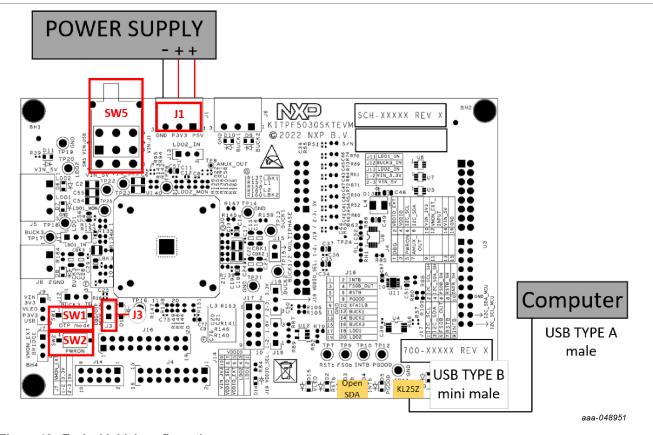


Figure 46. Typical initial configuration

To configure the hardware and workstation as illustrated in Figure 46, complete the following procedure:

1. Install jumpers and switches for the configuration shown in <u>Table 22</u>.

Board	Configuration								
configuration	Normal mode	OTP / test mode entry							
Watchdog configuration	Watchdog windowing enabled, 2 seconds INIT_FS timeout (OTP WDW_INF = 0)	Watchdog windowing disabled,	OTP programming / emulation,						
	Watchdog windowing disabled, no INIT_FS timeout (OTP WDW_INF = 1)	no INIT_FS timeout	Debug mode enabled						
J3 (DBG)	Open	Connect 1 to 2 DBG pin voltage pulled to 4.5 V or 7.95 V (SW1							
SW2 (PWRON)	Close (I	Close (PWRON pin high-logic level)							
SW5 (VIN)	Midd	le position (supplies OFF)							
SW1 (OTP mode)	Open (DBG = VIN	_5V)	Close (OTP mode ON)						

Table 22. Hardware configuration

- 2. Connect the Windows PC USB port to the KITPF5030SKTEVM board using the provided USB 2.0 cable.
- 3. If external power supplies are used, set the power supplies to 3.3 V and 5.0 V, and current limit to 1.0 A. With power turned off, attach the power supplies positive and negative outputs to J1, then turn on.
- 4. Put SW5 in LEFT position if USB power is used or RIGHT position if external power supply is used.

At this step, if the product is in OTP mode entry configuration, all regulators are OFF. The user can power up with an OTP configuration or configure the mirror registers before powering up. Power-up sequence starts as soon as one of these four actions occurs:

- J3 jumper is removed
- SW1 is switched OFF
- OTP mode exit command is sent using I²C
- NXP GUI button "Exit OTP Mode" is clicked

7.4 Working in OTP emulation mode

At start-up, the device always uses the content of the mirror register. This content can come from OTP fuse or from a configuration written directly in the mirror register. OTP emulation means that the user can emulate the fuse content by writing in the mirror register, which allows trials before burning the OTP.

- 1. Configure the hardware for OTP mode entry.
- 2. Launch the NXP GUI for Automotive PMIC Families software.
- 3. Create an OTP configuration and export/generate the TBB/OTP script file.
- 4. Establishing the connection between the NXP GUI and the hardware.

MCU: FRDM-KL25Z State: CONNECTED	Protocol: I ² C Firmware: 0.3 Application 3.1.144 Device Mode: user-mode Color legend: High Low	FS CURRENT STATE :	OTP_MODE
			000 04

Check that the fail-safe state machine is in OTP MODE state and "Exit OTP mode" must be green. If not, check 1 and redo this step. While in OTP mode, all regulators are off.

- 5. On the script editor, load the TBB/OTP script file and send content to the mirror registers.
- 6. Click "Exit OTP mode" button, if all goes right, regulators start-up and fail-safe state machine must be in INIT FS state.

MCU: FRDM-KL25Z State: CONNECTED	Protocol: I ² C Firmware: 0.3 Application 3.1.144 Device Mode: test-mode Color legend: High Low FS CURRENT STATE :	INIT_FS
		aaa-044295

- a. If the mirror registers are filled (with a configuration using the Script editor), that configuration is used in the emulation session.
- b. If the mirror registers are not filled (with a configuration using the Script editor), the currently programmed OTP fuse configuration is used, if it exists.

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c. Otherwise, the mirror registers are not filled and the OTP fuse is not burned. The device does not start up properly.

Device is in Debug mode. As long as Debug mode is not exited by writing FS_STATES: [FS_DBG_MODE_EXIT] bit to 1, the FS0B pin cannot be released.

7.5 Releasing FS0B script

The following script can be used to release FS0B:

- Disable the watchdog windowing (simple watchdog configuration is used here).
- Close the initialization phase with (a first) good watchdog refresh.

Table 23 Release FS0B sequence example for simple watchdog (ASIL B)

- Exit the Debug mode.
- Send six (default) additional consecutive good watchdog refreshes to revert the fault error counter to 0.
- Release FS0B pin, which is only valid if watchdog windowing is activated in OTP.

Table 20. Release i oub sequence example for simple wateraog (Aoie D)									
	Step	Register name	Value	Description					

Step	Register name	Value	Description
1	FS_WD_WINDOW_DUR	0x020B	WDW_PERIOD[4:0] = 0x00000 (watchdog disabled)
2	FS_NOT_WD_WINDOW_DUR	0xFD04	NOT of FS_WD_WINDOW_DUR
3	FS_WD_ANSWER	0x5AB2	1st good watchdog answer (close the initialization phase)
4	FS_STATES	0x4000	FS_DBG_MODE_EXIT = 1 (exit debug mode)
5	FS_WD_ANSWER	0x5AB2	2nd good watchdog answer
6	FS_WD_ANSWER	0x5AB2	3rd good watchdog answer
7	FS_WD_ANSWER	0x5AB2	4th good watchdog answer
8	FS_WD_ANSWER	0x5AB2	5th good watchdog answer
9	FS_WD_ANSWER	0x5AB2	6th good watchdog answer
10	FS_WD_ANSWER	0x5AB2	7th good watchdog answer
11	FS_RELEASE_FS0B	0xB2A5	FS0B pin released (pulled to high level)

This sequence can be sent using a script built with NXP GUI. There are two options:

- Clicking ACCESS > WatchDog > "Watchdog Management" > "FS0B Release script". Remember to chose appropriated "Watchdog Type" before.
- Clicking SCRIPT (editor) > Generator > "FS0B_RELEASE_XX_WATCHDOG", then click "RUN".

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8 References

[1] **KITPF5030SKTEVM** — detailed information on this board, including documentation, downloads, and software and tools

http://www.nxp.com/KITPF5030SKTEVM

- [2] **PF5030** detailed information on PF5030 <u>http://www.nxp.com/PF5030</u>
- [3] NXP GUI for Automotive PMIC Families Software GUI for NXP Automotive PMIC products https://www.nxp.com/PMIC-GUI-SW

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