UM11854

KITPF5030SKTEVM programming board

Rev. 1 — 9 March 2023 User manual

Document information

Information	Content
Keywords	PF5030, KITPF5030SKTEVM, KL25Z, I^2C, spf-53091
Abstract	The KITPF5030SKTEVM provides flexibility to explore all the features of the device and make measurements on the main part of the application.

Revision history

Rev	Date	Description
v.1	20230309	Initial release

Important notice

NXP provides the enclosed product(s) under the following conditions:

This evaluation kit is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This evaluation board may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. This evaluation board is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

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1 Introduction

The KITPF5030SKTEVM board user manual is intended for the engineers involved in the evaluation, design, implementation, and validation of PF5030 Configurable Power Management IC.

The KITPF5030SKTEVM enables development on PF5030 family of devices. The kit can be connected to the NXP GUI software, which allows the user to explore registers, try OTP configurations, and burn the part.

The devices can be placed and removed easily from the board using the socket. This board supports the PF5030 family of devices.The delivered board consists of a soldered device with empty OTP content in order to leave the opportunity to the user to burn the OTP configuration. The board contains a superset device PPF5030BMDA0ES, allowing tests on all the PF5030 derivatives. Each device OTP can be burned twice, which provides flexibility.

2 Finding resources and information on the NXP website

NXP Semiconductors provides online resources for this evaluation board and its supported devices on http://www.nxp.com.

The information page for KITPF5030SKTEVM board is available at http://www.nxp.com/KITPF5030SKTEVM. The information page provides overview information, documentation, software and tools, parametric data, ordering information and a Getting Started tab. The Getting Started tab provides quick-reference information applicable to using the KITPF5030SKTEVM board, including the downloadable assets referenced in this document.

The information page for "NXP GUI for Automotive PMIC Families" is at http://www.nxp.com/NXP GUI for Automotive PMIC Families. The information page provides overview information, documentation, downloads, and development tools.

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3 Getting ready

Working with the KITPF5030SKTEVM requires the kit contents, additional hardware, and a Windows PC workstation with installed software.

3.1 Kit contents

- Assembled and tested KITPF5030SKTEVM connected to a FRDM-KL25Z in an anti-static bag
- 2 ft or 3 ft USB-STD A to USB-B-mini cable
- 1x Pluggable terminal block, two positions, straight, 3.81 mm pitch
- 3x Pluggable terminal block, three positions, straight, 3.81 mm pitch
- Jumpers mounted on board
- Quick Start Guide

3.2 Additional hardware

In addition to the kit contents, the following hardware is necessary or beneficial when working with this kit.

- One or two power supplies with a range from 3.3 V to 5.0 V, and a current limit set initially to 1.0 A

3.3 Windows PC workstation

This evaluation board requires a Windows PC workstation. Meeting these minimum specifications should produce great results when working with this evaluation board.

- USB-enabled computer with Windows 7 or Windows 10

3.4 Software

Installing software is necessary to work with this evaluation board. All listed software is available on the evaluation boards information page.

- http://www.nxp.com/KITPF5030SKTEVM
- NXP GUI for automotive PMIC families - latest version

4 Getting to know the hardware

The KITPF5030SKTEVM provides flexibility to explore all the features of the device and make measurements on the main part of the application. In combination with the FRDM-KL25Z MCU board, the NXP GUI software allows access to the registers in read and write mode. All regulators are accessible through connectors. DC-DC switching nodes and other nonuser signals are mapped on test points. Digital signals (I^2C, RSTB) are accessible through connectors. Pin PWRON has a switch to control them. A supply switch is available to power on or off the device.

The main purpose of this kit is to burn the OTP configuration.The main purpose of this kit is to evaluate PF5030 in automotive applications. The device always starts loading the fused configuration (OTP) (that may be blank) to the mirror registers, then the user can override the mirrors using Emulation mode. The device can be programmed/fused two times. This board is able to fuse the OTP without any extra tools or board. In Emulation mode, as long as the power is supplied, the board configuration stays valid. However, the main and fail-safe configurations are lost when the device restarts or goes into deep fail-safe (DEEP-FS) state, because OTP is reloaded and overwrite the mirrors content.

Note: *Due to the socket, this kit is not optimized for performance measurement or current higher than 1.0 A.*

4.1 Kit overview

The KITPF5030SKTEVM is a hardware evaluation tool that allows OTP burning. Due to the socket, PF5030 part can be configured without the need to solder it. Devices can be programmed two times.The KITPF5030SKTEVM is a hardware evaluation tool that allows performance test. PF5030 can be evaluated with this board because it is populated with a superset part. The PPF5030BMDA0ES part soldered on the board can be fused twice.

An Emulation mode is possible to test as many configurations as needed. From USB voltage, an external DC-DC provides VDDIO_SEL voltage with a choice of 1.8 V, 3.3 V (default), or 5.0 V. Furthermore, another external DC-DC generates the OTP programming voltage (7.95 V) without any need for an external power supply.

4.2 KITPF5030SKTEVM features

- VIN power supply connector (1x or 2x 3.3 V to 5.0 V)
- BUCK1 and BUCK2: 0.7 V to 1.5 V up to 1.0 A (socket limit)
- BUCK3: 1.0 V to 3.3 V up to 1.0 A (socket limit)
- LDO1 and LDO2: 1.5 V to 5.0 V
- PWRON switch
- FS0B external safety pin
- Embedded USB connection for easy connection to software NXP GUI (access to I^2C bus, IOs, RSTB, FS0B, INTB, debug, AMUX_OUT, regulators, register access, OTP emulation, and OTP programming)
- LEDs that indicate signals and regulator status
- Support OTP fuse capabilities
- Voltage monitoring jumper setting

4.3 Schematic, board layout, and bill of materials

The schematic, board layout, and bill of materials for the KITPF5030SKTEVM board are available at http://www.nxp.com/KITPF5030SKTEVM.

4.3.1 VMON board configuration

The VMON configuration is highly dependent on the use case. This kit is delivered with a default configuration.

The user can assign VMON_EXT differently to address the use case using J4 and J7 connectors shown in Figure 1. J7 is used to select the VMON_EXT (VMON0) external resistor divider to monitor 3.3 V or 5.0 V. J4 is used to connect the VMON_EXT external resistor divider input VMON_EXT_INPUT to an external voltage, VIN_3V3, or VIN_5V. By default, VMON_EXT is monitoring VIN_3V3.

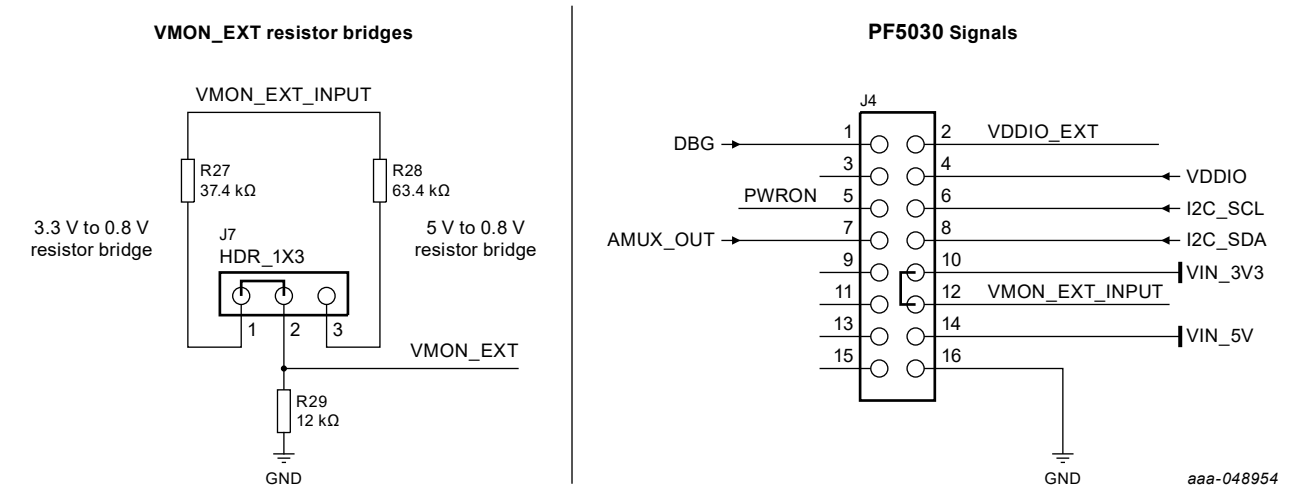

Figure 1. VMON_EXT assignment (VIN_3V3 default)

By default, BUCK2_FB (VMON2) is connected to BUCK2 though R162. However, When BUCK2 is disabled or used in multiphase with BUCK1, BUCK2_FB can be connected to an external voltage. R162 must be removed in this case and the internal DAC must be configured to the voltage monitoring target.

By default, LDO1_MON (VMON4) and LDO2_MON (VMON5) pins are tied to LDO1 and LDO2, respectively. LDO1_MON and LDO2_MON can be used to monitor an external voltage using test points TP25 (LDO1_MON) and TP26 (LDO2_MON), then R154 and/or R156 must be removed. Figure 2 shows the corresponding part of the schematic. The internal resistors dividers can be configured to select the voltage monitoring target.

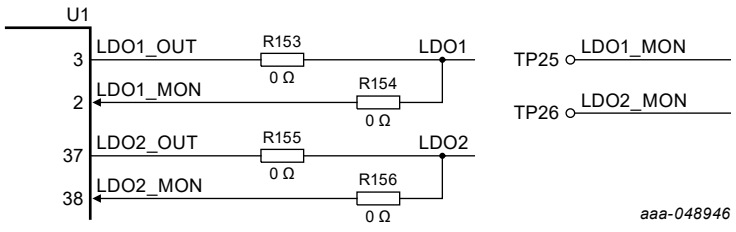

Figure 2. LDO1_MON and LDO2_MON input configuration

4.3.2 I²C

The I²C bus is connected to KL25Z MCU to communicate with NXP GUI. Another MCU can be connected to the I²C bus on J4 connector, but J17 1-2 and 3-4 must be removed to disconnect the FRDM-KL25Z MCU (see Figure 3). In addition to this change, make sure that the VDDIO voltage domain and ground are the same on MCU side and KITPF5030SKTEVM side.

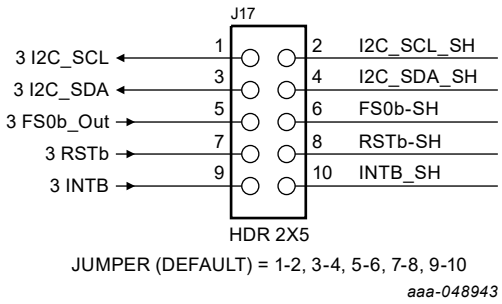

Figure 3. I²C connection to FRDM-KL25Z

4.3.3 VDDIO

The VDDIO pin is powered through VDDIO net and is used to supply internal buffers and I^2C communication.

The selection of VDDIO is made using J14 connector as shown in Figure 4. By default, an external LDO is provided to feed VDDIO through the VDDIO_SEL net.

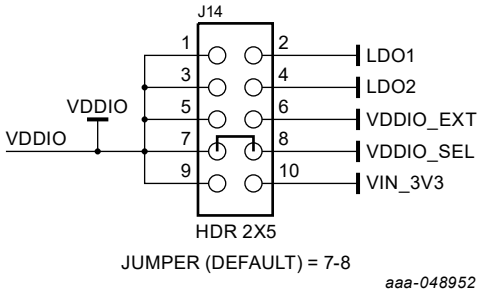

Figure 4. VDDIO selection

The I^2C is compatible with 1.8 V, 3.3 V, and 5.0 V, therefore VDDIO_SEL voltage is configurable between 1.8 V, 3.3 V, or 5.0 V using J18 and J19 connectors (3.3 V by default) shown in Figure 5.

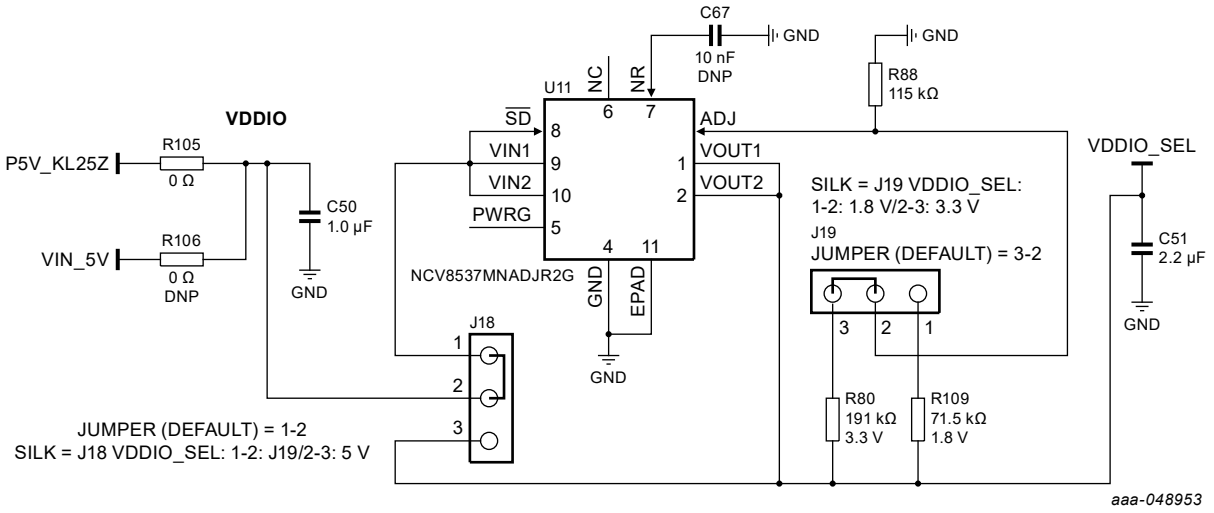

Figure 5. VDDIO_SEL supply voltage selection

4.4 Kit featured components

Figure 6 identifies important components and Table 1 provides details.

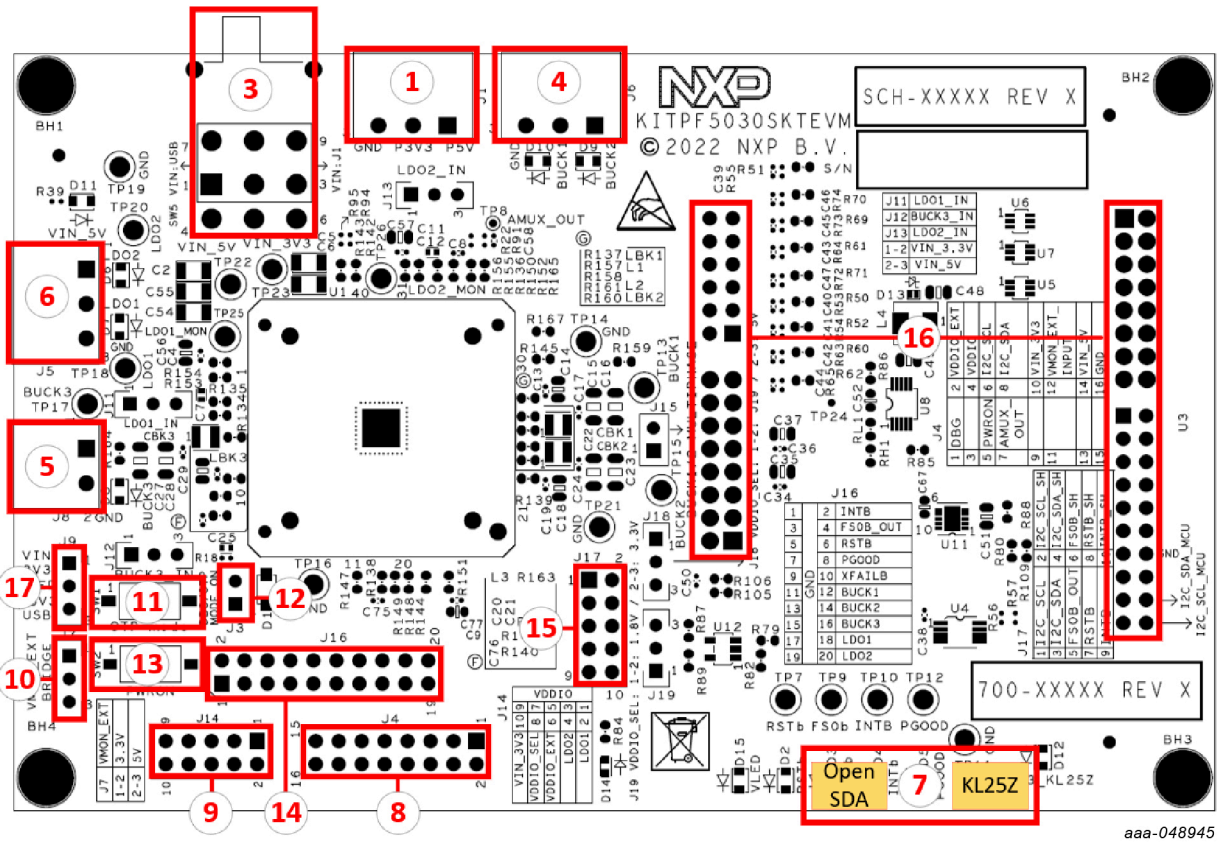

Figure 6. Evaluation board featured components location

Table 1. Evaluation board featured components location

Number	Description
1	VIN_5V and VIN_3V3 power supply input
3	VIN three position switch • Left position: VIN from USB • Middle position: board not supplied • Right position: VIN from J1
4	BUCK1/2 regulators output
5	BUCK3 regulator output
6	LDO1/2 regulators output
7	USB connectors (OpenSDA for MCU flash; KL25Z for NXP GUI control)
8	Debug connectivity. Access to PF5030 signals
9	VDDIO selection
10	VMON_EXT resistor bridge configuration (choice between monitoring 3.3 V or 5.0 V)
11	OTP mode switch
12	DBG pin to ground if unplugged

Table 1. Evaluation board featured components location*...continued*

Number	Description
13	PWRON pin switch
14	Signal debug connector
15	FRDM-KL25Z board signals connection
16	FRDM-KL25Z board connectors
17	VLED supply configuration

4.4.1 Connectors

Figure 7 shows the location of connectors on the board.

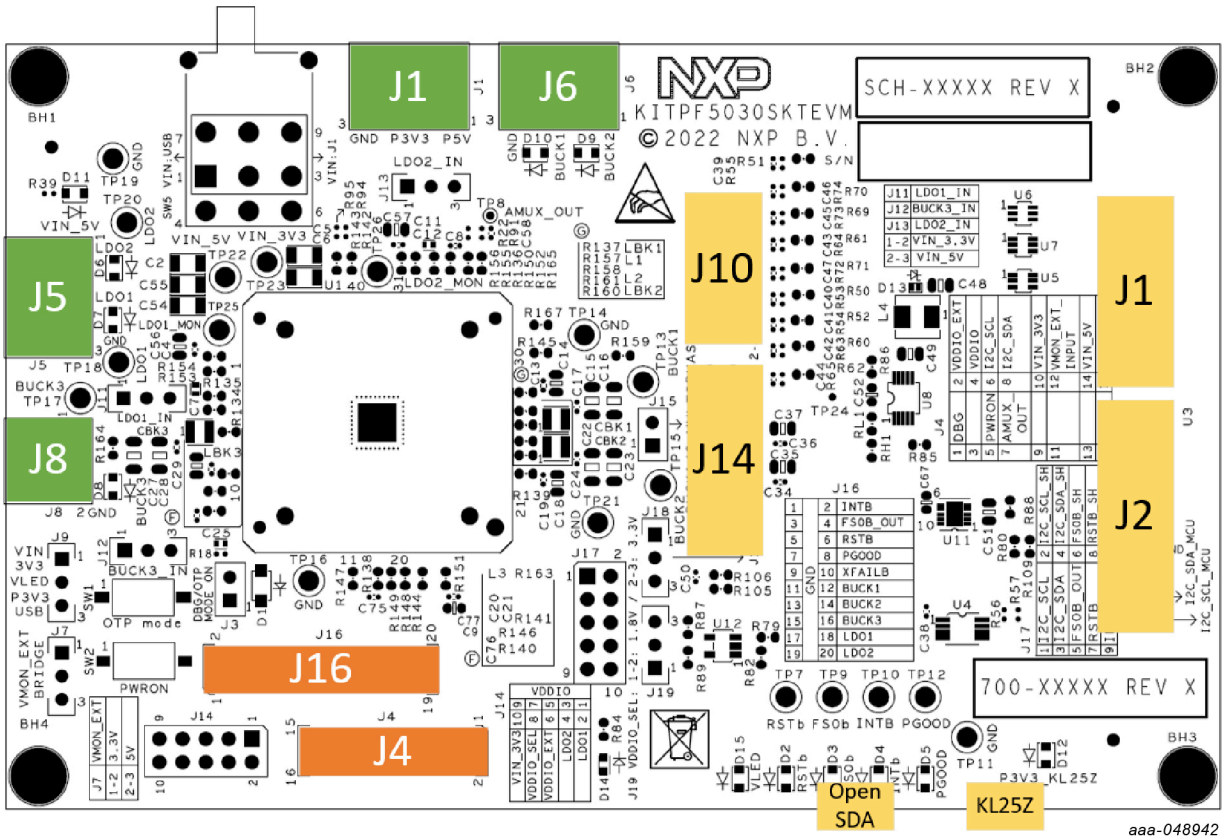

Figure 7. Evaluation board connectors location

4.4.1.1 VIN connector (J1)

Table 2. VIN_5V and VIN_3V3 connector (J1)

Schematic label	Signal name	Description
J1-1	VIN_5V	5 V voltage supply input
J1-2	VIN_3V3	3.3 V voltage supply input
J1-3	GND	Ground

4.4.1.2 Output power supply connectors

Table 3. LDO1/2 connector (J5)

Schematic label	Signal name	Description
J5-1	LDO2	LDO2 regulator output
J5-2	LDO1	LDO1 regulator output
J5-3	GND	Ground

Table 4. BUCK1/2 connector (J6)

Schematic label	Signal name	Description
J6-1	BUCK2	BUCK2 regulator output
J6-2	BUCK1	BUCK1 regulator output
J6-3	GND	Ground

Table 5. BUCK3 connector (J8)

Schematic label	Signal name	Description
J8-1	BUCK3	BUCK3 regulator output
J8-2	GND	Ground

4.4.1.3 Debug connector (J4)

Table 6. Debug connector (J4)

Schematic label	Signal name	Description
J4-1	n.c.	Not connected
J4-2	VDDIO_EXT	External VDDIO voltage supply
J4-3	INTB	Interrupt output pin (active low)
J4-4	n.c.	Not connected
J4-5	PWRON	PWRON input pin
J4-6	I2C_SCL	I^2C serial clock
J4-7	AMUX_OUT	Analog multiplexer output
J4-8	I2C_SDA	I^2C serial data
J4-9	n.c.	Not connected
J4-10	VIN_3V3	VIN_3V3 voltage supply
J4-11	n.c.	Not connected
J4-12	VMON_EXT_INPUT	VMON_EXT voltage divider input
J4-13	n.c.	Not connected
J4-14	VIN_5V	VIN_5V voltage supply
J4-15	n.c.	Not connected
J4-16	GND	Ground

4.4.1.4 Voltage monitoring connector (J16)

Table 7. Voltage monitoring connector (J16)

Schematic label	Signal name	Description
J16-1	GND	Ground
J16-2	INTB	Interrupt output pin (active low-logic level)
J16-3	GND	Ground
J16-4	FS0B_out	Fail-safe pin (active low-logic level)

Table 7. Voltage monitoring connector (J16)*...continued*

Schematic label	Signal name	Description
J16-5	GND	Ground
J16-6	RSTB	Reset input / output pin (active low-logic level)
J16-7	GND	Ground
J16-8	PGOOD	Power good output pin
J16-9	GND	Ground
J16-10	XFAILB	Power synchronization input/output with NXP low voltage PMIC
J16-11	GND	Ground
J16-12	BUCK1	BUCK1 regulator output
J16-13	GND	Ground
J16-14	BUCK2	BUCK2 regulator output
J16-15	GND	Ground
J16-16	BUCK3	BUCK3 regulator output
J16-17	GND	Ground
J16-18	LDO1	LDO1 regulator output
J16-19	GND	Ground
J16-20	LDO2	LDO2 regulator output

4.4.1.5 FRDM-KL25Z board connectors

Table 8. FRDM-KL25Z safety output connector (J1)

Schematic label	Signal name	Description
J1-1 to J1-9	n.c.	Not connected
J1-6	INTB_MCU	Interruption (active low-logic level)
J1-7	n.c.	Not connected
J1-8	RSTB_MCU	Reset (active low-logic level)
J1-9 to J1-11	n.c.	Not connected
J1-12	FS0b_MCU	Fail-safe (active low-logic level)
J1-13 to J1-16	n.c.	Not connected

Table 9. FRDM-KL25Z I^2C connector (J2)

Schematic label	Signal name	Description
J2-1 to J2-13	n.c.	Not connected
J2-14	GND	Ground
J2-15 to J2-17	n.c.	Not connected
J2-18	I2C_SDA_MCU	I^2C serial data line
J2-19	n.c.	Not connected
J2-20	I2C_SCL_MCU	I^2C serial clock line

Table 10. FRDM-KL25Z ADC connector (J10)

Schematic label	Signal name	Description
J10-1	BUCK2_ADC	BUCK2 regulator output to KL25Z ADC
J10-2	DBG_ADC	DBG pin voltage to KL25Z ADC
J10-3	BUCK1_ADC	BUCK1 regulator output to KL25Z ADC
J10-4	AMUX_ADC	AMUX pin to KL25Z ADC
J10-5	BUCK3_ADC	BUCK3 regulator output to KL25Z ADC
J10-6	LDO1_ADC	LDO1 regulator output to KL25Z ADC
J10-7	n.c.	Not connected
J10-8	LDO2_ADC	LDO2 regulator output to KL25Z ADC
J10-9	n.c.	Not connected
J10-10	VIN_ADC	VIN pin voltage to KL25Z ADC
J10-11	n.c.	Not connected
J10-12	VDDIO_ADC	VDDIO pin voltage to KL25Z ADC

Table 11. FRDM-KL25Z supply connector (J14)

Schematic label	Signal name	Description
J14-1 to J14-3	n.c.	Not connected
J14-4	P3V3_KL25Z	3.3 V generated from KL25Z
J14-5 to J14-7	n.c.	Not connected
J14-8	P3V3_KL25Z	3.3 V generated from KL25Z
J14-9	n.c.	Not connected
J14-10	P5V_KL25Z	5.0 V generated from USB
J14-11	n.c.	Not connected
J14-12	GND	Ground
J14-13	n.c.	Not connected
J14-14	GND	Ground
J14-15	n.c.	Not connected
J14-16	n.c.	Not connected

Table 12. FRDM-KL25Z USB connectors

Schematic label	Signal name	Description
KL25Z	NA	USB connector used to communicate with the PF5030 part
OpenSDA	NA	USB connector used to flash the KL25Z MCU

4.4.2 Test points

Figure 8 shows test points that provide access to various signals to and from the boards.

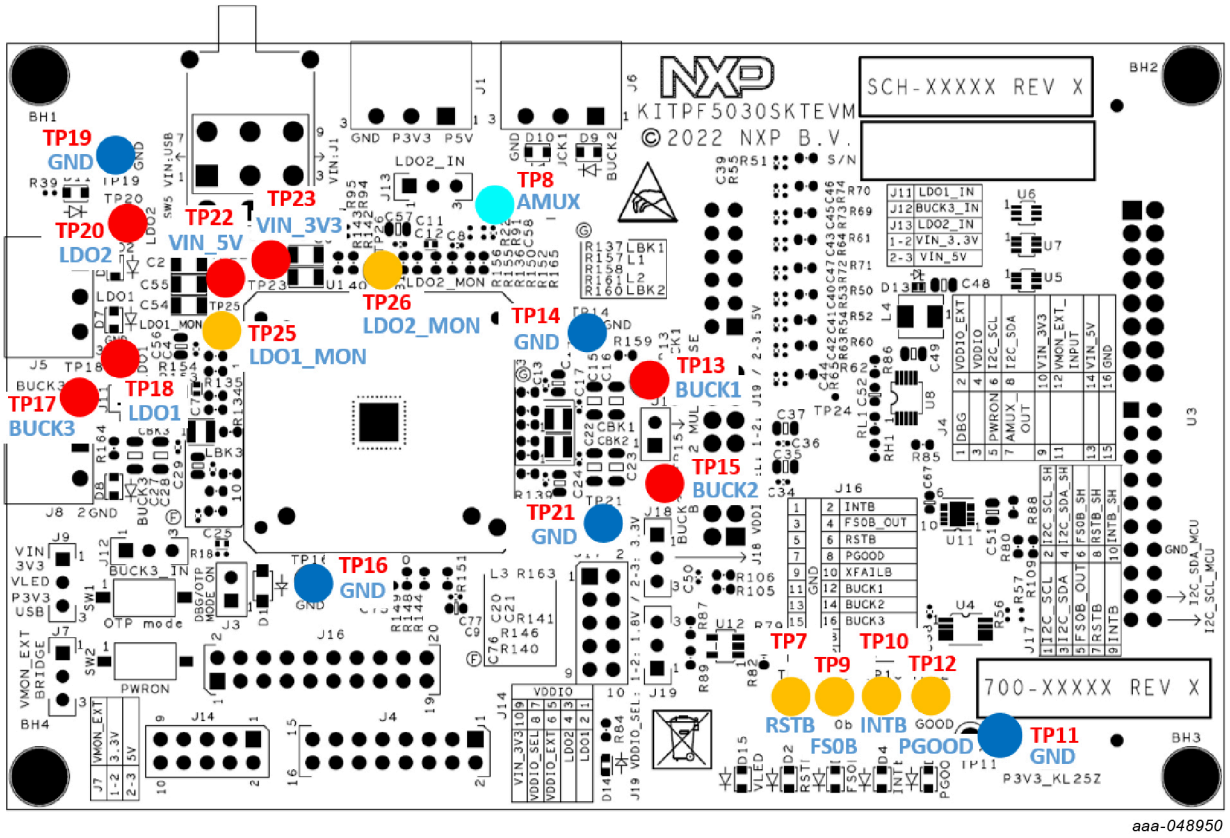

Figure 8. Evaluation board test points

Table 13. Evaluation board test points description

Test point name	Signal name	Description
TP7	RSTB	Reset pin (active low)
TP8	AMUX	Analog multiplexer output
TP9	FS0B	Fail-safe pin (active low)
TP10	INTB	Interruption pin (active low)
TP12	PGOOD	Power good pin (active high)
TP13	BUCK1	BUCK1 regulator output
TP15	BUCK2	BUCK2 regulator output
TP17	BUCK3	BUCK3 regulator output
TP18	LDO1	LDO1 regulator output
TP20	LDO2	LDO2 regulator output
TP22	VIN_5V	VIN pin voltage
TP23	VIN_3V3	BUCK1/2_IN pin voltage
TP25	LDO1_MON	LDO1_MON pin voltage
TP26	LDO2_MON	LDO2_MON IN pin voltage
TP11, TP14, TP16, TP19, TP21	GND	Ground

4.4.3 Jumpers

Figure 9 shows jumper locations for board configuration.

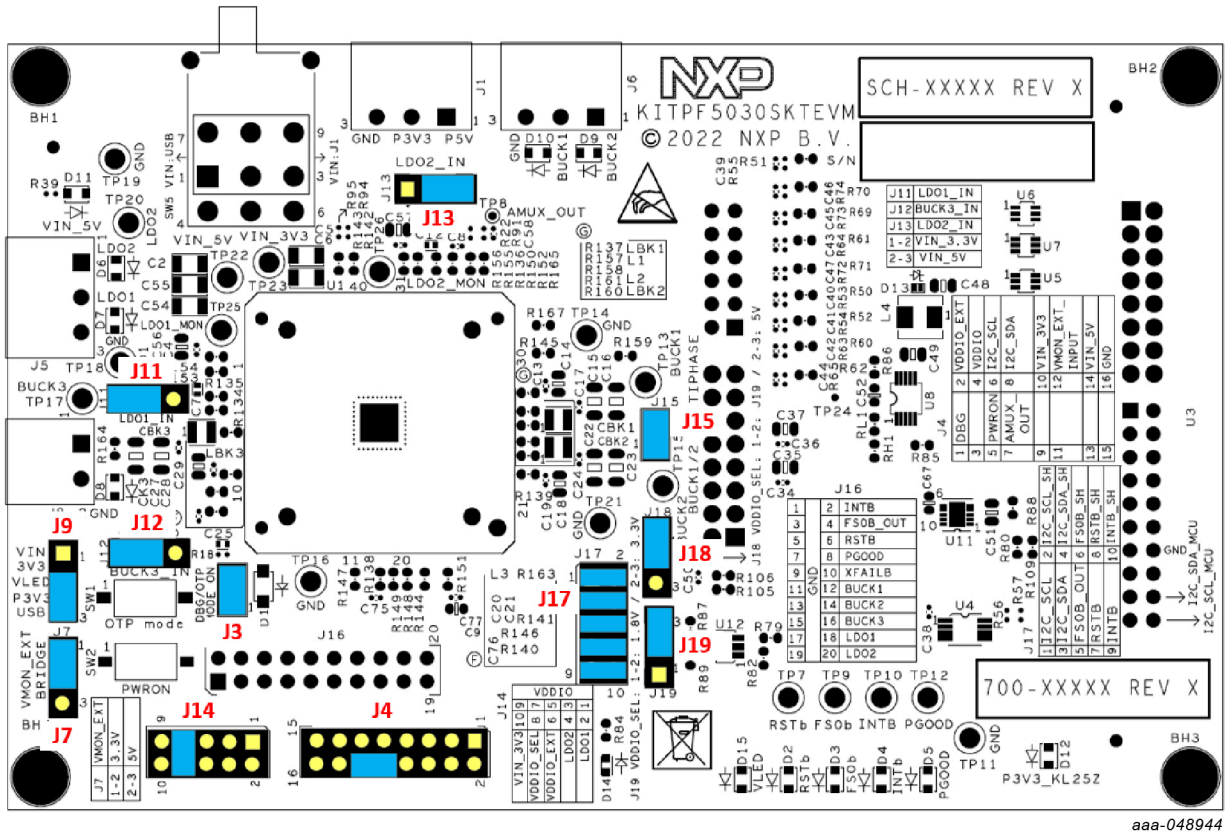

Figure 9. Evaluation board jumpers location (with default position)

Table 14. Evaluation board jumpers description

Name	Function	Pin number	Description
J3	Apply voltage to DBG pin	1–2	Either 4.5 V (DBG mode) or 7.95 V (OTP mode). See SW1 position
J4	VMON_EXT input selection	10–12	VIN_3V3
		12–14	VIN_5V
J7	VLED selection	1–2	VIN_3V3
		2–3	P3V3_KL25Z
J9	VMON_EXT resistor bridge selection	1–2	Monitors 3.3 V
		2–3	Monitors 5.0 V
J11	LDO1 input	1–2	LDO1_IN tied to VIN_3V3
		2–3	LDO1_IN tied to VIN_5V
J12	BUCK3 input	1–2	BUCK3_IN tied to VIN_3V3
		2–3	BUCK3_IN tied to VIN_5V
J13	LDO2 input	1–2	LDO2_IN tied to VIN_3V3
		2–3	LDO2_IN tied to VIN_5V

Table 14. Evaluation board jumpers description*...continued*

Name	Function	Pin number	Description
J14	VDDIO input	1−2	VDDIO tied to LDO1
		3-4	VDDIO tied to LDO2
		5-6	VDDIO tied to VDDIO_EXT
		7-8	VDDIO tied to VDDIO_SEL
		9-10	VDDIO tied to VIN_3V3
J15	BUCK1/2 multiphase	1−2	BUCK2 tied to BUCK1
J17	I^2C and safety IOs connection to FRDM-KL25Z	1-2	I^2C SCL
		3-4	I^2C SDA
		5-6	FS0B_out
		7-8	RSTB
		9-10	INTB
J18	VDDIO_SEL selection A	1−2	See J19
		2−3	VDDIO_SEL voltage @ 5.0 V
J19	VDDIO_SEL selection B	1−2	VDDIO_SEL voltage @ 1.8 V
		2−3	VDDIO_SEL voltage @ 3.3 V

4.4.4 LED signaling

Figure 10 shows the LEDs provided as visual output devices for the evaluation board:

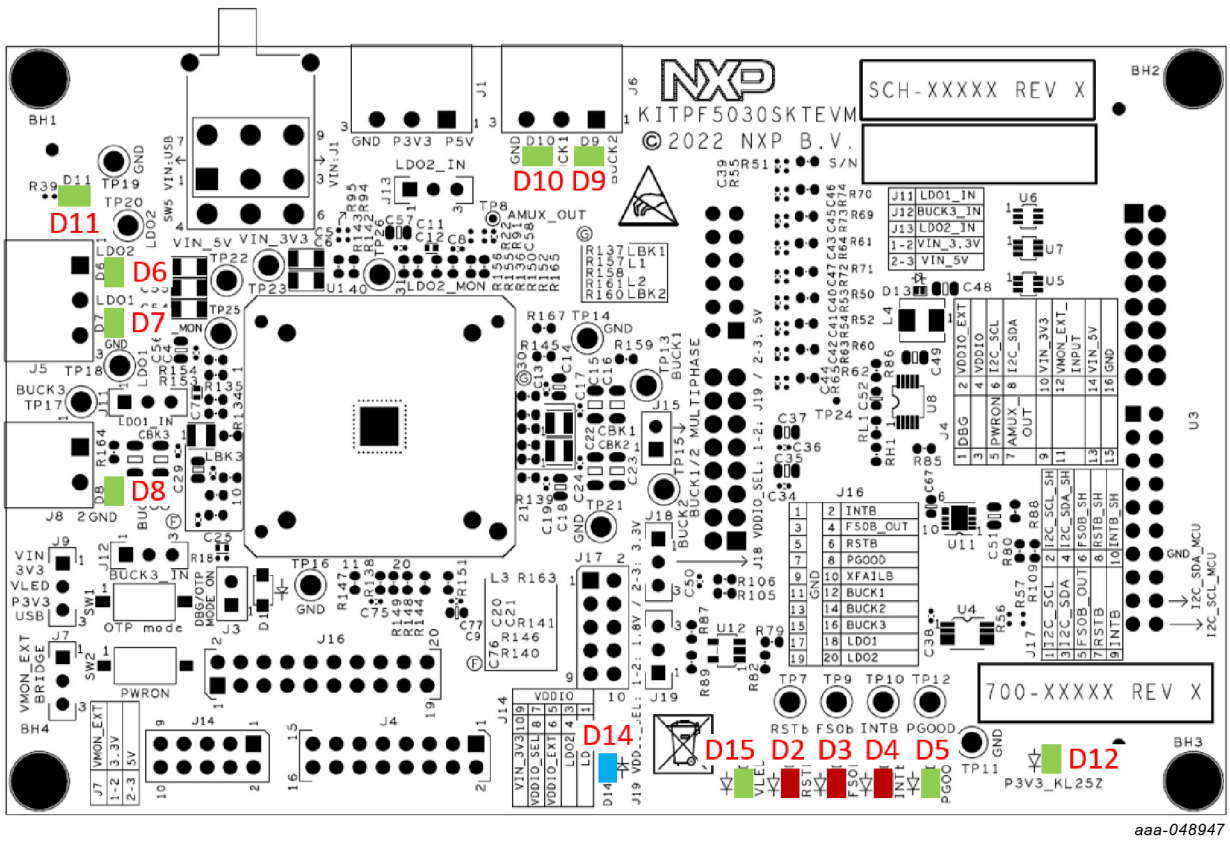

Figure 10. Evaluation board LED signaling location

Table 15. Evaluation board LED signaling description

Label	Name	Color	Description
D2	RSTB	Red	RSTB asserted (low-logic level)
D3	FS0B	Red	FS0B asserted (low-logic level)
D4	INTB	Red	INTB asserted (low-logic level)
D5	PGOOD	Green	PGOOD released
D6	LDO2	Green	LDO2 ON
D7	LDO1	Green	LDO1 ON
D8	BUCK3	Green	BUCK3 ON
D9	BUCK2	Green	BUCK2 ON
D10	BUCK1	Green	BUCK1 ON
D11	VIN_5V	Green	VIN_5V ON
D12	P3V3_KL25Z	Green	P3V3_KL25Z ON
D14	DBG ≥ 7.85 V	Blue	DBG pin voltage ≥ 7.85 V (OTP programming)
D15	VLED	Green	VLED ON

4.4.5 Switches

Figure 11 and Figure 12 show switches locations for board operation.

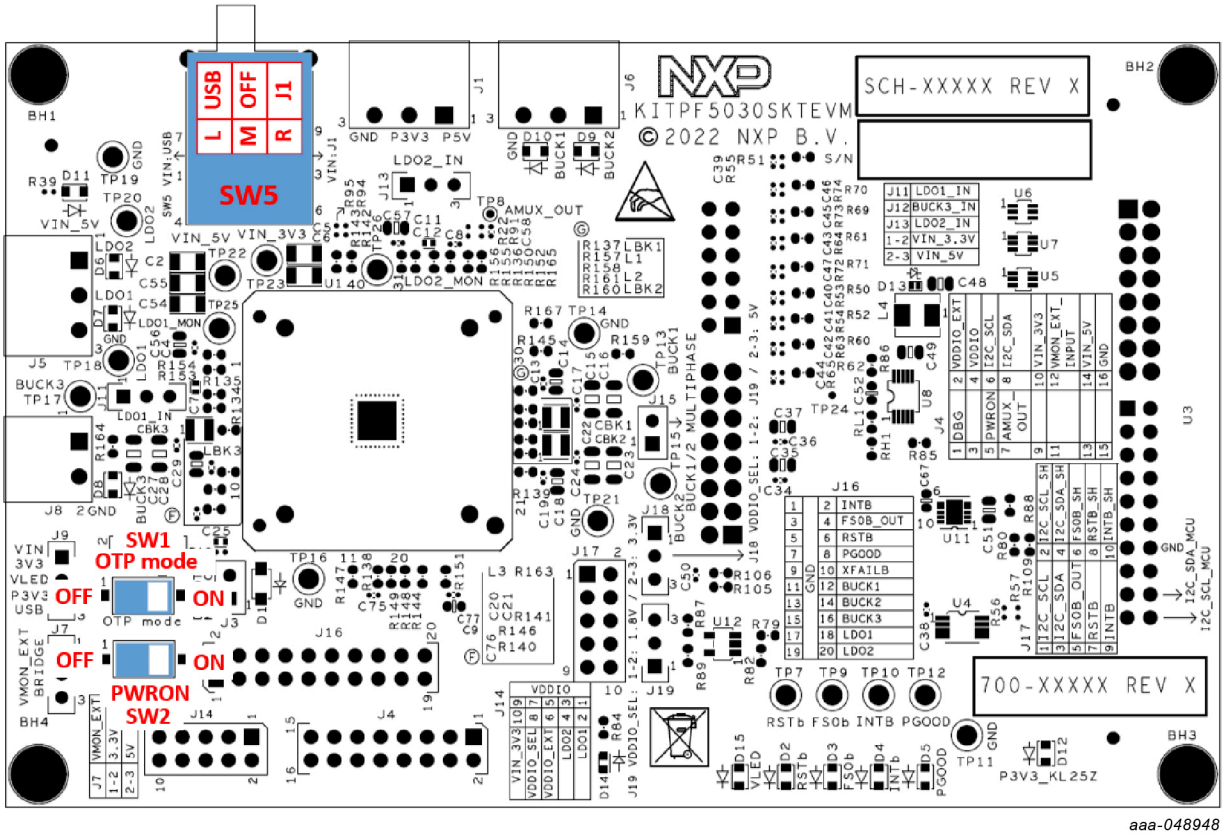

Figure 11. Switches location top

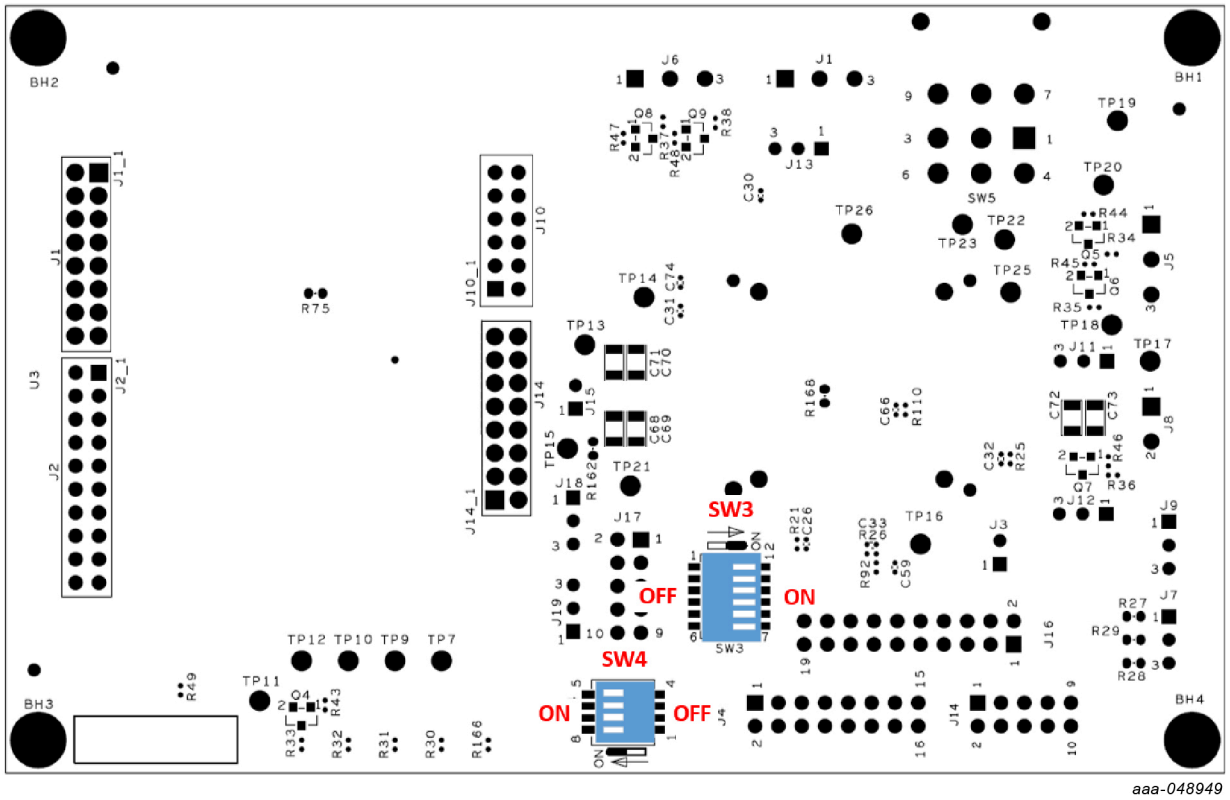

Figure 12. Switches location bottom

Table 16. SW1 description

Position	Function	Description
RIGHT	OTP mode ON	PF5030 OTP can be emulated and programmed when J3 populated
LEFT	OTP mode OFF	PF5030 OTP cannot be emulated and programmed

Table 17. SW2 description

Position	Function	Description
RIGHT	PWRON pin high	PF5030 can power up
LEFT	PWRON pin low	PF5030 cannot power up

Table 18. SW3 description

Switch number	Line	LED	Description
1	VIN_5V	D11	Each LED is connected through an independent switch. Disconnecting them allows more accurate efficiency measurement. The switches also disconnect the FRDM-KL25Z ADC inputs.
2	BUCK1	D10	
3	BUCK2	D9	
4	BUCK3	D8	
5	LDO1	D7	
6	LDO2	D6	

Table 19. SW4 description

Switch number	Line	LED	Description
1	PGOOD	D5	Each LED is connected through an independent switch. Disconnecting them allows more accurate efficiency measurement. The switches also disconnect the level shifters to the FRDM-KL25Z inputs.
2	INTB	D4	
3	FS0B	D3	
4	RSTB	D2	

Table 20. SW5 description

Position	Function	Description
RIGHT	VIN ON	PF5030 supplied from USB
MIDDLE	VIN OFF	PF5030 not supplied
LEFT	VIN ON	PF5030 supplied from J1

5 Installing and configuring software and tools

The programming/evaluation boards are always delivered with the GUI firmware already flashed. If MCU firmware is already flashed, ignore this section. If it is specified that firmware must be updated or it is malfunctioning, follow these instructions.

5.1 Flashing or updating the FRDM-KL25Z GUI firmware

If bootloader is already loaded in the FRDM-KL25Z board, steps 1-3 are not required. Start from step 4.

1. Disable the Storage Service and Windows Search: Run Services, double click, and stop them as shown in Figure 13.

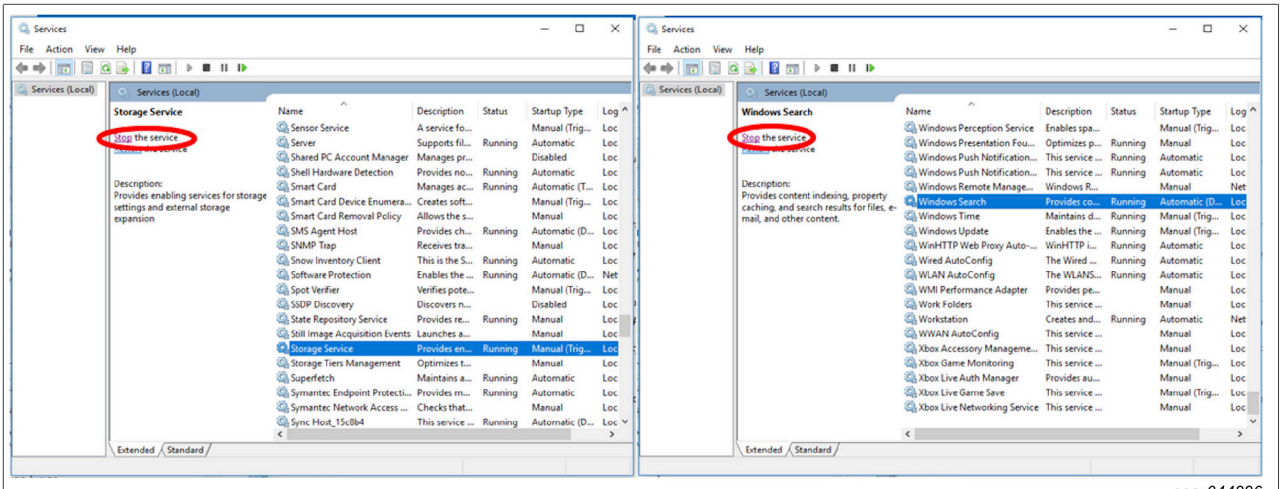

Figure 13. Services configuration

2. Press the RST push button and connect the USB cable to the SDA port on the FRDM-KL25Z board.
   - A new “bootloader” device appears on the left pane of the file explorer
3. Drag and drop the file “MSD-DEBUG-FRDM-KL25Z_Pemicro_v118.SDA” to the bootloader drive
   Ensure that there is enough time for the firmware to be saved in the bootloader
4. Disconnect the USB cable, then reconnect it to the SDA port **WITHOUT** pressing the RST push button
   - This time, FRDM_KL25Z device appears on the left pane of the file explorer as in Figure 14.

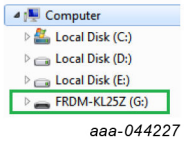

Figure 14. FRDM-KL25Z in left pane

5. Locate the file “nxp-gui-fw-frdmkl25z-usb_hid-device_<version>.bin” from the package. Drag and drop this file into the FRDM_KL25Z device.
   Ensure that there is enough time for the firmware to be saved.
6. Freedom board firmware is successfully loaded. Disconnect the USB-cable and reconnect it to the KL25Z USB port.

5.2 Installing NXP GUI software package

To install the "NXP GUI for Automotive PMIC Families" or obtain the NXP GUI package, unzip an open "1 - NXP_GUI_Setup" folder as shown in Figure 15.

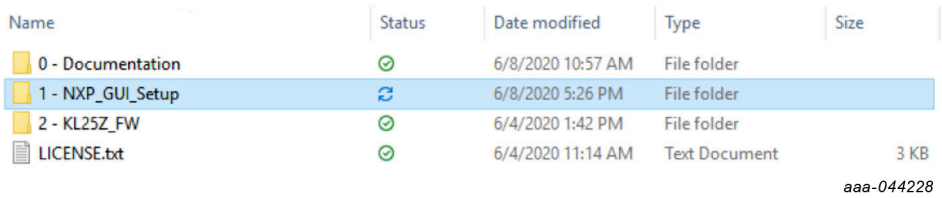

Figure 15. NXP_GUI_Setup folder

Then double click on the "NXP_GUI-version-Setup.exe" shown in Figure 16 and follow the instructions.

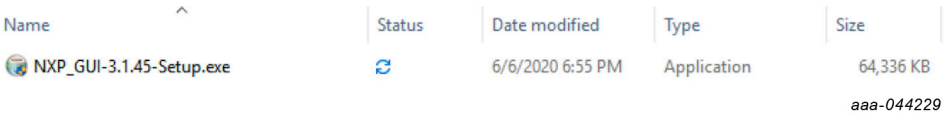

Figure 16. NXP_GUI_version_Setup.exe

To install the application on Windows PC, proceed with the pop-up windows shown in Figure 17 and Figure 18.

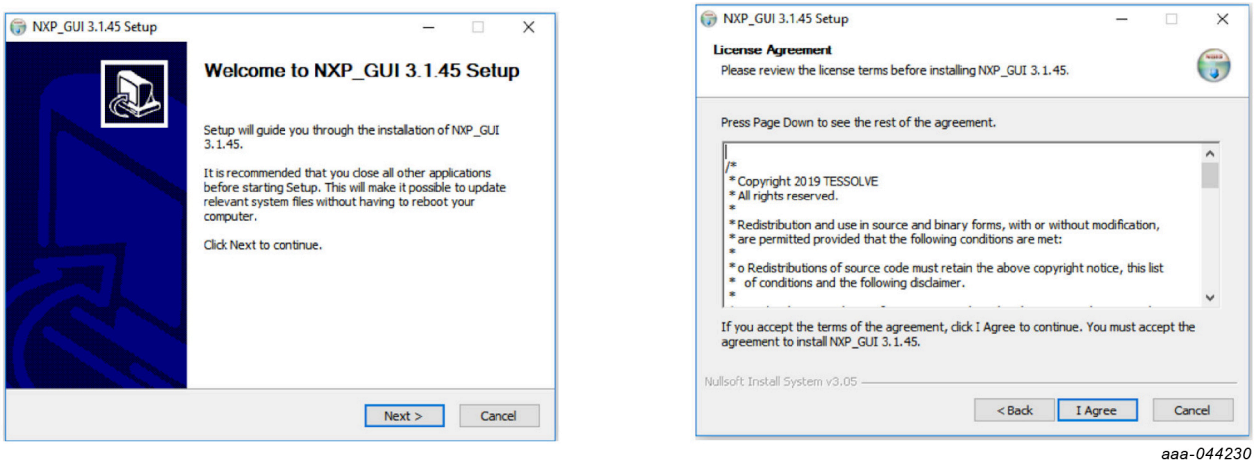

Figure 17. NXP GUI setup 1/2

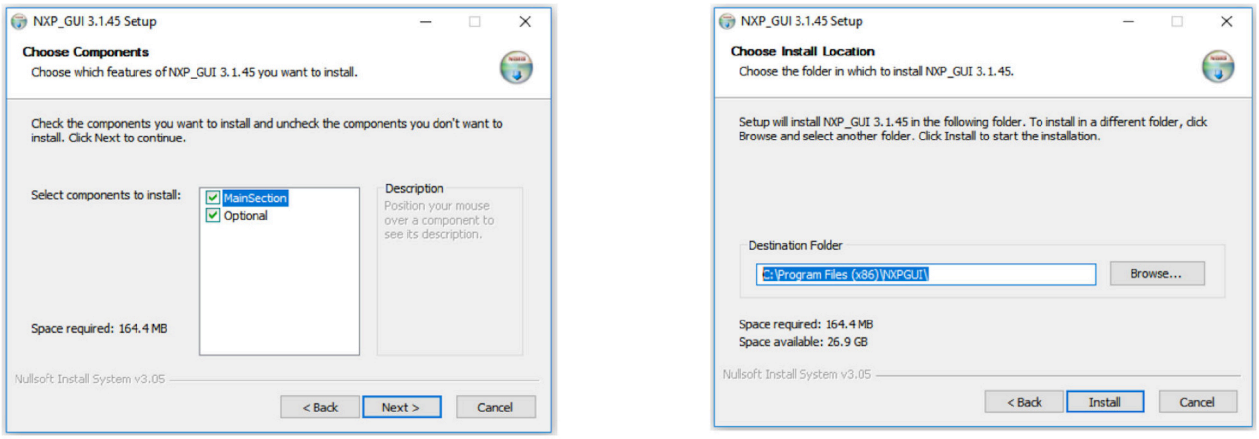

Figure 18. NXP GUI setup 2/2

Select the options shown in Figure 19 before completing the installation of the setup:

- Run NXP_GUI
- Show Readme

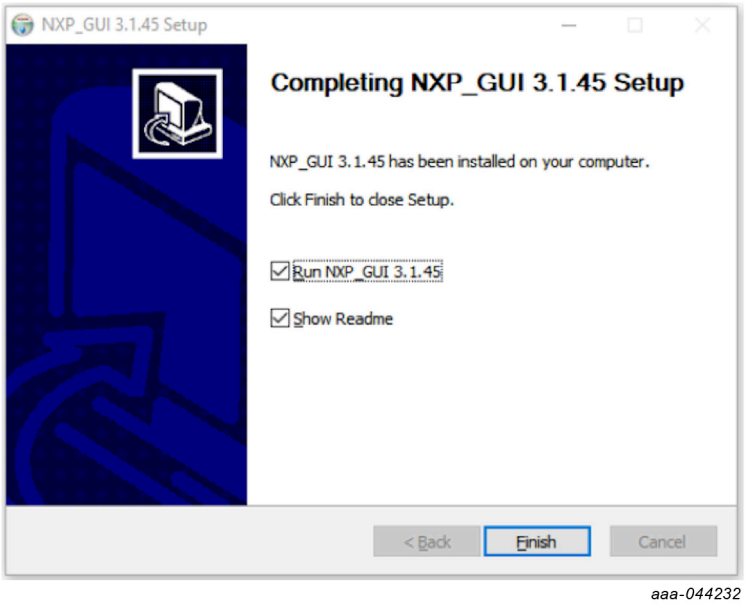

Figure 19. NXP GUI setup completion

Select **Finish** to complete the installation.

When installation is finished, you can search the application on the Windows search bar as “NXPGUI”. Click to launch.

6 Using PF5030 NXP GUI

To follow the steps in this section, ensure that the board is connected using the appropriate hardware configuration.

Always use the latest version of the NXP GUI.

6.1 Starting the PF5030 NXP GUI

When your kit is ready and the NXP GUI is installed, click to launch the GUI from your Windows search bar. When the kit selection window appears, as shown in Figure 20, select PF5030.

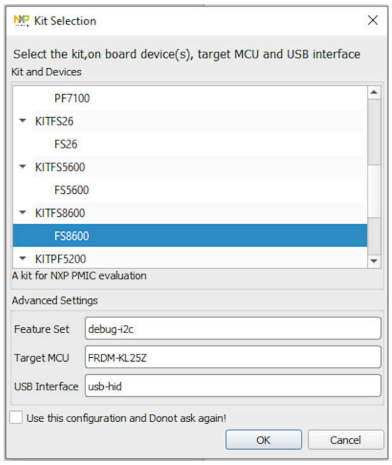

Figure 20. Kit selection window

To avoid the kit selection window on every launch, you can check the box “Use this configuration and do not ask again”. The window shown in Figure 21 opens.

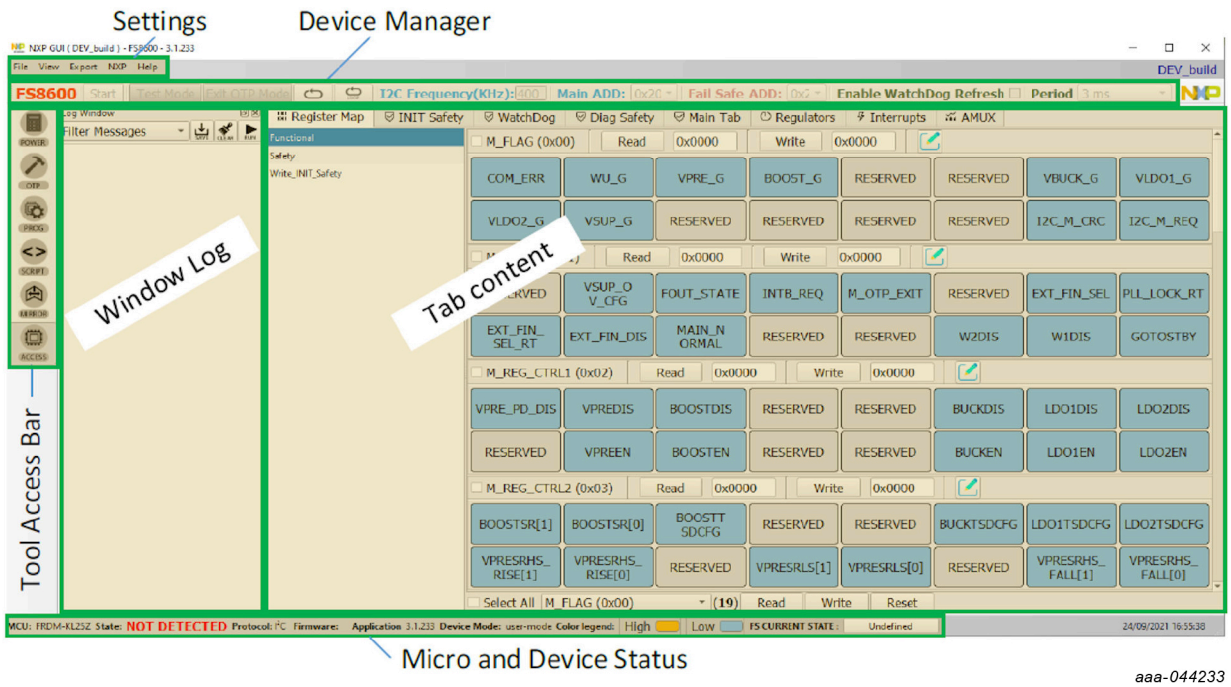

Figure 21. NXP GUI framework

You are now using the PF5030 GUI interface. It can be divided in several parts:

- **Settings:** Import or export files, configure framework.
- **Device Manager:** Start communication with device. Enter or exit test mode. I^2C communication settings.
- **Tool Access Bar:** Quick access to the PF5030 evaluation tools and features.
- **Window Log:** Microcontroller and device communication events.
- **Tab Content:** Content of each tool or tab. There can be more tabs, boxes, or windows.
- **Micro and Device Status:** Indicates if the computer USB is connected to the kit. Displays firmware and GUI version. Displays the current state of the fail-safe state machine. Click Display button to refresh.

Note: *The tool access bar shows the GUI tools in the sequence that they must be used. The first step is to verify device POWER dissipation and then configure the OTP. When the power is verified and OTP is done, the device can be programmed or emulated with a SCRIPT. MIRROR registers can be read/modified to a configuration validation. To verify states and configure safety reactions, the Access tab allows registers handling.*

6.2 Power tab

The POWER tool allows the calculation of power management power dissipation.

User must start by setting or importing an OTP configuration to preset all regulators, then entering the current consumption of each rail.

As PF5030 can be supplied by more than one voltage rail, two input supply rails can be set on "INPUT PARAMETERS" group. Once the voltages are set, each regulator must be associated to one of those rails. The voltages set are used to calculate the power dissipation. The calculated absorbed input currents are assigned to the associated rail.

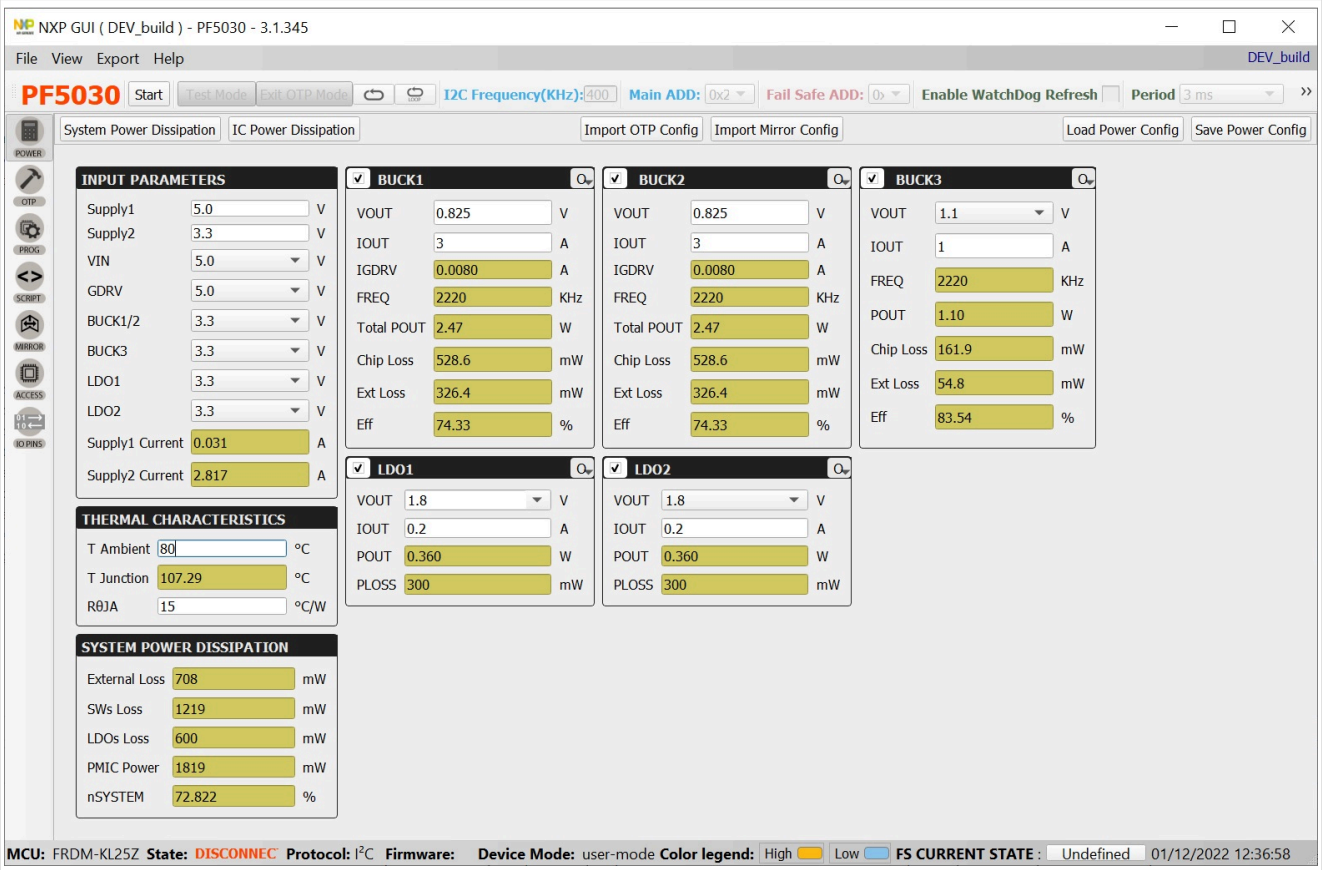

Figure 22. NXP GUI framework - POWER tab

Each regulator can be enabled / disabled by clicking on the upper left corner check box.

Additional options are available on the menu on the upper right corner of each regulation, such as:

- **Operation mode**: Single or multiphase, regulator or load switch
- **Component selection**: input / output capacitors, inductor and DCR. DCR is automatically changed based on inductor value and can be reedited
- **Advanced parameters**: detailed losses summary
- **Efficiency chart**: regulator losses / output current plot at current junction temperature
- **Power chart**: regulator losses partition

6.3 OTP tab

The OTP tool allows the configuration of OTP registers and generates scripts for OTP emulation or OTP programming. These scripts program parameters that the main state machine and the fail-safe state machine control.

At the right side, fill **Customer Details** and **Program Details** sub-windows. Set **Device Core ID** and **Device Type** for device pre-configuration.

The OTP tool includes the following tabs:

- System Configuration
- Switching and LDO Regulators
- Functional Safety

These tabs are used to define the entire PF5030 OTP configuration.

When the OTP configuration is defined, TBB/OTP scripts can be generated using the Export menu. Generate a TBB file for emulation and an OTP file for OTP programming.

It is possible to save a configuration to use or modify it later. To export the OTP configuration, click "Save Config". To import a configuration initially saved from the OTP tool or the Mirrors tab, click the Import button.

6.3.1 System configuration tab

The system configuration tab has several sections, divided into two groups. The first group is related to OTP configuration itself:

- **System Configuration**: I^2C addresses, VIN threshold, program ID, fault retry management, regulator assignment
- **Clock and Synchronization**: Clock modulation, XFAILB synchronization
- **VMON OV Deep Fail-safe Reaction**: configures device reaction when OV event is detected.
- **Power Sequence Configuration**: This box is used to define the power sequence of the device and device reaction when TSD happens. If the configuration is modified, the power-up sequence graph is updated automatically.

Figure 23 shows an OTP configuration example.

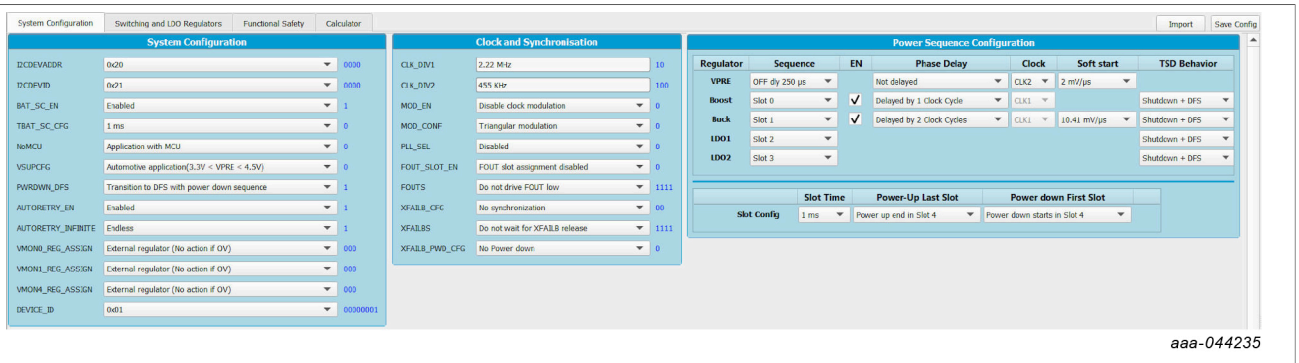

Figure 23. OTP System Configuration Tab, part 1 of 2: OTP configuration

The second group is related to VMON board connection and startup sequence diagram:

- Voltage monitoring recap for power-up sequence diagram drawing: This box is NOT related to the OTP configuration. It allows the definition of an assignment between the VMONx and the regulators to plot the power-up sequence graph. It does not configure any registers. It is only used as information. It is saved as comment on the configuration script.
- Power-up sequence diagram: This diagram reflects the power-up sequence of the PF5030 depending on the OTP configuration. To plot the associated configuration, it uses the “Voltage Monitoring Recap”. The power-up sequence timing may not be 100 % accurate. If shown, the RSTB, the FOUT, and the XFAILB voltages are different from 3.3 V to differentiate between the different curves.

Figure 24 shows a voltage monitoring recap connection and the resulting power-up sequence diagram.

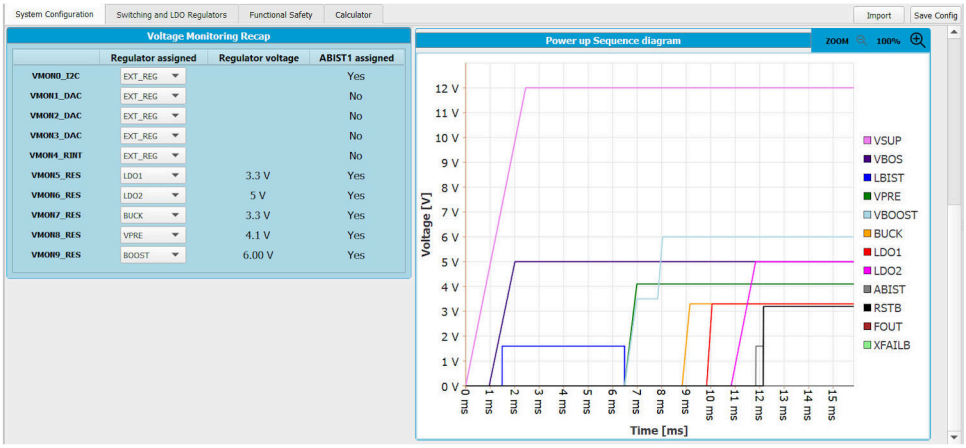

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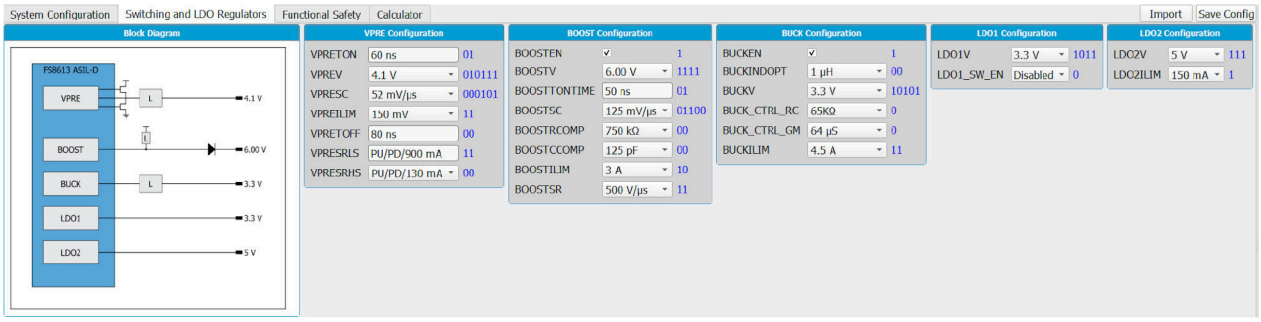
Figure 24. OTP System Configuration tab, part 2 of 2: Power-up sequence diagram

6.3.2 Switching and LDO regulators tab

The switching and LDO Regulators tab shown in Figure 25 has several sections:

- **Block diagram**: Summarizes the output voltage and startup slot of each regulator
- **SMPSs configuration**: Switching Mode Power Supplies configuration.
- **LDOs configuration**: Linear dropout regulators configuration



aaa-044237

Figure 25. OTP SMPS and LDO regulators Configuration tab

6.3.3 Functional safety tab

The functional safety tab shown in Figure 26 has several sections:

- **System Safety Configuration**: Watchdog, RSTB, PGOOD, safety path, SVS clamp
- **Voltage Monitoring**: Define the voltage monitoring configuration. Some protections have been implemented to avoid OTP configuration issue.

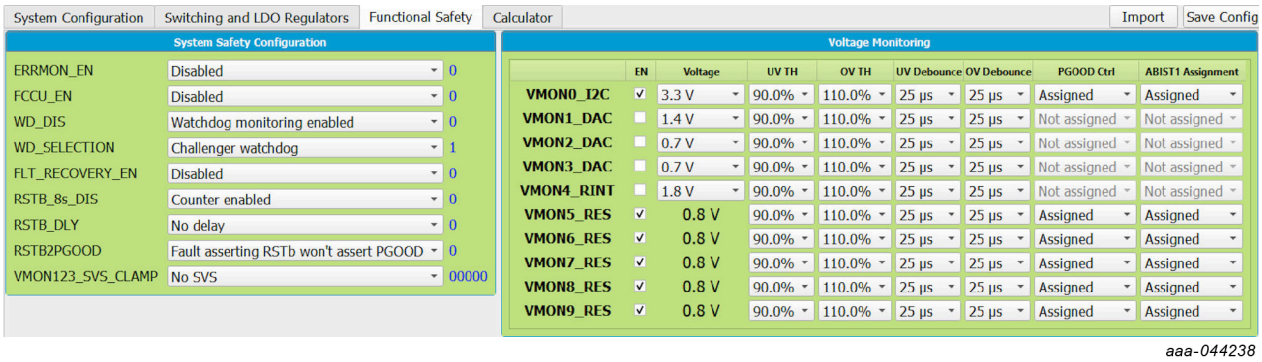
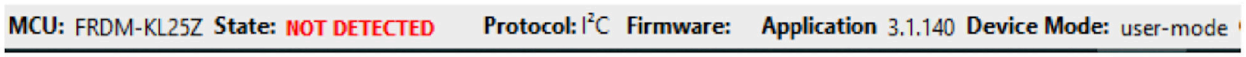


Figure 26. OTP Functional Safety tab

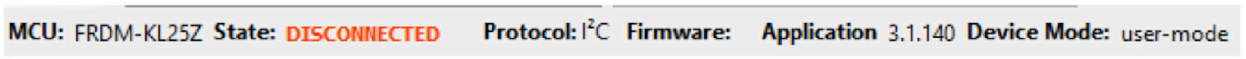
6.4 Establishing the connection between the NXP GUI and the hardware

The device manager allows the connection of the PF5030 development board with the NXP GUI.

Before plugging the KL25Z USB port to the computer, the MCU is in a “NOT DETECTED” state.



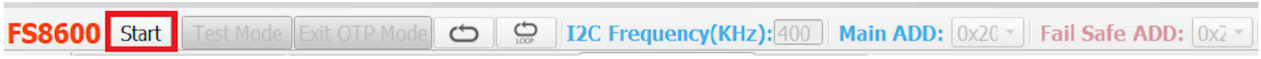
After plugging in the USB, the MCU state changes to “DISCONNECTED.” **If the state does not change, press the RST button on the freedom board.**



At this state, the communication with the MCU can be started.

The MCU state changes to “CONNECTED” and the firmware version is displayed.

To start the communication with the PF5030, click the "Start" button. The GUI is able to identify the device address to establish the communication.



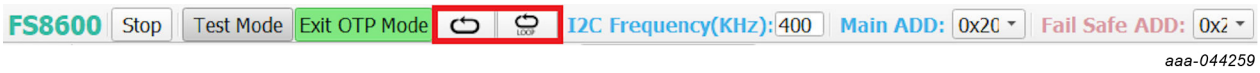
When the communication has started successfully, the PF5030 (device name) switches to green.

When the device starts with the DBG pin voltage at 7.95 V (EVB OTP mode LED on), the state machine stops at the Main/FS OTP MODE state.

The current mode can be read using the refresh button and loop refresh button highlighted in red. Clicking refresh reads the state one time. Clicking the loop refresh latches and reads the state periodically until a new click deactivates it.

When the “Exit OTP mode” button is green, the device is in OTP mode. When in OTP mode, device I²C register addresses are the default values 0x20 for main and 0x21 for fail-safe. An "Exit OTP mode" button click sends

commands to the main state and the fail-safe state machine to exit OTP mode and initiate device start-up. The addresses are automatically updated to keep device communication.



Test mode can be enabled and disabled by clicking the Test Mode button when DBG pin voltage is 7.95 V (EVB OTP mode LED on). When the button is green, Test mode is activated. The button state can also be refreshed by clicking the arrow loop buttons.

Figure 27. GUI and device in test mode

The current device mode (user / test) is shown on the device status bar.

Test mode can be entered when device is not in OTP mode.

When in OTP mode, the device is necessarily in Debug mode.

6.5 OTP mode and device programming

Device enters OTP mode when the DBG pin voltage is set to 7.95 V before start-up. The OTP mode consists of a device state machine stop at Main/FS OTP MODE states. When in Main/FS OTP mode states, the I^2C addresses are 0x20 for main and 0x21 for fail-safe. The Main/FS OTP mode states are left when one of these conditions is met:

- Imposing DBG pin voltage inferior to 5.5 V
- Sending Main/FS OTP mode exit command through I^2C
- Clicking NXP GUI button "Exit OTP Mode"

The NXP GUI is able to identify these addresses automatically from the device.

Then, the device addresses are set based on the mirror registers values. User can only change these addresses in the mirror register in Test mode.

6.5.1 Device programming

The Device Programming tab shown in Figure 28 allows OTP device programming using a file initially generated by the OTP tool. This tab is only available when **Test mode** is active.

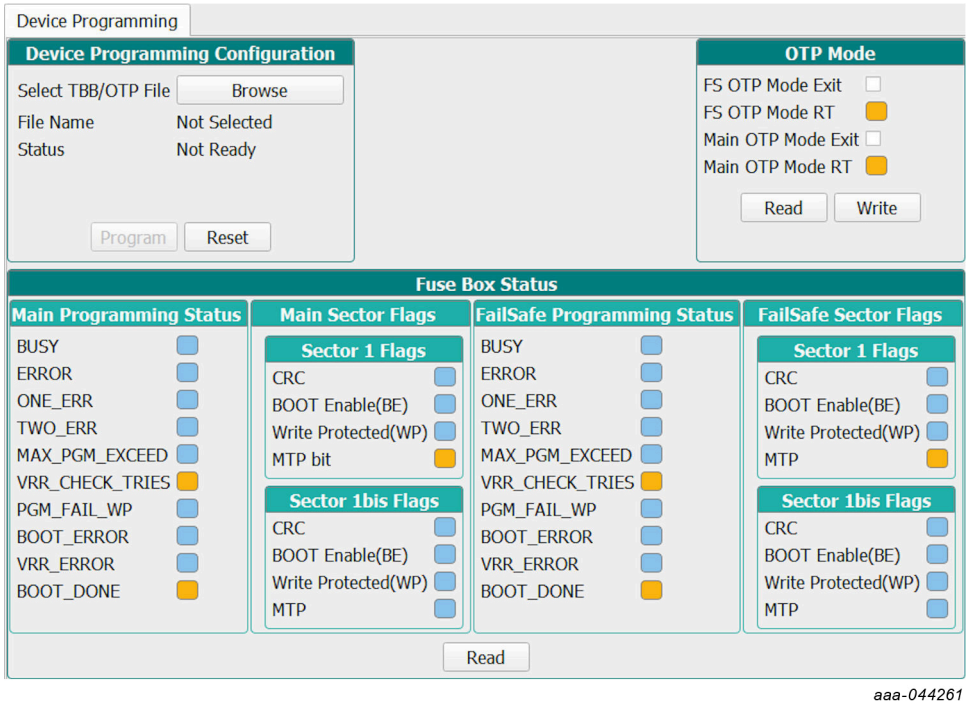


Figure 28. Device programming

To set up the hardware before OTP burning, see Section 7.3 configure put device in OTP mode, then follow the steps:

- Start the device in **OTP mode**.
- Enter **Test mode**.
- Browse and load the script file you want to burn (OTP or TBB type).
- The program button is available.
- Click **Program**.

Before programming, the GUI verifies if the DBG pin voltage is 7.95 V.

If the DBG pin voltage is less than 7.95 V, a pop-up window is shown requiring to turn on the 7.95 V. The blue LED on the board indicates that an 7.95 V voltage is available on the DBG pin. At the end of the first OTP programming, the MTP index = 1, WP, BE, and CRC flags are orange.

The Main/Fail-safe sector flags provide the OTP fuse status, as shown in Table 21. It helps to determine how many times the part was burned.

Table 21. OTP burning flag status

OTP burning step	Sector	BE	WP	CRC	MTP index
mirrors empty, OTP not burned	1	blue	blue	blue	orange
	1bis	blue	blue	blue	blue
mirrors filled, OTP not burned	1	blue	blue	orange	orange
	1bis	blue	blue	orange	blue
OTP burned once	1	orange	orange	orange	orange
OTP burned twice	1bis	orange	orange	orange	orange

The example shown in Figure 28 corresponds to the OTP not burned, mirrors empty line in Table 21.

To check if a valid OTP configuration is already burned, switch off the supply and then on again. Start the device by clicking the "Exit OTP Mode" button. The device starts with the OTP configuration.

6.6 User mode controls

The device operation is called **User mode** when the Main/FS state machines are not in OTP MODE state and not in Test Mode. In this mode, the main/fail-safe addresses come from mirror registers / fused OTP.

When using the EVB, the voltages on device pins can be verified in ACCESS > AMUX > ADC Measurements (see Section 6.6.3.9).

6.6.1 Working with the script editor

The register and OTP emulation can be configured with the script editor shown in Figure 29. The script editor is useful for trying various OTP configurations in OTP mode.

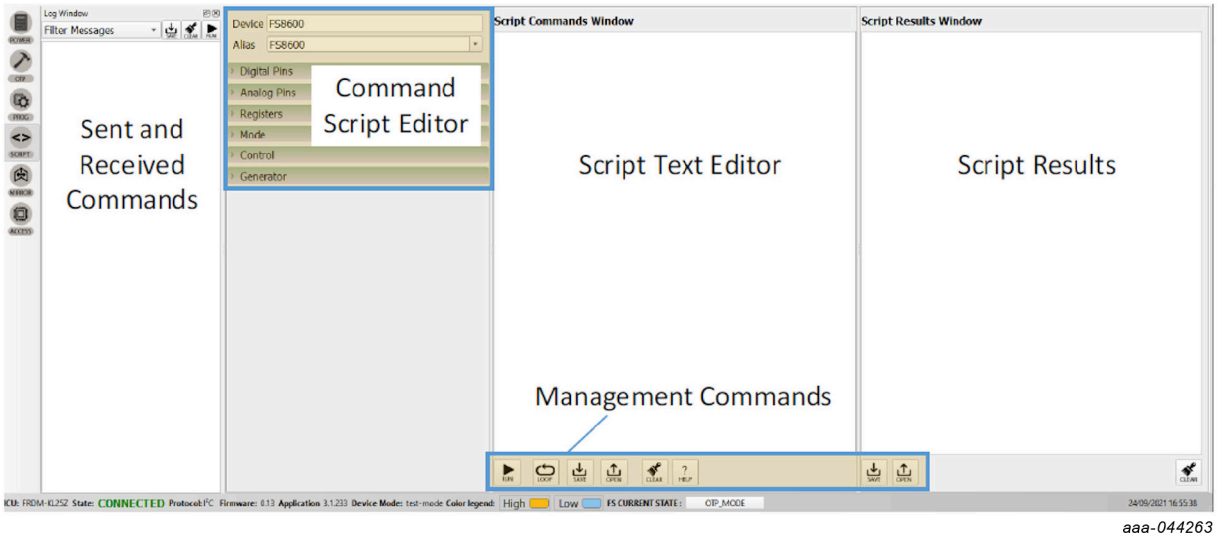


Figure 29. Script editor

The main subareas of this panel are:

- **Command Script Editor**: Builds commands to be sent to the device.
- **Script Text Editor**: Sends a sequence of register configurations from a text file or from a command edited directly in this area.
- **Script Results**: Displays result status of each command sent to the device.
- **Sent and Received Commands**: Displays a summary of commands sent and received from the device.
- **Management Commands**: Used for scripts.

6.6.1.1 Command script editor

Using the script editor, you can execute any command either directly or from a file. It is also possible to save and modify a script. Using the brush symbol, it is possible to clean windows if necessary.

All commands must follow a specific syntax. The Help menu describes the commands available in the script editor and the syntax to be used.

Figure 30 shows an example of building a command from the panel.

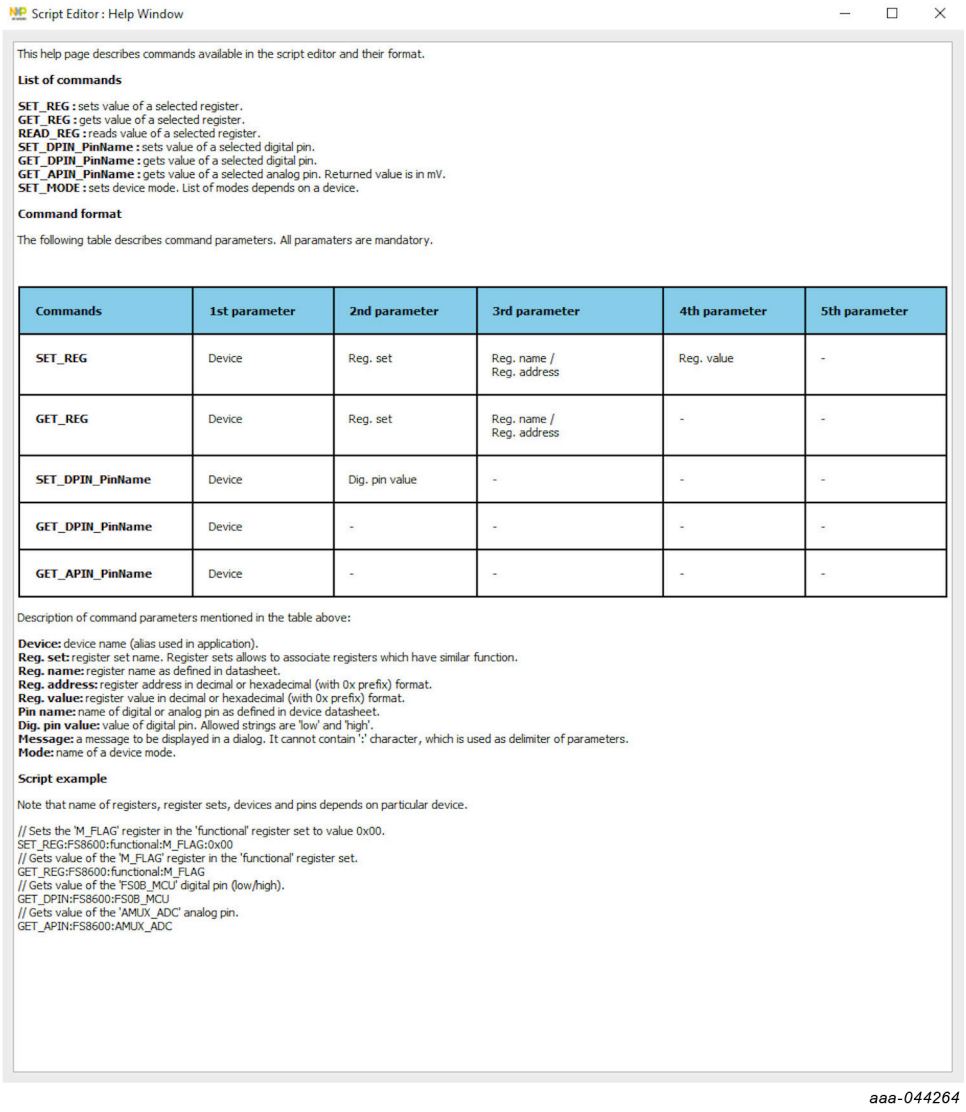


Figure 30. Script editor Help window

6.6.1.2 Management commands

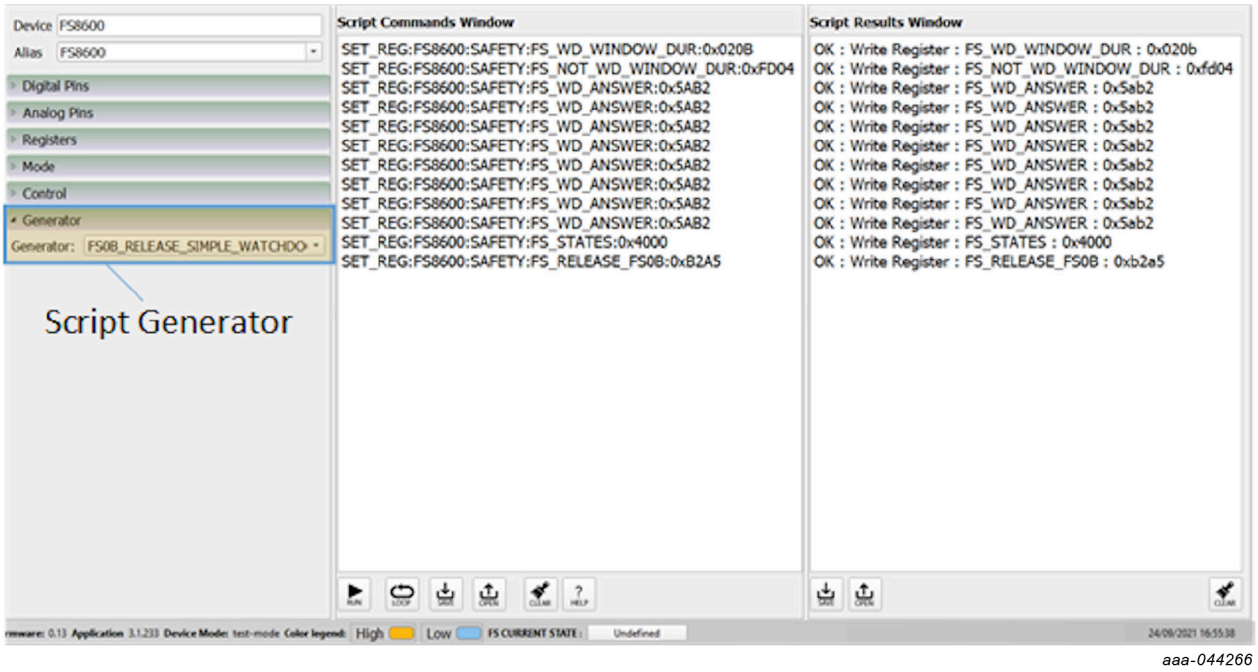
Some commands are used for formatting the scripts. Figure 31 shows the description of each button.

Figure 31. Script editor commands

- **Run**: Runs the script once.
- **Loop**: Runs the script continuously in a loop.
- **Save**: Save the script that is present in the script command window in text file.
- **Open**: Open a saved script from the desired location.
- **ATE**: Saves the script in ATE format.
- **Clear**: Clears the script command window.
- **Script Editor Help Window**: Describes the commands available in script editor and their formats.

6.6.1.3 Script generator

The script editor allows the user to save script sequence files, as shown in Figure 32. However, a script sequence file is already saved as an example in the script generator. This script is used to release FS0B when the PF5030 is using simple watchdog.



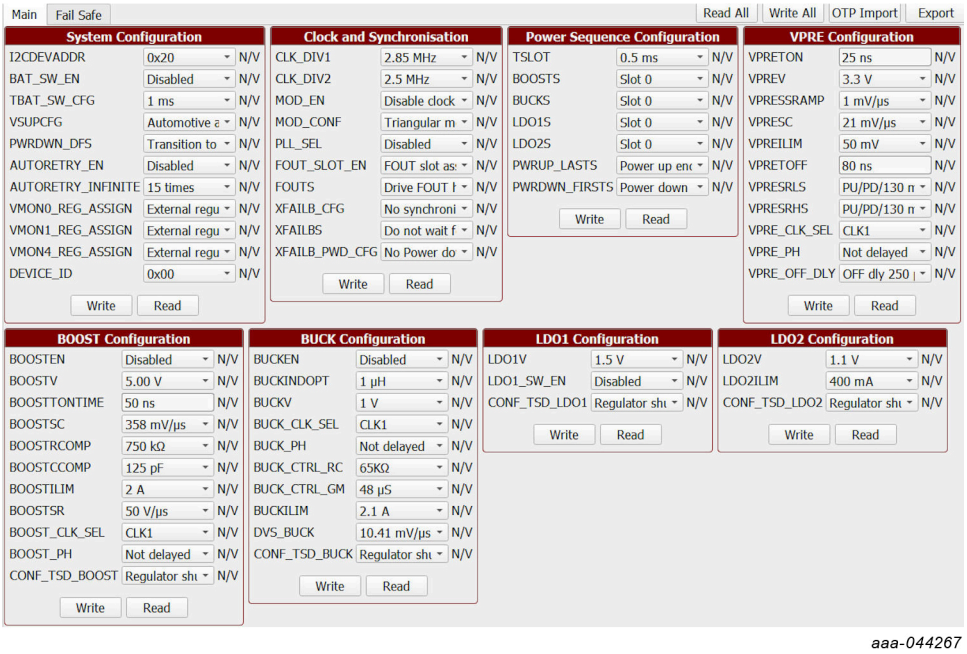
aaa-044266

Figure 32. Script generator

6.6.2 Mirrors tab

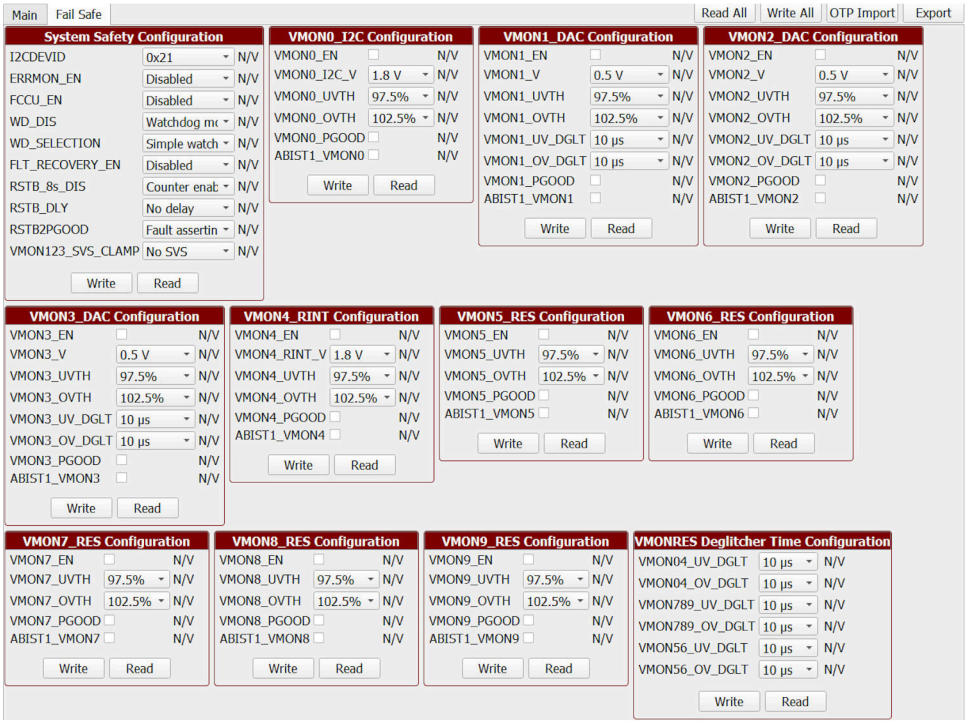
Test mode must be applied to enable the Mirrors tab. This tab is divided in main and fail-safe mirrors registers, shown in Figure 33 and Figure 34, respectively.

The "Read All" / "Write All" buttons can be used to read/write all the mirror registers. The mirrors configuration content can be exported and imported in the OTP tool as OTP configuration to generate TBB/OTP script files.



aaa-044267

Figure 33. Main mirrors tab



aaa-044268

Figure 34. Fail-safe mirrors tab

6.6.3 Access tab

6.6.3.1 Register map

All PF5030 I^2C registers can be accessed in write and read mode using this tab shown in Figure 35. These registers are divided into three sections:

- **Functional**: Main functional I^2C registers (diagnostics, configuration, and controls)
- **Safety**: Safety I^2C registers (diagnostics and configuration)
- **Write INIT safety**: Safety registers that can be written only during initialization phase (INIT_FS state).

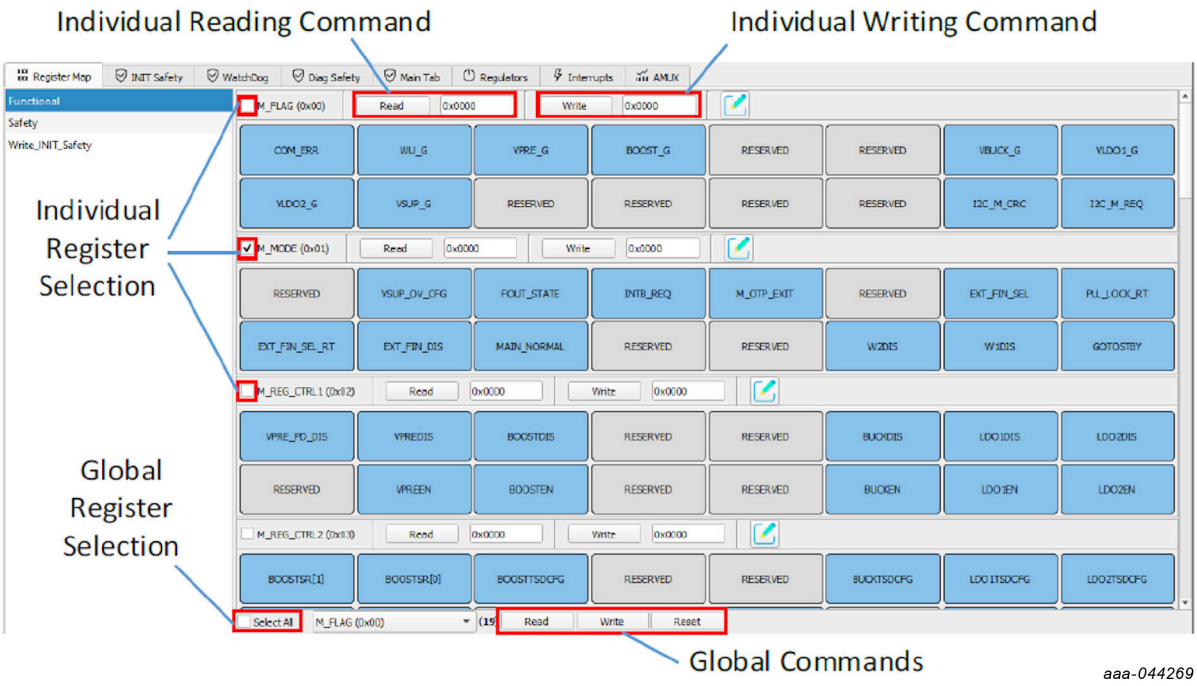


Figure 35. Register map access

To read the values of a register, click the **READ** button. The value is read from the device and is displayed on a label near the **READ** button. It is also displayed in the log window.

To write the bit values individually, click the desired bit. The corresponding bit button color changes. The value is updated in the log window. Click the WRITE button to write the register. To write the values through a text box near the **WRITE** button, enter the appropriate write value. Then click the **WRITE** button to write the register.

When registers have been selected, global commands can also be used:

- **WRITE**: Writes data to all the selected register at once.
- **READ**: Reads data back from the selected register at once.
- **RESET**: Resets all the input text boxes to 0x00. Write bits are set to 0. Change register bit buttons are set to the default setting.

The value can also be written by selecting the Edit option near the **WRITE** button. Bits and corresponding values are displayed in a pop window as shown in Figure 36. Select the options of all write bits, close the input dialog box, and click the **WRITE** button. Selected input combinations are written to the register.

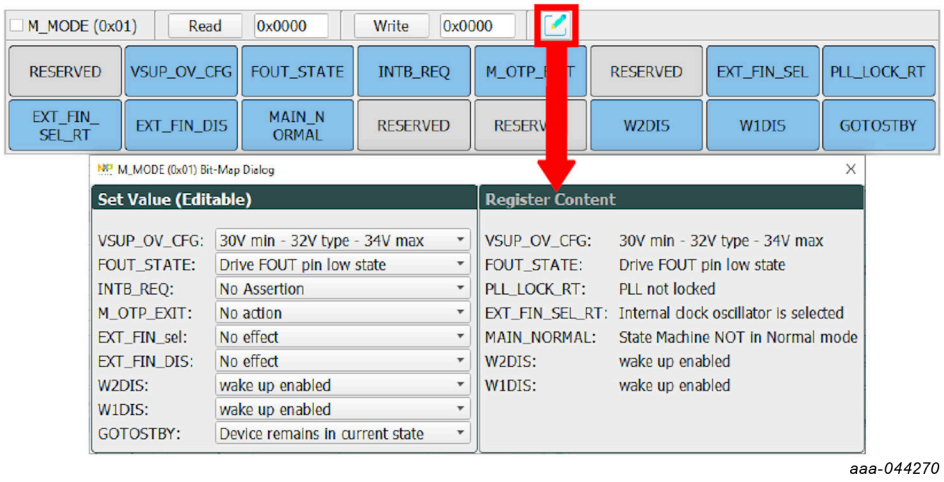


Figure 36. Bitmap dialog

Writing an INIT_FS register automatically updates the corresponding NOT register.

6.6.3.2 INIT Safety tab

This tab allows the initialization phase (INIT_FS state) configuration, that must be done before the first good watchdog refresh until the 2 seconds timeout limit.

In this tab, safety features can be configured, such as the safety output reaction when voltage monitoring fault is detected, watchdog refresh counter, fault error counter, as shown in Figure 37. The Analog Built-In Self-Test 2 ABIST2 (used for voltage monitoring assigned to external regulator), the VMON1 Static Voltage Scaling, counters limit, and other INIT_FS registers are also configurable from this tab. See the PF5030 data sheet for a complete description of these registers.

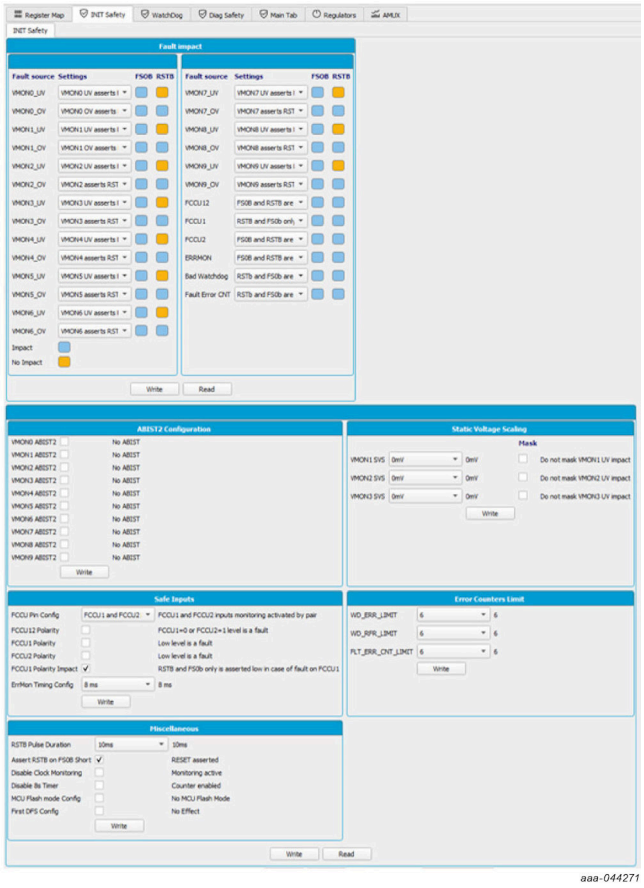


Figure 37. INIT safety tab

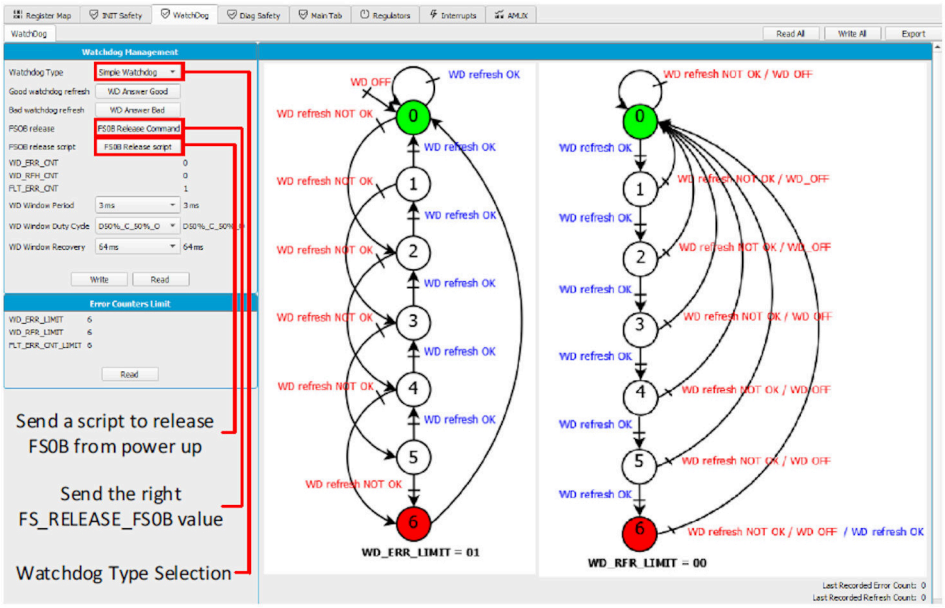
To ease the configuration, Read and Write All buttons are implemented.

6.6.3.3 Watchdog tab

The watchdog tab gathers all the registers and configurations having an impact on the watchdog, except "Watchdog Type". The watchdog error and refresh counters are displayed depending on the limit configuration. Watchdog answers can be generated and sent to the device depending on the watchdog type. The watchdog type configured in the OTP must be manually selected in the drop-down list to explore the watchdog features. If the user is not aware of the type of watchdog configured in the OTP, it can be found in Mirrors tab.

The "FS0B Release Command" calculates and sends the right secure 16-bit word to release FS0B.

A simplified way to release FS0B after power-up is to select the right type of watchdog configured in the OTP and then click the "FS0B Release script" button. This action sends the right sequence to close the initialization sequence, sets the error counter back to 0, and then releases FS0B, shown in Figure 38.

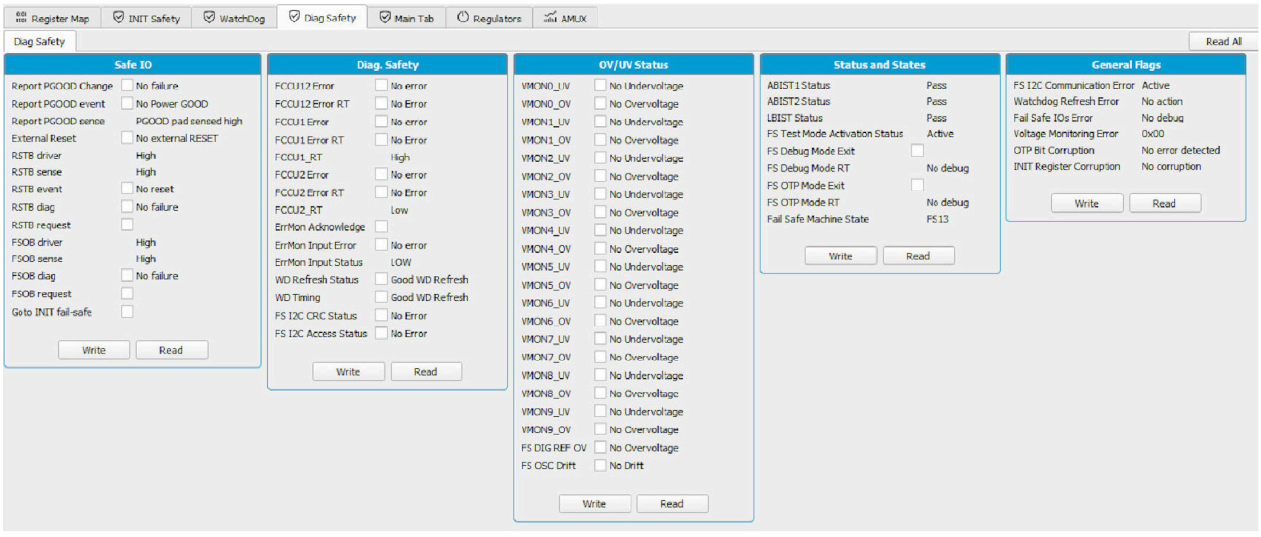


aaa-044272

Figure 38. Watchdog tab

6.6.3.4 Diagnostic Safety tab

The diagnostic safety tab shown in Figure 39 makes it possible to know the safety status of the device. The safety function events, like voltage monitoring flags, analog and logical BIST status, and safety pins are automatically reported in this tab. The PF5030 can also get out of OTP or Debug mode using this tab.



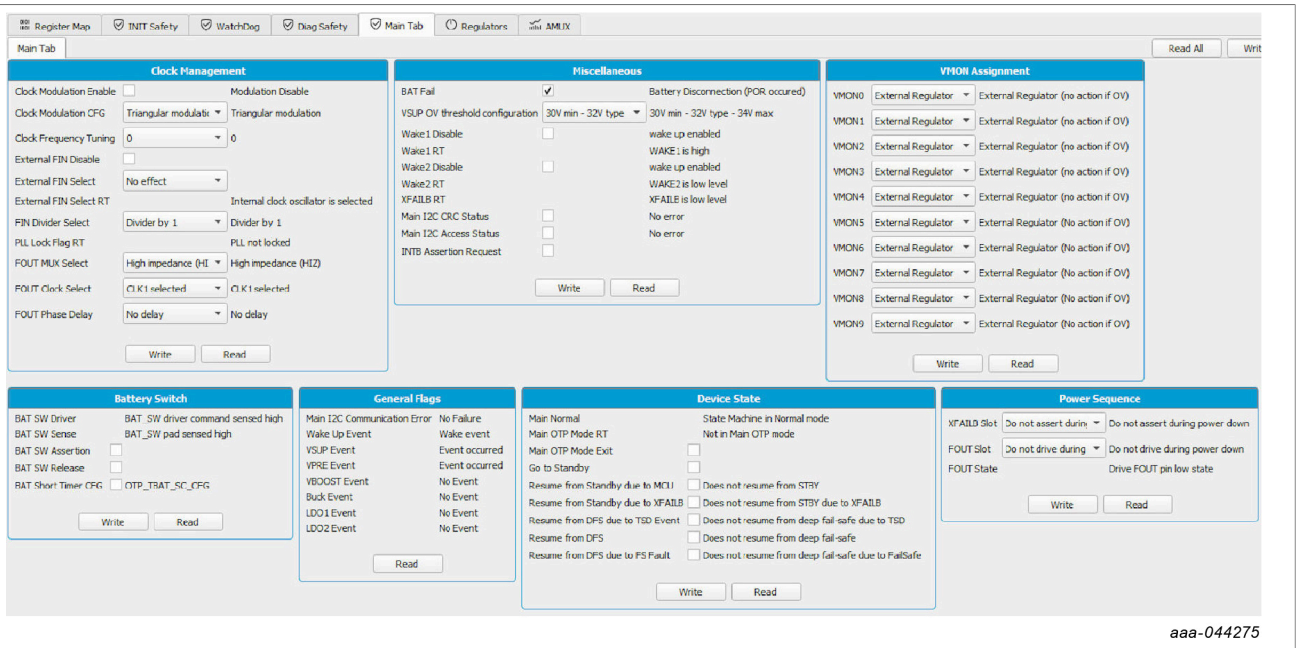
aaa-044274

Figure 39. Diagnostic safety tab

6.6.3.5 Main tab

Main configuration is possible from the main tab shown in Figure 40. The clock management box allows the configuration of the clock modulation. A regulator can be assigned to a voltage monitoring using the VMON assignment box, leading to a shutdown if OV occurs on the associated regulator.

The PF5030 can enter STANDBY/LPOFF state using the "Go to Standby" command, setting the bit GOTO_STBY = 1.



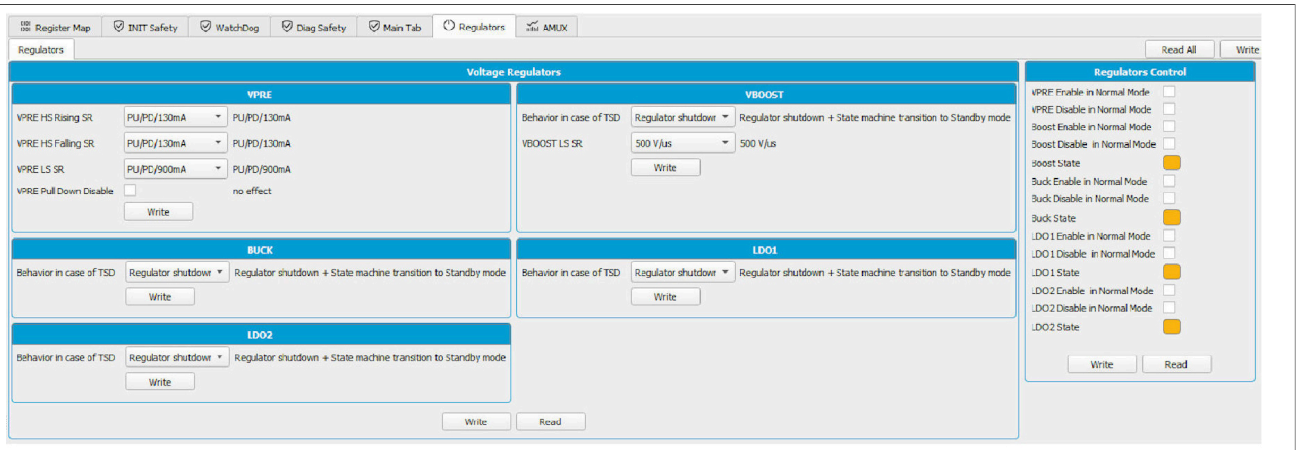
aaa-044275

Figure 40. Main tab

6.6.3.6 Regulators tab

The regulator tab shown in Figure 41 is used to configure the PF5030 SMPS or LDO. Regulators can be enabled or disabled on registers using I^2C commands, and the state / status of each regulators is also shown.

Each regulator has its own thermal shutdown (TSD) protection. After a TSD, the regulator is automatically re-enabled when the temperature returns to the normal operation range. Nevertheless, an additional configuration, by regulator, is available to make device transition to deep fail-safe (DEEP-FS) state in case of TSD and consequently shut down all regulators. In a practical perspective, it means that TSD on regulators supplying MCU rails can be configured to make a transition to DEEP-FS while regulators supplying external loads wont.



aaa-044276

Figure 41. Regulators tab

6.6.3.7 Main interrupts tab

The main interrupts tab shown in Figure 42 allows the monitoring of the regulators, the wake inputs, and the communication events or status. It allows the reading, writing, and polling of overvoltage/undervoltage, overtemperature, and overcurrent flags.

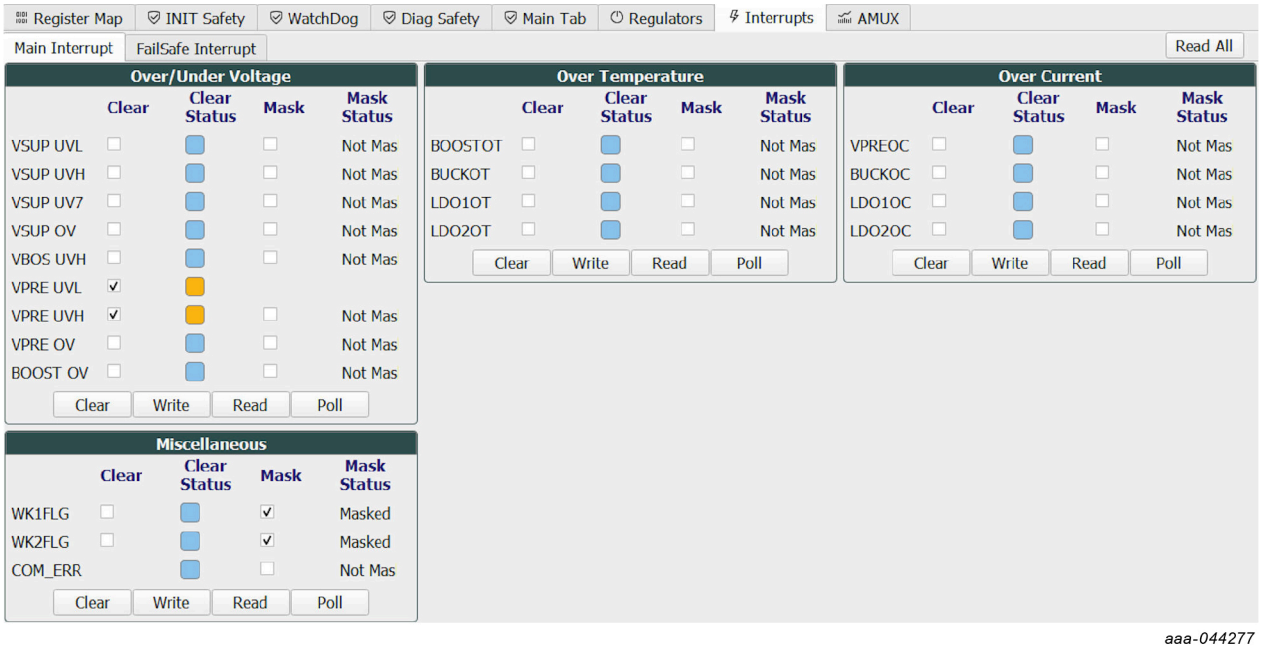


Figure 42. Interrupts tab

Different commands can be used to manage the interrupts:

- **Clear**: Interrupt flags latched and selected are cleared
- **Write**: Masks an interruption when the mask is selected
- **Read**: Gives the status of all interrupts
- **Poll**: Reads interrupts values in a loop

Additionally, **Clear All** / **Read All** buttons are available to control all interrupts on one click.

6.6.3.8 Fail-safe interrupts tab

The fail-safe interrupts tab shown in Figure 43 allows the monitoring of the overvoltage/undervoltage fail-safe monitoring status and the watchdog. It allows the reading, writing, and polling of overvoltage/undervoltage flags.

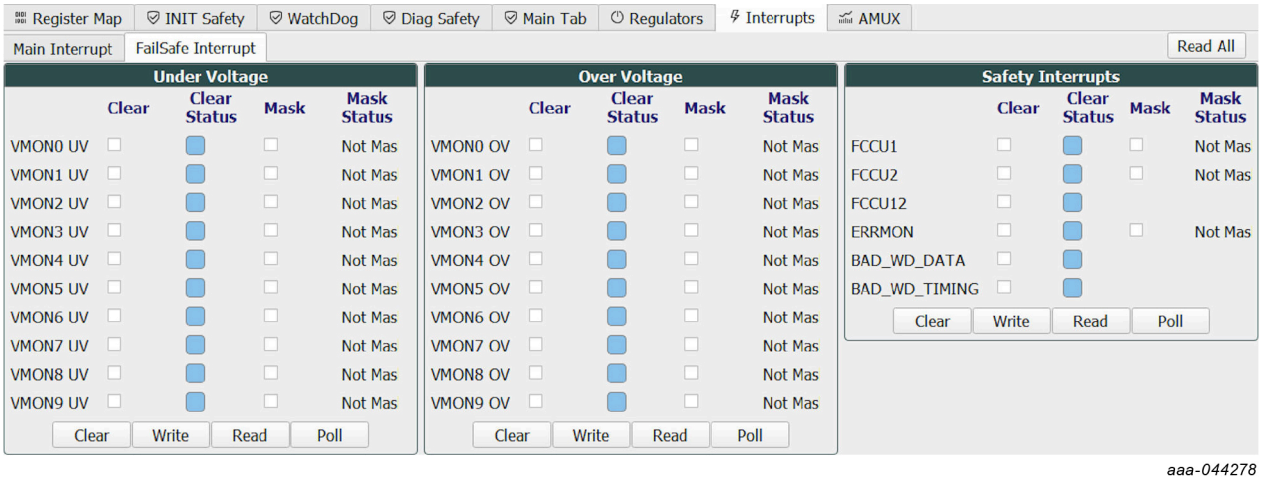


Figure 43. Fail-safe interrupts tab

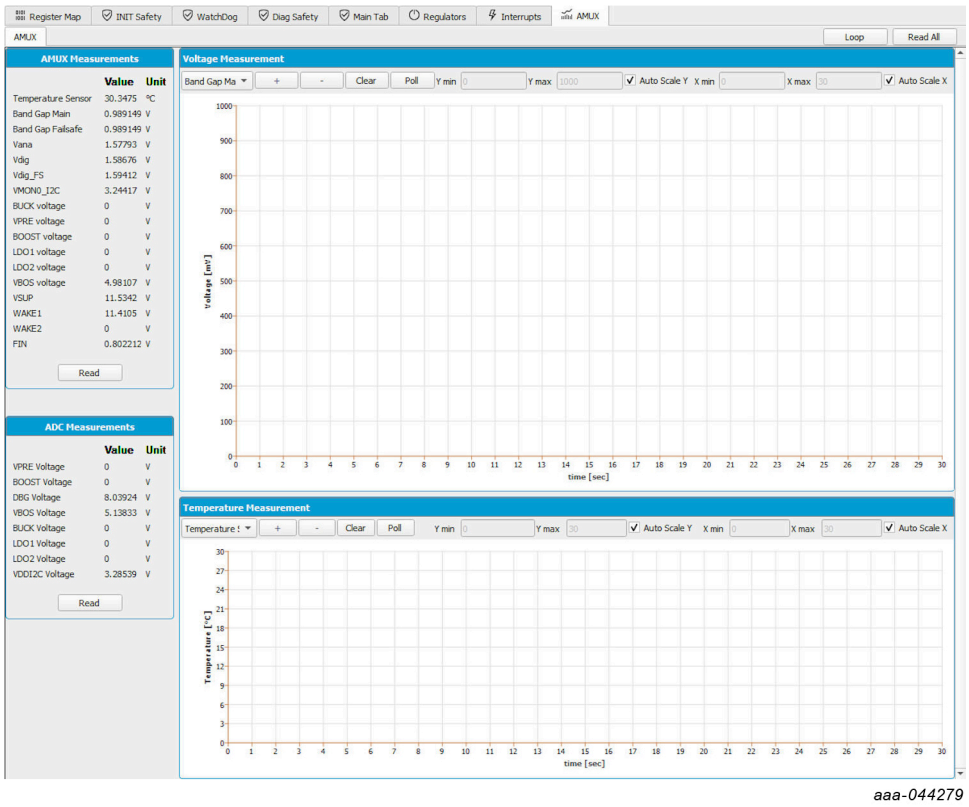
The same set of commands is used as the set to manage the interrupts as main interrupts.

6.6.3.9 AMUX

The AMUX tab shown in Figure 44 allows the selection of an AMUX pin channel and gets its current value by using the exclusive KL25Z AMUX ADC channel. You can do a single read or display various channels dynamically on the voltage or temperature graph. The displayed values already apply the divider and temperature formulas.

The input / output voltage rails are also monitored independently using additional the KL25Z ADC channels.

To use the dynamic graph, select the channel then click the “+” button to add to the graph. To start polling, click the "Poll" button. Click the "Poll" button again to stop measurements.



aaa-044279

Figure 44. AMUX measurements

7 Using an evaluation board

Before starting the process, consult the development board scheme and user manual to configure the required use case.

Learn about OTP before operating with the device. The device has a high level of flexibility due to the parameter configuration available in the OTP. It impacts the functionality of the device. It is key to understand how OTP parameters can be programmed, the interaction with mirror registers, and the PF5030 device.

The OTP-related operations can only be performed in test mode (emulation) and OTP mode (programming, test mode is enabled automatically). When using emulation, the device loses the configuration when the power supply is switched off, when the device enters deep fail-safe (DEEP-FS) state, or when it goes standby.

7.1 OTP and mirrors registers

The device incorporates two OTP blocks. One is for the main section, the other for the fail-safe section. During configuration, each of them uses dedicated sectors.

Each block is divided in two sectors, S1 and S1bis respectively, so the device can be fused two times. The OTP configuration scheme is shown in Figure 45 (same implementation for main and fail-safe).

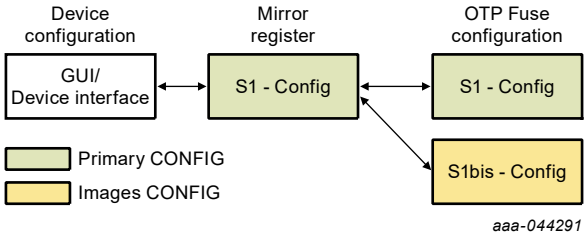


Figure 45. OTP block diagram

At device starts-up, the content of the valid (last programmed) sector is loaded into mirror registers. The mirror register content is accessible from the NXP GUI, using specific I^2C commands. The NXP GUI manages the mirror configuration, which facilitates access. The mirror register content handling is called "OTP emulation".

To burn the OTP configuration, the mirror register content must be loaded with the desired content. Then a command must be sent to burn the mirror content to the next available OTP sector. The first sector to be burned is S1, the second S1bis. The NXP GUI automatically manages the next sector to be burned. It is not possible to revert to the previous sector. When the user reaches the sector S1bis, there is no other possibility for burn. However, the emulation is still available.

7.2 Device modes

There are several modes that describe device operation.

There are three modes to run the device:

- **User mode**: Only user-related registers can be accessed and handled.
- **OTP mode**: OTP fuse content loaded to mirror registers. OTP programming / emulation (mirror registers handling) possible.
- **Test mode**: OTP programming and mirror registers handling (emulation) granted.

There are two modes to run the device related to the fail-safe state machine:

- **Normal mode**: Watchdog windowing and initialization (INIT_FS state) timeout depend on OTP configuration.
- **Debug mode**: Watchdog windowing disabled, no initialization timeout, fail-safe safety reactions disabled.

Debug and OTP modes are enabled by applying voltage on DBG pin during startup and/or restart.

OTP mode activation implies in Debug mode activation.

Debug and OTP modes can be disabled with an I^2C command.

Test mode can be enabled at any moment with an I^2C command when the voltage is applied on DBG pin.

7.3 Configuring the hardware for start-up

Figure 46 presents a typical hardware configuration incorporating the development board, power supply and, Windows PC workstation.

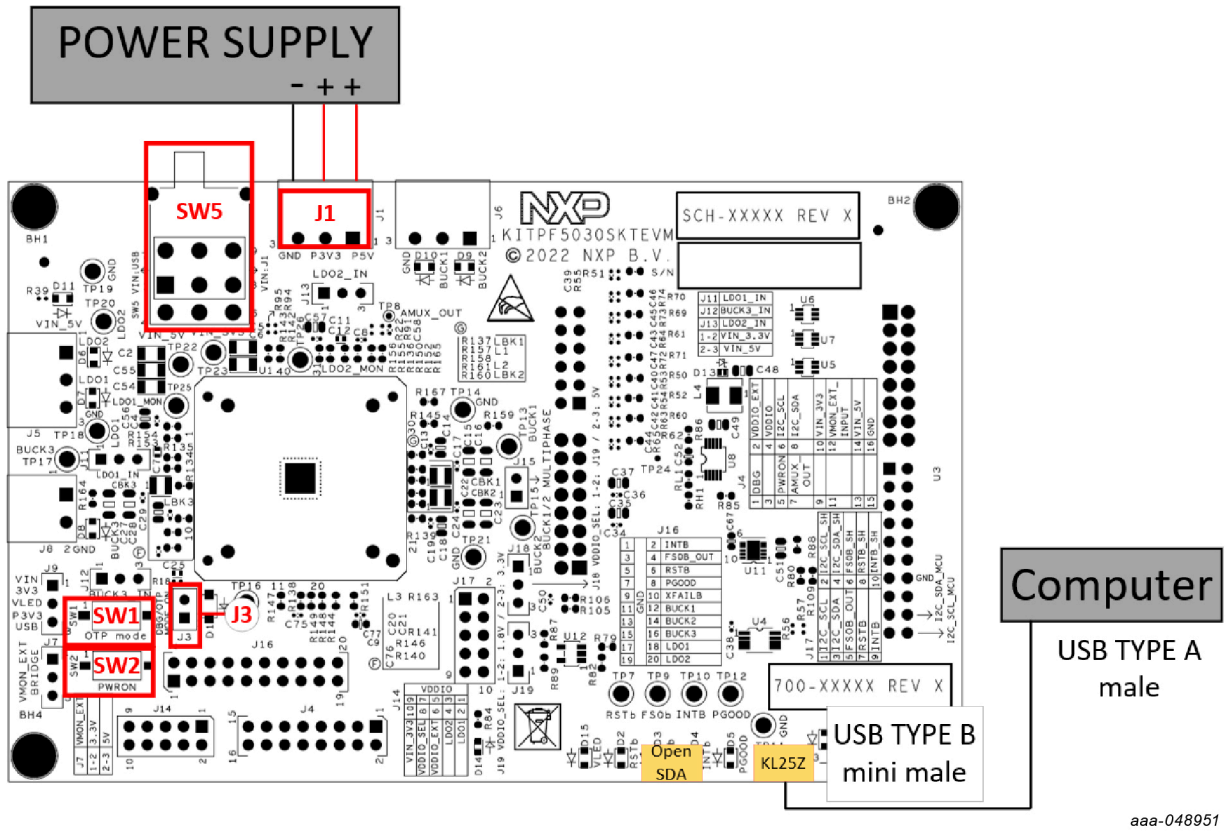


Figure 46. Typical initial configuration

To configure the hardware and workstation as illustrated in Figure 46, complete the following procedure:

1. Install jumpers and switches for the configuration shown in Table 22.

Table 22. Hardware configuration

Board configuration	Configuration		
	Normal mode	Debug mode entry	OTP / test mode entry
Watchdog configuration	Watchdog windowing enabled, 2 seconds INIT_FS timeout (OTP WDW_INF = 0)	Watchdog windowing disabled, no INIT_FS timeout	OTP programming / emulation, Debug mode enabled
	Watchdog windowing disabled, no INIT_FS timeout (OTP WDW_INF = 1)		
J3 (DBG)	Open	Connect 1 to 2 DBG pin voltage pulled to 4.5 V or 7.95 V (SW1)	
SW2 (PWRON)	Close (PWRON pin high-logic level)		
SW5 (VIN)	Middle position (supplies OFF)		
SW1 (OTP mode)	Open (DBG = VIN_5V)		Close (OTP mode ON)

2. Connect the Windows PC USB port to the KITPF5030SKTEVM board using the provided USB 2.0 cable.
3. If external power supplies are used, set the power supplies to 3.3 V and 5.0 V, and current limit to 1.0 A. With power turned off, attach the power supplies positive and negative outputs to J1, then turn on.
4. Put SW5 in LEFT position if USB power is used or RIGHT position if external power supply is used.

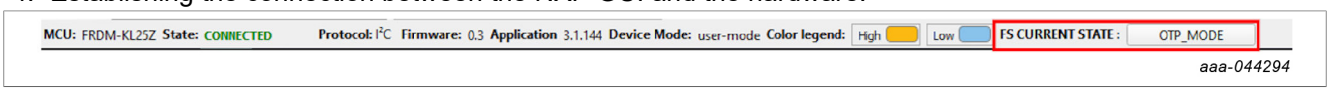
At this step, if the product is in OTP mode entry configuration, all regulators are OFF. The user can power up with an OTP configuration or configure the mirror registers before powering up. Power-up sequence starts as soon as one of these four actions occurs:

- J3 jumper is removed
- SW1 is switched OFF
- OTP mode exit command is sent using I^2C
- NXP GUI button "Exit OTP Mode" is clicked

7.4 Working in OTP emulation mode

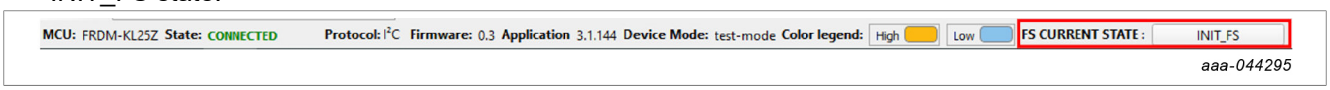
At start-up, the device always uses the content of the mirror register. This content can come from OTP fuse or from a configuration written directly in the mirror register. OTP emulation means that the user can emulate the fuse content by writing in the mirror register, which allows trials before burning the OTP.

1. Configure the hardware for OTP mode entry.
2. Launch the NXP GUI for Automotive PMIC Families software.
3. Create an OTP configuration and export/generate the TBB/OTP script file.
4. Establishing the connection between the NXP GUI and the hardware.



Check that the fail-safe state machine is in OTP MODE state and "Exit OTP mode" must be green. If not, check 1 and redo this step. While in OTP mode, all regulators are off.

5. On the script editor, load the TBB/OTP script file and send content to the mirror registers.
6. Click "Exit OTP mode" button, if all goes right, regulators start-up and fail-safe state machine must be in INIT_FS state.



   a. If the mirror registers are filled (with a configuration using the Script editor), that configuration is used in the emulation session.
   b. If the mirror registers are not filled (with a configuration using the Script editor), the currently programmed OTP fuse configuration is used, if it exists.

c. Otherwise, the mirror registers are not filled and the OTP fuse is not burned. The device does not start up properly.

Device is in Debug mode. As long as Debug mode is not exited by writing FS_STATES: [FS_DBG_MODE_EXIT] bit to 1, the FS0B pin cannot be released.

7.5 Releasing FS0B script

The following script can be used to release FS0B:

- Disable the watchdog windowing (simple watchdog configuration is used here).
- Close the initialization phase with (a first) good watchdog refresh.
- Exit the Debug mode.
- Send six (default) additional consecutive good watchdog refreshes to revert the fault error counter to 0.
- Release FS0B pin, which is only valid if watchdog windowing is activated in OTP.

Table 23. Release FS0B sequence example for simple watchdog (ASIL B)

Step	Register name	Value	Description
1	FS_WD_WINDOW_DUR	0x020B	WDW_PERIOD[4:0] = 0x00000 (watchdog disabled)
2	FS_NOT_WD_WINDOW_DUR	0xFD04	NOT of FS_WD_WINDOW_DUR
3	FS_WD_ANSWER	0x5AB2	1st good watchdog answer (close the initialization phase)
4	FS_STATES	0x4000	FS_DBG_MODE_EXIT = 1 (exit debug mode)
5	FS_WD_ANSWER	0x5AB2	2nd good watchdog answer
6	FS_WD_ANSWER	0x5AB2	3rd good watchdog answer
7	FS_WD_ANSWER	0x5AB2	4th good watchdog answer
8	FS_WD_ANSWER	0x5AB2	5th good watchdog answer
9	FS_WD_ANSWER	0x5AB2	6th good watchdog answer
10	FS_WD_ANSWER	0x5AB2	7th good watchdog answer
11	FS_RELEASE_FS0B	0xB2A5	FS0B pin released (pulled to high level)

This sequence can be sent using a script built with NXP GUI. There are two options:

- Clicking ACCESS > WatchDog > "Watchdog Management" > "FS0B Release script". Remember to chose appropriated "Watchdog Type" before.
- Clicking SCRIPT (editor) > Generator > "FS0B_RELEASE_XX_WATCHDOG", then click "RUN".

8 References

[1] **KITPF5030SKTEVM** — detailed information on this board, including documentation, downloads, and software and tools
http://www.nxp.com/KITPF5030SKTEVM

[2] **PF5030** — detailed information on PF5030
http://www.nxp.com/PF5030

[3] **NXP GUI for Automotive PMIC Families** — Software GUI for NXP Automotive PMIC products
https://www.nxp.com/PMIC-GUI-SW

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Tables

Figures