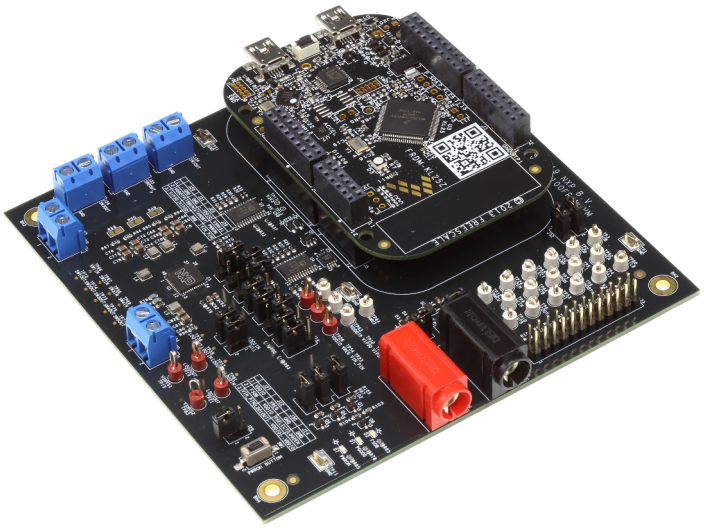
UM11487

KITPF7100FRDMEVM evaluation board

Rev. 1 — 15 September 2020 **User guide**



aaa-038925

Figure 1. KITPF7100FRDMEVM

Important Notice

NXP provides the enclosed product(s) under the following conditions:

This evaluation kit is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This evaluation board may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. This evaluation board is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

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1 Introduction

This document is the user guide for the PF7100 evaluation boards, intended for the engineers involved in the evaluation, design, implementation, and validation of multi-channel power management integrated circuit PF7100.

The scope of this document is to provide the user with information to evaluate the multi-channel power management integrated circuit PF7100. This document covers connecting the hardware, installing the software and tools, configuring the environment and using the kit.

The evaluation board provides full access to all the features in the PF7100 device.

2 Finding kit resources and information on the NXP web site

NXP Semiconductors provides online resources for evaluation boards and its supported device(s) on http://www.nxp.com.

The information page for evaluation boards are at http://www.nxp.com/KITPF7100FRDMEVM. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a **Getting Started** tab. The **Getting Started** tab provides quick-reference information applicable to these evaluation boards, including the downloadable assets referenced in this document.

2.1 Collaborate in the NXP community

The NXP community is for sharing ideas and tips, ask and answer technical questions, and receive input on just about any embedded design topic.

The NXP community is at http://community.nxp.com.

3 Getting ready

Working with these evaluation boards requires the kit contents, additional hardware and a Windows PC workstation with installed software.

3.1 Kit contents

- Assembled and tested evaluation board and preprogrammed FRDM-KL25Z microcontroller board in an anti-static bag
- USB-STD A to USB-B-mini cable
- Quick Start Guide

3.2 Additional hardware

In addition to the kit contents, the following hardware is necessary or beneficial when working with this kit.

- Power supply with a range of 3.0 V to 5.0 V and a current limit set initially to 1.0 A (maximum current consumption can be up to 7.0 A)

3.3 Windows PC workstation

This evaluation board requires a Windows PC workstation. Meeting these minimum specifications should produce great results when working with this evaluation board.

- USB-enabled computer with Windows 7, Windows 8, or Windows 10

3.4 Software

Installing software is necessary to work with this evaluation board. All listed software is available on the evaluation board's information page at http://www.nxp.com/KITPF7100FRDMEVM or from the provided link.

Software package NXP_GUI_PR_revision.zip contains:

- KL25Z firmware files
- PF7100 NXPGUI Setup
- OTP mirror register read script

4 Getting to know the hardware

The NXP analog product development boards provide an easy-to-use platform for evaluating NXP products. The boards support a range of analog, mixed-signal and power solutions. They incorporate monolithic integrated circuits and system-in-package devices that use proven high-volume technology. NXP products offer longer battery life, a smaller form factor, reduced component counts, lower cost and improved performance in powering state-of-the-art systems.

4.1 Kit overview

The customer evaluation board features the PF7100 power management IC. The kit integrates all hardware needed to fully evaluate the PMIC. The PF7100 on the board is without OTP pre-programmed, allows the user to define the OTP configuration for the device.

It integrates a communication bridge based on the FRDM-KL25Z freedom board to interface with the NXPGUI software, to fully configure, and control the PF7100 PMIC.

4.1.1 Evaluation board features

Buck regulators

- SW1, SW2, SW3, SW4, 0.4 V to 1.8 V; 2500 mA; 2 % accuracy and dynamic voltage scaling and single, dual, triple or quad-phase configuration
- SW5; 1.0 V to 4.1 V; 2500 mA; 2 % accuracy
- Configurable VTT termination mode on SW3
- Programmable current limit
- Spread-spectrum and manual tuning of switching frequency

LDO regulators

- 2x LDO regulator 0.8 V to 5.0 V, 400 mA: 3 % accuracy with optional load switch mode
- Selectable hardware/software control on LDO2

RTC supply VSNVSs

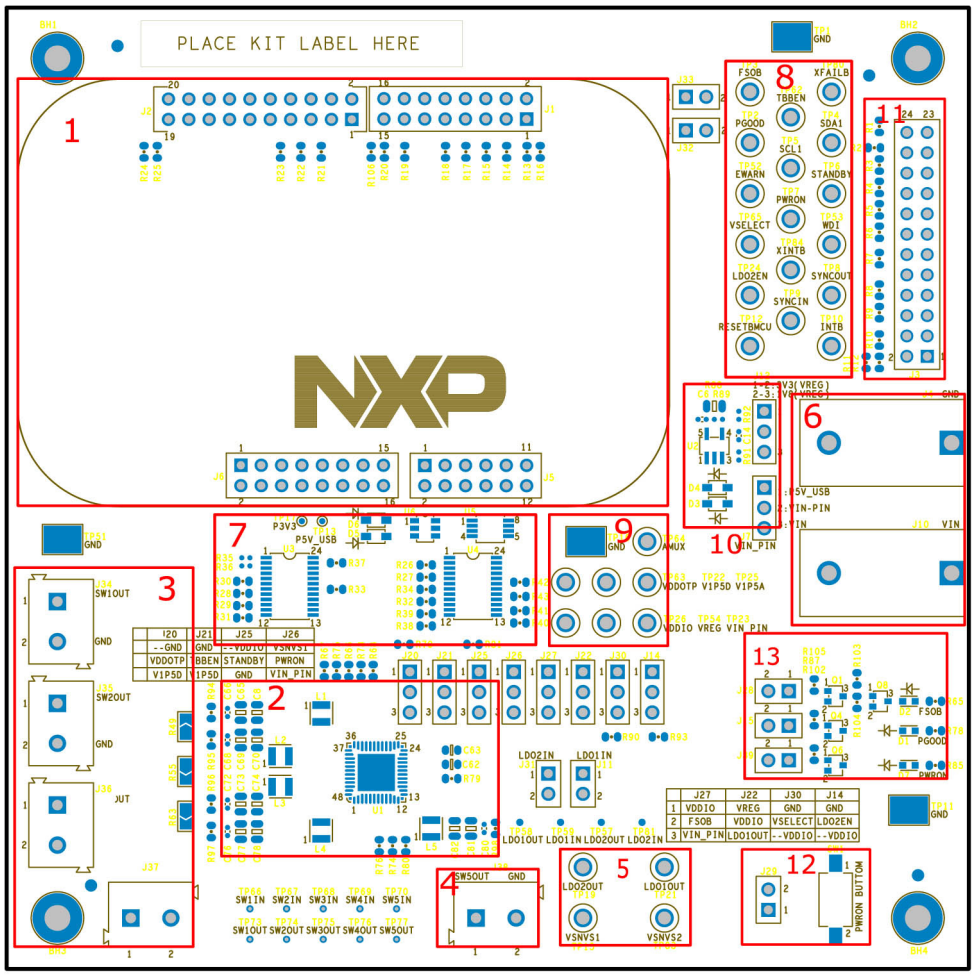
- VSNVS1, 1.8 V/3.0 V/3.3 V, 10 mA
- VSNVS2, 0.8 V/0.9 V/1.8 V, 10 mA

System features

- 2.5 V to 5.5 V operating input voltage range
- USB to I^2C communication via the FRDM-KL25Z interface
- Selectable hardwire default PMIC configuration or OTP/TBB operation
- Fast mode I^2C communication at 400 kHz (high-speed operation supported by PMIC)
- Advance system monitoring/diagnostic via PMIC and/or system AMUX
- Master/slave interface connector
- Onboard I/O regulator with 1.8 V/3.3 V selectable output voltage

4.2 Kit featured components

Figure 2 identifies important components on the board.



1. FRDM-KL25Z Freedom board connector
2. PF7100 PMIC
3. SW1, SW2, SW3, and SW4 power connector
4. SW5 power connector
5. LDO and VSNVS power connector
6. Input power banana jack
7. External analog multiplexer
8. PMIC I/O test points
9. Analog supplies test points
10. 1.8 V/3.3 V external LDO regulator
11. Master/slave interface connector
12. PWRON button
13. IO LED indicator

Figure 2. Evaluation board featured component locations

4.2.1 PF7100: 7-channel power management integrated circuit for high performance applications

4.2.1.1 General description

The PF7100 family of devices feature power management integrated circuit (PMIC) designed for high performance i.MX 8 applications. It features five high-efficiency buck converters and two linear regulators for powering the processor, memory and miscellaneous peripherals.

Built-in one time programmable memory stores key startup configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed I^2C after start up offering flexibility for different system states.

4.2.1.2 Features

- Five high-efficiency buck converters
- Two linear regulators with load switch options
- Two VSNVS regulators for RTC supply
- Watchdog timer/monitor
- Monitoring circuit developed in compliance with ASIL B process
- One time programmable device configuration
- 3.4 MHz I^2C communication interface
- 48-pin 7 x 7 QFN package

4.3 Schematic, board layout, and bill of materials

The board layout and bill of materials for the evaluation board are available at http://www.nxp.com/KITPF7100FRDMEVM.

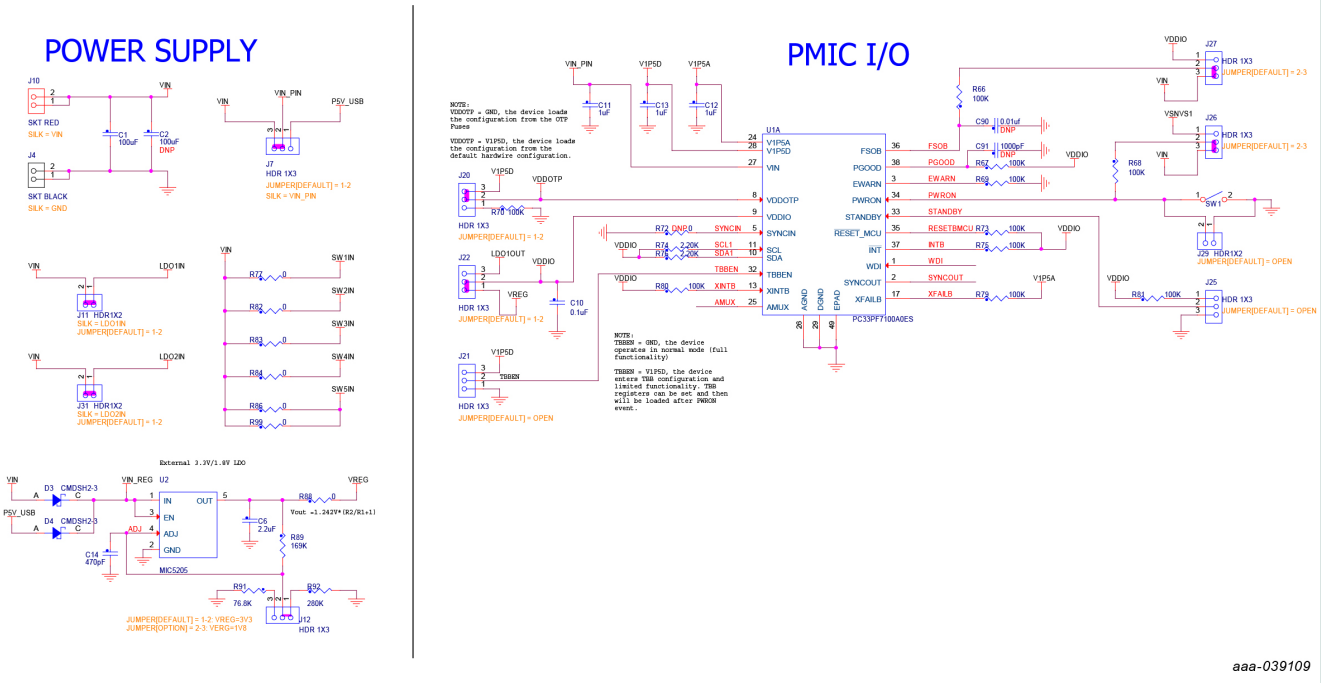


Figure 3. PF7100 system I/O

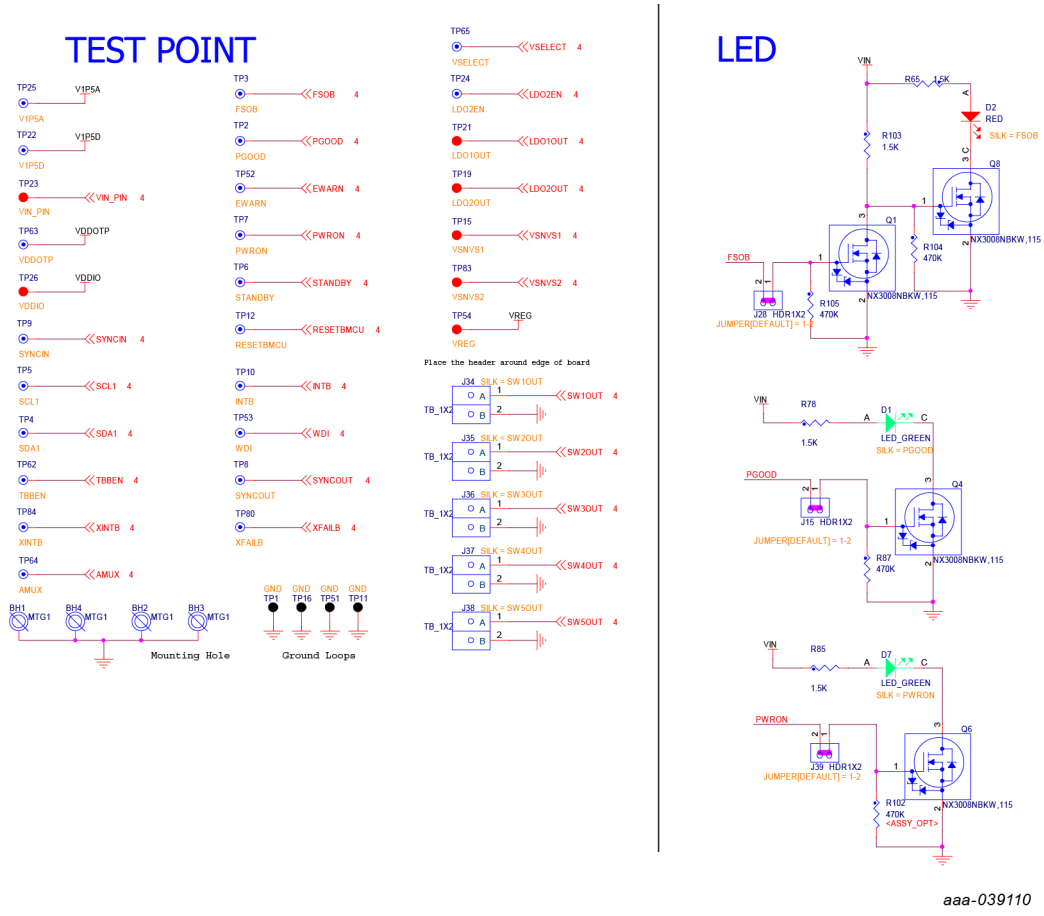


Figure 4. Test points

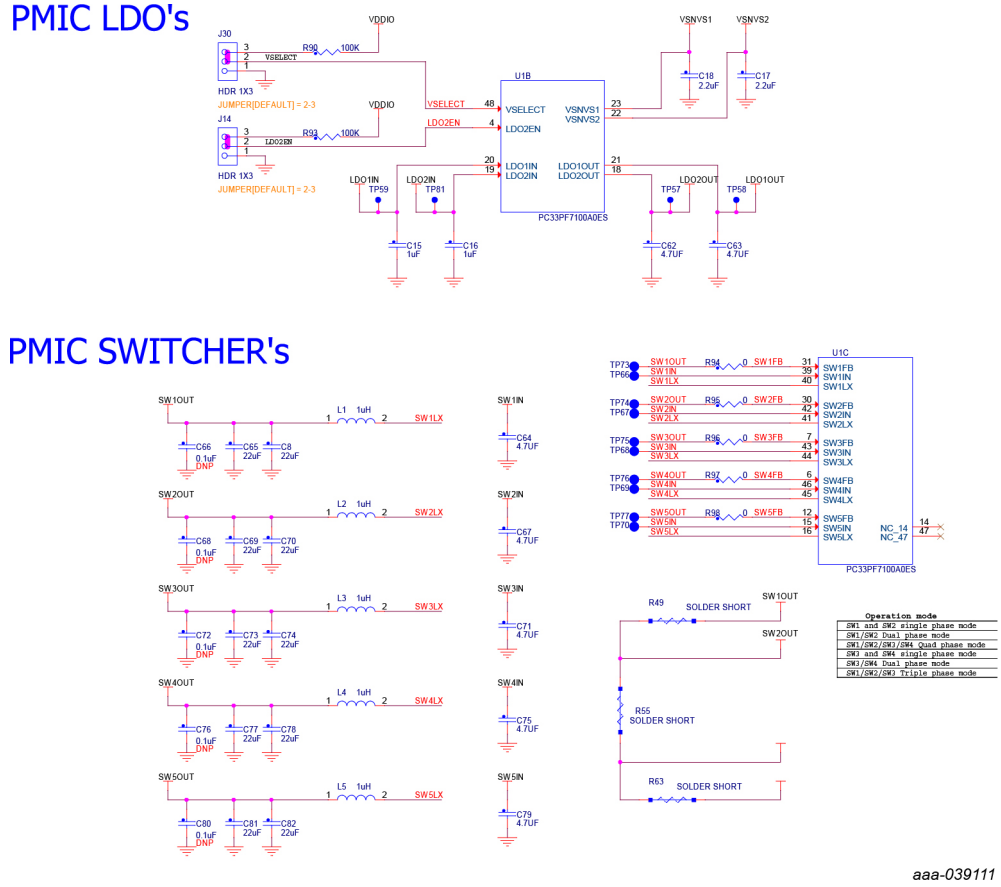


Figure 5. Regulators

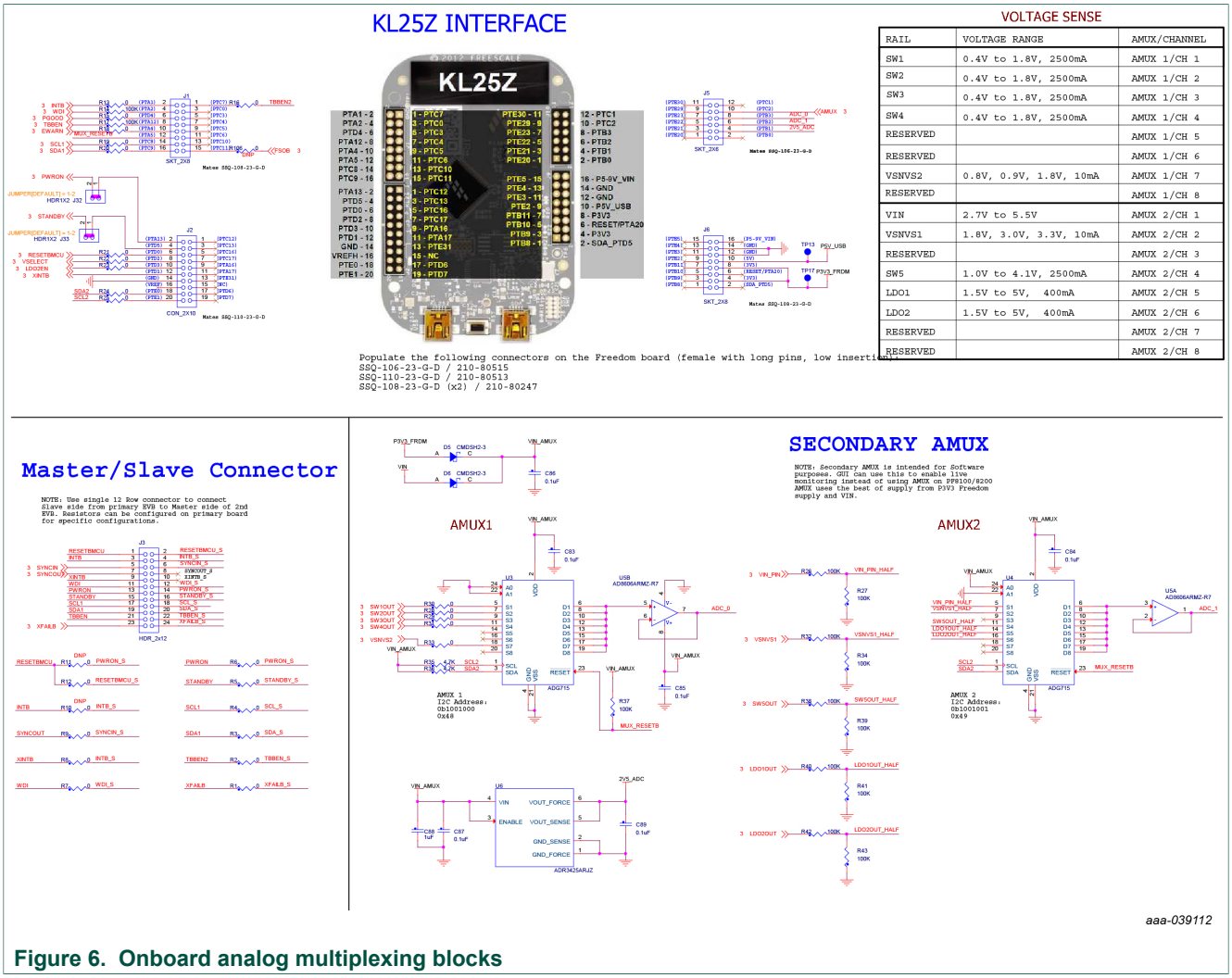


Figure 6. Onboard analog multiplexing blocks

4.4 Default jumper configurations

Table 1. Evaluation board jumper descriptions

Name	Default	Description
J1, J2, J5, J6	—	Freedom board interface
J3	—	Master/slave connector • Odd row is connected directly to pins in the Master board • Even row is used to connect a slave board signal • Interface connection is made via shunt resistors R1 to R11
J7	2-3 shorted	Select PMIC VIN supply • 1-2 → From Freedom board P5V_USB (used only for demo functional operation, no loading capability in this operation mode) • 2-3 → From main board VIN node
J11	Shorted	Connects LDO1IN to main board VIN node
J12	1-2 shorted	Selects the external LDO voltage • 1-2 → 3.3 V • 2-3 → 1.8 V

Name	Default	Description
J14	Open	LDO2EN pin control • 1-2 → LDO2EN pin pulled low • 2-3 → LDO2EN pin pulled high • Open → full MCU control with no pull-up
J15	Shorted	Enables the PGOOD green LED
J20	2-3 shorted	Selects PF7100 default register configuration • 1-2 → OTP mode • 2-3 → Hardwire mode
J21	Open	Enables TBB mode • 1-2 → TBB mode disabled • 2-3 → TBB mode enabled • Open → MCU has control of this pin
J22	1-2 shorted	Selects VDDIO supply • 1-2 → VDDIO is supplied by external LDO regulator • 2-3 → VDDIO is supplied by LDO1
J25	Open	Selects STANDBY pin voltage level • 1-2 → STANDBY pulled up to VDDIO • 2-3 → STANDBY pin low • Open → STANDBY pin controlled by MCU
J26	2-3 shorted	Controls PWRON pull-up source • 1-2 → PWRON pulled up to VSNVS1 • 2-3 → PWRON pulled up to VIN • Open → full MCU control with no pull-up
J27	2-3 shorted	Selects pull up for FSOB pin • 1-2 → FSOB pulled up to VDDIO • 2-3 → FSOB pulled up to VIN
J28	Shorted	Enables the FSOB red LED
J29	Open	Pulls down PWRON pin to ground
J30	2-3 shorted	VSELECT pin control • 1-2 → VSELECT pin pulled low • 2-3 → VSELECT pin pulled to VDDIO • Open → full MCU control with no pull-up
J31	Shorted	Connects LDO2IN to main board VIN node
J32	Shorted	PWRON connection from PMIC to MCU
J33	Shorted	STANDBY connection from PMIC to MCU
J39	Shorted	Enables the PWRON green LED

4.5 Test points

Table 2. Evaluation board test point descriptions

Name (label)	Signal name	Description
Ground test points		
TP1, TP11, TP16, TP51 (GND)	GND	Ground plane test points
Digital I/O signal		
TP2 (PGOOD)	PGOOD	Connected to pin 38 (PGOOD) on PMIC
TP3 (FSOB)	FSOB	Connected to pin 36 (FSOB) on PMIC
TP4 (SDA)	SDA1	Connected to pin 10 (SDA) on PMIC. Main system I^2C bus.

Name (label)	Signal name	Description
TP5 (SCL)	SCL1	Connected to pin 11 (SCL) on PMIC. Main system I^2C bus.
TP6 (STANDBY)	STANDBY	Connected to pin 33 (STANDBY) on PMIC
TP7 (PWRON)	PWRON	Connected to pin 34 (PWRON) on PMIC
TP8 (SYNCOUT)	SYNCOUT	Connected to pin 2 (SYNCOUT) on PMIC
TP9 (SYNCIN)	SYNCIN	Connected to pin 5 (SYNCIN) on PMIC
TP10 (INTB)	INTB	Connected to pin 37 (INTB) on PMIC
TP12 (RESETBMCU)	RESETBMCU	Connected to pin 35 (RESETBMCU) on PMIC
TP24 (LDO2EN)	LDO2EN	Connected to pin 4 (LDO2EN) on PMIC
TP52 (EWARN)	EWARN	Connected to pin 3 (EWARN) on PMIC
TP53 (WDI)	WDI	Connected to pin 1 (WDI) on PMIC
TP62 (TBBEN)	TBBEN	Connected to pin 32 (TBBEN) on PMIC
TP65 (VSELECT)	VSELECT	Connected to pin 48 (VSELECT) on PMIC
TP80 (XFAILB)	XFAILB	Connected to pin 17 (XFAILB) on PMIC
TP84 (XINTB)	XINTB	Connected to pin 13 (XINTB) on PMIC
Analog signals		
TP13 (P5V_USB)	P5V_USB	Connected to J6 pin 10 connects to Freedom board P5V_USB
TP15 (VSNVS1)	VSNVS1	Connected to pin 23 (VSNVS1) on PMIC
TP17 (P3V3_FRDM)	P3V3_FRDM	Connected to J6 pin 4/8 connects to Freedom board P3V3
TP22 (V1P5D)	V1P5D	Connected to pin 28 (V1P5D) on PMIC
TP23 (VIN_PIN)	VIN_PIN	Connected to pin 27 (VIN) on PMIC
TP25 (V1P5A)	V1P5A	Connected to pin 24 (V1P5A) on PMIC
TP26 (VDDIO)	VDDIO	Connected to pin 9 (VDDIO) on PMIC
TP54 (VREG)	VREG	1.8 V or 3.3 V external regulator output
TP63 (VDDOTP)	VDDOTP	Connected to pin 8 (VDDOTP) on PMIC
TP64 (AMUX)	AMUX	Connected to pin 25 (AMUX) on PMIC
TP83 (VSNVS2)	VSNVS2	Connected to pin 22 (VSNVS2) on PMIC
LDO test points		
TP19 (LDO2OUT)	LDO2OUT	Power path for the LDO2 output
TP21 (LDO1OUT)	LDO1OUT	Power path for the LDO1 output
TP57	LDO2OUT sense	LDO2 output sense path. Connected directly to pin 18 (LDO2OUT) on PMIC.
TP58	LDO1OUT sense	LDO1 output sense path. Connected directly to pin 15 (LDO1OUT) on PMIC.
TP59	LDO1IN sense	LDO1 input sense path. Connected directly to pin 20 (LDO1IN) on PMIC.
TP81	LDO2IN sense	LDO2 input sense path. Connected directly to pin 19 (LDO2IN) on PMIC.
Switching regulator test points		
TP66	SW1IN sense	SW1 input sense path. Connected directly to pin 39 (SW1IN) on PMIC.
TP67	SW2IN sense	SW2 input sense path. Connected directly to pin 42 (SW2IN) on PMIC.

Name (label)	Signal name	Description
TP68	SW3IN sense	SW3 input sense path. Connected directly to pin 43 (SW3IN) on PMIC.
TP69	SW4IN sense	SW4 input sense path. Connected directly to pin 46 (SW4IN) on PMIC.
TP70	SW5IN sense	SW5 input sense path. Connected directly to pin 15 (SW5IN) on PMIC.
TP73	SW1OUT sense	SW1 output sense path. Connected directly to pin 31 (SW1FB) on PMIC through R94.
TP74	SW2OUT sense	SW2 output sense path. Connected directly to pin 30 (SW2FB) on PMIC through R95.
TP75	SW3OUT sense	SW3 output sense path. Connected directly to pin 7 (SW3FB) on PMIC through R96.
TP76	SW4OUT sense	SW4 output sense path. Connected directly to pin 6 (SW4FB) on PMIC through R97.
TP77	SW5OUT sense	SW5 output sense path. Connected directly to pin 12 (SW5FB) on PMIC through R98.

4.6 Connectors

4.6.1 V_{IN} input power connector

V_{IN} is supplied to the board through standard banana jacks.

Table 3. V_{IN} Banana connectors

Schematic label	Signal name	Description
J4	GND	Main system ground
J10	V_{IN}	Main system input power supply System operating range from 2.5 V to 5.5 V

4.6.2 Switching regulators output power connectors

Table 4. SW1 through SW5 output power connector

Schematic label	Signal name	Description
J34-1	SW1OUT	SW1 regulator output
J34-2	GND	System ground
J35-1	SW2OUT	SW2 regulator output
J35-2	GND	System ground
J36-1	SW3OUT	SW3 regulator output
J36-2	GND	System ground
J37-1	SW4OUT	SW4 regulator output
J37-2	GND	System ground
J38-1	SW5OUT	SW5 regulator output
J38-2	GND	System ground

4.6.3 Interface connector

Table 5. Master/slave interface connector (J3)

Schematic label	Signal name	Description
J3-1	RESETBMCU	Direct connection to RESETBMCU pin on board
J3-2	RESETBMCU_S	Connection to external RESETBMU signal from slave PMIC • RESETBMCU_S may be connected to local RESETBMCU pin through R12 (default)
J3-3	INTB	Direct connection to INTB pin on board
J3-4	INTB_S	Connection to external INTB signal from slave PMIC • INTB_S may be connected to local INTB pin through R10 (optional) • INTB_S may be connected to local XINTB pin through R8 (default)
J3-5	SYNCIN	Direct connection to SYNCIN pin on board.
J3-6	SYNCIN_S	Connection to external SYNCIN signal from slave PMIC • SYNCIN_S may be connected to local SYNCOUT pin through R9 (default)
J3-7	SYNCOUT	Direct connection to SYNCOUT pin on board
J3-8	n.c.	not connected
J3-9	XINTB	Direct connection to XINTB pin on board
J3-10	n.c.	not connected
J3-11	WDI	Direct connection to WDI pin on board
J3-12	WDI_S	Connection to external WDI signal from slave PMIC • WDI_S may be connected to local WDI pin through R7 (default)
J3-13	PWRON	Direct connection to PWRON pin on board
J3-14	PWRON_S	Connection to external PWRON signal from slave PMIC • PWRON_S may be connected to RESETBMCU pin through R11 (optional) • PWRON_S may be connected to PWRON pin through R6 (default)
J3-15	STANDBY	Direct connection to STANDBY pin on board
J3-16	STANDBY_S	Connection to external STANDBY signal from slave PMIC • STANDBY_S may be connected to STANDBY pin through R5 (default)
J3-17	SCL1	Direct connection to SCL1 signal on board
J3-18	SCL_S	Connection to external SCL signal from slave PMIC • SCL_S may be connected to SCL1 pin through R4 (default)
J3-19	SDA1	Direct connection to SDA1 signal on board
J3-20	SDA_S	Connection to external SDA signal from slave PMIC • SDA_S may be connected to SDA1 pin through R3 (default)
J3-21	TBBEN	Direct connection to TBBEN pin on board
J3-22	TBBEN_S	Connection to external TBB signal from slave PMIC • TBBEN_S may be connected to TBBEN2 signal controlled by MCU through R2 (default)
J3-23	XFAIL	Direct connection to XFAILB pin on board

Schematic label	Signal name	Description
J3-24	XFAIL_S	Connection to external XFAILB signal from slave PMIC • XFAILB_S may be connected to XFAILB signal on PMIC through R1 (default)

5 Software and firmware preparation

5.1 Installing NXPGUI on your computer

The KITPF7100FRDMEVM can use the NXPGUI for any of the PF7100 devices. Prior to the installation of the NXPGUI software and performing device firmware updates (if needed), download and unzip the NXP_GUI_PR_version.zip file to any desired location.

Open and run the NXP_GUI_version_Setup.exe file from the unzipped package. This installs the NXPGUI software in the system. Install it in a local destination folder.

The installation package is available at http://www.nxp.com/KITPF7100FRDMEVM.

5.2 Updating the PF7100 NXPGUI firmware

The FRDM-KL25Z freedom board is used to operate as a communication bridge to interface the NXPGUI with the PMIC and other I^2C devices. The firmware is organized in three levels:

1. At first level, the SDA uses the BOOTLOADER to operate as the main path to flash the functional code of the SDA processor. The BOOTLOADER is preprogrammed on the FRDM-KL25Z freedom boards and cannot be reflashed to avoid permanent damage to the Freedom board.
2. At second level, the SDA provides a *firmware loader* for quick drag and drop update of the KL25Z MCU firmware.
3. At the third level, the KL25Z MCU provides the NXPGUI firmware in charge of converting the USB communication into MCU instructions to control digital I/Os as well as I^2C communication to the PMIC.

If the FRDM-KL25Z is not loaded with the correct firmware to support a future software upgrade, the firmware can be updated in few simple steps.

Note: *The following firmware updates are optional and can be skipped if the firmware is up-to-date.*

5.2.1 Flashing the FRDM-KL25Z firmware loader

- Press the push button on the Freedom board and connect the USB cable into the SDA port on the Freedom board. A new BOOTLOADER device should appear on the left pane of the file explorer. This step is optional and should be performed only if the FRDM_KL25Z driver does not appear when the SDA port is connected.

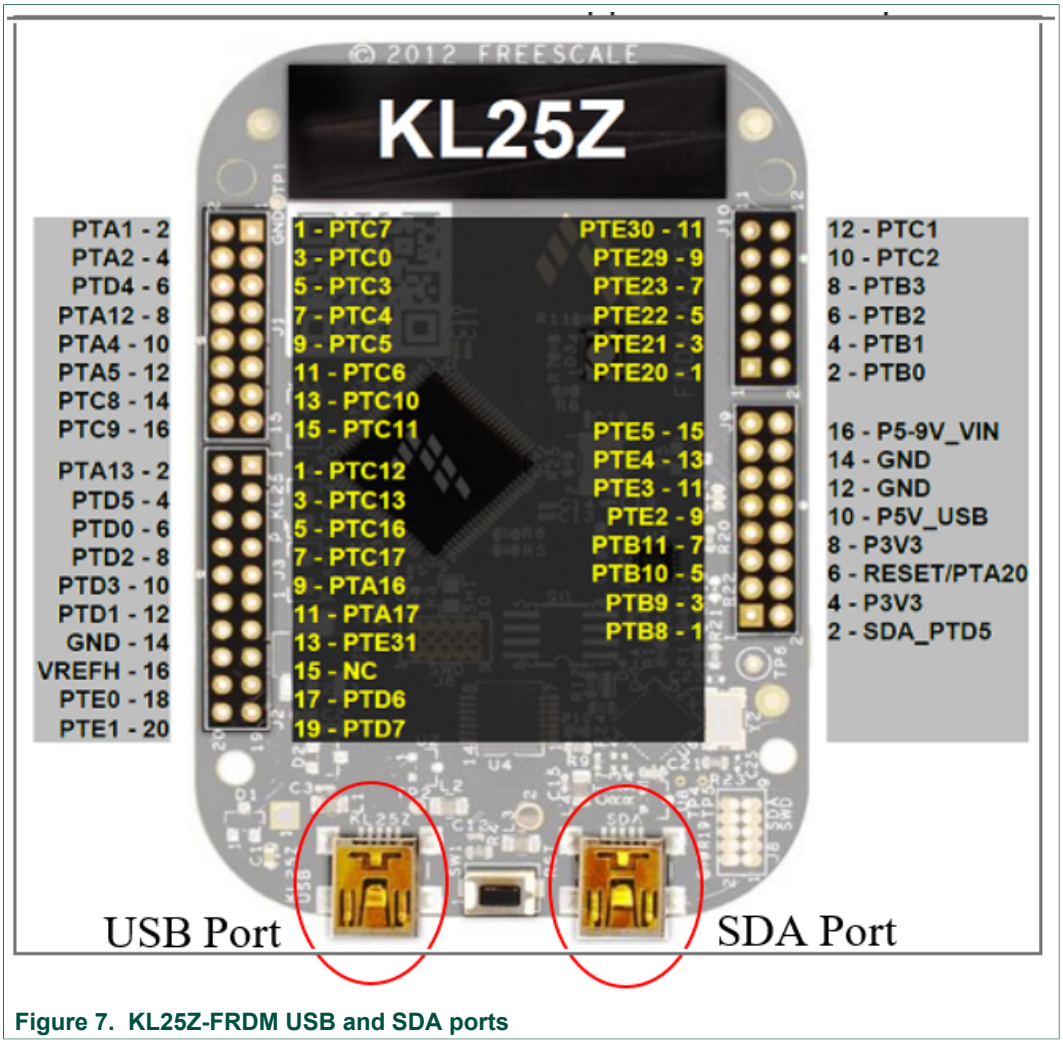


Figure 7. KL25Z-FRDM USB and SDA ports

- Drag and drop the file *MSD-DEBUG-FRDM-KL25Z_Pemicro_v118.SDA* into the BOOTLOADER drive. File should be located in the *KL25Z firmware* folder.
- Disconnect and reconnect the USB cable into the SDA port (this time without pressing the push button). A new device called *FRDM_KL25Z* is installed on the PC.

5.2.2 Flashing the NXPGUI firmware

If a new software or silicon release requires a firmware update on the FRDM-KL25Z freedom board, use the following steps to upgrade or downgrade the firmware of the freedom board as needed. Note that this procedure is needed only to update the firmware and may be skipped if no change is needed.

- Connect the USB cable in the SDA port (without holding the push button).The PC installs a new device called FRDM_KL25Z.
- Locate the ".bin" NXPGUI driver to be installed, for example *nxp-gui-fw-frdmkl25z-usb_hid-pf7100_version.bin* and drag and drop the file into the FRDM_KL25Z driver.
- Freedom board firmware is successfully loaded.

6 Configuring the hardware for startup

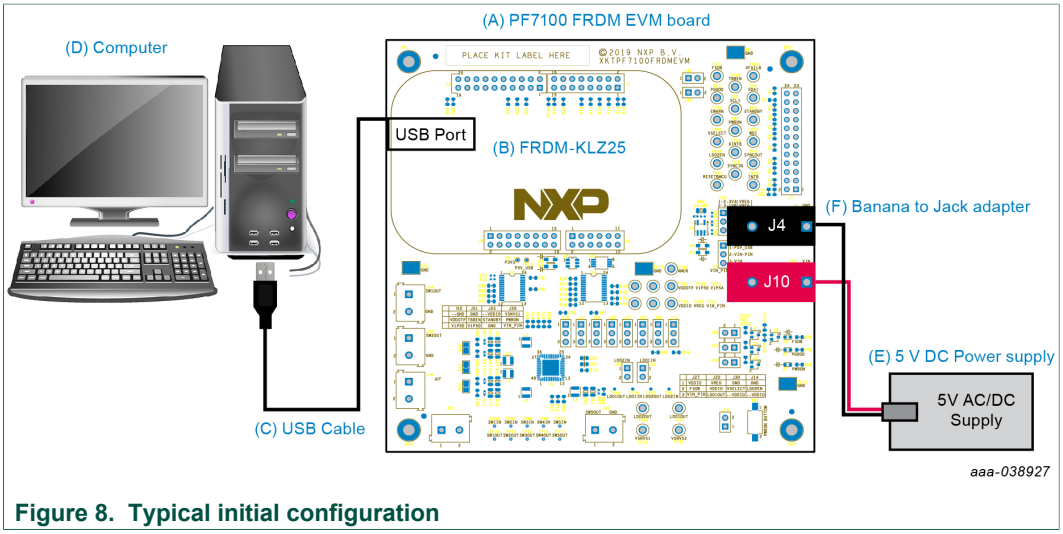


Figure 8. Typical initial configuration

1. Connect the USB cable from the PC to the USB port on the Freedom board, apply VIN to the evaluation board.
   - Provide external VIN between 3.0 V to 5.5 V on J10 (VIN) and J4 (GND).
     or
   - Short jumper J7 1-2 to provide 5.0 V Vin from Freedom board (use this mode of operation for functional demonstration only, no regulation loading allowed in this mode).
2. Open the NXPGUI application from the installation folder or from the **Start** menu to start the application.
3. The NXPGUI launcher is displayed with a list of possible configurations to load the NXPGUI. Select the appropriate option for device and silicon revision to be used. If the device revision populated on the KITPF7100FRDMEVM is not available in the list, contact your NXP representative to obtain the latest software update suitable for your device. Click **OK** to launch the NXPGUI.
4. Press **Reset** on the Freedom board, only if the board is not properly recognized.

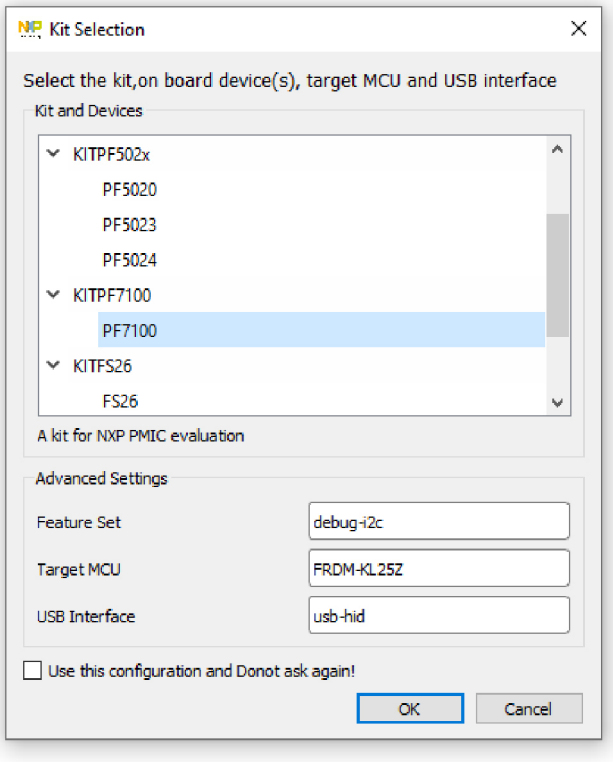
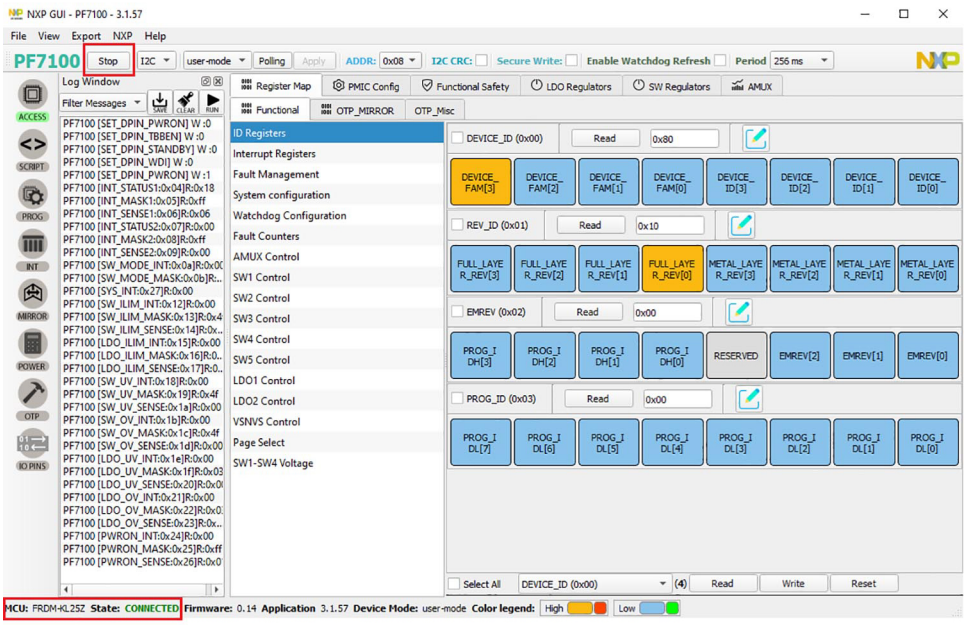


Figure 9. NXPGUI launcher

The USB-HID connection automatically searches for the KITPF7100FRDMEVM, if a valid board is connected. This is displayed by the active **Start** button on the top-left corner of the NXPGUI, then click **Start** to create a connection.

Figure 10. NXPGUI connection

The **Start** button changes to **Stop** after clicking. The device status can be read from the bottom-left corner of the NXPGUI.



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Once the device is connected, the system is ready for Hardwire or TBB operation as desired.

6.1 Operating in Hardwire mode

To operate the board with the default hardwire configuration:

- Open J29 and J26 to allow the MCU to control the PWRON pin
- Short J20 in position 2-3 (VDDOTP = V1P5D)
- Open J21 to allow the MCU to control the TBBEN pin

In Hardwire mode, the device is working with the predefined configuration, and the supplies turn On when the PWRON pin is set to high.

6.2 Operating in TBB mode

To operate the board in TBB mode:

- Open J29
- Short J20 in position 1-2 (OTP/TBB operation)
- Open J21 to allow the MCU to control the TBBEN pin

Use the TBB mode selection to enable access to the OTP mirror registers. Select the **tbb-mode** in main menu and click **Apply** button, the device moves to TBB mode.

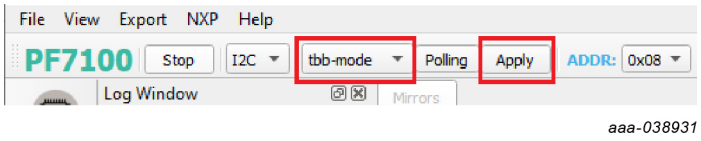

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Figure 11. TBB mode operation

When the device is operating in TBB mode, the NXPGUI uses command controls to communicate with the OTP mirror registers directly, enabling the user to set the configuration.

There are two ways to operate the device in TBB mode configurations:

1. Manual configuration of the OTP mirror registers using the **MIRROR** tab panel.
2. Run the TBB script on **SCRIPT** tab, the TBB script can be generated from **OTP** tab.

6.2.1 Manual TBB configuration

The **MIRROR** tab turns to be active on TBB mode. The user can click **Read All** button in **MIRROR** tab to read the mirror register contents from PF7100 device.

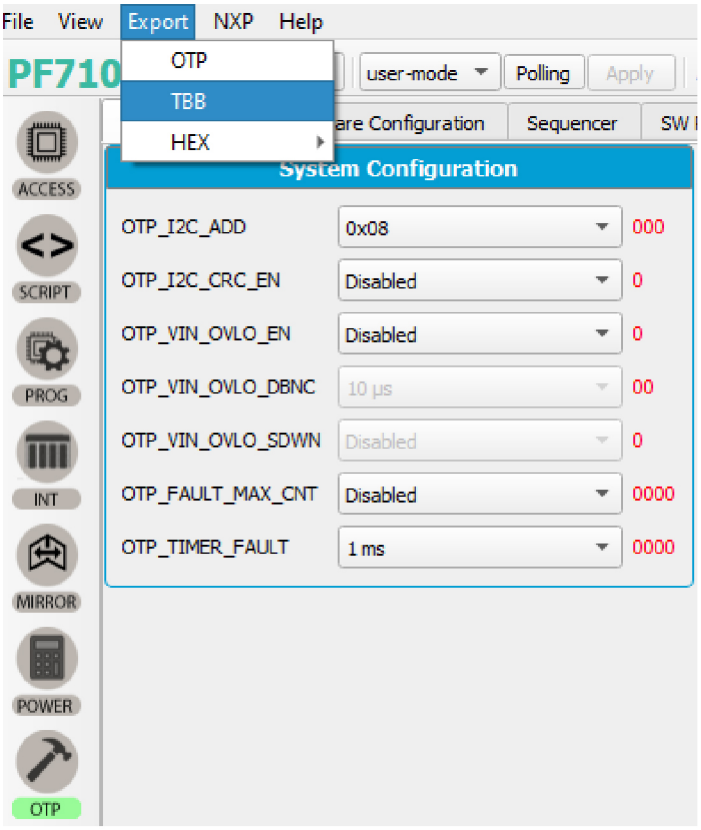
Use the drop-down boxes in **MIRROR** tab to select the mirror register values for PF7100 device. Click **Write** to implement the changes.

After configuring the features to be used during the device evaluation, change the operating mode to **user-mode** to generate a power on event and allow command controls to modify the functional I^2C registers again.

6.2.2 Generate script for TBB Configuration

To load the OTP mirror registers from a TBB script, the user can choose the device configuration and generate the TBB script with the NXPGUI **OTP** tab.

1. Set the desired OTP configuration using the down-down box in **OTP** tab panel. If there is a predefined OTP configuration script, the user can load it by clicking the **Import** button.
2. Select **TBB** bar from the **Export** tab in the menu and save the generated TBB file(.txt) in a known location with a desired filename.



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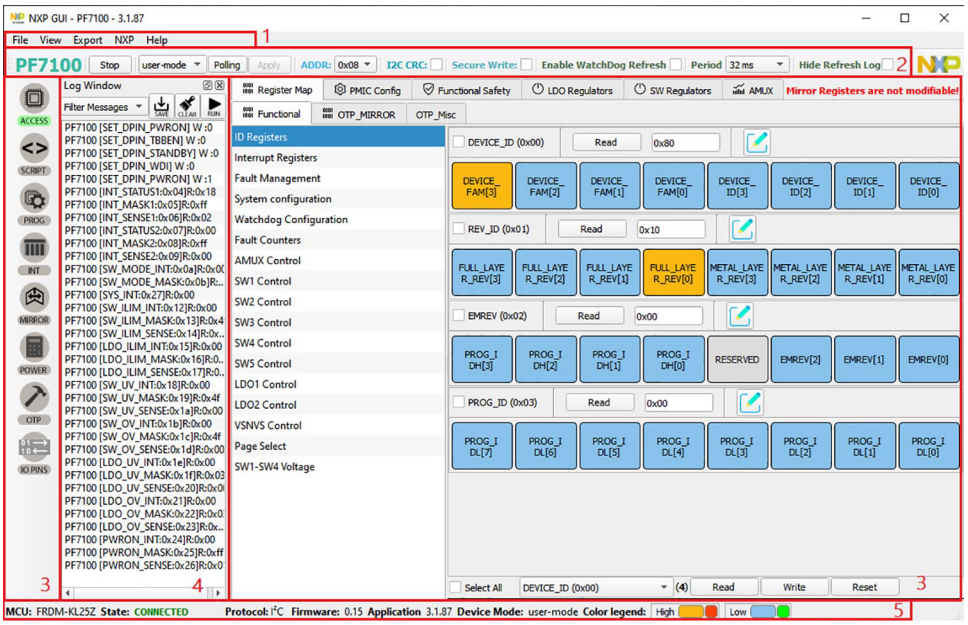
3. On the **SCRIPT** tab and **Script Commands Window** panel, click **OPEN** to load the TBB script created, and then click **Run** to start programming the PMIC. The TBB script contains commands that control the device to move into TBB mode and to write the mirror register values.

The device is automatically powered On with the selected TBB configuration after the programming is done.

7 The NXPGUI functional areas

Launch the NXPGUI and select PF7100 device, the NXPGUI workspace window is divided into five functional areas.



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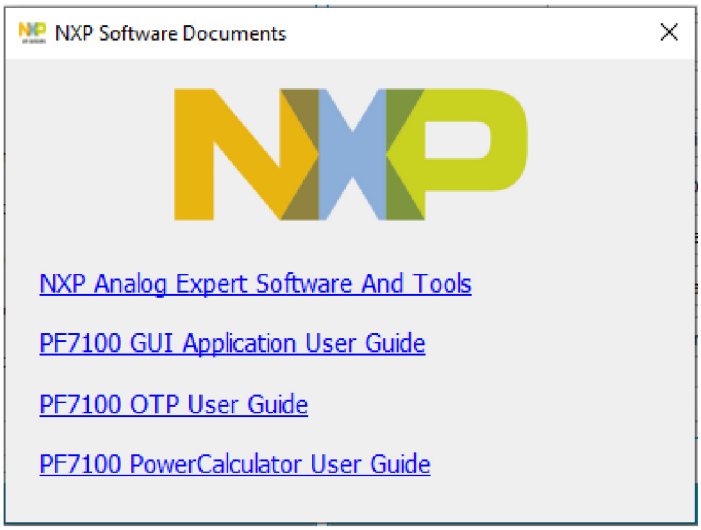
1. Main menu
2. Connection toolbar
3. Functional control area
4. Command log window
5. Status bar

Figure 12. NXPGUI functional areas

Go to **Help** in the main menu, and then click the **Documentation** bar to open the NXPGUI guide. The guide provides information on how to control the PMIC.



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The following sections introduce the main functions defined by each functional area.

7.1 Main menu

The main menu contains: load or save the OTP config file (.cfg), NXPGUI layout view selection, export OTP/TBB/HEX script, tool help documentation, and exit NXPGUI functions.

7.2 Connection toolbar

The connection toolbar contains the device start/stop connection button, device mode selection box, device I^2C address selection drop-down box, I^2C CRC enable checkbox, and cycling watchdog refresh checkbox functions.

7.3 Functional control area

The functional control area consists of several tabs.

- **ACCESS** tab: for the device functional registers and mirror registers access. The mirror registers are accessible in TBB mode.
- **SCRIPT** tab: for the scripts generation and run.
- **PROG** tab: for the device OTP programming. This tab contents are active in TBB mode. The config source is selectable from either the OTP configuration on NXPGUI **OTP** tab or an OTP script browsing from user's path.
- **INT** tab: to monitor/clear the device interruptions, set/clean the interruption masks. This tab contents are active in user mode.
- **MIRROR** tab: to read, write, and export the device mirror register values. This tab contents are active in TBB mode.
- **POWER** tab: to evaluate the device power dissipation with given loadings and configurations.
- **OTP** tab: to define the OTP configurations for the application. The user can save the configuration with the .cfg file or load the .cfg file to this page to check the OTP contents. This tab is available with the board either online or offline.
- **IO PINS** tab: to read and set the IO pins status.

7.4 Command log window

The command log area informs the user about application events. Verbosity level is given by application configuration. User can interact with the area using toolbar on the top, which has following functions: filter messages, save log and clean log.

7.5 Status bar

The status bar provides an overview of application conditions, including the MCU status, software version area, device current mode, and the color legend shown on the NXPGUI.

8 References

[1] **KITPF7100FRDMEVM** — detailed information on this board, including documentation, downloads, and software and tools
http://www.nxp.com/KITPF7100FRDMEVM

[2] **PF7100** — product information on multi-channel power management integrated circuit
https://www.nxp.com/products/PF7100

9 Revision history

Revision history

Rev	Date	Description
v.1	20200915	Initial version

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