UM11162 KITPF8200FRDMPGM programming board Rev. 1.0 — 23 April 2019

User guide





Introduction

This document is the user guide for the KITPF8200FRDMPGM programming board. This document is intended for the engineers involved in the evaluation, design, implementation, and validation of PF81/82 multi-channel power management integrated circuit.

The scope of this document is to provide the user with information to program the PF81/82 multi-channel power management integrated circuit. This document covers connecting the hardware, installing the software and tools, configuring the environment and using the kit.

Table 1. Device support

PMIC device	Qualification level	Link
PF8100/PF8200	Automotive/Industrial	http://www.nxp.com/PF8100-PF8200
PF8101/PF8201	Automotive/Industrial	http://www.nxp.com/PF8101-PF8201
PF8121	Consumer	http://www.nxp.com/PF8121

1 Finding kit resources and information on the NXP web site

NXP Semiconductors provides online resources for this programming board and its supported device(s) on <u>http://www.nxp.com</u>.

The information page for KITPF8200FRDMPGM programming board is at <u>https://www.nxp.com/KITPF8200FRDMPGM</u>. The information page provides overview information, specifications, ordering information, documentation and software. The **Documents and Software** tab provides quick-reference information applicable to using the KITPF8200FRDMPGM programming board, including the downloadable assets referenced in this document.

1.1 Collaborate in the NXP community

The NXP community is for sharing ideas and tips, ask and answer technical questions, and receive input on just about any embedded design topic.

The NXP community is at http://community.nxp.com.

2 Getting ready

Working with the KITPF8200FRDMPGM requires the kit contents and a Windows PC workstation with installed software.

2.1 Kit contents

- Assembled and tested KITPF8200FRDMPGM and preprogrammed FRDM-KL25Z microcontroller board in an anti-static bag
- 3.0ft. USB-STD A to USB-B-mini cable
- Quick Start Guide

2.2 Windows PC workstation

This programming board requires a Windows PC workstation with the following specifications

• USB-enabled computer with Windows 7, Windows 8, or Windows 10

2.3 Software

Installing software is necessary to work with this programming board. All listed software is available on the programming board's information page at https://www.nxp.com/kitPF8200FRDMPGM.

Software package NXP_FlexGUI_PF8x_Rev_0.7.x contains:

- KL25Z firmware files
- NXP PF8x FlexGUI

3 Getting to know the hardware

The NXP OTP programming boards provide an easy-to-use platform for programming the default configuration of the NXP PF81/82 power management products. The boards support all voltages and signals needed for OTP programming.

3.1 Kit overview

The KITPF8200FRDMPGM is a programming board featuring a 56-pin QFN socket compatible with all PF81/82 PMICs. The kit integrates all hardware needed to program the OTP registers in the PMIC.

It integrates a communication bridge based on the FRDM-KL25Z freedom board to communicate with the FlexGUI software interface to program the OTP configuration.

3.1.1 KITPF8200FRDMPGM features

Programming socket

• Clamshell 56-pin QFN socket

System features

- 5.0 V operating input voltage range (from USB connector)
- · Integrated boost converted to supply VDDOTP programming voltage
- USB to I²C communication via the FRDM-KL25Z interface
- Inline programming interface connector

3.2 Kit featured components

Figure 2 identifies important components on the KITPF8200FRDMPGM board.

KITPF8200FRDMPGM programming board



3.2.1 Supported PMICs

The PF81/82 family of devices feature power management integrated circuit (PMIC) designed for high performance i.MX 8 and S32V based applications. It features various devices with multiple high efficiency buck converters with the ability to operate in single or multiphase configuration as well as various linear regulators with selectable switch mode configuration.

Built-in one time programmable memory stores key startup configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed I²C after start up offering flexibility for different system states.

The PF81/82 family comprises five devices to address different market needs:

- PF8200 is the flagship version of this family providing a full feature PMIC with seven switching regulators and four LDOs, integrating functional safety mechanism to comply with the ISO 26262 standard and providing a powerful and flexible solution for ASIL B(D) automotive modules.
- PF8100 is the non-safety version of the higher end device, it features seven switching regulators and four LDOs, providing all the power management and digital control included in PF8200, without the functional safety overhead to provide a more economic platform for systems not required to meet the ASIL B qualification.
- PF8121 is the consumer version of the higher end device, it features seven switching regulators and four LDOs, providing same power management and digital control with

KITPF8200FRDMPGM programming board

standard consumer qualification rating to address a more cost effective platform for consumer applications.

- PF8201 is a reduced version of this PMIC, featuring five switching regulators and three LDOs, integrating functional safety mechanism to comply with the ISO 26262 standard and providing a powerful and flexible solution for lower end ASIL B(D) automotive modules.
- PF8101 is the non-safety version of the PF8201 device, it features five switching regulators and three LDOs, providing power management and digital control for lower end application, without the functional safety overhead to provide a more economic platform for systems not required to meet the ASIL B qualification.

All devices provide pin-to-pin compatibility on a small profile 8 x 8 mm, 56-pin QFN package compatible with the clamshell socket featured in the KITPF8200FRDMPGM.

3.3 Schematic, board layout and bill of materials

The board layout and bill of material for the KITPF8200FRDMPGM are available at <u>https://www.nxp.com/KITPF8200FRDMPGM</u>.

KITPF8200FRDMPGM programming board



KITPF8200FRDMPGM programming board



UM11162 User guide

KITPF8200FRDMPGM programming board



Figure 5. Jumper headers and connectors

3.4 Default jumper configurations

Table 2. KITPF8200FRDMPGM jumper locations

Name	Default	Description
J1, J2, J3, J4	—	Freedom board interface
J5	Shorted	Add VDDOTP external capacitance
J6	Shorted	Force VDDIO supply to 3.3 V from FRDM-KL25Z
J7	Disconnected	External VIN supply
8L	1-2 shorted	 KITPF8200FRDMPGM input supply selection 1-2 shorted: select USB 5.0 V from FRDM-KL25Z as input 3-4 shorted: select 3.3 V from FRDM-KL25Z as input

KITPF8200FRDMPGM programming board

Name	Default	Description
J10	Open	 PWRON voltage selection 1-2 shorted: force PWRON high 2-3 shorted: force PWRON low Open: allow MCU to control PWRON pin
J12	Open	Force VDDOTP to ground
J13	Open	 TBBEN voltage selection 1-2 shorted: force TBBEN high 2-3 shorted: force TBBEN low Open: allow MCU to control TBBEN pin
J14	Open	 Force VIN for the boost converter 1-2: disconnect VIN from the boost converter 2-3: force VIN to supply the boost converter Open: allow the MCU to control the boost input voltage supply
J15	—	Inline programming connector

3.5 Inline programming interface configuration

In order to provide connectivity for programming of a PF81/82 device on a target board, a set of jumper wires have been provided.



For systems that require inline programming capabilities, the following circuits should be provided in order to be able to interface with the KITPF8200FRDMPGM programming board via the interface connector.

KITPF8200FRDMPGM programming board



UM11162 User guide

Note: Inline programming interface connector may require to mirror signals depending on the cable configuration used to connect with the KITPF8200FRDMPGM programmer.

Note: Configuration signal may require isolation from the main system in order to allow proper communication with the PMIC during OTP programming procedure. Such isolation may be achieved via 1x2 pin header, 0Ω resistor or a dip switch array.

Note: TBBEN2 and GPIO pins in KITPF8200FRDMPGM interface connector are intended for advance system configuration connection as needed.

Note: Make sure to use a connector cable 8 inch or shorter to communicate between the KITPF8200FRDMPGM and the target board.

3.6 Test points

The following test points provide access to various signals to and from the board.

Test point name	Signal name	Description
Digital I/O signal		
TP1	VIN	Connected to pin 50 (VIN) on the socket
TP2	VDDIO	Connected to pin 54 (VDDIO) on socket
TP3	VDDOTP	Connected to pin 53 (VDDOTP) on the socket
TP4	V1P5A	Connected to pin 41 (V1P5A) on the socket
TP5	V1P5D	Connected to pin 40 (V1P5D) on the socket
TP6	SDA	Connected to pin 56 (SDA) on PMIC. Main system I ² C bus.
TP7	SCL	Connected to pin 55 (SCL) on PMIC. Main system I ² C bus.
TP8	TBBEN1	Connected to pin 14 (TBBEN) on the socket
TP9	PWRON	Connected to pin 22 (PWRON) on the socket
TP10	VDDOTPEN	Connected to VDDOTP enable FET on the boost converter block
TP11	TBBEN2	Connected to pin 3 (TBBEN2) on the inline programming connector provided to support dual PMIC programming when performing inline programming
Ground test points		
TP12, TP13, TP14, TP15	GND	Ground plane test points

Table 3. KITPF8200FRDMPGM test points

4 Installing and configuring software and tools

The KITPF8200FRDMPGM uses FlexGUI software for any of the PF81/82 devices. Prior to the installation of the FlexGUI software and performing device firmware updates (if needed), download and unzip the NXP_FlexGUI_PF8x_REV_0.7.x.zip file in a desired location.

The installation package is available at https://www.nxp.com/KITPF8200FRDMPGM.

4.1 Installing the Java JRE

1. Download Java JRE (Java SE Runtime Environment), available at <u>http://www.oracle.com/technetwork/java/javase/downloads/jre8-downloads-2133155.html</u> (8u162 or newer).

KITPF8200FRDMPGM programming board

- 2. Open the installer and follow the installation instructions.
- 3. Following the successful installation, restart the computer.

4.2 Installing FlexGUI software package

The FlexGUI software installation requires only extracting the zip file in a desired location.

- 1. If necessary, install the Java JRE and Windows 7 FlexGUI driver.
- 2. Download the latest FlexGUI (32-bit or 64-bit) version, NXP_FlexGUI_PF8x_REV_0.7.x.zip, available at <u>www.nxp.com/</u> <u>KITPF8200FRDMPGM</u>.
- 3. Extract all the files to a desired location on your PC.

FlexGUI is started by running the batch file, NXP_FlexGUI_PF8x_Rev_0.7.x\NXP FlexGUI\bin\flexgui-app-pf8xxxx.bat.

The FlexGUI Rev 0.7.0 or higher, interfaces with the FRDM-KL25Z freedom board via USB-HID protocol which should be recognized automatically by the Windows OS eliminating the need for any extra hardware drivers. See <u>Section 4.4 "Updating the PF81/82 FlexGUI firmware"</u> for details on how to install or update the FRDM-KL25Z, in case the board is not loaded with the latest firmware and USB-HID support.

4.3 Uninstalling the application

The FlexGUI software does not store any files outside of its installation folder.

To uninstall FlexGUI, delete the flexgui.

4.4 Updating the PF81/82 FlexGUI firmware

The FRDM-KL25Z freedom board is used as a communication bridge to interface the FlexGUI with the PMIC and other I^2C devices. The firmware is organized in three levels:

- 1. At first level, the SDA uses the BOOTLOADER to operate as the main path to flash the functional code of the SDA processor. The BOOTLOADER is preprogrammed on the FRDM-KL25Z freedom boards and cannot be reflashed to avoid permanent damage to the Freedom board.
- 2. At second level, the SDA provides a *firmware loader* for drag and drop update of the KL25Z MCU firmware.
- At the third level, the KL25Z MCU provides the FlexGUI firmware in charge of converting the USB communication into MCU instructions to control digital I/Os as well as I²C communication to the PMIC.

If the FRDM-KL25Z is not loaded with the correct firmware to support a future software upgrade, the firmware can be updated in few simple steps.

Note: The following firmware updates are optional and can be skipped if the firmware is up-to-date.

4.4.1 Flashing the FRDM-KL25Z firmware loader

 Press the push button on the Freedom board and connect the USB cable into the SDA port on the Freedom board. A new BOOTLOADER device should appear on the left pane of the file explorer. This step is optional and should be performed only if the FRDM_KL25Z driver does not appear when the SDA port is connected.

KITPF8200FRDMPGM programming board



2. Drag and drop the file *MSD-DEBUG-FRDM-KL25Z_Pemicro_v118.SDA* into the BOOTLOADER drive. File should be located in the *KL25Z firmware* folder.

📙 🔄 🚽 🗧 KL25Z firmware					-		\times
File Home Share Vi	2W						~ ?
\leftarrow \rightarrow \checkmark \uparrow \blacksquare $<$ NXP_Flex	GUI_PF8200_Rev_0	0.8.0 > KL25Z firmware	~ Ü	Sear	ch KL25Z firmware		٩
		Name			Date modified	Туре	
Quick access		🧧 flexgui-fw-kl25z-usb-hid-pf8x00-v0.1.1.bin			2/15/2019 3:48 PM	BIN File	
Downloads	*	MSD-DEBUG-FRDM-KL25Z_Pemicro_v118.SDA			12/13/2015 7:43 PM	SDA File	
esktop	*						
NXP							
🝊 OneDrive - NXP							
SNXL12029							
🕩 Network							
		<					>
2 items 1 item selected 198 K	3					E	=

3. Disconnect and reconnect the USB cable into the SDA port (this time without pressing the push button). A new device called *FRDM_KL25Z* is installed on the PC.

4.4.2 Flashing the FlexGUI firmware

If a new software or silicon release requires a firmware update on the FRDM-KL25Z freedom board, use the following procedure to upgrade or downgrade the firmware of the freedom board as needed. Note that this procedure is needed only to update the firmware and may be skipped if no change is needed.

- 1. Connect the USB cable in the SDA port (without holding the push button).
- 2. Locate the ".bin" FlexGUI driver to be installed, for example *flexgui-fw-kl25z-usb-hid-pf8x00-v0.1.1.bin*, drag and drop the file into the FRDM_KL25Z driver.



3. Freedom board firmware is successfully loaded.

5 Configuring the hardware



Figure 9 presents a typical hardware configuration incorporating the development board and Windows PC workstation.

To configure the hardware and workstation as illustrated in <u>Figure 9</u>, complete the following procedure:

1. Plug the KITPF8200FRDMPGM board on top of the FRDM-KL25Z board.

- For standalone chip programming: introduce a PF8x QFN device in the socket (ensure pin 1 is properly aligned)
- For inline programming: connect the interface connector to the system board and ensure VIN power is provided either from the programmer or at the system board. Ensure SCL and SDA pins are connected only to the PMIC and isolated from the system bus to avoid the unpowered system from pulling down/up the signal causing communication problems.
- 2. Connect the USB cable from the PC to the USB port on the Freedom board.Verify that the board is receiving power (green LED is lit).
- 3. Press **Reset** button on the Freedom board, to ensure board is properly recognized.

6 Generating OTP configuration

- 1. Choose the desired OTP configuration using the corresponding *PF8xxx Custom OTP Request Form* file provided in the *Scripts and Forms* folder. Make sure to use the correct form and device number matching the samples to be programmed.
- 2. Ensure the device name is set to the same device in the FlexGUI launcher in order to generate the correct commands to interface with the FlexGUI script editor.
- Generate an OTP script using the file generation section on the OTP request form, make sure to fill all required fields marked with a * to enable the file generation. Also, select the **PF8x Programmer** option to generate the proper code for OTP programming using the KITPF8200FRDMPGM programmer.



4. Save the generated OTP file in a known location.

7 **Programming OTP configuration with the FlexGUI**

After connecting the KITPF8200FRDMPGM board, use the following steps to program the OTP configuration in the target PF81/PF82 device.

7.1 Starting the FlexGUI application

1. Browse to the *NXP_FlexGUI/bin/* folder and double-click on the **flexgui-app-8xxx.jar** executable to start the application.

2. After FlexGUI is launched with the flexgui-app.bat file, the FlexGUI launcher displays available kits. Select the configuration option matching the device to be programmed, i.e. PF8100, PF8200, PF801, PF8201, or PF8121.

If the device revision populated on the KITPF8200FRDMPGM is not available in the list, please contact your NXP representative to obtain the latest software update suitable for your device.

NP FlexGUI Launcher	×
Select a kit, device(s) and its features	
Kit and device(s) KITPF8200FRDMEVM PF8200 B0 Release KITPF8201FRDMEVM KITPF8100FRDMEVM KITPF8101FRDMEVM KITPF8101FRDMEVM KITPF8121FRDMEVM KITPF8121FRDMEVM A kit for PF8200 evaluation.	
 Advanced settings Features production Use this configuration and do not ask again 	
ОК	Cancel

3. When the FlexGUI is done loading, the USB-HID connection will automatically search for the KITPF8200FRDMPGM, if a valid board is connected, the corresponding *Vendor ID* and *Product ID* should appear, then click **Start** to create a connection.

KITPF8200FRDMPGM programming board



Once the device is connected, the system is ready to perform the OTP programming using the script editor.

7.2 Loading OTP script

- 1. To begin the OTP configuration on the PMIC, select the **Script Editor** tab and load the OTP script generated with the OTP request form spreadsheet.
- 2. Run the OTP script and wait for the GUI to finish the burning sequence.

Device: FRB&xx Alias: ··No values ····································	PFBxxxx Script editor		
Alias: • No values • • Digital pins // Cutomer. NXP // Pogarn. (Ladd the Projec Name for this Request] // Sample marking: MG3PF8100CCES // Bagisters // Jotte: 2/25/2019 * Mode SET_DPIN/PF8.002WD01/ow SET_DPIN/PF8.002WD01/ow SET_DPIN/PF8.002WD01/ow SET_DPIN/PF8.002WD01/ow SET_DPIN/PF8.002WD01/ow SET_DPIN/PF8.002WD01/ow SET_DPIN/PF8.002WD01/ow SET_DPIN/PF8.002WD01/ow SET_DPIN/PF8.002WD01/ow SET_DPIN/PF8.002WD01/ow SET_DPIN/PF8.002WD01/PKNigh SET_REG/PF8.0007TP_MIRROR.01TP_CTRL2.0x0 SET_REG/PF8.0007TP_MIRROR.01TP_CTRL2.0x0 SET_REG/PF8.00007P_MIRROR.01TP_CTRL2.0x0 SET_REG/PF8.00007P_MIRROR.01TP_CTRL2.0x0 SET_REG/PF8.00007P_MIRROR.01TP_CTRL2.0x0 SET_REG/PF8.00007P_MIRROR.01TP_CTRL2.0x0 SET_REG/PF8.00007P_MIRROR.01TP_CTRL2.0x0 SET_REG/PF8.00007P_MIRROR.01TP_CTRL2.0x0 SET_REG/PF8.00007P_MIRROR.01TP_CTRL2.0x0 SET_REG/PF8.00007P_MIRROR.01TP_VND_D.0UVTRE0.0x0 SET_REG/PF8.00007P_MIRROR.01TP_VND_D.0UVTRE0.0x0 SET_REG/PF8.00007P_MIRROR.01TP_VND_D.0UVTRE0.0x0 SET_REG/PF8.00007P_MIRROR.01TP_FWRLD_D.0UVTRE0.0x0 SET_REG/PF8.00007P_MIRROR.01TP_VND_D.0UV1.000 SET_REG/PF8.00007P_MIRROR.01TP_FWRLD_D.0UV1.000 SET_REG/PF8.00007P_MIRROR.01TP_MIRDR.01UV1.000 </th <th>Device: PFBxxxx</th> <th>Commands:</th> <th>Results:</th>	Device: PFBxxxx	Commands:	Results:
SET_REG.PF8.d00.OTP_MIRROR.OTP_WD_EXPIRE.06.07 SET_REG.PF8.d00.OTP_MIRROR.OTP_VBU_COUNTER.06.4F SET_REG.PF8.d00.OTP_MIRROR.OTP_FAULT_TUNERS.000 SET_REG.PF8.d00.OTP_MIRROR.OTP_WRUD_DLV3.040 SET_REG.PF8.d00.OTP_MIRROR.OTP_WRUD_DLV3.040 SET_REG.PF8.d00.OTP_MIRROR.OTP_PWRUD_DLV3.041 SET_REG.PF8.d00.OTP_MIRROR.OTP_PWRUD_DLV3.041 SET_REG.PF8.d00.OTP_MIRROR.OTP_WRUD_DLV3.041 SET_REG.PF8.d00.OTP_MIRROR.OTP_WRUD_DLV3.041 SET_REG.PF8.d00.OTP_MIRROR.OTP_WRUD_DLV3.041 SET_REG.PF8.d00.OTP_MIRROR.OTP_WRUD_DLV3.041 SET_REG.PF8.d00.OTP_MIRROR.OTP_WRUD_DLV3.041 SET_REG.PF8.d00.OTP_MIRROR.OTP_MRUD_DLV3.041 SET_REG.PF8.d00.OTP_MIRROR.OTP_MRUD_DLV3.041 SET_REG.PF8.d00.OTP_MIRROR.OTP_MRUD_DLV3.041 SET_REG.PF8.d00.OTP_MIRROR.OTP_MRUD_DLV3.041 SET_REG.PF8.d00.OTP_MIRROR.OTP_MRUD_DLV3.041 SET_REG.PF8.d00.OTP_MIRROR.OTP_MRUD_DLV3.041 SET_REG.PF8.d00.OTP_MIRROR.OTP_MRUD_DLV3.041 SET_REG.PF8.d00.OTP_MIRROR.OTP_MRUD_DLV3.041 SET_REG.PF8.d00.OTP_MIRROR.OTP_MRUD_DLV3.041 SET_REG.PF8.d00.OTP_MIRROR.OTP_MRUD_DLV3.041 SET_REG.PF8.d00.OTP_MIRROR.OTP_MRUD_DLV3.041 SET_REG.PF8.d00.OTP_MIRROR.OTP_MRUD_DLV3.041 SET_REG.PF8.d00.OTP_MIRROR.OTP_MRUD_DLV3.041 SET_REG.PF8.d00.OTP_MIRROR.OTP_MRUD_DLV3.041 SET_REG.PF8.d00.OTP_MIRROR.OTP_MRUD_DLV3.041 SET_REG.PF8.d00.OTP_MIRROR.OTP_MRUD_DLV3.041 SET_REG.PF8.d00.OTP_MIRROR.OTP_MRUD_DLV3.041 SET_REG.PF8.d00.OTP_MIRROR.OTP	Device: PFBaxx Alias: No values > Digital pins > Analog pins > Registers > Mode > Generator	Commands: // Device Configuration: PF8100 // Customer: NXP // Program: [Add the Projec Name for this Request] // Sample marking: MC33PF8100CCES // Date: 2/25/2019 // Time: 10:12:28 PM // Generated from Spreadsheet Revision: Rev 3.3 SET_DPIN>PF8:00:PBK00N20MOW SET_DPIN>PF8:00:TBBENhigh SET_DPIN>PF8:00:TBBENhigh SET_DPIN>PF8:00:TBBENhigh SET_DPIN>PF8:00:TBBENhigh SET_DPIN>PF8:00:TBBENhigh SET_DPIN>PF8:00:TBBENhigh SET_REG/PF8:00:OTP_MIRROR:OTP_IS:08_SELECT:0x:00 SET_REG/PF8:00:OTP_MIRROR:OTP_IS:08_SELECT:0x:00 SET_REG/PF8:00:OTP_MIRROR:OTP_IS:08_SELECT:0x:00 SET_REG/PF8:00:OTP_MIRROR:OTP_CTRL:0x:05 SET_REG/PF8:00:OTP_MIRROR:OTP_MIRROR:0TP_CTRL:0x:05 SET_REG/PF8:00:OTP_MIRROR:0TP_MIRC:0TP_CTRL:0x:05 SET_REG/PF8:00:OTP_MIRROR:0TP_MIRC:0TP_MIRC:0TP_MIRC:0TP_MIRC:0TP_MIRC:0TP_MIRC:0TP_MIRC:0TP_MIRC:0TP	Results:
		SET_REGPF8A00-OTP_MIRROR-OTP_WO_CONTROUDD SET_REGPF8A00-OTP_MIRROR-OTP_WO_COUNTER/0A4F SET_REGPF8A00-OTP_MIRROR-OTP_KAULC_OUNTER/0A4F SET_REGPF8A00-OTP_MIRROR-OTP_FAULT_TIMERS:0A0F SET_REGPF8A00-OTP_MIRROR-OTP_FAULT_TIMERS:0A0F SET_REGPF8A00-OTP_MIRROR-OTP_PAURON_UV1:0A00 SET_REGPF8A00-OTP_MIRROR-OTP_MIRROR-OTP_PAURON_UV1:0A00 SET_REGPF8A00-OTP_MIRROR-OTP	GUI: 0.9.1 FW: 0.1.0 Wed Apr 10 08:47:30 MST 2019 🔗

- 3. To verify proper configuration of the device, stop the communication with the device, disconnect and reconnect the USB cable, and establish connection with the board again (this process is needed to ensure the PMIC has a complete power cycle and the new OTP configuration is loaded in the Mirror registers).
- 4. Use the *Read Customer OTP Mirror Registers* provided in the *Scripts and Forms* folder.
- 5. First command provides the device ID
 - PF8100 = 0x40

- PF8200 = 0x48
- PF8101 = 0x41
- PF8201 = 0x49
- PF8121 = 0x42
- 6. Last two commands verify the proper programming of the Mirror register sector status. If SECT_STATUS = 0x3F & FSTATUS = 0x00, the part is programmed correctly.
- 7. All other lines output the programmed value of the Mirror registers.

Note: The OTP programming script generated with the PF8x00_OTP_Request_Form Rev 3.2 or higher provides an update in the verification code that enables a valid programming self-check without the need to follow steps 3 to 7.

KITPF8200FRDMPGM programming board

8 References

[1] **KITPF8200FRDMPGM** — detailed information on this board, including documentation, downloads, and software and tools

http://www.nxp.com/KITPF8200FRDMPGM

- [2] **PF8100/PF8200** product information on multi-channel power management integrated circuit <u>http://www.nxp.com/PF8100-PF8200</u>
- [3] **PF8101/PF8201** product information on multi-channel power management integrated circuit <u>http://www.nxp.com/PF8101-PF8201</u>
- [4] **PF8121** product information on multi-channel power management integrated circuit <u>http://www.nxp.com/PF8121</u>

9 Revision history

Revision	history
----------	---------

Rev	Date	Description
v.1	20190423	Initial version

KITPF8200FRDMPGM programming board

10 Legal information

10.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

10.2 Disclaimers

Limited warranty and liability - Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a

default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer. In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages. Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US\$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

10.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

NXP — is a trademark of NXP B.V.

KITPF8200FRDMPGM programming board

Tables

Tab. 1.	Device support2
Tab. 2.	KITPF8200FRDMPGM jumper locations9

Figures

Fig. 1.	KITPF8200FRDMPGM	1
Fig. 2.	KITPF8200FRDMPGM featured component	
	locations	5
Fig. 3.	PMIC socket connections	7
Fig. 4.	VDDOTP boost converter	3
Fig. 5.	Jumper headers and connectors	9

Fig. 6.	Inline programming interface connector	10
Fig. 7.	PMIC control signals	11
Fig. 8.	Programming interface	11
Fig. 9.	Typical initial configuration	15
Fig. 10.	FlexGUI connection	18