Kneron KL720series AI SoC

Demo Board (BGA269, 9x9)

Product Information

Revision History:

version	description	date
0.1	Initial version	2020/09/21
1.0	Update Pic.	2020/12/07
1.1	Update boost table	2020/12/23
1.2	Modify Peripherals List	2021/1/12

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1. Overview

1.1 General description

Kneron KL720 series is an AI SoC targeting smart-home and IoT segment with Kneron NPU core inside to accelerate neural network processing and enabling devices with edge AI ability to achieve Kneron's AI everywhere vision.

This document describes how to use the KL720 AI SoC Development Kit (BGA269, 9x9).

2. Hardware description

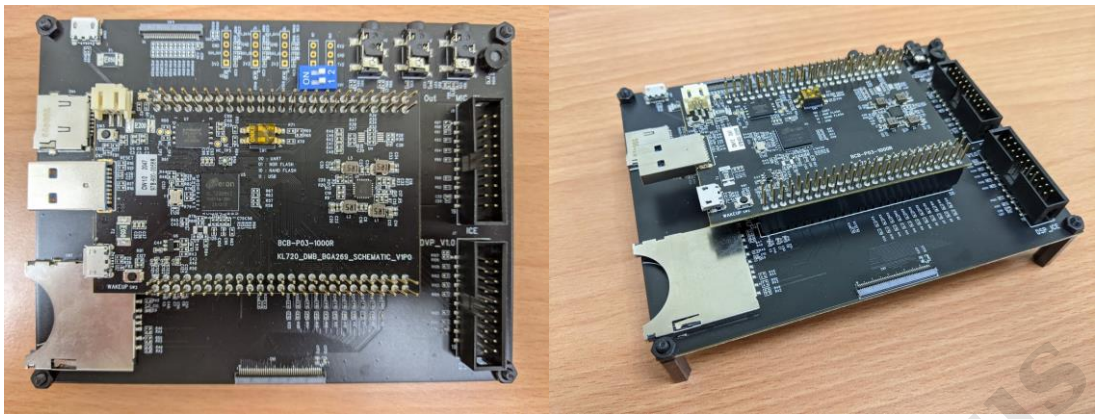
2.1 Product SPEC

Product name	**Kneron KL720 series AI SoC Development Kit (BGA269, 9x9)**
Kneron part number	
Main board dimension	**100(L) x 60(W) x 1.6(H) mm**
Working voltage	**5V**
DDR memory size	**1Gb**
SPI NOR Flash size	**1Gb**
Switch & button	**Reset button x 1 , Wakeup button x1 , Boot Switch x1**
Interface - Power	**DC Jack (5V) x 1**
Interface – Fixed I/O	**USB3.0 Cable x1**

2.2 Inside the box

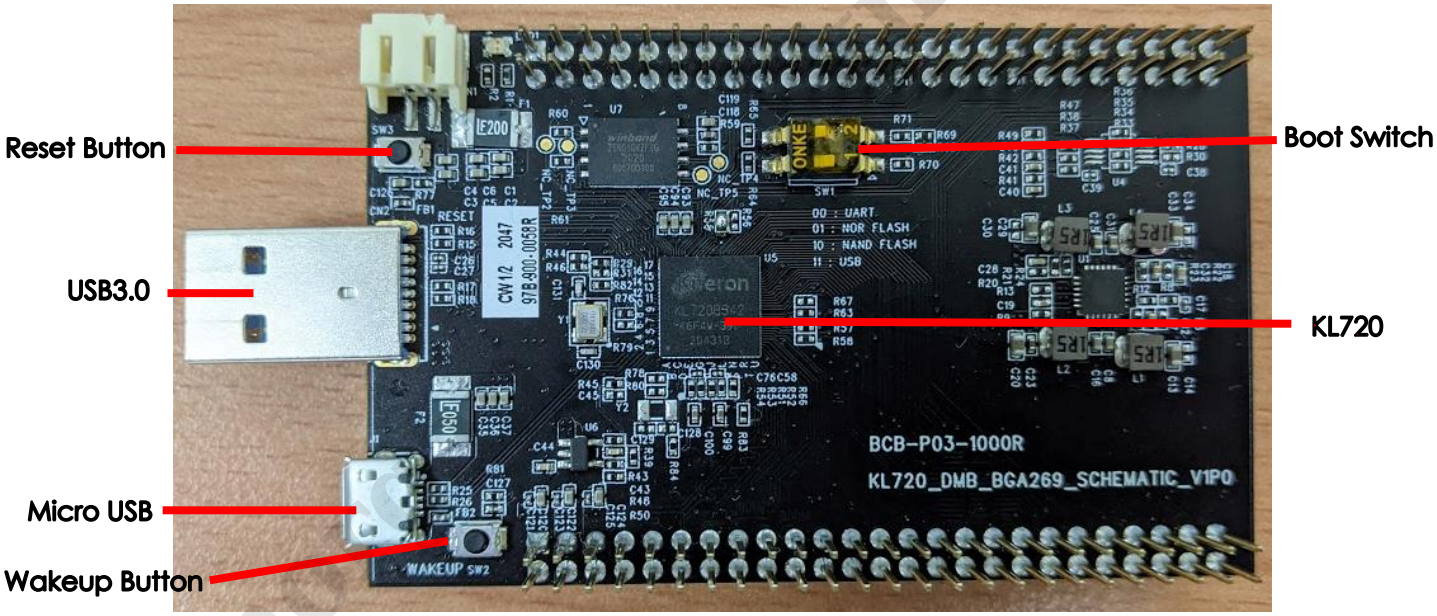
i. Main board x 1
ii. IO daughter board x 1
iii. USB3.0 Cable x 1

2.3 Assembly



2.4 Main board description

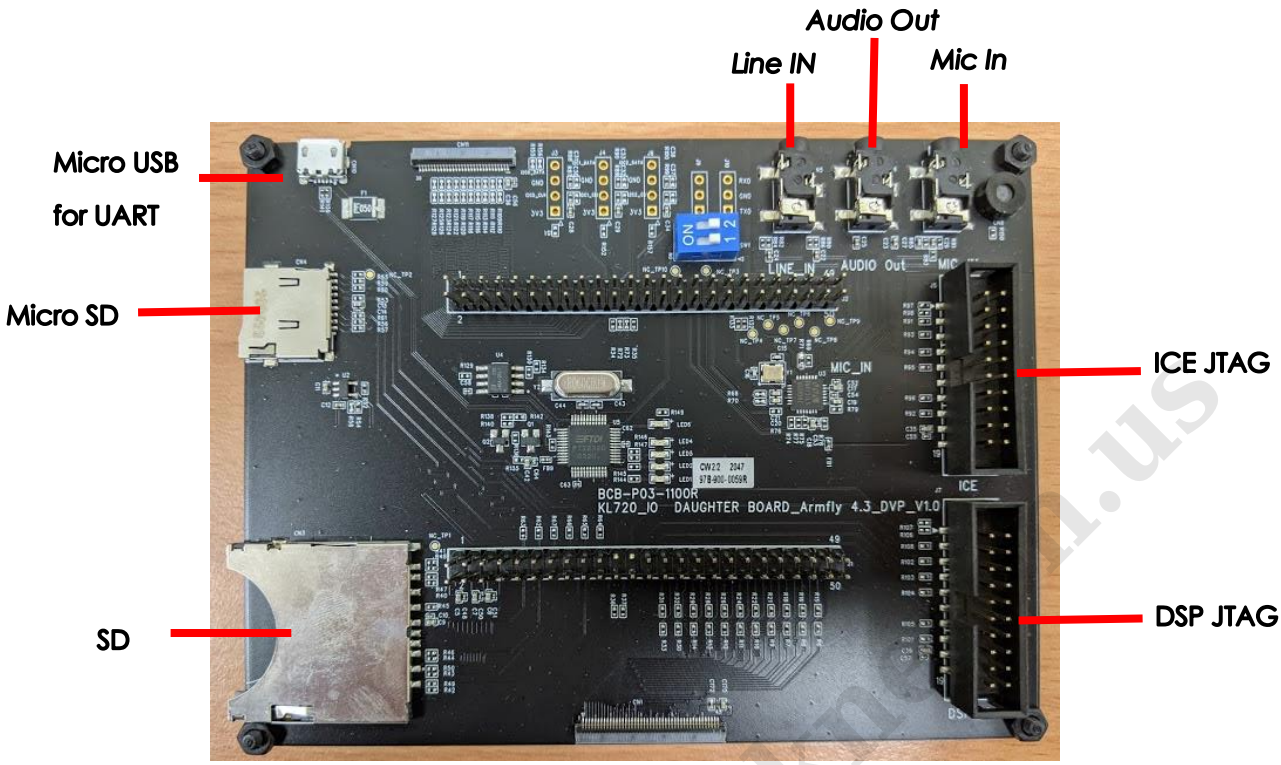
Here's the overview of all functions on the main board.



Here's the major component you must know before you start your design:

- KL720: AI SoC.
- DC Jack: 5V input for the demo board though 5V/4A adaptor.
- USB3.0: a connector that used USB3.0 connector for developing.
- USB2.0: a connector that used Micro USB connector for developing.
- Reset BTN: a button that used to reset the KL720.
- Wakeup BTN: a button that used to wake up KL720 from RTC mode.
- Boot Switch: Selection for boot from SPI / USB or UART.

Here's the overview of all functions on the IO board.



As you can see in the picture, here's the major component you must know before you start your design:

- Micro USB for UART: a connector that uses a Micro USB cable for developing.
- Micro / SD: a connector that use a SD Card or Micro SD Card
- JTAG: a connector that uses JTAG/ICE cable for developing.
- Audio: a 3.5" audio connector to input or output audio signal.

2.5 Pin mux

To make some flexibility for the developers. Some IOs also offers different functionality, users can simply choose different functions.

IO Port Name	PKG 9x9	PKG 11x11	IO Bank	Mode0	DIR	Mode1	DIR	Mode2	DIR	Mode3	DIR
X_DPI_PCLKI		V	Bank0 by ExtReg	DPI_PCLKI	I	DPI_PCLKI	I	DPI_PCLKI	I	DPI_PCLKI	I
X_DPI_VSI		V		DPI_VSI	I	DPI_VSI	I	DPI_VSI	I	DPI_VSI	I
X_DPI_HSI		V		DPI_HSI	I	DPI_HSI	I	DPI_HSI	I	DPI_HSI	I
X_DPI_DEI		V		DPI_DEI	I	DPI_DEI	I	DPI_DEI	I	DPI_DEI	I
X_DPI_DATAI[0]		V		DPI_DATAI[0]	I	DPI_DATAI[0]	I	DPI_DATAI[0]	I	DPI_DATAI[0]	I
X_DPI_DATAI[1]		V		DPI_DATAI[1]	I	DPI_DATAI[1]	I	DPI_DATAI[1]	I	DPI_DATAI[1]	I
X_DPI_DATAI[2]		V		DPI_DATAI[2]	I	DPI_DATAI[2]	I	DPI_DATAI[2]	I	DPI_DATAI[2]	I
X_DPI_DATAI[3]		V		DPI_DATAI[3]	I	DPI_DATAI[3]	I	DPI_DATAI[3]	I	DPI_DATAI[3]	I
X_DPI_DATAI[4]		V		DPI_DATAI[4]	I	DPI_DATAI[4]	I	DPI_DATAI[4]	I	DPI_DATAI[4]	I
X_DPI_DATAI[5]		V		DPI_DATAI[5]	I	DPI_DATAI[5]	I	DPI_DATAI[5]	I	DPI_DATAI[5]	I
X_DPI_DATAI[6]		V		DPI_DATAI[6]	I	DPI_DATAI[6]	I	DPI_DATAI[6]	I	DPI_DATAI[6]	I
X_DPI_DATAI[7]		V		DPI_DATAI[7]	I	DPI_DATAI[7]	I	DPI_DATAI[7]	I	DPI_DATAI[7]	I
X_DPI_DATAI[8]		V		DPI_DATAI[8]	I	DPI_DATAI[8]	I	DPI_DATAI[8]	I	DPI_DATAI[8]	I
X_DPI_DATAI[9]		V		DPI_DATAI[9]	I	DPI_DATAI[9]	I	DPI_DATAI[9]	I	DPI_DATAI[9]	I
X_DPI_DATAI[10]		V		DPI_DATAI[10]	I	DPI_DATAI[10]	I	DPI_DATAI[10]	I	DPI_DATAI[10]	I
X_DPI_DATAI[11]		V		DPI_DATAI[11]	I	DPI_DATAI[11]	I	DPI_DATAI[11]	I	DPI_DATAI[11]	I
X_DPI_DATAI[12]		V		DPI_DATAI[12]	I	DPI_DATAI[12]	I	DPI_DATAI[12]	I	DPI_DATAI[12]	I
X_DPI_DATAI[13]		V		DPI_DATAI[13]	I	DPI_DATAI[13]	I	DPI_DATAI[13]	I	DPI_DATAI[13]	I
X_DPI_DATAI[14]		V		DPI_DATAI[14]	I	DPI_DATAI[14]	I	DPI_DATAI[14]	I	DPI_DATAI[14]	I
X_DPI_DATAI[15]		V		DPI_DATAI[15]	I	DPI_DATAI[15]	I	DPI_DATAI[15]	I	DPI_DATAI[15]	I
X_SPI_CS_N	V	V	Bank1 by IO	SPI_CS_N	O	SPI_CS_N	O	SPI_CS_N	O	SPI_CS_N	O
X_SPI_CLK	V	V		SPI_CLK	O	SPI_CLK	O	SPI_CLK	O	SPI_CLK	O
X_SPI_DO	V	V		SPI_DO	O	SPI_DO	O	SPI_DO	O	SPI_DO	O
X_SPI_DI	V	V		SPI_DI	I	SPI_DI	I	SPI_DI	I	SPI_DI	I
X_SPI_WP_N	V	V		SPI_WP_N	O	SPI_WP_N	O	SPI_WP_N	O	SPI_WP_N	O
X_SPI_HOLD_N	V	V		SPI_HOLD_N	O	SPI_HOLD_N	O	SPI_HOLD_N	O	SPI_HOLD_N	O
X_I2C0_CLK	V	V		I2C0_CLK	I/O	I2C0_CLK	I/O	I2C0_CLK	I/O	1'b0	I
X_I2C0_DATA	V	V		I2C0_DATA	I/O	I2C0_DATA	I/O	I2C0_DATA	I/O	1'b0	I
X_MCLK	V	V		MCLK	O	MCLK	O	MCLK	O	MCLK	O
X_SSP0_CLK	V	V		SSP0_CLK	I/O	SSP0_CLK	I/O	SSP0_CLK	I/O	SSP0_CLK	I/O

X_SSP0_CS0	V	V		SSP0_CS0	I/O	SSP0_CS0	I/O	SSP0_CS0	I/O	SSP0_CS0	I/O
X_SSP0_CS1		V		SSP0_CS1	I/O	SSP0_CS1	I	SSP0_CS1	I	SSP0_CS1	I
IO Port Name	**PKG 9x9**	**PKG 11x11**	**IO Bank**	**Mode0**	**DIR**	**Mode1**	**DIR**	**Mode2**	**DIR**	**Mode3**	**DIR**
X_SSP0_DI	V	V		SSP0_DI	I	SSP0_DI	I	SSP0_DI	I	SSP0_DI	I
X_SSP0_DO	V	V		SSP0_DO	O	SSP0_DO	O	SSP0_DO	O	SSP0_DO	O
X_UART0_TX	V	V		UART0_TX	O	UART1_TX	O	UART1_TX	O	UART1_TX	O
X_UART0_RX	V	V		UART0_RX	I	UART1_RX	I	UART1_RX	I	1'b0	I
X_TRACE_CLK		V		Reserve	O	UART1_DCD	I	UART1_DCD	I	1'b0	I
X_TRACE_DATA[0]		V		Reserve	O	UART1_DTR	O	UART1_DTR	O	1'b0	I
X_TRACE_DATA[1]		V		Reserve	O	UART1_DSR	I	UART1_DSR	I	1'b0	I
X_TRACE_DATA[2]		V		Reserve	O	UART1_RTS	O	UART1_RTS	O	1'b0	I
X_TRACE_DATA[3]		V		Reserve	O	UART1_CTS	I	UART1_CTS	I	UART1_CTS	I
X_UART1_RI		V		UART1_RI	I	UART1_RI	I	UART1_RI	I	UART1_RI	I
X_I2C1_CLK	V	V	Bank3 by ExtReg	I2C1_CLK	I/O	I2C1_CLK	I/O	I2C1_CLK	I/O	1'b0	I
X_I2C1_DATA	V	V		I2C1_DATA	I/O	I2C1_DATA	I/O	I2C1_DATA	I/O	1'b0	I
X_SSP1_CLK	V	V		SSP1_CLK	I/O	DPI_DATAO[13]	O	SSP1_CLK	I/O	SSP1_CLK	I/O
X_SSP1_CS	V	V		SSP1_CS	I/O	DPI_DATAO[14]	O	SSP1_CS	I/O	SSP1_CS	I/O
X_SSP1_DI	V	V		SSP1_DI	I	DPI_DATAO[15]	O	SSP1_DI	I	SSP1_DI	I
X_SSP1_DO	V	V		SSP1_DO	O	DPI_DATAO[16]	O	SSP1_DO	O	SSP1_DO	O
X_SSP1_DCX	V	V		SSP1_DCX	O	DPI_DATAO[17]	O	SSP1_DCX	O	SSP1_DCX	O
X_PWM1	V	V		PWM1	O	PWM1	O	DSP_JTAG_TDO	O	DPI_DATAO[12]	I
X_DPI_PCLKO	V	V		DPI_PCLKO	O	DPI_PCLKO	O	DPI_PCLKO	O	DPI_PCLKO	O
X_DPI_VSO	V	V		DPI_VSO	O	DPI_VSO	O	DPI_VSO	O	DPI_VSO	O
X_DPI_HSO	V	V		DPI_HSO	O	DPI_HSO	O	DPI_HSO	O	DPI_HSO	O
X_DPI_DEO	V	V		DPI_DEO	O	DPI_DEO	O	DPI_DEO	O	DPI_DEO	O
X_DPI_DATAO[0]	V	V		DPI_DATAO[0]	O	DSP_JTAG_TRST_N	I	DPI_DATAO[0]	O	DPI_DATAO[0]	O
X_DPI_DATAO[1]	V	V		DPI_DATAO[1]	O	DSP_JTAG_TDI	I	DPI_DATAO[1]	O	DPI_DATAO[1]	O
X_DPI_DATAO[2]	V	V		DPI_DATAO[2]	O	DSP_JTAG_TMS	I	DPI_DATAO[2]	O	DPI_DATAO[2]	O
X_DPI_DATAO[3]	V	V		DPI_DATAO[3]	O	DSP_JTAG_TCK	I	DPI_DATAO[3]	O	DPI_DATAO[3]	O
X_DPI_DATAO[4]	V	V		DPI_DATAO[4]	O	UART1_TX	O	DPI_DATAO[4]	O	DPI_DATAO[4]	O
X_DPI_DATAO[5]	V	V		DPI_DATAO[5]	O	UART1_RX	I	DPI_DATAO[5]	O	DPI_DATAO[5]	O
X_DPI_DATAO[6]	V	V		DPI_DATAO[6]	O	DPI_DATAO[6]	O	DPI_DATAO[6]	O	DPI_DATAO[6]	O
X_DPI_DATAO[7]	V	V		DPI_DATAO[7]	O	DPI_DATAO[7]	O	DPI_DATAO[7]	O	DPI_DATAO[7]	O
X_DPI_DATAO[8]	V	V		DPI_DATAO[8]	O	DPI_DATAO[8]	O	DPI_DATAO[8]	O	DPI_DATAO[8]	O

X_DPI_DATAO[9]	V	V		DPI_DATAO[9]	O	DPI_DATAO[9]	O	DPI_DATAO[9]	O	DPI_DATAO[9]	O
X_DPI_DATAO[10]	V	V		DPI_DATAO[10]	O	DPI_DATAO[10]	O	DPI_DATAO[10]	O	DPI_DATAO[10]	O
IO Port Name	**PKG 9x9**	**PKG 11x11**	**IO Bank**	**Mode0**	**DIR**	**Mode1**	**DIR**	**Mode2**	**DIR**	**Mode3**	**DIR**
X_DPI_DATAO[11]	V	V		DPI_DATAO[11]	O	DPI_DATAO[11]	O	DPI_DATAO[11]	O	DPI_DATAO[11]	O
X_I2C2_CLK		V	Bank2 by IO	I2C2_CLK	I/O	I2C2_CLK	I/O	I2C2_CLK	I/O	1'b0	I
X_I2C2_DATA		V		I2C2_DATA	I/O	I2C2_DATA	I/O	I2C2_DATA	I/O	1'b0	I
X_DSP_TRSTN	V	V		DSP_JTAG_TRST_N	I	UART0_TX	O	UART0_TX	O	1'b0	I
X_DSP_TDI	V	V		DSP_JTAG_TDI	I	UART0_RX	I	UART0_RX	I	1'b0	I
X_DSP_TDO		V		DSP_JTAG_TDO	O	UART0_IRDA_RX_H	I	UART0_IRDA_RX_H	I	1'b0	I
X_DSP_TMS		V		DSP_JTAG_TMS	I	UART0_IRDA_RX_L	I	UART0_IRDA_RX_L	I	1'b0	I
X_DSP_TCK		V		DSP_JTAG_TCK	I	UART0_IRDA_TX	O	UART0_IRDA_TX	O	MCU_JTAG_TDO	O
X_PWM0	V	V		PWM0	O	PWM0	O	PWM0	O	1'b0	I
X_JTAG_TRSTN	V	V	Bank4 (3.3V)	MCU_JTAG_TRST_N	I	HSPI_CLK	I	HSPI_CLK	I	1'b0	I
X_JTAG_TDI	V	V		MCU_JTAG_TDI	I	HSPI_CS	I	HSPI_CS	I	1'b0	I
X_JTAG_TMS	V	V		MCU_JTAG_TMS	I	HSPI_DI	I	HSPI_DI	I	1'b0	I
X_JTAG_TCK	V	V		MCU_JTAG_TCK	I	HSPI_DO	O	HSPI_DO	O	1'b0	I
X_SD1_D3	V	V		SD1_D3	I/O	SD1_D3	I/O	SD1_D3	I/O	SD1_D3	I/O
X_SD1_D2	V	V		SD1_D2	I/O	SD1_D2	I/O	SD1_D2	I/O	SD1_D2	I/O
X_SD1_D1	V	V		SD1_D1	I/O	SD1_D1	I/O	SD1_D1	I/O	SD1_D1	I/O
X_SD1_D0	V	V		SD1_D0	I/O	SD1_D0	I/O	SD1_D0	I/O	SD1_D0	I/O
X_SD1_CMD	V	V		SD1_CMD	I/O	SD1_CMD	I/O	SD1_CMD	I/O	SD1_CMD	I/O
X_SD1_CLK	V	V		SD1_CLK	O	SD1_CLK	O	SD1_CLK	O	SD1_CLK	O
X_SD0_D3	V	V		SD0_D3	I/O	SD0_D3	I/O	SD0_D3	I/O	SD0_D3	I/O
X_SD0_D2	V	V		SD0_D2	I/O	SD0_D2	I/O	SD0_D2	I/O	SD0_D2	I/O
X_SD0_D1	V	V		SD0_D1	I/O	SD0_D1	I/O	SD0_D1	I/O	SD0_D1	I/O
X_SD0_D0	V	V		SD0_D0	I/O	SD0_D0	I/O	SD0_D0	I/O	SD0_D0	I/O
X_SD0_CMD	V	V		SD0_CMD	I/O	SD0_CMD	I/O	SD0_CMD	I/O	SD0_CMD	I/O
X_SD0_CLK	V	V		SD0_CLK	O	SD0_CLK	O	SD0_CLK	O	SD0_CLK	O
X_SD0_CARD_PWN	V	V		SD0_CARD_PWREN	O	SD0_CARD_PWREN	O	SD0_CARD_PWREN	O	SD0_CARD_PWREN	O
X_SD0_CARD_DET	V	V		SD0_CARD_DET	I	SD0_CARD_DET	I	SD0_CARD_DET	I	SD0_CARD_DET	I
X_JTAG_TDO	V	V		MCU_JTAG_TDO	O	SD0_W_PORT	I	SD0_W_PORT	I	SD0_W_PORT	I

Pin mux table 1/2

IO Port Name	**PKG 9x9**	**PKG 11x11**	**IO Bank**	**Mode4**	**DIR**	**Mode5**	**DIR**	**Mode6**	**DIR**	**Mode7**	**DIR**

X_DPI_PCLKI		V	Bank0 by ExtReg	DPI_PCLKI	I	DPI_PCLKI	I	DPI_PCLKI	I	DPI_PCLKI	I
X_DPI_VSI		V		DPI_VSI	I	DPI_VSI	I	DPI_VSI	I	DPI_VSI	I
X_DPI_HSI		V		DPI_HSI	I	DPI_HSI	I	DPI_HSI	I	DPI_HSI	I
X_DPI_DEI		V		DPI_DEI	I	DPI_DEI	I	DPI_DEI	I	DPI_DEI	I
X_DPI_DATAI[0]		V		DPI_DATAI[0]	I	DPI_DATAI[0]	I	DPI_DATAI[0]	I	DPI_DATAI[0]	I
X_DPI_DATAI[1]		V		DPI_DATAI[1]	I	DPI_DATAI[1]	I	DPI_DATAI[1]	I	DPI_DATAI[1]	I
X_DPI_DATAI[2]		V		DPI_DATAI[2]	I	DPI_DATAI[2]	I	DPI_DATAI[2]	I	DPI_DATAI[2]	I
X_DPI_DATAI[3]		V		DPI_DATAI[3]	I	DPI_DATAI[3]	I	DPI_DATAI[3]	I	DPI_DATAI[3]	I
X_DPI_DATAI[4]		V		DPI_DATAI[4]	I	DPI_DATAI[4]	I	DPI_DATAI[4]	I	DPI_DATAI[4]	I
X_DPI_DATAI[5]		V		DPI_DATAI[5]	I	DPI_DATAI[5]	I	DPI_DATAI[5]	I	DPI_DATAI[5]	I
X_DPI_DATAI[6]		V		DPI_DATAI[6]	I	DPI_DATAI[6]	I	DPI_DATAI[6]	I	DPI_DATAI[6]	I
X_DPI_DATAI[7]		V		DPI_DATAI[7]	I	DPI_DATAI[7]	I	DPI_DATAI[7]	I	DPI_DATAI[7]	I
X_DPI_DATAI[8]		V		DPI_DATAI[8]	I	DPI_DATAI[8]	I	DPI_DATAI[8]	I	DPI_DATAI[8]	I
X_DPI_DATAI[9]		V		DPI_DATAI[9]	I	DPI_DATAI[9]	I	DPI_DATAI[9]	I	DPI_DATAI[9]	I
X_DPI_DATAI[10]		V		DPI_DATAI[10]	I	DPI_DATAI[10]	I	DPI_DATAI[10]	I	DPI_DATAI[10]	I
X_DPI_DATAI[11]		V		DPI_DATAI[11]	I	DPI_DATAI[11]	I	DPI_DATAI[11]	I	DPI_DATAI[11]	I
X_DPI_DATAI[12]		V		DPI_DATAI[12]	I	DPI_DATAI[12]	I	DPI_DATAI[12]	I	DPI_DATAI[12]	I
X_DPI_DATAI[13]		V		DPI_DATAI[13]	I	DPI_DATAI[13]	I	DPI_DATAI[13]	I	DPI_DATAI[13]	I
X_DPI_DATAI[14]		V		DPI_DATAI[14]	I	DPI_DATAI[14]	I	DPI_DATAI[14]	I	DPI_DATAI[14]	I
X_DPI_DATAI[15]		V		DPI_DATAI[15]	I	DPI_DATAI[15]	I	DPI_DATAI[15]	I	DPI_DATAI[15]	I
X_SPI_CS_N	V	V	Bank1 by IO	SPI_CS_N	O	SPI_CS_N	O	SPI_CS_N	O	SPI_CS_N	O
X_SPI_CLK	V	V		SPI_CLK	O	SPI_CLK	O	SPI_CLK	O	SPI_CLK	O
X_SPI_DO	V	V		SPI_DO	O	SPI_DO	O	SPI_DO	O	SPI_DO	O
X_SPI_DI	V	V		SPI_DI	I	SPI_DI	I	SPI_DI	I	SPI_DI	I
X_SPI_WP_N	V	V		SPI_WP_N	O	SPI_WP_N	O	SPI_WP_N	O	SPI_WP_N	O
X_SPI_HOLD_N	V	V		SPI_HOLD_N	O	SPI_HOLD_N	O	SPI_HOLD_N	O	SPI_HOLD_N	O
X_I2C0_CLK	V	V		PWM0	O	I2C0_CLK	I/O	CORE_DBG_0	O	GPIO_0	I/O
X_I2C0_DATA	V	V		PWM1	O	I2C0_DATA	I/O	CORE_DBG_1	O	GPIO_1	I/O
X_MCLK	V	V		MCLK	O	MCLK	O	MCLK	O	MCLK	O
X_SSP0_CLK	V	V		SSP0_CLK	I/O	SSP0_CLK	I/O	SSP0_CLK	I/O	SSP0_CLK	I/O
X_SSP0_CS0	V	V		SSP0_CS0	I/O	SSP0_CS0	I/O	SSP0_CS0	I/O	SSP0_CS0	I/O
X_SSP0_CS1		V		SSP0_CS1	I	SSP0_CS1	I	SSP0_CS1	I	SSP0_CS1	I/O
IO Port Name	**PKG 9x9**	**PKG 11x11**	**IO Bank**	**Mode4**	**DIR**	**Mode5**	**DIR**	**Mode6**	**DIR**	**Mode7**	**DIR**
X_SSP0_DI	V	V		SSP0_DI	I	SSP0_DI	I	SSP0_DI	I	SSP0_DI	I

X_SSP0_DO	V	V		SSP0_DO	O	SSP0_DO	O	SSP0_DO	O	SSP0_DO	O
X_UART0_TX	V	V		UART1_TX	O	UART1_TX	O	CORE_DBG_15	O	GPIO_15	I/O
X_UART0_RX	V	V		UART1_RX	I	UART1_RX	I	CORE_DBG_16	O	GPIO_16	I/O
X_TRACE_CLK		V		UART1_DCD	I	UART1_DCD	I	CORE_DBG_17	O	GPIO_17	I/O
X_TRACE_DATA[0]		V		UART1_DTR	O	UART1_DTR	O	CORE_DBG_18	O	GPIO_18	I/O
X_TRACE_DATA[1]		V		UART1_DSR	I	UART1_DSR	I	CORE_DBG_19	O	GPIO_19	I/O
X_TRACE_DATA[2]		V		UART1_RTS	O	UART1_RTS	O	CORE_DBG_20	O	GPIO_20	I/O
X_TRACE_DATA[3]		V		UART1_CTS	I	UART1_CTS	I	CORE_DBG_21	O	GPIO_21	I/O
X_UART1_RI		V		UART1_RI	I	UART1_RI	I	CORE_DBG_22	O	GPIO_22	I/O
X_I2C1_CLK	V	V	Bank3 by ExtReg	UART0_TX	O	MCU_JTAG_TRST_N	I	CORE_DBG_2	O	GPIO_2	I/O
X_I2C1_DATA	V	V		UART0_RX	I	MCU_JTAG_TDI	I	CORE_DBG_3	O	GPIO_3	I/O
X_SSP1_CLK	V	V		SSP1_CLK	I/O	SSP1_CLK	O	SSP1_CLK	I/O	SSP1_CLK	I/O
X_SSP1_CS	V	V		SSP1_CS	I/O	SSP1_CS	O	SSP1_CS	I/O	SSP1_CS	I/O
X_SSP1_DI	V	V		SSP1_DI	I	SSP1_DI	O	SSP1_DI	I	SSP1_DI	I
X_SSP1_DO	V	V		SSP1_DO	O	SSP1_DO	O	SSP1_DO	O	SSP1_DO	O
X_SSP1_DCX	V	V		SSP1_DCX	O	SSP1_DCX	O	SSP1_DCX	O	SSP1_DCX	O
X_PWM1	V	V		I2C0_DATA	I/O	PWM1	O	CORE_DBG_27	O	GPIO_27	I/O
X_DPI_PCLKO	V	V		DPI_PCLKO	O	DPI_PCLKO	O	DPI_PCLKO	O	DPI_PCLKO	O
X_DPI_VSO	V	V		DPI_VSO	O	DPI_VSO	O	DPI_VSO	O	DPI_VSO	O
X_DPI_HSO	V	V		DPI_HSO	O	DPI_HSO	O	DPI_HSO	O	DPI_HSO	O
X_DPI_DEO	V	V		DPI_DEO	O	DPI_DEO	O	DPI_DEO	O	DPI_DEO	O
X_DPI_DATAO[0]	V	V		DPI_DATAO[0]	O	DPI_DATAO[0]	O	DPI_DATAO[0]	O	DPI_DATAO[0]	O
X_DPI_DATAO[1]	V	V		DPI_DATAO[1]	O	DPI_DATAO[1]	O	DPI_DATAO[1]	O	DPI_DATAO[1]	O
X_DPI_DATAO[2]	V	V		DPI_DATAO[2]	O	DPI_DATAO[2]	O	DPI_DATAO[2]	O	DPI_DATAO[2]	O
X_DPI_DATAO[3]	V	V		DPI_DATAO[3]	O	DPI_DATAO[3]	O	DPI_DATAO[3]	O	DPI_DATAO[3]	O
X_DPI_DATAO[4]	V	V		DPI_DATAO[4]	O	DPI_DATAO[4]	O	DPI_DATAO[4]	O	DPI_DATAO[4]	O
X_DPI_DATAO[5]	V	V		DPI_DATAO[5]	O	DPI_DATAO[5]	O	DPI_DATAO[5]	O	DPI_DATAO[5]	O
X_DPI_DATAO[6]	V	V		DPI_DATAO[6]	O	DPI_DATAO[6]	O	DPI_DATAO[6]	O	DPI_DATAO[6]	O
X_DPI_DATAO[7]	V	V		DPI_DATAO[7]	O	DPI_DATAO[7]	O	DPI_DATAO[7]	O	DPI_DATAO[7]	O
X_DPI_DATAO[8]	V	V		DPI_DATAO[8]	O	DPI_DATAO[8]	O	CORE_DBG_28	O	GPIO_28	I/O
X_DPI_DATAO[9]	V	V		DPI_DATAO[9]	O	DPI_DATAO[9]	O	CORE_DBG_29	O	GPIO_29	I/O
X_DPI_DATAO[10]	V	V		DPI_DATAO[10]	O	DPI_DATAO[10]	O	CORE_DBG_30	O	GPIO_30	I/O
IO Port Name	**PKG 9x9**	**PKG 11x11**	**IO Bank**	**Mode4**	**DIR**	**Mode5**	**DIR**	**Mode6**	**DIR**	**Mode7**	**DIR**
X_DPI_DATAO[11]	V	V		DPI_DATAO[11]	O	DPI_DATAO[11]	O	CORE_DBG_31	O	GPIO_31	I/O

X_I2C2_CLK		V	Bank2 by IO	Reserve	I	MCU_JTAG_TMS	I	CORE_DBG_4	O	GPIO_4	I/O
X_I2C2_DATA		V		Reserve	I	MCU_JTAG_TCK	I	CORE_DBG_5	O	GPIO_5	I/O
X_DSP_TRSTN	V	V		I2C1_CLK	I/O	Reserve	O	CORE_DBG_10	O	GPIO_10	I/O
X_DSP_TDI	V	V		I2C1_DATA	I/O	Reserve	O	CORE_DBG_11	O	GPIO_11	I/O
X_DSP_TDO		V		I2C2_CLK	I/O	Reserve	O	CORE_DBG_12	O	GPIO_12	I/O
X_DSP_TMS		V		I2C2_DATA	I/O	Reserve	O	CORE_DBG_13	O	GPIO_13	I/O
X_DSP_TCK		V		Reserve	O	Reserve	O	CORE_DBG_14	O	GPIO_14	I/O
X_PWM0	V	V		I2C0_CLK	I/O	PWM0	O	CORE_DBG_26	O	GPIO_26	I/O
X_JTAG_TRSTN	V	V	Bank4 (3.3V)	SSP0_CS0	I/O	HSPI_CLK	I	CORE_DBG_6	O	GPIO_6	I/O
X_JTAG_TDI	V	V		SSP0_CS1	I	HSPI_CS	I	CORE_DBG_7	O	GPIO_7	I/O
X_JTAG_TMS	V	V		SSP0_DI	I	HSPI_DI	I	CORE_DBG_8	O	GPIO_8	I/O
X_JTAG_TCK	V	V		SSP0_DO	O	HSPI_DO	O	CORE_DBG_9	O	GPIO_9	I/O
X_SD1_D3	V	V		SD1_D3	I/O	SD1_D3	I/O	SD1_D3	I/O	SD1_D3	I/O
X_SD1_D2	V	V		SD1_D2	I/O	SD1_D2	I/O	SD1_D2	I/O	SD1_D2	I/O
X_SD1_D1	V	V		SD1_D1	I/O	SD1_D1	I/O	SD1_D1	I/O	SD1_D1	I/O
X_SD1_D0	V	V		SD1_D0	I/O	SD1_D0	I/O	SD1_D0	I/O	SD1_D0	I/O
X_SD1_CMD	V	V		SD1_CMD	I/O	SD1_CMD	I/O	SD1_CMD	I/O	SD1_CMD	I/O
X_SD1_CLK	V	V		SD1_CLK	O	SD1_CLK	O	SD1_CLK	O	SD1_CLK	O
X_SD0_D3	V	V		SD0_D3	I/O	SD0_D3	I/O	SD0_D3	I/O	SD0_D3	I/O
X_SD0_D2	V	V		SD0_D2	I/O	SD0_D2	I/O	SD0_D2	I/O	SD0_D2	I/O
X_SD0_D1	V	V		SD0_D1	I/O	SD0_D1	I/O	SD0_D1	I/O	SD0_D1	I/O
X_SD0_D0	V	V		SD0_D0	I/O	SD0_D0	I/O	SD0_D0	I/O	SD0_D0	I/O
X_SD0_CMD	V	V		SD0_CMD	I/O	SD0_CMD	I/O	SD0_CMD	I/O	SD0_CMD	I/O
X_SD0_CLK	V	V		SD0_CLK	O	SD0_CLK	O	SD0_CLK	O	SD0_CLK	O
X_SD0_CARD_PWN	V	V		SD0_CARD_PWREN	O	SD0_CARD_PWREN	O	CORE_DBG_23	O	GPIO_23	I/O
X_SD0_CARD_DET	V	V		SD0_CARD_DET	I	SD0_CARD_DET	I	CORE_DBG_24	O	GPIO_24	I/O
X_JTAG_TDO	V	V		SD0_W_PORT	I	SD0_W_PORT	I	CORE_DBG_25	O	GPIO_25	I/O

Pin mux table 2/2

3. Peripherals

Here list the peripherals you need for the board development.

3.1 USB3.0 Cable

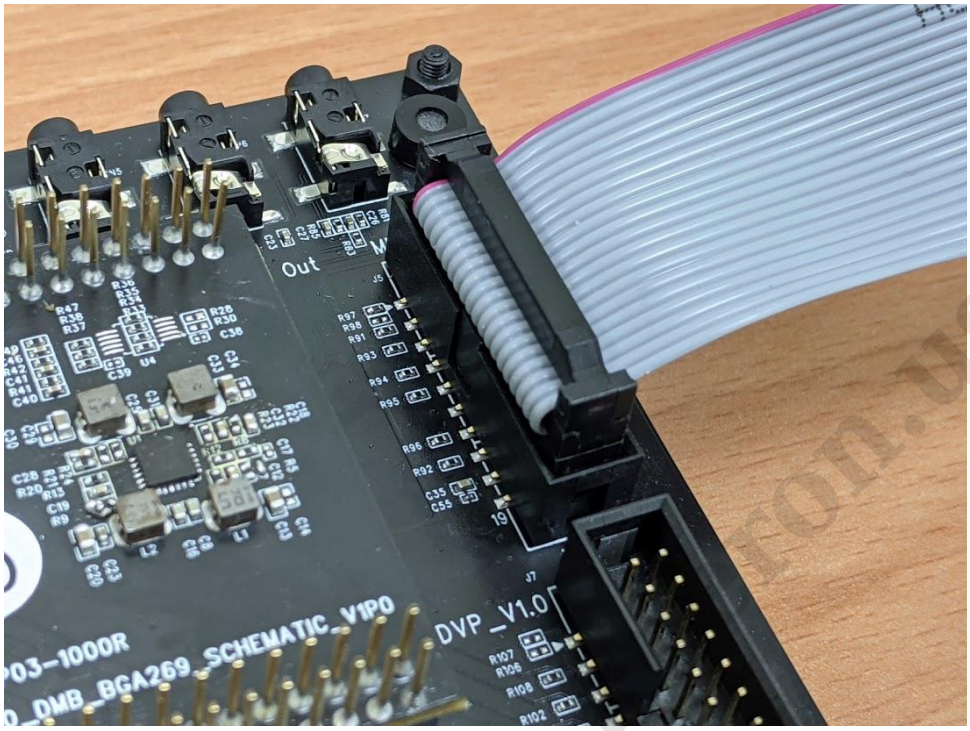
Figure, USB3.0 cable

3.2 JTAG cable (not included in Kneron shipping box)

Figure, JTAG cable

3.3 Connecting JTAG

Connecting JTAG cable like picture shown below:



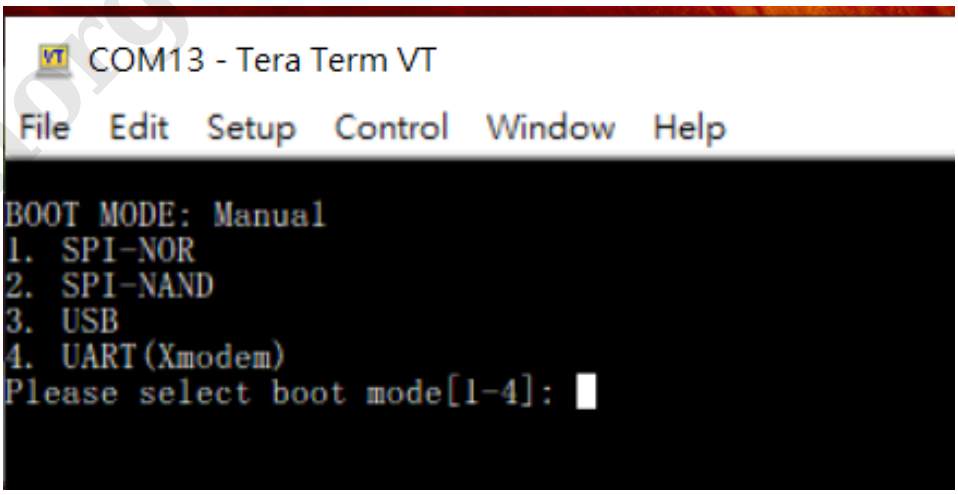
Figure, connecting JTAG cable

4. KL720 Power on and System

4.1 Bring Up procedure

Open UART COM port debug windows (Tera term or Putty) /UART Port and Baud rate: 115200

You will see boot message



Figure, boot message

4.2 Select Boot Switch

Use Boot Switch to selection for boot from SPI / USB or UART, and reference below to select.

Boot Mode	BOOT_SPL_SEL = {X_SSP1_DO, X_SSP0_DO}
UART	00
NOR FLASH	01
NAND FLASH	10
USB	11

Example: Boot from NAND FLASH, X_SSP1_DO pull high and X_SSP0_DO pull low.

4.3 Connecting JTAGs

Open KL720 Daisy-chain project.

On SCPU JLink Setting

Edit SCPU JTAG JLink Setting