KSZ8041NL

10Base-T/100Base-TX
Physical Layer Transceiver

Evaluation Board User's Guide

Revision 1.1 / May 2007

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Revision History

Revision	Date	Summary of Changes
1.0	4/3/07	Initial Release
1.1	5/24/07	Added 100pF capacitor (C53) to BOM.

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1.0 Introduction

The KSZ8041NL is a 10Base-T/100Base-TX Physical Layer Transceiver with MII and RMII MAC interfaces. It utilizes a unique mixed-signal design to extend signaling distance while reducing power consumption, and offers HP Auto MDI/MDI-X for reliable detection of and correction for crossover and straight-through cables, eliminating the need to differentiate between crossover and straight-through cables.

The KSZ8041NL comes in a 32-pin, lead-free MLF® (QFN per JDEC) package and provides an ideal solution for 10Base-T/100Base-TX applications that have tight PCB board space.

The KSZ8041NL Eval Board (KSZ8041NL-EVAL) provides a convenient platform to evaluate the KSZ8041NL features. All KSZ8041NL configuration pins are accessible either by jumpers, test points or interface connectors.

2.0 Board Features

- Micrel KSZ8041NL 10Base-T/100Base-TX Physical Layer Transceiver
- RJ-45 Jack for Fast Ethernet cable interface
- HP Auto-MDIX for automatic detection and correction for straight-through and crossover cables
- MII (Media Independent Interface) Connector to interface with a MAC controller
- RMII (Reduced MII) option using MII Connector
- 2 LED Indicators for status and activity
- Jumpers to configure strapping pins
- Manual Reset Button for quick reboot after re-configuration of strapping pins

3.0 Evaluation Kit Contents

The KSZ8041NL Evaluation Kit includes the following hardware:

- KSZ8041NL Evaluation Board

A design package with the following collaterals that can be downloaded from Micrel's website at http://www.micrel.com

- KSZ8041NL Eval Board Schematic (PDF and OrCAD DSN file)
- KSZ8041NL_TL-FTL Eval Boards Gerber Files (PDF version included)
- KSZ8041NL Eval Board User's Guide (this document)
- KSZ8041NL Recommended Land Pattern for PCB Layout
- KSZ8041NL IBIS Model

and the KSZ8041NL Datasheet which is also available from Micrel's website.

4.0 Hardware Description

The KSZ8041NL-EVAL (shown in Figure 1) comes in a compact form factor and plugs directly into industry standard test equipment such as Spirent SmartBits, or other boards with Ethernet MACs that expose the MII interface. Configuration of the KSZ8041NL is accomplished through on-board jumper selections and/or by PHY register access via the MDC/MDIO management pins of the MII Interface.

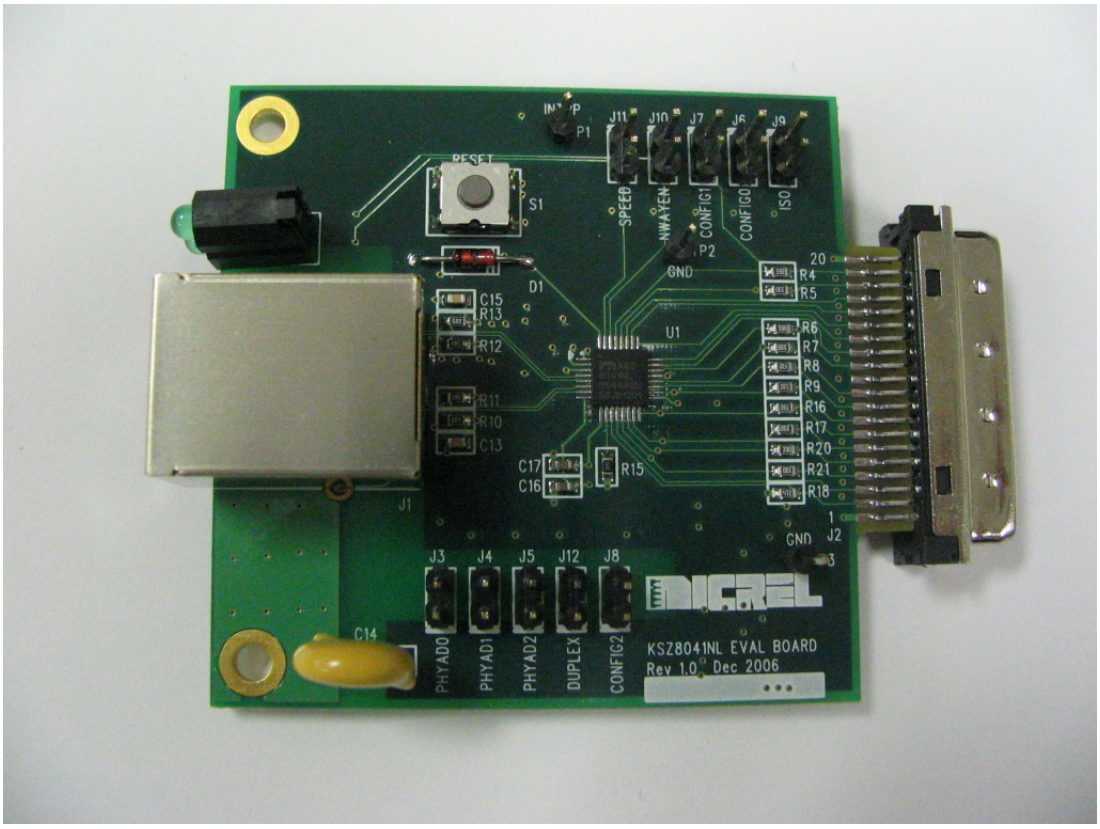

Figure 1. KSZ8041NL Evaluation Board

Other features include a RJ-45 Jack for Fast Ethernet cable connection, programmable LED indicators for reporting link status and activity, and a manual reset button for quick reboot after re-configuration of strapping pins.

The KSZ8041NL-EVAL receives +5V DC input power through its MII connector.

4.1 MII (Media Independent Interface)

The KSZ8041NL-EVAL receives power and accesses MII data and management information from the MII connector J2. Figure 2 shows the MII interface connection with Spirent SmartBits.

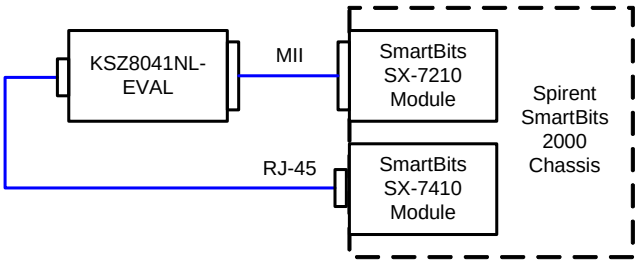

Figure 2. KSZ8041NL-EVAL MII Interface Connection with Spirent SmartBits

Connections with other boards that also expose the MII interface are possible. Figure 3 shows the KSZ8041NL-EVAL connected to the Micrel KSZ8893MQL Evaluation Board.

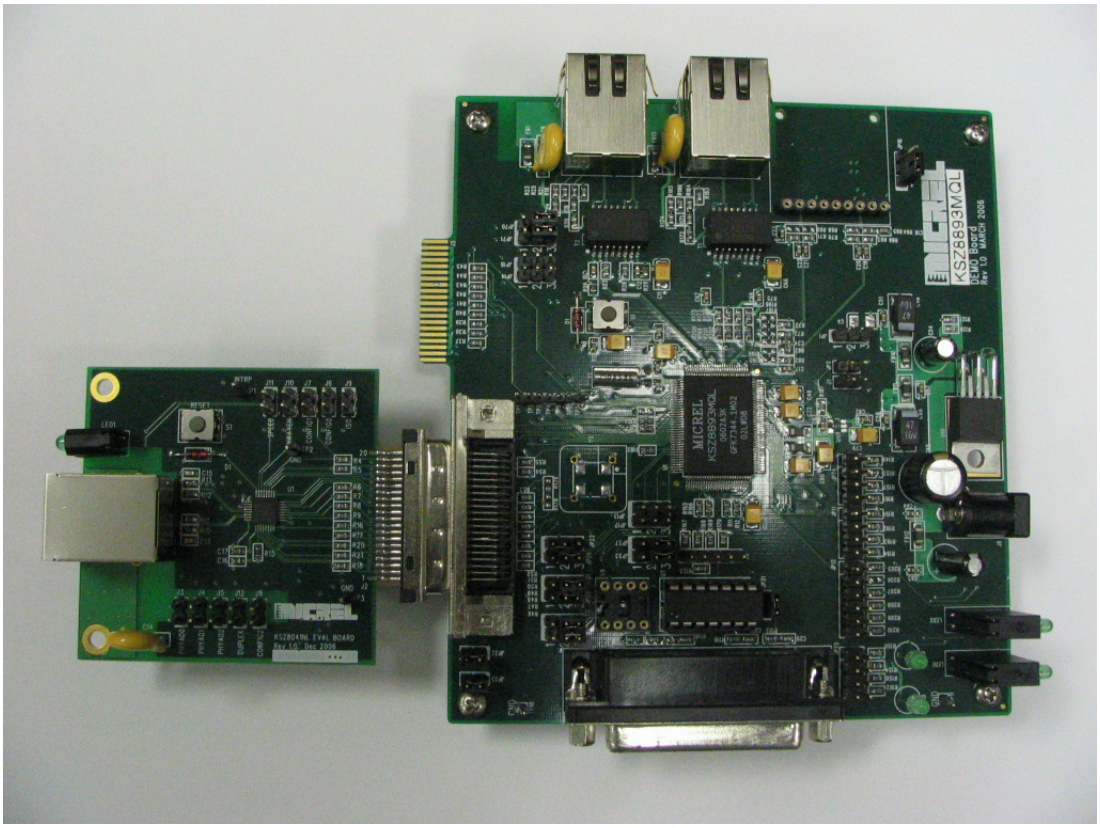

Figure 3. KSZ8041NL-EVAL interfacing with KSZ8893MQL Evaluation Board

The MII interface is defined by Clause 22 of the IEEE 802.3 Specification. MII Management (MIIM) is conducted thru pins MDC (clock line) and MDIO (data line). MIIM allows upper-layer devices to monitor and control the states of the KSZ8041NL. An external device with MDC/MDIO capability can be used to read the PHY status or configure the PHY registers. The MIIM frame format and timing information can be found in the KSZ8041NL Datasheet and in Clause 22 of the IEEE 802.3 Specification.

The KSZ8041NL-EVAL has a 40-pin male edge connector that interfaces with and plugs directly into the SmartBits SX-7210 Module or other Fast Ethernet MAC boards with the mating AMP 787170-4 (40-pin, right angle, female) connector. Table 1 lists the pin outs for the MII interface on connector J2.

Pin #	Signal	Pin #	Signal
1	+5V	21	+5V
2	MDIO	22	Ground
3	MDC	23	Ground
4	RXD3	24	Ground
5	RXD2	25	Ground
6	RXD1	26	Ground
7	RXD0	27	Ground
8	RXDV	28	Ground
9	RXCLK	29	Ground
10	RXER	30	Ground
11	TXER	31	Ground
12	TXCLK	32	Ground
13	TXEN	33	Ground
14	TXD0	34	Ground
15	TXD1	35	Ground
16	TXD2	36	Ground
17	TXD3	37	Ground
18	COL	38	Ground
19	CRS	39	Ground
20	+5V	40	+5V

Table 1. Connector J2 - MII Pin Definition

4.1.1 RMII (Reduced Media Independent Interface) Option

The KSZ8041NL-EVAL can use its 40-pin male edge connector (J2) with some minor board population changes to interface with RMII MACs. Like MII mode, the KSZ8041NL-EVAL receives power and accesses RMII data and management information via connector J2 in RMII mode.

Figure 3 shows the KSZ8041NL-EVAL interfacing with the KSZ8893MQL Evaluation Board in MII mode. Alternatively, both KSZ8041NL and KSZ8893MQL devices can be configured to RMII mode and interface with each other using the same J2 connector interface. For this setup, the

RMII 50MHz reference clock is sourced from the KSZ8893MQL Evaluation Board side. Refer to KSZ8893MQL Eval Board Schematic for additional population changes on the KSZ8893MQL side. For the KSZ8041NL-EVAL side, the board changes to support RMII mode are as follows:

1. Remove crystal circuit (Y1, C16, C17) and TXC clock termination (R6).
2. Populate R14 with 0 Ohm and R19 with 33 Ohm to connect RMII 50MHz reference clock (provided by MAC side via J2 pin 12) to U1 pin 9 (XI input).
3. Select RMII mode by setting strapping pins CONFIG[2:0] to '001'.

These board changes can also be found in the KSZ8041NL Eval Board Schematic.

Table 2 lists the pin outs for the RMII interface on connector J2.

Pin #	Signal	Pin #	Signal
1	+5V	21	+5V
2	MDIO	22	Ground
3	MDC	23	Ground
4	<not used>	24	Ground
5	<not used>	25	Ground
6	RXD[1]	26	Ground
7	RXD[0]	27	Ground
8	CRSDV	28	Ground
9	<not used>	29	Ground
10	RXER	30	Ground
11	<not used>	31	Ground
12	REF_CLK	32	Ground
13	TXEN	33	Ground
14	TXD0	34	Ground
15	TXD1	35	Ground
16	<not used>	36	Ground
17	<not used>	37	Ground
18	<not used>	38	Ground
19	<not used>	39	Ground
20	+5V	40	+5V

Table 2. Connector J2 - RMII Pin Definition

4.2 Jumper Setting & Definition

The KSZ8041NL-EVAL does not require any jumper for normal operation. At power-up, the KSZ8041NL is configured using the chip's internal pull-up and pull-down resistors with its default strapping pin values. Jumpers are provided to override the default settings, allowing for quick configuration and re-configuration of the board. To override the default settings, simply select and close the desired jumper setting(s) and toggle the on-board manual reset button (S1) for the new setting(s) to take effect.

The KSZ8041NL-EVAL jumper settings are defined in Table 3 below.

<table>
<tr><th>Jumper</th><th>Definition</th><th>Open (default)</th><th>Close</th></tr>
<tr><td>J3</td><td>PHYAD0</td><td>1</td><td>0</td></tr>
<tr><td>J4</td><td>PHYAD1</td><td>0</td><td>1</td></tr>
<tr><td>J5</td><td>PHYAD2</td><td>0</td><td>1</td></tr>
<tr><td>J6</td><td>CONFIG0</td><td colspan="2" rowspan="3"><table><tr><th>CONFIG[2:0]</th><th>Mode</th></tr><tr><td>[open, open, open]</td><td>MII (default)</td></tr><tr><td>[open, open, close]</td><td>RMII</td></tr><tr><td>[close, open, open]</td><td>PCS Loopback</td></tr></table>All other CONFIG[2:0] settings not listed are reserved (not used).</td></tr>
<tr><td>J7</td><td>CONFIG1</td></tr>
<tr><td>J8</td><td>CONFIG2</td></tr>
<tr><td>J9</td><td>Isolate Mode</td><td>Disable</td><td>Enable</td></tr>
<tr><td>J10</td><td>Auto-Negotiation</td><td>Enable</td><td>Disable</td></tr>
<tr><td>J11</td><td>Forced Speed</td><td>100Base-TX</td><td>10Base-T</td></tr>
<tr><td>J12</td><td>Forced Duplex</td><td>Half</td><td>Full</td></tr>
</table>

Table 3. KSZ8041NL-EVAL Jumper Definition

Table 4 lists the strapping pin definitions for the KSZ8041NL-EVAL jumpers.

<table>
<tr><th>Jumper</th><th>Pin</th><th>Pin Name</th><th>Pin Function</th></tr>
<tr><td>J5
J4
J3</td><td>15
14
13</td><td>PHYAD2
PHYAD1
PHYAD0</td><td>The PHY Address is latched at power-up / reset and is configurable to any value from 1 to 7.
The default PHY Address is 00001.
PHY Address bits [4:3] are always set to '00'.</td></tr>
<tr><td>J8
J7
J6</td><td>18
29
28</td><td>CONFIG2
CONFIG1
CONFIG0</td><td>The CONFIG[2:0] strap-in pins are latched at power-up / reset and are defined as follows:
<table><tr><th>CONFIG[2:0]</th><th>Mode</th></tr><tr><td>000</td><td>MII (default)</td></tr><tr><td>001</td><td>RMII</td></tr><tr><td>100</td><td>PCS Loopback</td></tr></table>All other CONFIG[2:0] settings not listed are reserved (not used).</td></tr>
<tr><td>J9</td><td>20</td><td>ISO</td><td>ISOLATE mode
Pull-up = Enable
Pull-down (default) = Disable
During power-up / reset, this pin value is latched into register 0h bit 10.</td></tr>
<tr><td>J11</td><td>31</td><td>SPEED</td><td>SPEED mode
Pull-up (default) = 100Mbps
Pull-down = 10Mbps
During power-up / reset, this pin value is latched into register 0h bit 13 as the Speed Select, and also is latched into register 4h (Auto-Negotiation Advertisement) as the Speed capability support.</td></tr>
<tr><td>J12</td><td>16</td><td>DUPLEX</td><td>DUPLEX mode
Pull-up (default) = Half Duplex
Pull-down = Full Duplex
During power-up / reset, this pin value is latched into register 0h bit 8 as the Duplex Mode.</td></tr>
<tr><td>J10</td><td>30</td><td>NWAYEN</td><td>Nway Auto-Negotiation Enable
Pull-up (default) = Enable Auto-Negotiation
Pull-down = Disable Auto-Negotiation
During power-up / reset, this pin value is latched into register 0h bit 12.</td></tr>
</table>

Table 4. Strapping Pin Definitions for KSZ8041NL-EVAL Jumpers

4.3 Test Point Definition

The KSZ8041NL-EVAL has three test points. They are defined in the following table.

Test Point	Definition
TP1	Interrupt Signal (pin 21) with external pull-up
TP2	Signal Ground
TP3	Signal Ground

Table 5. KSZ8041NL-EVAL Test Point Definition

4.4 RJ-45 Connector

The RJ-45 Connector (J1) is a TDK TLA-6T718 integrated magnetic jack. It connects to standard CAT-5 Ethernet cable to interface with 10Base-T/100Base-TX Ethernet devices.

J1 also supports Auto-MDIX and Auto-Negotiation / Forced Modes.

4.5 LED Indicators

A dual LED indicator (LED1) is located adjacent to the RJ-45 Connector. The top LED and bottom LED are connected to LED1 (pin 31) and LED0 (pin 30) of the KSZ8041NL, respectively.

The two LEDs are programmable to LED mode '00' or '01' via register 1Eh bits [15:14], and are defined in the following table.

<table>
<tr><th>LED Mode</th><th>LED1 (pin 31)</th><th>LED0 (pin 30)</th></tr>
<tr><td>00</td><td>
<table>
<tr><th>Speed</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>10BT</td><td>H</td><td>OFF</td></tr>
<tr><td>100BT</td><td>L</td><td>ON</td></tr>
</table>
</td><td>
<table>
<tr><th>Link/ Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Link</td><td>H</td><td>OFF</td></tr>
<tr><td>Link</td><td>L</td><td>ON</td></tr>
<tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr>
</table>
</td></tr>
<tr><td>01</td><td>
<table>
<tr><th>Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Activity</td><td>H</td><td>OFF</td></tr>
<tr><td>Activity</td><td>L</td><td>ON</td></tr>
</table>
</td><td>
<table>
<tr><th>Link</th><th>Pin State</th><th>Definition</th></tr>
<tr><td>No Link</td><td>H</td><td>OFF</td></tr>
<tr><td>Link</td><td>L</td><td>ON</td></tr>
</table>
</td></tr>
<tr><td>10</td><td>Reserved – not used</td><td>Reserved – not used</td></tr>
<tr><td>11</td><td>Reserved – not used</td><td>Reserved – not used</td></tr>
</table>

Table 6. KSZ8041NL-EVAL LED Definition