KSZ8342Q

Data Sheet

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1 General Description

The Micrel KSZ8342Q supplies a complete solution for converting analog signals from a traditional telephone of fax machine for transmission over IP. By incorporating an advanced DSP, the KSZ8342Q provides all logic necessary for performing analog to digital telephone. The KSZ8342Q device is available in a RoHS-compliant 128-lead QFP package.

The KSZ8342Q device leverages Micrel's core technology competencies including:

- IPv6
- Low Power
- Energy Efficient Ethernet (EEE)
- High degree of integration and compact design

Figure 1 shows a block diagram of the KSZ8342Q.

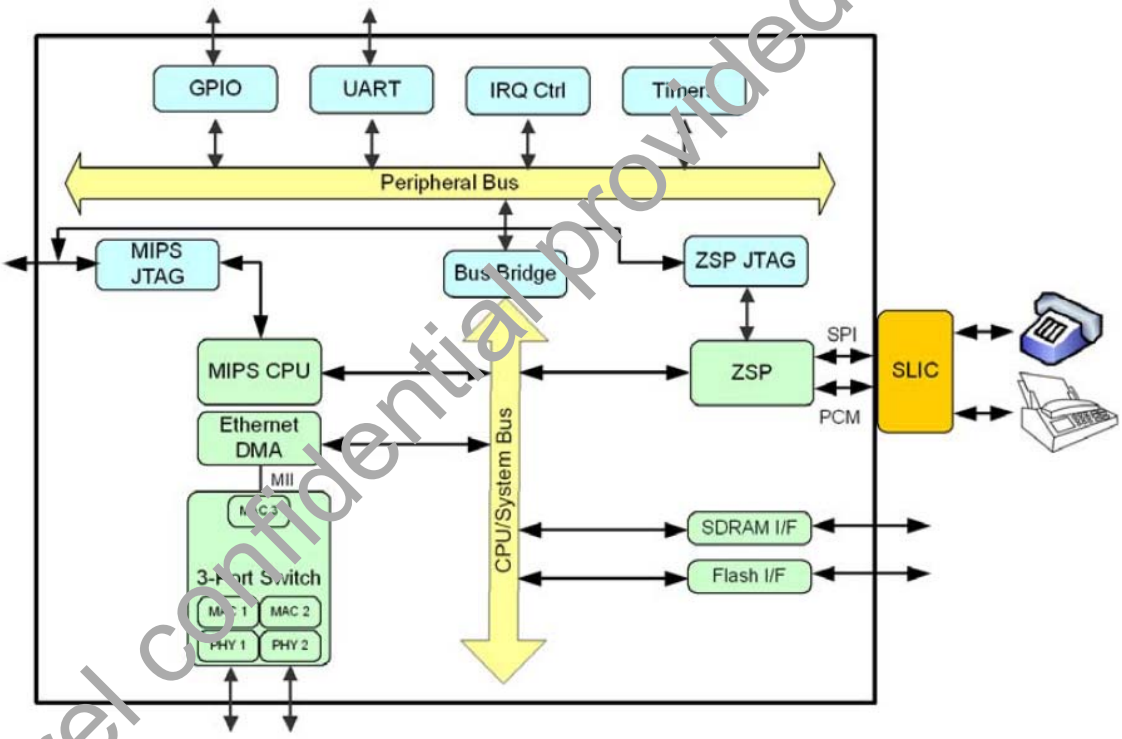


Figure 1. KSZ8342 Block Diagram

2 Features

Features of the KSZ8342 VoIP processor include:

MIPS™ Core Processor

The KSZ8342 integrates a MIPS32 M4KEc as the central processing unit for the VoIP SoC. This includes optimized MIPS32 M4KEc configuration options for VoIP including cache size, cache organization, CPU register size, and memory BIST.

ZSP400 Digital Signal Processor

Voice over IP applications require numerous speech codec technologies to convey voice signals over the TCP/IP networks. The major speech codecs implemented in the ZSP firmware include G.711 µ/A, G.722, G.722.1, G.722.2, G.723.1, G726, G.729A/B and G.167 Acoustic Echo Cancellation. The ZSP firmware is available in binary format.

Switch Engine

A 3-port switch engine contains a 10BASE-T/100BASE-TX MAC that supports full-duplex flow control and half-duplex back pressure collision flow control. The switch engine facilitates non-blocking packet switching at 1 Gbps, and programmable rate limiting from 0 - 100 Mbps on both input and output. The device contains broadcast storm protections and snooping support for Multicast packet filtering. Two ports are used to communicate with the external Ethernet interface. The third port is used for internal communication between the switch and the Ethernet DMA block as shown in Figure 1.

10/100 Mbps Ethernet PHY

The KSZ8342 contains two Ethernet PHY devices, one per port. Each 10/100 TX/RX PHY supports adaptive equalization and baseline wander correction. For maximum power savings, the PHY supports IEEE 802.3az MAC/PCS Energy Efficient Ethernet (EEE) functions. The PHY is IEEE 802.3az compliant and contains loopback functions, on-chip termination, an on-chip LDO and enhanced PLL for low EMI transmission. Note that the internal third communication port does not contain a PHY.

SDRAM Memory Support

The KSZ8342Q support SDR memory up to 64 MB. A 16-bit data width is implemented for the SDR.

UART and GPIO

The KSZ8342 contains a single industry-standard UART port. The KSZ8342Q 128-pin package contains 18 shared GPIO pins. There are no dedicated GPIO pins on the KSZ8342Q.

Interrupt Controller

An integrated central interrupt controller facilitates low-latency interrupt service.

Technology

The KSZ8342Q is fabricated using a 0.11 □m process with a 1.2V core voltage and a 3.3V I/O voltage. The KSZ8342Q is available in a 128-pin PQFP package.

Table 1 lists the external interface for both the KSZ8342Q VoIP devices.

Table 1. KSZ8342 External Interfaces

Interface	Usage
SDRAM Memory	Single data rate
Flash	4-bit wide serial NOR boot ROM
PCM	Analog telephone connections — data
SPI SLIC	Analog telephone connections — configuration and debug only
Ethernet Ports	Transmit/receive converted analog telephone signals — two ports
UART	Terminal connection
MIPS EJTAG / ZSP JTAG	Shared debug and test port for MIPS core and ZSP core

3 Applications

The KSZ8342Q provides the following external interfaces to support connection to one or more of the following peripherals shown in Figure 2.

- 2 Ethernet 802.3 transceiver interfaces
- 1 PCM interface for connection to analog telephone
- 1 DRAM (SDR) port
- 1 Flash (SPI NOR) port
- 1 UART port

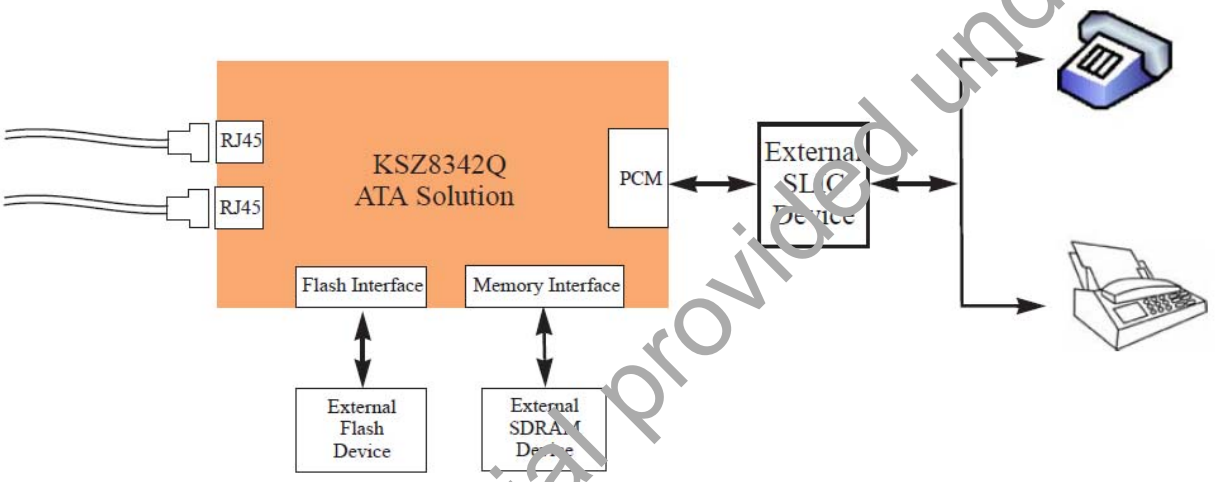
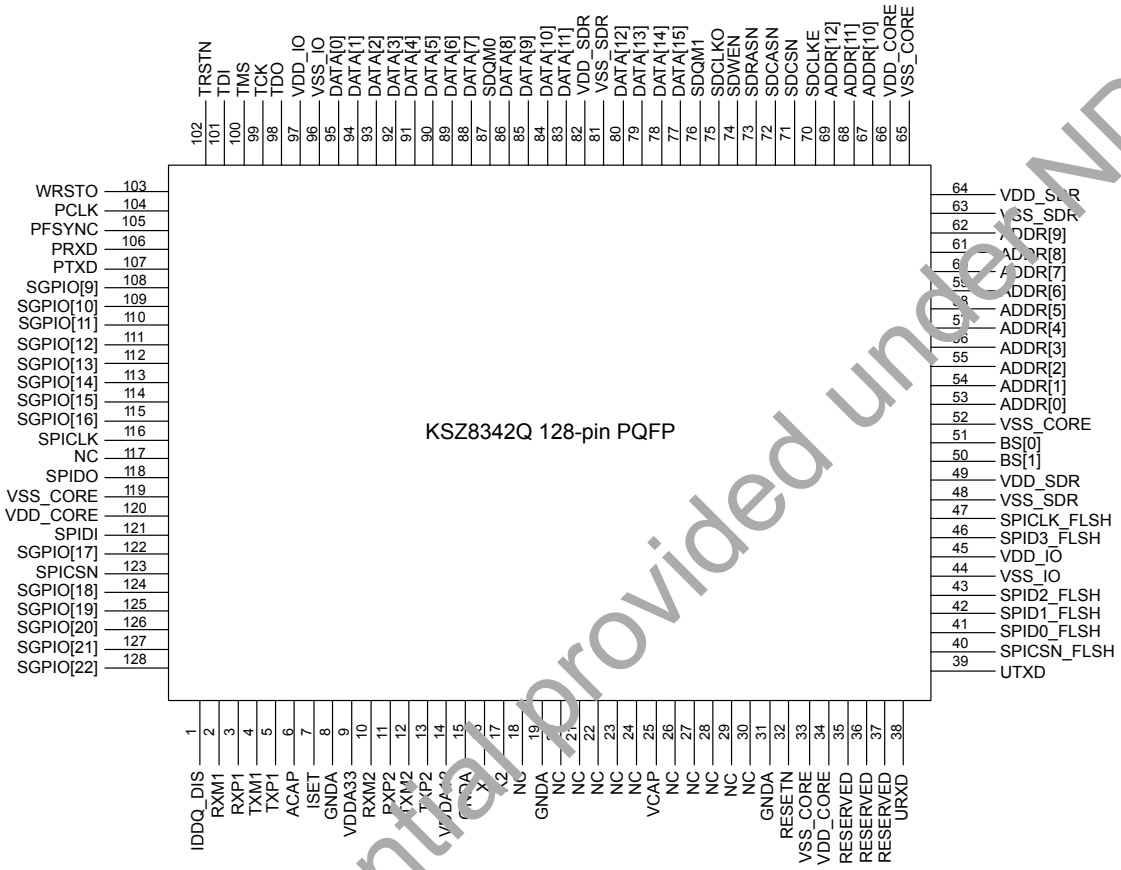


Figure 2. Typical KSZ8342 VoIP System Application

4 Part Ordering Information

Part Number	Temperature Range	Package	Lead Finish	Description
KSZ8342Q	0°C - +70°C	128-pin PQFP	Pb-free	Commercial temperature solution.
KSZ8342QI	-40°C - +85°C	128-pin PQFP	Pb-free	Industrial temperature solution.

5 Package Pinout



6 Pin Descriptions and Strapping Options

Table 2 lists the pin descriptions for the KSZ8342Q device. In this table, there are dedicated GPIO pins referred to by the name GPIO, and also multiplexed GPIO pin referred to by the name SGPIO.

Table 2. KSZ8342Q Pin Descriptions

KSZ8342Q Pin Number	Pin Name	Type	Description
1	IDDQ_DIS	I	This pin contains an internal pull-up and is used during device manufacturing and test. It must not be connected during normal operation.
2	RXM1	I/O	Physical receive or transmit signal (- differential).
3	RXP1	I/O	Physical receive or transmit signal (+ differential).
4	TXM1	I/O	Physical transmit or receive signal (- differential).
5	TXP1	I/O	Physical transmit or receive signal (+ differential).
6	ACAP	PWR	Connect to Pin 14 and a >1uF capacitor.
7	ISET	I	Set PHY transmit output current. Connect to ground through a 6.49 k Ohm 1% resistor.
8	GNDA	GND	Analog GND.
9	VDDA33	PWR	3.3V analog VDD.
10	RXM2	I/O	Physical receive or transmit signal (- differential).
11	RXP2	I/O	Physical receive or transmit signal (+ differential).
12	TXM2	I/O	Physical transmit or receive signal (- differential).
13	TXP2	I/O	Physical transmit or receive signal (+ differential).
14	VDDA12	PWR	Connect to Pin 6 (ACAP)
15	GNDA	GND	Analog GND.
16	X1	I LVTTL, 3.3-V tolerant	Crystal or oscillator clock connection. This signal is the source clock of the internal PLL. The clock frequency should be 25 MHz ± 50 ppm.

KSZ8342Q Pin Number	Pin Name	Type	Description
17	X2	O	Crystal clock pin. Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect.
18	NC	--	This pin is not connected and should be left open.
19	GNDA	GND	Analog GND.
20 - 24	NC	--	This pin is not connected and should be left open.
25	VCAP	O	Decoupling cap for internal biasing voltage.
26	NC	--	This pin is not connected and should be left open.
27	NC	--	This pin is not connected and should be left open.
28	NC	--	This pin is not connected and should be left open.
29	NC	--	This pin is not connected and should be left open.
30	NC	--	This pin is not connected and should be left open.
31	GNDA	GND	Analog GND.
32	RESETN	I	Hardware reset pin (active low).
33	VSS_CORE	GND	Digital core GND.
34	VDD_CORE	PWR	1.2V digital core VDD.
35 - 37	Reserved	I LVTTL Schmitt Trigger	This pin is used during manufacturing test and must be tied to ground during normal operation.
38	URXD	I LVTTL	UART receive data.
39	UTXD	O 8mA, LVTTL	UART transmit data.
40	SPICSN_FLSH	O 8mA, LVTTL	Serial NOR Flash memory chip select, asserted low. This output signal is connected to the chip select input of the NOR Flash.
41	SPIDO_FLSH	I/O 8mA, LVTTL	Serial NOR Flash data pin bit 0. This bidirectional signal is connected to the lowest-order data bit for 1-, 2- and 4-bit Flash devices.

KSZ8342Q Pin Number	Pin Name	Type	Description
42	SPID1_FLSH	I/O 8mA, LVTTL	Serial NOR Flash data pin bit 1. This bidirectional signal is connected to the high-order bit in a 2-bit Flash, or to bit 1 in a 4-bit Flash.
43	SPID2_FLSH	I/O 8mA, LVTTL	Serial NOR Flash data pin 2. This bidirectional signal is used only when connecting to a 4-bit Flash.
44	VSS_IO	GND	Digital I/O GND.
45	VDDIO	PWR	3.3V digital I/O VDD.
46	SPID3_FLSH	I/O 8mA, LVTTL	Serial NOR Flash data pin bit 3. This bidirectional signal is used only when connecting to a 4-bit Flash.
47	SPICLK_FLSH	O 8mA, LVTTL	Serial NOR Flash clock pin output. This signal connects to the clock input of the Flash device.
48	VSS_SDR	GND	GND for internal SDRAM memory controller.
49	VDD_SDR	PWR	3.3V for internal SDRAM memory controller.
50-51	BS[1:0]	I/O 8mA, LVTTL	SDRAM bank select [1:0]. For DRAM devices, these pins are used as SDRAM Bank Select pins BS[1:0].
52	VSS_CORE	GND	Digital core GND.
53-62	ADDR[0:9]	O SSTL18, LVTTL	SDRAM memory address pins [0:9].
63	VSS_SDR	GND	GND for internal SDRAM memory controller.
64	VDD_SDR	PWR	3.3V for internal SDRAM memory controller.
65	VSS_CORE	GND	Digital core GND.
66	VDD_CORE	PWR	1.2V digital core VDD.
67-69	ADDR[10:12]	O SSTL18, LVTTL	SDRAM memory address pins [10:12].
70	SDCLKE	O SSTL18, LVTTL	SDRAM clock enable. Clock Enable output for SDRAM interface. Can be used for power down mode.

KSZ8342Q Pin Number	Pin Name	Type	Description
71	SDCSN	O SSTL18, LVTTL	SDRAM chip select, asserted low.
72	SDCASN	O SSTL18, LVTTL	SDRAM column address Select, asserted low.
73	SDRASN	O SSTL18, LVTTL	SDRAM row address Select, asserted low.
74	SDWEN	O SSTL18, LVTTL	SDRAM write enable, asserted low.
75	SDCLKO	O SSTL18	SDRAM clock output. Clock output for SDRAM interface. Single ended clock for SDR, differential clock for SDRAM.
76	SDQM1	O SSTL18, LVTTL	SDRAM data mask.
77-80	DATA[15:12]	I/O SSTL18, LVTTL	Memory data bus[15:12] Bidirectional bus for 16-bit data input and output. The data bus is for SDRAM memory accesses.
81	VSS_SDR	GND	GND for internal SDRAM memory controller.
82	VDD_SDR	PWR	3.3V for internal SDRAM memory controller.
83-86	DATA[11:8]	I/O SSTL18, LVTTL	Memory data bus [11:8] Bidirectional bus for 16-bit data input and output. The data bus is for SDRAM memory accesses.
87	SDQM0	O SSTL18, LVTTL	SDRAM data mask.
88-95	DATA[7:0]	I/O SSTL18, LVTTL	Memory data bus [7:0] Bidirectional bus for 16-bit data input and output. The data bus is for SDRAM memory accesses.
96	VSS_IO	GND	Digital I/O GND.
97	VDD_IO	PWR	3.3V Digital I/O VDD.

KSZ8342Q Pin Number	Pin Name	Type	Description
98	TDO	O 4mA, LVTTL	JTAG test data output.
99	TCK	I LVTTL	JTAG test clock.
100	TMS	I LVTTL	JTAG test mode select.
101	TDI	I LVTTL	JTAG test data input.
102	TRSTN	I LVTTL Schmitt Trigger	JTAG test reset. Reset signal for JTAG controller.
103	WRSTO	O 8mA, LVTTL	Watchdog timer reset output When the Watchdog Timer expires, this signal will be asserted for at least 200 msec.
104	PCLK	I/O 8mA, LVTTL	PCM bus clock. Used for PCM bus timing.
105	PFSYNC	I/O 8mA, LVTTL	PCM frame sync. Frame synchronization signal for the PCM bus. This signal is synchronous to PCLK.
106	PRXD	I LVTTL	PCM receive data. Input data from PCM bus.
107	PTXD	O 8mA, LVTTL	PCM transmit data. Output data to PCM bus. The signal is synchronous to PCLK.
108 - 115	GPIO[9:16]	I/O 8mA, LVTTL	Shared GPIO pins 9 - 16.
116	SPICK	I/O 8mA, LVTTL	SLIC SPI clock output. This signal is used only for configuration and debug of the external SLIC device.
117	NC	--	This pin is not connected and should be left open.

KSZ8342Q Pin Number	Pin Name	Type	Description
118	SPIDO	O 8mA, LVTTL	SLIC SPI data output. This signal is used only for configuration and debug of the external SLIC device.
119	VSS_CORE	GND	Digital Core GND.
120	VDD_CORE	PWR	1.2V Digital Core VDD.
121	SPIDI	I 8mA, LVTTL	SLIC SPI data input. This signal is used only for configuration and debug of the external SLIC device.
122	SGPIO[17]	I/O 8mA, LVTTL	Shared GPIO pin 17.
123	SPICSN	O 8mA, LVTTL	SLIC SPI chip select output. This signal is used only for configuration and debug of the external SLIC device.
124-128	GPIO[18:22]	I/O 8mA, LVTTL	Shared GPIO pins 18 - 22.

7 System Memory Map

As noted earlier, the KSZ8342 supports up to 64MB of SDR memory. It supports up to 64MB of Serial Flash memory.

The system memory map is 512MB in size and is organized as shown in Figure 3. It consists of

- **System Registers**: 64KB located at the top of the memory map.
- **Flash memory**: is remapped at boot time by software. The KSZ8342 supports serial NOR Flash devices of 64MB in size. For NAND Flash devices, the memory is accessed indirectly. As such, NAND Flash is accessed via a 64KB space in the memory map.
- **ZSP Memory**: For the ZSP memory, bits 31:19 of the *ZSP External Memory* register located at offset address 0x0014 determines where the 512KB block of ZSP memory resides in physical address space.
- **SDR memory**: located at the bottom of the memory map.

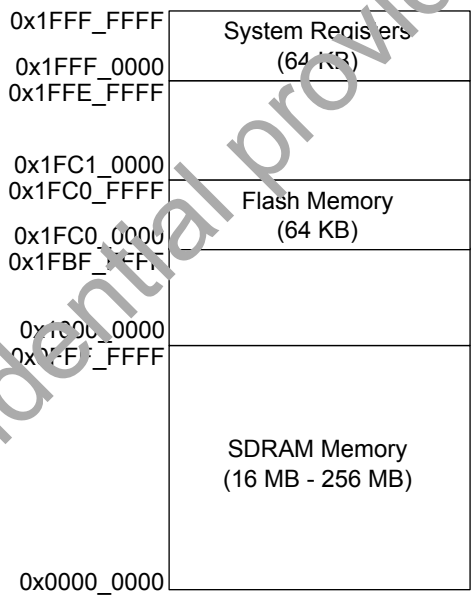


Figure 3. System Memory Map

8 MIPS Processor Core

The KSZ8342 integrates a MIPS32 M4KEc as the central processing unit for the VoIP SoC. This includes optimized MIPS32 M4KEc configuration options for VoIP, including cache size, cache organization, CPU register size, and memory BIST. This section provides an overview of the MIPS Processor. For further details see the section **"**MIPS32® 4KEc® Processor Core Datasheet, Revision 02.03, March 4, 2008."

The KSZ8342 implements the M4KEc with the following characteristics:

- 5 pipeline stages
- Clock speeds of 25/62.5/125/166 MHz
- 2 way set associative 16 KB I-Cache
- 2 way set associative 8 KB D-Cache
- 2 register file sets
- EJTAG TAP controller
- 4/2 Instruction/Data hardware breakpoints

The MIPS CPU clock rate is set via bits 2:0 of the *System Clock and Bus Control* register located at offset 0x000C.

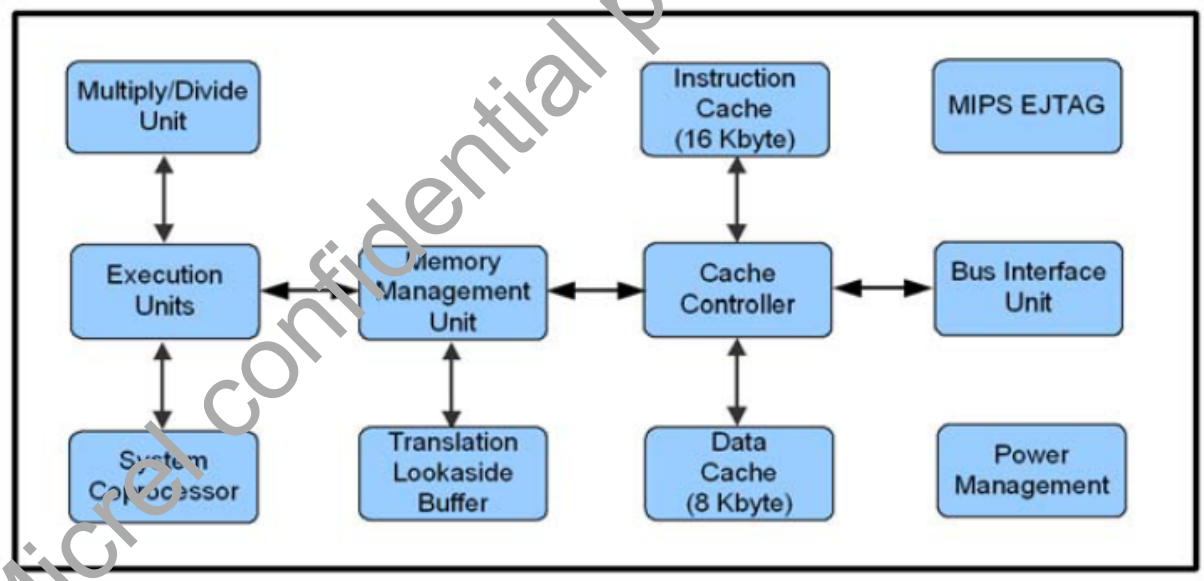


Figure 4. MIPS 4KEc Processor Block Diagram

8.1 Execution Units

The 4KEc core execution unit in the KSZ8342 VoIP solution implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous multiply/divide unit. The 4KEc™ core contains thirty-two 32-bit general-purpose registers used for integer operations and address calculation. The register file consists of two read ports and one write port and is fully bypassed to minimize operation latency in the pipeline.

The execution unit includes:

- 32-bit adder used for calculating the data address
- Address unit for calculating the next instruction address
- Branch determination and branch target calculation
- Load aligner
- Bypass multiplexers used to avoid stalls when executing instructions streams where data producing instructions are followed closely by consumers of their results.
- Zero/One detect unit for implementing the CLZ and CLO instructions
- Arithmetic Logic Unit (ALU) for performing bitwise logical operations

8.2 Multiply/Divide Unit (MDU)

The 4KEc core in the KSZ8342 VoIP solution contains a multiply/divide unit (MDU) that includes a separate pipeline for multiply and divide operations. This pipeline operates in parallel with the integer unit (IU) pipeline and does not stall when the IU pipeline stalls. This allows long-running MDU operations, such as a divide, to be partially masked by system stalls and/or other integer unit instructions.

The MDU supports execution of a 16x16 or 32x16 multiply operation every clock cycle; 32x32 multiply operations can be issued every other clock cycle. Appropriate interlocks are implemented to stall the issue of back-to-back 32x32 multiply operations. Multiply operand size is automatically determined by logic built into the MDU.

Divide operations are implemented with a simple 1 bit per clock iterative algorithm. Any attempt to issue a subsequent MDU instruction while a divide is still active causes an IU pipeline stall until the divide operation is completed.

8.3 System Coprocessor

The MIPS 4KEc system coprocessor (CP0) in the KSZ8342 VoIP solution is responsible for the virtual-to-physical address translation and cache protocols, the exception control system, the processor's diagnostics

capability, and the operating modes (kernel, user, and debug), interrupts enabled or disabled. Configuration information such as cache size and set associativity is available by accessing the CP0 registers.

8.4 Memory Management Unit

The MIPS 4KEc core in the KSZ8342 VoIP solution contains a fully functional MMU that interfaces between the execution unit and the cache controller. The TLB consists of two address translation buffers; a 16 dual-entry fully associative Joint TLB (JTLB) and a two-entry fully associative Instruction TLB (ITLB).

When an instruction address is calculated, the virtual address is compared to the contents of the two-entry ITLB. If the address is not found in the ITLB, the JTLB is accessed. If the entry is found in the JTLB, that entry is then written into the ITLB. If the entry is not found in the JTLB, a TLB refill exception is taken.

8.5 Translation Lookaside Buffer

The TLB consists of two address translation buffers;

- 16 dual-entry fully associative Joint TLB (JTLB)
- 2-entry fully associative Instruction TLB (ITLB)

8.5.1 Joint TLB

The MIPS 4KEc in the KSZ8342 VoIP solution implements a 16 dual-entry, fully associative Joint TLB (JTLB). The purpose of the TLB is to translate virtual addresses and their corresponding address space identifier (ASID) into a physical memory address. The JTLB is organized in page pairs to minimize the overall size. Each *tag* entry corresponds to 2-data entries, an even page entry and an odd page entry. The highest order virtual address bit not participating in the tag comparison is used to determine which of the data entries is used. Since page size can vary on a page-pair basis, the determination of which address bits participate in the comparison and which bit is used to make the even-odd determination is decided dynamically during the TLB lookup.

8.5.2 Instruction TLB

The Instruction TLB (ITLB) is a small 2-entry, fully associative TLB dedicated to performing translations for the instruction stream. The ITLB only maps 4-Kbyte pages/sub-pages. The ITLB is managed by hardware and is transparent to software. The larger JTLB is used for load/store address translations and as a backing store for the ITLB. If a fetch address cannot be translated by the ITLB, the JTLB is used to attempt to translate it in the following clock cycle. If successful, the translation information is copied into the ITLB for future use.

8.6 Cache Controller

The MIPS 4KEc core cache controller in the KSZ8342 VoIP solution is used to control accesses to the instruction and data cache. The KSZ8342 implements a 16 KB instruction cache and an 8 KB data cache. Each cache can each be accessed in a single processor cycle. In addition, each cache has its own 32-bit data path and both caches can be accessed in the same pipeline clock cycle. Bus Interface (BIU) The MIPS 4KEc Bus Interface Unit (BIU) in the KSZ8342 VoIP solution controls the external interface signals. Additionally, it contains the implementation of the 32-byte collapsing write buffer. The purpose of this buffer is to store and combine write transactions before issuing them at the external interface. Since the 4KEc core caches follow a write-through cache policy, the write buffer significantly reduces the number of writes transactions on the external interface as well as reducing the amount of stalling in the core due to issuance of multiple writes in a short period of time.

8.7 Enhanced JTAG (EJTAG)

The MIPS 4KEc core in the KSZ8342 VoIP solution includes an Enhanced JTAG (EJTAG) interface for use in the software debug of application and kernel code. In addition to standard user mode and kernel modes of operation, the 4KEc core provides a Debug mode which is entered after a debug exception (derived from a hardware breakpoint, single-step exception, etc.) is taken and continues until a debug exception return (DERET) instruction is executed. During this time the processor executes the debug exception handler routine. The EJTAG interface operates through the Test Access Port, a serial communication used for transferring test data in and out of the 4KEc core. In addition to the standard JTAG instructions, special instructions defined in the EJTAG specification define what registers are selected and how they are used. In the KSZ8342, the five external JTAG pins are multiplexed internally between the MIPS JTAG unit and the ZSP JTAG unit. Similarly, the TDO output pin is multiplexed between the two JTAG units. Which value is driven onto the TDO pin is determined using bit 8 of the ZSP Control register located at offset address 0x0018. If this bit is cleared, the result from the MIPS JTAG unit is driven onto TDO. If this bit is set, the result from the ZSP JTAG unit is driven onto TDO.

8.8 Power Management

The MIPS 4KEc core in the KSZ8342 VoIP solution offers a number of power management features, including low-power design, active power management and power-down modes of operation. The 4KEc core is a static design that supports a WAIT instruction designed to signal the rest of the device that execution and clocking should be halted, reducing system power consumption during idle periods.

The 4KEc™ core provides two mechanisms for system level low power support:

- Register controlled power management
- Instruction controlled power management

9 ZSP Voice Module Processor

The ZSP is to process audio data between the PCM controller and the MIPS CPU. Its main function includes voice data compression, decompression, PLC, dial tone generation, and miscellaneous speech CODEC functions. It contains an internal DMA for direct data transfer, between the ZSP and system DRAM/PCM (or A/D D/A). A special reset signal is controlled via a system register is used to enable the DMA (channel 0) to self-start voice codec firmware transfer onto I-MEM for the ZSP core.

Note that the ZSP processor does not include any programmable function that can be controlled by the user. All ZSP programming is done through the MIPS processor. The initial clock rate for the ZSP module is determined as shown in **Error! Reference source not found.**. This section provides an overview of the ZSP Voice Module Processor. For further details see the section “ZSP400 Digital Signal Processor Architecture, December 2001.”

9.1 ZSP Architecture

The ZSP core is a 16-bit fixed point four-way superscalar digital signal processor (DSP) core. The five-stage pipeline processes up to 20 instructions at a time. The ZSP includes two multiply-accumulate execution unit (MACs) and two arithmetic logic units (ALUs).

The ZSP supports contains a dual 5-stage pipeline that supports single cycle add-compare-select, bit manipulation, and 32-bit arithmetic and logic operations. The ZSP core generates separate 16-bit addresses for instruction fetches and data memory transactions.

9.2 8.2 ZSP Functional Units

The ZSP core consists of seven functional units:

- Data Unit
- Instruction Unit (32 KW)
- Pipeline Control Unit (32 KW)
- Arithmetic Logic Unit
- Multiply Accumulate Unit
- Operand Register File Unit
- Device Emulation Unit

A block diagram of the core illustrating how the functional units are interconnected is shown in Figure 5. Each of these blocks is described briefly in the following subsections.

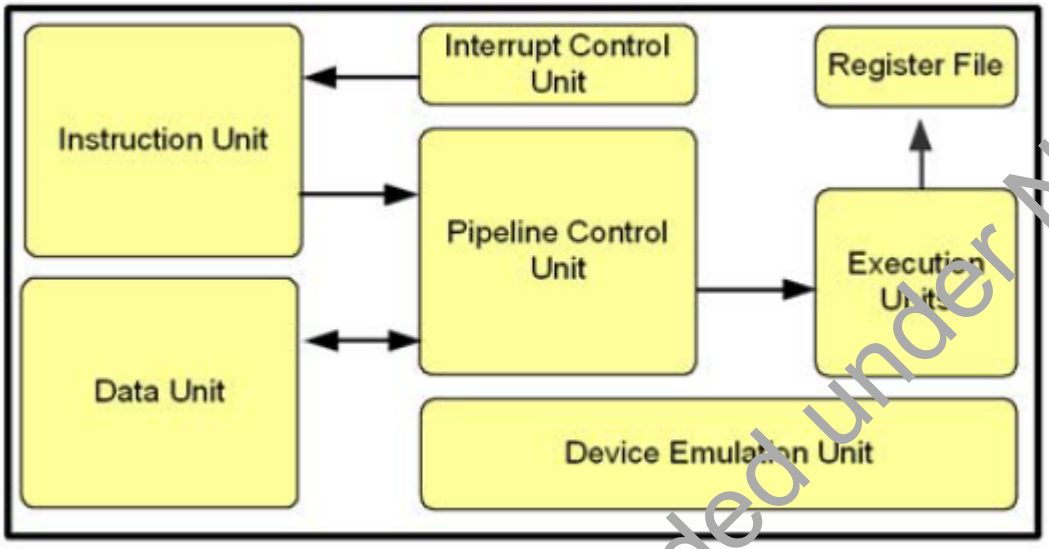


Figure 5. ZSP Internal Block Diagram

9.2.1 Instruction Unit

The instruction unit is comprised of the instruction cache, prefetch unit, program counter control, and instruction dispatcher. The instruction cache is direct-mapped and holds eight lines of four words each. Four instructions are prefetched each clock cycle and forwarded to the pipeline control unit for grouping. The prefetch unit utilizes static branch prediction and prefetch techniques to minimize cache miss penalties and reduce pipeline stalls.

9.2.2 Data Unit

The data unit is comprised of the data cache, data prefetch unit, circular buffers, and load/store arbitration unit. Each cycle the data unit can prefetch and cache four data words. The write logic can perform one single or double word store per cycle. The data unit also provides hardware for the implementation of two circular buffers and three data linking registers.

9.2.3 Pipeline Control Unit

The pipeline control unit groups instructions for parallel execution and synchronizes the execution of these instructions through the pipeline. To perform instruction grouping, the pipeline control unit resolves data and resource dependencies in the program sequence. This allows the hardware to schedule instructions for execution by the functional units, removing this task from the programmer or compiler. The pipeline control unit handles branch mispredictions, interrupts, and stalls from external memory accesses.

9.2.4 Execution Units

The ZSP contains two identical 16-bit ALUs which can work independently or together to form a single 32-bit ALU. In addition to traditional ALU functionality, the ALUs also provide bit manipulation and normalization capability.

In addition to the ALU's, the ZSP integrates two MAC units that can work together or independently. Independently, they can each perform a 16-bit by 16-bit multiply with a single 40-bit accumulation in a single cycle. Together, they work to perform a 32-bit by 32-bit multiply with 40-bit accumulation in a single cycle. The MACs also contain hardware support for complex multiplies and the functionality to perform a single-cycle add-compare select for Viterbi decoding.

9.2.5 Register Files

The ZSP has two register files: the operand register file and the control register file. The operand register file consists of 16 general purpose registers, half of which are shadowed. The control register file maintains registers which control the state and operation of the core. All registers are user visible (read and write).

9.2.6 Device Emulation Unit

The ZSP contains dedicated logic to support sophisticated emulation and debugging functions.

9.3 ZSP Boot Process

The ZSP processor in the KSZ8342 VoIP solution does not boot automatically on reset, but rather remains in the reset state. To boot the ZSP processor, software must set bit 0 of the *ZSP Control* register located at offset address 0x0018.

10 3-Port Switch

The KSZ8342 contains a 3-port switch. Two ports are used for external Ethernet communication and facilitate power efficient switching in 10/100 Mbps Ethernet applications. The third port is used internally to communicate with the Ethernet DMA controller. This concept is shown in Figure 6. Each of the blocks in this figure is described in the following subsections.

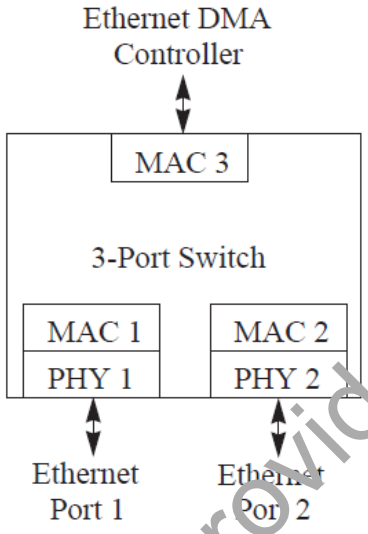


Figure 6. 3-Port Switch Connections

The switch contains advanced power management and sophisticated QoS features, including IPv6 priority classification support. Advanced power management features of the 3-port switch include hardware power down, software power down, per port power down, and the energy detect mode that shuts downs the transceiver when a port is idle.

The KSZ8342 VoIP SoC 3-port switch contains the following main features:

- Low Power (32 bit data width @ 31.25MHz)
- Non-blocking packet switching throughput at wire speed
- 2x 802.3 PHYs + 1x MII for internal EDMA
- IEEE 802.1Q VLAN support for up to 16 groups full-range of VLANID)
- VLAN ID tag/un-tag options, per-port basis
- IEEE 802.1p/q tag insertion or removal on a per port basis (egress)
- Programmable rate limiting from 0 to 100 Mbps at the ingress and egress ports

- Broadcast storm protection
- IEEE 802.1D Spanning Tree Protocol support
- Special Tagging Mode to inform the processor which ingress port
- IGMP v1/v2 Snooping support for multicast packet filtering
- Double Tagging support

10.1 Media Access Controller (MAC)

The KSZ8342 contains a dedicated Media Access Controller (MAC) for each Ethernet port. The MAC processes data moving between the 3-port switch and the PHY as shown in Figure 1. The MAC performs the following functions:

- Address Lookup
- Learning
- Migration
- Aging
- Forwarding

10.1.1 Address Lookup

An internal lookup table stores MAC addresses and their associated information. It contains a 1K Unicast address table plus switching information.

10.1.2 Learning

The KSZ8342 is guaranteed to learn 1K addresses and distinguishes itself from hash-based lookup tables, which depending on the operating environment and probabilities, may not guarantee the absolute number of addresses it can learn. The internal lookup engine updates its table with a new entry if the following conditions are met:

1. The received packet's Source Address (SA) does not exist in the lookup table.
2. The received packet is good; the packet has no receiving errors, and is of legal length. The lookup engine inserts the qualified SA into the table, along with the port number and time stamp. If the table is full, the last entry of the table is deleted to make room for the new entry.

10.1.3 Migration

The internal lookup engine also monitors whether a station has moved. If a station has moved, it will update the table accordingly. Migration happens when the following conditions are met:

1. The received packet's source address is in the table but the associated source port information is different.

2. The received packet is good; the packet has no receiving errors, and is of legal length.

The lookup engine will update the existing record in the table with the new source port information.

10.1.4 Aging

The lookup engine updates the time stamp information of a record whenever the corresponding SA appears. The time stamp is used in the aging process. If a record is not updated for a period of time, the lookup engine removes the record from the table. The lookup engine constantly performs the aging process and will continuously remove aging records. The aging period is about 300 seconds. This feature can be enabled or disabled through register 3 (0x03) bit [2].

10.1.5 Forwarding

The KSZ8342 forwards packets using the algorithm that is depicted in the following flowcharts. Figure 7 shows stage one of the forwarding algorithm where the search engine looks up the VLAN ID, static table, and dynamic table for the destination address, and comes up with "port to forward 1" (PTF1). PTF1 is then further modified by spanning tree, IGMP snooping, port mirroring, and port VLAN processes to come up with "port to forward 2" (PTF2), as shown in Figure 8. The packet is sent to PTF2.

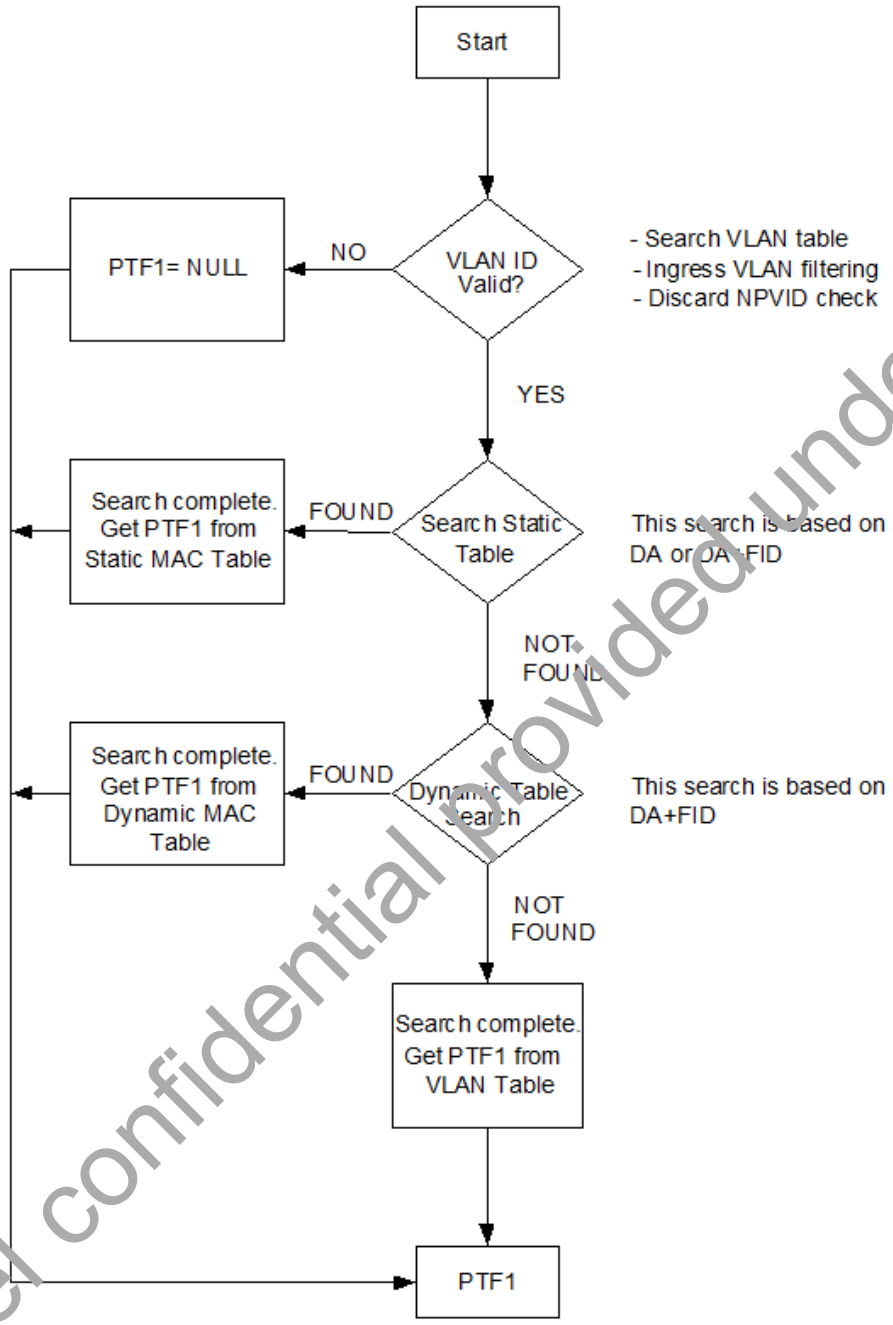


Figure 7. Destination Address Lookup Flow Chart, Stage 1

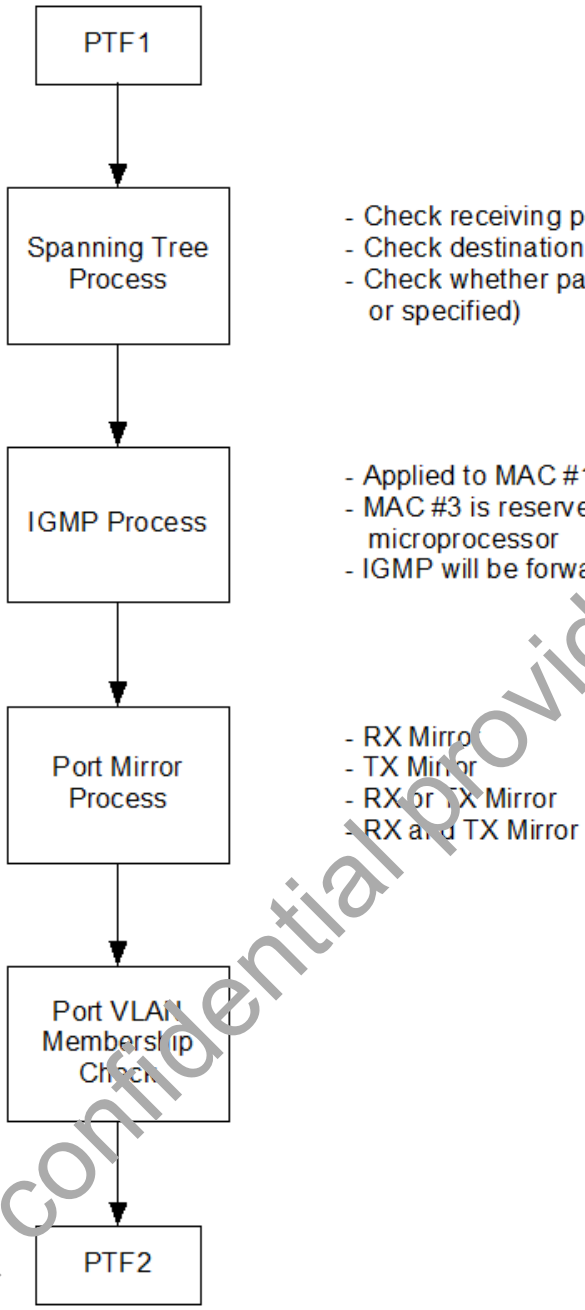


Figure 8. Destination Address Resolution Flow Chart, Stage 2

The switch will not forward the following types of packets:

- Error packets: These include framing errors, Frame Check Sequence (FCS) errors, alignment errors, and illegal size packet errors.
- IEEE802.3x PAUSE frames: The switch intercepts these packets and performs full duplex flow control accordingly.
- Local packets based on destination address (DA) lookup: If the destination port from the lookup table matches the port from which the packet originated, the packet is defined as "local."

10.1.6 MAC Operation

The KSZ8342 MAC strictly abides by IEEE 802.3 standards to maximize compatibility.

Inter Packet Gap (IPG)

If a frame is successfully transmitted, the 96 bits time IPG is measured between the two consecutive MTXEN. If the current packet is experiencing collision, the 96 bits time IPG is measured from MCRS and the next MTXEN.

Back-Off Algorithm

The KSZ8342 implements the IEEE 802.3 standard for the binary exponential back-off algorithm, and optional "aggressive mode" back-off. After 16 collisions, the packet is optionally dropped depending on the switch configuration for register 4 (0x04) bit [3].

Late Collision

If a transmit packet experiences collisions after 512 bit times of the transmission, the packet is dropped.

Illegal Frames

The KSZ8342 discards frames less than 64 bytes, and can be programmed to accept frames up to1518 bytes, 1536 bytes or 1916 bytes. These maximum frame size settings are programmed in register 4 (0x04). Since the KSZ8342 supports VLAN tags, the maximum sizing is adjusted when these tags are present.

Full Duplex Flow Control

The KSZ8342 supports standard IEEE 802.3x flow control frames on both transmit and receive sides. On the receive side, if the KSZ8342 receives a pause control frame, the KSZ8342 will not transmit the next normal frame until the timer, specified in the pause control frame, expires. If another pause frame is received before the current timer expires, the timer will be updated with the new value in the second pause frame. During this period (while it is flow controlled), only flow control packets from the KSZ8342 are transmitted.

On the transmit side, the KSZ8342 has intelligent and efficient ways to determine when to invoke flow control. The flow control is based on availability of the system resources, including available buffers, available transmit queues and available receive queues.

The KSZ8342 will flow control a port that has just received a packet if the destination port resource is busy. The KSZ8342 issues a flow control frame (XOFF), containing the maximum pause time defined by the IEEE 802.3x standard. Once the resource is freed up, the KSZ8342 sends out the other flow control frame (XON) with zero pause time to turn off the flow control (turn on transmission to the port). A hysteresis feature is provided to prevent the flow control mechanism from being constantly activated and deactivated.

The KSZ8342 flow controls all ports if the receive queue becomes full.

Half-Duplex Backpressure

A half-duplex backpressure option (not in IEEE 802.3 standards) is also provided. The activation and deactivation conditions are the same as full duplex flow control. If backpressure is required, the KSZ8342 sends preambles to defer the other stations' transmission (carrier sense deference).

To avoid jabber and excessive deference (as defined in the 802.3 standard), after a certain time, the KSZ8342 discontinues the carrier sense and then raises it again quickly. This short silent time (no carrier sense) prevents other stations from sending out packets thus keeping other stations in a carrier sense deferred state. If the port has packets to send during a backpressure situation, the carrier sense type backpressure is interrupted and those packets are transmitted instead. If there are no additional packets to send, carrier sense type backpressure is reactivated again until switch resources free up. If a collision occurs, the binary exponential back-off algorithm is skipped and carrier sense is generated immediately, thus reducing the chance of further collisions and carrier sense is maintained to prevent packet reception. To ensure no packet loss in 10 BASE-T or 100 BASE-TX half duplex modes, the user must enable the following:

- Aggressive back-off (register 3 (0x03), bit [0])
- No excessive collision drop (register 4 (0x04), bit [3])

Note: These bits are not set as defaults, as this is not the IEEE standard.

Broadcast Storm Protection

The KSZ8342 has an intelligent option to protect the switch system from receiving too many broadcast packets. As the broadcast packets are forwarded to all ports except the source port, an excessive number of switch resources (bandwidth and available space in transmit queues) may be utilized. The KSZ8342 has the option to include "multicast packets" for storm control. The broadcast storm rate parameters are programmed globally, and can be enabled or disabled on a per port basis. The rate is based on a 67ms interval for 100BT

and a 500ms interval for 10BT. At the beginning of each interval, the counter is cleared to zero, and the rate limit mechanism starts to count the number of bytes during the interval. The rate definition is described in register 6 (0x06) and 7 (0x07). The default setting is 0x63 (99 decimal).

This is equal to a rate of 1%, calculated as follows:

148,800 frames/sec * 67ms/interval * 1% = 99 frames/interval (approx.) = 0x63

Note: The number 148,800 frames/sec is based on 64-byte block of packets in 100BASE-TX with 12 bytes of IPG and 8 bytes of preamble between two packets.

Port Individual MAC Address and Source Port Filtering

The KSZ8342 provide individual MAC address for port 1 and port 2 respectively. They can be set at register 142-147 and 148-153. With this feature, the CPU connected to the port 3 can receive the packets from two internet subnets which have their own MAC address.

The packet will be filtered if its source address matches the MAC address of port 1 or port 2 when the register 21 and 37 bit 6 is set to 1 respectively. For example, the packet will be dropped after it completes the loop of a ring network.

10.2 Physical Layer (PHY)

The KSZ8342 implements a 2-port 10/100 Mbps PHY interface that contains the following main features.

- On-chip LDO
- Loopback PHY BIST test
- IEEE 802.3az MAC/PCS EEE function
- Enhanced PLL for low EMI transmission
- Intelligent power saving modes
- On-chip termination

Each Ethernet port in the KSZ8342 VoIP solution supports the following transfer protocols.

- 100BASE-T Transmit
- 100BASE-T Receive
- 10BASE-T Transmit
- 10BASE-T Receive

Each of these functions is described in the following subsections.

10.2.1 100BASE-T Transmit

The transmit function of the 100BASE-TX performs:

- Parallel-to-serial conversion
- 4B/5B coding
- scrambling
- NRZ-to-NRZI conversion
- MLT3 encoding and transmission

The data flow through the transmit circuit is as follows:

1. Parallel-to-serial conversion translates the MII data from the MAC into a 125MHz serial bit stream.
2. The data and control stream are converted into 4B/5B coding, followed by a scrambler.
3. The serialized data is converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output.
4. The output current is set by an external 1% 11.8k Ohm resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 100BASE-T output is also incorporated into the 100BASE-TX transmitter.

The 100BASE-T transmit logic also contains a scrambler. The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander. Transmitted data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence, and the receiver then de-scrambles the incoming data stream using the same sequence as at the transmitter.

10.2.2 100BASE-T Receive

The 100BASE-TX receiver function performs:

- Adaptive equalization
- DC restoration
- MLT3-to-NRZI conversion
- Data and clock recovery
- NRZI-to-NRZ conversion
- De-scrambling
- 4B/5B decoding
- Serial-to-parallel conversion

Incoming data passes through an equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance.

The variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

The equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range.

The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

10.2.3 10BASE-T Transmit

The 10BASE-T driver is incorporated with the 100BASE-TX driver to allow for transmission using the same magnetic. They are internally wave-shaped and pre-emphasized into outputs with typical 2.3V amplitude. The harmonic contents are at least 27dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

10.2.4 10BASE-T Receive

On the receive side, input buffers and level detecting squelch circuits are employed. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400mV or with short pulse widths to prevent noise at the RXP-or-RXM input from falsely triggering the decoder.

When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8342 decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

10.2.5 MDI/MDI-X Auto Crossover

To eliminate the need for crossover cables between similar devices, the KSZ8342 VoIP solution supports HP Auto MDI/MDI-X and IEEE 802.3u standard MDI/MDI-X auto crossover. HP Auto MDI/MDI-X is the default. The auto-sense function detects remote transmit and receive pairs and correctly assigns transmit and receive pairs for the KSZ8342 device. This feature is extremely useful when end users are unaware of cable types, and also, saves on an additional uplink configuration connection. The auto-crossover feature can be disabled through the port control registers, or MIIM PHY registers.

10.2.6 Auto-Negotiation

The KSZ8342 conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3u specification. Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the best common mode of operation. In auto negotiation, link partners advertise their capabilities across the link to each other. If auto-negotiation is not supported or the KSZ8342 link partner is forced to bypass auto-negotiation, the KSZ8342 sets its operating mode by observing the signal at its receiver. This is known as parallel detection, and allows the KSZ8342 to establish link by listening for a fixed signal protocol in the absence of auto-negotiation advertisement protocol. Figure 9 shows a flow diagram of the auto-negotiation process.

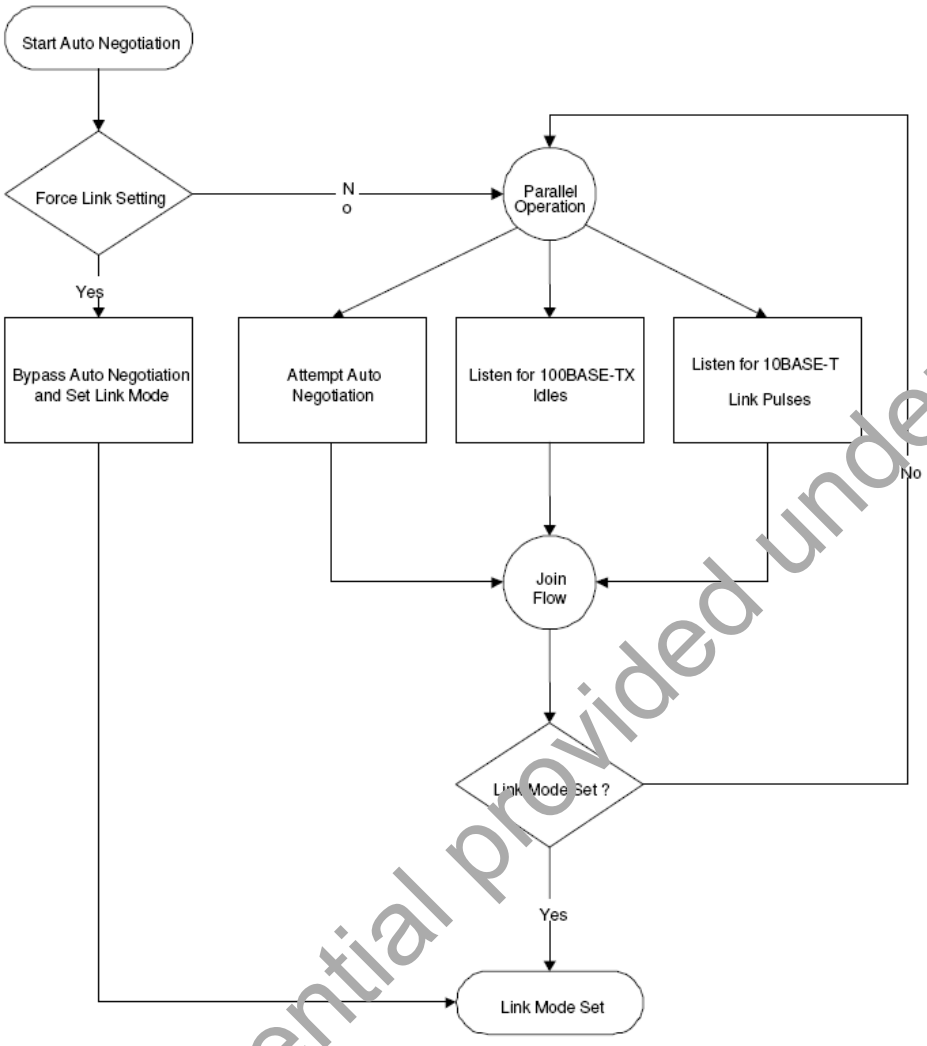


Figure 9. Auto Negotiation Process

10.2.7 PHY Power Management

The KSZ8342 supports enhanced power management feature in low power state with energy detection to ensure low-power dissipation during device idle periods. There are three operating modes under the power management function

- Normal Operation Mode
- Energy Detect Mode
- Port Based Power Down Mode

Table 3 indicates all internal function blocks status under four different power management operation modes. For more information, please refer to Section 10, “Energy Efficient Ethernet.”

Normal Operating Mode

This is the default setting bit[1:0] = 00 in register 195 after the chip power-up or hardware reset. When the KSZ8342 is in this mode, all PLL clocks are running. The PHY and MAC are on and the host interface is ready for a CPU read or write.

During the normal operation mode, the host CPU can set the bit[1:0] in register 195 to transit the current normal operation mode to any one of the other three power management operation

Energy Detect Mode

The energy detect mode provides a mechanism to save more power than in the normal operation mode when the KSZ8342 is not connected to an active link partner.

This mode can result in a power savings of up to 50% relative to normal mode. If the cable is unplugged, the KSZ8342 can automatically enter to a low power state (energy detect mode). In this mode the KSZ8342 transmits 120ns width pulses at a 1 pulse/s rate. Once activity resumes due to plugging a cable or attempting by the far end to establish link, the KSZ8342 can automatically power up to normal power state from the energy detect mode.

Energy detect mode consists of two states, normal power state and low power state. While in low power state, the KSZ8342 reduces power consumption by disabling all circuitry except the energy detect circuitry of the receiver. The energy detect mode is entered by setting bit[1:0] = 01 in register 195. When the KSZ8342 is in this mode, it monitors the cable energy. If there is no energy on the cable for a time longer than the programmed value in bits 7:0 (Go-Sleep time) in register 196, the KSZ8342 will go into a low power state.

Port based Power Down Mode

The KSZ8342 features a per-port power down mode. To save power, a PHY port that is not in use can be powered down via port control register 29 or 45 bit 3, or MIIM PHY register. It will saves about 15 mA per port.

Table 3. KSZ8342 Functional Block State per Power Management Operating Mode

KSZ8342 Functional Block	Power Management Operating Mode	
	Normal	Energy Detect
Internal PLL clocks	Enabled	Disabled
Transmit/Receive PHY	Enabled	Energy detect at Rx

MAC	Enabled	Disabled
Host Interface	Enabled	Disabled

10.3 Advanced Switch Functions

10.3.1 Bypass Mode

The KSZ8342 also offer a by-pass mode which enables system- level power saving. When the CPU (connected to Port 3) enters a power saving mode of power down or sleeping mode, the KSZ8342 switches to the by-pass mode in which the switch function between Port1 and Port2 is sustained. In the by-pass mode, the packets with DA to port 3 will be dropped and by pass the internal buffer memory, making the buffer memory more efficiency for the data transfer between port 1 and port 2. Specially, the power saving get more in energy detect mode with the by-pass to be used.

10.3.2 IEEE 802.1Q VLAN Support

The KSZ8342 supports 16 active VLANs out of the 4096 possible VLANs specified in the IEEE 802.1Q specification. KSZ8342 provides a 16-entry VLAN Table, which converts the 12-bits VLAN ID (VID) to the 4-bits Filter ID (FID) for address lookup. If a non-tagged or null-VID-tagged packet is received, the ingress port default VID is used for lookup. In VLAN mode, the lookup process starts with VLAN table lookup to determine whether the VID is valid. If the VID is not valid, the packet is dropped and its address is not learned. If the VID is valid, the FID is retrieved for further lookup. The FID + Destination Address (FID+DA) are used to determine the destination port. The FID + Source Address (FID+SA) are used for address learning.

Table 4. FID+ Destination Address Lookup in VLAN Mode

Destination Address Found in Static MAC Table?	Use FID Flag?	FID Match	DA + FID Found in Dynamic MAC Table?	Action Taken
No	Don't Care	Don't Care	No	Broadcast to the membership ports defined in the VLAN table bits [18:16]
No	Don't Care	Don't Care	Yes	Send to the destination port defined in the Dynamic MAC address table bits [53:52].
Yes	0	Don't Care	Don't Care	Sent to the destination port(s) defined in the Static MAC address table bits [50:48].
Yes	1	No	No	Broadcast to the membership ports defined in the VLAN table bits [18:16].
Yes	1	No	Yes	Send to the destination port defined in the Dynamic MAC address table bits [53:52]
Yes	1	Yes	Don't Care	Sent to the destination port(s) defined in the

Destination Address Found in Static MAC Table?	Use FID Flag?	FID Match	DA + FID Found in Dynamic MAC Table?	Action Taken
				Static MAC address table bits [50:48].

10.43-Port Switch QoS Priority Support

The KSZ8342 provides Quality of Service (QoS) for applications such as VoIP and video-conferencing. Offering four priority queues per port, the per-port transmit queue can be split into four priority queues, with queue 3 being the highest priority queue and queue 0 being the lowest. The transmit queue is split into four sections via the register interface. Note that if a port's transmit queue is not split, high priority and low priority packets have equal priority in the transmit queue.

There is an additional option to either always deliver high priority packets first, or use weighted fair queuing for the four priority queues.

10.4.1 Port-Based Priority

With port-based priority, each ingress port is individually classified as a high priority receiving port. All packets received at the high priority receiving port are marked as high priority and are sent to the high-priority transmit queue if the corresponding transmit queue is split.

10.4.2 802.1p-Based Priority

For 802.1p-based priority, the KSZ8342 examines the ingress (incoming) packets to determine whether they are tagged. If tagged, the 3-bit priority field in the VLAN tag is retrieved and compared against the "priority mapping" value. The "priority mapping" value is programmable via registers.

Figure 10 illustrates how the 802.1p priority field is embedded in the 802.1Q VLAN tag.

The KSZ8342 provides the option to insert or remove the priority tagged frame's header at each individual egress port. This header, consisting of the 2 bytes VLAN Protocol ID (VPID) and the 2- byte Tag Control Information field (TCI), is also referred to as the IEEE 802.1Q VLAN tag.

Tag Insertion selects which source port (ingress port) PVID can be inserted on the egress port for ports 1, 2 and 3, respectively. At the egress port, untagged packets are tagged with the ingress port's default tag. The CRC is recalculated for both tag insertion and tag removal.

802.1p Priority Field Re-mapping is a QoS feature that allows the KSZ8342 to set the "User Priority Ceiling" at any ingress port. If the ingress packet's priority field has a higher priority value than the default tag's priority field of the ingress port, the packet's priority field is replaced with the default tag's priority field.

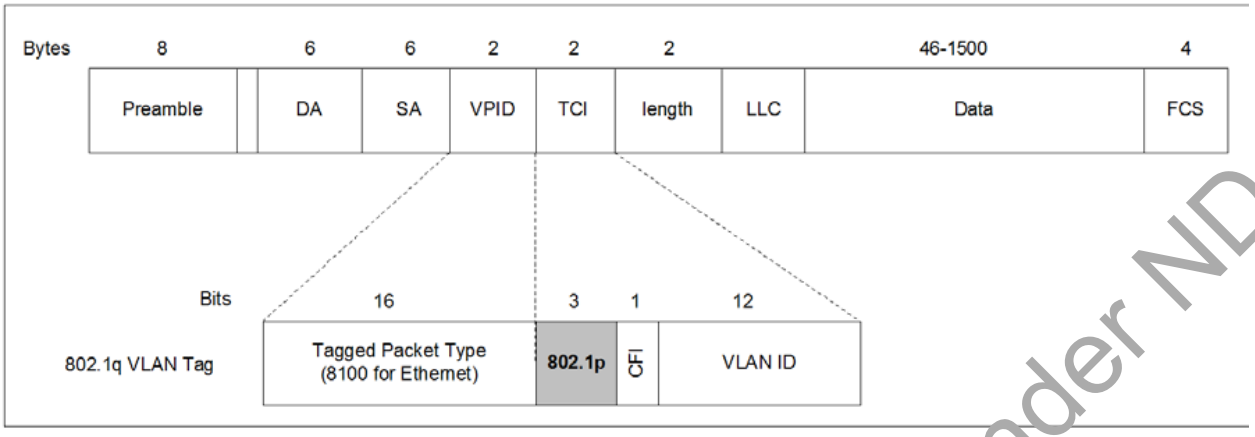


Figure 10. 802.1p Priority Field Format

10.4.3 DiffServ-Based Priority

DiffServ-based priority implements a fully decoded, 64-bit Differentiated Services Code Point (DSCP) protocol to determine packet priority from the 6-bit ToS field in the IP header. When the most significant 6 bits of the ToS field are fully decoded, the resultant of the 64 possibilities is compared with the corresponding bits in the DSCP register to determine priority.

10.4.4 Spanning Tree Support

To support spanning tree, port 3 is designated as the processor port. The other ports (port 1 and port 2) can be configured in one of the five spanning tree states via "transmit enable", "receive enable" and "learning disable" register settings. The following table shows the port setting and software actions taken for each of the five spanning tree states.

Table 5. Spanning Tree States

Spanning Tree State	State Definition	Port Setting	Software Action
Disable	The port should not forward or receive any packets. Learning is disabled	Transmit enable = 0, Receive enable = 0, Learning disable =1	The processor should not send any packets to the port. The switch may still send specific packets to the processor (packets that match some entries in the “static MAC table” with “overriding bit” set) and the processor should discard those packets. Address learning is dis- abled on the port in this state.
Blocking	Only packets to the	Transmit enable = 0,	The processor should not send any packets to the

Spanning Tree State	State Definition	Port Setting	Software Action
	processor are forwarded. Learning is disabled.	Receive enable = 0, Learning disable =1	port(s) in this state. The processor should program the “Static MAC table” with the entries that it needs to receive (for example, BPDU packets). The “overriding” bit should also be set so that the switch will forward those specific packets to the processor. Address learning is disabled on the port in this state.
Listening	Only packets to and from the processor are forwarded. Learning is disabled.	Transmit enable = 0, Receive enable = 0, Learning disable =1	The processor should program the “Static MAC table” with the entries that it needs to receive (for example, BPDU packets). The “overriding” bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state. Address learning is disabled on the port in this state.
Learning	Only packets to and from the processor are forwarded. Learning is enabled.	Transmit enable = 0, Receive enable = 0, Learning disable = 0	The processor should program the “Static MAC table” with the entries that it needs to receive (for example, BPDU packets). The “overriding” bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state. See “Tail Tagging Mode” for details. Address learning is enabled on the port in this state.
Forwarding	Packets are forwarded and received normally. Learning is enabled.	Transmit enable = 0, Receive enable = 1, Learning disable =1	The processor programs the “Static MAC table” with the entries that it needs to receive (for example, BPDU packets). The “overriding” bit is set so that the switch forwards those specific packets to the processor. The processor can send packets to the port(s) in this state. See “Tail Tagging Mode” for details. Address learning is enabled on the port in this state.

10.4.5 Rapid Spanning Tree Support

There are three operational states assigned to each port for rapid spanning tree support:

- Discarding
- Learning
- Forwarding

Discarding States

Discarding ports do not participate in the active topology and do not learn MAC addresses. The Discarding state includes three states of the disable, blocking and listening of the spanning tree protocol.

The port settings for the Discarding state are:

- Transmit enable = 0
- Receive enable = 0
- Learning disable = 1

Software action: the processor should not send any packets to the port. The switch may still send specific packets to the processor (packets that match some entries in the static table with "overriding bit" set) and the processor should discard those packets.

Note: the processor is connected to port 3 via the MII interface. Address learning is disabled on the port in this state.

Learning States

Ports in learning states learn MAC addresses, but do not forward user traffic. In the Learning state, only packets to and from the processor are forwarded. Learning is enabled.

The port settings for the Discarding state are:

- Transmit enable = 0
- Receive enable = 0
- Learning disable = 0

Software action: The processor should program the static MAC table with the entries that it needs to receive (e.g., BPDU packets). The "overriding" bit should be set so that the switch will for- ward those specific packets to the processor. The processor may send packets to the port(s) in this state. See Section 9.4.6 “Tail Tagging Mode” for details. Address learning is enabled on the port in this state.

Forwarding States

Ports in the Forwarding states fully participate in both data for- warding and MAC learning. In the Forwarding state, packets are forwarded and received normally. Learning is enabled.

The port settings for the Discarding state are:

- Transmit enable = 1
- Receive enable = 1
- Learning disable = 0

Software action: The processor should program the static MAC table with the entries that it needs to receive (e.g., BPDU packets). The "overriding" bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state, see "Tail Tagging Mode" section for details. Address learning is enabled on the port in this state.

10.4.6 Tail Tagging Mode

The Tail Tag is only seen and used by the port 3 interface, which should be connected to an Enhanced DMA controller. It is an effective way to retrieve the ingress port information for spanning tree protocol IGMP snooping and other applications. The Bit 1 and bit 0 in the one byte tail tagging is used to indicate the source/destination port in port 3. Bit 3 and bit 2 are used for the priority setting of the ingress frame in port 3. Other bits are not used. This format is shown in Figure 11.

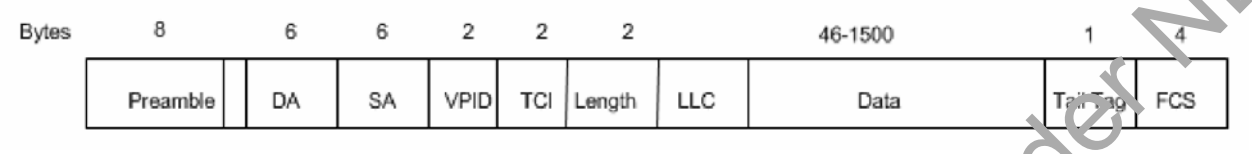


Figure 11. Tail Tag Frame Format

10.4.7 IGMP Support

For Internet Group Management Protocol (IGMP) support in layer 2, the KSZ8342 provides two components:

- IGMP Snooping
- Multicast Address Insertion in the Static MAC Table

IGMP Snooping

The KSZ8342 traps IGMP packets and forwards them only to the processor (port 3). The IGMP packets are identified as IP packets (either Ethernet IP packets, or IEEE 802.3 SNAP IP packets) with IP version = 0x4 and protocol version number = 0x2.

Multicast Address Insertion in the Static MAC Table

Once the multicast address is programmed in the Static MAC Table, the multicast session is trimmed to the subscribed ports, instead of broadcasting to all ports.

10.4.8 Port Mirroring Support

The KSZ8342 VoIP solution supports three modes of Port Mirroring:

- Receive Only
- Transmit Only
- Transmit and Receive

Receive Only

In receive only mode, all the packets received on the port are mirrored on the sniffer port. For example, port 1 is programmed to be "receive sniff" and port 3 is programmed to be the "sniffer port". A packet received on port 1 is destined to port 2 after the internal lookup. The KSZ8342 forwards the packet to both port 2 and port 3. The KSZ8342 can optionally even forward "bad" received packets to the "sniffer port".

Transmit only

In transmit only mode, all the packets transmitted on the port are mirrored on the sniffer port. For example, port 1 is programmed to be "transmit sniff" and port 3 is programmed to be the "sniffer port". A packet received on port 2 is destined to port 1 after the internal lookup. The KSZ8342 forwards the packet to both port 1 and port 3.

Transmit and Receive

In transmit and receive mode, all the packets received on port A and transmitted on port B are mirrored on the sniffer port. For example, port 1 is programmed to be "receive sniff", port 2 is programmed to be "transmit sniff", and port 3 is programmed to be the "sniffer port". A packet received on port 1 is destined to port 2 after the internal lookup. The KSZ8342 forwards the packet to both port 2 and port 3. Multiple ports can be selected as "receive sniff" or "transmit sniff". In addition, any port can be selected as the "sniffer port".

10.4.9 Rate Limiting Support

The KSZ8342 provides a fine resolution hardware rate limiting from 64Kbps to 99Mbps. The rate step is 64Kbps when the rate range is from 64Kbps to 960Kbps and 1Mbps for 1Mbps to 100Mbps (100BT) or to 10Mbps (10BT), depending on the negotiated data transfer rate (refer to Data Rate Limit Table). The rate limits on the "receive side" and on the "transmit side" (on a per port basis) are set independently.

For 10BASE-T, a rate setting above 10 Mbps means the rate is not limited. The size of each frame has options to include minimum IFG (Inter Frame Gap) or Preamble byte, in addition to the data field (from packet DA to FCS).

For ingress rate limiting, KSZ8342 provides options to selectively choose frames from all types; multicast, broadcast, and flooded unicast frames. The KSZ8342 counts the data rate from those selected type of frames. Packets are dropped at the ingress port when the data rate exceeds the specified rate limit.

For egress rate limiting, the “Leaky Bucket” algorithm is applied to each output priority queue for shaping output traffic. Inter frame gap is stretched on a per frame base to generate smooth, non-burst egress traffic. The throughput of each output priority queue is limited by the egress rate specified.

If any egress queue receives more traffic than the specified egress rate throughput, packets may be accumulated in the output queue and packet memory. After the memory of the queue or the port is used up, packet dropping or flow control will be triggered. As a result of congestion, the actual egress rate may be dominated by flow control/dropping at the ingress end, and may be therefore slightly less than the specified egress rate.

To reduce congestion, it is a good practice to make sure the egress bandwidth exceeds the ingress bandwidth.

10.4.10 Unicast MAC Address Filtering

The unicast MAC address filtering function works in conjunction with the static MAC address table. First, the static MAC address table is used to assign a dedicated MAC address to a specific port. If a Unicast MAC address is not recorded in the static table, it is also not learned in the dynamic MAC table. The KSZ8342 is then configured with the option to either filter or forward unicast packets for an unknown MAC address.

This function is useful in preventing the Broadcast of Unicast packets that could degrade the quality of the port in Internet VoIP applications.

10.4.11 Loopback Support

The KSZ8342 provides loopback support for remote diagnostic of failure. In loopback mode, the speed at both PHY ports needs to be set to 100BASE-TX. Two types of loopback are supported:

- Far-end Loopback
- Near-end (Remote) Loopback

Far-end Loopback

Far-end loopback is conducted between the KSZ8342's two PHY ports. Loopback path usage should be limited to a few packets at a time. The path should be used only for diagnostic purposes and cannot support large traffic.

The loopback path starts at the originating PHY port's receive inputs, wraps around at the "loopback" PHY port's PMD/PMA and ends at the originating PHY port's transmit outputs. The far-end loopback path is illustrated in Figure 12.

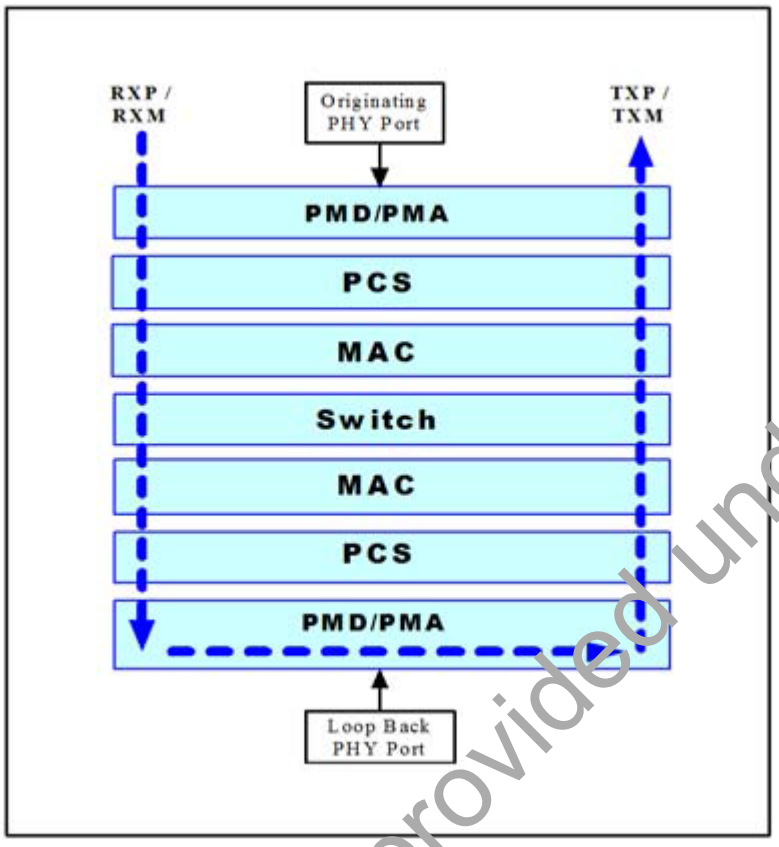


Figure 12. Far-End Loopback Path

Near-end (Remote) Loopback

Near-end (Remote) loopback is conducted at either PHY port 1 or PHY port 2 of the KSZ8342. The loopback path starts at the PHY port's receive inputs, wraps around at the same PHY port's PMD/PMA, and ends at the PHY port's transmit outputs.

The near-end loopback paths are illustrated in Figure 13.

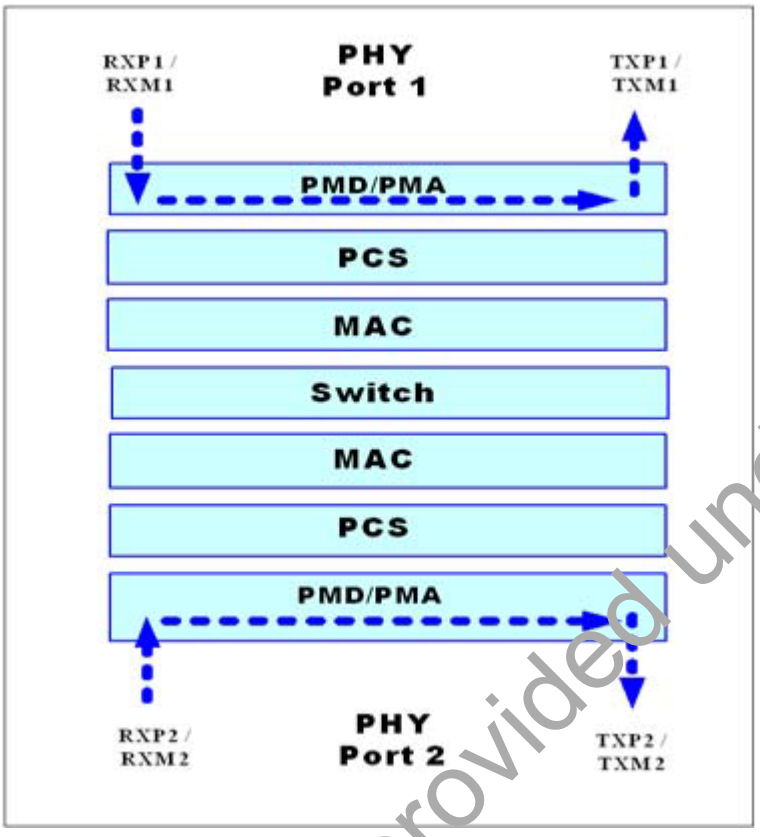


Figure 13. Near-End Loopback Path

10.4.12 Static MAC Address Table

The KSZ8342 supports both a static and a dynamic MAC address table. In response to a Destination Address (DA) look up, the KSZ8342 searches both tables to make a packet forwarding decision. In response to a Source Address (SA) look up, only the dynamic table is searched for aging, migration and learning purposes.

The static DA look up result takes precedence over the dynamic DA look up result. If there is a DA match in both tables, the result from the static table is used. The entries in the static table will not be aged out by the KSZ8342.

The static table is accessed by an external processor via the SPI interface. The external processor performs all addition, modification and deletion of static MAC table entries.

Table 6. Static MAC Address Table Bit Assignment

Bit(s)	Name	R/W	Description	Default
57:54	FID	R/W	Filter VLAN ID. Identifies on the 16 active VLAN's	0x0
53	Use FID	R/W	1: Use (FID+MAC) for static table look ups 0: Use MAC only for static table look ups	0
52	Override	R/W	1: Override port setting "transmit enable=0" or "receive enable=0" setting 0: No override	0
51	Valid	R/W	1: This entry is valid, the lookup result will be used 0: This entry is not valid	0
50:48	Forwarding Ports	R/W	These 3 bits control the forwarding port(s): 001: Forward to port 1 010: Forward to port 2 100: Forward to port 3 011: Forward to port 1 and port 2 110: Forward to port 2 and port 3 101: Forward to port 1 and port 3 111: Broadcasting (excluding the ingress port)	000
47:0	MAC Address	R/W	48-bit MAC Address	0x0000_0000_0000

Table 7. Static VLAN Table Bit Assignment

Bit(s)	Name	R/W	Description	Default
19	Valid	R/W	1: Entry is valid 0: Entry is invalid	1
18:16	Membership	R/W	Specify which ports are members of the VLAN. If a DA lookup fails (no match in both static and dynamic tables), the packet associated with this VLAN will be forwarded to ports specified in this field. For example, 101 means port 3 and 1 are in this VLAN.	111
15:12	FID	R/W	Filter ID. KSZ8342 supports 16 active VLANs represented by these four bit fields. FID is the mapped ID. If 802.1Q VLAN is enabled, the look up will be based on FID+DA and FID+SA.	0x0
11:0	VID	R/W	IEEE 802.1Q 12 bits VLAN ID	0x001

10.4.13 VLAN Table

The KSZ8342 uses the VLAN table to perform look ups. If 802.1Q VLAN mode is enabled, this table is used to retrieve the VLAN information that is associated with the ingress packet. This information includes FID (filter ID), VID (VLAN ID), and VLAN membership as described in Table 7.

If 802.1Q VLAN mode is enabled, the KSZ8342 will assign a VID to every ingress packet. If the packet is untagged or tagged with a null VID, the packet is assigned with the default port VID of the ingress port. If the packet is tagged with non-null VID, the VID in the tag will be used.

The look up process starts from the VLAN table look up. If the VID is not valid, the packet is dropped and no address learning takes place. If the VID is valid, the FID is retrieved. The FID+DA and FID+SA lookups are performed. The FID+DA look up determines the forwarding ports. If FID+DA fails, the packet will be broadcast to all the members (excluding the ingress port) of the VLAN. If FID+SA fails, the FID+SA will be learned.

10.4.14 Dynamic MAC Address Table

The KSZ8342 maintains the dynamic MAC address table. Read access is allowed only. The bit assignments for the dynamic VLAN address table are shown in Table 8.

Table 8. Dynamic VLAN Table Bit Assignment

Bit(s)	Name	R/W	Description	Default
71	Data Not Ready	RO	1: Entry is not ready. Continue retry until this bit samples as 0. 0: Entry is ready	1
70:67	Reserved	RO	Reserved	
66	MAC Empty	RO	1: there is no valid entry in the table 0: there are valid entries in the table	1
65:56	No of Valid Entries	RO	Indicates how many valid entries in the table 0x3FF: 1024 entries 0x3FE: 1023 entries 0x3FD: 1022 entries ..... 0x002: 3 entries 0x001: 2 entries 0x000 and bit 66 = 0: 1 entry 0x000 and bit 66 = 1: 0 entries	0x00_0000_0000

Bit(s)	Name	R/W	Description	Default
55:54	Time Stamp	RO	2 bits counter for internal aging.	
53:52	Source Port	RO	The source port where FID+MAC is learned . 00: port 1 01: port 2 10: port 3	00
51:48	FID	RO	Filter ID	0x0
47:0	MAC Address	RO	48-bit MAC Address	0x0000_0000_0000

10.4.15 MIB (Management Information Base) Counters

The KSZ8342 provides 32 MIB counters per port. These counters are used to monitor the port activity for network management. The MIB counters have two format groups: "Per Port" and "All Port Dropped Packet."

Per-Port MIB Counters

Per-port MIB counters are read using indirect memory accesses. The base address offsets and address ranges for all three ports are:

Port 1, base is 0x00 and range is (0x00-0x1F)

Port 2, base is 0x20 and range is (0x20-0x3F)

Port 3, base is 0x40 and range is (0x40-0x5F)

Port 1 MIB counters are read using the indirect memory offsets in Table 10.

All-Port Dropped Packet MIB Counters

Port 1 MIB counters are read using the indirect memory offsets in Table 11.

All Port Dropped Packet MIB counters are read using indirect memory access. The address offsets for these counters are shown in Table 12.

Additional MIB Counter Information

"Per Port" MIB counters are designed as "read clear." These counters are cleared after they are read.

"All Port Dropped Packet" MIB counters are not cleared after they are accessed and do not indicate overflow or validity; therefore, the application must keep track of overflow and valid conditions.

To read out all the counters, the best performance over the SPI bus is (160+3) * 8 * 200 = 260ms, where there are 160 registers, 3 overheads, 8 clocks per access, at 5MHz.

In the heaviest condition, the counters will overflow in 2 minutes. It is recommended that the software read all the counters at least every 30 seconds. A high performance SPI master is also recommended to prevent counter overflow.

Table 9. Format of Per-Port MIB Counters

Bit(s)	Name	R/W	Description	Default
31	Overflow	RO	1: Counter overflow. 0: No counter overflow	0
30	Count valid	RO	1: counter value is valid 0: counter value is not valid	0
29:0	Counter values	RO	Counter value	0

Table 10. Port 1 Per-Port MIB Counters Indirect Memory Offsets

Offset	Counter Name	Description
0x0	RxLoPriorityByte	Rx low-priority (default) octet count including bad packets.
0x1	RxHiPriorityByte	Rx hi-priority octet count including bad packets.
0x2	RxUndersizePkt	Rx undersize packets w/ good CRC.
0x3	RxFragments	Rx fragment packets w/ bad CRC, symbol errors or alignment errors.
0x4	RxOversize	Rx oversize packets w/ good CRC (max: 1536 or 1522 bytes).
0x5	RxJabbers	Rx packets longer than 1522 bytes w/ either CRC errors, alignment errors, or symbol errors (depends on max packet size setting).
0x6	RxSymbolError	Rx packets w/ invalid data symbol and legal packet size.
0x7	RxCRCError	Rx packets within (64 - 1522) bytes w/ an integral number of bytes and a bad CRC (upper limit depends on max packet size setting).
0x8	RxAlignmentError	Rx packets within (64 - 1522) bytes w/ a non-integral number of bytes and a bad CRC (upper limit depends on max packet size setting).
0x9	RxControl8808Pkts	Number of MAC control frames received by a port with 88-08h in EtherType field.

0xA	RxPausePkts	Number of PAUSE frames received by a port. PAUSE frame is qualified with EtherType (88-08h), DA, control opcode (00-01), data length (64B min), and a valid CRC.
0xB	RxBroadcast	Rx good broadcast packets (not including error broadcast packets or valid multicast packets).
0xC	RxMulticast	Rx good multicast packets (not including MAC control frames, error multicast packets or valid broadcast packets).
0xD	RxUnicast	Rx good unicast packets.
0xE	Rx64Octets	Total Rx packets (bad packets included) that were 64 octets in length.
0xF	Rx65to127Octets	Total Rx packets (bad packets included) that are between 65 and 127 octets in length.
0x10	Rx128to255Octets	Total Rx packets (bad packets included) that are between 128 and 255 octets in length.
0x11	Rx256to511Octets	Total Rx packets (bad packets included) that are between 256 and 511 octets in length.
0x12	Rx512to1023Octets	Total Rx packets (bad packets included) that are between 512 and 1023 octets in length.
0x13	Rx1024to1522Octets	Total Rx packets (bad packets included) that are between 1024 and 1522 octets in length (upper limit depends on max packet size setting).
0x14	TxLoPriorityByte	Tx lo-priority good octet count, including PAUSE packets.
0x15	TxHiPriorityByte	Tx hi-priority good octet count, including PAUSE packets.
0x16	TxLateCollision	The number of times a collision is detected later than 512 bit-times into the Tx of a packet.
0x17	TxPausePkts	Number of PAUSE frames transmitted by a port.
0x18	TxBroadcastPkts	Tx good broadcast packets (not including error broadcast or valid multicast packets).
0x19	TxMulticastPkts	Tx good multicast packets (not including error multicast packets or valid broadcast packets).
0x1A	TxUnicastPkts	Tx good unicast packets.
0x1B	TxDeferred	Tx packets by a port for which the 1st Tx attempt is delayed due to the busy medium.
0x1C	TxTotalCollision	Tx total collision, half duplex only.
0x1D	TxExcessiveCollision	A count of frames for which Tx fails due to excessive collisions.
0x1E	TxSingleCollision	Successfully Tx frames on a port for which Tx is inhibited by exactly one collision.
0x1F	TxMultipleCollision	Successfully Tx frames on a port for which Tx is inhibited by more than one collision.

Table 11. Format of "All-Port Dropped Packet" MIB Counter

Bit(s)	Name	R/W	Description	Default
31:16	Reserved	N/A	Reserved	N/A
15:0	Counter Value	RO	Counter value	0

Table 12. "All Port Dropped Packet" MIB Counters Indirect Memory Offsets

Offset	Counter Name	Description
0x100	Port 1 Tx Dropped Packets	Tx packets dropped due to lack of resources.
0x101	Port2 Tx Dropped Packets	Tx packets dropped due to lack of resources.
0x102	Port3 Tx Dropped Packets	Tx packets dropped due to lack of resources.
0x103	Port1 Rx Dropped Packets	Rx packets dropped due to lack of resources.
0x104	Port2 Rx Dropped Packets	Rx packets dropped due to lack of resources.
0x105	Port3 Rx Dropped Packets	Rx packets dropped due to lack of resources.

11 Ethernet DMA Controller

The KSZ8342 contains an Ethernet DMA controller that manages the communication between the MIPS CPU and the 3-port switch. The data transfer parameters, such as size of packet and starting address, are programmed into the Ethernet DMA controller by the MIPS CPU. The DMA controller then begins fetching the requested data and transmitting it to the 3-port switch for transfer into the external Ethernet ports. This concept is shown in Figure 14.

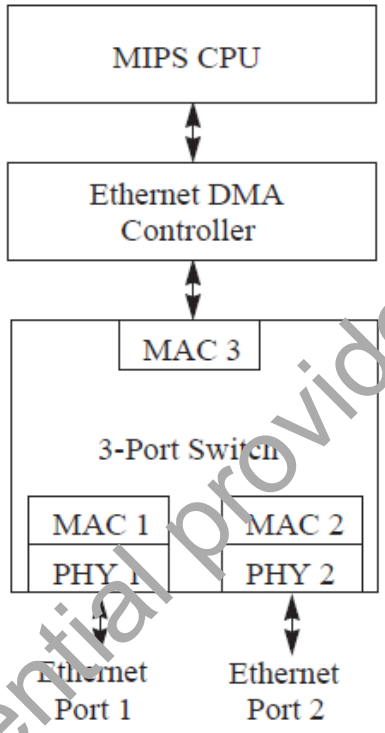


Figure 14. Ethernet DMA Controller Connections

The KSZ8342 and the driver communicate through the two data structures: System Configuration registers (SCRs) and Descriptor Lists and Data Buffers. This section describes the descriptors used to manage the flow of data between the Ethernet DMA controller and the 3-port switch. The KSZ8342 contains four transmit descriptors and four receive descriptors.

11.1 Descriptor Lists and Data Buffers

The KSZ8342 transfers received data frames to the receive buffer in host memory and transmits data from the transmit buffers in host memory. Descriptors that reside in the host memory act as pointers to these buffers.

There are two descriptor lists, one for receive and one for transmit for Ethernet MAC DMA. The base address of each list for Ethernet MAC DMA is written on ETDLB, and ERDLB, respectively. A descriptor list is forward-linked. The last descriptor may point back to the first entry to create a ring structure. Descriptors are chained by setting the next address to next buffer in both the receive and transmit descriptors.

The descriptor lists reside in the host physical memory address space. Each pointer points to one buffer and the second pointer points to the next descriptor. This enables the greatest flexibility for the host to chain any data buffers with discontinuous memory location. This eliminates processor-intensive tasks such as memory copying from the host to memory.

A data buffer contains of either an entire frame or part of a frame, but it cannot exceed a single frame. Buffers contain only data; buffer status is maintained in the descriptor. Data chaining refers to frames that span multiple data buffers. Data chaining can be enabled or disabled. Data buffers reside in host physical memory space.

The descriptor structures for Ethernet MAC DMA is collectively referred to as RDES0-3, and TDES0-3 for receive and transmit.

11.2 Receive Descriptors (RDES0-RDES3)

There are four receive descriptors, defined as RDES0 through RDES3. Receive descriptors and buffers addresses must be word aligned. Each receive descriptor provides one frame buffer, one byte count field, as well as control and status bits.

The following table shows the RDES0 descriptor bit fields.

Table 13. RDES0 Receive Descriptor Fields

Bit Field	Description
31	OWN Bit. When set, indicates that the descriptor is owned by the KSZ8342. When reset, indicates that the descriptor is owned by the host. The KSZ8342 clears this bit either when it completes the frame reception or when the buffers that are associated with this descriptor are full.

Bit Field	Description
30	FS First Descriptor. When set, indicates that this descriptor contains the first buffer of a frame. If the buffer size of the first buffer is 0, the next buffer contains the beginning of the frame.
29	LS Last Descriptor. When set, indicates that the buffer pointed by this descriptor is the last buffer of the frame.
28	IPE IP Checksum Error. When set, indicates that the received frame is an IP packet and its IP checksum field does not match. This bit is valid only when last descriptor is set.
27	TCPE TCP Checksum Error. When set, indicates that the received frame is a TCP/IP packet and its TCP checksum field does not match. This bit is valid only when last descriptor is set.
26	UDPE UDP Checksum Error. When set, indicates that the received frame is an UDP/IP packet and its UDP checksum field does not match. This bit is valid only when last descriptor is set.
25	ES Error Summary. Indicates the logical OR of the following RDES0 bits: CRC error, Frame too long, Runt frame. This bit is valid only when last descriptor is set.
24	MF Multicast Frame. When set, indicates that this frame has a Multicast address. This bit is valid only when last descriptor is set.
23:20	Reserved
19	RE Report on MII error. When set, indicates that a receive error in the physical layer was reported during the frame reception.
18	TL Frame Too Long. When set, indicates that the frame length exceeds the maximum size of 2000 bytes. This bit is valid only when last descriptor is set. Note: Frame Too Long is only a frame length indication and does not cause any frame truncation.
17	RF Runt Frame. When set, indicates that this frame was damaged by a collision or premature termination before the collision window has passed. Runt frames are passed on the host only if the pass bad-frames bit is set.
16	CE CRC Error. Wen set, indicates that a CRC error occurred on the received frame. This bit is valid only when last descriptor is set.

Bit Field	Description
15	FT Frame Type. When set, indicates that the frame is an Ethernet- type frame (frame length field is greater than 1500 bytes). When clear, indicates that the frame is an IEEE 802.3 frame. This bit is not valid for runt frames. This bit is valid only when last descriptor is set.
14:11	Reserved
10:0	FL Frame Length. Indicates the length, in bytes, of the received frame, including the CRC. This field is valid only when last descriptor is set and descriptor error is reset

Table 14. RDES1 Receive Descriptor Fields

Bit Field	Description
31:26	Reserved
25	RER Receive End of Ring. When set, indicates that the descriptor list reached its final descriptor. The KSZ8342 returns to the base address of the list, thus creating a descriptor ring.
24:12	Reserved
10:0	RBS Receive Buffer Size. Indicates the size, in bytes, of the receive data buffer. If the field is 0, the KSZ8342 ignores this buffer and moves to the next descriptor. The buffer size must be a multiple of 4.

Table 15. RDES2 Receive Descriptor Fields

Bit Field	Description
31:0	Buffer address. Indicates the physical memory address of the buffer. The buffer address must be word aligned.

Table 16. RDES3 Receive Descriptor Fields

Bit Field	Description
31:0	Next Descriptor Address. Indicates the physical memory address of the next descriptor in the descriptor ring. The buffer address must be word aligned.

11.3 Transmit Descriptors (TDES0-TDES3)

Transmit descriptors must be word aligned. Each descriptor provides one frame buffer, one byte count field, as well as control and status bits.

Table 17. TDES0 Receive Descriptor Fields

Bit Field	Description
31	OWN Bit. When set, indicates that the descriptor is owned by the KSZ8342. When cleared, indicates that the descriptor is owned by the host. The KSZ8342 clears this bit either when it completes the frame transmission or when the buffer allocated in the descriptor is empty. The ownership bit of the first descriptor of the frame should be set after all subsequent descriptors belonging to the same frame have been set. This avoids a possible race condition between the KSZ8342 fetching a descriptor and the driver setting an ownership bit.
30:0	Reserved

Table 18. TDES1 Receive Descriptor Fields

Bit Field	Description
31	IC Interrupt on Completion. When set, the KSZ8342 sets the transmit interrupt after the present frame has been transmitted. It is valid only when last segment is set.

Bit Field	Description
30	FS First Segment. When set, indicates that the buffer contains the first segment of a frame.
29	LS Last Segment. When set, indicates that the buffer contains the last segment of a frame.
28	IPCKG IP Checksum Generate. When set, the KSZ8342 generates the correct IP checksum for outgoing frames that contains IP protocol header. The KSZ8342 supports only standard IP header, i.e. IP with 20 byte header. When this feature is used, ADD CRC bit in the transmit mode register should always be set. This bit is used as a per-packet control when the IP checksum generate bit in the transmit mode register is not set. This bit should be always set for multiple-segment packets.
27	TCPCKG TCP Checksum Generate. When set, the KSZ8342 generates the correct TCP checksum for outgoing frames that contains IP and TCP protocol header. The KSZ8342 supports only standard IP header, i.e. IP with 20 byte header. When this feature is used, ADD CRC bit in the transmit mode register should always be set. This bit is used as a per-packet control when the TCP checksum generate bit in the transmit mode register is not set. This bit should be always set for multiple-segment packets.
26	UDPCKG UDP Checksum Generate. When set, the KSZ8342 generates the correct UDP checksum for outgoing frames that contains IP and UDP protocol header. The KSZ8342 supports only standard IP header, i.e. IP with 20 byte header. When this feature is used, ADD CRC bit in the transmit mode register should always be set. This bit is used as a per-packet control when the UDP checksum generate bit in the transmit mode register is not set.

Bit Field	Description
25	TER Transmit End of Ring. When set, indicates that the descriptor pointer has reached its final descriptor. The KSZ8342 returns to the base address of the list, forming a descriptor ring.
24:11	Reserved
10:0	TBS Transmit Buffer Size. Indicates the size, in bytes, of the transmit data buffer. If this field is 0, the KSZ8342 ignores this buffer and moves to the next descriptor.

Table 19. TDES2 Receive Descriptor Fields

Bit Field	Description
31:0	Buffer address. Indicates the physical memory address of the buffer. There is no limitation on the transmit buffer address alignment.

Table 20. TDES3 Receive Descriptor Fields

Bit Field	Description
31:0	Next Descriptor Address. Indicates the physical memory address of the next descriptor in the descriptor ring. The buffer address must be word aligned.

12 Memory Interfaces

The KSZ8342Q supports two types of memory, SDRAM and Flash. Each of these interfaces is described in the following subsections.

12.1 SDRAM Interface

The KSZ8342Q memory controller supports single-data-rate (SDR) memory devices with 16-bit data widths and speeds up to 125 MHz. The controller also supports the DRAM self-refresh mode and can be placed into the power saving mode when not in use.

Table 21 shows the characteristics of the memory interface.

Table 21. Main Memory Parameters

Product	Package Size	Memory Interface	Frequency	Signaling
KSZ8342Q	128-pin	SDR	125 MHz	3.3V (LVCMOS)

12.2 Flash Interface

The KSZ8342Q Flash memory interface uses the SPI port to transmit Flash data to the device and has the following features.

- Supports direct and indirect accesses.
- Supports single and quad data transitions.
- Supports Mode 0 or Mode 3 operation.
- Supports direct (Flash space) access for performance consideration.
- Supports indirect (register space) access for flexibility consideration.
- Supports burst read access in direct mode that matches MIPS burst length (1, 2, 4, 16 bytes).
- Support 1~4 bytes read/write access in indirect mode.
- Single 50 MHz clock frequency for simpler design.

12.2.1 Indirect Accesses

Indirect read/write accesses used register space to transfer data to and from the Flash. One register is used to store the address and control information for the type of Flash access. Hardware uses this register to

address the Flash device. A second register is used to store write data going to the Flash device, or read data coming from the Flash device.

Indirect mode supports 1~4 bytes per read/write access and provides a flexible access mechanism that enables software to support instructions from different serial NOR vendors.

12.2.2 Direct Accesses

Direct read accesses use Flash memory space to access the Flash device. In this case, commands are driven directly onto the Flash interface. Direct mode supports burst access which match MIPS burst size (1, 2, 4, or 16 bytes). This mode typically provides better performance than indirect mode and contains two configurable read options

- Read data (single IO)
- Fast read quad output (quad IO)

12.2.3 SPI Frequency

In the KSZ8342Q architecture, the SPI clock is always a divide-by 4 of the CPU (or DRAM memory clock frequency). For example, if the frequency of the CPU is 100 MHz, the SPI frequency is 25 MHz and the cycle time is calculated as follows:

1 / 25 MHz - 2 ns = 40 ns - 2 ns = 38 ns

In another example, if the frequency of the CPU is 125 MHz, the SPI frequency is 31.25 MHz and the cycle time is calculated as follows:

1 / 31.25 MHz - 2 ns = 32 ns - 2 ns = 30 ns

As shown in the above examples, as the CPU frequency is increased, the SPI cycle time decreases.

12.2.4 Flash Configurations

The interface supports data widths of 1, 2, and 4 bits as described below.

1-bit Flash Interface

The 1-bit Flash data interface support a single dedicated input pin and a single dedicated output. This interface is shown in Figure 15.

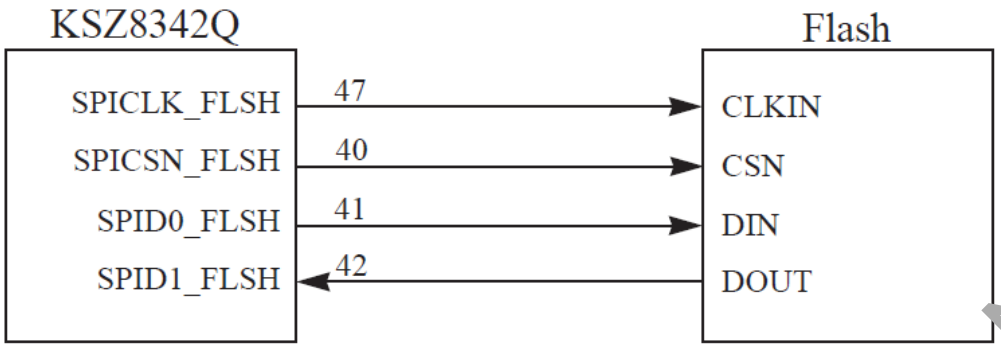


Figure 15. 1-bit SPI Data Interface

Figure 16 shows an example of a page write operation for a 1-bit SPI Flash. In this example, the address and write data are presented at the same time.

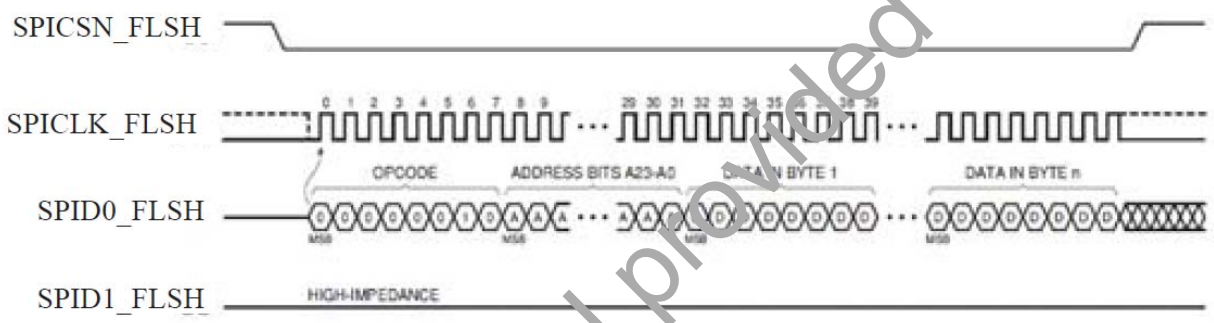


Figure 16. 1-bit SPI Flash Page Write

Figure 17 shows an example of a read operation for a 1-bit SPI Flash. In this example, the address is driven onto the bus first. The Flash device decodes the address and control information and drives the corresponding data onto the bus after the appropriate latency has been met.

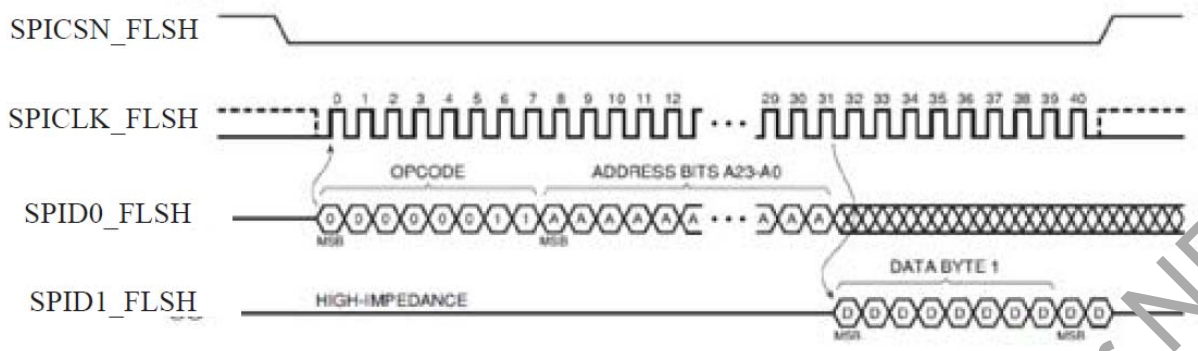


Figure 17. 1-bit SPI Flash Page Read

2-bit Flash Interface

The 2-bit Flash data interface supports two data inputs and one data output pin. In this configuration, there are two data pins (SPID0_FLSH/SPID1_FLSH) used to transfer read data from the Flash to the KSZ8342Q. Only one pin (SPID0_FLSH) is used to write data to the Flash. In this case, SPID0_FLSH is configured as a bidirectional pin. In output mode, data is written from the KSZ8342Q to the DIN pin of the Flash. In input mode, the KSZ8342Q reads data from the Flash on the SPID0_FLSH and SPID1_FLSH pins. This interface is shown in Figure 18.

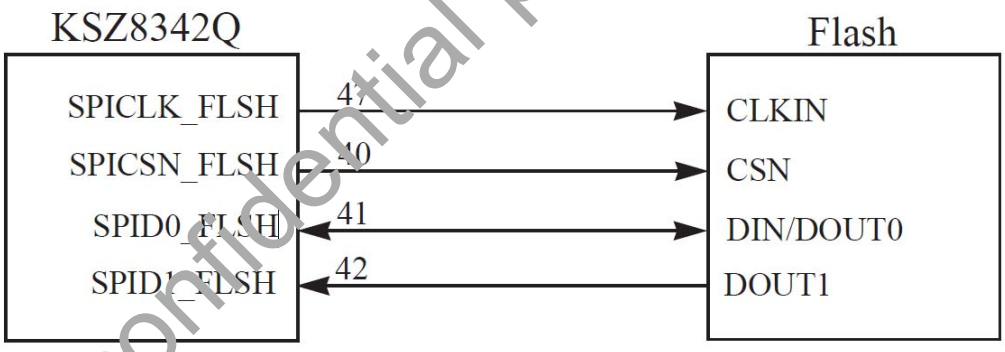


Figure 18. 2-bit SPI Data Interface

4-bit Flash Interface

The 4-bit Flash data interface supports four data inputs and one data output pin. In this configuration, there are four data pins (SPID0_FLSH/SPID1_FLSH/SPID2_FLSH/SPID3_FLSH) used to transfer read data from the Flash to the KSZ8342Q. Only one pin (SPID0_FLSH) is used to write data to the Flash. In this case, SPID0 is configured as a bidirectional pin. In output mode, data is written from the KSZ8342Q to the DIN pin

of the Flash. In input mode, the KSZ8342Q reads data from the Flash on the SPID0_FLSH - SPID3_FLSH pins. This interface is shown in Figure 19.

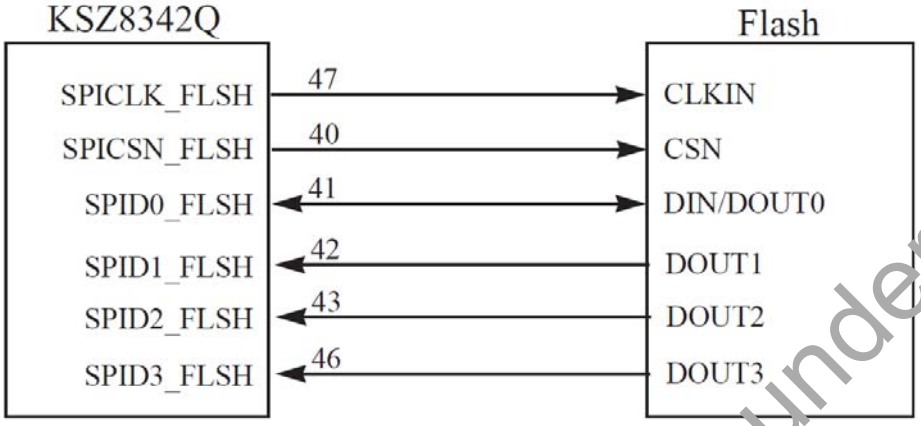


Figure 19. 4-bit SPI Data Interface

Figure 20 shows an example of a read operation for a 4-bit SPI Flash. In this example, the address is driven onto the bus first. The Flash device decodes the address and control information and drives the corresponding data onto the four data pins after the appropriate latency has been met.

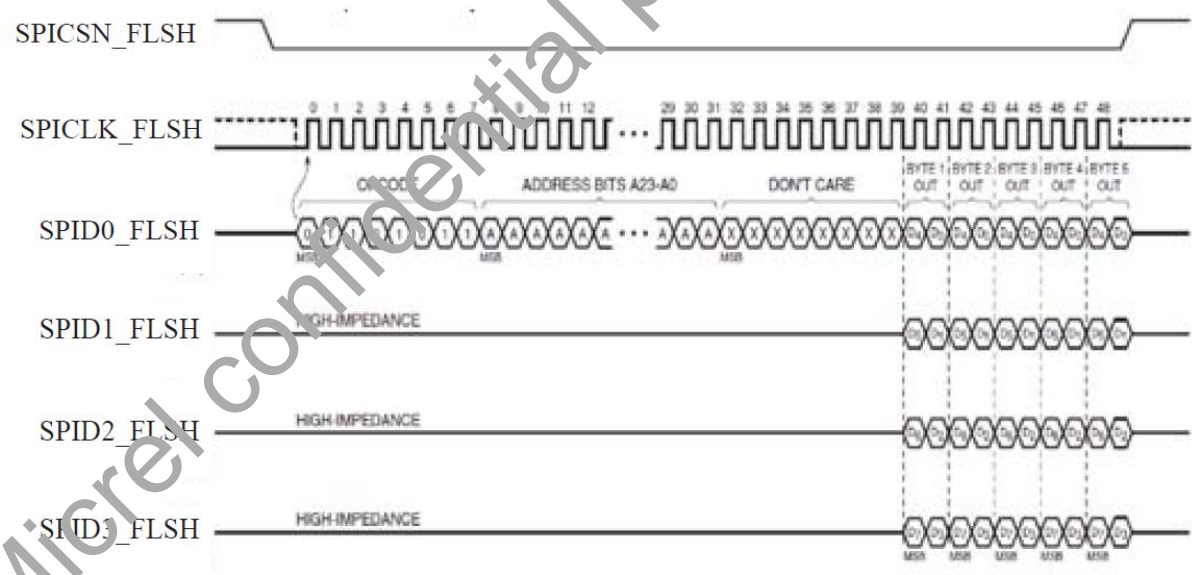


Figure 20. 4-bit SPI Flash Read

13 PCM Interface

The 2-channel PCM interface is controlled by the on-chip ZSP400 DSP and is used to transfer voice/data signals to and from the telephone. The PCM data interface can be configured for 8-, 16-, or 24-bit widths.

The programmable 8 or 16 kHz sampling rate supports both narrow band and wide band voice channels with 64 time slots. Other features of the PCM interface include.

- PCM Highway Interface
- Master/Slave modes support
- Programmable bit clock 512 KHz - 8.192 MHz
- 64 programmable time slots
- Frame sync start offset and stretch support

The KSZ8342Q uses a PCM port to communicate with analog devices. The interface support a single dedicated transmit pin and a single dedicated receive pin. The PCM interface is shown in Figure 21.

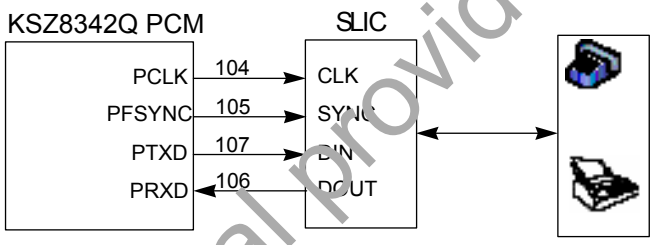


Figure 21. PCM Interface

14 SPI SLIC Interface

For the SLIC interface, please reference the KSZ8342Q reference design. Micrel has selected a SLIC device for this reference design. Users can select a different SLIC device conforming to the timing diagrams described in Section 22.

The KSZ8342Q interface uses a 1-bit SPI port to configure and debug the SLIC device connected to the external analog devices. The 1-bit data interface support a single dedicated input pin and a single dedicated output. This interface is shown in Figure 22.

Note that the SPI SLIC interface is used for initial register configuration and control of the SLIC device, and for debugging. This interface is not used during normal operation. Normal communication with the analog device is facilitated through the PCM interface described above.

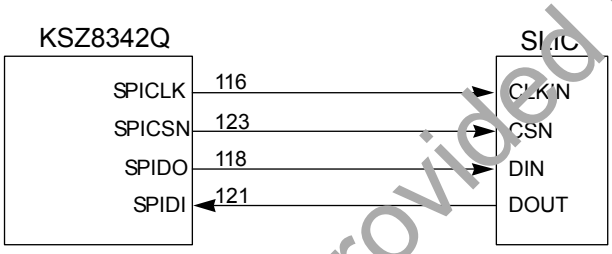


Figure 22. SPI SLIC Interface

15 UART

The KSZ8342 contains a single 2-wire UART port that supports duplex operation via dedicated transmit and receive pins. The UART interface operates at frequencies of 25 MHz, 62.5 MHz, 125 MHz, or 166 MHz. The frequency is selected using bits 6:5 of the *UART Modem Control* register at offset 0x2010. The UART port supports odd and even parity, where parity can also be disabled, as well as 1 or 2 stop bits, and character lengths of 5, 6, 7, or 8 bits.

The UART Line Control register at offset 0x200C specifies the asynchronous data frame for transmitting and receiving as shown in Figure 23 below.

As shown in this figure, the first high-to-low transition is detected as the *Start* bit. *Start* bit is low and *Stop* bit is high. Due to the noise, a short glitch might happen on the bus. To avoid detecting the wrong *Start* bit, three samples at clock (Frclk) 7, 8, and 9 after high-to-low transition are taken on the bus. If at least two out of three samples are low, then a *Start* bit is detected. Otherwise, the high-to-low transition is treated as a glitch. The *Frclk* and *Fsample* timing parameters are defined by the *Baud Rate Divisor* register located at offset 0x201C.

The UART support both the industry-standard 16550 mode and the 16450 mode. When in 16550 mode, the internal transmit and receive FIFO's are enabled. When in 16450 mode, the internal transmit and receive FIFO's are disabled. The mode is controlled by bit 0 of the *UART FIFO Control* register located at offset 0x2008.

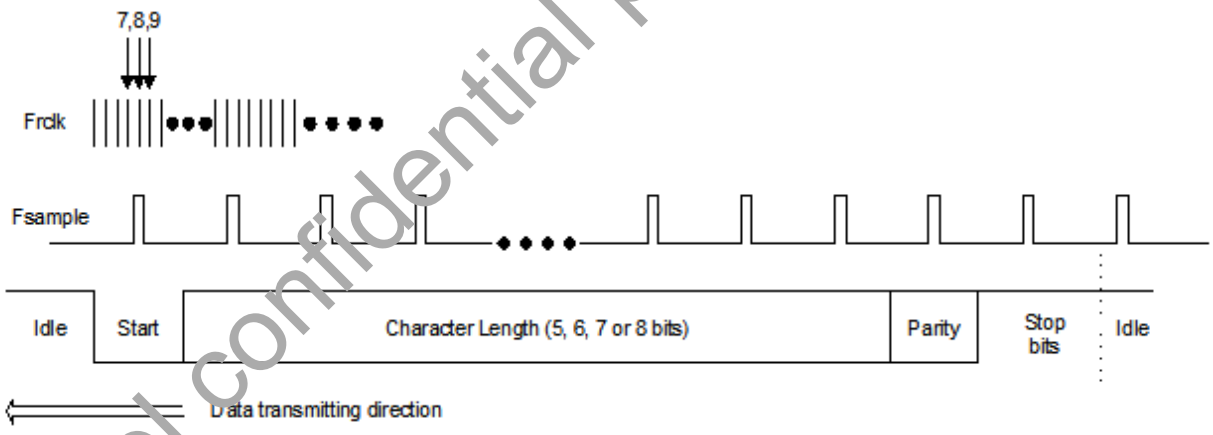


Figure 23. Basic UART Transfer Sequence

16 Interrupt Control

The interrupt control logic handles all interrupts coming from both internal and external sources. Some of these sources are as follows:

- MIPS CPU
- Keypad
- ZSP
- MAC
- CODEC
- UART
- Timer
- PCM
- Ethernet DMA controller
- Switch
- External

The priority of these interrupt sources can be configured via the register interface. As shown, interrupt requests can be generated by internal functional blocks as well as external pins. The KSZ8342 interrupt controller has an interrupt status bit for each interrupt source.

In general, the following registers are used to control interrupt generation and handling:

- *Interrupt Priority Registers*: the index number of each interrupt source is written to the pre-defined interrupt priority register field to obtain the priority. The interrupt priorities are predefined from 0 to 15.
- *Interrupt Status Register*: indicates the interrupt status.
- *Interrupt Enable Register*: enables the interrupts.

17 GPIO

The number of dedicated and shared GPIO pins in the KSZ8342 depends on the package type as shown in Table 22 below. Each I/O pin can be configured as Input or Output. As shown above, some of the I/O pins are shared with the external interrupts and timer output.

Table 22. KSZ8342 GPIO Options

Product	Shared GPIO
KSZ8342Q	14

18 Timers

The KSZ8342 has two 32-bit timers (Timer 0 and Timer 1). When the timer expires, it generates a pulse on the I/O pins. Through the register interface, the host can control the time-out period as well as the pulse duration. The output signals are TOUT0 and TOUT1, respectively. Both timers can be enabled or disabled to save power. Interrupts can be generated for each timer by setting the corresponding interrupt control registers.

A timer generates a one-shot pulse with a preset timer clock duration whenever a time-out occurs. The duration of the one-shot pulse is also programmable by the host. This pulse consequently generates a time-out interrupt that is directly observable at the timer's configured output pin. The timer frequency is calculated as follows:

fTOUT = fMCLK / (Timer data value + Pulse data value)

where the frequency of MCLK is 25MHz. When the timer is enabled, it loads a data value to its count register and begins decrementing the count register value. When the timer expires, the corresponding TOUT pin is asserted. Then it loads the pulse count value into the count register and starts decrementing.

When the pulse data count reaches zero, the associated interrupt is asserted (if enabled), the TOUT pin is de-asserted, and the timer data value is reloaded again for the next time-out. This process repeats until the timer is disabled.

19 Power Signals

The KSZ8342Q device requires the voltages shown in Table 23.

Table 23. KSZ8342 Power Signals

Power Signal Name	Device Pin	Requirement
VDDA33	9	3.3V analog VDD
VDDA12	14	1.2V VDDA (Internal LDO Output)
VDD_CORE	34, 66, 120	Digital Core 1.2V VDD
VDD_IO	45, 97	3.3V Digital I/O VDD
VDD_SDR	49, 64, 82	Memory I/O VDD = 3.3V (For SDRAM Memory Controller)
GNDA	8, 15, 19, 31	Analog GND
VSS_CORE	33, 52, 65, 119	Digital Core GND
VSS_IO	44, 96	Digital IO GND
VSS_SDR	48, 63, 81	Memory I/O GND. (For SDRAM Memory Controller)

20 Power Management

There are several features incorporated within the KSZ8342Q device which will assist in keeping power usage to a minimum.

20.1 PHY Power Management

The KSZ8342Q supports enhanced power management feature in low power state with energy detection to ensure low-power dissipation during device idle periods. There are three operating modes under the power management function

- Normal Operation Mode
- Energy Detect Mode
- Port Based Power Down Mode
- Energy Efficient Ethernet (EEE)

KSZ8342Q Functional Block State per Power Management Operating Mode indicates all internal function blocks status under four different power management operation modes.

20.1.1 Normal Operating Mode

This is the default setting bit[1:0] = 00 in Register 195 after the chip power-up or hardware reset. When the KSZ8342Q is in this mode, all PLL clocks are running. The PHY and MAC are on and the host interface is ready for a CPU read or write.

During the normal operation mode, the host CPU can set the bit[1:0] in Register 195 to transit the current normal operation mode to any one of the other three power management operation modes.

20.1.2 Energy Detect Mode

The energy detect mode provides a mechanism to save more power than in the normal operation mode when the KSZ8342Q is not connected to an active link partner.

This mode can result in a power savings of up to 50% relative to normal mode. If the cable is unplugged, the KSZ8342Q can automatically enter to a low power state (energy detect mode). In this mode the KSZ8342Q transmits 120ns width pulses at a 1 pulse/s rate. Once activity resumes due to plugging a cable or attempting by the far end to establish link, the KSZ8342Q can automatically power up to normal power state from the energy detect mode.

Energy detect mode consists of two states, normal power state and low power state. While in low power state, the KSZ8342Q reduces power consumption by disabling all circuitry except the energy detect circuitry of the receiver. The energy detect mode is entered by setting bit[1:0] = 01 in Register 195. When the KSZ8342Q is in this mode, it monitors the cable energy. If there is no energy on the cable for a time longer than the programmed value in bits [7:0] (Go-Sleep time) in Register 196, the KSZ8342Q will go into a low power state.

20.1.3 Port based Power Down Mode

The KSZ8342Q features a per-port power down mode. To save power, a PHY port that is not in use can be powered down via port control Register 29 or 45 bit [3], or MIIM PHY register. It will saves about 15 mA per port.

20.1.4 Power Saving Mode

The power saving mode is entered when auto-negotiation mode is enabled, the cable is disconnected, all PLL clocks are enabled, the MAC is on, all internal registers value cannot be changed, and the host interface is ready for CPU read or write. This mode mainly controls the PHY transceiver ON/OFF status based on line status to achieve power saving. The PHY remains transmitting and only turns off the unused receiver block. Once activity resumes due to plugging a cable or attempting by the far end to establish link, the KSZ8342Q transitions to the normal power state from power saving mode.

20.1.5 Port based Power Down Mode

The KSZ8342Q features a per-port power down mode. To save power, a PHY port that is not in use can be powered down via port control Register 29 or 45 bit [3], or MIIM PHY register. It will saves about 15 mA per port.

20.1.6 Energy Efficient Ethernet

Energy Efficient Ethernet (EEE) is implemented in the KSZ8342Q device as described in the IEEE 802.3AZ specification. EEE saves power by keeping the voltage on the Ethernet cable at approximately 0V for as often as possible during periods of no traffic activity. This is called Low Power mode or state (LPI). However, the link will respond automatically when traffic resumes and do so in such a way as to not cause blocking or dropping of any packets. The wake up time for 100BaseT is specified to be less than 20.5 µs.

The transmit and receive directions are independently controlled. Note the EEE is not specified or implemented for 10BaseT. In 10BaseT, the transmitter is already OFF during idle periods.

The main energy savings from EEE is done at the PHY level. However, the KSZ8342Q device reduces the power consumption not only in the PHY block but also in the MAC and switch blocks by shutting down any unused clocks as much as possible when the device is in the LPI state.

A comprehensive LPI request on/off policy is also built-in at the switch level to determine when to issue LPI requests and when to stop the LPI request. Some software control options are provided in the device to terminate the LPI request in the early phase when certain events occur to reduce the latency impact during LPI recovery. A configurable LPI recovery time register is provided at each port to specify the recovery time (25 us at default).

20.2 MIPS Processor

There are two main ways to reduce power consumption in the MIPS processor.

- WAIT instruction: Execution of the WAIT instruction puts the core into a low-power mode where many of the internal clocks are suspended. The processor will emerge from the suspended state when it senses an interrupt. Most of the core logic is stopped, but the Count register, in particular, continues to run.
- The $Status_{RP}$ bit: Setting this bit does not affect the core directly, but rather its state is made available at the core interface on the SI_RP pin. External logic is encouraged to use this signal to gate the master clock input to the core.

Refer to documentation on the MIPS processor for more information on power management.

Table 23. KSZ8342Q Functional Block State per Power Management Operating Mode

KSZ8342Q Functional Block	Power Management Operating Mode	
	Normal	**Energy Detect**
Internal PLL clocks	Enabled	Disabled
Transmit/Receive PHY	Enabled	Energy detect at Rx
MAC	Enabled	Disabled
MIPS Processor	Enabled	Disabled

21 Electrical Specifications

21.1 Absolute Maximum Ratings

Table 24. Absolute Maximum Ratings – Device

Parameter	Value
Supply voltage (VDDA12, VDD_CORE)	-0.3 – 2.4V
Supply voltage (VDDA33, VDD_IO, VDD_SDR)	-0.3 - 4.0V
Output voltage	-0.3 - 4.0V
Input voltage	-0.3 - 4.0V
Lead Temperature	270 °C
Ambient Temperature	0 - 70 °C
Junction Temperature	125 °C
Storage Temperature	-55 °C to 150 °C
Junction Thermal Resistance (LQFP Package)	30.28 C/W
HBM ESD Rating	2 KV

21.2 Operating Ratings

Table 25. Operating Ratings

Parameter	Value
VDDA33, VDD_IO, VDD_SDR	3.135V - 3.465V
VDDA12, VDD_CORE	1.14V - 1.26V

21.3 SDRAM Memory Interface

The KSZ8341 device conforms to the SDR standard for single data rate timing and electrical characteristics. As such, SDR timing and electrical specifications are not described in this document. Rather, Table 26 lists the SDR devices that have been tested and qualified by Micrel. The use of SDR memory devices other than those listed in this table may cause undesirable behavior of the memory interface.

Table 26. Supported SDR Memory Devices

Mfg.	Part Number	Size and Organization	
Micron	48LC16M16A2	256 Mb	16M x 16

21.4 Flash Memory Interface

The KSZ8342Q device conforms to the industry standard for Flash timing and electrical characteristics. As such, Flash timing and electrical specifications are not described in this document. Although the KSZ8342Q supports NOR Flash sizes as small as 4 Mb, Micrel recommends the use of Flash devices that are at least 32 Mb or larger. Some example SPI NOR Flash devices below are listed by size. All devices support 3V signaling and are housed in an 8-pin SOIC package.

Table 27. Supported Flash memory Modules

Manufacturer	Part Number	Size	Maximum Frequency
Micron	M25P32-VMW6TG	32 Mb	75 MHz
Microchip	SST25VF032B-80-4I-S2AF	32 Mb	80 MHz
Macronix	MX25L6445EM2I-10G	64 Mb	83.3 MHz

21.5 3-Port Switch Electrical Characteristics

Each PHY port's transformer consumes an additional 45mA @3.3V for 100BASE-TX and 70mA @ 3.3V for 10BASE-T at full traffic.

Table 28. 3-Port Switch Electrical Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
100BASE-TX Operation (All Ports @ 100% Utilization)						
I_{dd1}	100BASE-TX (transceiver + digital I/O)	VDDA33, VDD_IO = 3.3V		112		mA
10BASE-T Operation (All Ports @ 100% Utilization)						

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{dd2}	10BASE-T (transceiver + digital I/O)	VDDA33, VDD_IO = 3.3V		92		mA
Power Management Mode						
I_{dd3}	Power Saving Mode	Ethernet cable disconnected & Auto-Neg		89		mA
I_{dd4}	Soft Power Down Mode			6.2		mA
I_{dd5}	Energy Detect Mode	Unplug Port 1 and Port 2		42		mA
TTL Inputs (VDD_IO = 3.3V)						
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IN}	Input Current	V_{IN} = GND ~ VDD_IO	-10		10	µA
TTL Outputs (VDD_IO = 3.3V)						
V_{OH}	Output High Voltage	I_{OH} = -8mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8mA			0.4	V
$\|I_{OZ}\|$	Output Tri-State Leakage				10	µA

22 Timing Specifications

22.1 SPI Interface Timing

The following subsections describe the SPI timing characteristics for the Flash and SLIC interfaces.

22.1.1 SPI Write Timing

Figure 24 shows the timing diagram for the SPI SLIC and Flash interfaces during a write operation.

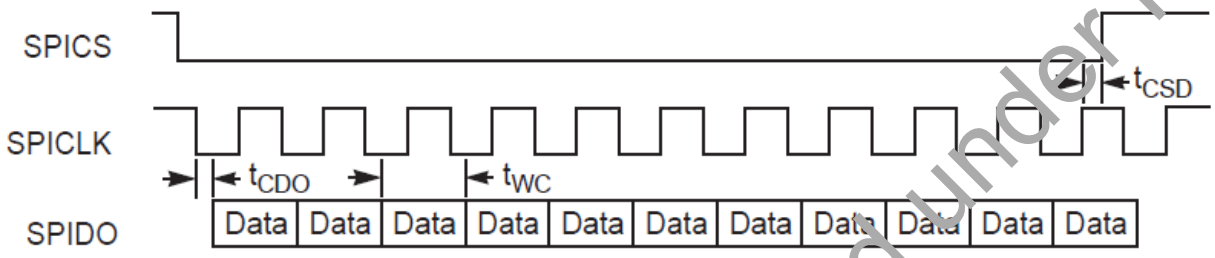


Figure 24. SPI Write Timing

Table 29 shows the AC timing characteristics for the SPI SLIC and Flash interfaces during a write operation. All times are in nanoseconds. Note that only the SPID0 bit is used during a write operation. The SPID1 through SPID3 signals are used only during read operations as described in the following subsection.

Table 29. SPI Flash and SLIC Write Timing

Timing	Description	SPI Flash	SPI SLIC
t_{CDO}	SPICLK falling edge to data out.	1 (max)	2 (max)
t_{CSD}	SPICLK rising edge to SPICS de-asserted.	12 (min)	16 (min)
t_{WC}	One write cycle	(1/freq) - 2	(1/freq) - 2

In the table above, the write cycle time described in the tWC parameter depends on the clock frequency. In the KSZ8342 architecture, the SPI clock is always a /4 of the CPU (or DRAM memory clock frequency). For example, if the frequency of the device is 100 MHz, the SPI frequency is 25 MHz and the cycle time is calculated as follows:

1 / 25 MHz - 2 ns = 40 ns - 2 ns = 38 ns

In another example, if the frequency of the CPU is 125 MHz, the SPI frequency is 31.25 MHz and the cycle time is calculated as follows:

1 / 31.25 MHz - 2 ns = 32 ns - 2 ns = 30 ns

As shown in the above examples, as the CPU frequency is increased, the SPI cycle time decreases.

22.1.2 SPI Read Timing

Figure 25 shows the timing diagram for the SPI SLIC and Flash interfaces during a read operation.

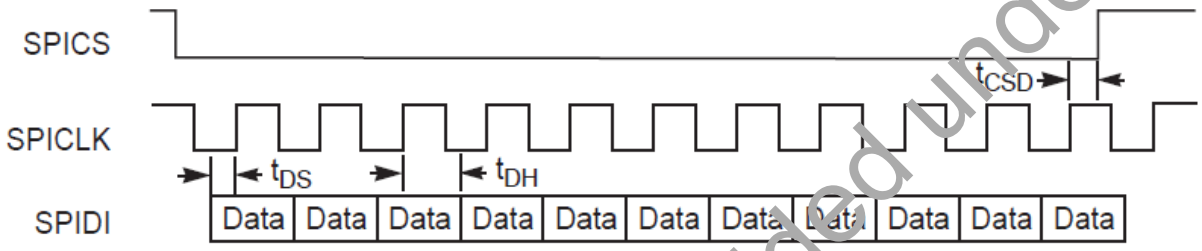


Figure 25. SPI Read Timing

Table 30 shows the AC timing characteristics for the SPI SLIC and Flash interfaces during a read operation. All times are in nanoseconds. Note that up to four read pins (SPID0 through SPID3) can be used during a read operation depending on the size of the memory device. The SPID0 signal is the only data pin used during a write operation as described in the previous subsection.

Table 30. SPI Flash and SLIC Read Timing

Timing	Description	SPI Flash	SPI SLIC
t_{DS}	Read data setup time	0.5 (min)	0.5 (min)
t_{DH}	Read data hold time	5 (min)	8 (min)
t_{CSD}	SPICLK rising edge to SPICS de-asserted.	12 (min)	16 (min)

22.2 Auto-Negotiation Timing

Figure 26 and Table 31 show the Auto-Negotiation timing for the KSZ8342Q device.

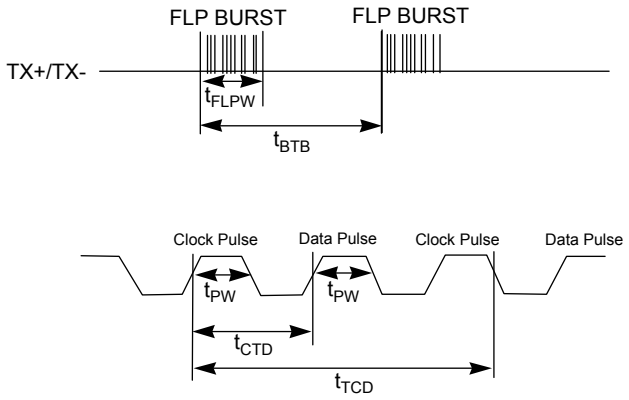


Figure 26. Auto-Negotiation Timing

Table 31. Auto-Negotiation Timing

Timing	Description	Min	Typ	Max	Unit
t_{BTB}	FLP burst to FLP burst	8	16	24	ms
t_{FLPW}	FLP burst width		2		ms
t_{PW}	Clock/Data pulse width		100		ns
t_{CTD}	Clock pulse to data pulse	55.5	64	69.5	µs
t_{TCD}	Clock pulse to clock pulse	111	128	139	µs
	Number of clock/data pulses per burst	17		33	

22.3 Reset Circuit Guidelines

Figure 27 illustrates the recommended reset circuit for powering up the KSZ8342Q device if reset is triggered by the power supply

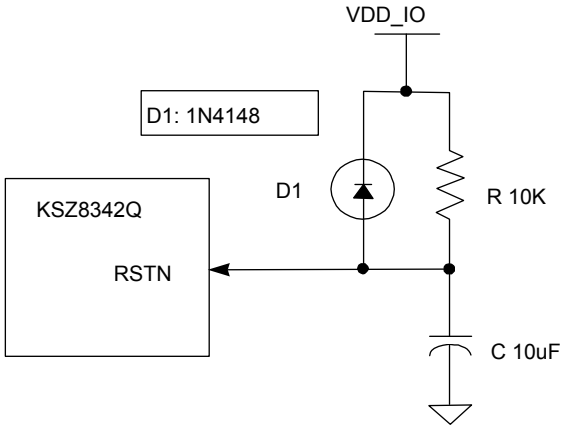


Figure 27. Simple Reset Circuit

Figure 28 illustrates the recommended reset circuit for applications where reset is driven by another device (e.g., CPU or FPGA). At power-on-reset, R, C and D1 provide the necessary ramp rise time to reset the KSZ8342Q device. The RST_OUT_N from CPU/FPGA provides the warm reset after power up.

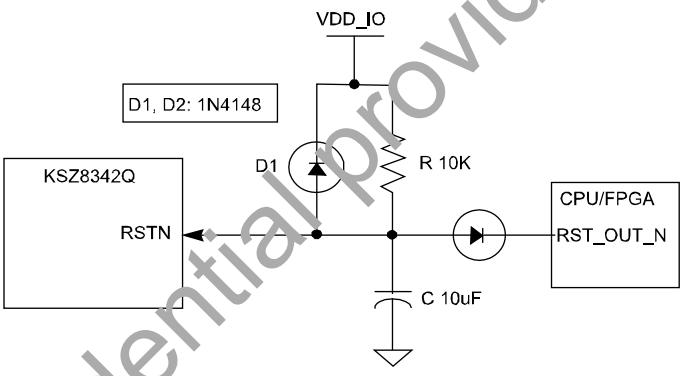


Figure 28. Reset Circuit with CPU/FPGA

22.4 Reset and Power Sequencing Timing

Figure 29 and Table 32 show the reset and power sequencing requirements for the KSZ8342Q device.

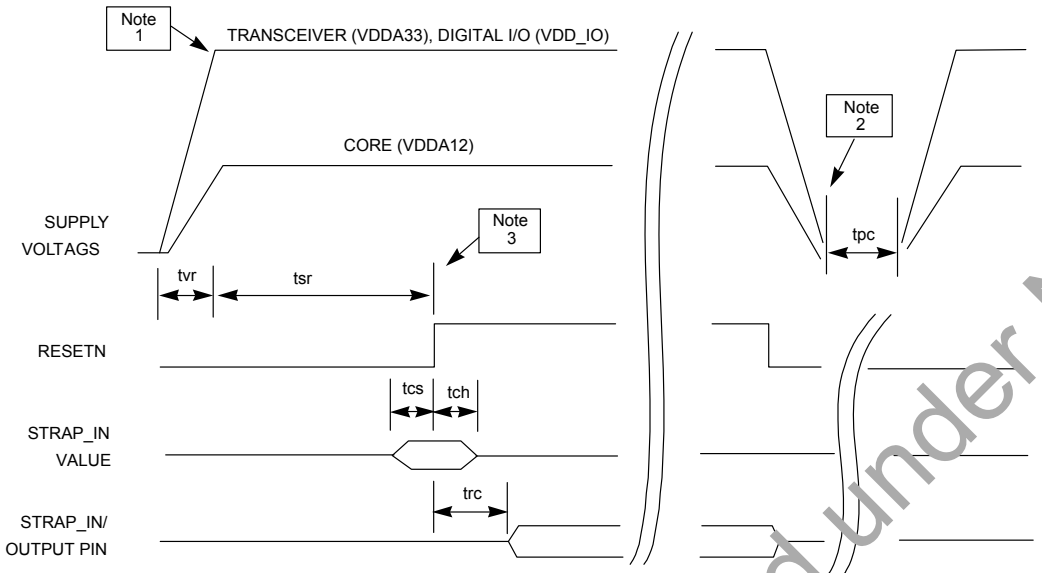


Figure 29. Reset and Power Sequence Timing

Table 32. Reset and Power Sequence Timing

Timing	Description	Min	Max	Unit
t_{SR}	Stable supply voltage to Reset high.	10		mS
t_{CS}	Configuration setup time	5		nS
t_{CH}	Configuration hold time	6		nS
t_{RC}	Reset to strap-in to drive output	6		nS

NOTE 1: The recommended powering sequence is to bring up all voltages at the same time. However, if that cannot be attained, then a recommended power-up sequence is to have the transceiver (VDD33) and digital I/Os (VDD_IO) voltages power up before the 1.2V core (VDD_CORE) voltage. If the 1.2V core must power-up first, the maximum lead time for the 1.2V core voltage with respect to the transceiver and digital I/O voltages should be 200µs. There is no power sequence requirement between transceiver (VDDA33) and digital I/Os

(VDD_IO) power rails. The power-up waveforms should be monotonic for all supply voltages to the KSZ8342Q.

NOTE 2: After the de-assertion of reset, it is recommended to wait a minimum of 100µs before starting programming of the device through any interface.

NOTE 3: The recommended power-down sequence is to have the 1.2V core voltage power down first before powering down the transceiver and digital I/O voltages.

22.5 Reference Clock

A crystal or external clock source, such as an oscillator, is used to provide the reference clock for the KSZ8342Q. The reference clock is 25 MHz for all operating modes of the KSZ8342Q.

Figure 30 shows the reference clock connection to XI and X2 pins of the KSZ8342Q using a crystal. Note that the value of the capacitors used with the crystal will **vary** depending on the specific crystal product used. A design should incorporate a footprint for a resistor to limit the current to the crystal and reduce EMI. Depending on the crystal used, this can be installed or not. If not installed, a zero Ohm resistor can be used.

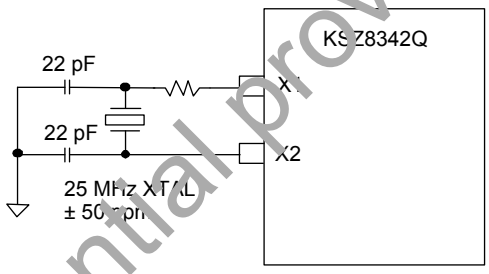


Figure 30. Crystal Clock Connection Using X1 and X2

Figure 31 shows the reference clock connection to XI pin of the KSZ8342Q using an oscillator.

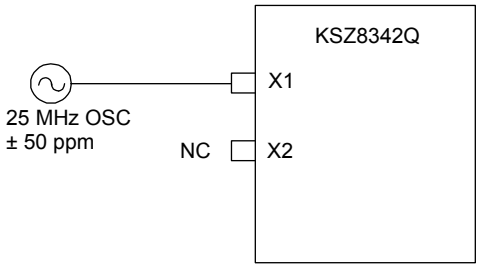


Figure 31. Oscillator Clock Connection Using X1

Table 33 shows reference crystal parameters.

Table 33. Typical Reference Crystal Characteristics

Characteristics	Value	Units
Frequency	25.0	MHz
Frequency tolerance (max)	±50	ppm
Load capacitance (max)	22	pF
Series resistance	40	Ω

22.6 Transformer Selection

A 1:1 isolation transformer is required at the line interface. An isolation transformer with integrated common-mode choke is recommended for exceeding FCC requirements. Table 34 shows the recommended transformer characteristics.

Table 34. Transformer Characteristics

Parameter	Value	Test Condition
Turns Ratio	1CT:1CT	
Open-Circuit Inductance (min)	350 μH	100 mV, 100 kHz, 8 mA
Leakage Inductance (max)	0.4 μH	1 MHz (min)
Inter-Winding Capacitance (max)	12 pF	
D.C Resistance (max)	0.9 Ω	
Insertion Loss (max)	-1.0 dB	100 kHz - 100 MHz
HIPOT (min)	1500 Vrms	

Table 35 shows a list of qualified single port magnetics. Note that all of the products listed are single-port and support auto MDI-X.

Table 35. Qualified Single-Port Magnetics

Magnetic Manufacturer	Part Number
Pulse	H1102
Pulse (low cost)	H1260
Transpower	HB726
Bel Fuse	S558-5999-U7
Delta	LF8505
LanKom	LF-H41S
TDK (Mag Jack	TLA-6T71[illegible]

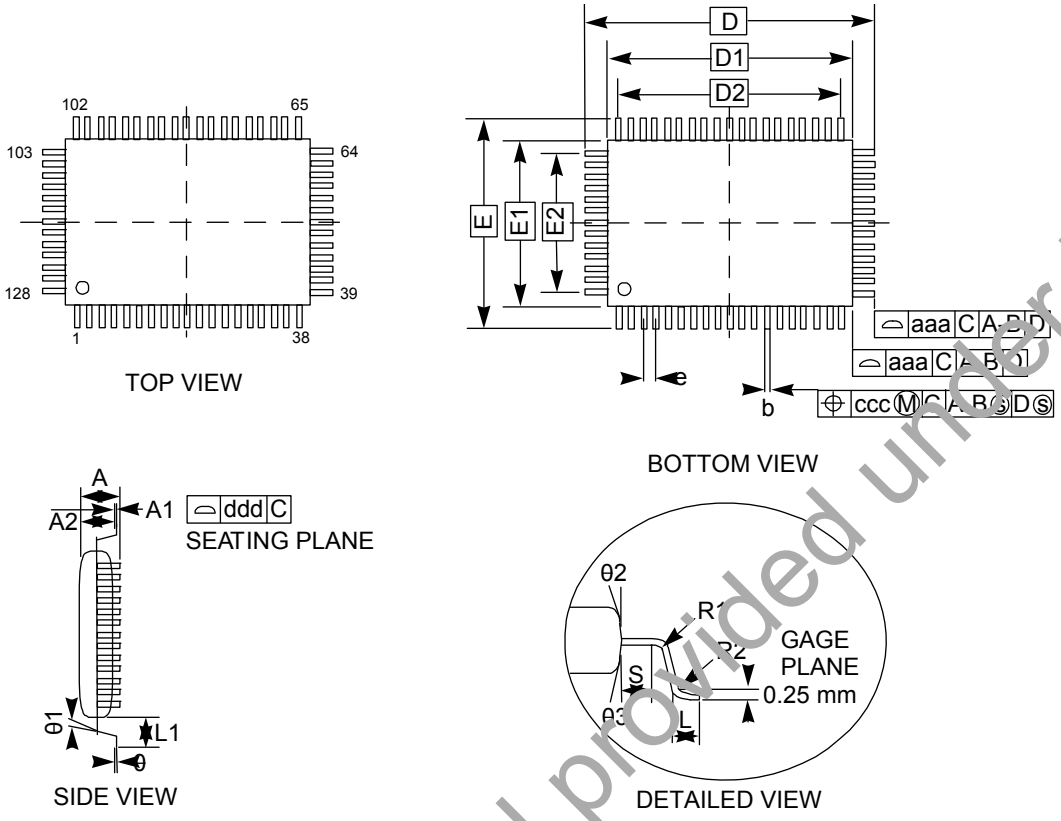
23 Thermal Specifications

The following table lists the thermal specifications.

Table 36. KSZ8342 Thermal Specifications

Parameter	176-Pin LQFP	128-Pin QFP	Units
$Theta_{JA}$	31.3	41.5	°C/W
Ta	70	70	°C
Tj	125	125	°C
Tj - Ta	55	55	°C
Power Allowed	1.76	133	W

24 Mechanical Specifications



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A			3.40			0.134
A1	0.25			0.010		
A2	2.50	2.72	2.90	0.098	0.107	0.114
D	23.20 BASIC			0.913 BASIC		
D1	20.00 BASIC			0.787 BASIC		
E	17.20 BASIC			0.677 BASIC		
E1	14.00 BASIC			0.551 BASIC		
R2	0.13		0.30	0.005		0.012
R1	0.13			0.005		
θ	0°		7°	0°		7°
θ1	0°			0°		
θ2	15° REF			15° REF		

SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60 REF			0.63 REF		
S	0.20			0.008		
b	0.170	0.200	0.270	0.007	0.008	0.011
e	0.50 BSC			0.020 BSC		
D2	18.50			0.728		
E2	12.50			0.492		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Figure 32. KSZ8342Q 128-Pin Package Mechanical Specifications

Figure 32 shows the recommended land pattern for the 128-pin PQFP package. In this figure, all units are in millimeters, and all tolerances are ± 0.05 mm.

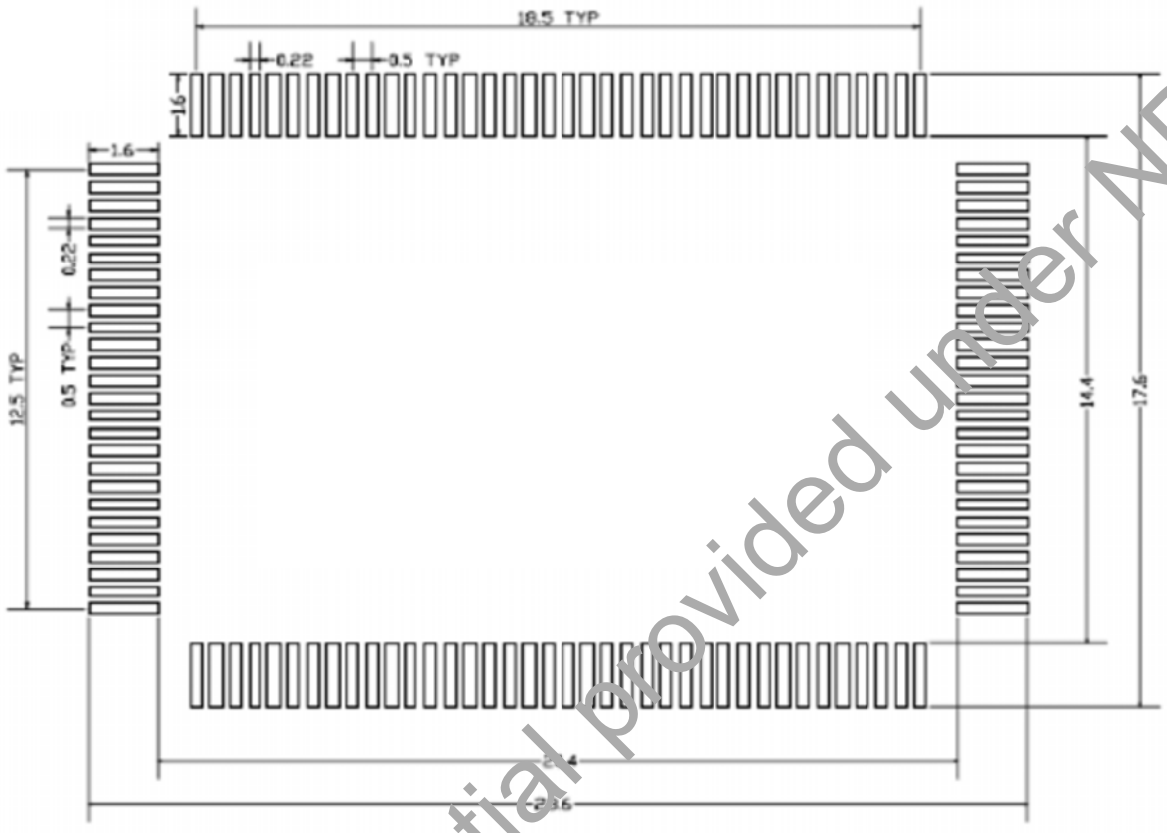


Figure 33. Recommended Land Pattern for 128-pin PQFP Package