TABLE 4-1: MAPPING OF FUNCTIONAL AREAS WITHIN THE ADDRESS SPACE (CONTINUED)

Register Locations	Device Area	Description
0x17 - 0x4F	PHY1 to PHY4 MIIM Registers Mapping to Those Port Registers' Address Range	The same PHY registers as specified in IEEE 802.3 specification.

4.1 Register Map

TABLE 4-2: DIRECT REGISTERS

Address	Contents
0x00-0x01	Family ID, Chip ID, Revision ID, and start switch Registers
0x02-0x0D	Global Control Registers 0 – 11
0x0E-0x0F	Global Power-Down Management Control Registers
0x10-0x14	Port 1 Control Registers 0 – 4
0x15	Port 1 Authentication Control Register
0x16-0x18	Port 1 Reserved (Factory Test Registers)
0x19-0x1F	Port 1 Control/Status Registers
0x20-0x24	Port 2 Control Registers 0 – 4
0x25	Port 2 Authentication Control Register
0x26-0x28	Port 2 Reserved (Factory Test Registers)
0x29-0x2F	Port 2 Control/Status Registers
0x30-0x34	Port 3 Control Registers 0 – 4
0x35	Port 3 Authentication Control Register
0x36-0x38	Port 3 Registered (Factory Test Registers)
0x39-0x3F	Port 3 Control/Status Registers
0x40-0x44	Port 4 Control Registers 0 – 4
0x45	Port 4 Authentication Control Register
0x46-0x48	Port 4 Reserved (Factory Test Registers)
0x49-0x4F	Port 4 Control/Status Registers
0x50-0x54	Port 5 Control Registers 0 – 4
0x56-0x58	Port 5 Reserved (Factory Test Registers)
0x59-0x5F	Port 5 Control/Status Registers
0x60-0x67	Reserved (Factory Testing Registers)
0x68-0x6D	MAC Address Registers
0x6E-0x6F	Indirect Access Control Registers
0x70-0x78	Indirect Data Registers
0x79-0x7B	Reserved (Factory Testing Registers)
0x7C-0x7D	Global Interrupt and Mask Registers
0x7E-0x7F	ACL Interrupt Status and Control Registers
0x80-0x87	Global Control Registers 12 – 19
0x88	Switch Self-Test Control Register
0x89-0x8F	QM Global Control Registers
0x90-0x9F	Global TOS Priority Control Registers 0 - 15
0xA0	Global Indirect Byte Register
0xA0-0xAF	Reserved (Factory Testing Registers)
0xB0-0xBE	Port 1 Control Registers