



SMARTsemi™

SMARTsemi
Memory IC Datasheet
DDR3-1866 2Gb x8

June 22, 2022

Rev 1.0



Part Number Decoder

| K | T | D | M | 2 | G | 3 | C | 8 | 1 | 8 | B | G | x | E | A | T |
|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |

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|-------|--|
| 1-2 | IC Supplier KT: SMARTsemi |
| 3-4 | Product Family DM: DRAM |
| 5-6 | Density 2G: 2Gb |
| 7 | Technology 3: DDR3 |
| 8 | Voltage C: 1.35V/1.5V |
| 9 | Width 8: x8 |
| 10-11 | Speed 18: DDR3-1866 |
| 12-13 | Package BG: Mono BGA |
| 14 | Temperature C: Commercial I: Industrial |
| 15-16 | Internal Code EA: For Internal Use |
| 17 | Packaging T: Tray |

Revision History

| Date | Rev | Description |
|---------------|-----|------------------|
| June 22, 2022 | 1.0 | Initial release. |

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DDR3(L) SDRAM

32M x 8 Bit x 8 Banks
DDR3(L) SDRAM

Features

- **Interface and Power Supply**
 - SSTL_135: VDD/VDDQ = 1.35V(-0.067V/+0.1V)
 - SSTL_15: VDD/VDDQ = 1.5V(±0.075V)
- **JEDEC DDR3(L) Compliant**
 - 8n Prefetch Architecture
 - Differential Clock (CK/CK) and Data Strobe (DQS/DQS)
 - Double-data rate on DQs, DQS and DM
- **Data Integrity**
 - Auto Refresh and Self Refresh Modes
- **Power Saving Mode**
 - Partial Array Self Refresh (PASR)
 - Power Down Mode
- **Signal Integrity**
 - Configurable DS for system compatibility
 - Configurable On-Die Termination
 - ZQ Calibration for DS/ODT impedance accuracy via external ZQ pad (240 ohm ± 1%)
- **Signal Synchronization**
 - Write Leveling via MR settings
 - Read Leveling via MPR
- **Programmable Functions**
 - CAS Latency (5/6/7/8/9/10/11/12/13/14)
 - CAS Write Latency (5/6/7/8/9/10)
 - Additive Latency (0/CL-1/CL-2)
 - Write Recovery Time (5/6/7/8/10/12/14/16)
 - Burst Type (Sequential/Interleaved)
 - Burst Length (BL8/BC4/BC4 or 8 on the fly)
 - Self Refresh Temperature Range (Normal/Extended)
 - Output Driver Impedance (34/40)
 - On-Die Termination of RTT_Nom (20/30/40/60/120)
 - On-Die Termination of RTT_WR (60/120)
 - Precharge Power Down (slow/fast)

Ordering Information

| Product ID | Max Freq. | V _{DD} | Data Rate (CL-tRCD-tRP) | Package | Temperature | Packing | Comments |
|-------------------|-----------|-----------------|-------------------------|-------------|-------------|---------|----------|
| KTDM2G3C818BGCEAT | 933MHz | 1.35V/1.5V | DDR3(L)-1866 (13-13-13) | 78 ball BGA | Commercial | Tray | Pb-free |
| KTDM2G3C818BGIEAT | 933MHz | 1.35V/1.5V | DDR3(L)-1866 (13-13-13) | 78 ball BGA | Industrial | Tray | Pb-free |

Description

The 2Gb Double-Data-Rate-3 (DDR3(L)) DRAM is double data rate architecture to achieve high-speed operation. It is internally configured as an eight-bank DRAM.

The 2Gb chip is organized as 32Mbit x 8 I/Os x 8 bank devices. These synchronous devices achieve high speed double-data-rate transfer rates of up to 1866 Mb/sec/pin for general applications.

The chip is designed to comply with all key DDR3(L) DRAM key features and all of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and CK falling). All I/Os are synchronized with a differential DQS pair in a source synchronous fashion.

These devices operate with a single 1.35V -0.067V/+0.1V or 1.5V ± 0.075V power supply and are available in BGA packages.

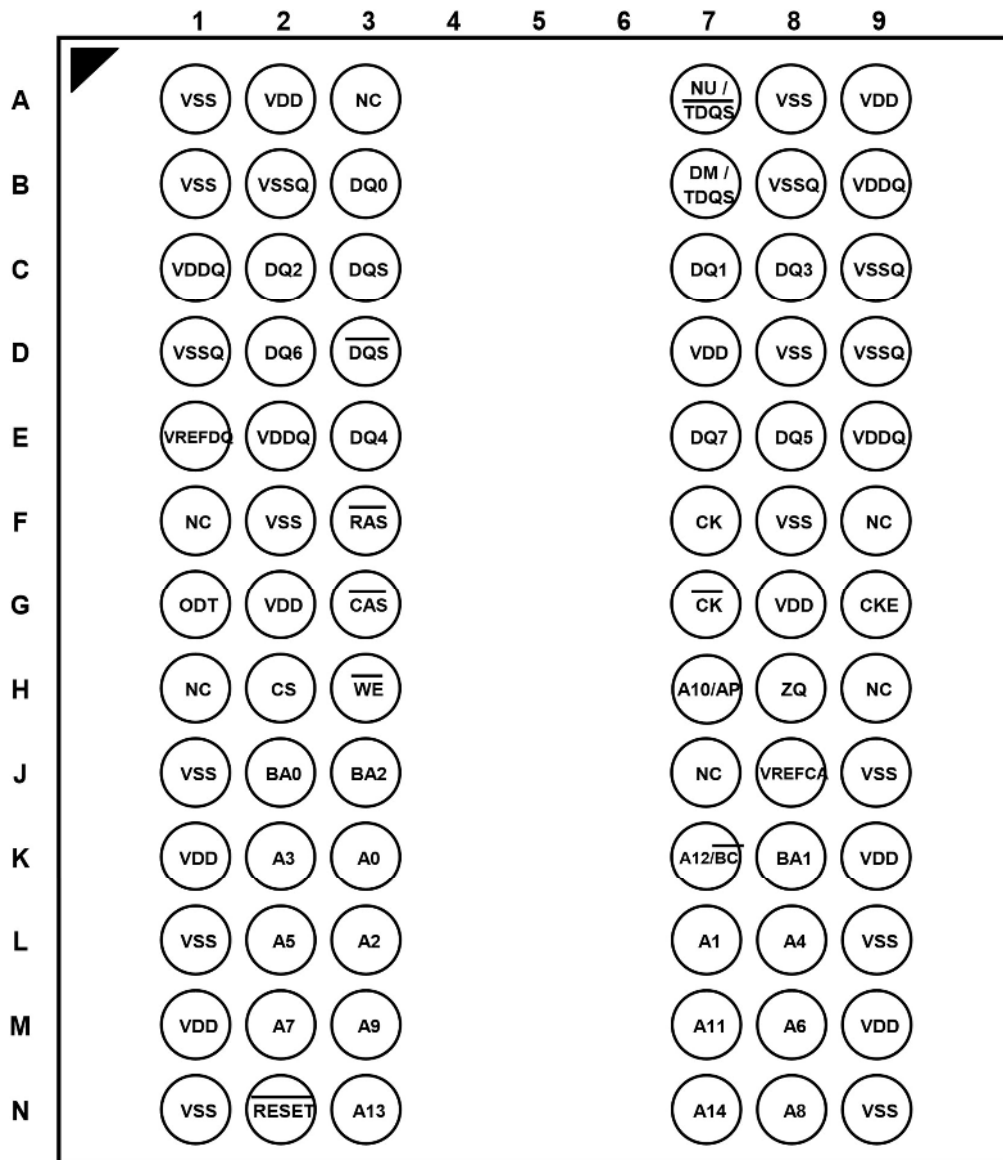
DDR3(L) SDRAM Addressing

| Configuration | 256Mb x 8 |
|--|-----------|
| # of Bank | 8 |
| Bank Address | BA0 – BA2 |
| Auto precharge | A10/ P |
| BL switch on the fly | A12/BC |
| Row Address | A0 – A14 |
| Column Address | A0 – A9 |
| Page size | 1KB |
| <p>Note:</p> <p>Page size is the number of bytes of data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered. Page size is per bank, calculated as follows</p> $\text{Page size} = 2^{\text{COLBITS}} * \text{ORG} / 8$ <p>where</p> <p>COLBITS = the number of column address bits</p> <p>ORG = the number of I/O (DQ) bits</p> | |

Pin Configuration – 78 balls BGA Package

< TOP View >

See the balls through the package



Input / Output Functional Description

| Symbol | Type | Function |
|---|--------------|--|
| CK, \overline{CK} | Input | Clock: CK and \overline{CK} are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of \overline{CK} . |
| CKE | Input | Clock Enable: CKE high activates, and CKE low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, \overline{CK} , ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh. |
| \overline{CS} | Input | Chip Select: All commands are masked when \overline{CS} is registered HIGH. \overline{CS} provides for external rank selection on systems with multiple ranks. \overline{CS} is considered part of the command code. |
| \overline{RAS} , \overline{CAS} , \overline{WE} | Input | Command Inputs: \overline{RAS} , \overline{CAS} and \overline{WE} (along with \overline{CS}) define the command being entered. |
| DM, | Input | Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM or TDQS/TDQS is enabled by Mode Register A11 setting in MR1. |
| BA0 - BA2 | Input | Bank Address Inputs: BA0, BA1, and BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle. |
| A10 / AP | Input | Auto-Precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses. |
| A0 – A14 | Input | Address Inputs: Provide the row address for Activate commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/BC have additional function; as below.) The address inputs also provide the op-code during Mode Register Set commands. |
| A12/ \overline{BC} | Input | Burst Chop: A12/ \overline{BC} is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH: no burst chop; LOW: burst chopped). |
| ODT | Input | On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3(L) SDRAM. When enabled, ODT is applied to each DQ, DQS, DQS and DM. The ODT pin will be ignored if MR1 and MR2 are programmed to disable RTT. |
| TDQS, \overline{TDQS} | Output | Termination Data Strobe: TDQS/ \overline{TDQS} is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS/ \overline{TDQS} that is applied to DQS/ \overline{DQS} . When disabled via mode register A11 = 0 in MR1, DM/TDQS will provide the data mask function and \overline{TDQS} is not used. |
| \overline{RESET} | Input | Active Low Asynchronous Reset: Reset is active when \overline{RESET} is LOW, and inactive when \overline{RESET} is HIGH. \overline{RESET} must be HIGH during normal operation. \overline{RESET} is a CMOS rail-to-rail signal with DC high and low at 80% and 20% of VDD, i.e. 1.20V for DC high and 0.30V for DC low. |
| DQ | Input/output | Data Inputs/Output: Bi-directional data bus. |

| Symbol | Type | Function |
|---|--------------|--|
| DQS, $\overline{\text{DQS}}$ | Input/output | Data Strobe: output with read data, input with write data. Edge aligned with read data, centered with write data. The data strobes DQS are paired with differential signals $\overline{\text{DQS}}$ respectively, to provide differential pair signaling to the system during both reads and writes. DDR3(L) SDRAM supports differential data strobe only and does not support single-ended.. |
| NC | - | No Connect: No internal electrical connection is present. |
| VDDQ | Supply | DQ Power Supply: 1.35V -0.067V/+0.1V or 1.5V \pm 0.075V |
| VDD | Supply | Power Supply: 1.35V -0.067V/+0.1V or 1.5V \pm 0.075V |
| VSSQ | Supply | DQ Ground |
| VSS | Supply | Ground |
| VREFCA | Supply | Reference voltage for CA |
| VREFDQ | Supply | Reference voltage for DQ |
| ZQ | Supply | Reference pin for ZQ calibration. |
| Note: Input only pins (BA0-BA2, A0-A14, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{CS}}$, CKE, ODT, and $\overline{\text{RESET}}$) do not supply termination. | | |

Absolute Maximum Ratings

Absolute Maximum DC Ratings

| Symbol | Parameter | Rating | Unit | Note |
|------------------------------------|-------------------------------------|-------------|------|------|
| VDD | Voltage on VDD pin relative to VSS | -0.4 ~ 1.80 | V | 1,3 |
| VDDQ | Voltage on VDDQ pin relative to VSS | -0.4 ~ 1.80 | V | 1,3 |
| V _{IN} , V _{OUT} | Voltage on any pin relative to VSS | -0.4 ~ 1.80 | V | 1 |
| T _{STG} | Storage Temperature | -55 ~ 150 | °C | 1,2 |

Note:

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Storage Temperature is the case surface temperature on the center/top side of the DRAM.
- VDD and VDDQ must be within 300mV of each other at all times; and VREF must be not greater than 0.6 x DDQ, when VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

DRAM Component Operating Temperature Range

Temperature Range

| Symbol | Parameter | Value | Unit | Note |
|-------------------|---|-----------|------|------|
| T _{OPER} | Normal Operating Temperature Range - Commercial | 0 to 85 | °C | 1,2 |
| | Normal Operating Temperature Range - Industrial | -40 to 85 | | |
| | Extended Temperature Range | 85 to 95 | °C | 1,3 |

Note:

- Operating Temperature T_{OPER} is the case surface temperature on the center/top side of the DRAM.
- The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85°C for Commercial temperature or -40 to 85°C for Industrial temperature under all operating conditions.
- Some applications require operation of the DRAM in the Extended Temperature Range.
 - Refresh commands must be doubled in frequency, therefore, reducing the Refresh interval tREFI to 3.9us.
 - If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6=0 and MR2 A7=1) or enable the optional Auto Self-Refresh mode (MR2 A6=1 and MR2 A7=0).

AC & DC Operating Conditions

Recommended DC Operating Conditions

| Symbol | Parameter | Operation Voltage | Rating | | | Unit | Note |
|--------|---------------------------|-------------------|--------|------|-------|------|-------|
| | | | Min. | Typ. | Max. | | |
| VDD | Supply Voltage | 1.5V | 1.425 | 1.5 | 1.575 | V | 1,2 |
| | | 1.35V | 1.283 | 1.35 | 1.45 | V | 3,4,5 |
| VDDQ | Supply Voltage for Output | 1.5V | 1.425 | 1.5 | 1.575 | V | 1,2 |
| | | 1.35V | 1.283 | 1.35 | 1.45 | V | 3,4,5 |

Note:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. Maximum DC value may not be greater than 1.425V. The DC value is the linear average of VDD/VDDQ(t) over a very long period of time.
4. If maximum limit is exceeded, input levels shall be governed by DDR3 specifications.
5. Under these supply voltages, the device operates to this DDR3L specification.

AC & DC Input Measurement Levels

AC and DC Logic Input Levels for Single-Ended Signals

AC and DC Input Levels for Single-Ended Command and Address Signals

Single-Ended AC and DC Input Levels for Command and Address

| Symbol | Parameter | DDR3-1866 | | Unit | Note |
|---------------|---------------------------------------|--------------|--------------|------|-------|
| | | Min. | Max. | | |
| VIH.CA(DC100) | DC input logic high | VREF + 0.1 | VDD | V | 1,5 |
| VIL.CA(DC100) | DC input logic low | VSS | VREF - 0.1 | V | 1,6 |
| VIH.CA(AC175) | AC input logic high | - | - | V | 1,2,7 |
| VIL.CA(AC175) | AC input logic low | - | - | V | 1,2,8 |
| VIH.CA(AC150) | AC input logic high | - | - | V | 1,2,7 |
| VIL.CA(AC150) | AC input logic low | - | - | V | 1,2,8 |
| VIH.CA(AC135) | AC input logic high | VREF + 0.135 | Note2 | V | 1,2,7 |
| VIL.CA(AC135) | AC input logic low | Note2 | VREF - 0.135 | V | 1,2,8 |
| VIH.CA(AC125) | AC input logic high | VREF + 0.125 | Note2 | V | 1,2,7 |
| VIL.CA(AC125) | AC input logic low | Note2 | VREF - 0.125 | V | 1,2,8 |
| VREFCA(DC) | Reference Voltage for ADD, CMD inputs | 0.49 * VDD | 0.51 * VDD | V | 3,4,9 |

Note:

- For input only pins except $\overline{\text{RESET}}$. VREF=VREFCA(DC).
- See "Overshoot and Undershoot Specifications".
- The ac peak noise on VREF may not allow VREF to deviate from VREFCA(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV).
- For reference: approx. VDD/2 +/- 15 mV.
- VIH(DC) is used as a simplified symbol for VIH.CA(DC100).
- VIL(DC) is used as a simplified symbol for VIL.CA(DC100).
- VIH(AC) is used as a simplified symbol for VIH.CA(AC175), VIH.CA(AC150), VIH.CA(AC135), and VIH.CA(AC125); VIH.CA(AC175) value is used when VREF + 0.175V is referenced, VIH.CA(AC150) value is used when VREF + 0.150V is referenced, VIH.CA(AC135) value is used when VREF + 0.135V is referenced, and VIH.CA(AC125) value is used when VREF + 0.125V is referenced.
- VIL(AC) is used as a simplified symbol for VIL.CA(AC175), VIL.CA(AC150), VIL.CA(AC135) and VIL.CA(AC125); VIL.CA(AC175) value is used when VREF - 0.175V is referenced, VIL.CA(AC150) value is used when VREF - 0.150V is referenced, VIL.CA(AC135) value is used when VREF - 0.135V is referenced, and VIL.CA(AC125) value is used when VREF - 0.125V is referenced.
- VREFCA(DC) is measured relative to VDD at the same point in time on the same device.

Single-Ended AC and DC Input Levels for Command and Address - Continued

| Symbol | Parameter | DDR3L-1866 | | Unit | Note |
|--|---------------------------------------|--------------|--------------|------|------|
| | | Min. | Max. | | |
| VIH.CA(DC90) | DC input logic high | VREF + 0.09 | VDD | V | 1 |
| VIL.CA(DC90) | DC input logic low | VSS | VREF - 0.09 | V | 1 |
| VIH.CA(AC160) | AC input logic high | - | - | V | 1,2 |
| VIL.CA(AC160) | AC input logic low | - | - | V | 1,2 |
| VIH.CA(AC135) | AC input logic high | VREF + 0.135 | Note2 | V | 1,2 |
| VIL.CA(AC135) | AC input logic low | Note2 | VREF -0.135 | V | 1,2 |
| VIH.CA(AC125) | AC input logic high | VREF + 0.125 | Note2 | V | 1,2 |
| VIL.CA(AC125) | AC input logic low | Note2 | VREF - 0.125 | V | 1,2 |
| VREFCA(DC) | Reference Voltage for ADD, CMD inputs | 0.49 * VDD | 0.51 * VDD | V | 3,4 |
| Note: <ol style="list-style-type: none"> 1. For input only pins except $\overline{\text{RESET}}$.VREF=VREFCA(DC). 2. See "Overshoot and Undershoot Specifications". 3. The ac peak noise on VREF may not allow VREF to deviate from VREFCA(DC) by more than +/-1% VDD (for reference: approx. +/- 13.5 mV). 4. For reference: approx. VDD/2 +/- 13.5mV. | | | | | |

AC and DC Input Levels for Single-Ended Data Signals
Single-Ended AC and DC Input Levels for DQ and DM

| Symbol | Parameter | DDR3-1866 | | Unit | Note |
|---------------|-------------------------------------|--------------|--------------|------|-------|
| | | Min. | Max. | | |
| VIH.DQ(DC100) | DC input logic high | VREF + 0.1 | VDD | V | 1,5 |
| VIL.DQ(DC100) | DC input logic low | VSS | VREF - 0.1 | V | 1,6 |
| VIH.DQ(AC175) | AC input logic high | - | - | V | 1,2,7 |
| VIL.DQ(AC175) | AC input logic low | - | - | V | 1,2,8 |
| VIH.DQ(AC150) | AC input logic high | - | - | V | 1,2,7 |
| VIL.DQ(AC150) | AC input logic low | - | - | V | 1,2,8 |
| VIH.DQ(AC135) | AC input logic high | VREF + 0.135 | Note2 | V | 1,2,7 |
| VIL.DQ(AC135) | AC input logic low | Note2 | VREF - 0.135 | V | 1,2,8 |
| VREFDQ(DC) | Reference Voltage for DQ, DM inputs | 0.49 * VDD | 0.51 * VDD | V | 3,4,9 |

Note:

1. VREF = VREFDQ(DC).
2. See "Overshoot and Undershoot Specifications".
3. The ac peak noise on VREF may not allow VREF to deviate from VREFDQ(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV).
4. For reference: approx. VDD/2 +/- 15 mV.
5. VIH(DC) is used as a simplified symbol for VIH.DQ(DC100).
6. VIL(DC) is used as a simplified symbol for VIL.DQ(DC100).
7. VIH(AC) is used as a simplified symbol for VIH.DQ(AC175), VIH.DQ(AC150), and VIH.DQ(AC135); VIH.DQ(AC175) value is used when VREF + 0.175V is referenced, VIH.DQ(AC150) value is used when VREF + 0.150V is referenced, and VIH.DQ(AC135) value is used when VREF + 0.135V is referenced.
8. VIL(AC) is used as a simplified symbol for VIL.DQ(AC175), VIL.DQ(AC150), and VIL.DQ(AC135); VIL.DQ(AC175) value is used when VREF - 0.175V is referenced, VIL.DQ(AC150) value is used when VREF - 0.150V is referenced, and VIL.DQ(AC135) value is used when VREF - 0.135V is referenced.
9. VREFDQ(DC) is measured relative to VDD at the same point in time on the same device.

Single-Ended AC and DC Input Levels for DQ and DM - Continued

| Symbol | Parameter | DDR3L-1866 | | Unit | Note |
|---|-------------------------------------|--------------|--------------|------|------|
| | | Min. | Max. | | |
| VIH.DQ(DC90) | DC input logic high | VREF + 0.09 | VDD | V | 1 |
| VIL.DQ(DC90) | DC input logic low | VSS | VREF - 0.09 | V | 1 |
| VIH.DQ(AC135) | AC input logic high | - | - | V | 1,2 |
| VIL.DQ(AC135) | AC input logic low | - | - | V | 1,2 |
| VIH.DQ(AC130) | AC input logic high | VREF + 0.130 | Note2 | V | 1,2 |
| VIL.DQ(AC130) | AC input logic low | Note2 | VREF - 0.130 | V | 1,2 |
| VREFDQ(DC) | Reference Voltage for DQ, DM inputs | 0.49 * VDD | 0.51 * VDD | V | 3,4 |
| Note: 1. VREF = VREFDQ(DC). 2. See "Overshoot and Undershoot Specifications". 3. The ac peak noise on VREF may not allow VREF to deviate from VREFDQ(DC) by more than +/-1% VDD (for reference: approx. +/- 13.5 mV). 4. For reference: approx. VDD/2 +/- 13.5 mV. | | | | | |

VREF Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages VREFCA and VREFDQ are illustrated in the following figure. It shows a valid reference voltage VREF (t) as a function of time. (VREF stands for VREFCA and VREFDQ likewise).

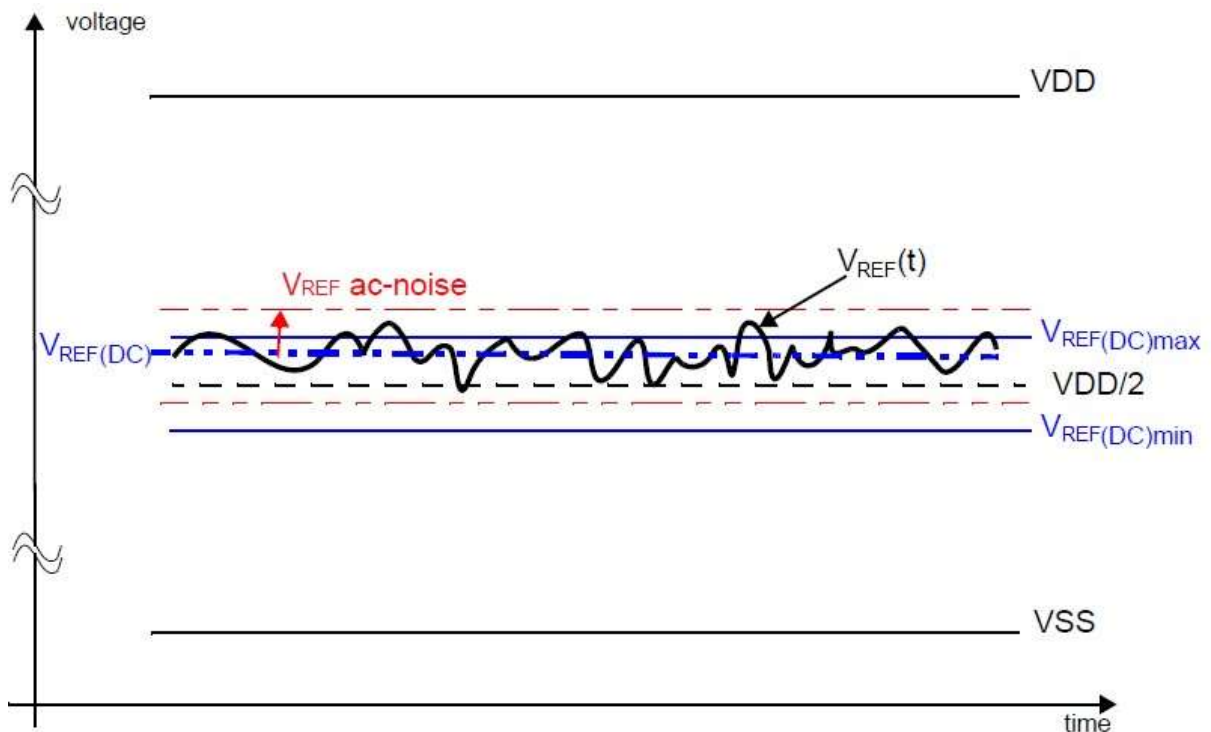
VREF(DC) is the linear average of VREF(t) over a very long period of time (e.g., 1 sec). This average has to meet the min/max requirement in previous page. Furthermore VREF(t) may temporarily deviate from VREF(DC) by no more than $\pm 1\%$ VDD.

The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC), and VIL(DC) are dependent on VREF. "VREF" shall be understood as VREF(DC).

The clarifies that dc-variations of VREF affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for VREF(DC) deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and de-rating values need to include time and voltage associated with VREF ac-noise. Timing and voltage effects due to ac-noise on VREF up to the specified limit ($\pm 1\%$ of VDD) are included in DRAM timing and their associated de-ratings.

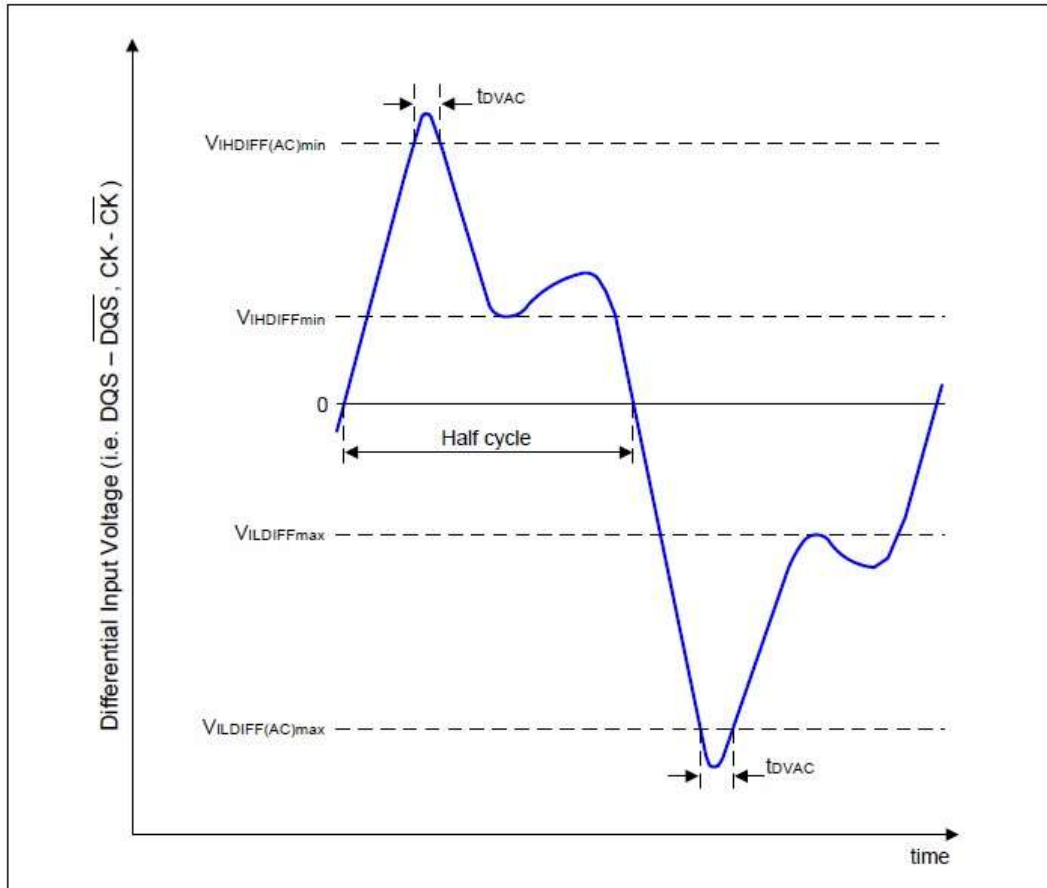
Illustration of VREF(DC) tolerance and VREF ac-noise limits



AC and DC Logic Input Levels for Differential Signals

Differential signal definition

Definition of differential ac-swing and “time above ac-level” tDVAC



Differential swing requirements for clock (CK - \overline{CK}) and strobe (DQS - \overline{DQS})
Differential AC and DC Input Levels
Differential AC and DC Input Levels

| Symbol | Parameter | DDR3-1866 | | Unit | Note |
|---|-------------------------------|----------------------|---------------------|------|------|
| | | Min. | Max. | | |
| VIHdiff | Differential input logic high | +0.200 | Note3 | V | 1 |
| VILdiff | Differential input logic low | Note3 | -0.200 | V | 1 |
| VIHdiff(AC) | Differential input high ac | 2 x (VIH(AC) – VREF) | Note3 | V | 2 |
| VILdiff(AC) | Differential input low ac | Note3 | 2 x (VIL(AC)- VREF) | V | 2 |
| Note: <ol style="list-style-type: none"> Used to define a differential signal slew-rate. For CK - \overline{CK} use VIH/VIL(AC) of ADD/CMD and VREFCA; for DQS - \overline{DQS}, DQSL, \overline{DQSL}, DQSU, \overline{DQSU} use VIH/VIL(AC) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also there. These values are not defined, however the single-ended signals CK, \overline{CK}, DQS, \overline{DQS}, DQSL, \overline{DQSL}, DQSU, \overline{DQSU} need to be within the respective limits (VIH(DC)max, VIL(DC)min) for single-ended signals as well as limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot Specifications". | | | | | |

| Symbol | Parameter | DDR3L-1866 | | Unit | Note |
|---|-------------------------------|----------------------|----------------------|------|------|
| | | Min. | Max. | | |
| VIHdiff | Differential input logic high | +0.180 | Note3 | V | 1 |
| VILdiff | Differential input logic low | Note3 | -0.180 | V | 1 |
| VIHdiff(AC) | Differential input high ac | 2 x (VIH(AC) – VREF) | Note3 | V | 2 |
| VILdiff(AC) | Differential input low ac | Note3 | 2 x (VIL(AC) - VREF) | V | 2 |
| Note: <ol style="list-style-type: none"> Used to define a differential signal slew-rate. For CK - \overline{CK} use VIH/VIL(AC) of ADD/CMD and VREFCA; for DQS - \overline{DQS}, DQSL, \overline{DQSL}, DQSU, \overline{DQSU} use VIH/VIL(AC) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also there. These values are not defined, however the single-ended signals CK, \overline{CK}, DQS, \overline{DQS}, DQSL, \overline{DQSL}, DQSU, \overline{DQSU} need to be within the respective limits (VIH(DC)max, VIL(DC)min) for single-ended signals as well as limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot Specifications". | | | | | |

Allowed time before ringback (tDVAC) for CK – CK and DQS - DQS

| Slew Rate [V/ns] | DDR3-1866 | | | |
|------------------|---|------|--|------|
| | tDVAC [ps] @ VIH/Ldiff(AC) = 300mV | | tDVAC [ps] @ VIH/Ldiff(AC) = (CK-CK) only | |
| | Min. | Max. | Min. | Max. |
| > 4.0 | 134 | - | 139 | - |
| 4.0 | 134 | - | 139 | - |
| 3.0 | 112 | - | 118 | - |
| 2.0 | 67 | - | 77 | - |
| 1.8 | 52 | - | 63 | - |
| 1.6 | 33 | - | 45 | - |
| 1.4 | 9 | - | 23 | - |
| 1.2 | note | - | note | - |
| 1.0 | note | - | note | - |
| < 1.0 | note | - | note | - |

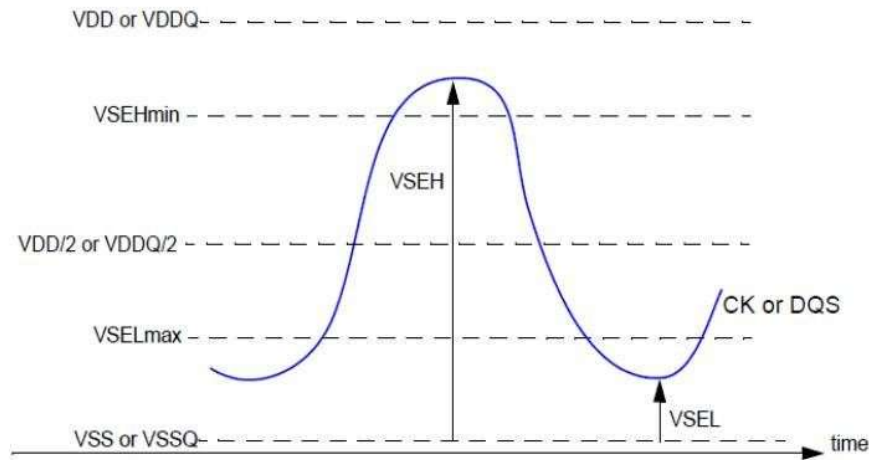
| Slew Rate [V/ns] | DDR3L-1866 | | | | | |
|------------------|---|------|---|------|---|------|
| | tDVAC [ps] @ VIH/Ldiff(AC) = 270mV | | tDVAC [ps] @ VIH/Ldiff(AC) = 250mV | | tDVAC [ps] @ VIH/Ldiff(AC) = 260mV | |
| | Min. | Max. | Min. | Max. | Min. | Max. |
| > 4.0 | 163 | - | 168 | - | 176 | - |
| 4.0 | 163 | - | 168 | - | 176 | - |
| 3.0 | 140 | - | 147 | - | 154 | - |
| 2.0 | 95 | - | 105 | - | 111 | - |
| 1.8 | 80 | - | 91 | - | 97 | - |
| 1.6 | 62 | - | 74 | - | 78 | - |
| 1.4 | 37 | - | 52 | - | 56 | - |
| 1.2 | 5 | - | 22 | - | 24 | - |
| 1.0 | note | - | note | - | note | - |
| < 1.0 | note | - | note | - | note | - |

Single-ended requirements for differential signals

Each individual component of a differential signal (CK, DQS, DQSL, DQSU, $\overline{\text{CK}}$, $\overline{\text{DQS}}$, $\overline{\text{DQSL}}$, or $\overline{\text{DQSU}}$) has also to comply with certain requirements for single-ended signals.

CK and $\overline{\text{CK}}$ have to approximately reach VSEHmin / VSELmax (approximately equal to the ac-levels (VIH (AC) / VIL (AC)) for ADD/CMD signals) in every half-cycle. DQS, DQSL, DQSU, $\overline{\text{DQS}}$, $\overline{\text{DQSL}}$, $\overline{\text{DQSU}}$ have to reach VSEHmin / VSELmax (approximately the ac-levels (VIH (AC) / VIL (AC)) for DQ signals) in every half-cycle preceding and following a valid transition.

Note that the applicable ac-levels for ADD/CMD and DQ's might be different per speed-bin etc. E.g., if VIH.CA (AC150) / VIL.CA (AC150) is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK and $\overline{\text{CK}}$.



Note that, while ADD/CMD and DQ signal requirements are with respect to Vref, the single-ended components of differential signals have a requirement with respect to VDD / 2; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSELmax, VSEHmin has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Single-ended levels for CK, DQS, DQSL, DQSU, $\overline{\text{CK}}$, $\overline{\text{DQS}}$, $\overline{\text{DQSL}}$ or $\overline{\text{DQSU}}$

| Symbol | Parameter | DDR3(L)-1866 | | Unit | Note |
|--------|--|--------------------------|--------------------------|------|------|
| | | Min. | Max. | | |
| VSEH | Single-ended high level for strobes | $(\text{VDD}/2) + 0.175$ | note3 | V | 1, 2 |
| | Single-ended high level for CK, $\overline{\text{CK}}$ | $(\text{VDD}/2) + 0.175$ | note3 | V | 1, 2 |
| VSEL | Single-ended low level for strobes | note3 | $(\text{VDD}/2) - 0.175$ | V | 1, 2 |
| | Single-ended low level for CK, $\overline{\text{CK}}$ | note3 | $(\text{VDD}/2) - 0.175$ | V | 1, 2 |

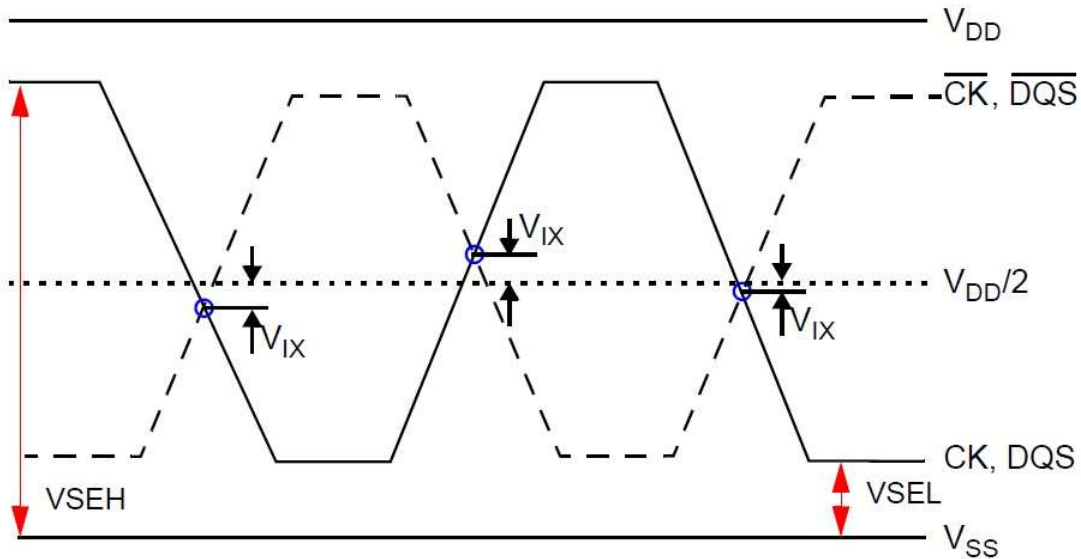
Note:

- For CK, $\overline{\text{CK}}$ use VIH.CA (AC) /VIL.CA (AC) of ADD/CMD; for strobes (DQS, DQSL, DQSU, $\overline{\text{DQS}}$, $\overline{\text{DQSL}}$, $\overline{\text{DQSU}}$) use VIH.DQ (AC)/VIL.CA (AC) of DQs.
- VIH.DQ (AC)/VIL.CA (AC) for DQs is based on VREFDQ; VIH.CA (AC) /VIL.CA (AC) for ADD/CMD is based on VREFCA; if a reduced AC-high or AC-low level is used for a signal group, then the reduced level applies also there.
- These values are not defined, however the single-ended signals CK, $\overline{\text{CK}}$, DQS, $\overline{\text{DQS}}$, DQSL, $\overline{\text{DQSL}}$, DQSU, $\overline{\text{DQSU}}$ need to be within the respective limits (VIH(DC)max, VIL(DC)min) for single-ended signals as well as limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot Specifications".

Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, \overline{CK} and DQS, \overline{DQS}) must meet the requirements in the following table. The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complete signal to the midlevel between of V_{DD} and V_{SS} .

V_{IX} Definition



Cross point voltage for differential input signals (CK, DQS)

| Symbol | Parameter | DDR3-1866 | | DDR3L-1866 | | Unit | Note |
|---------------|---|-----------|------|------------|------|------|------|
| | | Min. | Max. | Min. | Max. | | |
| $V_{IX}(CK)$ | Differential Input Cross Point Voltage relative to $V_{DD}/2$ for CK, \overline{CK} | -150 | 150 | -150 | +150 | mV | 1 |
| | | -175 | 175 | - | - | mV | 2 |
| $V_{IX}(DQS)$ | Differential Input Cross Point Voltage relative to $V_{DD}/2$ for DQS, \overline{DQS} | -150 | 150 | -150 | +150 | mV | 1 |

Note:

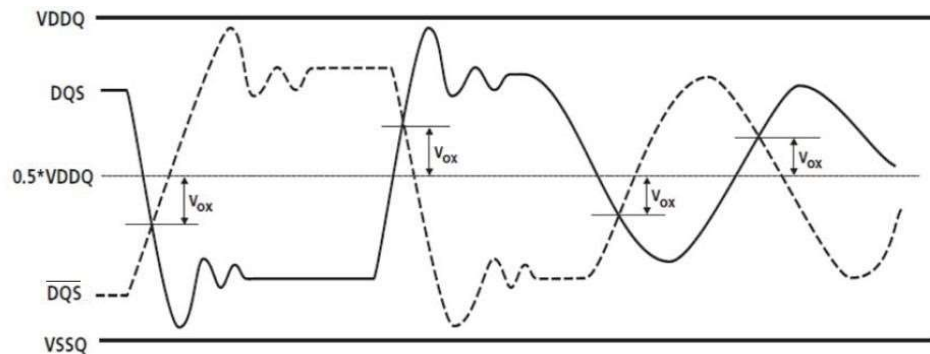
- The relation between V_{IX} Min/Max and V_{SEL}/V_{SEH} should satisfy following.
 $(V_{DD}/2) + V_{IX}(\text{Min.}) - V_{SEL} \geq 25\text{mV}$
 $V_{SEH} - ((V_{DD}/2) + V_{IX}(\text{Max.})) \geq 25\text{mV}$
- Extended range for V_{IX} is only allowed for clock and if single-ended clock input signals CK and \overline{CK} are monotonic with a single-ended swing V_{SEL} / V_{SEH} of at least $V_{DD}/2 \pm 250\text{mV}$, and when the differential slew rate of $CK-\overline{CK}$ is larger than 3V/ns .

DQS Output Cross point voltage – DDR3L-1866 V_{ox}

| Symbol | Parameter | DQS/ \overline{DQS} Differential Slew Rate | | | | | | | | | | Unit |
|----------|---|--|-------|-------|-------|-------|-------|-------|--------|--------|------|------|
| | | 3.5V/ns | 4V/ns | 5V/ns | 6V/ns | 7V/ns | 8V/ns | 9V/ns | 10V/ns | 12V/ns | | |
| V_{ox} | Deviation of DQS/ \overline{DQS} output cross point voltage from 0.5 x VDDQ | Max | +90 | +105 | +130 | +155 | +180 | +205 | +205 | +205 | +205 | mV |
| | | Min | -90 | -105 | -130 | -155 | -180 | -205 | -205 | -205 | -205 | |

Note:

1. Measured using an effective test load of 25 Ω to 0.5*VDDQ at each of the differential outputs.
2. For a differential slew rate in between the listed values, the V_{ox} value may be obtained by linear interpolation.
3. Refer to the following figure for reference drawing, DQS/ \overline{DQS} shown single-ended for measurement point.
4. The DQS/ \overline{DQS} pins under test are not required to be able to drive each of the slew rates listed in the table; the pins under test will provide one V_{ox} value when tested with specified test condition. The DQS and \overline{DQS} differential slew rate when measuring V_{ox} determines which V_{ox} limits to use.

Definition of Output cross point voltage for DQS and \overline{DQS}


Slew Rate Definitions for Single-Ended Input Signals

See “Address / Command Setup, Hold and Derating” for single-ended slew rate definitions for address and command signals. See “Data Setup, Hold and Slew Rate Derating” for single-ended slew rate definitions for data signals.

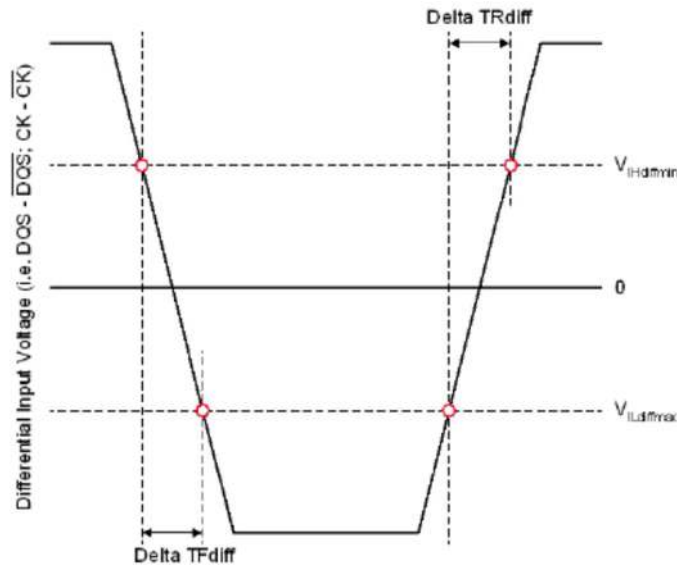
Slew Rate Definition for Differential Input Signals

Input slew rate for differential signals (CK, \overline{CK} and DQS, \overline{DQS}) are defined and measured as shown below.

Differential Input Slew Rate Definition

| Description | Measured | | Defined by |
|---|------------|------------|---|
| | From | To | |
| Differential input slew rate for rising edge (CK- \overline{CK} & DQS- \overline{DQS}) | VILdiffmax | VIHdiffmin | $[VIHdiffmin - VILdiffmax] / \Delta TRdiff$ |
| Differential input slew rate for falling edge (CK- \overline{CK} & DQS- \overline{DQS}) | VIHdiffmin | VILdiffmax | $[VIHdiffmin - VILdiffmax] / \Delta TFdiff$ |
| The differential signal (i.e., CK- \overline{CK} & DQS- \overline{DQS}) must be linear between these thresholds. | | | |

Differential Input Slew Rate Definition for DQS, \overline{DQS} and CK, \overline{CK}



AC and DC Output Measurement Levels

Single Ended AC and DC Output Levels

| Symbol | Parameter | Value | Unit | Note |
|---------|---|--------------|------|------|
| VOH(DC) | DC output high measurement level (for IV curve linearity) | 0.8xVDDQ | V | |
| VOM(DC) | DC output mid measurement level (for IV curve linearity) | 0.5xVDDQ | V | |
| VOL(DC) | DC output low measurement level (fro IV curve linearity) | 0.2xVDDQ | V | |
| VOH(AC) | AC output high measurement level (for output SR) | VTT+0.1xVDDQ | V | 1 |
| VOL(AC) | AC output low measurement level (for output SR) | VTT-0.1xVDDQ | V | 1 |

Note:

1. The swing of $\pm 0.1 \times VDDQ$ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to $VTT = VDDQ/2$.

Differential AC and DC Output Levels

| Symbol | Parameter | Value | Unit | Note |
|-------------|---|-------------|------|------|
| VOHdiff(AC) | AC differential output high measurement level (for output SR) | +0.2 x VDDQ | V | 1 |
| VOLdiff(AC) | AC differential output low measurement level (for output SR) | -0.2 x VDDQ | V | 1 |

Note:

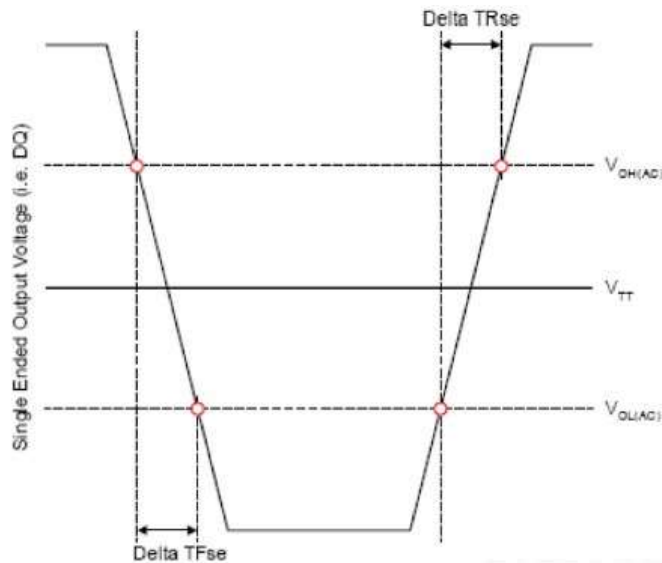
1. The swing of $\pm 0.2 \times VDDQ$ is based on approximately 50% of the static differential output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to $VTT=VDDQ/2$ at each of the differential outputs.

Single Ended Output Slew Rate

Single Ended Output Slew Rate Definition

| Description | Measured | | Defined by |
|--|----------|---------|-----------------------------------|
| | From | To | |
| Single-ended output slew rate for rising edge | VOL(AC) | VOH(AC) | $[VOH(AC)-VOL(AC)] / \Delta TRse$ |
| Single-ended output slew rate for falling edge | VOH(AC) | VOL(AC) | $[VOH(AC)-VOL(AC)] / \Delta TFse$ |

Note: Output slew rate is verified by design and characterization, and may not be subject to production test.



Output Slew Rate (single-ended)

| Parameter | Symbol | DDR3L-1866 | | DDR3-1866 | | Unit |
|-------------------------------|--------|------------|------------------|-----------|------------------|------|
| | | Min. | Max. | Min. | Max. | |
| Single-ended Output Slew Rate | SRQse | 1.75 | 5 ⁽¹⁾ | 2.5 | 5 ⁽¹⁾ | V/ns |

Description:

SR: Slew Rate.

Q: Query Output (like in DQ, which stands for Data-in, Query -Output).

se:Single-ended signals.

For Ron = Rz0/7 setting.

Note:

1. In two cases, a maximum slew rate of 6V/ns applies for a single DQ signal within a byte lane.

Case 1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).

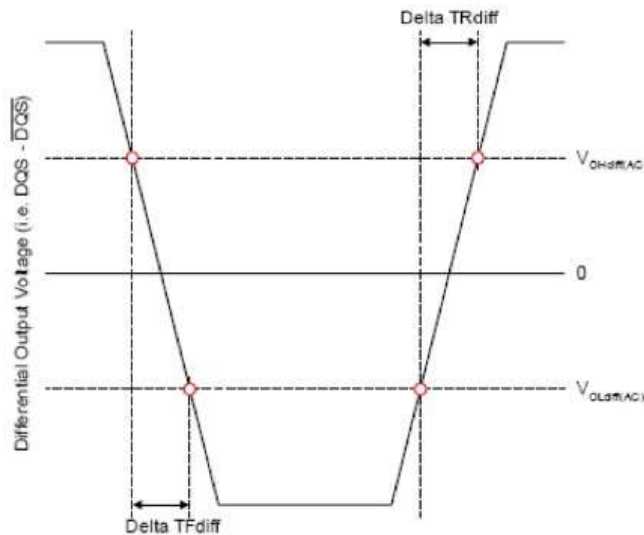
Case 2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 5 V/ns applies.

Differential Output Slew Rate

Differential Output Slew Rate Definition

| Description | Measured | | Defined by |
|--|-------------|-------------|---|
| | From | To | |
| Differential output slew rate for rising edge | VOLdiff(AC) | VOHdiff(AC) | $[VOHdiff(AC) - VOLdiff(AC)] / \Delta TRdiff$ |
| Differential output slew rate for falling edge | VOHdiff(AC) | VOLdiff(AC) | $[VOHdiff(AC) - VOLdiff(AC)] / \Delta TFdiff$ |

Note: Output slew rate is verified by design and characterization, and may not be subject to production test.



Differential Output Slew Rate

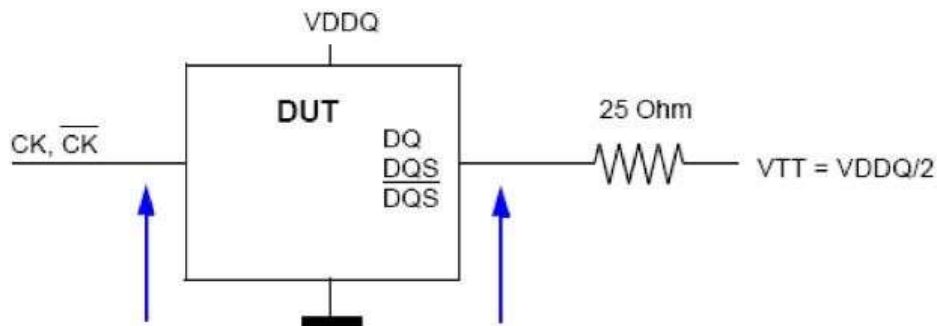
| Parameter | Symbol | DDR3L-1866 | | DDR3-1866 | | Unit |
|-------------------------------|---------|------------|------|-----------|------|------|
| | | Min. | Max. | Min. | Max. | |
| Differential Output Slew Rate | SRQdiff | 3.5 | 12 | 5 | 12 | V/ns |

Description:
 SR: Slew Rate.
 Q: Query Output (like in DQ, which stands for Data-in, Query -Output).
 diff: Differential signals.
 For Ron = Rzq/7 setting

Reference Load for AC Timing and Output Slew Rate

The following figure represents the effective reference load of 25 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.



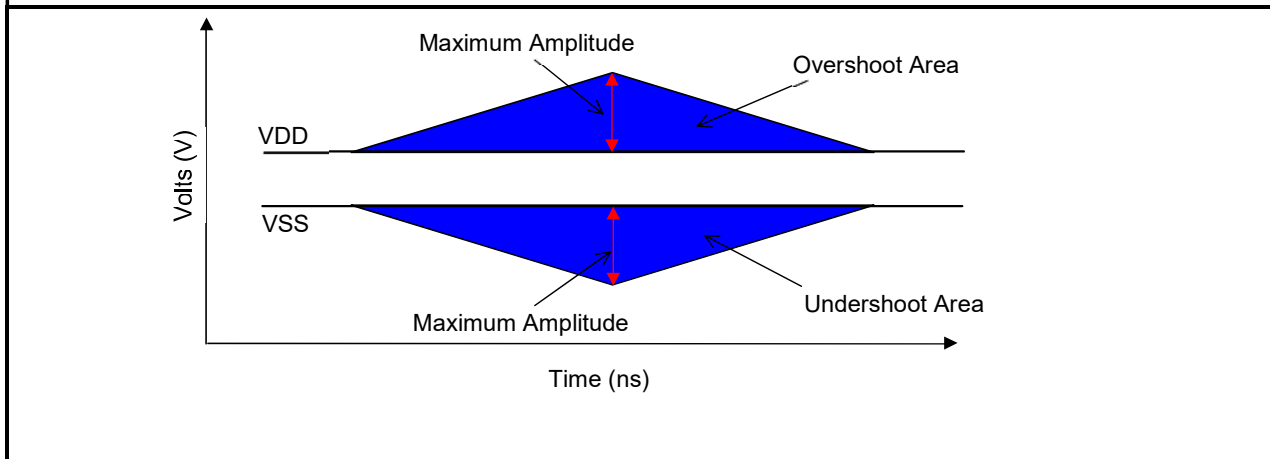
Overshoot and Undershoot Specifications

AC Overshoot/Undershoot Specification for Address and Control Pins

| Item | DDR3(L)-1866 | Unit |
|---|--------------|------|
| Maximum peak amplitude allowed for overshoot area ¹ | 0.4 | V |
| Maximum peak amplitude allowed for undershoot area ² | 0.4 | V |
| Maximum overshoot area above VDD | 0.28 | V-ns |
| Maximum undershoot area below VSS | 0.28 | V-ns |

Note:

1. The sum of the applied voltage (VDD) and peak amplitude overshoot voltage is not to exceed absolute maximum DC ratings.
2. The sum of applied voltage (VDD) and the peak amplitude undershoot voltage is not to exceed absolute maximum DC ratings.

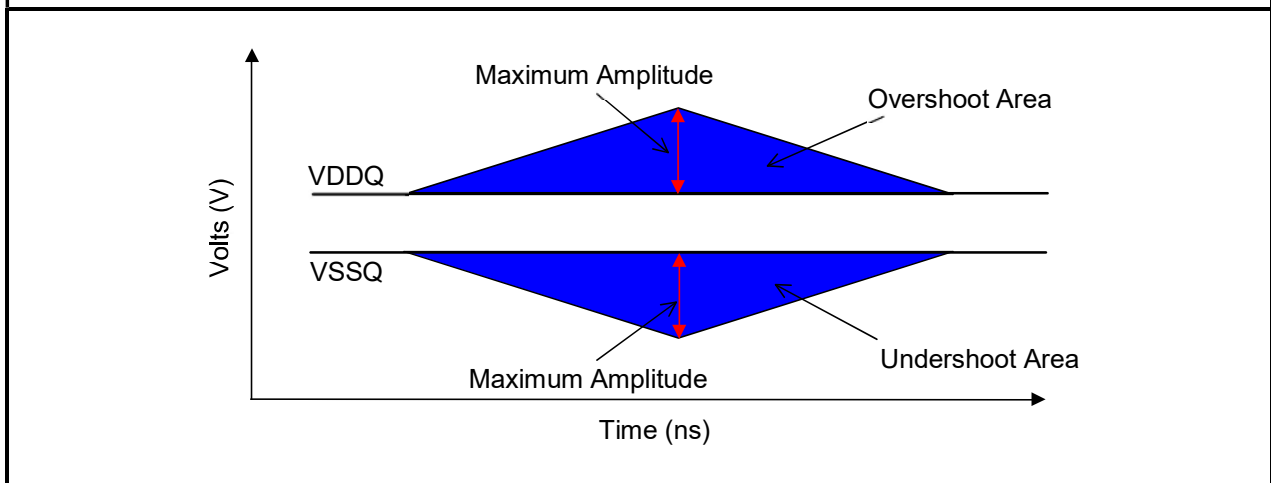


AC Overshoot/Undershoot Specification for Clock, Data, Strobe, and Mask

| Item | DDR3(L)-1866 | Unit |
|---|--------------|------|
| Maximum peak amplitude allowed for overshoot area ¹ | 0.4 | V |
| Maximum peak amplitude allowed for undershoot area ² | 0.4 | V |
| Maximum overshoot area above VDDQ | 0.11 | V-ns |
| Maximum undershoot area below VSSQ | 0.11 | V-ns |

Note:

1. The sum of the applied voltage (VDD) and peak amplitude overshoot voltage is not to exceed absolute maximum DC ratings.
2. The sum of applied voltage (VDD) and the peak amplitude undershoot voltage is not to exceed absolute maximum DC ratings.



34 Ohm Output Driver DC Electrical Characteristics

A Functional representation of the output buffer is shown as below. Output driver impedance R_{ON} is defined by the value of the external reference resistor R_{ZQ} as follows:

$$R_{ON34} = R_{ZQ} / 7 \text{ (nominal 34.4ohms +/-10% with nominal } R_{ZQ}=240\text{ohms)}$$

The individual pull-up and pull-down resistors ($R_{ON_{Pu}}$ and $R_{ON_{Pd}}$) are defined as follows:

$$R_{ON_{Pu}} = [V_{DDQ} - V_{OUT}] / |I_{OUT}| \text{ ----- under the condition that } R_{ON_{Pd}} \text{ is turned off (1)}$$

$$R_{ON_{Pd}} = V_{OUT} / |I_{OUT}| \text{ -----under the condition that } R_{ON_{Pu}} \text{ is turned off (2)}$$

Output Driver: Definition of Voltages and Currents



Output Driver DC Electrical Characteristics, assuming $R_{ZQ} = 240\text{ohms}$; entire operating temperature range; after proper ZQ calibration

| RON _{Nom} | Resistor | V _{OUT} | Min. | Nom. | Max. | Unit | Note |
|--|---------------------|--------------------|------|------|------|---------------------|-------|
| DDR3L | | | | | | | |
| 34 ohms | RON _{34Pd} | VOLdc = 0.2 x VDDQ | 0.6 | 1.0 | 1.15 | R _{ZQ} / 7 | 1,2,3 |
| | | VOMdc = 0.5 x VDDQ | 0.9 | 1.0 | 1.15 | R _{ZQ} / 7 | 1,2,3 |
| | | VOHdc = 0.8 x VDDQ | 0.9 | 1.0 | 1.45 | R _{ZQ} / 7 | 1,2,3 |
| | RON _{34Pu} | VOLdc = 0.2 x VDDQ | 0.9 | 1.0 | 1.45 | R _{ZQ} / 7 | 1,2,3 |
| | | VOMdc = 0.5 x VDDQ | 0.9 | 1.0 | 1.15 | R _{ZQ} / 7 | 1,2,3 |
| | | VOHdc = 0.8 x VDDQ | 0.6 | 1.0 | 1.15 | R _{ZQ} / 7 | 1,2,3 |
| 40 ohms | RON _{40pd} | VOLdc = 0.2 x VDDQ | 0.6 | 1.0 | 1.15 | R _{ZQ} / 6 | 1,2,3 |
| | | VOMdc = 0.5 x VDDQ | 0.9 | 1.0 | 1.15 | R _{ZQ} / 6 | 1,2,3 |
| | | VOHdc = 0.8 x VDDQ | 0.9 | 1.0 | 1.45 | R _{ZQ} / 6 | 1,2,3 |
| | RON _{40pu} | VOLdc = 0.2 x VDDQ | 0.9 | 1.0 | 1.45 | R _{ZQ} / 6 | 1,2,3 |
| | | VOMdc = 0.5 x VDDQ | 0.9 | 1.0 | 1.15 | R _{ZQ} / 6 | 1,2,3 |
| | | VOHdc = 0.8 x VDDQ | 0.6 | 1.0 | 1.15 | R _{ZQ} / 6 | 1,2,3 |
| Mismatch between pull-up and pull-down, MM _{PuPd} | | VOMdc = 0.5 x VDDQ | -10 | | +10 | % | 1,2,4 |
| DDR3 | | | | | | | |
| 34 ohms | RON _{34Pd} | VOLdc = 0.2 x VDDQ | 0.6 | 1.0 | 1.1 | R _{ZQ} / 7 | 1,2,3 |
| | | VOMdc = 0.5 x VDDQ | 0.9 | 1.0 | 1.1 | R _{ZQ} / 7 | 1,2,3 |
| | | VOHdc = 0.8 x VDDQ | 0.9 | 1.0 | 1.4 | R _{ZQ} / 7 | 1,2,3 |
| | RON _{34Pu} | VOLdc = 0.2 x VDDQ | 0.9 | 1.0 | 1.4 | R _{ZQ} / 7 | 1,2,3 |
| | | VOMdc = 0.5 x VDDQ | 0.9 | 1.0 | 1.1 | R _{ZQ} / 7 | 1,2,3 |
| | | VOHdc = 0.8 x VDDQ | 0.6 | 1.0 | 1.1 | R _{ZQ} / 7 | 1,2,3 |
| 40 ohms | RON _{40pd} | VOLdc = 0.2 x VDDQ | 0.6 | 1.0 | 1.1 | R _{ZQ} / 6 | 1,2,3 |
| | | VOMdc = 0.5 x VDDQ | 0.9 | 1.0 | 1.1 | R _{ZQ} / 6 | 1,2,3 |
| | | VOHdc = 0.8 x VDDQ | 0.9 | 1.0 | 1.4 | R _{ZQ} / 6 | 1,2,3 |
| | RON _{40pu} | VOLdc = 0.2 x VDDQ | 0.9 | 1.0 | 1.4 | R _{ZQ} / 6 | 1,2,3 |
| | | VOMdc = 0.5 x VDDQ | 0.9 | 1.0 | 1.1 | R _{ZQ} / 6 | 1,2,3 |
| | | VOHdc = 0.8 x VDDQ | 0.6 | 1.0 | 1.1 | R _{ZQ} / 6 | 1,2,3 |
| Mismatch between pull-up and pull-down, MM _{PuPd} | | VOMdc = 0.5 x VDDQ | -10 | | +10 | % | 1,2,4 |

Note:

- The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
- The tolerance limits are specified under the condition that VDDQ = VDD and that VSSQ = VSS.
- Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 x VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above. e.g. calibration at 0.2 x VDDQ and 0.8 x VDDQ.
- Measurement definition for mismatch between pull-up and pull-down, MM_{PuPd}:

 Measure RON_{Pu} and RON_{Pd}, both at 0.5 x VDDQ:

$$MM_{PuPd} = [RON_{Pu} - RON_{Pd}] / RON_{Nom} \times 100$$

Output Driver Temperature and Voltage sensitivity

If temperature and/or voltage after calibration, the tolerance limits widen according to the following table.

$\Delta T = T - T(@\text{calibration})$; $\Delta V = VDDQ - VDDQ(@\text{calibration})$; $VDD = VDDQ$

Note: dRONdT and dRONdV are not subject to production test but are verified by design and characterization.

Output Driver Sensitivity Definition

| Items | Min. | Max. | Unit |
|------------------|---|---|------------|
| $RON_{PU}@VOHdc$ | $0.6 - dRONdTH * \Delta T - dRONdVH * \Delta V$ | $1.1 + dRONdTH * \Delta T - dRONdVH * \Delta V$ | $R_{ZQ}/7$ |
| $RON@VOMdc$ | $0.9 - dRONdTM * \Delta T - dRONdVM * \Delta V$ | $1.1 + dRONdTM * \Delta T - dRONdVM * \Delta V$ | $R_{ZQ}/7$ |
| $RON_{PD}@VOLdc$ | $0.6 - dRONdTL * \Delta T - dRONdVL * \Delta V$ | $1.1 + dRONdTL * \Delta T - dRONdVL * \Delta V$ | $R_{ZQ}/7$ |

Output Driver Voltage and Temperature Sensitivity

| Speed Bin | DDR3(L)-1866 | | Unit |
|-----------|--------------|------|------|
| Items | Min. | Max. | |
| dRONdTM | 0 | 1.5 | %/°C |
| dRONdVM | 0 | 0.13 | %/mV |
| dRONdTL | 0 | 1.5 | %/°C |
| dRONdVL | 0 | 0.13 | %/mV |
| dRONdTH | 0 | 1.5 | %/°C |
| dRONdVH | 0 | 0.13 | %/mV |

Note: These parameters may not be subject to production test. They are verified by design and characterization.

On-Die Termination (ODT) Levels and I-V Characteristics

On-Die Termination effective resistance R_{TT} is defined by bits A9, A6, and A2 of the MR1 Register.

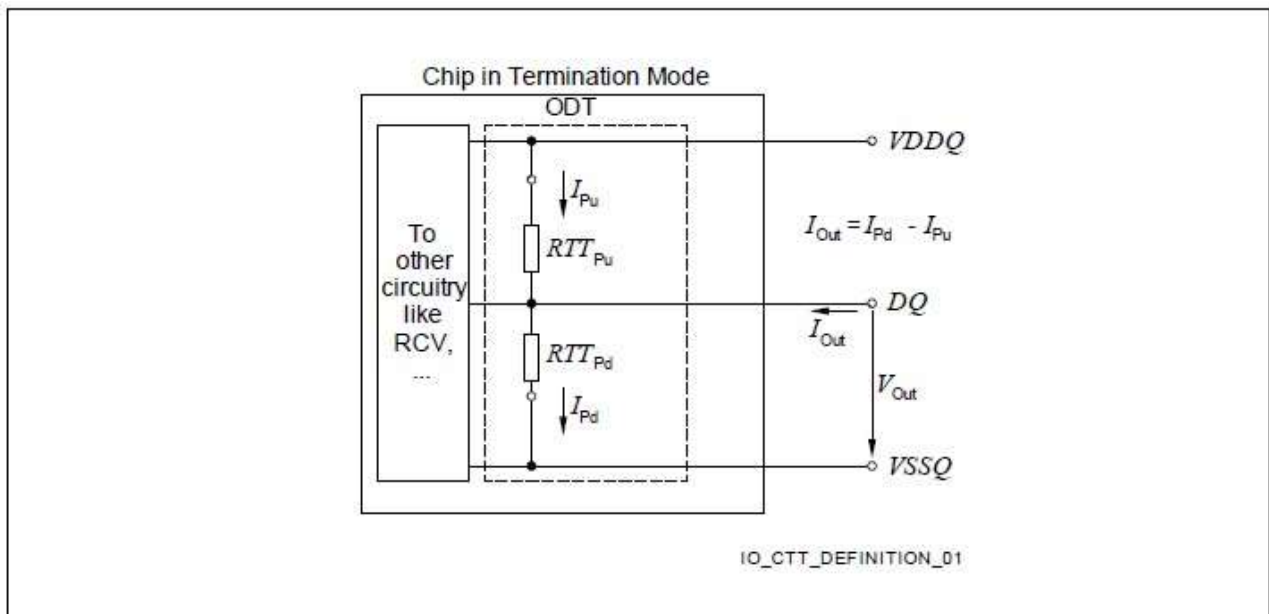
ODT is applied to the DQ, DM, DQS/ \overline{DQS} pins.

A functional representation of the on-die termination is shown in the following figure. The individual pull-up and pull-down resistors ($R_{TT_{Pu}}$ and $R_{TT_{Pd}}$) are defined as follows:

$$R_{TT_{Pu}} = [V_{DDQ} - V_{OUT}] / |I_{OUT}| \text{ ----- under the condition that } R_{TT_{Pd}} \text{ is turned off (3)}$$

$$R_{TT_{Pd}} = V_{OUT} / |I_{OUT}| \text{ ----- under the condition that } R_{TT_{Pu}} \text{ is turned off (4)}$$

On-Die Termination: Definition of Voltages and Currents



ODT DC Electrical Characteristics

The following table provides an overview of the ODT DC electrical characteristics. The values for $R_{TT_{60Pd120}}$, $R_{TT_{60Pu120}}$, $R_{TT_{120Pd240}}$, $R_{TT_{120Pu240}}$, $R_{TT_{40Pd80}}$, $R_{TT_{40Pu80}}$, $R_{TT_{30Pd60}}$, $R_{TT_{30Pu60}}$, $R_{TT_{20Pd40}}$, $R_{TT_{20Pu40}}$ are not specification requirements, but can be used as design guide lines:

ODT DC Electrical Characteristics, assuming $R_{ZQ} = 240\text{ohms} \pm 1\%$ entire operating temperature range; after proper ZQ calibration

| DDR3L | | | | | | | | | | |
|------------------------|--------------------|---|--------------------|------------------------|--------------------|------|---------------------|---------|--------------------|---------|
| MR1 A9,A6,A2 | RTT | Resistor | V _{OUT} | Min. | Nom. | Max. | Unit | Note | | |
| 0,1,0 | 120Ω | RTT _{120Pd240} | VOLdc = 0.2 x VDDQ | 0.6 | 1 | 1.15 | R _{ZQ} | 1,2,3,4 | | |
| | | | 0.5 x VDDQ | 0.9 | 1 | 1.15 | R _{ZQ} | 1,2,3,4 | | |
| | | | VOHdc = 0.8 x VDDQ | 0.9 | 1 | 1.45 | R _{ZQ} | 1,2,3,4 | | |
| | | RTT _{120Pu240} | VOLdc = 0.2 x VDDQ | 0.9 | 1 | 1.45 | R _{ZQ} | 1,2,3,4 | | |
| | | | 0.5 x VDDQ | 0.9 | 1 | 1.15 | R _{ZQ} | 1,2,3,4 | | |
| | | | VOHdc = 0.8 x VDDQ | 0.6 | 1 | 1.15 | R _{ZQ} | 1,2,3,4 | | |
| | | RTT ₁₂₀ | VIL(AC) to VIH(AC) | 0.9 | 1 | 1.65 | R _{ZQ} /2 | 1,2,5 | | |
| | | 0, 0, 1 | 60Ω | RTT _{60Pd120} | VOLdc = 0.2 x VDDQ | 0.6 | 1 | 1.15 | R _{ZQ} /2 | 1,2,3,4 |
| | | | | | 0.5 x VDDQ | 0.9 | 1 | 1.15 | R _{ZQ} /2 | 1,2,3,4 |
| VOHdc = 0.8 x VDDQ | 0.9 | | | | 1 | 1.45 | R _{ZQ} /2 | 1,2,3,4 | | |
| RTT _{60Pu120} | VOLdc = 0.2 x VDDQ | | | 0.9 | 1 | 1.45 | R _{ZQ} /2 | 1,2,3,4 | | |
| | 0.5 x VDDQ | | | 0.9 | 1 | 1.15 | R _{ZQ} /2 | 1,2,3,4 | | |
| | VOHdc = 0.8 x VDDQ | | | 0.6 | 1 | 1.15 | R _{ZQ} /2 | 1,2,3,4 | | |
| RTT ₆₀ | VIL(AC) to VIH(AC) | | | 0.9 | 1 | 1.65 | R _{ZQ} /4 | 1,2,5 | | |
| 0, 1, 1 | 40Ω | | | RTT _{40Pd80} | VOLdc = 0.2 x VDDQ | 0.6 | 1 | 1.15 | R _{ZQ} /3 | 1,2,3,4 |
| | | | | | 0.5 x VDDQ | 0.9 | 1 | 1.15 | R _{ZQ} /3 | 1,2,3,4 |
| | | VOHdc = 0.8 x VDDQ | 0.9 | | 1 | 1.45 | R _{ZQ} /3 | 1,2,3,4 | | |
| | | RTT _{40Pu80} | VOLdc = 0.2 x VDDQ | 0.9 | 1 | 1.45 | R _{ZQ} /3 | 1,2,3,4 | | |
| | | | 0.5 x VDDQ | 0.9 | 1 | 1.15 | R _{ZQ} /3 | 1,2,3,4 | | |
| | | | VOHdc = 0.8 x VDDQ | 0.6 | 1 | 1.15 | R _{ZQ} /3 | 1,2,3,4 | | |
| | | RTT ₄₀ | VIL(AC) to VIH(AC) | 0.9 | 1 | 1.65 | R _{ZQ} /6 | 1,2,5 | | |
| | | 1, 0, 1 | 30Ω | RTT _{30Pd60} | VOLdc = 0.2 x VDDQ | 0.6 | 1 | 1.15 | R _{ZQ} /4 | 1,2,3,4 |
| | | | | | 0.5 x VDDQ | 0.9 | 1 | 1.15 | R _{ZQ} /4 | 1,2,3,4 |
| VOHdc = 0.8 x VDDQ | 0.9 | | | | 1 | 1.45 | R _{ZQ} /4 | 1,2,3,4 | | |
| RTT _{30Pu60} | VOLdc = 0.2 x VDDQ | | | 0.9 | 1 | 1.45 | R _{ZQ} /4 | 1,2,3,4 | | |
| | 0.5 x VDDQ | | | 0.9 | 1 | 1.15 | R _{ZQ} /4 | 1,2,3,4 | | |
| | VOHdc = 0.8 x VDDQ | | | 0.6 | 1 | 1.15 | R _{ZQ} /4 | 1,2,3,4 | | |
| RTT ₃₀ | VIL(AC) to VIH(AC) | | | 0.9 | 1 | 1.65 | R _{ZQ} /8 | 1,2,5 | | |
| 1, 0, 0 | 20Ω | | | RTT _{20Pd40} | VOLdc = 0.2 x VDDQ | 0.6 | 1 | 1.15 | R _{ZQ} /6 | 1,2,3,4 |
| | | | | | 0.5 x VDDQ | 0.9 | 1 | 1.15 | R _{ZQ} /6 | 1,2,3,4 |
| | | VOHdc = 0.8 x VDDQ | 0.9 | | 1 | 1.45 | R _{ZQ} /6 | 1,2,3,4 | | |
| | | RTT _{20Pu40} | VOLdc = 0.2 x VDDQ | 0.9 | 1 | 1.45 | R _{ZQ} /6 | 1,2,3,4 | | |
| | | | 0.5 x VDDQ | 0.9 | 1 | 1.15 | R _{ZQ} /6 | 1,2,3,4 | | |
| | | | VOHdc = 0.8 x VDDQ | 0.6 | 1 | 1.15 | R _{ZQ} /6 | 1,2,3,4 | | |
| | | RTT ₂₀ | VIL(AC) to VIH(AC) | 0.9 | 1 | 1.65 | R _{ZQ} /12 | 1,2,5 | | |
| | | Deviation of V _M w.r.t. VDDQ/2, Delta V _M | | | | -5 | | +5 | % | 1,2,5,6 |

| DDR3 | | | | | | | | |
|---|--------------------|-------------------------|--------------------|------|---------------------|-------|--------------------|---------|
| MR1 A9,A6,A2 | RTT | Resistor | V _{OUT} | Min. | Nom. | Max. | Unit | Note |
| 0, 1, 0 | 120Ω | RTT _{120Pd240} | VOLdc = 0.2 x VDDQ | 0.6 | 1 | 1.1 | R _{ZQ} | 1,2,3,4 |
| | | | 0.5 x VDDQ | 0.9 | 1 | 1.1 | R _{ZQ} | 1,2,3,4 |
| | | | VOHdc = 0.8 x VDDQ | 0.9 | 1 | 1.4 | R _{ZQ} | 1,2,3,4 |
| | | RTT _{120Pu240} | VOLdc = 0.2 x VDDQ | 0.9 | 1 | 1.4 | R _{ZQ} | 1,2,3,4 |
| | | | 0.5 x VDDQ | 0.9 | 1 | 1.1 | R _{ZQ} | 1,2,3,4 |
| | | | VOHdc = 0.8 x VDDQ | 0.6 | 1 | 1.1 | R _{ZQ} | 1,2,3,4 |
| RTT ₁₂₀ | VIL(AC) to VIH(AC) | 0.9 | 1 | 1.6 | R _{ZQ} /2 | 1,2,5 | | |
| 0, 0, 1 | 60Ω | RTT _{60Pd120} | VOLdc = 0.2 x VDDQ | 0.6 | 1 | 1.1 | R _{ZQ} /2 | 1,2,3,4 |
| | | | 0.5 x VDDQ | 0.9 | 1 | 1.1 | R _{ZQ} /2 | 1,2,3,4 |
| | | | VOHdc = 0.8 x VDDQ | 0.9 | 1 | 1.4 | R _{ZQ} /2 | 1,2,3,4 |
| | | RTT _{60Pu120} | VOLdc = 0.2 x VDDQ | 0.9 | 1 | 1.4 | R _{ZQ} /2 | 1,2,3,4 |
| | | | 0.5 x VDDQ | 0.9 | 1 | 1.1 | R _{ZQ} /2 | 1,2,3,4 |
| | | | VOHdc = 0.8 x VDDQ | 0.6 | 1 | 1.1 | R _{ZQ} /2 | 1,2,3,4 |
| RTT ₆₀ | VIL(AC) to VIH(AC) | 0.9 | 1 | 1.6 | R _{ZQ} /4 | 1,2,5 | | |
| 0, 1, 1 | 40Ω | RTT _{40Pd80} | VOLdc = 0.2 x VDDQ | 0.6 | 1 | 1.1 | R _{ZQ} /3 | 1,2,3,4 |
| | | | 0.5 x VDDQ | 0.9 | 1 | 1.1 | R _{ZQ} /3 | 1,2,3,4 |
| | | | VOHdc = 0.8 x VDDQ | 0.9 | 1 | 1.4 | R _{ZQ} /3 | 1,2,3,4 |
| | | RTT _{40Pu80} | VOLdc = 0.2 x VDDQ | 0.9 | 1 | 1.4 | R _{ZQ} /3 | 1,2,3,4 |
| | | | 0.5 x VDDQ | 0.9 | 1 | 1.1 | R _{ZQ} /3 | 1,2,3,4 |
| | | | VOHdc = 0.8 x VDDQ | 0.6 | 1 | 1.1 | R _{ZQ} /3 | 1,2,3,4 |
| RTT ₄₀ | VIL(AC) to VIH(AC) | 0.9 | 1 | 1.6 | R _{ZQ} /6 | 1,2,5 | | |
| 1, 0, 1 | 30Ω | RTT _{30Pd60} | VOLdc = 0.2 x VDDQ | 0.6 | 1 | 1.1 | R _{ZQ} /4 | 1,2,3,4 |
| | | | 0.5 x VDDQ | 0.9 | 1 | 1.1 | R _{ZQ} /4 | 1,2,3,4 |
| | | | VOHdc = 0.8 x VDDQ | 0.9 | 1 | 1.4 | R _{ZQ} /4 | 1,2,3,4 |
| | | RTT _{30Pu60} | VOLdc = 0.2 x VDDQ | 0.9 | 1 | 1.4 | R _{ZQ} /4 | 1,2,3,4 |
| | | | 0.5 x VDDQ | 0.9 | 1 | 1.1 | R _{ZQ} /4 | 1,2,3,4 |
| | | | VOHdc = 0.8 x VDDQ | 0.6 | 1 | 1.1 | R _{ZQ} /4 | 1,2,3,4 |
| RTT ₃₀ | VIL(AC) to VIH(AC) | 0.9 | 1 | 1.6 | R _{ZQ} /8 | 1,2,5 | | |
| 1, 0, 0 | 20Ω | RTT _{20Pd40} | VOLdc = 0.2 x VDDQ | 0.6 | 1 | 1.1 | R _{ZQ} /6 | 1,2,3,4 |
| | | | 0.5 x VDDQ | 0.9 | 1 | 1.1 | R _{ZQ} /6 | 1,2,3,4 |
| | | | VOHdc = 0.8 x VDDQ | 0.9 | 1 | 1.4 | R _{ZQ} /6 | 1,2,3,4 |
| | | RTT _{20Pu40} | VOLdc = 0.2 x VDDQ | 0.9 | 1 | 1.4 | R _{ZQ} /6 | 1,2,3,4 |
| | | | 0.5 x VDDQ | 0.9 | 1 | 1.1 | R _{ZQ} /6 | 1,2,3,4 |
| | | | VOHdc = 0.8 x VDDQ | 0.6 | 1 | 1.1 | R _{ZQ} /6 | 1,2,3,4 |
| RTT ₂₀ | VIL(AC) to VIH(AC) | 0.9 | 1 | 1.6 | R _{ZQ} /12 | 1,2,5 | | |
| Deviation of V _M w.r.t. VDDQ/2, Delta V _M | | | | -5 | | +5 | % | 1,2,5,6 |

Note:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. The tolerance limits are specified under the condition that VDDQ = VDD and that VSSQ = VSS.
3. Pull-down and pull-up ODT resistors are recommended to be calibrated at 0.5 x VDDQ. Other calibration may be used to achieve the linearity spec shown above.
4. Not a specification requirement, but a design guide line.
5. Measurement definition for RTT:
Apply VIH(AC) to pin under test and measure current I(VIH(AC)), then apply VIL(AC) to pin under test and measure current I(VIL(AC)) respectively.
$$RTT = [VIH(AC) - VIL(AC)] / [I(VIH(AC)) - I(VIL(AC))]$$
6. Measurement definition for VM and Delta VM:
Measure voltage (VM) at test pin (midpoint) with no lead: $\Delta V_M = [2V_M / VDDQ - 1] \times 100$

ODT Temperature and Voltage sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the following table.

$\Delta T = T - T(@\text{calibration})$; $\Delta V = VDDQ - VDDQ(@\text{calibration})$; $VDD = VDDQ$

ODT Sensitivity Definition

| Symbol | Min. | Max. | Unit |
|--------|---|---|----------------|
| RTT | $0.9 - dRTTdT * \Delta T - dRTTdV * \Delta V$ | $1.6 + dRTTdT * \Delta T + dRTTdV * \Delta V$ | RZQ/2,4,6,8,12 |

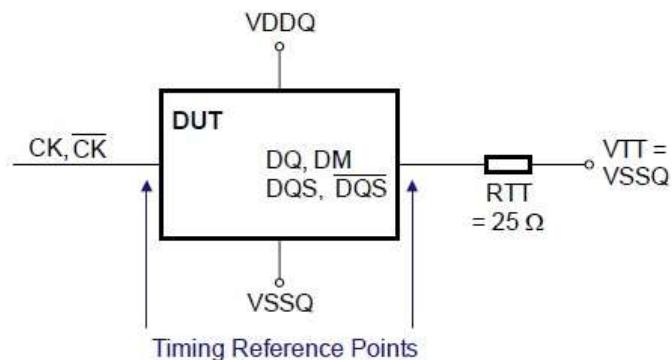
ODT Voltage and Temperature Sensitivity

| Symbol | Min. | Max. | Unit |
|--------|------|------|------|
| dRTTdT | 0 | 1.5 | %/°C |
| dRTTdV | 0 | 0.15 | %/mV |

Note: These parameters may not be subject to production test. They are verified by design and characterization.

ODT Timing Definitions
Test Load for ODT Timings

Different than for timing measurements, the reference load for ODT timings is defined in the following figure.

ODT Timing Reference Load


ODT Timing Definitions

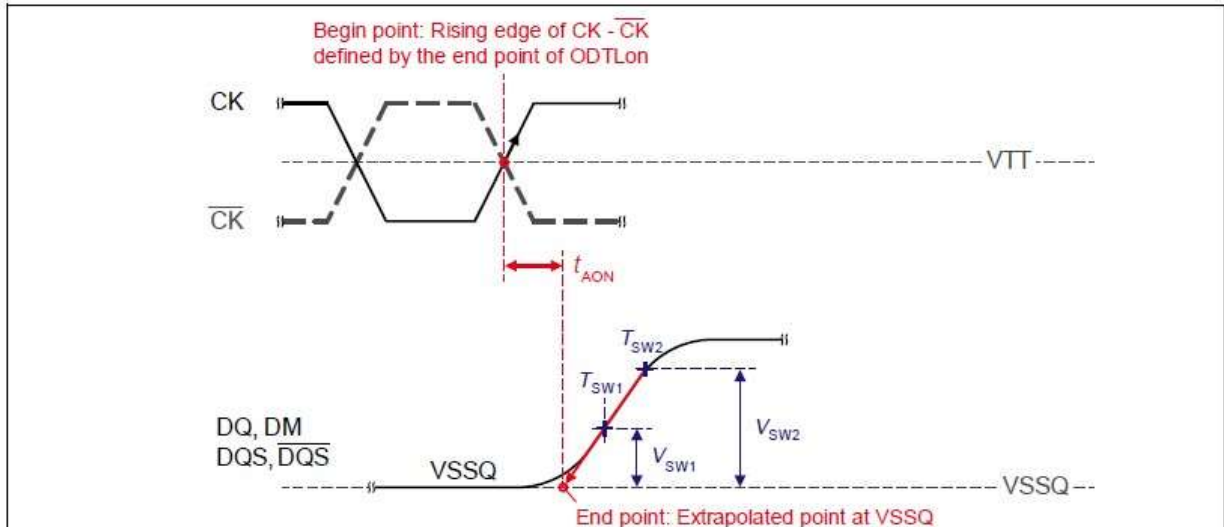
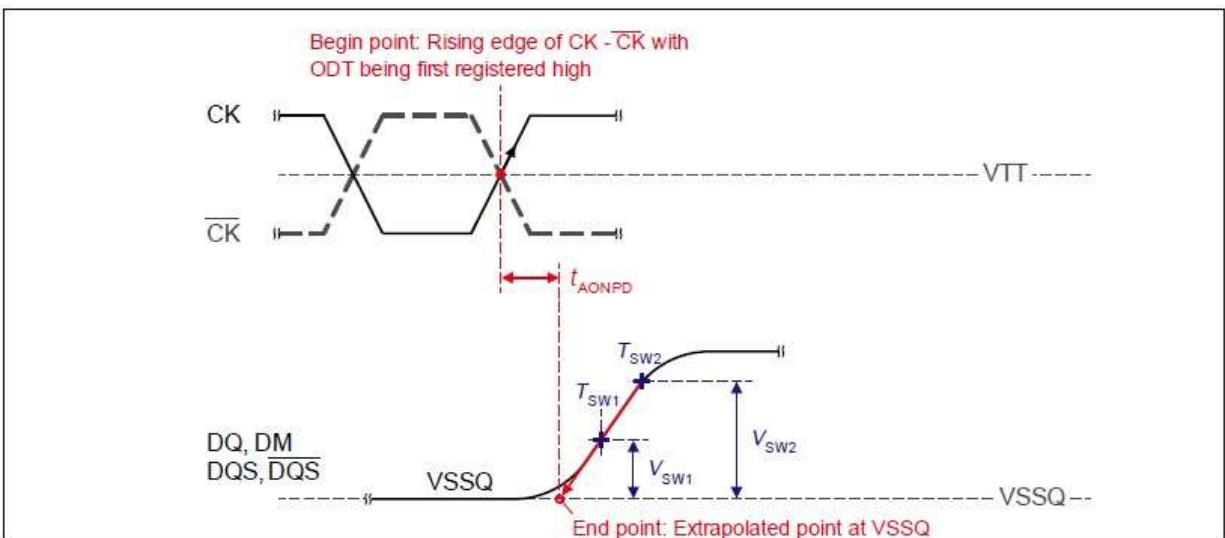
Definitions for tAON, tAONPD, tAOF, tAOFPD, and tADC are provided in the following table and subsequent figures.

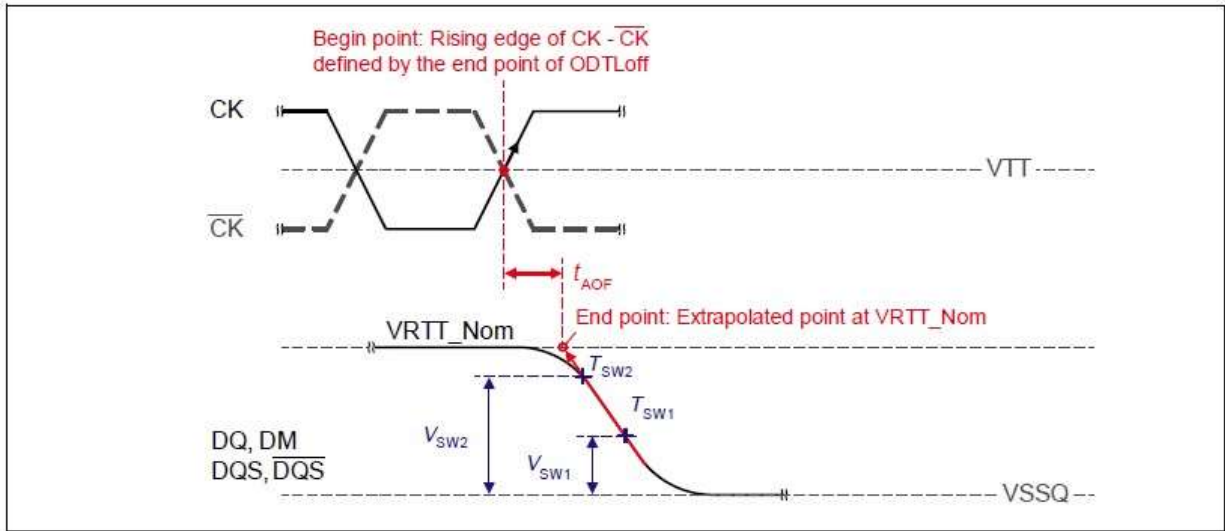
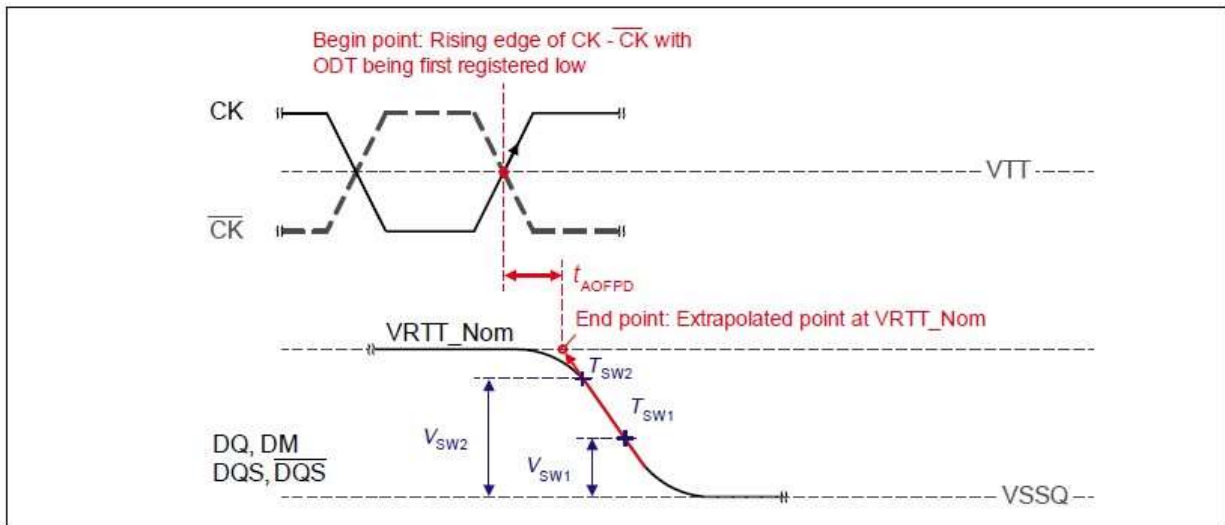
| Symbol | Begin Point Definition | End Point Definition |
|--------|--|--|
| tAON | Rising edge of CK - \overline{CK} defined by the end point of ODTLon | Extrapolated point at VSSQ |
| tAONPD | Rising edge of CK - \overline{CK} with ODT being first registered high | Extrapolated point at VSSQ |
| tAOF | Rising edge of CK - \overline{CK} defined by the end point of ODTLoff | End point: Extrapolated point at VRTT_Nom |
| tAOFPD | Rising edge of CK - \overline{CK} with ODT being first registered low | End point: Extrapolated point at VRTT_Nom |
| tADC | Rising edge of CK - \overline{CK} defined by the end point of ODTLcnw, ODTLcwn4, or ODTLcwn8 | End point: Extrapolated point at VRTT_Wr and VRTT_Nom respectively |

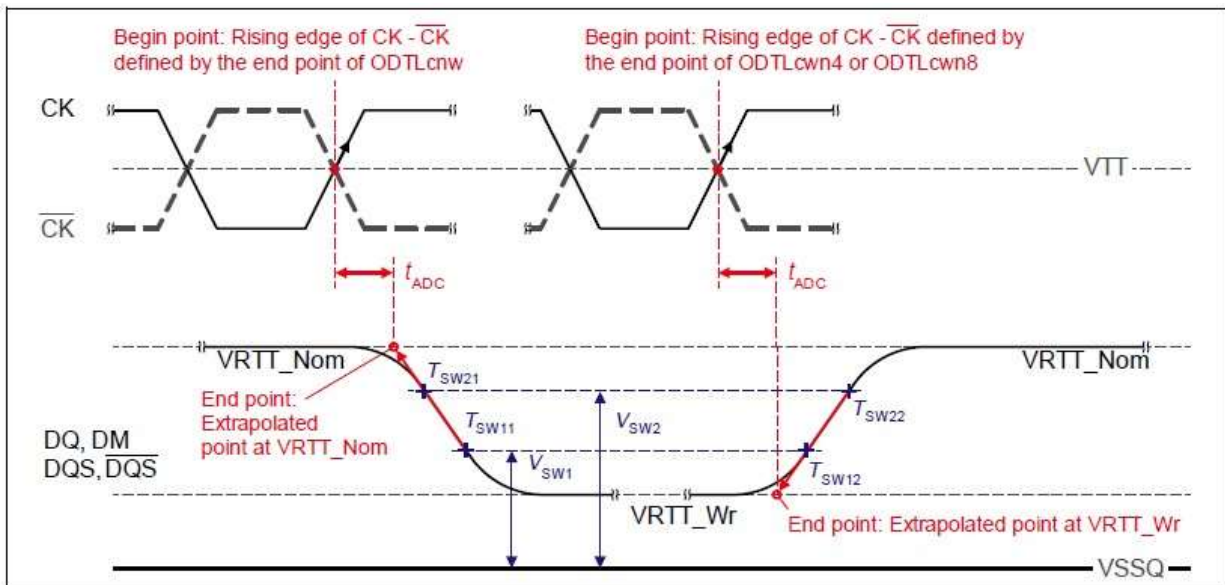
Reference Settings for ODT Timing Measurements

| DDR3 | | | | | |
|--------------------|-----------------|----------------|----------------------|----------------------|------|
| Measured Parameter | RTT_Nom Setting | RTT_Wr Setting | V _{sw1} [V] | V _{sw2} [V] | Note |
| tAON | RZQ/4 | NA | 0.05 | 0.10 | |
| | RZQ/12 | NA | 0.10 | 0.20 | |
| tAONPD | RZQ/4 | NA | 0.05 | 0.10 | |
| | RZQ/12 | NA | 0.10 | 0.20 | |
| tAOF | RZQ/4 | NA | 0.05 | 0.10 | |
| | RZQ/12 | NA | 0.10 | 0.20 | |
| tAOFPD | RZQ/4 | NA | 0.05 | 0.10 | |
| | RZQ/12 | NA | 0.10 | 0.20 | |
| tADC | RZQ/12 | RZQ/2 | 0.20 | 0.30 | |

| DDR3L | | | | | |
|--------------------|-----------------|----------------|----------------------|----------------------|------|
| Measured Parameter | RTT_Nom Setting | RTT_Wr Setting | V _{sw1} [V] | V _{sw2} [V] | Note |
| tAON | RZQ/4 | NA | 0.05 | 0.10 | |
| | RZQ/12 | NA | 0.10 | 0.20 | |
| tAONPD | RZQ/4 | NA | 0.05 | 0.10 | |
| | RZQ/12 | NA | 0.10 | 0.20 | |
| tAOF | RZQ/4 | NA | 0.05 | 0.10 | |
| | RZQ/12 | NA | 0.10 | 0.20 | |
| tAOFPD | RZQ/4 | NA | 0.05 | 0.10 | |
| | RZQ/12 | NA | 0.10 | 0.20 | |
| tADC | RZQ/12 | RZQ/2 | 0.20 | 0.25 | |

Definition of t_{AON}

Definition of t_{AONPD}


Definition of t_{AOF}

Definition of t_{AOFPD}


Definition of t_{ADC}


Input / Output Capacitance

| Symbol | Parameter | 1866 | | Unit | Note |
|--------------------|--|------|------|------|----------|
| | | Min. | Max | | |
| C_{IO} (DDR3) | Input/output capacitance (DQ, DM, DQS, \overline{DQS}) | 1.4 | 2.2 | pF | 1,2,3 |
| C_{IO} (DDR3L) | | 1.4 | 2.1 | | |
| C_{CK} | Input capacitance, CK and \overline{CK} | 0.8 | 1.3 | pF | 2,3 |
| C_{DCK} | Input capacitance delta, CK and \overline{CK} | 0 | 0.15 | pF | 2,3,4 |
| C_{DDQS} | Input/output capacitance delta, DQS and \overline{DQS} | 0 | 0.15 | pF | 2,3,5 |
| C_I (DDR3) | Input capacitance, CTRL, ADD, CMD input-only pins | 0.75 | 1.2 | pF | 2,3,6 |
| C_I (DDR3L) | | 0.75 | 1.2 | | |
| C_{DI_CTRL} | Input capacitance delta, all CTRL input-only pins | -0.4 | 0.2 | pF | 2,3,7,8 |
| $C_{DI_ADD_CMD}$ | Input capacitance delta, all ADD/CMD input-only pins | -0.4 | 0.4 | pF | 2,3,9,10 |
| C_{DIO} | Input/output capacitance delta, DQ, DM, DQS, \overline{DQS} | -0.5 | 0.3 | pF | 2,3,11 |
| C_{ZQ} | Input/output capacitance of ZQ pin | - | 3 | pF | 2,3,12 |

Note:

1. Although the DM pin has different functions, the loading matches DQ and DQS.
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 ("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)") with VDD, VDDQ, VSS, VSSQ applied and all other pins floating (except the pin under test, CKE, RESET and ODT as necessary). VDD=VDDQ=1.5V for DDR3 / 1.35V for DDR3L, VBIAS=VDD/2 and on-die termination off.
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here.
4. Absolute value of $C_{CK}-C_{\overline{CK}}$.
5. Absolute value of $C_{IO}(DQS)-C_{IO}(\overline{DQS})$.
6. C_I applies to ODT, CS, CKE, A0-A14, BA0-BA2, \overline{RAS} , \overline{CAS} , \overline{WE} .
7. C_{DI_CTRL} applies to ODT, \overline{CS} and CKE.
8. $C_{DI_CTRL}=C_I(CTRL)-0.5*(C_I(CLK)+C_I(\overline{CLK}))$.
9. $C_{DI_ADD_CMD}$ applies to A0-A14, BA0-BA2, \overline{RAS} , \overline{CAS} and \overline{WE} .
10. $C_{DI_ADD_CMD}=C_I(ADD_CMD) - 0.5*(C_I(CLK)+C_I(\overline{CLK}))$.
11. $C_{DIO}=C_{IO}(DQ,DM) - 0.5*(C_{IO}(DQS)+C_{IO}(\overline{DQS}))$.
12. Maximum external load capacitance on ZQ pin: 5 pF.

IDD and IDDQ Specification Parameters and Test Conditions

IDD and IDDQ Measurement Conditions

In this chapter, IDD and IDDQ measurement conditions such as test load and patterns are defined. The following figure shows the setup and test load for IDD and IDDQ measurements.

- **IDD currents** (such as IDD0, IDD1, IDD2N, IDD2NT, IDD2P0, IDD2P1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6, IDD6ET, IDD6TC and IDD7) are measured as time-averaged currents with all VDD balls of the DDR3(L) SDRAM under test tied together. Any IDDQ current is not included in IDD currents.
- **IDDQ currents** (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR3(L) SDRAM under test tied together. Any IDD current is not included in IDDQ currents.

Attention: IDDQ values cannot be directly used to calculate IO power of the DDR3(L) SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in following figure. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

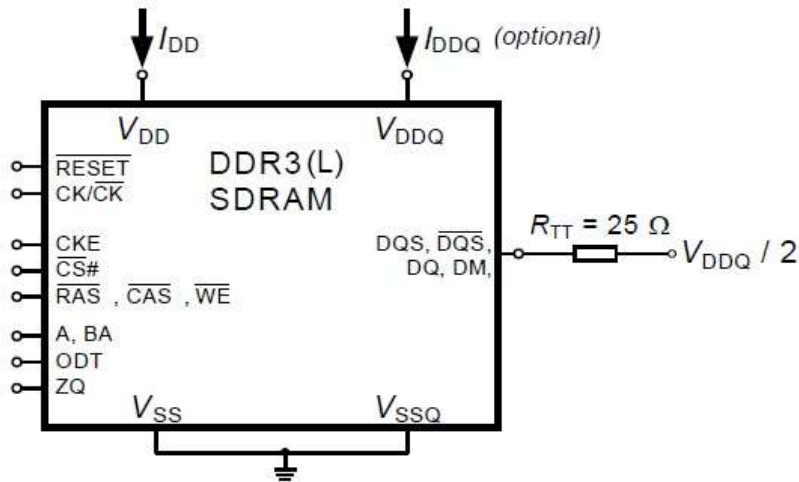
For IDD and IDDQ measurements, the following definitions apply:

- “0” and “LOW” is defined as $V_{IN} \leq V_{ILAC}(\max)$.
- “1” and “HIGH” is defined as $V_{IN} \geq V_{IHAC}(\min)$. • “MID-LEVEL” is defined as inputs are $V_{REF} = V_{DD} / 2$.
- Timings used for IDD and IDDQ Measurement-Loop Patterns are provided in “Timings used for IDD and IDDQ Measurement-Loop Patterns” Table.
- Basic IDD and IDDQ Measurement Conditions are described in “Basic IDD and IDDQ Measurement Conditions” Table.
- Detailed IDD and IDDQ Measurement-Loop Patterns are described in “IDDx Measurement-Loop Pattern” Tables.
- IDD Measurements are done after properly initializing the DDR3(L) SDRAM. This includes but is not limited to setting $R_{ON} = R_{ZQ}/7$ (34 Ohm in MR1);
 $Q_{off} = 0B$ (Output Buffer enabled in MR1);
 $R_{TT_Nom} = R_{ZQ}/6$ (40 Ohm in MR1);
 $R_{TT_Wr} = R_{ZQ}/2$ (120 Ohm in MR2);

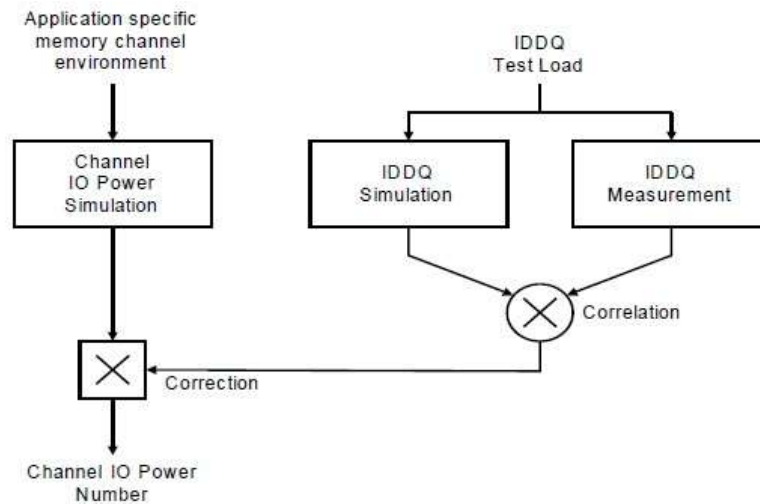
Attention: The IDD and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.

Define D = { \overline{CS} , \overline{RAS} , \overline{CAS} , \overline{WE} } := {HIGH, LOW, LOW, LOW}

Define D# = { \overline{CS} , \overline{RAS} , \overline{CAS} , \overline{WE} } := {HIGH, HIGH, HIGH, HIGH}

Measurement Setup and Test Load for IDD and IDDQ Measurements


Note: DIMM level Output test load condition may be different from above.

Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement.


Timings used for IDD and IDDQ Measurement-Loop Patterns

| Symbol | DDR3(L)-1866 (13-13-13) | Unit |
|--------|-------------------------|------|
| tCK | 1.071 | ns |
| CL | 13 | nCK |
| nRCD | 13 | nCK |
| nRC | 45 | nCK |
| nRAS | 32 | nCK |
| nRP | 13 | nCK |
| nFAW | 26 | nCK |
| nRRD | 5 | nCK |
| nRFC | 150 | nCK |

Basic IDD and IDDQ Measurement Conditions

| Symbol | Description |
|--------|---|
| IDD0 | <p>Operating One Bank Active-Precharge Current</p> <p>CKE: High; External clock: On; tCK, nRC, nRAS, CL: see “Timings used for IDD and IDDQ Measurement-Loop Patterns” Table; BL: 8⁽¹⁾; AL: 0; CS: High between ACT and PRE; Command, Address, Bank Address Inputs: partially toggling according to “IDD0 Measurement-Loop Pattern” Table; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0, 0, 1,1,2,2... Output Buffer and RTT: Enabled in Mode Registers⁽²⁾; ODT Signal: stable at 0; Pattern Details: see “IDD0 Measurement-Loop Pattern” Table</p> |
| IDD1 | <p>Operating One Bank Active-Read-Precharge Current</p> <p>CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see “Timings used for IDD and IDDQ Measurement-Loop Patterns” Table; BL: 8^(1,6); AL: 0; CS: High between ACT, RD and PRE; Command, Address, Bank Address Inputs, Data IO: partially toggling according to “IDD1 Measurement-Loop Pattern” Table; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0, 0, 1,1,2,2... Output Buffer and RTT: Enabled in Mode Registers⁽²⁾; ODT Signal: stable at 0; Pattern Details: see “IDD1 Measurement-Loop Pattern” Table</p> |
| IDD2N | <p>Precharge Standby Current</p> <p>CKE: High; External clock: On; tCK, CL: see “Timings used for IDD and IDDQ Measurement-Loop Patterns” Table; BL: 8⁽¹⁾; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to “IDD2N Measurement-Loop Pattern” Table; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers⁽²⁾; ODT Signal: stable at 0. Pattern Details: see “IDD2N Measurement-Loop Pattern” Table</p> |
| IDD2NT | <p>Precharge Standby ODT Current</p> <p>CKE: High; External clock: On; tCK, CL: see “Timings used for IDD and IDDQ Measurement-Loop Patterns” Table; BL: 8⁽¹⁾; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to “IDD2NT Measurement-Loop Pattern” Table; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers⁽²⁾; ODT Signal: toggling according to “IDD2NT Measurement-Loop Pattern” Table; Pattern Details: see “IDD2NT Measurement-Loop Pattern” Table</p> |
| IDD2P0 | <p>Precharge Power-Down Current Slow Exit</p> <p>CKE: Low; External clock: On; tCK, CL: see “Timings used for IDD and IDDQ Measurement-Loop Patterns” Table; BL: 8⁽¹⁾; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers⁽²⁾; ODT Signal: stable at 0; Precharge Power Down Mode: Slow Exit⁽³⁾</p> |

| Symbol | Description |
|--------|---|
| IDD2P1 | <p>Precharge Power-Down Current Fast Exit</p> <p>CKE: Low; External clock: On; tCK, CL: see “Timings used for IDD and IDDQ Measurement-Loop Patterns” Table; BL: 8⁽¹⁾; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ⁽²⁾; ODT Signal: stable at 0; Precharge Power Down Mode: Fast Exit ⁽³⁾</p> |
| IDD2Q | <p>Precharge Quiet Standby Current</p> <p>CKE: High; External clock: On; tCK, CL: see “Timings used for IDD and IDDQ Measurement-Loop Patterns” Table; BL: 8⁽¹⁾; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ⁽²⁾; ODT Signal: stable at 0.</p> |
| IDD3N | <p>Active Standby Current</p> <p>CKE: High; External clock: On; tCK, CL: see “Timings used for IDD and IDDQ Measurement-Loop Patterns” Table; BL: 8⁽¹⁾; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to “IDD3N Measurement-Loop Pattern” Table; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers ⁽²⁾; ODT Signal: stable at 0; Pattern Details: see “IDD3N Measurement-Loop Pattern” Table</p> |
| IDD3P | <p>Active Power-Down Current</p> <p>CKE: Low; External clock: On; tCK, CL: see “Timings used for IDD and IDDQ Measurement-Loop Patterns” Table; BL: 8⁽¹⁾; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers ⁽²⁾; ODT Signal: stable at 0.</p> |
| IDD4R | <p>Operating Burst Read Current</p> <p>CKE: High; External clock: On; tCK, CL: see “Timings used for IDD and IDDQ Measurement-Loop Patterns” Table; BL: 8^(1,6); AL: 0; CS: High between RD; Command, Address, Bank Address Inputs: partially toggling according to “IDD4R and IDD4W Measurement-Loop Pattern” Table; Data IO: seamless read data burst with different data between one burst and the next one according to “IDD4R and IDD4W Measurement-Loop Pattern” Table; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers ⁽²⁾; ODT Signal: stable at 0; Pattern Details: see “IDD4R and IDD4W Measurement-Loop Pattern” Table</p> |
| IDD4W | <p>Operating Burst Write Current</p> <p>CKE: High; External clock: On; tCK, CL: see “Timings used for IDD and IDDQ Measurement-Loop Patterns” Table; BL: 8⁽¹⁾; AL: 0; CS: High between WR; Command, Address, Bank Address Inputs: partially toggling according to “IDD4R and IDD4W Measurement-Loop Pattern” Table; Data IO: seamless write data burst with different data between one burst and the next one according to “IDD4R and IDD4W Measurement-Loop Pattern” Table; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0, 0, 1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers ⁽²⁾; ODT Signal: stable at HIGH Pattern Details: see “IDD4R and IDD4W Measurement-Loop Pattern” Table</p> |

| Symbol | Description |
|---|---|
| IDD5B | <p>Burst Refresh Current</p> <p>CKE: High; External clock: On; tCK, CL, nRFC: see “Timings used for IDD and IDDQ Measurement-Loop Patterns” Table; BL: 8⁽¹⁾; AL: 0; CS: High between REF; Command, Address, Bank Address Inputs: partially toggling according to “IDD5B Measurement-Loop Pattern” Table; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: REF command every nRFC; Output Buffer and RTT: Enabled in Mode Registers ⁽²⁾; ODT Signal: stable at 0; Pattern Details: see “IDD5B Measurement-Loop Pattern” Table</p> |
| IDD6 | <p>Self Refresh Current: Normal Temperature Range</p> <p>T_{OPER}: 0 - 85°C or -40 - 85°C; Auto Self-Refresh (ASR): Disabled⁽⁴⁾; Self-Refresh Temperature Range (SRT): Normal⁽⁵⁾; CKE: Low; External clock: Off; CK and CK: LOW; CL: see “Timings used for IDD and IDDQ Measurement-Loop Patterns” Table; BL: 8⁽¹⁾; AL: 0; CS, Command, Address, Bank Address, Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers ⁽²⁾; ODT Signal: MID-LEVEL</p> |
| IDD6ET | <p>Self-Refresh Current: Extended Temperature Range ⁽⁶⁾</p> <p>T_{OPER}: 0 - 95°C or -40 - 95°C; Auto Self-Refresh (ASR): Disabled⁽⁴⁾; Self-Refresh Temperature Range (SRT): Extended⁽⁵⁾; CKE: Low; External clock: Off; CK and CK: LOW; CL: see “Timings used for IDD and IDDQ Measurement-Loop Patterns” Table; BL: 8⁽¹⁾; AL: 0; CS, Command, Address, Bank Address, Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers ⁽²⁾; ODT Signal: MID-LEVEL</p> |
| IDD7 | <p>Operating Bank Interleave Read Current</p> <p>CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see “Timings used for IDD and IDDQ Measurement-Loop Patterns” Table; BL: 8^(1,6); AL: CL-1; CS: High between ACT and RDA; Command, Address, Bank Address inputs: partially toggling according to “IDD7 Measurement-Loop Pattern” Table; Data IO: read data bursts with different data between one burst and the next one according to “IDD7 Measurement-Loop Pattern” Table; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers ⁽²⁾; ODT Signal: stable at 0; Pattern Details: see “IDD7 Measurement-Loop Pattern” Table</p> |
| IDD8 | <p>RESET Low Current</p> <p>RESET : LOW; External clock: Off; CK and CK: LOW; CKE: FLOATING; CS, Command, Address, Bank Address, Data IO: FLOATING; ODT Signal: FLOATING; RESET Low current reading is valid once power is stable and RESET has been LOW for at least 1ms.</p> |
| <p>Note:</p> <ol style="list-style-type: none"> Burst Length: BL8 fixed by MRS: set MR0 A[1,0] = 00B. Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_Wr enable: set MR2 A[10,9] = 10B. Precharge Power Down Mode: set MR0 A12 = 0B for Slow Exit or MR0 A12 = 1B for Fast Exit. Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature. Self-Refresh Temperature Range (SRT): set MR2 A7 = 0B for normal or 1B for extended temperature range. Read Burst Type: Nibble Sequential, set MR0 A[3] = 0B. | |

IDD0 Measurement-Loop Pattern¹

| CK, /CK | CKE | Sub-Loop | Cycle Number | Command | /CS | /RAS | /CAS | /WE | ODT | BA[2:0] | A[13:11] | A[10] | A[9:7] | A[6:3] | A[2:0] | Data ² | | |
|----------|-------------|---|--------------|--|-----|------|------|-----|-----|---------|----------|-------|--------|--------|--------|-------------------|---|---|
| toggling | Static High | 0 | 0 | ACT | 0 | 0 | 1 | 1 | 0 | 0 | 00 | 0 | 0 | 0 | 0 | - | | |
| | | | 1, 2 | D, D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 00 | 0 | 0 | 0 | 0 | - | |
| | | | 3, 4 | D#, D# | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 00 | 0 | 0 | 0 | 0 | - | |
| | | | ... | repeat pattern 1...4 until nRAS - 1, truncate if necessary | | | | | | | | | | | | | | |
| | | | nRAS | PRE | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 00 | 0 | 0 | 0 | 0 | - | |
| | | | ... | repeat pattern 1...4 until nRC - 1, truncate if necessary | | | | | | | | | | | | | | |
| | | | 1*nRC + 0 | ACT | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 00 | 0 | 0 | F | 0 | - | |
| | | | 1*nRC + 1, 2 | D, D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 | 0 | 0 | F | 0 | - |
| | | | 1*nRC + 3, 4 | D#, D# | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 00 | 0 | 0 | F | 0 | - |
| | | | ... | repeat pattern nRC + 1,...,4 until 1*nRC + nRAS - 1, truncate if necessary | | | | | | | | | | | | | | |
| | | | 1*nRC + nRAS | PRE | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 00 | 0 | 0 | F | 0 | - |
| | | | ... | repeat nRC + 1,...,4 until 2*nRC - 1, truncate if necessary | | | | | | | | | | | | | | |
| | | 1 | 2*nRC | repeat Sub-Loop 0, use BA[2:0] = 1 instead | | | | | | | | | | | | | | |
| | | 2 | 4*nRC | repeat Sub-Loop 0, use BA[2:0] = 2 instead | | | | | | | | | | | | | | |
| | | 3 | 6*nRC | repeat Sub-Loop 0, use BA[2:0] = 3 instead | | | | | | | | | | | | | | |
| | | 4 | 8*nRC | repeat Sub-Loop 0, use BA[2:0] = 4 instead | | | | | | | | | | | | | | |
| | | 5 | 10*nRC | repeat Sub-Loop 0, use BA[2:0] = 5 instead | | | | | | | | | | | | | | |
| | | 6 | 12*nRC | repeat Sub-Loop 0, use BA[2:0] = 6 instead | | | | | | | | | | | | | | |
| 7 | 14*nRC | repeat Sub-Loop 0, use BA[2:0] = 7 instead | | | | | | | | | | | | | | | | |

Note:

- DM must be driven LOW all the time. DQS, DQS are MID-LEVEL.
- DQ signals are MID-LEVEL.

IDD1 Measurement-Loop Pattern¹

| CK, /CK | CKE | Sub-Loop | Cycle Number | Command | /CS | /RAS | /CAS | /WE | ODT | BA[2:0] | A[13:11] | A[10] | A[9:7] | A[6:3] | A[2:0] | Data ² | | | |
|----------|-------------|----------|--------------|---|---|------|------|-----|-----|---------|----------|-------|--------|--------|--------|-------------------|----------|--|--|
| toggling | Static High | 0 | 0 | ACT | 0 | 0 | 1 | 1 | 0 | 0 | 00 | 0 | 0 | 0 | 0 | - | | | |
| | | | 1, 2 | D, D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 00 | 0 | 0 | 0 | 0 | - | | |
| | | | 3, 4 | D#, D# | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 00 | 0 | 0 | 0 | 0 | - | | |
| | | | ... | repeat pattern 1...4 until nRCD - 1, truncate if necessary | | | | | | | | | | | | | | | |
| | | | nRCD | RD | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 00 | 0 | 0 | 0 | 0 | 00000000 | | |
| | | | ... | repeat pattern 1...4 until nRAS - 1, truncate if necessary | | | | | | | | | | | | | | | |
| | | | nRAS | PRE | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 00 | 0 | 0 | 0 | 0 | - | | |
| | | | ... | repeat pattern 1...4 until nRC - 1, truncate if necessary | | | | | | | | | | | | | | | |
| | | | 1*nRC + 0 | ACT | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 00 | 0 | 0 | F | 0 | - | | |
| | | | 1*nRC + 1, 2 | D, D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 00 | 0 | 0 | F | 0 | - | | |
| | | | 1*nRC + 3, 4 | D#, D# | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 00 | 0 | 0 | F | 0 | - | | |
| | | | ... | repeat pattern nRC + 1,..., 4 until nRC + nRCD - 1, truncate if necessary | | | | | | | | | | | | | | | |
| | | | 1*nRC + nRCD | RD | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 00 | 0 | 0 | F | 0 | 00110011 | | |
| | | | ... | repeat pattern nRC + 1,..., 4 until nRC + nRAS - 1, truncate if necessary | | | | | | | | | | | | | | | |
| | | | 1*nRC + nRAS | PRE | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 00 | 0 | 0 | F | 0 | - | | |
| | | | ... | repeat pattern nRC + 1,..., 4 until 2 * nRC - 1, truncate if necessary | | | | | | | | | | | | | | | |
| | | | 1 | 2*nRC | repeat Sub-Loop 0, use BA[2:0] = 1 instead | | | | | | | | | | | | | | |
| | | | 2 | 4*nRC | repeat Sub-Loop 0, use BA[2:0] = 2 instead | | | | | | | | | | | | | | |
| | | 3 | 6*nRC | repeat Sub-Loop 0, use BA[2:0] = 3 instead | | | | | | | | | | | | | | | |
| | | 4 | 8*nRC | repeat Sub-Loop 0, use BA[2:0] = 4 instead | | | | | | | | | | | | | | | |
| | | 5 | 10*nRC | repeat Sub-Loop 0, use BA[2:0] = 5 instead | | | | | | | | | | | | | | | |
| | | 6 | 12*nRC | repeat Sub-Loop 0, use BA[2:0] = 6 instead | | | | | | | | | | | | | | | |
| | | 7 | 14*nRC | repeat Sub-Loop 0, use BA[2:0] = 7 instead | | | | | | | | | | | | | | | |

Note:

- DM must be driven LOW all the time. DQS, DQS are used according to RD Commands, otherwise MID-LEVEL.
- Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

IDD2N and IDD3N Measurement-Loop Pattern¹

| CK, /CK | CKE | Sub-Loop | Cycle Number | Command | /CS | /RAS | /CAS | /WE | ODT | BA[2:0] | A[13:11] | A[10] | A[9:7] | A[6:3] | A[2:0] | Data ² | | |
|----------|-------------|----------|--------------|---|-----|------|------|-----|-----|---------|----------|-------|--------|--------|--------|-------------------|---|---|
| toggling | Static High | 0 | 0 | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | | |
| | | | 1 | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | |
| | | | 2 | D# | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | F | 0 | - |
| | | | 3 | D# | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | F | 0 | - |
| | | 1 | 4-7 | repeat Sub-Loop 0, use BA[2:0] = 1 instead | | | | | | | | | | | | | | |
| | | 2 | 8-11 | repeat Sub-Loop 0, use BA[2:0] = 2 instead | | | | | | | | | | | | | | |
| | | 3 | 12-15 | repeat Sub-Loop 0, use BA[2:0] = 3 instead | | | | | | | | | | | | | | |
| | | 4 | 16-19 | repeat Sub-Loop 0, use BA[2:0] = 4 instead | | | | | | | | | | | | | | |
| | | 5 | 20-23 | repeat Sub-Loop 0, use BA[2:0] = 5 instead | | | | | | | | | | | | | | |
| | | 6 | 24-27 | repeat Sub-Loop 0, use BA[2:0] = 6 instead | | | | | | | | | | | | | | |
| | | 7 | 28-31 | repeat Sub-Loop 0, use BA[2:0] = 7 instead | | | | | | | | | | | | | | |

Note:

- DM must be driven LOW all the time. DQS, $\overline{\text{DQS}}$ are MID-LEVEL.
- DQ signals are MID-LEVEL.

IDD2NT Measurement-Loop Pattern¹

| CK, /CK | CKE | Sub-Loop | Cycle Number | Command | /CS | /RAS | /CAS | /WE | ODT | BA[2:0] | A[13:11] | A[10] | A[9:7] | A[6:3] | A[2:0] | Data ² | | |
|----------|-------------|----------|--------------|--|-----|------|------|-----|-----|---------|----------|-------|--------|--------|--------|-------------------|---|---|
| toggling | Static High | 0 | 0 | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | | |
| | | | 1 | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | |
| | | | 2 | D# | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | F | 0 | - |
| | | | 3 | D# | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | F | 0 | - |
| | | 1 | 4-7 | repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 1 | | | | | | | | | | | | | | |
| | | 2 | 8-11 | repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 2 | | | | | | | | | | | | | | |
| | | 3 | 12-15 | repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 3 | | | | | | | | | | | | | | |
| | | 4 | 16-19 | repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 4 | | | | | | | | | | | | | | |
| | | 5 | 20-23 | repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 5 | | | | | | | | | | | | | | |
| | | 6 | 24-27 | repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 6 | | | | | | | | | | | | | | |
| | | 7 | 28-31 | repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 7 | | | | | | | | | | | | | | |

Note:

- DM must be driven LOW all the time. DQS, $\overline{\text{DQS}}$ are MID-LEVEL.
- DQ signals are MID-LEVEL.

IDD4R and IDDQ4R Measurement-Loop Pattern¹

| CK, /CK | CKE | Sub-Loop | Cycle Number | Command | /CS | /RAS | /CAS | /WE | ODT | BA[2:0] | A[13:11] | A[10] | A[9:7] | A[6:3] | A[2:0] | Data ² | | |
|----------|-------------|----------|--------------|---|-----|------|------|-----|-----|---------|----------|-------|--------|--------|--------|-------------------|----------|--|
| toggling | Static High | 0 | 0 | RD | 0 | 1 | 0 | 1 | 0 | 0 | 00 | 0 | 0 | 0 | 0 | 00000000 | | |
| | | | 1 | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 00 | 0 | 0 | 0 | 0 | - | |
| | | | 2, 3 | D#, D# | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 00 | 0 | 0 | 0 | 0 | - | |
| | | | 4 | RD | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 00 | 0 | 0 | F | 0 | 00110011 | |
| | | | 5 | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 00 | 0 | 0 | F | 0 | - | |
| | | | 6, 7 | D#, D# | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 00 | 0 | 0 | F | 0 | - | |
| | | 1 | 8-15 | repeat Sub-Loop 0, but BA[2:0] = 1 | | | | | | | | | | | | | | |
| | | 2 | 16-23 | repeat Sub-Loop 0, but BA[2:0] = 2 | | | | | | | | | | | | | | |
| | | 3 | 24-31 | repeat Sub-Loop 0, but BA[2:0] = 3 | | | | | | | | | | | | | | |
| | | 4 | 32-39 | repeat Sub-Loop 0, but BA[2:0] = 4 | | | | | | | | | | | | | | |
| | | 5 | 40-47 | repeat Sub-Loop 0, but BA[2:0] = 5 | | | | | | | | | | | | | | |
| | | 6 | 48-55 | repeat Sub-Loop 0, but BA[2:0] = 6 | | | | | | | | | | | | | | |
| | | 7 | 56-63 | repeat Sub-Loop 0, but BA[2:0] = 7 | | | | | | | | | | | | | | |

Note:

- DM must be driven LOW all the time. DQS, $\overline{\text{DQS}}$ are used according to RD Commands, otherwise MID-LEVEL.
- Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

IDD4W Measurement-Loop Pattern¹

| CK, /CK | CKE | Sub-Loop | Cycle Number | Command | /CS | /RAS | /CAS | /WE | ODT | BA[2:0] | A[13:11] | A[10] | A[9:7] | A[6:3] | A[2:0] | Data ² | | |
|----------|-------------|----------|--------------|---|-----|------|------|-----|-----|---------|----------|-------|--------|--------|--------|-------------------|----------|--|
| toggling | Static High | 0 | 0 | WR | 0 | 1 | 0 | 0 | 1 | 0 | 00 | 0 | 0 | 0 | 0 | 00000000 | | |
| | | | 1 | D | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 00 | 0 | 0 | 0 | 0 | - | |
| | | | 2, 3 | D#, D# | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 00 | 0 | 0 | 0 | 0 | - | |
| | | | 4 | WR | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 00 | 0 | 0 | F | 0 | 00110011 | |
| | | | 5 | D | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 00 | 0 | 0 | F | 0 | - | |
| | | | 6, 7 | D#, D# | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 00 | 0 | 0 | F | 0 | - | |
| | | 1 | 8-15 | repeat Sub-Loop 0, but BA[2:0] = 1 | | | | | | | | | | | | | | |
| | | 2 | 16-23 | repeat Sub-Loop 0, but BA[2:0] = 2 | | | | | | | | | | | | | | |
| | | 3 | 24-31 | repeat Sub-Loop 0, but BA[2:0] = 3 | | | | | | | | | | | | | | |
| | | 4 | 32-39 | repeat Sub-Loop 0, but BA[2:0] = 4 | | | | | | | | | | | | | | |
| | | 5 | 40-47 | repeat Sub-Loop 0, but BA[2:0] = 5 | | | | | | | | | | | | | | |
| | | 6 | 48-55 | repeat Sub-Loop 0, but BA[2:0] = 6 | | | | | | | | | | | | | | |
| | | 7 | 56-63 | repeat Sub-Loop 0, but BA[2:0] = 7 | | | | | | | | | | | | | | |

Note:

- DM must be driven LOW all the time. DQS, $\overline{\text{DQS}}$ are used according to WR Commands, otherwise MID-LEVEL.
- Burst Sequence driven on each DQ signal by Write Command. Outside burst operation, DQ signals are MID-LEVEL.

IDD5B Measurement-Loop Pattern¹

| CK, /CK | CKE | Sub-Loop | Cycle Number | Command | /CS | /RAS | /CAS | /WE | ODT | BA[2:0] | A[13:11] | A[10] | A[9:7] | A[6:3] | A[2:0] | Data ² | | |
|----------|-------------|----------|--------------|--|-----|------|------|-----|-----|---------|----------|-------|--------|--------|--------|-------------------|---|--|
| toggling | Static High | 0 | 0 | REF | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | | |
| | | 1 | 1, 2 | D, D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 00 | 0 | 0 | 0 | 0 | - | |
| | | | 3, 4 | D#, D# | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 00 | 0 | 0 | F | 0 | - | |
| | | | 5...8 | repeat cycles 1...4, but BA[2:0] = 1 | | | | | | | | | | | | | | |
| | | | 9...12 | repeat cycles 1...4, but BA[2:0] = 2 | | | | | | | | | | | | | | |
| | | | 13...16 | repeat cycles 1...4, but BA[2:0] = 3 | | | | | | | | | | | | | | |
| | | | 17...20 | repeat cycles 1...4, but BA[2:0] = 4 | | | | | | | | | | | | | | |
| | | | 21...24 | repeat cycles 1...4, but BA[2:0] = 5 | | | | | | | | | | | | | | |
| | | | 25...28 | repeat cycles 1...4, but BA[2:0] = 6 | | | | | | | | | | | | | | |
| | | | 29...32 | repeat cycles 1...4, but BA[2:0] = 7 | | | | | | | | | | | | | | |
| | | 2 | 33...nRFC-1 | repeat Sub-Loop 1, until nRFC - 1. Truncate, if necessary | | | | | | | | | | | | | | |

Note:

- DM must be driven LOW all the time. DQS, $\overline{\text{DQS}}$ are MID-LEVEL.
- DQ signals are MID-LEVEL.

IDD7 Measurement-Loop Pattern¹

ATTENTION: Sub-Loops 10-19 have inverse A[6:3] Pattern and Data Pattern than Sub-Loops 0-9

| CK, /CK | CKE | Sub-Loop | Cycle Number | Command | /CS | /RAS | /CAS | /WE | ODT | BA[2:0] | A[13:11] | A[10] | A[9:7] | A[6:3] | A[2:0] | Data ² | | |
|----------|-------------|----------|--------------|--|-----|------|------|-----|-----|---------|----------|-------|--------|--------|--------|-------------------|----------|----------|
| toggling | Static High | 0 | 0 | ACT | 0 | 0 | 1 | 1 | 0 | 0 | 00 | 0 | 0 | 0 | 0 | - | | |
| | | | 1 | RDA | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 00 | 1 | 0 | 0 | 0 | 00000000 | |
| | | | 2 | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | |
| | | | ... | repeat above D Command until nRRD - 1 | | | | | | | | | | | | | | |
| | | 1 | nRRD | ACT | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 00 | 0 | 0 | F | 0 | - |
| | | | nRRD + 1 | RDA | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 00 | 1 | 0 | F | 0 | 00110011 |
| | | | nRRD + 2 | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 00 | 0 | 0 | F | 0 | - |
| | | | ... | repeat above D Command until 2 * nRRD - 1 | | | | | | | | | | | | | | |
| | | 2 | 2*nRRD | repeat Sub-Loop 0, but BA[2:0] = 2 | | | | | | | | | | | | | | |
| | | 3 | 3*nRRD | repeat Sub-Loop 1, but BA[2:0] = 3 | | | | | | | | | | | | | | |
| | | 4 | 4*nRRD | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 3 | 00 | 0 | 0 | F | 0 | - |
| | | | | Assert and repeat above D Command until nFAW - 1, if necessary | | | | | | | | | | | | | | |
| | | 5 | nFAW | repeat Sub-Loop 0, but BA[2:0] = 4 | | | | | | | | | | | | | | |

| CK, /CK | CKE | Sub-Loop | Cycle Number | Command | /CS | /RAS | /CAS | /WE | ODT | BA[2:0] | A[13:11] | A[10] | A[9:7] | A[6:3] | A[2:0] | Data ² |
|--|-----|----------|-------------------|--|-----|------|------|-----|-----|---------|----------|-------|--------|--------|--------|-------------------|
| | | 6 | nFAW + nRRD | repeat Sub-Loop 1, but BA[2:0] = 5 | | | | | | | | | | | | |
| | | 7 | nFAW + 2*nRRD | repeat Sub-Loop 0, but BA[2:0] = 6 | | | | | | | | | | | | |
| | | 8 | nFAW + 3*nRRD | repeat Sub-Loop 1, but BA[2:0] = 7 | | | | | | | | | | | | |
| | | 9 | nFAW + 4*nRRD | D | 1 | 0 | 0 | 0 | 0 | 7 | 00 | 0 | 0 | F | 0 | - |
| Assert and repeat above D Command until 2 * nFAW - 1, if necessary | | | | | | | | | | | | | | | | |
| | | 10 | 2*nFAW + 0 | ACT | 0 | 0 | 1 | 1 | 0 | 0 | 00 | 0 | 0 | F | 0 | - |
| | | | 2*nFAW + 1 | RDA | | 1 | 0 | 1 | 0 | 0 | 00 | 1 | 0 | F | 0 | 00110011 |
| | | | 2*nFAW + 2 | D | 1 | 0 | 0 | 0 | 0 | 0 | 00 | 0 | 0 | F | 0 | - |
| repeat above D Command until 2 * nFAW + nRRD - 1 | | | | | | | | | | | | | | | | |
| | | 11 | 2*nFAW + nRRD | ACT | 0 | 0 | 1 | 1 | 0 | 1 | 00 | 0 | 0 | 0 | 0 | - |
| | | | 2*nFAW + nRRD + 1 | RDA | 0 | 1 | 0 | 1 | 0 | 1 | 00 | 1 | 0 | 0 | 0 | 00000000 |
| | | | 2*nFAW + nRRD + 2 | D | 1 | 0 | 0 | 0 | 0 | 1 | 00 | 0 | 0 | 0 | 0 | - |
| repeat above D Command until 2 * nFAW + 2 * nRRD - 1 | | | | | | | | | | | | | | | | |
| | | 12 | 2*nFAW + 2*nRRD | repeat Sub-Loop 10, but BA[2:0] = 2 | | | | | | | | | | | | |
| | | 13 | 2*nFAW + 3*nRRD | repeat Sub-Loop 11, but BA[2:0] = 3 | | | | | | | | | | | | |
| | | 14 | 2*nFAW + 4*nRRD | D | 1 | 0 | 0 | 0 | 0 | 3 | 00 | 0 | 0 | 0 | 0 | - |
| Assert and repeat above D Command until 3 * nFAW - 1, if necessary | | | | | | | | | | | | | | | | |
| | | 15 | 3*nFAW | repeat Sub-Loop 10, but BA[2:0] = 4 | | | | | | | | | | | | |
| | | 16 | 3*nFAW + nRRD | repeat Sub-Loop 11, but BA[2:0] = 5 | | | | | | | | | | | | |
| | | 17 | 3*nFAW + 2*nRRD | repeat Sub-Loop 10, but BA[2:0] = 6 | | | | | | | | | | | | |
| | | 18 | 3*nFAW + 3*nRRD | repeat Sub-Loop 11, but BA[2:0] = 7 | | | | | | | | | | | | |
| | | 19 | 3*nFAW + 4*nRRD | D | 1 | 0 | 0 | 0 | 0 | 7 | 00 | 0 | 0 | 0 | 0 | - |
| Assert and repeat above D Command until 4 * nFAW - 1, if necessary | | | | | | | | | | | | | | | | |

Note:

- DM must be driven LOW all the time. DQS, $\overline{\text{DQS}}$ are used according to RD Commands, otherwise MID-LEVEL.
- Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

IDD Specifications³

| Symbol | Parameter/ Condition | DDR3L-1866 | Unit |
|---------------------|---|------------|------|
| IDD0 | Operating Current 0 One Bank Activate -> Precharge | TBD | mA |
| IDD1 | Operating Current 1 One Bank Activate -> Read -> Precharge | TBD | mA |
| IDD2P0 (SLOW) | Precharge Power-Down Current Slow Exit - MR0 bit A12 = 0 | TBD | mA |
| IDD2P1 (FAST) | Precharge Power-Down Current Fast Exit - MR0 bit A12 = 1 | TBD | mA |
| IDD2Q | Precharge Quiet Standby Current | TBD | mA |
| IDD2N | Precharge Standby Current | TBD | mA |
| IDD2NT | Precharge Standby ODT IDDQ Current | TBD | mA |
| IDD3N | Active Standby Current | TBD | mA |
| IDD3P | Active Power-Down Current Always Fast Exit | TBD | mA |
| IDD4R | Operating Current Burst Read | TBD | mA |
| IDD4W | Operating Current Burst Write | TBD | mA |
| IDD5B | Burst Refresh Current | TBD | mA |
| IDD6 ¹ | Self-Refresh Current: Normal Temperature Range (0-85°C or -40-85°C) | TBD | mA |
| IDD6ET ² | Self-Refresh Current: Extended Temperature Range (0-95°C or -40-95°C) | TBD | mA |
| IDD7 | All Bank Interleave Read Current | TBD | mA |
| IDD8 | Reset Low Current | TBD | mA |

Note:

1. IDD6: SRT is 'Normal', ASR is disabled. Value is maximum.
2. IDD6ET: SRT is 'Extended', ASR is disabled. Value is maximum.
3. IDD will be derated (increased) when above 95°C.

IDD Specifications- Continued³

| Symbol | Parameter/ Condition | DDR3-1866 | Unit |
|---------------------|---|-----------|------|
| IDD0 | Operating Current 0 One Bank Activate -> Precharge | TBD | mA |
| IDD1 | Operating Current 1 One Bank Activate -> Read -> Precharge | TBD | mA |
| IDD2P0 (SLOW) | Precharge Power-Down Current Slow Exit - MR0 bit A12 = 0 | TBD | mA |
| IDD2P1 (FAST) | Precharge Power-Down Current Fast Exit - MR0 bit A12 = 1 | TBD | mA |
| IDD2Q | Precharge Quiet Standby Current | TBD | mA |
| IDD2N | Precharge Standby Current | TBD | mA |
| IDD2NT | Precharge Standby ODT IDDQ Current | TBD | mA |
| IDD3N | Active Standby Current | TBD | mA |
| IDD3P | Active Power-Down Current Always Fast Exit | TBD | mA |
| IDD4R | Operating Current Burst Read | TBD | mA |
| IDD4W | Operating Current Burst Write | TBD | mA |
| IDD5B | Burst Refresh Current | TBD | mA |
| IDD6 ¹ | Self-Refresh Current: Normal Temperature Range (0-85°C or -40-85°C) | TBD | mA |
| IDD6ET ² | Self-Refresh Current: Extended Temperature Range (0-95°C or -40-95°C) | TBD | mA |
| IDD7 | All Bank Interleave Read Current | TBD | mA |
| IDD8 | Reset Low Current | TBD | mA |

Note:

1. IDD6: SRT is 'Normal', ASR is disabled. Value is maximum.
2. IDD6ET: SRT is 'Extended', ASR is disabled. Value is maximum.
3. IDD will be derated (increased) when above 95°C

Electrical Characteristics & AC Timing

Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the DDR3 (L) SDRAM device.

Definition for tCK(avg)

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(\text{avg}) = \left(\sum_{j=1}^N tCK_j \right) / N$$

where $N = 200$

Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. tCK(abs) is not subject to production test.

Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(\text{avg}) = \left(\sum_{j=1}^N tCH_j \right) / (N \times tCK(\text{avg}))$$

where $N = 200$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(\text{avg}) = \left(\sum_{j=1}^N tCL_j \right) / (N \times tCK(\text{avg}))$$

where $N = 200$

Definition for tJIT(per) and tJIT(per, lck)

tJIT(per) is defined as the largest deviation of any signal tCK from tCK(avg).

$tJIT(per) = \text{Min/max of } \{tCK_i - tCK(avg)\}$ where $i = 1$ to 200}.

tJIT(per) defines the single period jitter when the DLL is already locked.

tJIT(per,lck) uses the same definition for single period jitter, during the DLL locking period only.

tJIT(per) and tJIT(per,lck) are not subject to production test.

Definition for tJIT(cc) and tJIT(cc, lck)

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles.

$tJIT(cc) = \text{Max of } |tCK_{i+1} - tCK_i|$.

tJIT(cc) defines the cycle to cycle jitter when the DLL is already locked.

tJIT(cc,lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only.

tJIT(cc) and tJIT(cc,lck) are not subject to production test.

Definition for tERR(nper)

tERR is defined as the cumulative error across n multiple consecutive cycles from tCK(avg). tERR is not subject to production test.

Refresh parameters

| Parameter | Symbol | | Value | Unit |
|--|--------|-----------------------------------|-------|------|
| REF command to ACT or REF command time | tRFC | | 160 | ns |
| Average periodic refresh interval | tREFI | 0°C ≤ T _{OPER} ≤ +85°C | 7.8 | us |
| | | -40°C ≤ T _{OPER} ≤ +85°C | | |
| | | 85°C < T _{OPER} ≤ +105°C | 3.9 | us |

Standard Speed Bins
Speed Bins and Operating Conditions

| Speed Bins | | DDR3(L)-1866 (13-13-13) | | Unit | Note | |
|----------------------|--|-------------------------|----------|---------|-------|---------|
| Symbol | Parameter | Min | Max | | | |
| tAA | Internal read command to first data | 13.91 | 20 | ns | | |
| tRCD | ACT to internal read or write delay time | 13.91 | - | ns | | |
| tRP | PRE command period | 13.91 | - | ns | | |
| tRC | ACT to ACT or REF command period | 47.91 | - | ns | | |
| tRAS | ACT to PRE command period | 34 | 9*tREFI | ns | | |
| tCK (avg) | CL6 | CWL5 | 2.5 | 3.3 | ns | 1,2,3,5 |
| | | CWL6/7/8/9 | Reserved | | ns | 4 |
| | CL7 | CWL5 | Reserved | | ns | 4 |
| | | CWL6 | 1.875 | < 2.5 | ns | 1,2,3,5 |
| | | CWL7/8/9 | Reserved | | ns | 4 |
| | CL8 | CWL5 | Reserved | | ns | 4 |
| | | CWL6 | 1.875 | < 2.5 | ns | 1,2,3,5 |
| | | CWL7/8/9 | Reserved | | ns | 4 |
| | CL9 | CWL5/6 | Reserved | | ns | 4 |
| | | CWL7 | 1.5 | < 1.875 | ns | 1,2,3,5 |
| | | CWL8/9 | Reserved | | ns | 4 |
| | CL10 | CWL5/6 | Reserved | | ns | 4 |
| | | CWL7 | 1.5 | < 1.875 | ns | 1,2,3,5 |
| | | CWL8 | Reserved | | ns | 4 |
| | CL11 | CWL5/6/7 | Reserved | | ns | 4 |
| | | CWL8 | 1.25 | < 1.5 | ns | 1,2,3,5 |
| | | CWL9 | Reserved | | ns | 4 |
| | CL12 | CWL5/6/7/8 | Reserved | | ns | 4 |
| | | CWL9 | Reserved | | ns | 4 |
| | CL13 | CWL5/6/7/8 | Reserved | | ns | 4 |
| CWL9 | | 1.07 | < 1.25 | ns | 1,2,3 | |
| Supported CL | | 6,7,8,9,10,11,13 | | nCK | | |
| Supported CWL | | 5,6,7,8,9 | | nCK | | |

Note:

Absolute Specification (T_{OPER} ; VDDQ = VDD = 1.5V +/- 0.075 V for DDR3; VDDQ = VDD = 1.35V -0.067V/+0.1V for DDR3(L))

1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(avg) value (3.0, 2.5, 1.875, 1.5, 1.25, 1.07 ns) when calculating CL [nCK] = tAA [ns] / tCK(Avg) [ns], rounding up to the next 'Supported CL', where tCK(avg) = 3.0 ns should only be used for CL = 5 calculation.
3. tCK(avg).MAX limits: Calculate $tCK(avg) = tAA.MAX / CL\ SELECTED$ and round the resulting tCK(avg) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.5 ns or 1.25 ns or 1.07 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. Any DDR3(L)-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.

Timing Parameters by Speed Bin

VDDQ = VDD = 1.5V +/- 0.075 V for DDR3; VDDQ = VDD = 1.35V -0.067V/+0.1V for DDR3(L)

| Parameter | Symbol | DDR3(L)-1866 | | Unit | Note |
|---|---------------|-----------------------------------|-----------------------------------|----------|---------|
| | | Min. | Max. | | |
| Clock Timing | | | | | |
| Minimum Clock Cycle Time (DLL off mode) | tCK (DLL_off) | 8 | - | ns | 6 |
| Average Clock Period | tCK(avg) | Refer to "Standard Speed Bins" | | | |
| Average high pulse width | tCH(avg) | 0.47 | 0.53 | tCK(avg) | |
| Average low pulse width | tCL(avg) | 0.47 | 0.53 | tCK(avg) | |
| Absolute Clock Period | tCK(abs) | tCK(avg)min = tJIT(per)min | tCK(avg)max = tJIT(per)max | ps | |
| Absolute clock HIGH pulse width | tCH(abs) | 0.43 | - | tCK(avg) | 25 |
| Absolute clock LOW pulse width | tCL(abs) | 0.43 | - | tCK(avg) | 26 |
| Clock Period Jitter | JIT(per) | -60 | 60 | ps | |
| Clock Period Jitter during DLL locking period | JIT(per, lck) | -50 | 50 | ps | |
| Cycle to Cycle Period Jitter | tJIT(cc) | 120 | | ps | |
| Cycle to Cycle Period Jitter during DLL locking period | JIT(cc, lck) | 100 | | ps | |
| Duty Cycle Jitter | tJIT(duty) | - | - | - | |
| Cumulative error across 2 cycles | tERR(2per) | -88 | 88 | ps | |
| Cumulative error across 3 cycles | tERR(3per) | -105 | 105 | ps | |
| Cumulative error across 4 cycles | tERR(4per) | -117 | 117 | ps | |
| Cumulative error across 5 cycles | tERR(5per) | -126 | 126 | ps | |
| Cumulative error across 6 cycles | tERR(6per) | -133 | 133 | ps | |
| Cumulative error across 7 cycles | tERR(7per) | -139 | 139 | ps | |
| Cumulative error across 8 cycles | tERR(8per) | -145 | 145 | ps | |
| Cumulative error across 9 cycles | tERR(9per) | -150 | 150 | ps | |
| Cumulative error across 10 cycles | tERR(10per) | -154 | 154 | ps | |
| Cumulative error across 11 cycles | tERR(11per) | -158 | 158 | ps | |
| Cumulative error across 12 cycles | tERR(12per) | -161 | 161 | ps | |
| Cumulative error across n = 13,14...49,50 cycles | tERR(nper) | $(1 + 0.68\ln(n)) * tJIT(per)min$ | $(1 + 0.68\ln(n)) * tJIT(per)max$ | ps | 24 |
| Data Timing | | | | | |
| DQS, \overline{DQS} to DQ skew, per group, per access | tDQSQ | - | 85 | ps | 13 |
| DQ output hold time from DQS, \overline{DQS} | tQH | 0.38 | - | tCK(avg) | 13,g |
| DQ low-impedance time from CK, \overline{CK} | tLZ(DQ) | -390 | 195 | ps | 13,14,f |
| DQ high-impedance time from CK, \overline{CK} | tHZ(DQ) | - | 195 | ps | 13,14,f |

| Parameter | Symbol | DDR3(L)-1866 | | Unit | Note |
|--|---|--------------|---------|----------|---------|
| | | Min. | Max. | | |
| Data setup time to DQS, \overline{DQS} referenced to VIH (AC) / VIL(AC) levels | tDS(base) AC150 DDR3 | - | - | ps | d,17 |
| | tDS(base) AC135 DDR3 | 68 | - | ps | d,17 |
| | tDS(base) AC135 SR = 1V/ns DDR3L | - | - | ps | d,17 |
| | tDS(base) AC130 SR=2V/ns DDR3L | 70 | - | ps | d |
| Data hold time from DQS, \overline{DQS} referenced to VIH(DC) / VIL(DC) levels | tDH(base) DC100 DDR3 | - | - | ps | d,17 |
| | tDH(base) DC90 SR = 1V/ns DDR3L | - | - | ps | d,17 |
| | tDH(base) DC90 SR=2V/ns DDR3L | 75 | - | ps | d |
| DQ and DM Input pulse width for each input | tDIPW | 320 | - | ps | 28 |
| DQS, \overline{DQS} differential READ Preamble | tRPRE | 0.9 | Note 19 | tCK(avg) | 13,19,g |
| DQS, \overline{DQS} differential READ Postamble | tRPST | 0.3 | Note 11 | tCK(avg) | 11,13,g |
| DQS, \overline{DQS} differential output high time | tQSH | 0.4 | - | tCK(avg) | 13,g |
| DQS, \overline{DQS} differential output low time | tQSL | 0.4 | - | tCK(avg) | 13,g |
| DQS, \overline{DQS} differential WRITE Preamble | tWPRE | 0.9 | - | tCK(avg) | 1 |
| DQS, \overline{DQS} differential WRITE Postamble | tWPST | 0.3 | - | tCK(avg) | 1 |
| DQS, \overline{DQS} rising edge output access time from rising CK,CK | tDQCK | -195 | 195 | ps | 13,f |
| DQS and \overline{DQS} low-impedance time (Referenced from RL-1) | tLZ(DQS) | -390 | 195 | ps | 13,14,f |
| DQS and \overline{DQS} high-impedance time (Referenced from RL+BL/2) | tHZ(DQS) | - | 195 | ps | 13,14,f |
| DQS, \overline{DQS} differential input low pulse width | tDQSL | 0.45 | 0.55 | tCK(avg) | 29,31 |
| DQS, \overline{DQS} differential input high pulse width | tDQSH | 0.45 | 0.55 | tCK(avg) | 30,31 |

| Parameter | Symbol | DDR3(L)-1866 | | Unit | Note |
|---|---|--------------------------------|------|----------|---------|
| | | Min. | Max. | | |
| DQS, $\overline{\text{DQS}}$ rising edge to CK, CK rising edge | tDQSS | -0.27 | 0.27 | tCK(avg) | c |
| DQS, $\overline{\text{DQS}}$ falling edge setup time to CK, CK rising edge | tDSS | 0.18 | - | tCK(avg) | c,32 |
| DQS, $\overline{\text{DQS}}$ falling edge hold time from CK, CK rising edge | tDSH | 0.18 | - | tCK(avg) | c,32 |
| Command and Address Timing | | | | | |
| DLL locking time | tDLLK | 512 | - | nCK | |
| Internal READ Command to PRECHARGE Command delay | tRTP | max(4tCK, 7.5ns) | - | | e |
| Delay from start of internal write transaction to internal read command | tWTR | max(4tCK, 7.5ns) | - | | e,18 |
| WRITE recovery time | tWR | 15 | - | ns | e,18 |
| Mode Register Set command cycle time | tMRD | 4 | - | nCK | |
| Mode Register Set command update delay | tMOD | max(12tCK, 15ns) | - | | |
| ACT to internal read or write delay time | tRCD | Refer to "Standard Speed Bins" | | | e |
| PRE command period | tRP | Refer to "Standard Speed Bins" | | | e |
| ACT to ACT or REF command period | tRC | Refer to "Standard Speed Bins" | | | e |
| ACTIVE to PRECHARGE command period | tRAS | Refer to "Standard Speed Bins" | | | e |
| $\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ command delay | tCCD | 4 | - | nCK | |
| Auto precharge write recovery + precharge time | tDAL(min) | WR + round up(tRP / tCK(avg)) | | nCK | |
| Multi-Purpose Register Recovery Time | tMPRR | 1 | - | nCK | 22 |
| ACTIVE to ACTIVE command period for 1KB page size | tRRD | Max(4tCK, 5ns) | - | | e |
| Four activate window for 1KB page size | tFAW | 27 | - | ns | e |
| Command and Address setup time to CK, CK referenced to VIH(AC) / VIL(AC) levels | tIS(base) AC175 DDR3 | - | - | ps | b,16 |
| | tIS(base) AC150 DDR3 | - | - | ps | b,16,27 |
| | tIS(base) AC125 DDR3 | 150 | - | ps | b,16,27 |
| | tIS(base) AC160 SR = 1V/ns DDR3L | - | - | ps | b,16 |
| | tIS(base) AC135 SR = 1V/ns DDR3L | 65 | - | ps | b,16 |

| Parameter | Symbol | DDR3(L)-1866 | | Unit | Note |
|--|---|------------------------------------|------|------|------|
| | | Min. | Max. | | |
| | tIS(base) AC125 SR = 1V/ns DDR3L | 150 | - | ps | b,16 |
| Command and Address hold time from CK, $\overline{\text{CK}}$ referenced to VIH(DC) / VIL(DC) levels | tIH(base) DC100 DDR3 | 100 | - | ps | b,16 |
| | tIH(base) DC90 SR = 1V/ns DDR3L | 110 | - | ps | b,16 |
| Control and Address Input pulse width for each input | tIPW | 535 | - | ps | 28 |
| Calibration Timing | | | | | |
| Power-up and $\overline{\text{RESET}}$ calibration time | tZQinit | max(512 tCK, 640ns) | - | - | |
| Normal operation Full calibration time | tZQoper | max(256 tCK, 320ns) | - | - | |
| Normal operation Short calibration time | tZQCS | max(64 tCK, 80ns) | - | - | 23 |
| Reset Timing | | | | | |
| Exit Reset from CKE HIGH to a valid command | tXPR | max(5 tCK, tRFC(min) + 10ns) | - | - | |
| Self Refresh Timing | | | | | |
| Exit Self Refresh to commands not requiring a locked DLL | tXS | max(5 tCK, tRFC(min) + 10ns) | - | - | |
| Exit Self Refresh to commands requiring a locked DLL | tXSDLL | tDLLK(min) | - | nCK | |
| Minimum CKE low width for Self Refresh entry to exit timing | tCKESR | tCKE(min) + 1 tCK | - | - | |
| Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE) | tCKSRE | max(5 tCK, 10 ns) | - | - | |
| Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit | tCKSRX | max(5 tCK, 10 ns) | - | - | |
| Power Down Timing | | | | | |
| Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL | tXP | max(3tCK, 6ns) | - | | |
| CKE minimum pulse width | tCKE | max(3tCK, 5ns) | - | | |
| Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL | tXPDLL | max(10 tCK, 24ns) | - | | 2 |
| Command pass disable delay | tCPDED | 2 | - | nCK | |

| Parameter | Symbol | DDR3(L)-1866 | | Unit | Note |
|--|----------|---------------------------|---------|----------|-------|
| | | Min. | Max. | | |
| Power Down Entry to Exit Timing | tPD | tCKE(min) | 9*tREFI | | 15 |
| Timing of ACT command to Power Down entry | tACTPDEN | 1 | - | nCK | 20 |
| Timing of PRE or PREA command to Power Down entry | tPRPDEN | 1 | - | nCK | 20 |
| Timing of RD/RDA command to Power Down entry | tRDPDEN | RL+4+1 | - | nCK | |
| Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF) | tWRPDEN | WL + 4 + (tWR / tCK(avg)) | - | nCK | 9 |
| Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF) | tWRAPDEN | WL+4+WR+1 | - | nCK | 10 |
| Timing of WR command to Power Down entry (BC4MRS) | tWRPDEN | WL + 2 + (tWR / tCK(avg)) | - | nCK | 9 |
| Timing of WRA command to Power Down entry (BC4MRS) | tWRAPDEN | WL + 2 + WR + 1 | - | nCK | 10 |
| Timing of REF command to Power Down entry | tREFPDEN | 1 | - | nCK | 20,21 |
| Timing of MRS command to Power Down entry | tMRSPDEN | tMOD(min) | - | | |
| ODT Timing | | | | | |
| ODT turn on Latency | ODTLon | WL-2=CWL+AL-2 | | nCK | |
| ODT turn off Latency | ODTLoFF | WL-2=CWL+AL-2 | | nCK | |
| ODT high time without write command or with write command and BC4 | ODTH4 | 4 | - | nCK | |
| ODT high time with Write command and BL8 | ODTH8 | 6 | - | nCK | |
| Asynchronous RTT turn-on delay (Power-Down with DLL frozen) | tAONPD | 2 | 8.5 | ns | |
| Asynchronous RTT turn-off delay (Power-Down with DLL frozen) | tAOFPD | 2 | 8.5 | ns | |
| RTT turn-on | tAON | -195 | 195 | ps | 7,f |
| RTT_Nom and RTT_WR turn-off time from ODTLoFF reference | tAOF | 0.3 | 0.7 | tCK(avg) | 8,f |
| RTT dynamic change skew | tADC | 0.3 | 0.7 | tCK(avg) | f |
| Write Leveling Timing | | | | | |
| First DQS/ \overline{DQS} rising edge after write leveling mode is programmed | tWLMRD | 40 | - | nCK | 3 |
| DQS/ \overline{DQS} delay after write leveling mode is programmed | tWLDQSEN | 25 | - | nCK | 3 |
| Write leveling setup time from rising CK, CK crossing to rising DQS, \overline{DQS} crossing | tWLS | 140 | - | ps | |
| Write leveling hold time from rising DQS, \overline{DQS} crossing to rising CK, CK crossing | tWLH | 140 | - | ps | |

| Parameter | Symbol | DDR3(L)-1866 | | Unit | Note |
|-----------------------------|--------|--------------|------|------|------|
| | | Min. | Max. | | |
| Write leveling output delay | tWLO | 0 | 7.5 | ns | |
| Write leveling output error | tWLOE | 0 | 2 | ns | |

Jitter Notes

- a. Unit “tCK(avg)” represents the actual tCK(avg) of the input clock under operation. Unit “nCK” represents one clock cycle of the input clock, counting the actual clock edges. Ex) tMRD=4 [nCK] means; if one Mode Register Set command is registered at T_m, another Mode Register Set command may be registered at T_m+4, even if (T_m+4-T_m) is 4 x tCK(avg) + tERR(4per), min.
- b. These parameters are measured from a command/address signal (CKE, \overline{CS} , \overline{RAS} , \overline{CAS} , \overline{WE} , ODT, BA0, A0, A1, etc) transition edge to its respective clock signal (CK/ \overline{CK}) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.
- c. These parameters are measured from a data strobe signal (DQS(L/U), $\overline{DQS(L/U)}$) crossing to its respective clock signal (CK, \overline{CK}) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.
- d. These parameters are measured from a data signal (DM(L/U), DQ(L/U)0, DQ(L/U)1, etc.) transition edge to its respective data strobe signal (DQS(L/U), $\overline{DQS(L/U)}$) crossing.
- e. For these parameters, the DDR3(L) SDRAM device supports tPARAM [nCK] = RU{tPARAM[ns] / tCK(avg)[ns]}, which is in clock cycles, assuming all input clock jitter specifications are satisfied.
- f. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(mper), act of the input clock, where 2 ≤ m ≤ 12. (Output derating is relative to the SDRAM input clock.)
- g. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per),act of the input clock. (Output deratings are relative to the SDRAM input clock.)

Timing Parameter Notes

1. Actual value dependent upon measurement level definitions see Figure - “Method for calculating tWPRE transitions and endpoints” and “Method for calculating tWPST transitions and endpoints”.
2. Commands requiring a locked DLL are: READ (and RAP) are synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in mode register.
5. Value must be rounded-up to next higher integer value.
6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.
7. For definition of RTT-on time tAON, see “Timing Parameters”.
8. For definition of RTT-off time tAOF, see “Timing Parameters”.
9. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.
10. WR in clock cycles are programmed in MR0.
11. The maximum read postamble is bounded by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side. See Figure - “Clock to Data Strobe Relationship”.
12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by TBD.
13. Value is only valid for RON34.
14. Single ended signal parameter.
15. tREFI depends on T_{OPER}.
16. tIS(base) and tIH(base) values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, \overline{CK} differential slew rate.
Note for DQ and DM signals, VREF(DC)=VREFDQ(DC). For input only pins except \overline{RESET} , VREF(DC)=VREFCA(DC). See “Address / Command Setup, Hold and Derating”
17. tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, \overline{DQS} differential slew rate.
Note for DQ and DM signals, VREF(DC)=VREFDQ(DC). For input only pins except \overline{RESET} , VREF(DC)=VREFCA(DC). See “Data Setup, Hold and Slew Rate Derating”.
18. Start of internal write transaction is defined as follows:
For BL8 (fixed by MRS and on-the-fly): Rising clock edge 4 clock cycles after WL.
For BC4 (on-the-fly): Rising clock edge 4 clock cycles after WL.
For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.
19. The maximum read preamble is bound by tLZ (DQS)min on the left side and tDQSCK(max) on the right side. See Figure - “Clock to Data Strobe Relationship”.
20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
21. Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required. See “Power-Down clarifications - Case 2”.
22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.

23. One ZQCS command can effectively correct a minimum of 0.5% (ZQ Correction) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the “Output Driver Voltage and Temperature Sensitivity” and “ODT Voltage and Temperature Sensitivity” tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters.

One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

ZQ Correction

$$\frac{0.5}{(TSens \times Tdriftrate) + (VSens \times Vdriftrate)}$$

where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

For example, if TSens = 1.5%/°C, VSens = 0.15%/mV, Tdriftrate = 1 °C/sec and Vdriftrate = 15mV/sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128\text{ms}$$

24. n = from 13 cycles to 50 cycles. This row defines 38 parameters.
25. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
26. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
27. The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100ps of derating to accommodate for the lower alternate threshold of 150mV and another 25ps to account for the earlier reference point [(175mV – 150mV) / 1V/ns].
28. Pulse width of a input signal is defined as the width between the first crossing of VREF(DC) and the consecutive crossing of VREF(DC).
29. tDQSL describes the instantaneous differential input low pulse width on DQS - \overline{DQS} , as measured from one falling edge to the next consecutive rising edge.
30. tDQSH describes the instantaneous differential input high pulse width on DQS - \overline{DQS} , as measured from one rising edge to the next consecutive falling edge.
31. tDQSH,act + tDQSL,act = 1 tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.
32. tDSH,act + tDSS,act = 1 tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.

Address / Command Setup, Hold and Derating

For all input signals the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS(base) and tIH(base) and tIH(base) value to the delta tIS and delta tIH derating value respectively.

Example: tIS (total setup time) = tIS(base) + delta tIS

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIH(AC)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIL(AC)max. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF (DC) to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(DC) to ac region', the slew rate of the tangent line to the actual signal from the ac level to dc level is used for derating value.

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VREF(DC). Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VREF(DC). If the actual signal is always later than the nominal slew rate line between shaded 'dc to VREF(DC) region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to VREF(DC) region', the slew rate of a tangent line to the actual signal from the dc level to VREF(DC) level is used for derating value. For a valid transition the input signal has to remain above/below VIH/IL(AC) for some time tVAC. Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(AC) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(AC).

For slew rates in between the values listed in following tables, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

ADD/CMD Setup and Hold Base-Values for 1V/ns

| Grade | Symbol | Reference | 1866 | Unit | Note |
|-------|-----------------|----------------------|------|------|------|
| DDR3 | tIS(base) AC175 | VIH/L(AC) | - | ps | 1 |
| | tIS(base) AC150 | VIH/L(AC) | - | ps | 1,2 |
| | tIS(base) AC135 | VIH/L(AC) | 60 | ps | 1 |
| | tIS(base) AC125 | VIH/L(AC) | 150 | ps | 1,3 |
| | tIH(base) DC100 | VIH/L(DC) | 100 | ps | 1 |
| DDR3L | tIS(base) AC160 | VIH/L(AC): SR =1V/ns | - | ps | 1 |
| | tIS(base) AC135 | VIH/L(AC): SR =1V/ns | 65 | ps | 1,4 |
| | tIS(base) AC125 | VIH/L(AC): SR =1V/ns | 150 | ps | 1,5 |
| | tIH(base) DC90 | VIH/L(DC): SR =1V/ns | 110 | ps | 1 |

Derating values DDR3-1866 tIS/tIH – AC/DC based AC135 Threshold

| | | ΔtIS, ΔtIH derating in [ps] AC/DC based | | | | | | | | | | | | | | | |
|--------------------------|-----|---|------|----------|------|----------|------|----------|------|----------|------|----------|------|----------|------|----------|------|
| | | AC 135 Threshold -> VIH (AC) = VREF (DC) + 135mV, VIL (AC) = VREF(DC) - 135mV | | | | | | | | | | | | | | | |
| | | CK,/CK Differential Slew Rate | | | | | | | | | | | | | | | |
| | | 4.0 V/ns | | 3.0 V/ns | | 2.0 V/ns | | 1.8 V/ns | | 1.6 V/ns | | 1.4 V/ns | | 1.2 V/ns | | 1.0 V/ns | |
| | | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH |
| CMD/ADD Slew Rate (V/ns) | 2 | 68 | 50 | 68 | 50 | 68 | 50 | 76 | 58 | 84 | 66 | 92 | 74 | 100 | 84 | 108 | 100 |
| | 1.5 | 45 | 34 | 45 | 34 | 45 | 34 | 53 | 42 | 61 | 50 | 69 | 58 | 77 | 68 | 85 | 84 |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 8 | 8 | 16 | 16 | 24 | 24 | 32 | 34 | 40 | 50 |
| | 0.9 | 2 | -4 | 2 | -4 | 2 | -4 | 10 | 4 | 18 | 12 | 26 | 20 | 34 | 30 | 42 | 46 |
| | 0.8 | 3 | -10 | 3 | -10 | 3 | -10 | 11 | -2 | 19 | 6 | 27 | 14 | 35 | 24 | 43 | 40 |
| | 0.7 | 6 | -16 | 6 | -16 | 6 | -16 | 14 | -8 | 22 | 0 | 30 | 8 | 38 | 18 | 46 | 34 |
| | 0.6 | 9 | -26 | 9 | -26 | 9 | -26 | 17 | -18 | 25 | -10 | 33 | -2 | 41 | 8 | 49 | 24 |
| | 0.5 | 5 | -40 | 5 | -40 | 5 | -40 | 13 | -32 | 21 | -24 | 29 | -16 | 37 | -6 | 45 | 10 |
| | 0.4 | -3 | -60 | -3 | -60 | -3 | -60 | 6 | -52 | 14 | -44 | 22 | -36 | 30 | -26 | 38 | -10 |

Derating values DDR3-1866 tIS/tIH – AC/DC based AC125 Threshold

| | | ΔtIS, ΔtIH derating in [ps] AC/DC based | | | | | | | | | | | | | | | |
|--------------------------|-----|---|------|----------|------|----------|------|----------|------|----------|------|----------|------|----------|------|----------|------|
| | | AC 125 Threshold -> VIH (AC) = VREF (DC) + 125mV, VIL (AC) = VREF(DC) - 125mV | | | | | | | | | | | | | | | |
| | | CK,/CK Differential Slew Rate | | | | | | | | | | | | | | | |
| | | 4.0 V/ns | | 3.0 V/ns | | 2.0 V/ns | | 1.8 V/ns | | 1.6 V/ns | | 1.4 V/ns | | 1.2 V/ns | | 1.0 V/ns | |
| | | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH |
| CMD/ADD Slew Rate (V/ns) | 2 | 63 | 50 | 63 | 50 | 63 | 50 | 71 | 58 | 79 | 66 | 87 | 74 | 95 | 84 | 103 | 100 |
| | 1.5 | 42 | 34 | 42 | 34 | 42 | 34 | 50 | 42 | 58 | 50 | 66 | 58 | 74 | 68 | 82 | 84 |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 8 | 8 | 16 | 16 | 24 | 24 | 32 | 34 | 40 | 50 |
| | 0.9 | 4 | -4 | 4 | -4 | 4 | -4 | 12 | 4 | 20 | 12 | 28 | 20 | 36 | 30 | 44 | 46 |
| | 0.8 | 6 | -10 | 6 | -10 | 6 | -10 | 14 | -2 | 22 | 6 | 30 | 14 | 38 | 24 | 46 | 40 |
| | 0.7 | 11 | -16 | 11 | -16 | 11 | -16 | 19 | -8 | 27 | 0 | 35 | 8 | 43 | 18 | 51 | 34 |
| | 0.6 | 16 | -26 | 16 | -26 | 16 | -26 | 24 | -18 | 32 | -10 | 40 | -2 | 48 | 8 | 56 | 24 |
| | 0.5 | 15 | -40 | 15 | -40 | 15 | -40 | 23 | -32 | 31 | -24 | 39 | -16 | 47 | -6 | 55 | 10 |
| | 0.4 | 13 | -60 | 13 | -60 | 13 | -60 | 21 | -52 | 29 | -44 | 37 | -36 | 45 | -26 | 53 | -10 |

Derating values DDR3L-1866 tIS/tIH – AC/DC based AC125 Threshold

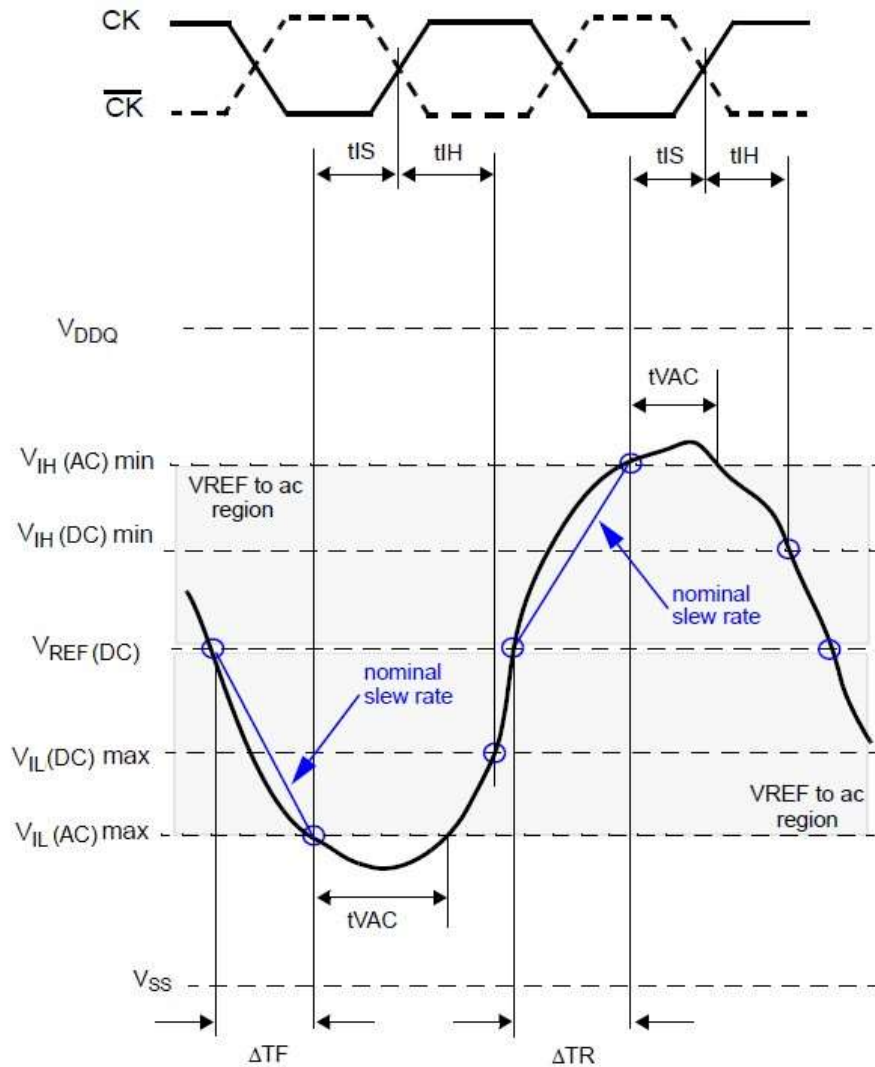
| | | $\Delta tIS, \Delta tIH$ derating in [ps] AC/DC based | | | | | | | | | | | | | | | |
|--------------------------|-----|---|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| | | AC 125 Threshold -> $V_{IH}(AC) = V_{REF}(DC) + 125mV$, $V_{IL}(AC) = V_{REF}(DC) - 125mV$ | | | | | | | | | | | | | | | |
| | | CK,/CK Differential Slew Rate | | | | | | | | | | | | | | | |
| | | 4.0 V/ns | | 3.0 V/ns | | 2.0 V/ns | | 1.8 V/ns | | 1.6 V/ns | | 1.4 V/ns | | 1.2 V/ns | | 1.0 V/ns | |
| | | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH |
| CMD/ADD Slew Rate (V/ns) | 2 | 63 | 45 | 63 | 45 | 63 | 45 | 71 | 53 | 79 | 61 | 87 | 69 | 95 | 79 | 103 | 95 |
| | 1.5 | 42 | 30 | 42 | 30 | 42 | 30 | 50 | 38 | 58 | 46 | 66 | 54 | 74 | 64 | 82 | 80 |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 8 | 8 | 16 | 16 | 24 | 24 | 32 | 34 | 40 | 50 |
| | 0.9 | 3 | -3 | 3 | -3 | 3 | -3 | 11 | 5 | 19 | 13 | 27 | 21 | 35 | 31 | 43 | 47 |
| | 0.8 | 6 | -8 | 6 | -8 | 6 | -8 | 14 | 1 | 22 | 9 | 30 | 17 | 38 | 27 | 46 | 43 |
| | 0.7 | 10 | -13 | 10 | -13 | 10 | -13 | 18 | -5 | 26 | 3 | 34 | 11 | 42 | 21 | 50 | 37 |
| | 0.6 | 16 | -20 | 16 | -20 | 16 | -20 | 24 | -12 | 32 | 4 | 40 | -4 | 48 | 14 | 56 | 30 |
| | 0.5 | 15 | -30 | 15 | 0 | 15 | -30 | 23 | -22 | 31 | -14 | 39 | -6 | 47 | 4 | 55 | 20 |
| 0.4 | 13 | -45 | 13 | -45 | 13 | -45 | 21 | -37 | 29 | -29 | 37 | -21 | 45 | -11 | 53 | 5 | |

Required time tVAC above VIH(AC) {below VIL(AC)} for ADD/CMD transition

| Slew Rate [V/ns] | DDR3 | | DDR3L | |
|------------------|-------------------|-------------------|-------------------|-------------------|
| | 1866 | | 1866 | |
| | tVAC @ 135mV [ps] | tVAC @ 125mV [ps] | tVAC @ 135mV [ps] | tVAC @ 125mV [ps] |
| | min | min | min | min |
| >2.0 | 168 | 173 | 200 | 205 |
| 2 | 168 | 173 | 200 | 205 |
| 1.5 | 145 | 152 | 178 | 184 |
| 1 | 100 | 110 | 133 | 143 |
| 0.9 | 85 | 96 | 118 | 129 |
| 0.8 | 66 | 79 | 99 | 111 |
| 0.7 | 42 | 56 | 75 | 89 |
| 0.6 | 10 | 27 | 43 | 59 |
| 0.5 | Note | Note | Note | 18 |
| <0.5 | Note | Note | Note | 18 |

Note: Rising input signal shall become equal to or greater than $V_{IH}(AC)$ level and falling input signal shall become equal to or less than $V_{IL}(AC)$ level.

Illustration of nominal slew rate and tVAC for setup time tIS (for ADD/CMD with respect to clock)

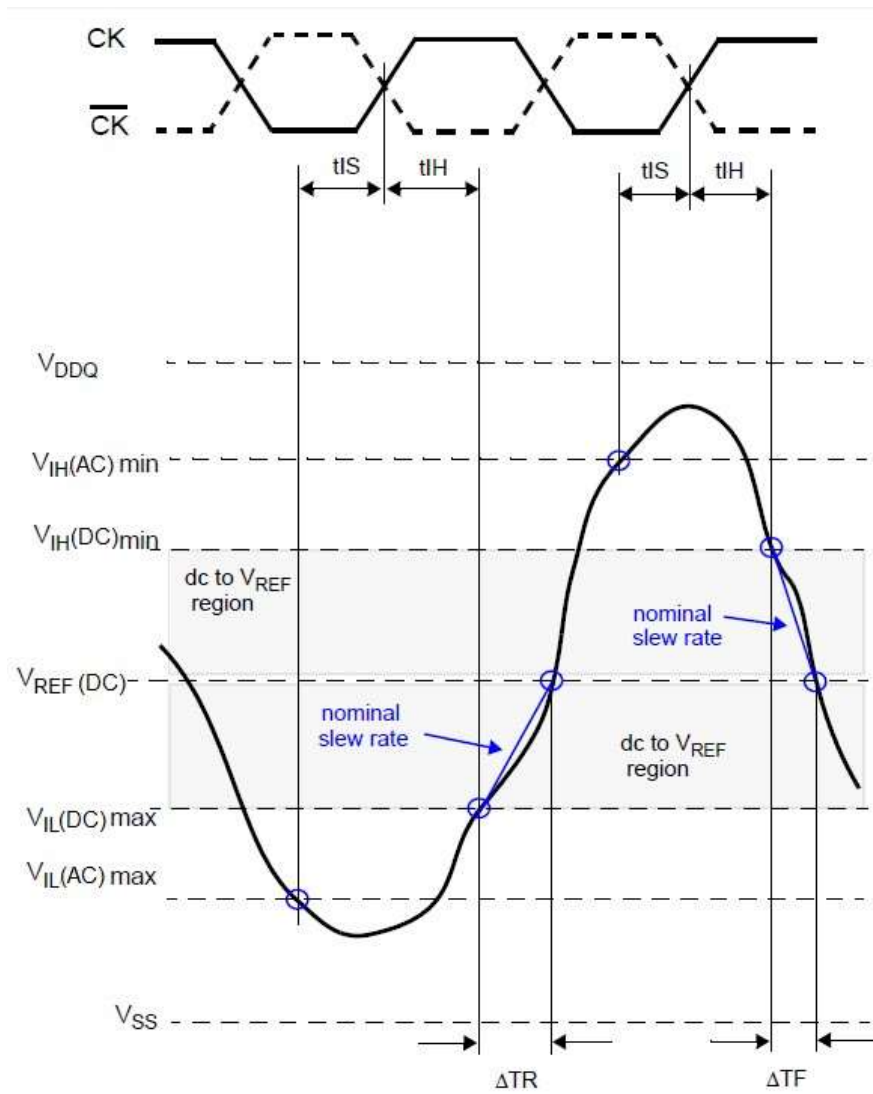


$$\text{Setup Slew Rate} = \frac{V_{REF(DC)} - V_{IL(AC) \max}}{\Delta TF}$$

Falling Signal

$$\text{Setup Slew Rate} = \frac{V_{IH(AC) \min} - V_{REF(DC)}}{\Delta TR}$$

Rising Signal

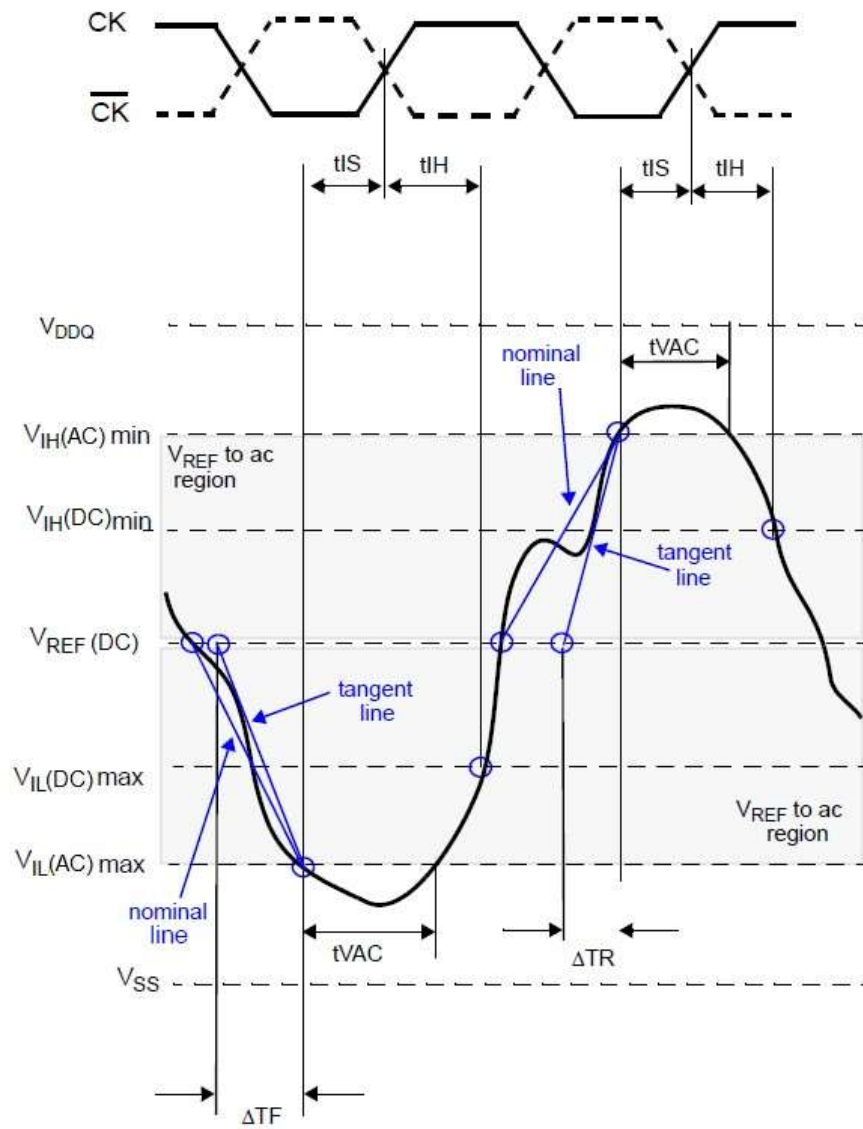
Illustration of nominal slew rate for hold time t_{IH} (for ADD/CMD with respect to clock)


$$\text{Hold Slew Rate} = \frac{V_{REF(DC)} - V_{IL(DC)max}}{\Delta TR}$$

Rising Signal

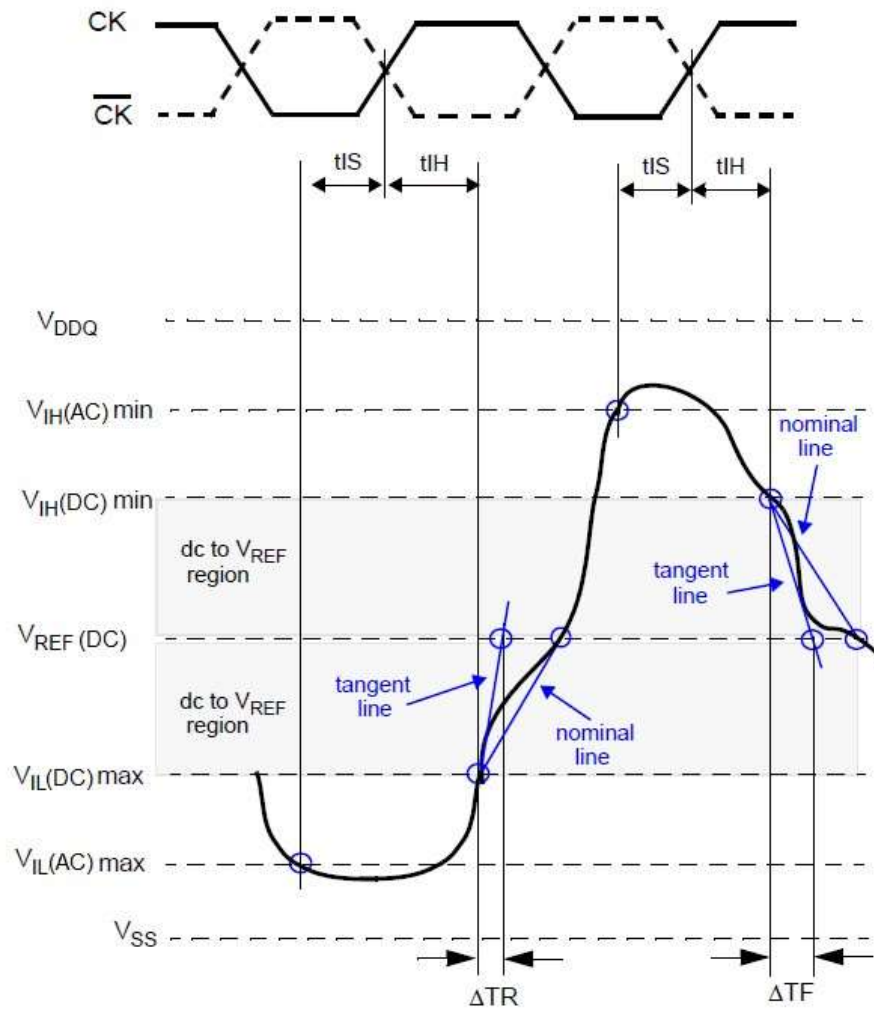
$$\text{Hold Slew Rate} = \frac{V_{IH(DC)min} - V_{REF(DC)}}{\Delta TF}$$

Falling Signal

Illustration of tangent line for setup time tIS (for ADD/CMD with respect to clock)


$$\begin{aligned} \text{Setup Slew Rate} &= \frac{\text{tangent line} [V_{REF(DC)} - V_{IL(AC)max}]}{\Delta TF} \\ \text{Falling Signal} & \end{aligned}$$

$$\begin{aligned} \text{Setup Slew Rate} &= \frac{\text{tangent line} [V_{IH(AC)min} - V_{REF(DC)}]}{\Delta TR} \\ \text{Rising Signal} & \end{aligned}$$

Illustration of tangent line for for hold time tIH (for ADD/CMD with respect to clock)


$$\text{Hold Slew Rate} = \frac{\text{tangent line [VREF(DC) - VIL(DC)max]}}{\Delta \text{ TR}}$$

Rising Signal

$$\text{Hold Slew Rate} = \frac{\text{tangent line [VIH(DC)min - VREF(DC)]}}{\Delta \text{ TF}}$$

Falling Signal

Data Setup, Hold and Slew Rate Derating

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDH(base) and tDS(base) value to the delta tDS and delta tDH derating value respectively.

Example: tDS (total setup time) = tDS(base) + delta tDS

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIH(AC)min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIL(AC)max. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(DC) to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(DC) to ac region', the slew rate of the tangent line to the actual signal from the ac level to dc level is used for derating value.

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VREF(DC). Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VREF(DC). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to VREF(DC) region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to VREF(DC) region', the slew rate of a tangent line to the actual signal from the dc level to VREF(DC) level is used for derating value.

For a valid transition the input signal has to remain above/below VIH/IL(AC) for some time tVAC.

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(AC) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(AC).

For slew rates in between the values listed in the following tables, the derating values may be obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

Data Setup and Hold Base-Values

| Grade | Symbol | Reference | 1866 | Unit | Note |
|-------|-----------------|-----------------------|------|------|------|
| DDR3 | tDS(base) AC150 | VIH/L(AC) : SR =1V/ns | - | ps | 2 |
| | tDS(base) AC135 | VIH/L(AC) : SR =1V/ns | - | ps | 2 |
| | tDS(base) AC135 | VIH/L(AC) : SR =2V/ns | 68 | ps | 1 |
| | tDH(base) DC100 | VIH/L(DC) : SR =1V/ns | - | ps | 2 |
| | tDH(base) DC100 | VIH/L(DC) : SR =2V/ns | 70 | ps | 1 |
| DDR3L | tDS(base) AC135 | VIH/L(AC) : SR =1V/ns | - | ps | 2 |
| | tDS(base) AC130 | VIH/L(AC) : SR =2V/ns | 70 | ps | 1 |
| | tDH(base) DC90 | VIH/L(DC) : SR =2V/ns | 75 | ps | 1 |
| | tDH(base) DC90 | VIH/L(DC) : SR =1V/ns | - | ps | 2 |

Note:

1. AC/DC referenced for 2V/ns DQ-slew rate and 4V/ns DQS slew rate.
2. AC/DC referenced for 1V/ns DQ-slew rate and 2V/ns DQS slew rate.

Derating values DDR3-1866 tDS/tDH – AC/DC based AC135 Threshold

| | | $\Delta tDS, \Delta tDH$ derating in [ps] AC/DC based | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------|-----|---|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| | | AC 135 Threshold -> $V_{IH} (AC) = V_{REF} (DC) + 135mV, V_{IL} (AC) = V_{REF}(DC) - 135mV$ | | | | | | | | | | | | | | | | | | | | | | | |
| | | DC 100 Threshold -> $V_{IH} (DC) = V_{REF} (DC) + 100mV, V_{IL} (DC) = V_{REF}(DC) - 100mV$ | | | | | | | | | | | | | | | | | | | | | | | |
| | | 8.0 V/ns | | 7.0 V/ns | | 6.0 V/ns | | 5.0 V/ns | | 4.0 V/ns | | 3.0 V/ns | | 2.0 V/ns | | 1.8 V/ns | | 1.6 V/ns | | 1.4 V/ns | | 1.2 V/ns | | 1.0 V/ns | |
| | | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH |
| DQ Slew Rate (V/ns) | 4 | 34 | 25 | 34 | 25 | 34 | 25 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| | 3.5 | 29 | 21 | 29 | 21 | 29 | 21 | 29 | 21 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| | 3 | 23 | 17 | 23 | 17 | 23 | 17 | 23 | 17 | 23 | 17 | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| | 2.5 | - | - | 14 | 10 | 14 | 10 | 14 | 10 | 14 | 10 | 14 | 10 | - | - | - | - | - | - | - | - | - | - | - | - |
| | 2 | - | - | - | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | - | - | - | - | - | - | - | - | - |
| | 1.5 | - | - | - | - | - | - | -23 | -17 | -23 | -17 | -23 | -17 | -23 | -17 | -15 | -9 | - | - | - | - | - | - | - | - |
| | 1 | - | - | - | - | - | - | - | - | -68 | -50 | -68 | -50 | -68 | -50 | -60 | -42 | -52 | -34 | - | - | - | - | - | - |
| | 0.9 | - | - | - | - | - | - | - | - | - | - | -66 | -54 | -66 | -54 | -58 | -46 | -50 | -38 | -42 | -30 | - | - | - | - |
| | 0.8 | - | - | - | - | - | - | - | - | - | - | - | - | - | -64 | -60 | -56 | -52 | -48 | -44 | -40 | -36 | -32 | -26 | - |
| | 0.7 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | -53 | -59 | -45 | -51 | -37 | -43 | -29 | -33 | -21 |
| 0.6 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | -43 | -61 | -35 | -53 | -27 | -43 | -19 | |
| 0.5 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | -39 | -66 | -31 | -56 | -23 | |
| 0.4 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | -38 | -76 | -30 | |

Note: Cell contents shaded in gray are defined as 'not supported'.

Derating values DDR3L-1866 tDS/tDH – AC/DC based AC130 Threshold

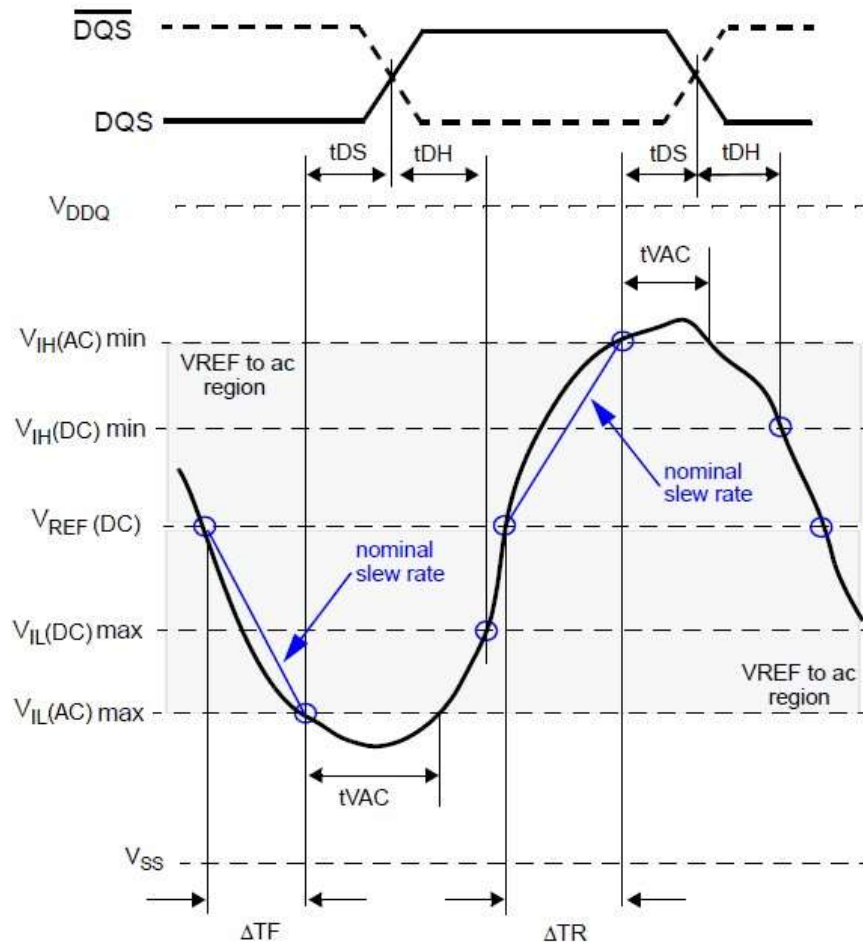
| | | $\Delta tDS, \Delta tDH$ derating in [ps] AC/DC based | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------|-----|---|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| | | AC 130 Threshold -> $V_{IH} (AC) = V_{REF} (DC) + 130mV, V_{IL} (AC) = V_{REF}(DC) - 130mV$ | | | | | | | | | | | | | | | | | | | | | | | |
| | | DQS, /DQS Differential Slew Rate | | | | | | | | | | | | | | | | | | | | | | | |
| | | 8.0 V/ns | | 7.0 V/ns | | 6.0 V/ns | | 5.0 V/ns | | 4.0 V/ns | | 3.0 V/ns | | 2.0 V/ns | | 1.8 V/ns | | 1.6 V/ns | | 1.4 V/ns | | 1.2 V/ns | | 1.0 V/ns | |
| | | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH |
| DQ Slew Rate (V/ns) | 4 | 33 | 23 | 33 | 23 | 33 | 23 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| | 3.5 | 28 | 19 | 28 | 19 | 28 | 19 | 28 | 19 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| | 3 | 22 | 15 | 22 | 15 | 22 | 15 | 22 | 15 | 22 | 15 | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| | 2.5 | - | - | 13 | 9 | 13 | 9 | 13 | 9 | 13 | 9 | 13 | 9 | - | - | - | - | - | - | - | - | - | - | - | |
| | 2 | - | - | - | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | - | - | - | - | - | - | - | - | |
| | 1.5 | - | - | - | - | - | - | -22 | -15 | -22 | -15 | -22 | -15 | -22 | -15 | -14 | -7 | - | - | - | - | - | - | - | |
| | 1 | - | - | - | - | - | - | - | - | -65 | -45 | -65 | -45 | -65 | -45 | -57 | -37 | -49 | -29 | - | - | - | - | - | |
| | 0.9 | - | - | - | - | - | - | - | - | - | - | -62 | -48 | -62 | -48 | -54 | -40 | -46 | -32 | -38 | -24 | - | - | - | |
| | 0.8 | - | - | - | - | - | - | - | - | - | - | - | - | - | -61 | -53 | -53 | -45 | -45 | -37 | -37 | -29 | -29 | -19 | |
| | 0.7 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | -49 | -50 | -41 | -42 | -33 | -34 | -25 | -24 | |
| 0.6 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | -37 | -49 | -29 | -41 | -21 | -31 | | |
| 0.5 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | -31 | -51 | -23 | -41 | | |
| 0.4 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | -28 | -56 | | |

Note: Cell contents shaded in gray are defined as 'not supported'.

Required time tVAC above VIH(AC) {below VIL(AC)} for valid DQ transition

| Slew Rate [V/ns] | DDR3 | DDR3L |
|------------------|-------------------|-------------------|
| | 1866 | 1866 |
| | tVAC @ 135mV [ps] | tVAC @ 130mV [ps] |
| | min | min |
| >2.0 | 93 | 95 |
| 2 | 93 | 95 |
| 1.5 | 70 | 73 |
| 1 | 25 | 30 |
| 0.9 | Note | 16 |
| 0.8 | Note | Note |
| 0.7 | - | - |
| 0.6 | - | - |
| 0.5 | - | - |
| <0.5 | - | - |

Note: Rising input signal shall become equal to or greater than VIH(AC) level and falling input signal shall become equal to or less than VIL(AC) level.

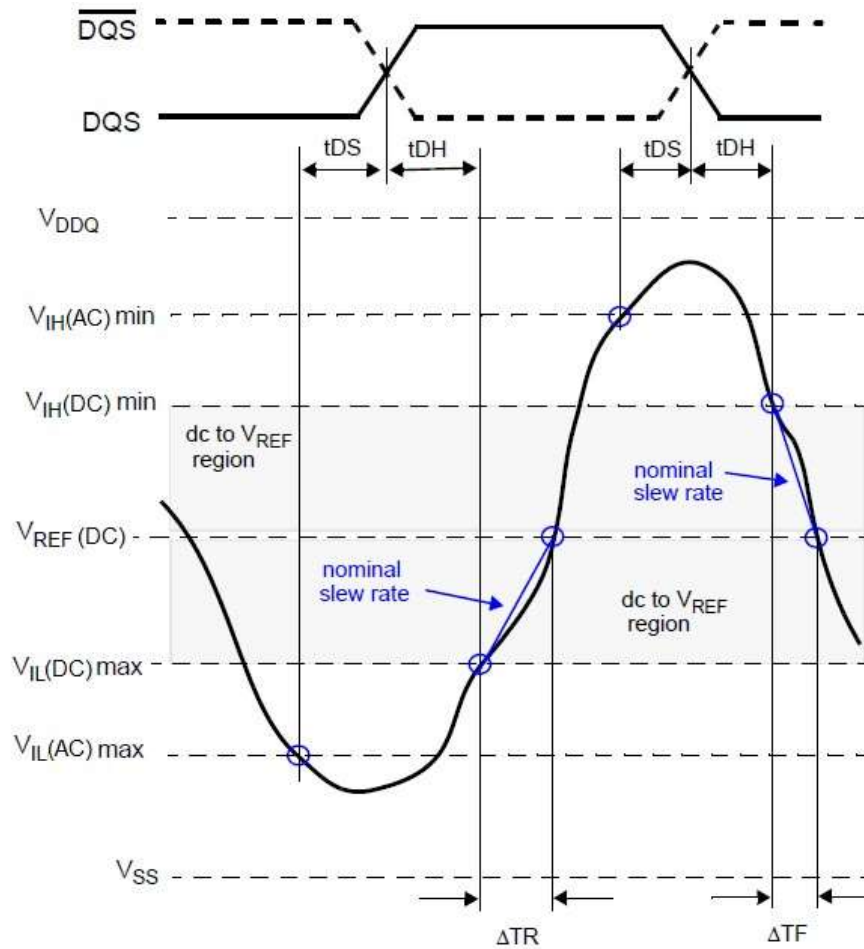
Illustration of nominal slew rate and tVAC for setup time tDS (for DQ with respect to strobe)


$$\text{Setup Slew Rate} = \frac{V_{REF(DC)} - V_{IL(AC) \max}}{\Delta TF}$$

Falling Signal

$$\text{Setup Slew Rate} = \frac{V_{IH(AC) \min} - V_{REF(DC)}}{\Delta TR}$$

Rising Signal

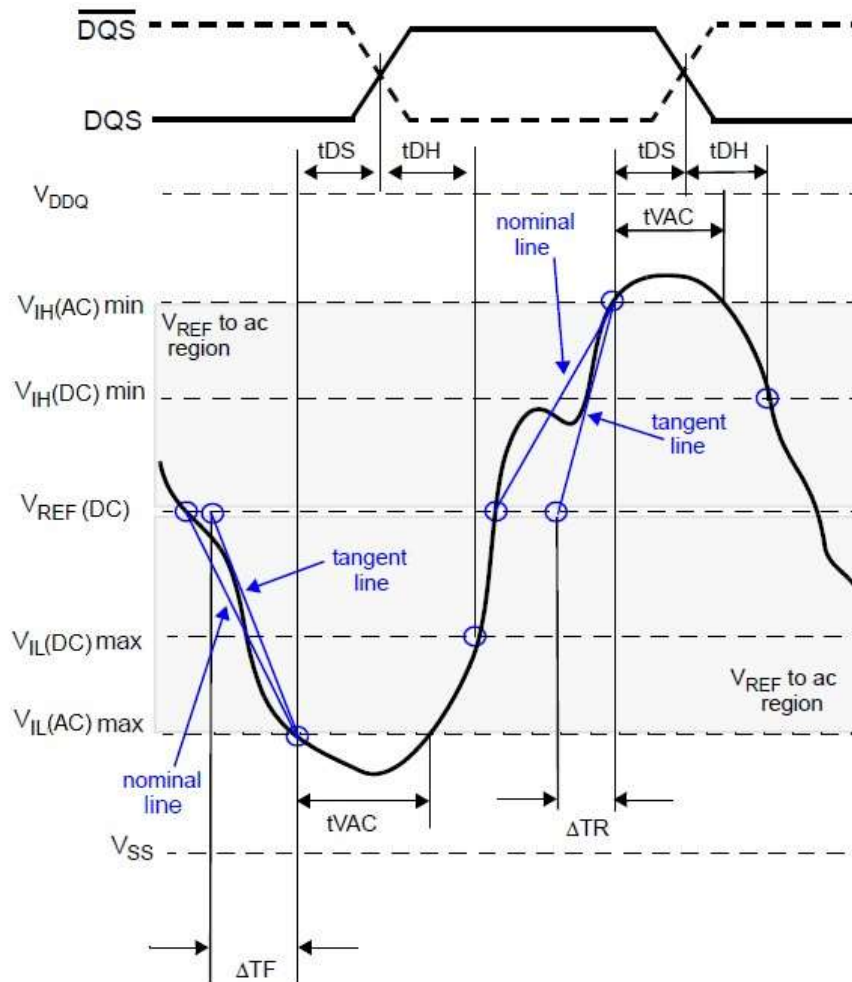
Illustration of nominal slew rate for hold time t_{DH} (for DQ with respect to strobe)


$$\text{Hold Slew Rate} = \frac{V_{REF(DC)} - V_{IL(DC)max}}{\Delta TR}$$

Rising Signal

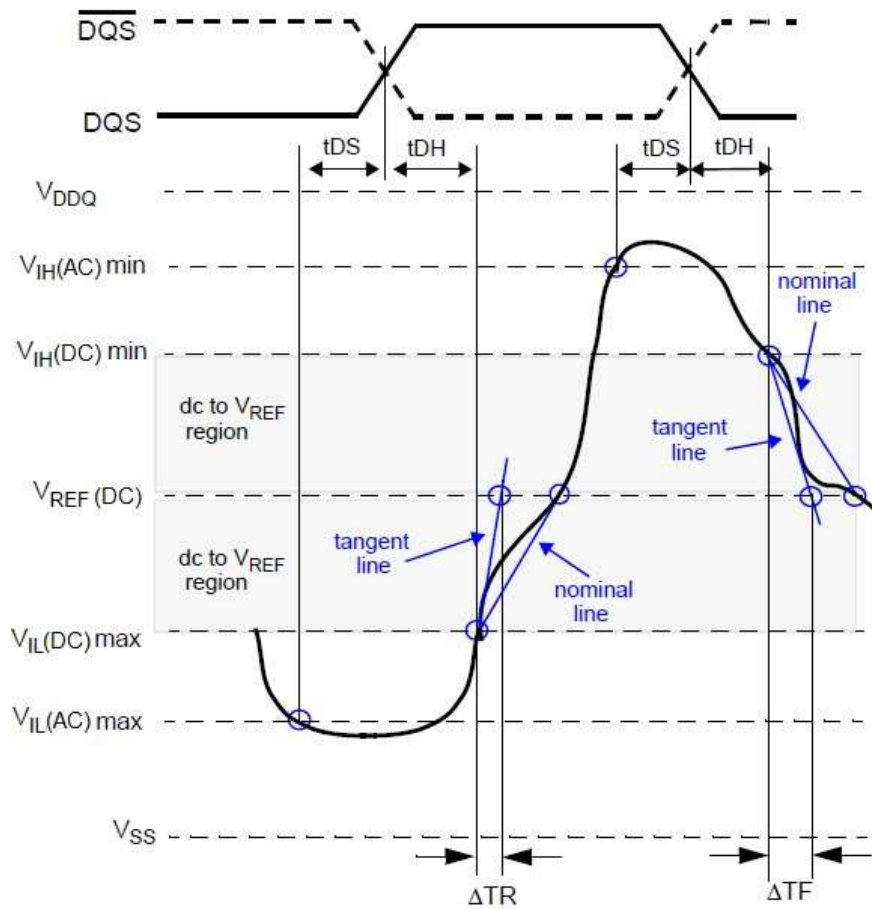
$$\text{Hold Slew Rate} = \frac{V_{IH(DC)min} - V_{REF(DC)}}{\Delta TF}$$

Falling Signal

Illustration of tangent line for setup time tDS (for DQ with respect to strobe)


$$\begin{aligned} \text{Setup Slew Rate} &= \frac{\text{tangent line} [V_{REF}(DC) - V_{IL}(AC)_{max}]}{\Delta TF} \\ \text{Falling Signal} & \end{aligned}$$

$$\begin{aligned} \text{Setup Slew Rate} &= \frac{\text{tangent line} [V_{IH}(AC)_{min} - V_{REF}(DC)]}{\Delta TR} \\ \text{Rising Signal} & \end{aligned}$$

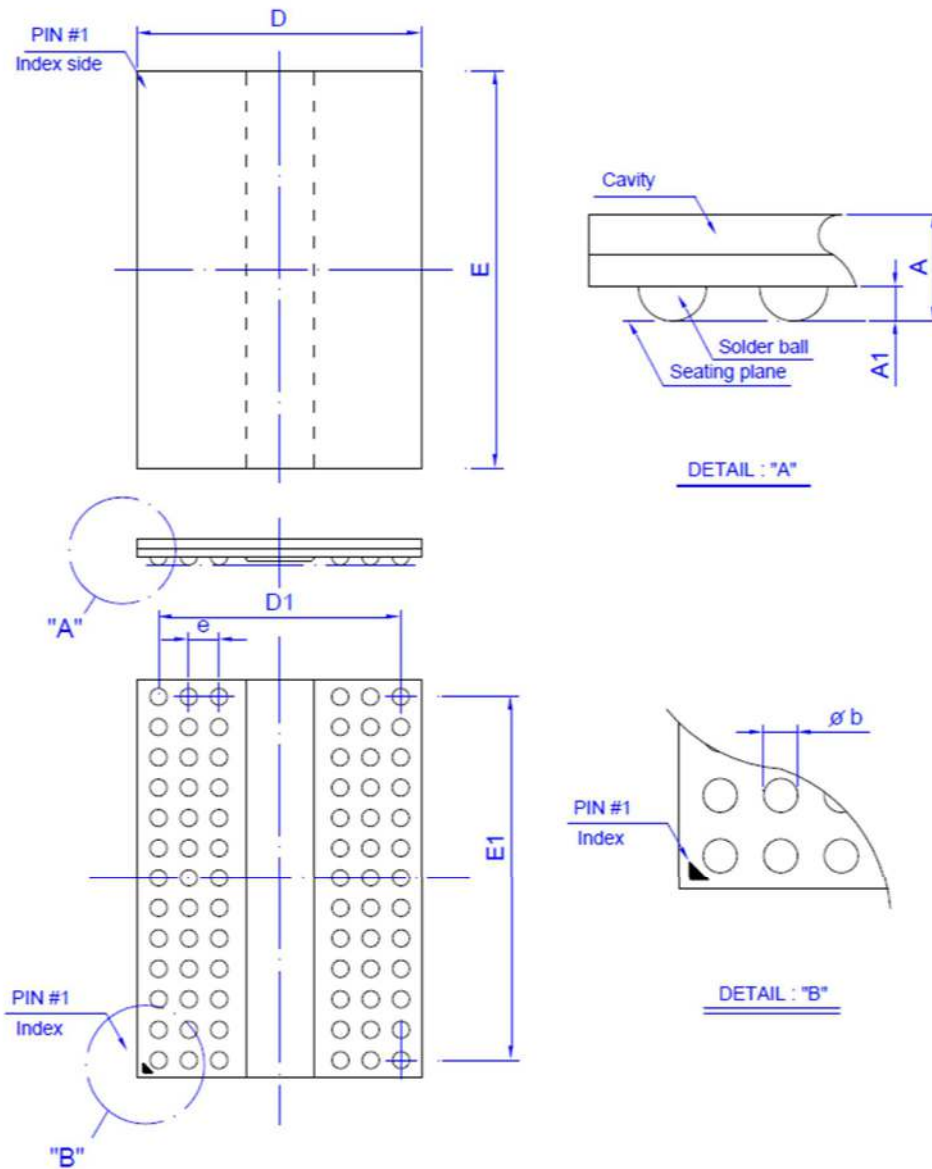
Illustration of tangent line for hold time tDH (for DQ with respect to strobe)


$$\text{Hold Slew Rate} = \frac{\text{tangent line [VREF(DC) - VIL(DC)max]}}{\Delta TR}$$

Rising Signal

$$\text{Hold Slew Rate} = \frac{\text{tangent line [VIH(DC)min - VREF(DC)]}}{\Delta TF}$$

Falling Signal

PACKING DIMENSIONS
78-BALL DDR SDRAM (7.5x10.5 mm)


| Symbol | Dimension in mm | | | Dimension in inch | | |
|----------------|-----------------|-------|-------|-------------------|-------|-------|
| | Min | Norm | Max | Min | Norm | Max |
| A | | | 1.00 | | | 0.039 |
| A ₁ | 0.29 | 0.34 | 0.40 | 0.011 | 0.013 | 0.016 |
| Φ_b | 0.40 | 0.45 | 0.52 | 0.016 | 0.018 | 0.021 |
| D | 7.40 | 7.5 | 7.6 | 0.291 | 0.295 | 0.299 |
| E | 10.40 | 10.50 | 10.60 | 0.409 | 0.413 | 0.417 |
| D ₁ | 6.40 BSC | | | 0.252 BSC | | |
| E ₁ | 9.60 BSC | | | 0.378 BSC | | |
| e | 0.80 BSC | | | 0.031 BSC | | |

Controlling dimension : Millimeter.