5W Wireless Power Receiver for WPC/Qi BPP

Features

- Single-Chip Solution for 5Watt wireless power
- WPC/Qi v1.3 Standards Compliant
- 97% Peak Efficiency from Coil to $5V_{OUT}$ in LDO mode
- Full Synchronous Rectification with Low-R_{DSON}
- 5V LDO Mode or Pass-Through Mode configurable
  - Up to 1.5A peak output current
  - Pass-Through Mode for increased efficiency
  - Short-circuit protection and current limiting
- Embedded Microcontroller and OTP Memory
- Configurable Foreign Object Detection (FOD)
- Standard Firmware with optional external resistor configuration of FOD operating parameters
- Optional I^2C connection for monitoring/configuration and system performance analysis
- Device Enable control pin for extremely low power consumption while in disabled mode
- Optional open-drain Interrupt output pin
- Proprietary, robust internal Over-Voltage Protection
  - Without any external "Sink" resistor or other devices
- Optional external NTC Over-Temperature Protection
- -40°C to 85°C operating temperature range
- 52-bump WLCSP 2.66 x 3.90mm (0.4mm pitch)

Brief Description

The KTE7000 is a single-chip 5Watt wireless power receiver that conforms to WPC/Qi standards v1.3 Baseline Power Profile (BPP) specifications. A wireless power receiver provides regulated DC output power derived from AC power that is magnetically coupled into a connected wireless power receiver coil.

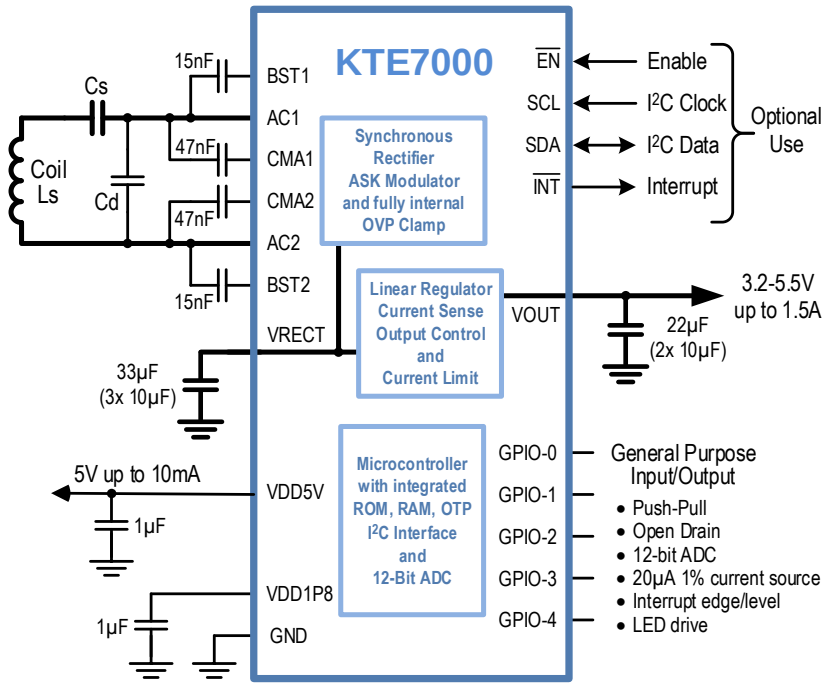
The KTE7000 integrates a full-synchronous rectifier and an LDO to efficiently convert the wireless AC power into 5V DC output power at up to 1.5A. An embedded microcontroller with ROM and OTP memory provides power management, protection, and communications with the power transmitter.

The KTE7000 is packaged in an advanced, fully "green" compliant, 2.66mm x 3.90mm, 52-bump Wafer-Level Chip-Scale Package (6x9 WLCSP).

Applications

- Mobile Internet Devices, IoT, Accessories
- Battery Powered Medical, Industrial, Consumer
- Wireless Headsets, Headphones, Earbuds

Typical Application

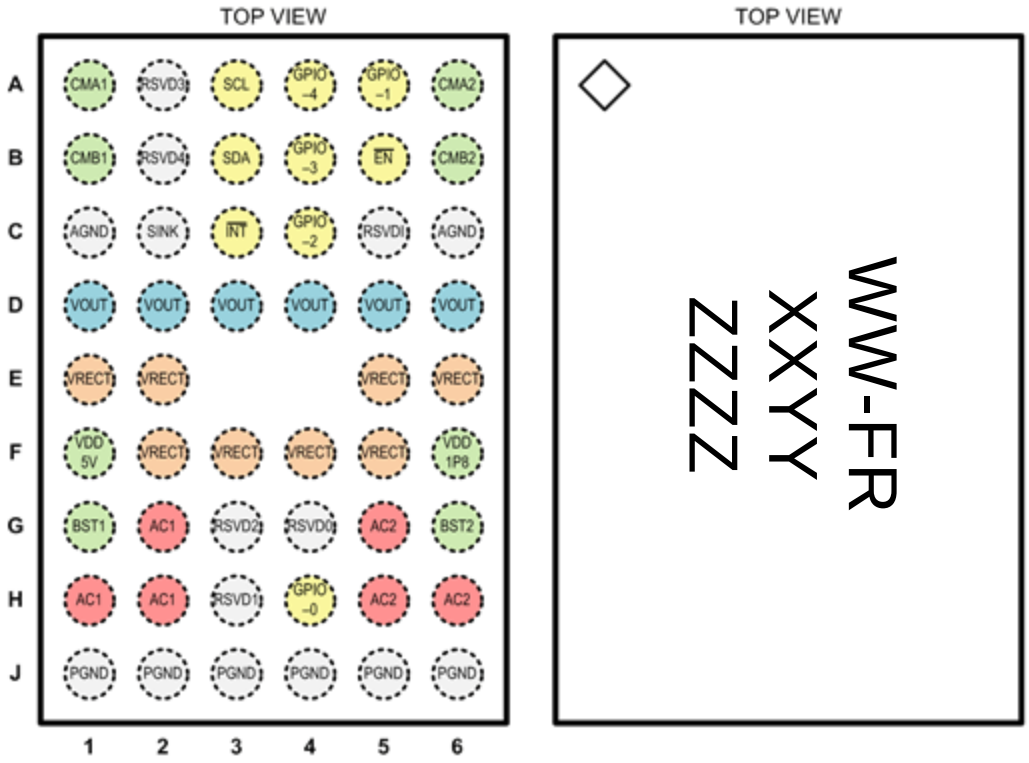


Pin Descriptions

Pin #	Name	Function
G2, H1, H2	AC1	AC Power Input 1 – input to synchronous rectifier. Connect to power input resonant LC tank.
G5, H5, H6	AC2	AC Power Input 2 – input to synchronous rectifier. Connect to power input resonant LC tank.
E1, E2, E5, E6, F2, F3, F4, F5	VRECT	Rectifier DC Output Voltage and LDO Input – connect external bypass/bulk capacitors from these pins to the ground plane using multiple vias.
D1, D2, D3, D4, D5, D6	VOUT	LDO Output Voltage – connect external bypass/bulk capacitors from these pins to the ground plane using multiple vias. Supports 5V output into loads up to 1.5A.
F1	VDD5V	Internal 5V LDO Bias – connect an external 1µF bypass capacitor from this pin to the ground plane using an unshared via. Supports 5V loads up to 10mA.
F6	VDD1P8	Internal 1.8V LDO Bias – connect an external 1µF bypass capacitor from this pin to the ground plane using an unshared via.
G1	BST1	Bootstrap 1 – gate driver charge pump for internal synchronous rectifier AC1 high-side MOSFET. Connect a 15nF capacitor from this pin to AC1.
G6	BST2	Bootstrap 2 – gate driver charge pump for internal synchronous rectifier AC2 high-side MOSFET. Connect a 15nF capacitor from this pin to AC2.
A1	CMA1	Communication Load Capacitance for AC1 – connect a capacitor from this pin to AC1. Capacitor value is typically 22nF-47nF and should be optimized for the application..
A6	CMA2	Communication Load Capacitance for AC2 – connect a capacitor from this pin to AC2. Capacitor value is typically 22nF-47nF and should be optimized for the application.
B1	CMB1	Optional Communication Load Capacitance for AC1 – normally not connected; leave floating.
B6	CMB2	Optional Communication Load Capacitance for AC2 – normally not connected; leave floating.
B5	$\overline{EN}$	Active-Low Enable Input – connect to ground or logic 0 to enable the IC.
A3	SCL	I^2C Clock Input – connect to the master's I^2C clock output and a pull-up resistor to the system I/O voltage rail. Connect to ground if not used.
B3	SDA	I^2C Data Input/Output – connect to the master's I^2C data line and a pull-up resistor to the system I/O voltage rail. Connect to ground if not used.
C3	$\overline{INT}$	Active-Low Interrupt Open-Drain Output – connect to the master's interrupt input and a pull-up resistor to the system I/O voltage rail. Connect to ground if not used.
A4, A5, B4, C4, H4	GPIO-n	General Purpose Input/Outputs – optional configuration pins for NTC, FOD gain and offset, and LDO vs. Pass-Through mode. Leave floating (N.C.) for default configuration.
C2	SINK	High voltage clamp - internally connected to VRECT. Preferred configuration is to connect this pin externally to VRECT. For simplified layout, leave as floating (no connect).
A2, B2, C5, G3, G4, H3	RSVDn	Reserved – not used in the application; connect to ground.
J1, J2, J3, J4, J5, J6	PGND	Power Ground – connect to the ground plane using multiple vias.
C1, C6	AGND	Analog Ground – connect to the ground plane using unshared vias.

Pinout Diagram

WLCSP69-52



52-bump 2.66mm x 3.90mm x 0.620mm
WLCSP Package, 0.4mm pitch

Top Mark
WW = Device ID, FR = Firmware Code
XX = Date Code, YY = Assembly Code
ZZZZ = Serial Number

Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
V_{AC}	AC1, AC2 to PGND	-0.3 to 26	V
V_{RECT}	VRECT to PGND	-0.3 to 26	V
$V_{RECT-AC}$	VRECT to AC1, VRECT to AC2	-0.3 to 26	V
V_{SINK}	SINK to PGND	-0.3 to 26	V
$V_{PGND-AGND}$	PGND to AGND	-0.3 to 0.3	V
V_{OUT}	VOUT to AGND	-0.3 to 26	V
$V_{RECT-OUT}$	VRECT to VOUT	-0.3 to 26	V
V_{BST}	BST1, BST2 to AGND	-0.3 to 26	V
V_{BST-AC}	BST1 to AC1, BST2 to AC2	-0.3 to 6	V
V_{CM}	CMA1, CMA2, CMB1, CMB2 to AGND	-0.3 to 26	V
V_{DD5V}	VDD5V to AGND	-0.3 to 6	V
V_{DD1P8}	VDD1P8 to AGND	-0.3 to 2	V
$V_{\overline{EN}}$	$\overline{EN}$ to AGND	-0.3 to 28	V
V_{I2C}	SCL, SDA, $\overline{INT}$ to AGND	-0.3 to 6	V
V_{GPIO}	GPIO-0, GPIO-1, GPIO-2, GPIO-3, GPIO-4 to AGND	-0.3 to V_{DD5V}+0.3	V
V_{RSVD}	RSVD0, RSVD1, RSVD2, RSVD3, RSVD4, RSVDI to AGND	-0.3 to V_{DD5V}+0.3	V
I_{AC}	AC1, AC2 Current	2.6	A
I_{OUT}	VOUT Current	2.6	A
T_J	Operating Temperature Range	-40 to 150	°C
T_S	Storage Temperature Range	-55 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	260	°C

ESD Ratings[2]

Symbol	Description	Value	Units
V_{ESD_HBM}	JEDEC JS-001-2017 Human Body Model (all pins)	±2	kV

Thermal Capabilities[3]

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance – Junction to Ambient	47	°C/W
Θ_{JB}	Thermal Resistance – Junction to Board	4.38	°C/W
P_D	Maximum Continuous Power Dissipation at 25°C (T_J = 125°C)	2.13	W
$\Delta P_D/\Delta T$	Derating Factor Above T_A = 25°C	-21.3	mW/°C

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
2. ESD Ratings conform to JEDEC industry standards. Some pins may actually have higher performance.
3. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.

Recommended Operating Conditions

Symbol	Description	Value	Units
C_{DD5V}	VDD5V Capacitor	1	µF
C_{DD1P8}	VDD1P8 Capacitor	1	µF
C_{RECT}	VRECT Capacitor(s) (≥25V rating)	3x10 or 1x33	µF
C_{OUT}	VOUT Capacitor(s)	2x10 or 1x22	µF
	VOUT Effective Capacitance (at 5V DC bias)	>8	µF
I_{OUT}	VOUT Current	0 to 1.5	A
I_{VDD5V}	VDD5V Current (output available for application circuit)	0 to 10	mA
T_A	Ambient Operating Temperature Range	-40 to 85	°C
T_J	Die Operating Temperature Range	-40 to 125	°C

Ordering Information

Part Number	Marking[4]	Operating Temperature	Package
KTE7000ENAA-__-TB[5]	PKFRXXYYZZZZ	-40°C to +85°C	WLCSP69-52

4. “PK” is the KTE7000 device ID, “FR” is the firmware code, “XX” is the date code, “YY is the assembly code, and “ZZZZ” is the serial number.

5. Firmware code is included in the ordering part number. Please contact Kinetic Sales for further details.

Electrical Characteristics[6]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C. Typical values are specified at T_A = +25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
Supply Specifications						
V_{UVLO}	VRECT Under-Voltage Lockout	V_{RECT} rising threshold		3.06	3.2[7]	V
		Hysteresis		150		mV
I_{RECT}	VRECT Quiescent Current	$\overline{EN}$ = 0, V_{RECT} = 7V		4.5		mA
I_{SHDN}	VRECT Shutdown Current	$\overline{EN}$ = 1, V_{RECT} = 7V		18		µA
V_{DD5V}	VDD5V Output Voltage	$I_{LOAD} \leq$ 10mA	4.5	5	5.5	V
V_{DD1P8}	VDD1P8 Output Voltage	No external load	1.62	1.8	1.98	V
Thermal Shutdown Specifications						
T_{J_SHDN}	IC Junction Thermal Shutdown	T_J rising threshold		140		°C
		Hysteresis		20		°C
Logic Pin Specifications ($\overline{EN}$, $\overline{INT}$, GPIO-n)						
V_{IH}	Input Logic High ($\overline{EN}$)		1.4			V
V_{IL}	Input Logic Low ($\overline{EN}$)				0.3	V
I_{I_LK}	Input Logic Leakage ($\overline{EN}$)	T_A = 25°C, V_I = 0V or 5V	-1		1	µA
V_{OL}	Output Logic Low ($\overline{INT}$)	I_{O_SINK} = 5mA			0.4	V
I_{O_LK}	Output Logic Leakage ($\overline{INT}$)	T_A = 25°C, V_O = high-Z or 5V	-1		1	µA
I_{O_SRC}	Output I_{SOURCE} (GPIO-n)		19.80	20	20.20	µA
I_{O_SRC}	Output I_{SOURCE} (GPIO-1,2,3,4)		19.65	20	20.35	µA
I²C Interface Specifications (SCL, SDA), see Figure 1.						
V_{IH}	Input Logic High Threshold		1.4			V
V_{IL}	Input Logic Low Threshold				0.4	V
V_{OL}	SDA Output Logic Low	I_{SDA} = 5mA			0.4	V
t_1	SCL clock period		2.5			µs
t_2	Data in setup time to SCL high[8]		100			ns
t_3	Data out stable after SCL low		0			ns
t_4	SDA low setup time to SCL low (Start)[8]		100			ns
t_5	SDA high hold time after SCL high (Stop)[8]		100			ns
Synchronous Rectifier Specifications						
R_{DS_SW}	Rectifier Switch Drain-Source On-Resistance	I_{SW} = 0.5A		40		mΩ
CMA1, CMA2, CMB1, CMB2, SINK Specifications						
R_{ON_CM}	CMxx On Resistance	I_{CMxx} = 200mA		1		Ω
I_{CM_LK}	CMxx Leakage Current	V_{CMxx} = 20V		1		µA
I_{SINK_LK}	SINK Leakage Current	V_{SINK} = 20V		1		µA

6. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

7. Value is guaranteed only at room temperature.

8. Guaranteed by design, not tested in production.

Electrical Characteristics (continued)[6]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C. Typical values are specified at T_A = +25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
VOUT LDO Specifications						
V_{OUT}	Output Mode	V_{RECT} = 5.30V	4.85	5	5.15	V
V_{OUT_LDR}	VOUT Load Regulation	LDO Mode		12		mV/A
V_{OUT_LNR}	VOUT Line Regulation	LDO Mode		4		mV/V
I_{OUT_PEAK}	Peak Current Capability		1.5			A
$V_{RECT-OUT}$	VRECT to VOUT Dropout Voltage	I_{OUT} = 1A; V_{RECT} droops 10% below the LDO regulated output value		50	100	mV
V_{OUT_OV}	Overvoltage Threshold	Rising		15		%
		Falling		10		
I_{OUT_OVSINK}	Overvoltage Sink Current	V_{OUT} greater than V_{OUT_OV} threshold		10		mA
ADC Specifications						
V_{ADC_FS}	ADC Full Scale Voltage[8]			2.048		V
f_{SAMPLE}	ADC Sample Rate[8]			200		kSa/s
N	ADC Output Resolution[8]			12		bit
DNL	ADC Differential Nonlinearity			2		LSB
INL	ADC Integral Nonlinearity			2		LSB

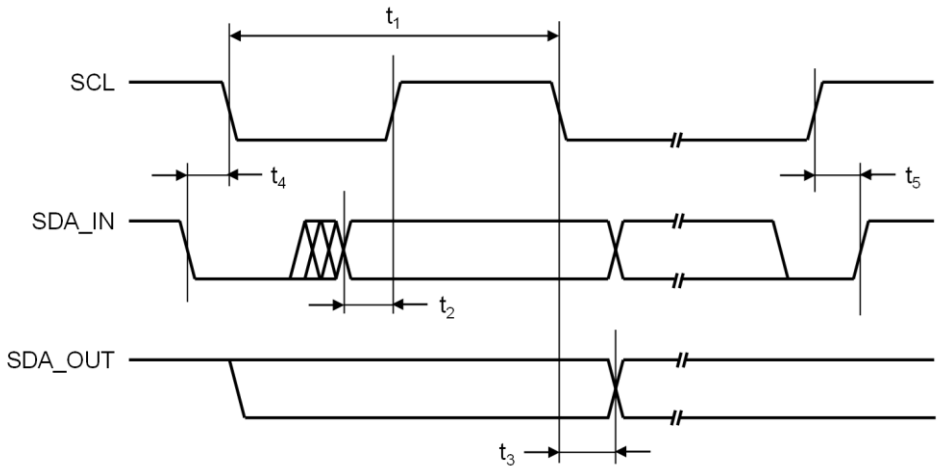
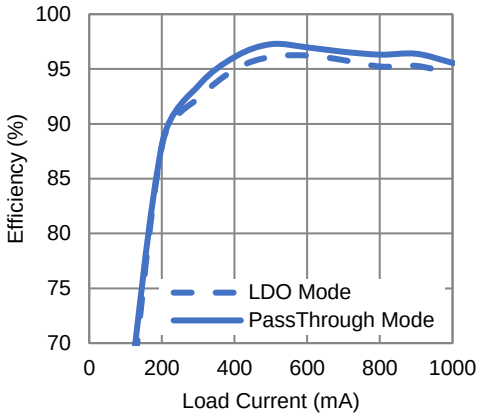


Figure 1. I²C Compatible Interface Timing Diagram

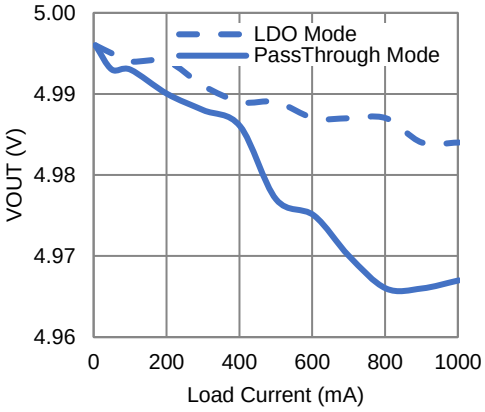
Typical Characteristics

Unless otherwise noted, V_{OUT} = 5V, T_A = 25°C.

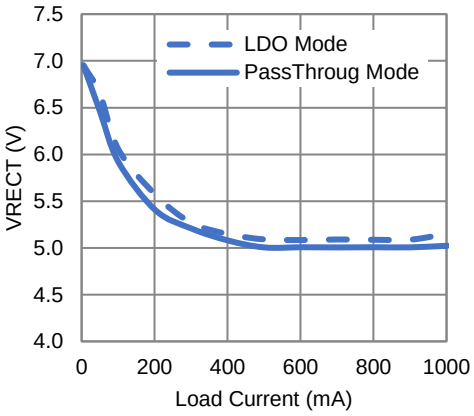
Efficiency (Coil to VOUT) vs. Load



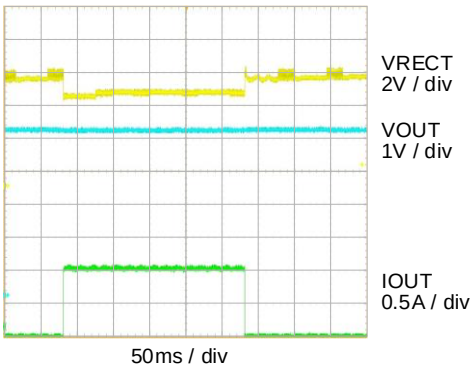
VOUT vs. Load



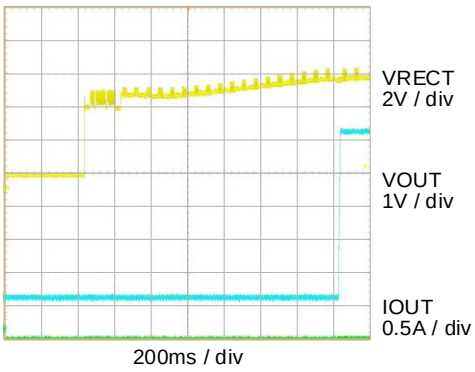
VRECT Profile vs. Load



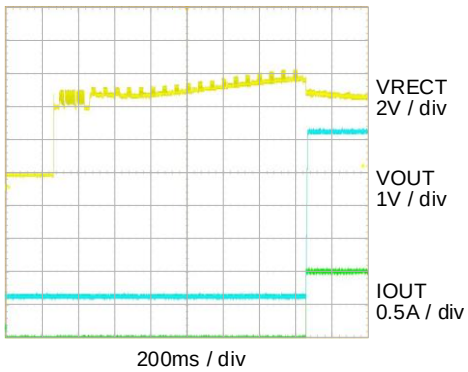
BPP, VOUT = 5V, 0 to 1A Load Transient



BPP, VOUT = 5V, Startup Without Load



BPP, VOUT = 5V, Startup With 1A Load



Detailed Application Schematic

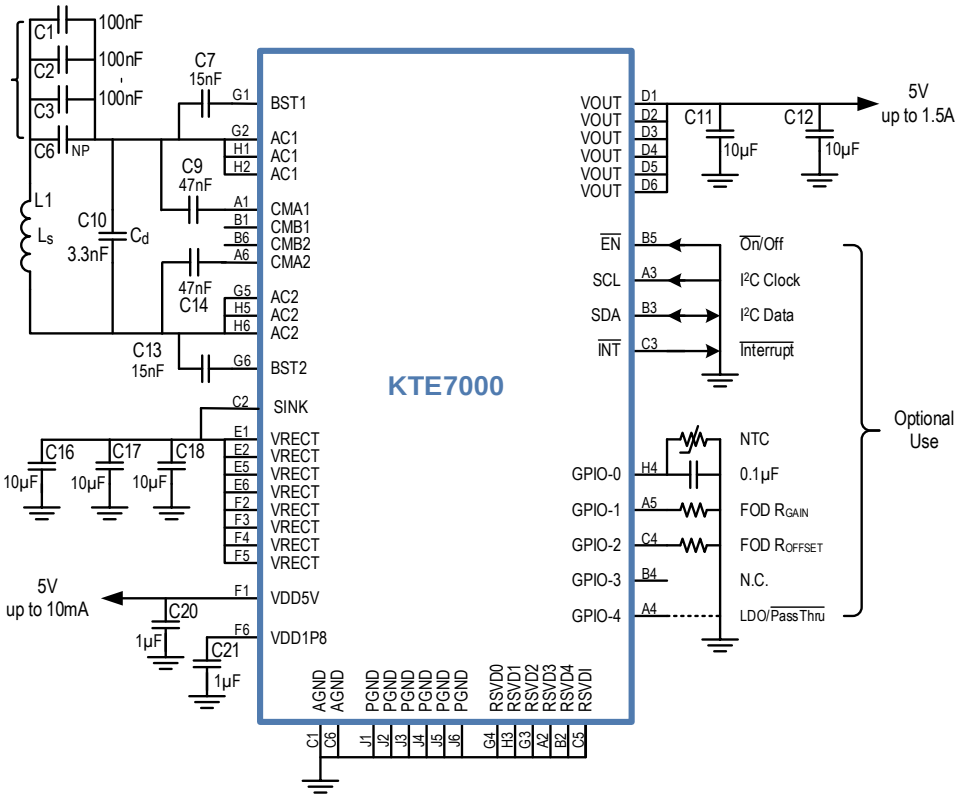


Figure 2. Detailed Application Schematic

BOM

Item	Quantity	Reference	Description	Value	Manufacturer
1	4	C1, C2, C3	CAP CER 0.1µF 50V X7R	100nF	Murata
2	2	C7, C13	CAP CER 0.015µF 50V X7R	15nF	Yageo
3	1	C10	CAP CER 3300PF 50V X7R	3.3nF	Yageo
4	2	C9, C14[9]	CAP CER 47nF 50V X7R	47nF	Murata
5	3	C16, C17, C18[10]	CAP CER 10µF 25V X5R	10µF	Murata
5	2	C11, C12[10]	CAP CER 10µF 10V (or 6.3V) X5R	10µF	Murata
6	2	C20, C21	CAP CER 1µF 10V X5R	1µF	Yageo
7	1	U1	Wireless charger receiver	KTE7000	Kinetic Technologies
8	1	RX COIL	WPC receiver coil, ACR = 0.22Ω p/n ASC-504060E00-S00	8.2µH	Amotech

9. The optimum capacitor value depends strongly on the electro-mechanical properties of the receiver coil and target operating range. The traditional 47nF value is larger than needed for most applications and newer designs are typically using 33nF or 22nF.

10. For low-cost applications and where device height is not critical, multiple devices may be replaced by single devices or fewer devices of equivalent total value. For large capacitor values, electrolytic capacitors may be used with a 0.1µF ceramic capacitor in parallel.

Functional Description

The KTE7000 is a single-chip 5W wireless power receiver that conforms to WPC/Qi v1.3 Baseline Power Profile (BPP) standards. This device is fully compatible with all WPC/Qi certified transmitters and will operate in BPP mode (Baseline Power Profile) when interoperating with BPP Transmitters or when interoperating with EPP (Extended Power Profile) transmitters. A wireless power receiver provides regulated DC output power derived from AC power that is magnetically coupled into the wireless power receiver coil.

The KTE7000 integrates a full-synchronous rectifier and an LDO to efficiently convert the wireless AC power into 5V DC power at up to 1.5A. An embedded microcontroller with ROM and OTP memory provides power management, protection, and communications with the power transmitter.

Full-Bridge Synchronous Rectifier

The KTE7000 includes a full-bridge synchronous rectifier comprised of four low-R_{DSON} MOSFET switches for high-efficiency AC-to-DC power conversion. The AC input to the rectifier is at pins AC1 and AC2, while the unregulated DC output is from pins VRECT to PGND. The rectified DC voltage and energy are stored in off-chip bulk capacitors connected to the VRECT pin.

Proprietary Overvoltage Protection

Fully internal proprietary overvoltage protection actively prevents damage to the KTE7000 from transient overvoltage events. This includes various possible application scenarios, including “jiggle” events that can occur when dynamically moving the receiver coil in relation to the transmitter surface. Conventional solutions typically rely upon external resistors and/or other devices to dissipate excess energy in attempts to prevent overvoltage damage. External devices are often physically too small to safely manage overvoltage without damage. The KTE7000 utilizes proprietary overvoltage protection that is more robust and does not require any external components.

LDO Mode

The KTE7000 integrates a high-power, low-dropout (LDO) linear regulator that provides a stable and accurate DC output for system loads up to 1.5A.

The LDO input is internally connected to the rectifier’s output at VRECT, and the regulated output voltage is available at VOUT. Communications from the KTE7000 with the WPC transmitter automatically adjusts the transmitter’s output power such that the KTE7000’s rectifier output maintains the proper headroom for optimum operation of the LDO.

The LDO Mode is appropriate for applications that require a regulated 5V system rail. Select the default LDO Mode by leaving the GPIO-4 pin floating (no connect) or tie this pin to VDD1P8.

Pass-Through Mode

The KTE7000 includes a Pass-Through Mode for the LDO. In the Pass-Through Mode, the LDO is set to the normal target regulator output voltage. However, the KTE7000 firmware communicates back to the WPC transmitter to maintain VRECT only slightly higher than the target VOUT voltage at higher power levels. This reduces the power dissipation normally associated with the voltage drop across an LDO necessary to maintain complete VOUT regulation at high output currents. At low output current, some headroom is maintained. This is necessary to prevent excessive VOUT drop caused by coil physics in the case when there is a sudden large increase in the output load.

The Pass-Through Mode is appropriate for battery charging or other applications that prioritize highest efficiency over output voltage accuracy. Select the Pass-Through Mode by connecting the GPIO-4 pin to ground.

Under-Voltage Protection

The KTE7000 includes under-voltage protection when VRECT falls approximately 3.5V. This temporarily disables VOUT as to give the system a chance to restore normal operation. This can avoid resetting the KTE7000 from undervoltage conditions. Resetting of KTE7000 will result in forced termination of the power transfer from the power transmitter.

Output Overvoltage Protection

The KTE7000 includes output overvoltage protection that applies a 10mA current sink to VOUT whenever the output voltage exceeds its nominal regulation set-point by more than 15%. The current sink is disabled when the output voltage returns to within 10% above nominal. This quickly reduces the VOUT voltage to normal after any VOUT increase that may occur when there is a sudden decrease in the VOUT load current.

Embedded Microcontroller and OTP Memory

The KTE7000 includes an embedded microcontroller with one-time programmable (OTP) memory configured with firmware that conforms to WPC/Qi v1.3 standards.

Standard Firmware

The standard firmware in the KTE7000 meets WPC/Qi v1.3 specifications and can operate autonomously without any interaction with an optional host applications processor. Although this firmware is pre-programmed, optional external resistors can be added to implement commonly needed adjustments such as changing the FOD (Foreign Object Detection) settings.

Optional $\overline{EN}$ Input

The KTE7000 has an optional $\overline{EN}$ logic input pin to enable and disable the IC into a low power state. Connect the $\overline{EN}$ pin to ground to allow the device to function whenever there is sufficient VRECT for operation. In applications where it is useful to enable/disable the device, drive the $\overline{EN}$ pin with an appropriate voltage for the disabled state.

Optional I^2C Interface and $\overline{INT}$ Flag

The KTE7000 includes an optional I^2C serial interface and an open-drain interrupt flag. These interfaces may be used with Kinetic engineering development tools, and also, to support additional new functionality implemented by future versions of KTE7000 firmware.

GPIO Pins and Optional Configuration

The KTE7000 has five GPIO pins, GPIO-0 through GPIO-4, which are used for optional input/output features and for option configuration. The configurable adjustments include NTC over-temperature protection (GPIO-0), FOD gain (GPIO-1), FOD offset (GPIO-2), and LDO Mode vs. Pass-Through Mode (GPIO-4). At present, GPIO-3 is reserved for future and custom use and should be left floating (no connect).

Each GPIO may be optionally configured to have connected a 20µA high precision current source. Depending upon the application needs, this pin may be left floating (no connect), shorted to ground, or connected to an external configuration resistor. The voltage on the pin is measured by the integrated ADC and interpreted by firmware. See the *Applications Information* section in this datasheet for details regarding selecting optional resistor values.

Optional NTC Over-Temperature Protection

Pin GPIO-0 is configured to bias and measure an external negative temperature coefficient (NTC) thermistor. Typically, this feature is used to detect over-temperature near the receiver coil and transmitter coil interface.

The KTE7000 sends an End Power packet with the condition code “over temperature” when the voltage on GPIO-0 is less than 328mV, corresponding to a high temperature condition. Qi transmitters are required to shut off immediately upon receiving this code. Generally, all Qi transmitters will shut down for a long period of time to allow the receiver to cool down before attempting to restart the power transfer.

The GPIO-0 pin sources 20µA, which is converted to a temperature-dependent voltage by the thermistor. In applications with over-temperature protection, normally select an NTC thermistor with $R_{25°C}$ = 47kΩ and β = 4050 to disable wireless power when the NTC temperature exceeds 50°C. The temperature threshold may be adjusted via NTC selection and even adding additional normal resistors around the NTC. See the *Applications Information* section in this datasheet for details on selecting the thermistor.

If not using the NTC, leave the GPIO-0 pin floating (not connected to anything).

Optional FOD Gain and Offset Adjustment

FOD is an acronym for “Foreign Object Detection”. FOD is a mandatory safety feature required by the WPC specifications. The purpose of FOD is to prevent possibly dangerous heating of metal objects (‘foreign’ objects). Such heating can result from objects having exposure to the magnetic charging field from the wireless power transmitter. It is a requirement for the wireless power receiver to accurately report the received power as packet data sent to the transmitter. The transmitter compares the reported received power to the amount of power being transmitted. If too much power is being lost, the transmitter may stop delivering power for reason of power lost into a possible foreign object.

The Kinetic EVB (Evaluation Board) is highly efficient, having a very high-quality coil and being constructed without any “friendly” metals in the magnetic charging field area. The EVB power measurement and FOD related parameters are very accurately calibrated and do not need any adjustment. However, a final application configuration may have a different receiver coil or may have metal components (screws, frame, battery, PCB wiring, etc.) nearby the receiver coil. Such “friendly” metal will increase the power lost in the wireless power receiver system. These power loss differences must be compensated so that the amount of power reported by the receiver in the Received Power Packet (RPP) is accurate and within WPC specification requirements.

The KTE7000 includes optional resistor adjustments for Foreign Object Detection (FOD) Gain and Offset to allow proper calibration across varying applications. Typically, real product applications will have losses that are greater than the losses that exist in the calibrated EVB. For this reason, most of the adjustment range is a positive value. For losses that are proportional to the power level, the FOD Gain can be adjusted. For losses that are a constant amount regardless of the power level, the FOD Offset value can be adjusted. Both of these adjustments affect the value contained in the RPP packet that is communicated to the power transmitter.

To adjust FOD Gain and FOD Offset, external resistors can be attached to KTE7000 GPIO pins to make the required change. For details about this adjustment, refer to the *Optional FOD R_{GAIN} Selection* and *Optional FOD R_{OFFSET} Selection* sections within the *Applications Information* of this datasheet. If the default Gain and/or Offset values can be used without any change, then leave the respective GPIO pin floating (not connected to anything).

Applications Information

Coil Selection

Select a coil that meets the needs of the application. Consider form-factor, series resistance and inductance. Larger diameter coils generally perform better. The coil should include a low-loss magnetic shielding material that is sufficient to prevent magnetic flux from interacting with metallic objects behind the coil or very close to the coil windings. To obtain WPC/Qi certification, the receiver must work with all WPC/Qi certified transmitters.

Capacitor Selection

Ceramic capacitors with X5R, X6S, or X7R ratings are recommended due to their low ESR, low ESL, low temperature coefficients, and small physical sizes. Consider the voltage rating, size, and DC bias derating characteristic of the capacitor.

Cs and Cd Capacitor Selection

Choose Cs and Cd per the guidelines set forth by the WPC/Qi v1.3 BPP specifications. Use small ceramic capacitors with 50V or more rating.

Select the value of Cs for primary resonance at 100kHz:

$$f_s = \frac{1}{2\pi\sqrt{L'_s C_s}} = 100kHz$$

where L'_S is the self-inductance of the coil when placed and aligned on the interface surface of a power transmitter.

Select the value of Cd for secondary resonance at 1MHz:

$$f_d = \frac{1}{2\pi\sqrt{L_s\left(\frac{1}{C_s}+\frac{1}{C_d}\right)^{-1}}} = 1MHz$$

where L_S is the self-inductance of the coil when away from the interface surface of a power transmitter, but including any “friendly” magnetic material that is part of the receiver design.

C_{BSTn} Capacitor Selection

Choose ceramic boost capacitors with voltage rating of 50V and 15nF nominal capacitance. Typically, 0402 (1005M) case-size is sufficient.

C_{CMAn} Capacitor Selection

Choose ceramic modulation capacitors with voltage rating of 50V and 47nF nominal capacitance. Typically, 0402 (1005M) case-size is sufficient.

C_{RECT} Capacitor Selection

Choose ceramic rectifier output capacitor(s) with voltage rating of 25V or more and 30µF total nominal capacitance or more. Typically, three 10µF capacitors in parallel, each with 0603 (1608M) case-size or larger, is a good choice. Larger values and larger case-size provide more effective capacitance when considering the DC bias derating characteristic of the capacitor. If a low-cost electrolytic type capacitor is used, an additional 0.1µF capacitor should be placed in parallel with the electrolytic capacitor.

C_{OUT} Capacitor Selection

Choose ceramic LDO output capacitor(s) with voltage rating of 10V or more and 20µF total nominal capacitance or more. Typically, two 10µF capacitors in parallel, each with 0603 (1608M) case-size or larger, is a good choice. Larger values and larger case-size provide more effective capacitance when considering the DC bias derating characteristic of the capacitor. The LDO requires a minimum of 8µF *effective* output capacitance. If a low-cost electrolytic type capacitor is used, an additional 0.1µF capacitor should be placed in parallel with the electrolytic capacitor.

C_{VDD5V} and C_{VDD1P8} Capacitor Selection

Choose ceramic VDD5V and VDD1P8 output capacitors with voltage rating of 6.3V or more and 1µF nominal capacitance each. Typically, 0402 (1005M) case-size is sufficient.

C_{NTC} Capacitor Selection

When using the optional NTC thermistor, place a 0.1µF ceramic bypass capacitor from GPIO-0 to ground, local to the IC, in order to reject noise. If not using the NTC, leave the GPIO-0 pin floating (no connect).

Optional NTC Thermistor Selection

The KTE7000 is optimized for an NTC thermistor with $R_{25°C}$ = 47kΩ and β = 4050 to disable wireless power when the NTC temperature exceeds 50°C. Thermistor resistance vs. temperature is given as:

$$R_T = R_{298°K}\left[e^{\beta\left(\frac{1}{T}-\frac{1}{298°K}\right)}\right]$$

where T is in degrees Kelvin, 0°C = 273°K, 25°C = 298°K and 50°C = 323°K.

The GPIO-0 pin is configured as a 20µA current source to bias the NTC. As temperature increases, the thermistor resistance reduces, causing the voltage at GPIO-0 to also reduce. An over-temperature condition at 323°K = 50°C rising threshold is detected when the NTC resistance falls below 16,416Ω, which corresponds to a 328mV falling threshold at GPIO-0.

To increase the over-temperature protection threshold, add resistance in series with the NTC and/or choose an appropriate different NTC device. For example, with the suggested NTC device, add a 5.1kΩ normal resistor in series for a 333°K = 60°C rising threshold.

To decrease the over-temperature protection threshold, add resistance in parallel with the NTC. For example, with the suggested NTC device, add a 91kΩ normal resistor in parallel for a 318°K = 45°C rising threshold.

Thermistors with different beta (β) temperature characteristic may be used. Use the above thermistor formula with the GPIO-0 pin's 20µA current source value, a 328mV falling threshold, and Ohm's Law (V = I*R) to calculate the over-temperature threshold and adjust as necessary.

If not using the NTC, leave the GPIO-0 pin floating (not connected to anything).

Optional FOD R_{GAIN} Selection

If necessary, add an optional resistor from GPIO-1 to ground to adjust the FOD gain. The adjustment changes the calculation of the total received power value that is communicated to the transmitter in the Received Power Packet (RPP). This adjustment can be made using the following table values. Resistor tolerance must be 1% or better for guaranteed selection of the desired FOD gain value. Please note that the resistor value is measured only at the time of the initial power-on time of the receiver.

Table 1. FOD R_{GAIN} Selection

FOD R_{GAIN}	RPP Gain Change
R_{GAIN} and R_{OFFSET} <1k	+1.4W added to RPP
<1k	-4.7%
5k	-3.1%
10k	-1.6%
15k	+1.6%
20k	+3.1%
25k	+4.7%
30k	+6.3%
35k	+7.8%
40k	+9.3%
45k	+10.9%
50k	+12.5%
Floating (no connect)	0%

Optional FOD R_{OFFSET} Selection

If necessary, add an optional resistor from GPIO-2 to ground to adjust the FOD offset. The adjustment changes the calculation of the total received power value that is communicated to the transmitter in the Received Power Packet (RPP). This adjustment can be made using the following table values. Resistor tolerance must be 1% or better for guaranteed selection of the desired FOD offset value. Please note that the resistor value is measured only at the time of the initial power-on time of the receiver.

Table 2. FOD R_{OFFSET} Selection

FOD R_{OFFSET}	RPP Offset Change
R_{GAIN} and R_{OFFSET} <1k	+1.4W added to RPP
<1k	-117mW
5k	-78mW
10k	-39mW
15k	0
20k	+39mW
25k	+78mW
30k	+117mW
35k	+156mW
40k	+195mW
45k	+234mW
50k	+273mW
Floating (no connect)	0

Recommended PCB Layout

See Figure 3 for the recommended PCB layout. The drawing is to scale. Larger external components are 0603 (1608M) size, while smaller components are 0402 (1005M) size. It is possible to fit the entire solution in under 47mm^2. However, depending upon PCB design and assembly rules, the component-to-component minimum distance may need to be increased.

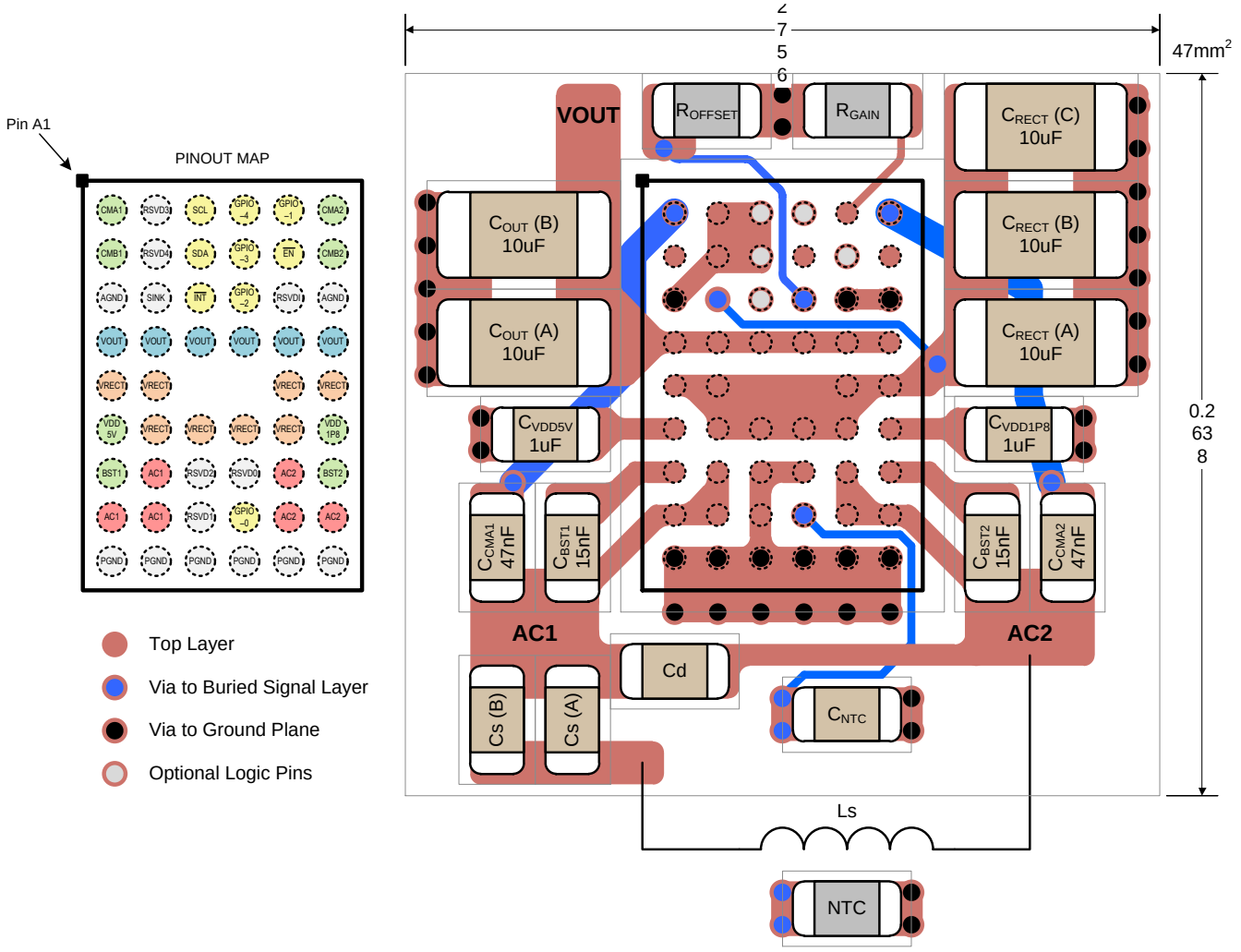


Figure 3. Recommended PCB Layout

The above layout is optimized for good EMI and thermal performance. For diagnostic purposes, it is preferred to route the SCL and SDA pins to test points. If SCL and SDA are used in the application, they are also routed to the host controller I^{2}C bus and pull-up resistors. If not used, the SCL and SDA test points are tied to ground, but in a way that can be disconnected by cutting the PCB trace wires, or by removing zero-ohm resistors. This makes it possible to use I^{2}C for analysis of system performance during development.

Evaluation Kit

The KTE7000 evaluation kit (EVK) is available to aid design-in. Consult an authorized Kinetic Technologies representative for more information.

Notes and Quick-Start Procedure:

1. Connect a voltmeter and a load from VOUT to GND at the top edge of the EVK. Resistive loads, actual circuit loads, and high-quality electronic loads are preferred. Some low-quality electronic loads may have start-up issues and should be avoided.
2. For operation, place the EVK coil area on a Qi certified transmitter with the component side and shield material facing away from transmitter surface. (Thus, the bare PCB material of the EVK is directly touching the transmitter surface). This is important, because all Qi applications require a spacer between the receiver coil and the transmitter surface. The PCB material of the EVK serves as a 1mm spacer for this purpose. If the EVK is placed upside down on the transmitter surface, the shield material on top of the coil will block the magnetic flux from the transmitter, and the EVK will not function at all. Please note that the actual coil winding is not visible, because it is between the shield material and the PCB material.

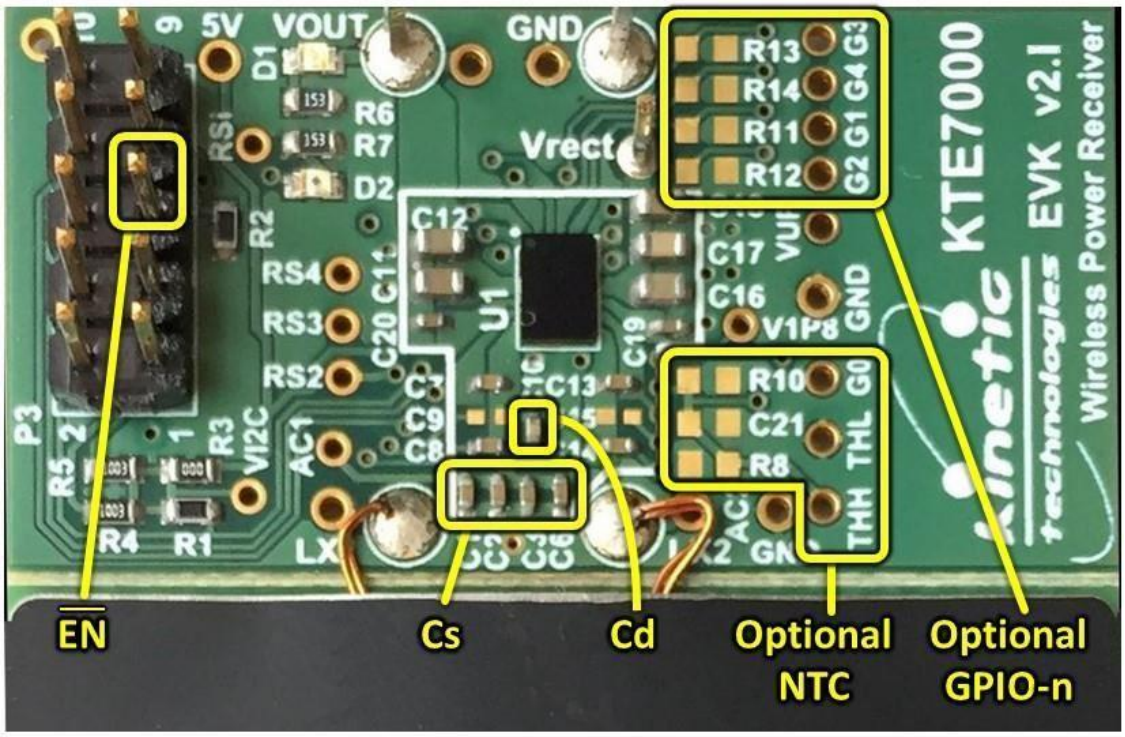


Figure 4. Photo of Evaluation Kit