Datasheet Brief
KTM50x0

For full datasheet, click HERE.

USB Type-C / DisplayPort 1.4 MST Hub (DSC)

Features

- USB Type-C DisplayPort Alt-mode de-mux
  - Simultaneous USB3.2 Gen2 and 2 lanes DP1.4a input OR 4 lanes DP1.4a input
  - Flip option for connector plug orientation
  - DP lane swap and polarity swap
- DisplayPort® (DP) ver.1.4a compliant receiver
  - Link rate 1.62 / 2.74 / 5.4 / 8.1Gbps
  - 1, 2, or 4 lanes configuration
  - MST up to 6 streams (compressed /uncompressed)
  - FEC Decode
  - DSC Transport & Decode
  - AUX CH 1 Mbps
  - HPD_OUT
  - Adaptive receiver equalization
  - TPS4 EQ Phase LT support
  - Scrambling of main link data
  - De-spreading of link frequency
  - Video Stream Handling
    - RGB/ YCC 444/422/420 pixel format up to 16 bpc
    - Up to 1080 Mpix/sec dual pixel path
  - DPCD
    - DPCD data structure revision 1.4
    - DSC support capability & control
    - FEC capability & control
    - SST Split SDP capability
    - VSC_EXT_SDP for VESA & CTA
    - Protocol converter capability & control
    - Virtual DP Peer Device capability & control
    - CEC tunneling over AUX
  - Chainable SDP packets (2KB or more metadata per stream)
  - Adaptive Sync SDP
  - PPS SDPAudio stream handling
    - Non-HBR Compressed Formats
      - 2/8 ch layouts
      - Up to 192kHz sample rates
      - Dolby Digital, Digital+, Atmos
  - HBR Audio Formats
    - 8 ch layout
    - Up to 1536kHz sample rates
    - Dolby TrueHD, Atmos, DTS Master
    - LPCM Formats
    - 2/8/16/32 Ch
    - Up to 192kHz sample rates
    - 3D LPCM, speaker allocation & mapping
  - OneBit DSD Formats
    - 2/8 ch
    - Single & Double Rate
    - 12288 kHz sample rates
  - DST DSD Formats
    - Single/Double rate
    - Up to 22579.2kHz
  - Audio InfoFrame/ ACP/ ISRC/ Audio Metadata DI packets
- Triple DP1.4a / HDMI2.0b (DP++) transmitters
  - DP mode
    - Lane count, Link rate conversion
    - Link rate 1.62 / 2.74 / 5.4 / 8.1Gbps
    - 1, 2, or 4 lanes configuration
    - DSC stream transport with FEC Encode
    - MST up to 6 streams (compressed / uncompressed)
    - AUX CH 1 Mbps
    - 3.3V HPD_IN
  - HDMI mode
    - TX1 & TX3: VML AC coupled HDMI
    - TX2: CML DC-coupled HDMI
    - No External Level shifters needed
    - 600 MHz maximum TMDS character clock
    - TMDS character-clock divide_by_4 mode
    - HPD_IN (5V Tolerant)
    - DDC CH (5V Tolerant)
- HDMI 2.1 Features
  - Through 6GHz TMDS Mode
  - Supports 4k120Hz,4:2:0, 8bpc with Adaptive Sync to VRR conversion
  - Dynamic HDR Metadata through Extended Metadata Packet
  - Supports VRR, FVA, QMS, QFT, ALLM
  - Scrambler for DP/HDMI output
  - Programmable signal amplitude and edge rate control
  - Programmable pre-emphasis control
  - Pixel format RGB / YCC 444/422/420
  - Deep color up to 16 bits per color
  - 3D video timings
  - CEC support – snooping, tunneling
  - SCDC read request handling
  - Metadata handling
  - Conversion to DVI output
  - Link power management

Features (continued)

- USB3.2 compliant re-timer
  - 5Gbps and 10Gbps support
  - Spread spectrum clocking
  - LFPS polling and processing
  - Lane polarity inversion
  - Bit level re-timer for SS mode
  - SRIS (Separate Reference Clock Independent SSC) for SSP mode
  - Adaptive Receiver Equalization
  - Multi-tap FIR EQ Transmitter Emphasis
- Video processing
  - MST to SST conversions or pass-through
  - SST lef-right separation
  - Color space conversion from RGB to YCC
  - Colorimetry support: BT2020, BT709, BT601, and Adobe RGB
  - Color bit depth expansion (10 to 12 bits) 16 bits per color pass through
  - DP to HDMI Stereoscopic 3D Transport
  - Frame sequential to stacked top-bottom conversion
  - Pass through of other 3D formats
  - Programmable coefficient 3x3 matrix
    - Programmable input offset
    - Programmable output offset
    - Programmable output clipping levels
  - Chroma down sampling
    - 5-tap H & V FIR filters with programmable coefficients
    - 12 bits per color input width
    - 12 bits per color output width
    - YCbCr444 to YCbCr420 conversion
    - YCbCr444 to YCbCr422 conversion
  - Pass through for YCbCr444/422/420
  - Dual DSC1.2A stream decoding
  - 1/2/4 Slice DSC1.2Aa RGB/YCC444/422/420 10-b format support
  - FEC decoding / encoding
  - Video Horizontal blanking expansion
  - Pixel stream de-skewing
  - Adaptive Sync Video
- Max video resolution and color depth on DP output uncompressed
  - 5K3K60Hz, RGB/YCbCr444, 8 bpc
  - 8K4K60Hz, YCbCr420 up to 8 bpc
  - 4K2K120Hz, RGB/YCbCr444, 8 bpc
- Max video resolution and color depth on DP output compressed (DSC)
  - 8K4K60Hz, RGB/YCC444 up to 8 bpc
  - 5K3K60Hz, RGB/YCbCr444, 12 bpc
  - 4x 4K2K60Hz, RGB/YCbCr444, 8 bpc
- Max video resolution and color depth on HDMI TX
  - 4Kp60Hz, RGB/YCbCr444, 8 bpc
  - 4Kp60Hz, YCbCr420, up to 16 bpc
  - 4Kp30Hz, RGB/YCbCr444, up to 16 bpc
- Audio processing
  - Audio stream forwarding from DP RX to HDMI TX
  - Conversion to I2S or TDM audio output (8 CH)
  - Conversion to SPDIF audio output (2CH)
- HDCP support
  - HDCP1.3 to HDCP1.4 Repeater function
  - HDCP2.3 to HDCP1.4 Repeater function
  - HDCP2.3 to HDCP2.3 Repeater function
  - Read- protected embedded HDCP keys
- Enhanced security
  - Encrypted on-chip key storage
  - RSA-2048bit signed application firmware
  - Secure Boot & In-system Programming
  - Test, debug ports deactivation
- Metadata handling
  - HDMI TX DVI/HDMI mode setting (DPCD register)
  - YCbCr444-420 conversion (DPCD register)
  - IEC60958 BYTE3 channel status overwrite
  - CTA861G INFO FRAME generation
  - CTA861.3 HDR and Mastering InfoFrame
  - Chainable VSC_EXT SDP packing format
- ARM processor and peripheral controllers
  - ARM Cortex M3 core
  - SPI controller
  - I2C master, slave controller
  - On-Chip, RAM, ROM, OTP
- Device configuration options
  - Application FW stored in SPI flash
  - AUX CH, I2C host interface
- Internal video pattern generator
  - Configurable through vendor specific DPCD registers
- EMI reduction support
  - Spread spectrum for DP input, output
  - Scrambler for DP and HDMI outputs
- Low power operation
  - 860mW nominal operation with retimer
  - 700mW nominal operation without retimer
  - Under 10mW Standby operation
- ESD specification
  - ESD: ±2kV HBM, 500 V CDM
- Package
  - 289 LFBGA (12 x 12mm)
  - Halogen free Halogen free RoHS and Green Compliant
- Power supply voltages
  - 1.8V Analog and I/O, 0.95V Analog and core

Description

The KTM50x0 is an advanced DisplayPort1.4a MST hub with an integrated USB type-C de-multiplexer, targeted primarily for Mobile Notebook accessory and display applications. This device functions as a multi-stream audio-video splitter and protocol converter with an HDCP1.x/ HDCP2.3 repeater supporting both compressed (DSC) and uncompressed AV streams.

KTM50x0 has a DP alt-mode capable USB Type-C Upstream Facing Port (UFP). The four high speed lanes of UFP can receive DP1.4a MST audio-video and USB3.2 Gen2 data streams simultaneously. The input lane mapping is flexible and meets standard DP or the USB Type-C connector with flip orientation requirements. The incoming DP and USB signals are de-multiplexed, retimed, and transmitted on the Downstream Facing Ports (DFP). The KTM50x0 consists of three AC coupled DP/DP++ or DC coupled HDMI/DVI DFPs, each with four high-speed lanes and one USB port with USB3.2 TX and RX pair. The Stream Routing Logic in KTM50x0 allows flexible routing of incoming DP MST stream converted into any combination of MST or SST streams on any of the DFP video ports with link rate and lane count change option. Also, the SST stream can be replicated on two or more DFP ports. In addition, the DP SST stream can be converted into a HDMI or DVI output (TMDS signal format).

The combo receiver in KTM50x0 supports all DP standard data rates up to HBR3 (8.1 Gbps/lane) and USB3.2 Gen1 (5.0 Gbps) and Gen2 (10.0 Gbps). The dual mode (DP++) transmitters support DP standard data rates up to 8.1 Gbps/lane and TMDS data rates up to 6.0 Gbps/lane. The side-band channel uses 1.0 Mbps Manchester-coded AUX signaling for DP and DDC signaling up to 100kbps for the HDMI interface.

KTM50x0 is capable of processing up to six DP audio-video streams compressed or uncompressed. FEC decoding and encoding is employed for the reliable reception and transmission of DSC1.2a compressed streams. These streams can be part of one single large video timing or six independent video timings from a single source with corresponding independent multi-channel audio. The highest video timing per stream and the number of streams transported is limited by the DP1.4a and HDMI2.0 link bandwidth. When the received DP MST stream is in DSC1.2a compressed format, KTM50x0 can decode the streams (max two streams) or pass through to the downstream sink or to another cascaded KTM50x0 device. If a DP source sends an 8k4k60Hz RGB/YCC444 DSC1.2a encoded video as four 4k2k60Hz MST, then two KTM50x0 devices are needed to decode all four streams. KTM50x0 supports both RGB 444 and YCC444/422/420 video pixel encoding formats with a color depth up to 16 bpc (bits per component or 48 bits per pixel). It has a pixel processing unit capable of video pixel encoding format conversion from RGB444 to YCC444 with bit depth expansion and down scaling from YCC444 to YCC422/420. Pixel format conversion along with horizontal blanking expansion improves interoperability and smooth rendering of CVT video timings from a mobile PC on a consumer displays such as TVs and projectors which supports only CEA timings.

KTM50x0 processes High Dynamic Range (HDR) video content specified in BT601, BT709, BT2020, BT2100 , Adobe RGB colorimetry format with the proper metadata conversion from DP to HDMI. It also offers secure reception and transmission of high bandwidth digital audio and video content with HDCP1.x or HDCP2.3 content protection. As a branch device KTM50x0 functions as a HDCP1.x and HDCP2.3 repeater between the DP source and DP or HDMI sink.

KTM50x0 uses an external 25 MHz reference clock for its operation. The reference clock can be generated from a 25MHz crystal or from an external source. It has a 300MHz ARM Cortex M3 CPU with on-chip memories for code and data storage. The peripheral subsystem includes SPI, UART (debug only), and I2C master, slave interfaces. An internal Power-On Reset (POR) circuit senses the voltage on the reset input and provides the chip reset during system power-up. The KTM50x0 uses an external 16 Mbit SPI flash memory for storing the RSA-2048 signed application firmware with fail-safe recovery. At boot up, the CPU goes through a secure boot process authenticating the application code image stored in the SPI flash. It supports both standard mode and quad mode SPI operation. Firmware update for the SPI flash is done securely through the DP AUX_CH or I2C host interface (Secure In-System-Programming).

Table 1. Part Numbers

Features	KTM5000	KTM5010	KTM5020	KTM5030
Input	DP (4 Lanes)	DP (4 Lanes)	USB-C (DP alt-mode) (DP 4 lanes OR 2 lanes DP and 2 lanes USB3.2)	USB-C (DP alt-mode) (DP 4 lanes OR 2 lanes DP and 2 lanes USB3.2)
Outputs	3x DP++ (DP or HDMI)	3x DP++ (DP or HDMI)	3x DP++ (DP or HDMI) 1x USB3.2	3x DP++ (DP or HDMI) 1x USB3.2
USB De-mux & Re-timer	No	No	Yes	Yes
HDCP2.2	Yes	Yes	Yes	Yes
HDR, Pixel Processor	Yes	Yes	No	Yes
DSC & FEC	No	Yes	No	Yes
Package	LFBGA 12x12mm / 0.65mm pitch	LFBGA 12x12mm / 0.65mm pitch	LFBGA 12x12mm / 0.65mm pitch	LFBGA 12x12mm / 0.65mm pitch

Applications

The target applications of the KTM50x0 are:

- Mobile PC docking stations
- Dongles
- MST video hubs
- AR / VR devices
- High end displays such as digital signage
- Daisy-chain monitors

DisplayPort and USB Type-C are the prominent interfaces in these applications and the KTM50x0 offers the highest performance at the optimum bill of material cost.

Docking Station Application

In a mobile docking station topology, the KTM50x0 is part of a larger system which has a system controller such as TCPC, USB hub, etc. The docking station can be a traditional dock with a custom connector or a travel dock with a USB Type-C tethered cable. The audio-video interface between the notebook and the docking station is either DP or DP Alt-Mode over USB Type-C. The KTM50x0 is an ideal device for a Type-C docking station where it can function as a Type-C Port Manager (TCPM) along with an external TCPC device (e.g. Kinetic MCDP9000 TCPC). It is designed with integrated features such as a USB-C de-mux, a video hub, a protocol converter, and an HDCP repeater in a single chip. The downstream video ports can be configured as DP1.4a or HDMI2.0 depending on the requirements.

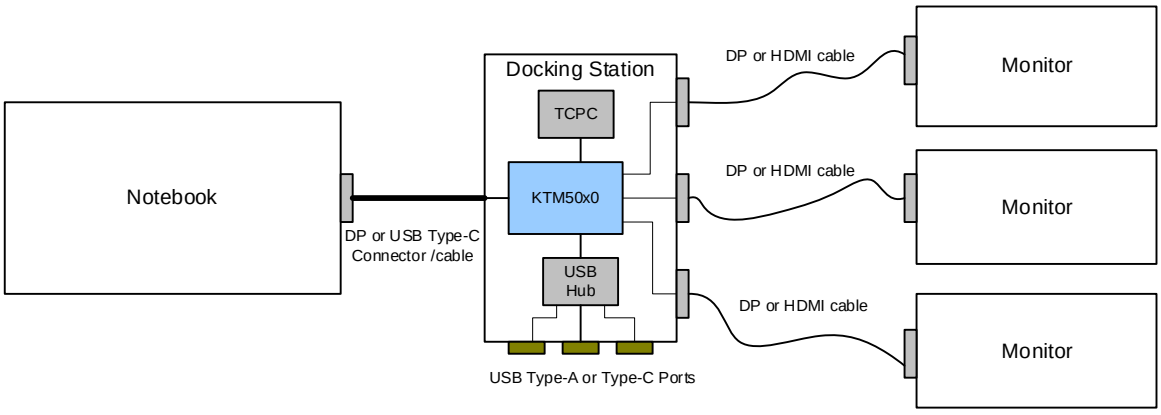

Figure 1. KTM50x0 Docking Station Use Case

Daisy-Chain Monitor / Signage Application

A daisy-chain monitor or signage featuring the USB Type-C connector supporting the DP Alt-mode requires a USB Type-C de-mux and a DP MST hub device with two or more video outputs. KTM50x0 is an ideal fit for such applications where it can receive the USB and multiple video streams simultaneously. It then routes one of the video stream to the internal SoC and the remaining streams to the downstream units. In this use case, the KTM50x0 can support two 4K60Hz displays without DSC or up to four 4K60Hz displays with DSC.

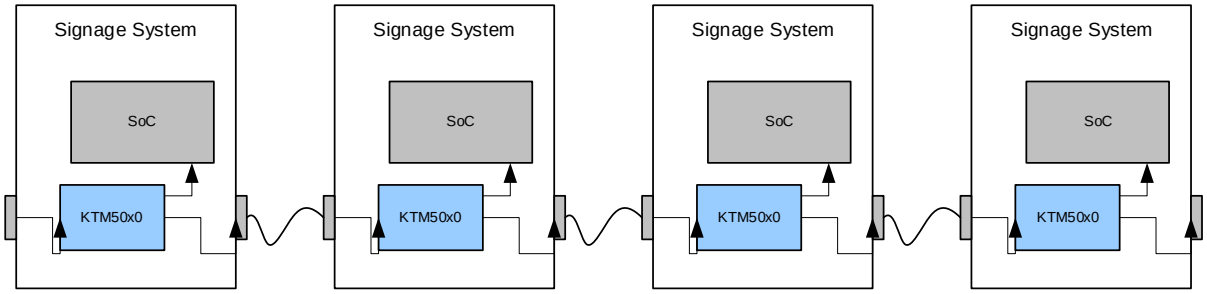

Figure 2. KTM50x0 Digital Signage Use Case

AR/VR Application

The current AR/VR head mount displays use a video splitter device for routing the video from the graphics source to the dual OLED panels. Future designs are targeting higher video resolutions, refresh rates, and low latency. The KTM50x0 is suitable for such designs; it can deliver up to 2x 2560x2160 @120 Hz without DSC or up to 2x 3860x2160@ 90 Hz with DSC. Additionally, the KTM50x0 can generate a global frame synchronization signal for synchronizing the video with the sensor inputs. Also it can deliver up to 8CH compressed or LPCM audio through the I2S or TDM format to audio codec for the best quality audio experience.

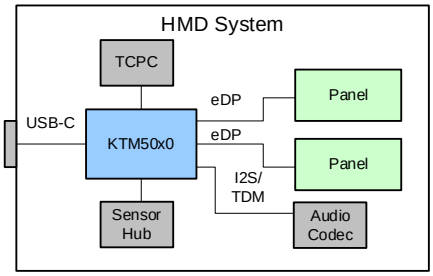

Figure 3. KTM50x0 AR/VR Head Mount Display Use Case