5A Slew Rate Controlled Load Switch with Reverse Blocking

Features

- Operating Range: 1.5V~5.5V
- Low $R_{DS(ON)}$ MOSFET: Typ. 13.4mΩ @ 3.3V
- Continuous DC current up to 5A
- Built-in slew rate controlled turn-on: 2.7ms
- Low quiescent current < 1µA
- ESD Protection
  - Human Body Model : 8kV
  - Charged Device Model : 2.0kV
  - Compliance to IEC61000-4-2 Level 4
    - Contact Discharge : 8kV
    - Air Discharge : 15kV
- Output Auto Discharge when Disabled option (-1)
- Pb-Free Packages:
  - WLCSP-6, 1.0 x 1.5mm
  - RoHS and Green Compliant
- -40°C to +85°C Temperature Range

Applications

- Mobile Phones & Tablets
- SSD (Solid State Drive)
- Portable Instruments
- DSC, DVR, GPS

Brief Description

The KTS1605 is slew rate controlled load switch designed for 1.5V to 5.5V operation. It features a controlled soft-on slew rate of typical 2.7ms that limits the inrush current for designs with heavy capacitive loads and thereby minimizing any resulting voltage droop at the power rails.

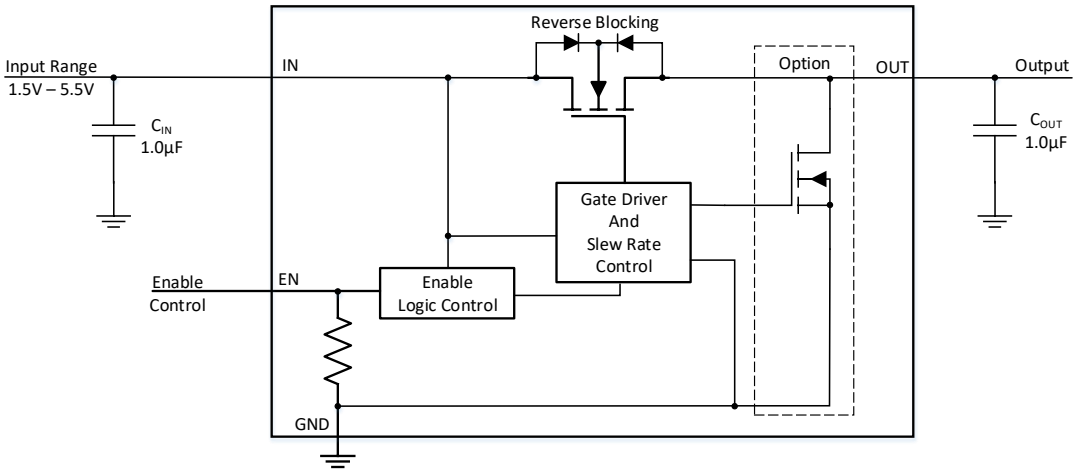
The very low $R_{DS(ON)}$ allows currents up to 5A, whilst minimizing the power dissipation and voltage drop from supply to load. The KTS1605 features an active high enable pin, which is capable of interfacing directly with low input control signals, without any additional level shifting circuitry. The KTS1605 also includes an active pull-down to ensure the device remains off, should the enable be allowed to float.

The KTS1605 provides reverse blocking in the OFF state to ensure that power supplies are not discharged.

In addition, the KTS1605 has an option for output auto discharge feature. This enables the device to quickly discharge the output when the device is disabled.

The KTS1605 is available in an optimized, lead-free, fully green compliant, small 6-pin WLCSP 1.0 x 1.5mm package with 0.5mm pitch

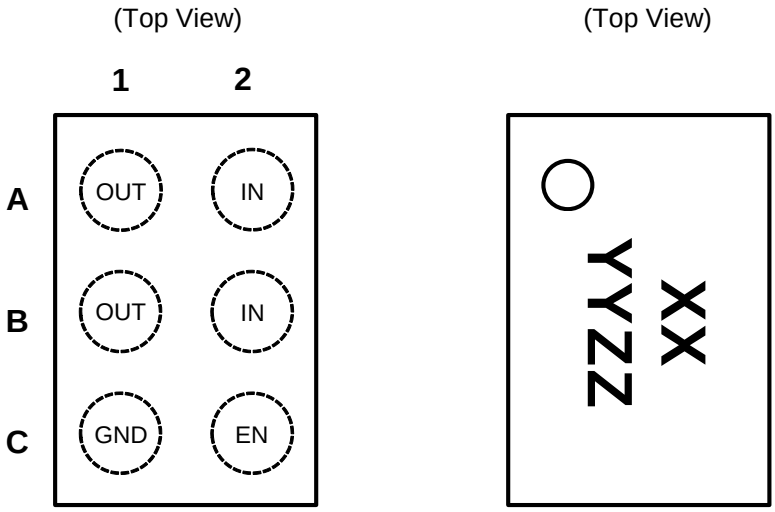
Typical Application



Pin Descriptions

Pin #	Name	Function
A1, B1	OUT	Power−switch output. Connect a 1.0uF ceramic capacitor from OUT to GND as close as possible to the IC is recommended. (-1) Option includes an output discharge transistor.
A2, B2	IN	Power−switch input voltage. Connect a 1.0µF or greater ceramic capacitor from IN to GND as close as possible to the IC.
C1	GND	Ground connection
C2	EN	Enable input, logic high turns on power switch.

WLCSP-6, 1.0 x 1.5 x 0.620 mm



6-Bump 1.0mm x 1.5mm x 0.620mm micro SMD Package
Top Mark
XX = Device Code
YY = Date Code, ZZ = Assembly Code

Absolute Maximum Ratings[1]

(T_A = 25°C unless otherwise noted)

Symbol	Description	Value	Units
IN, OUT, EN	Input voltage, Enable Input Voltage, Output Voltage to GND	-0.3 to +6.0	V
ISW	Maximum Continuous Switch Current (I_{MAX})	5.0	A
ESD IEC	ESD Withstand Voltage (IEC 61000−4−2)[2] (IN and OUT when bypassed with 1.0µF capacitor minimum)	Air: 15 Contact: 8	kV
ESD HBM	Human Body Model (HBM) ESD Rating[3,4]	8	kV
ESD CDM	Charge Device Model (CDM) Rating[3,4]	2.0	
ESD MM	Machine Model (MM) ESD Rating	400	V
T_J	Operating Junction Temperature Range	-40 to 125	°C
T_S	Storage Temperature Range	-65 to 150	
T^{LEAD}	Maximum Soldering Temperature (at leads, 10sec)	300	
MSL	Moisture Sensitivity[5]	Level 1	

Thermal Capabilities[6]

Symbol	Description	Value	Units
θ_{JA}	Thermal Resistance – Junction to Ambient	85	°C/W
P_D	Maximum Power Dissipation at $T_A \leq 25°C$	1.17	W
$\Delta P_D/°C$	Derating Factor Above T_A = 25°C	1.17	mW/°C

Ordering Information

Part Number	Marking[7]	Operating Temperature	Auto-Discharge	Package
KTS1605EUB-TR	JCYYZZ	-40°C to +85°C	NO	WLCSP-6 1.0 x 1.5 x 0.620mm
KTS1605EUB-1-TR	JLYYZZ		YES	

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
2. Guaranteed by design and not 100% tested
3. According to JEDEC standard JESD22−A108
4. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114 for all pins.
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115 for all pins.
5. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020.
6. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to a PCB board.
7. “JC/JL” is the device Code, “YYZZ” the date and assembly code.

Electical Characteristics[8]

The *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C, V_{IN} = 1.5V to 5.5V unless otherwise noted, while *Typ* values are specified at V_{IN} = 4.5V and room temperature (T_A = 25°C) unless otherwise noted.

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage Range		1.5		5.5	V
I_Q	Quiescent Current	V_{IN} = 1.5V to 5.5V, EN = Active, I_{OUT} = 0mA		8	14	µA
I_{Q_OFF}	No Load Quiescent Current	V_{IN} = 1.5V to 5.5V, EN = Inactive, OUT = OPEN			1.0	µA
I_{SD}	Shutdown Current	V_{IN} = 1.5V to 5.5V, EN = GND, OUT = GND, T_A = -40°C to +85°C		2.0	4.0	µA
I_{EN_LEAK}	EN Input Leakage Current	V_{EN} = 5.5V, V_{IN} = 0V	-10		10	µA
		V_{EN} = 0V, V_{IN} = 5.5V	-1.0		1.0	
$R_{DS(ON)}$	On-Resistance	V_{IN} = 5.5V, I_{OUT} = 1A, T_A = 25°C		10.2	15.0	mΩ
		V_{IN} = 5.0V, I_{OUT} = 1A[9]		10.5		
		V_{IN} = 4.5V, I_{OUT} = 1A, T_A = 25°C		11.1	16.0	
		V_{IN} = 3.3V, I_{OUT} = 500mA, T_A = 25°C		13.4	18.0	
		V_{IN} = 2.5V, I_{OUT} = 500mA[9]		16.6		
		V_{IN} = 1.8V, I_{OUT} = 500mA[9]		23.0		
		V_{IN} = 1.5V, I_{OUT} = 500mA, T_A = 25°C		29.4	40.0	
V_{IH}	EN Input Logic High Level	V_{IN} = 1.5V to 5.5V	1.15			V
V_{IL}	EN Input Logic Low Level	V_{IN} = 1.8V to 5.5V			0.65	
		V_{IN} = 1.5V to 1.8V			0.60	
R_{OUT_PD}	OUT Pull-Down (Option -1)	V_{EN} = 0V[9], I_{PD} = 2mA		30		Ω
R_{EN_DOWN}	EN Pull-down Resistor	V_{IN} = V_{EN} = 1.5V to 5.5V	6.38	7.65	8.86	MΩ
I_{OUT_OUT}	VOUT Shutdown Current	V_{EN} = 0V, V_{OUT} = 4.2V, V_{IN} = Short to GND			1.0	µA
t_{DELAY_ON}	Turn-On Delay Time[10]	V_{IN} = 4.5V, R_{LOAD} = 5Ω, C_{LOAD} = 100µF, T_A = 25°C		1.7		ms
t_R	V_{OUT} Rise Time[10]			2.7		
t_{ON}	Turn-On Time[11]			4.4		
t_{DELAY_ON}	Turn-On Delay Time[10]	V_{IN} = 4.5V, R_{LOAD} = 150Ω, C_{LOAD} = 100µF, T_A = 25°C		1.7		ms
t_R	V_{OUT} Rise Time[10]			1.5		
t_{ON}	Turn-On Time[11]			3.2		
t_{DELAY_OFF}	Turn-Off Delay Time[10]	V = 4.5V, R_{LOAD} = 150Ω, C_{LOAD} = 100µF, T_A = 25°C		1.8		ms
t_F	V_{OUT} Fall Time[10]			34		
t_{OFF}	Turn-Off Time[12]			35		
t_{DELAY_OFF}	Turn-Off Delay Time[10]	V = 4.5V, R_{LOAD} = 150Ω, C_{LOAD} = 100µF, T_A = 25°C KTS1605-1 Only		0.8		ms
t_F	V_{OUT} Fall Time[10]			9.0		
t_{OFF}	Turn-Off Time[12]			9.8		

8. All specifications are 100% production tested at T_A = +25°C, unless otherwise noted. Specifications are over -40°C to +85°C and are guaranteed by design

9. Guaranteed by design and not 100% tested

10. t_{DELAY_ON}/t_{DELAY_OFF}/t_R/t_F are defined in Figure 1

11. t_{ON} = t_R + t_{DELAY_ON}

12. t_{OFF} = t_F + t_{DELAY_OFF}

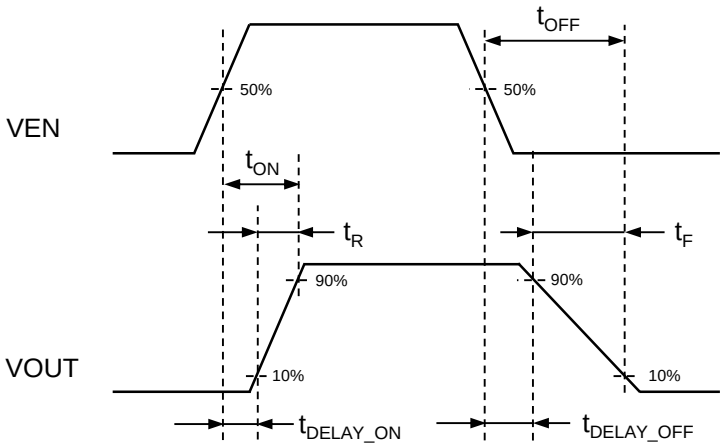
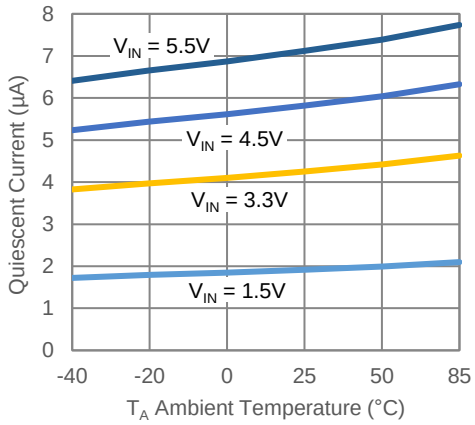


Figure 1. Timing Diagram

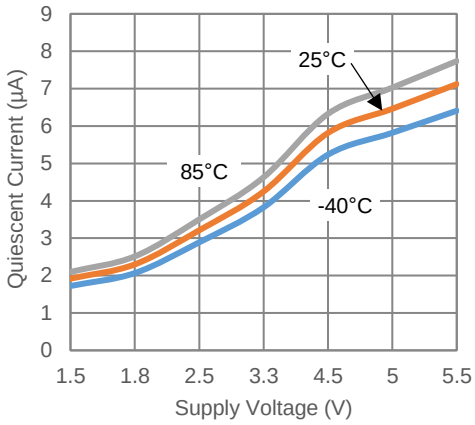
Typical Characteristics

V_{IN} = 5V, C_{IN} = 0.1µF, C_{OUT} = 1µF, Temp = 25°C unless otherwise specified.

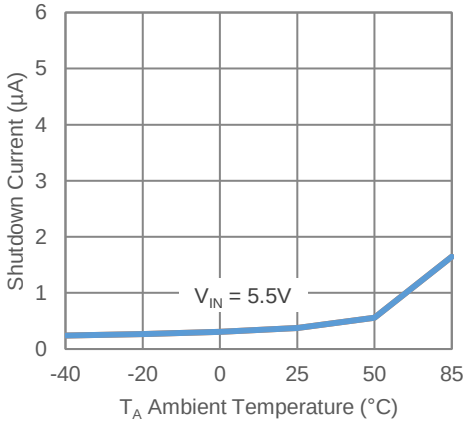
Quiescent Current vs. Temperature



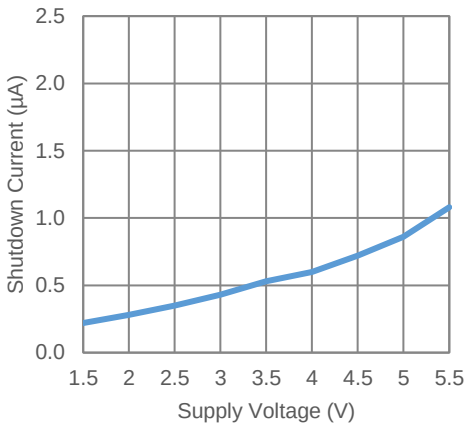
Quiescent Current vs. Supply Voltage



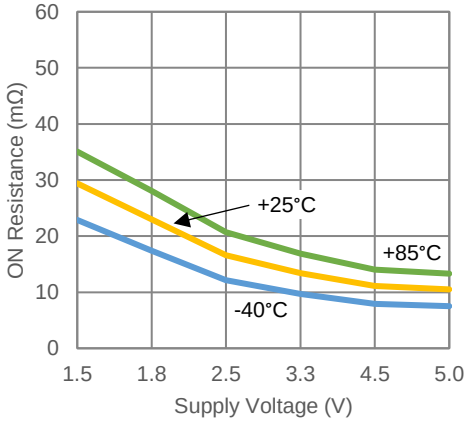
Shutdown Current vs. Temperature



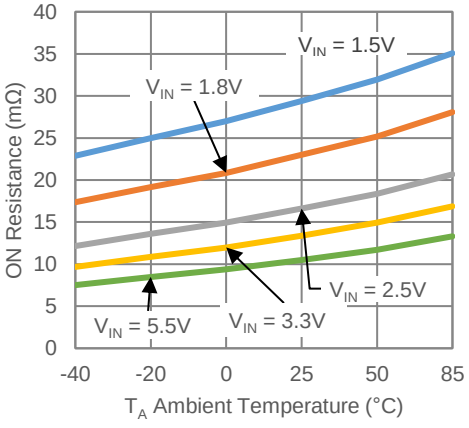
Shutdown Current vs. Supply Voltage



ON Resistance vs. Supply Voltage (I_{OUT} = 500mA)



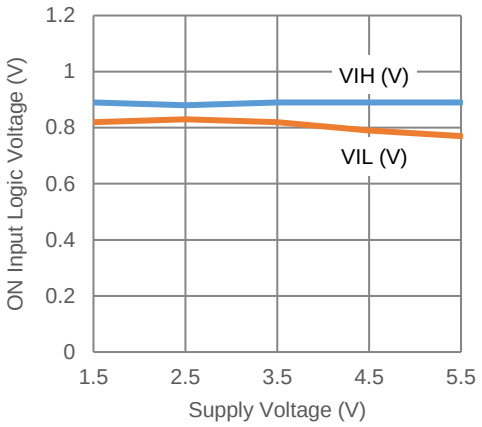
ON Resistance vs. Temperature (I_{OUT} = 500mA)



Typical Characteristics (continued)

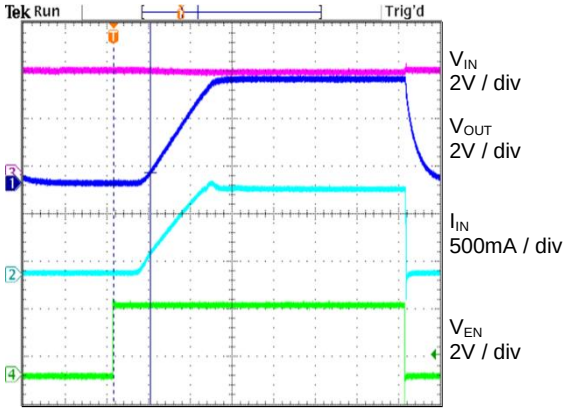
V_{IN} = 5V, C_{IN} = 0.1µF, C_{OUT} = 1µF, Temp = 25°C unless otherwise specified.

EN Pin Threshold vs. Supply Voltage



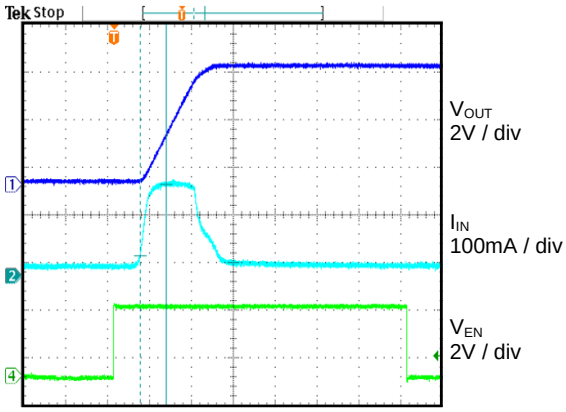
Turn-On & Turn-Off Response

(V_{IN} = 4.5V, C_{IN} = 10µF, C_{OUT} = 100µF, R_L = 5Ω)

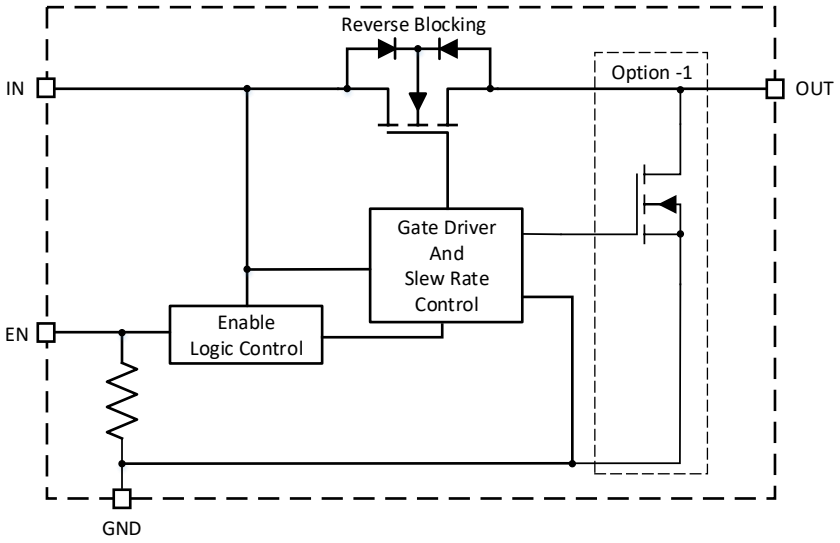


In-rush Current Waveform

(V_{IN} = 5.0V, C_{IN} = 10µF, C_{OUT} = 100µF, R_L = OPEN)



Functional Block Diagram



Functional Description

The KTS1605 is an advanced slew-rate controlled high-side load switch comprised of a low resistance MOSFET power switch, level shift with slew-rate control logic and reverse blocking protection. The KTS1605 is a low resistance MOSFET power distribution switch designed to connect an external voltage, such as a DC power supply or battery, directly to the system. The high-side MOSFET is turned-on sequence is initiated via an active high, low voltage logic voltage signal. Once above the input threshold voltage, the MOSFET turn-on is slew-rate limited to avoid excessive current surges, due to high capacitance loads. By limiting the turn-on, large voltage over-shoot can also be avoided. Once fully on the MOSFET will provide a low resistance path to the load, both minimizing the voltage drop from IN to OUT, while keeping the power dissipation to a minimum.

Should the voltage on the output of The KTS1605 switch, in the OFF state, be higher than the input voltage, Reverse Blocking circuitry will be activated to stem the flow of current preventing power supplies for discharging.

In addition, the KTS1605 has an option for output auto discharge feature. This enables the device to quickly discharge the output when the device is disabled.

The KTS1605 integrates a pull-down resistor on the enable pin to ensure that the device should remain OFF when the EN is left floating.

Application Information

Enable Input

The EN pin is compatible with active HIGH GPIO and CMOS logic voltage levels and operates over the 1.5V to 5.5V operating voltage range. The KTS1605 incorporates an internal pull-down resistor on the enable pin, to ensure that the device remains OFF, in the event that the pin is left floating.

Reverse Current Blocking

The KTS1605 implements reverse current blocking circuitry, to prevent reverse current flow through the switch. The reverse current blocking circuitry is active when the device is in the OFF state.

Auto Discharge Option

The KTS1605 has an option for auto discharging the output when the part is disabled. This enables the device to quickly discharge the output when the device is disabled, and to remove any residual capacitor voltage.

Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush currents, an input bypass capacitor is recommended. A minimum capacitance of 1.0µF, must be placed as close as possible between pins VIN and GND) to be Compliant with IEC 61000−4−2 (Level 4).

Higher value capacitors can further help to reduce the voltage drop. Ceramic capacitors are recommended for their ability to withstand input current surges from low impedance sources such as batteries in portable devices.

Output Capacitor

Depending on the sink current during system start-up and system turn-off, a capacitor must be placed on the output. A 1.0µF or larger capacitor across OUT and GND pins is recommended to accommodate load transient condition. This capacitor can also help to prevent parasitic inductance which can force the output voltage to fall below GND during turn-off. The output capacitor has minimal effect on The KTS1605's turn-on slew-rate time.

Inrush Current

Inrush current occurs when the device is turned on. Inrush current is dependent on output capacitance and slew-rate control capability, as expressed by:

$$I_{INRUSH} = C_{OUT} \times \frac{V_{IN} - V_{INITIAL}}{t_R} + I_{LOAD}$$

Where:

C_{OUT} - Output capacitance
t_R - Slew-rate or rise time at V_{OUT}
V_{IN} - Input voltage
$V_{INITIAL}$ - Initial voltage at C_{OUT}, usually GND
I_{LOAD} - Load current

The KTS1605 has a 2.7ms of slew-rate capability under $4.5V_{IN}$ at 1000uF of C_{OUT} and 5Ω of R_{LOAD} so inrush current can be minimized and no input voltage drop appears.

Layout Guidelines

The KTS1605 integrates a 5A rated MOSFET, and the PCB design rules must be respected to properly transfer the heat out of the silicon. By increasing PCB area, the $R\theta_{JA}$ of the package can be decreased, allowing higher power dissipation.

For the best performance, all traces should be as short as possible to minimize the inductance and parasitic effects. The input and output capacitors should be kept as close as possible to the input and output pins respectively. Using wide traces for input, output, and GND help reducing the case to ambient thermal impedance.

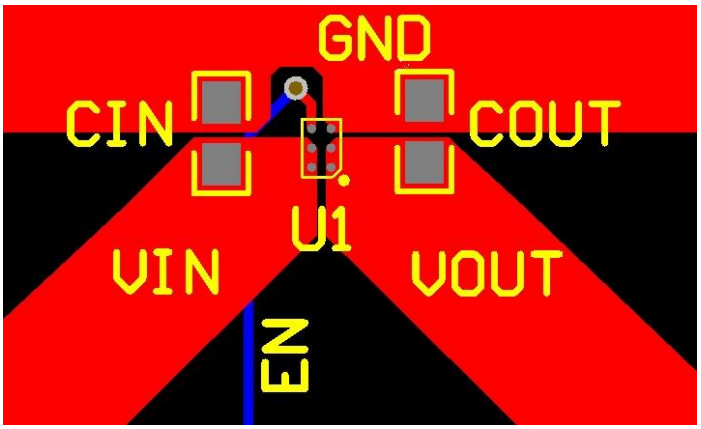


Figure 2. Recommended Layout for WLCSP-6 Package