

5A_{RMS} VBUS Current-Sink Protection Load Switch

Features

- 3V to 23V Operating Voltage Range
- 29V Abs. Max. Rating at IN and OUT
- 5A Continuous Current Rating
 - ▶ 10A Pulse Current Rating (duration Pd limited)
- 25mΩ typ. On-Resistance from IN to OUT
- Soft-Start (SS) Limits Inrush Current
- Over-Voltage Protection (OVP) at IN
 - ▶ 23V Internally Fixed
 - ▶ 4V to 23V External Resistor Programmable
- “Ideal Diode” Reverse Current Protection (RCP)
 - ▶ 20mV Forward Voltage and 15μs Fast Recovery
- Over-Current Protection (OCP) at OUT
- Short-Circuit Protection (SCP) at OUT
- Over-Temperature Protection (OTP)
- Transient Voltage Suppression (TVS) at IN
 - ▶ ±90V Surge Protection (IEC61000-4-5)
 - ▶ ±8kV ESD Contact Discharge (IEC61000-4-2)
 - ▶ ±15kV ESD Air Gap Discharge (IEC61000-4-2)
- EN or \overline{EN} Enable Logic Input Versions
- \overline{ACOK} Open-Drain Power Good Flag
- -40°C to 85°C Operating Temperature Range
- 15-bump WLCSP 2.62 x 1.64mm (0.5mm pitch)

Brief Description

KTS1698 is a low-resistance, high-current load switch with soft-start, over-voltage protection, reverse-current blocking, over-current protection, short-circuit protection, over-temperature protection, and integrated TVS. It is optimized to protect systems with USB Type-C PD ports and barrel connectors that sink up to 100W at 20V and must withstand up to 29V on VBUS.

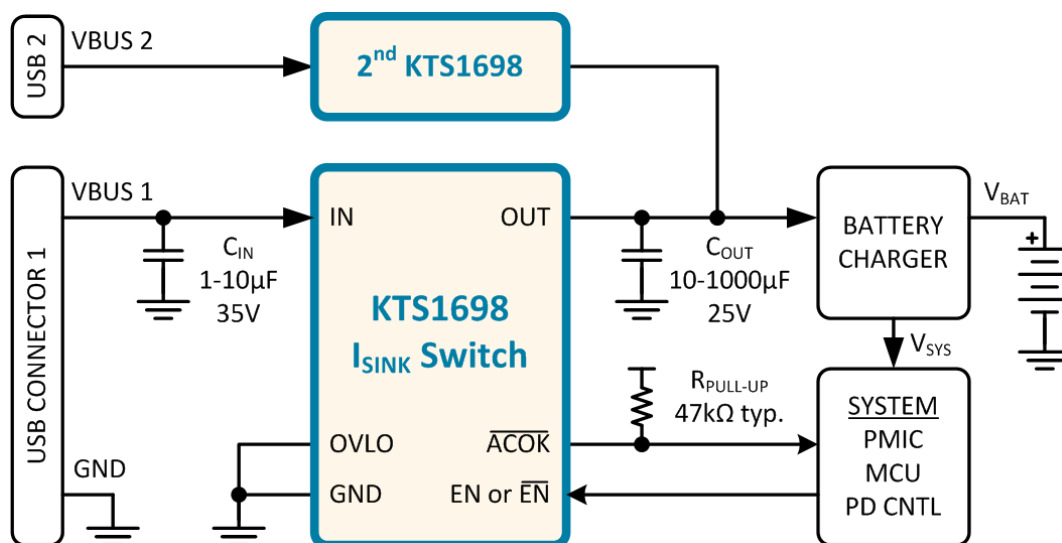
Automatic reverse-current blocking acts as an “ideal diode” and isolates VBUS when charging or powering the system via another port. Soft-start limits inrush current when turning on with large capacitors at the output. The integrated TVS provides IEC industry standard ESD and ±90V surge ratings. An \overline{ACOK} flag indicates when power is good.

KTS1698 is packaged in advanced, fully “green” compliant, 2.62 x 1.64mm, 15-bump Wafer-Level Chip-Scale Package (WLCSP).

Applications

- Desktop, Notebooks, Netbooks, Ultra-Books, Tablets
- Docking Stations, Monitors, Accessories

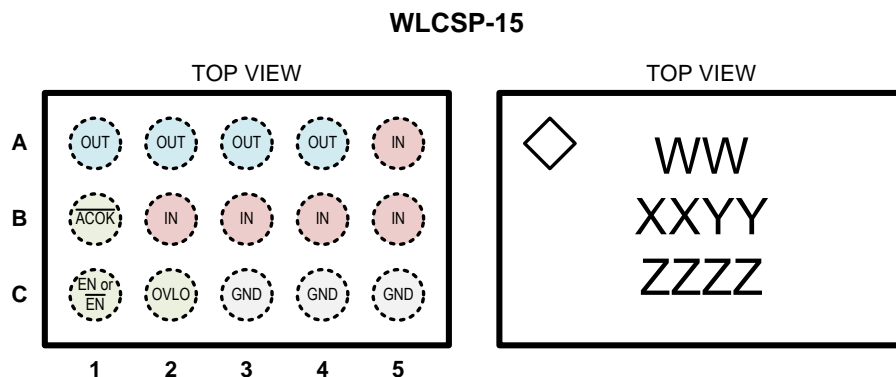
Typical Application



Ordering Information

| Part Number | Marking ¹ | Enable Polarity | Operating Temperature | Package |
|-----------------|----------------------|------------------------|-----------------------|----------|
| KTS1698AEDAB-TA | REXXYYZZZZ | $\overline{\text{EN}}$ | -40°C to +85°C | WLCSP-15 |
| KTS1698BEDAB-TA | __XXYYZZZZ | EN | -40°C to +85°C | WLCSP-15 |

Pinout Diagram



15-bump 2.62mm x 1.64mm x 0.62mm

WLCSP Package, 0.5mm pitch

Top Mark: WW = Device ID, XX = Date Code, YY = Assembly Code, ZZZZ = Serial Number

Pin Descriptions

| Pin # | Name | Function |
|--------------------|--------------------------|---|
| A1, A2, A3, A4 | OUT | Power Switch Output – connect to battery charger IC input (or Vsys in systems without rechargeable batteries). |
| A5, B2, B3, B4, B5 | IN | Power Switch Input – connect to power input port (VBUS on USB port). |
| B1 | $\overline{\text{ACOK}}$ | Power Good Flag – active-low, open-drain logic output. Connect to GND or leave floating if unused. |
| C1 | $\overline{\text{EN}}$ | Enable – active-low logic input (KTS1698A) |
| | EN | Enable – active-high logic input (KTS1698B) |
| C2 | OVLO | External OVLO Adjustment – connect to GND to use the internally fixed OVLO threshold. Connect an external resistive voltage divider from IN to OVLO to GND to set an adjustable the OVLO threshold. |
| C3, C4, C5 | GND | Ground |

1. "RE" is the device ID, "XX" is the date code, "YY" is the assembly code, and "ZZZZ" is the serial number.

Absolute Maximum Ratings²

| Symbol | Description | Value | Units |
|------------------------------------|--|-------------------------|-------|
| V _{IN} | IN to GND (continuous) | -0.3 to 29 | V |
| | IN to GND (during IEC61000-4-5 surge event) | -2 to 36 | |
| V _{OUT} | OUT to GND | -0.3 to 29 | V |
| V _{IN-OUT} | IN to OUT | -29 to 29 | V |
| V _{EN} , V _{EN1} | EN, EN to GND | -0.3 to 29 | V |
| V _{OVLO} | OVLO to GND | -0.3 to V _{IN} | V |
| V _{ACOK1} | ACOK to GND | -0.3 to 6 | V |
| I _{SW} | Maximum Switch Current (continuous) | 5 | A |
| | Peak Switch Current (duration is Pd limited) | 10 | |
| T _J | Operating Temperature Range | -40 to 150 | °C |
| s | Storage Temperature Range | -55 to 150 | °C |
| T _{LEAD} | Maximum Soldering Temperature (at leads, 10 sec) | 260 | °C |

ESD and Surge Ratings³

| Symbol | Description | Value | Units |
|----------------------|--|-------|-------|
| V _{ESD_HBM} | JEDEC JS-001-2017 Human Body Model (all pins) | ±2 | kV |
| V _{ESD_CD} | IEC61000-4-2 Contact Discharge (IN) | ±8 | kV |
| V _{ESD_AGD} | IEC61000-4-2 Air Gap Discharge (IN) | ±15 | kV |
| V _{SURGE} | IEC61000-4-5 Surge (IN, C _{IN} = 10µF, V _{IN} = -0.3 to 23V _{DC} ± V _{SURGE}) | ±90 | V |

Thermal Capabilities⁴

| Symbol | Description | Value | Units |
|---------------------|--|-------|-------|
| Θ _{JA} | Thermal Resistance – Junction to Ambient | 62.7 | °C/W |
| P _D | Maximum Power Dissipation at 25°C | 1.99 | W |
| ΔP _D /ΔT | Derating Factor Above T _A = 25°C (T _J = 150°C) | 15.9 | mW/°C |

- Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
- ESD and Surge Ratings conform to JEDEC and IEC industry standards. Some pins may have higher performance. Surge ratings apply with chip enabled, disabled, or unpowered, unless otherwise noted.
- Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.

Recommended Operating Conditions⁵

| Symbol | Description | Value | Units |
|-----------------------------------|--------------------------------|------------|-------|
| V _{IN} | Supply Voltage Operating Range | 3 to 23 | V |
| V _{OUT} | Output Voltage Range | 0 to 23 | V |
| V _{ACOK} | Power Good Flag Output Voltage | 0 to 5.5 | V |
| V _{OVLO} | OVLO Adjust Input Bias Voltage | | |
| V _{EN} , V _{EN} | Enable Logic Input Voltage | 0 to 23 | V |
| C _{IN} | Input Capacitance | 1 to 10 | μF |
| | | 35 | V |
| C _{OUT} | Output Capacitance | 10 to 1000 | μF |
| | | 25 | V |

Electrical Characteristics⁶

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C and V_{IN} = 3V to 20V. Typical values are specified at T_A = +25°C with V_{IN} = 5V.

Supply Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|----------------------|--------------------------------|--|-----|-----|------|-------|
| V _{IN} | Input Voltage Operating Range | | 3 | | 23 | V |
| V _{UVLO} | Under-Voltage Lockout | V _{IN} rising threshold | | 2.7 | 2.95 | V |
| | | Hysteresis | | 200 | | mV |
| I _Q | No-Load Supply Current | Enabled, V _{IN} = 5V, OUT = open | | 170 | | μA |
| | | Enabled, V _{IN} = 20V, OUT = open | | 215 | | μA |
| I _{SHDN} | Shutdown Supply Current | V _{IN} = 5V, OUT = open | | 1 | | μA |
| | | V _{IN} = 20V, OUT = open | | 2.6 | | μA |
| V _{OUT} | Output Voltage Operating Range | | 3 | | 23 | V |
| I _{OUT_RCP} | Output Supply Current in RCP | Enabled, V _{IN} = 0V, V _{OUT} = 5V | | 250 | | μA |

Logic Pin Specifications (EN, EN, ACOK)

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|-------------------|------------------------------------|---------------------------|-----|------|-----|-------|
| V _{IH} | Input Logic High (EN, EN) | | 1.2 | | | V |
| V _{IL} | Input Logic Low (EN, EN) | | | | 0.4 | V |
| R _{I_PD} | Input Logic Pull-Down (EN) | | | 2 | | MΩ |
| I _{I_LK} | Input Logic Leakage (EN) | V _I = 5V | -1 | | 1 | μA |
| | | V _I = 20V | -1 | | 1 | μA |
| V _{OL} | Output Logic Low (ACOK) | I _{O_SINK} = 1mA | | 0.01 | 0.2 | V |
| I _{O_LK} | Output Logic High-Z Leakage (ACOK) | V _O = 5V | -1 | | 1 | μA |

(continued next page)

5. The recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Kinetic does not recommend exceeding them or designing to Absolute Maximum Rating.

6. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

Electrical Characteristics (continued)⁷

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C and $V_{IN} = 3V$ to $20V$. Typical values are specified at $T_A = +25^\circ C$ with $V_{IN} = 5V$.

Switch Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|----------------------|---------------------------|--|-----|------|-----|-------|
| R _{ON} | Switch On-Resistance | V _{IN} = 5V, 240mA (max) test mode | | 25 | | mΩ |
| | | V _{IN} = 20V, 240mA (max) test mode | | 25 | | |
| I _{IN_OFF} | Switch Off-Leakage at IN | Shutdown, V _{IN} = 5V, V _{OUT} = 0V | | 1 | | μA |
| | | Shutdown, V _{IN} = 20V, V _{OUT} = 0V | | 2.6 | | |
| | | Shutdown, V _{IN} = 0V, V _{OUT} = 5V | | -170 | | pA |
| | | Shutdown, V _{IN} = 0V, V _{OUT} = 20V | | -270 | | |
| I _{OUT_OFF} | Switch Off-Leakage at OUT | Shutdown, V _{IN} = 0V, V _{OUT} = 5V | | 1 | | μA |
| | | Shutdown, V _{IN} = 0V, V _{OUT} = 20V | | 2.6 | | |

Soft-Start (SS) Specifications (see Figure 1)

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---------------------|---|--|-----|-----|-----|-------|
| t _{DEB} | Soft-Start Debounce Time ⁸ | R _L = 100Ω, C _{OUT} = 300μF, V _{IN} = 5V | | 18 | | ms |
| t _R | Soft-Start V _{OUT} Rising Slew-Rate Ramp Time ⁹ | R _L = 100Ω, C _{OUT} = 300μF, V _{IN} = 5V | | 2.3 | | ms |
| | | R _L = 100Ω, C _{OUT} = 300μF, V _{IN} = 20V | | 2.6 | | |
| I _{LIM_SS} | Soft-Start Current Limit | V _{IN} = 5V to 20V | | 2.6 | | A |
| t _{LIM_SS} | Soft-Start Current Limit Time | V _{IN} = 5V to 20V | | 7 | | ms |
| T _{ACOK} | Power Good Flag Delay after t _{CLP_SS} | V _{IN} = 5V to 20V | | 3 | | ms |
| t _{OFF} | Turn-Off Delay Time ¹⁰ | V _{IN} = 5V to 20V | 0 | | 10 | μs |

Over-Voltage Protection (OVP) Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|-----------------------|--|--|------|----------------------------------|------|-------|
| V _{OVP} | Internally Fixed Over-Voltage Protection | V _{IN} rising OVP threshold | 22 | 23 | 25 | V |
| | | Hysteresis, V _{OVLO} = 0V | | 300 | | mV |
| t _{OVP} | OVP Response Time ¹¹ | R _L = 100Ω, C _{OUT} = 0μF, V _{IN} > V _{OVP} , V _{OVLO} = 0V | | 90 | | ns |
| t _{OVP_REC} | OVP Recovery Time ¹² | | | t _{DEB} +t _R | | ms |
| V _{OVLO} | Externally Adjustable Over-Voltage Lockout | V _{OVLO} enable threshold | 0.15 | 0.25 | 0.35 | V |
| | | V _{OVLO} rising OVP threshold | 1.10 | 1.227 | 1.34 | V |
| | | Hysteresis | | 25 | | mV |
| t _{OVLO} | OVLO Response Time ¹³ | R _L = 100Ω, C _{OUT} = 0μF | | 300 | | ns |
| t _{OVLO_REC} | OVLO Recovery Time | | | t _{DEB} +t _R | | ms |

(continued next page)

7. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization, and correlation with statistical process controls.

8. t_{DEB} is time from EN = H and V_{UVLO} < V_{IN} < V_{OVP} until V_{OUT} = 10%*V_{IN}.

9. t_R is time from V_{OUT} = 10%*V_{IN} until V_{OUT} = 90%*V_{IN}.

10. t_{OFF} is time from disable logic until V_{OUT} begins to fall.

11. t_{OVP} is time from V_{IN} > V_{OVP} until V_{OUT} stops rising.

12. t_{OVP_REC} is time from V_{IN} < V_{OVP} until V_{OUT} = 90%*V_{IN}.

13. t_{OVLO} is time from V_{OVLO} rises above its OVP threshold until V_{OUT} stops rising.

Electrical Characteristics (continued)¹⁴

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C and $V_{IN} = 3V$ to $20V$. Typical values are specified at $T_A = +25^\circ C$ with $V_{IN} = 5V$.

Reverse Current Protection (RCP) Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|----------------|--------------------------------------|--|-----|-----|-----|---------|
| V_{RCP} | RCP Droop Regulation Voltage | $V_{RCP} = V_{IN} - V_{OUT}$, $I_{OUT} = 100mA$ | 10 | 20 | 30 | mV |
| t_{RCP_REC} | RCP Fast Recovery Time ¹⁵ | | | 15 | | μs |

Over-Current Protection (OCP) Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|----------------|---------------------------------|-----------------------|-----|---------------|-----|-------|
| I_{OCP} | Over-Current Threshold | 240mA (max) test mode | 10 | 13 | | A |
| t_{OCP} | OCP Response Time ¹⁶ | | | 100 | | ns |
| t_{OCP_REC} | OCP Recovery Time | | | $t_{DEB}+t_R$ | | ms |

Over-Temperature Protection (OTP) Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|----------------|---|------------------------|-----|---------------|-----|------------|
| T_{OTP} | IC Junction Over-Temperature Protection | T_J rising threshold | | 150 | | $^\circ C$ |
| | | Hysteresis | | 20 | | $^\circ C$ |
| t_{OTP_REC} | OTP Recovery Time | | | $t_{DEB}+t_R$ | | ms |

Transient Voltage Suppression (TVS) Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|-----------|-------------------|------------|-----|------|-----|-------|
| V_{TVS} | TVS Clamp Voltage | | | 32.5 | | V |

14. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

15. t_{RCP_REC} is time from $V_{OUT} < V_{IN} - 90mV$ until switch turns back on. Before measuring, first raise V_{OUT} higher than $V_{IN} + 300mV$.

16. t_{OCP} is time from $I_{OUT} > I_{OCP}$ until switch turns off.

Timing Diagrams

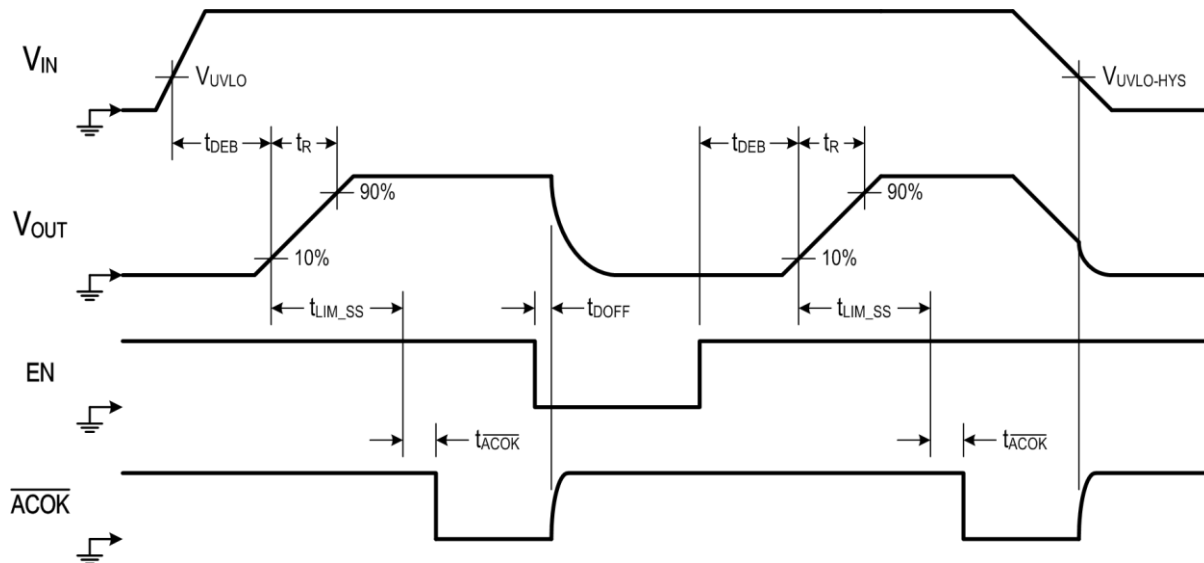


Figure 1. UVLO, Soft-Start and Turn-Off Timing Diagram

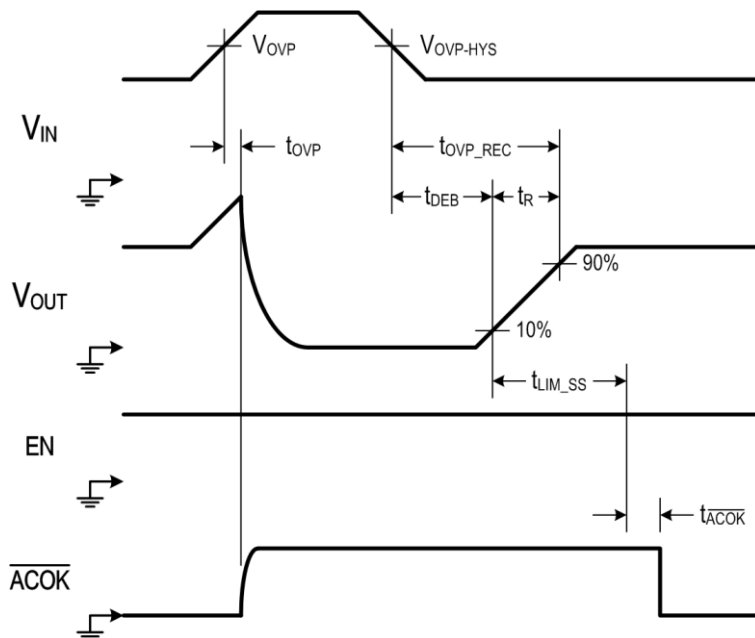


Figure 2. OVP Timing Diagram

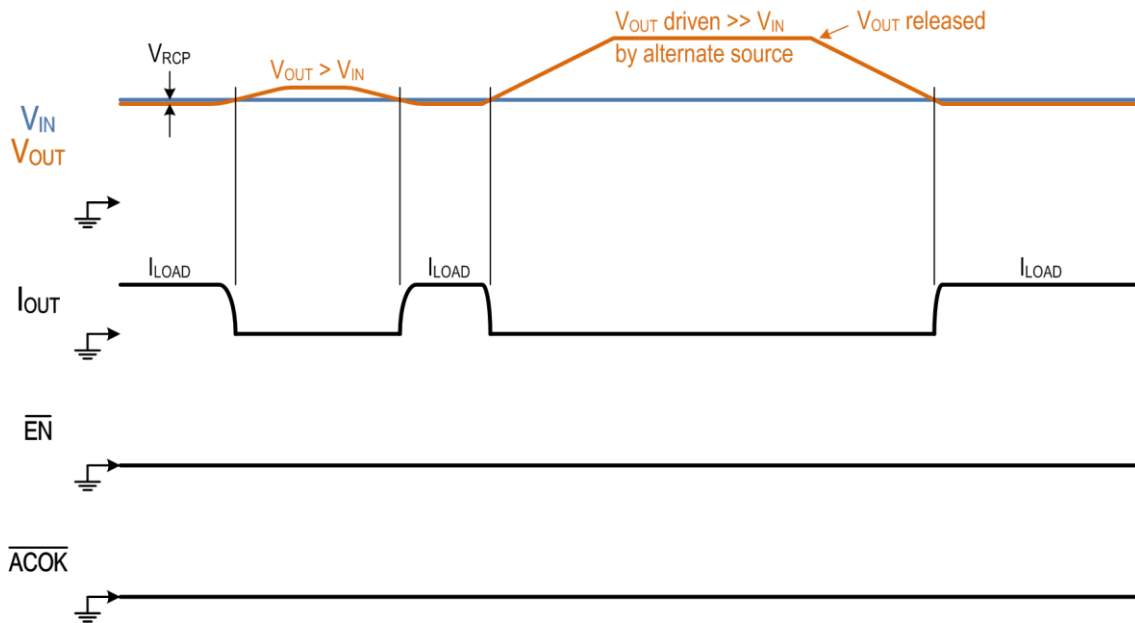


Figure 3. "Ideal Diode" RCP Timing Diagram with Fast Recovery

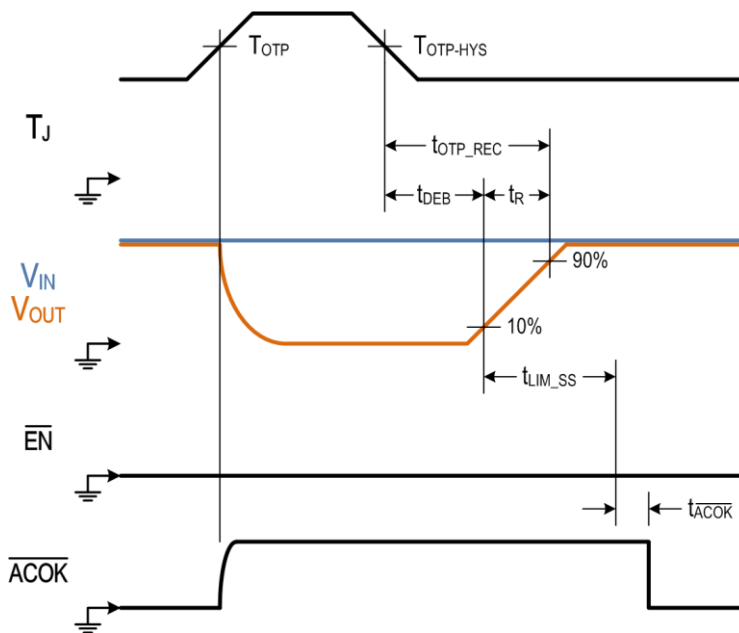


Figure 4. OTP Timing Diagram

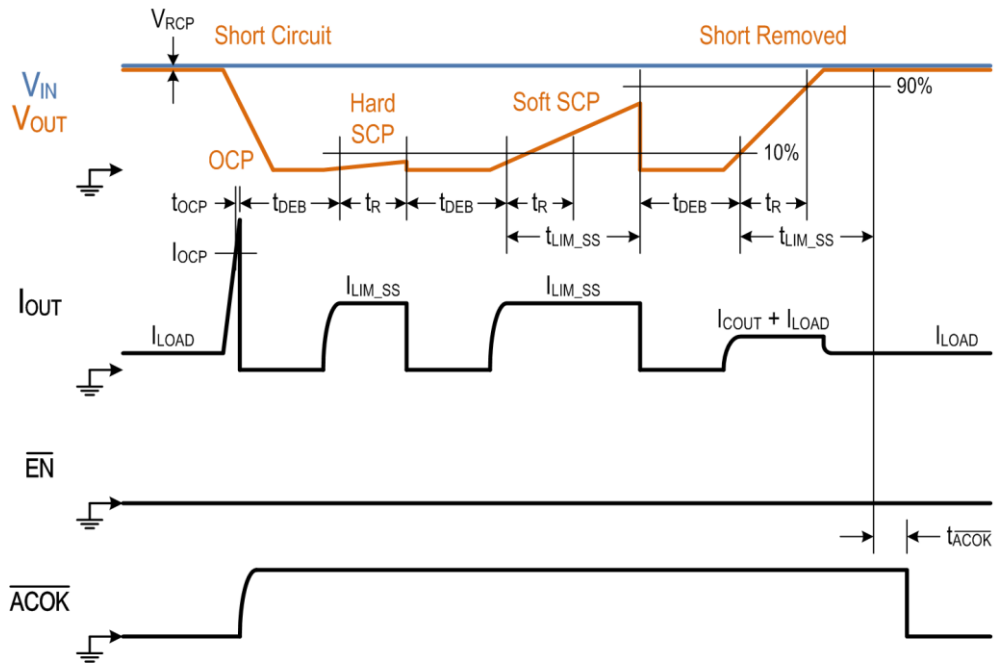
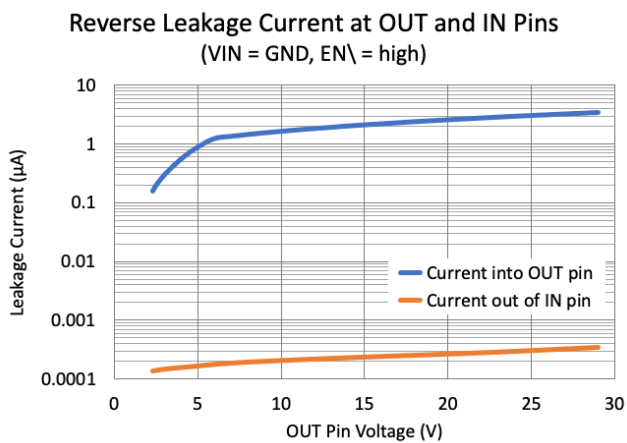
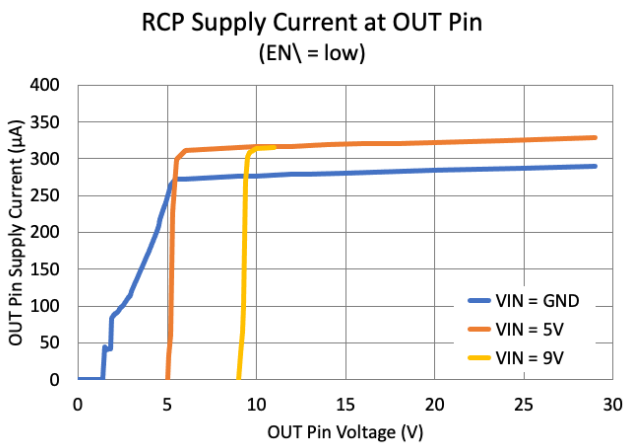
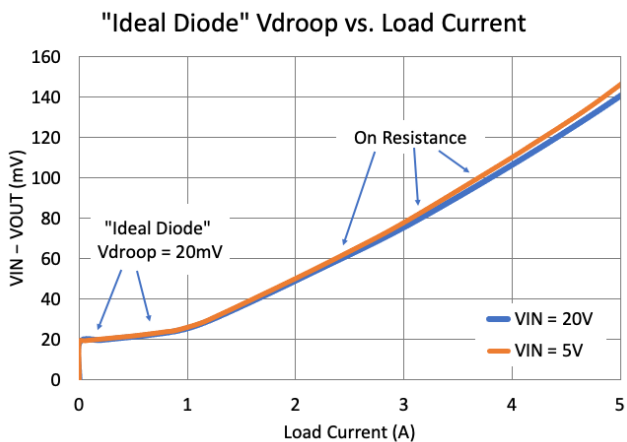
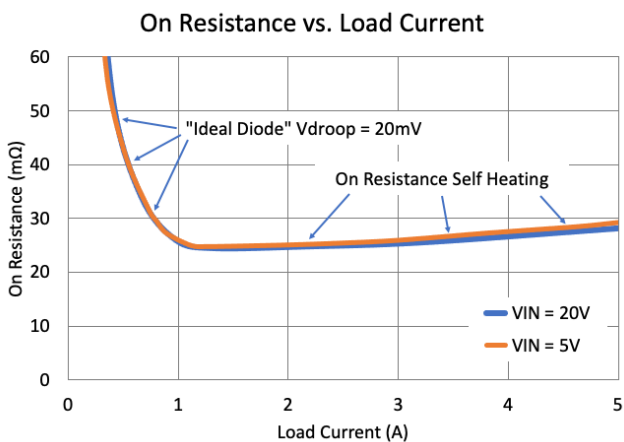
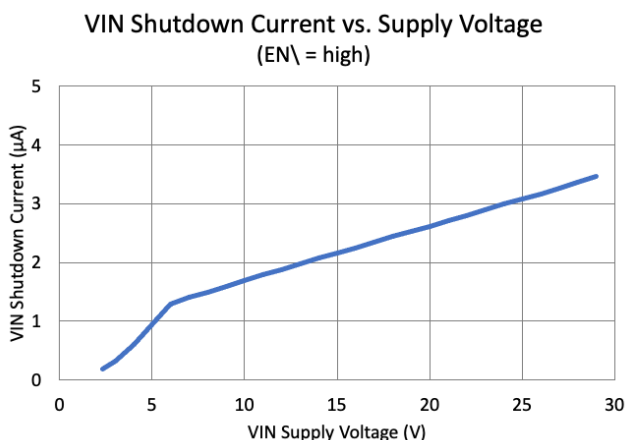
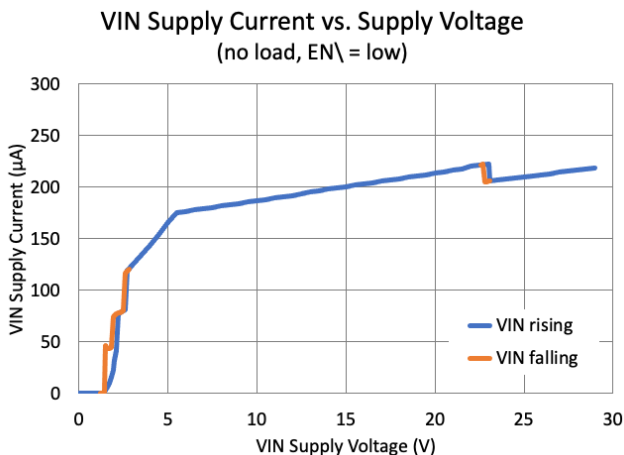


Figure 5. OCP and SCP Timing Diagram

Typical Characteristics

Unless otherwise noted, $T_A = +25^\circ\text{C}$ and $V_{IN} = 20\text{V}$.

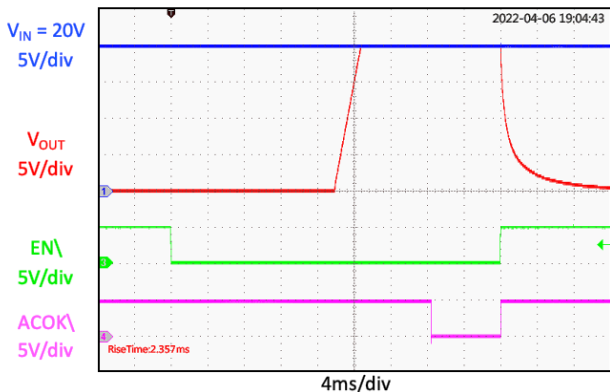


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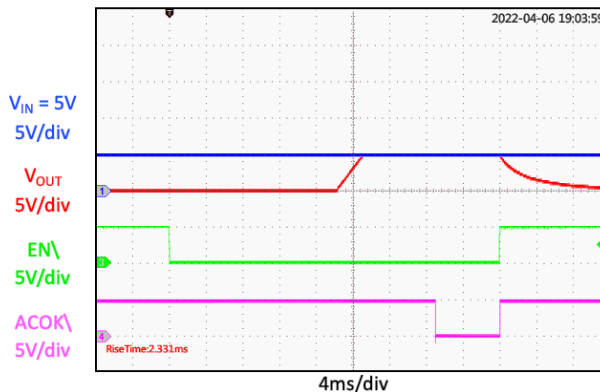
Typical Characteristics (continued)

Unless otherwise noted, $T_A = +25^\circ\text{C}$ and $V_{IN} = 20\text{V}$.

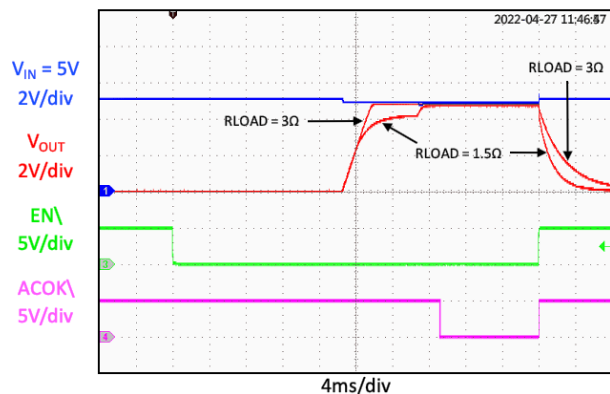
Enable, Soft-Start, Shutdown Response
($V_{IN} = 20\text{V}$)



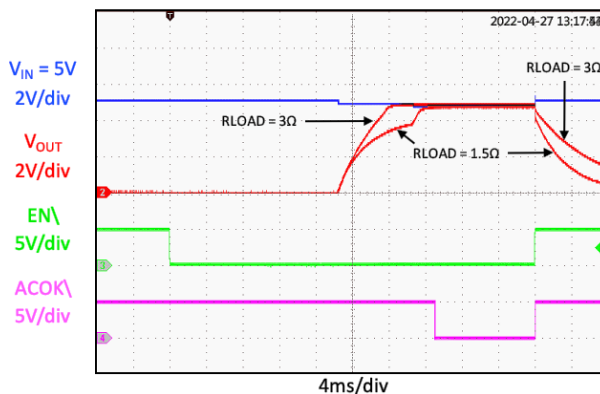
Enable, Soft-Start, Shutdown Response
($V_{IN} = 5\text{V}$)



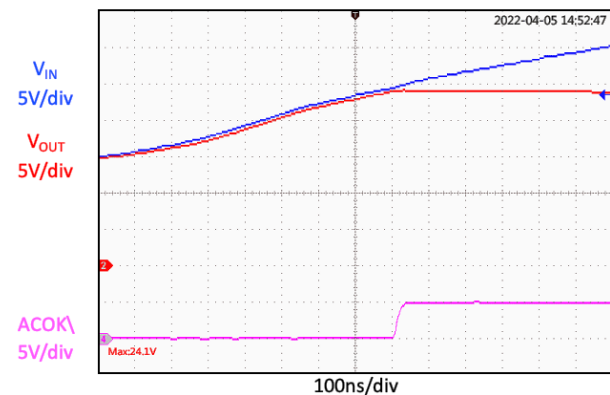
Heavy Load Soft-Start Response
($V_{IN} = 5\text{V}$, $C_{OUT} = 1000\mu\text{F}$)



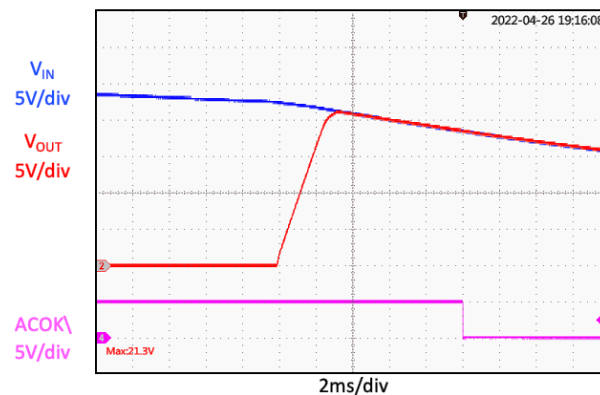
Heavy Load Soft-Start Response
($V_{IN} = 5\text{V}$, $C_{OUT} = 2200\mu\text{F}$)



OVP Response
($V_{IN} = 15\text{V} \rightarrow 28\text{V Short}$)



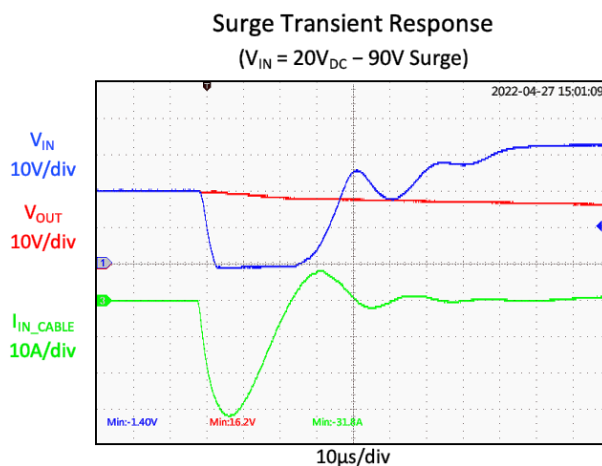
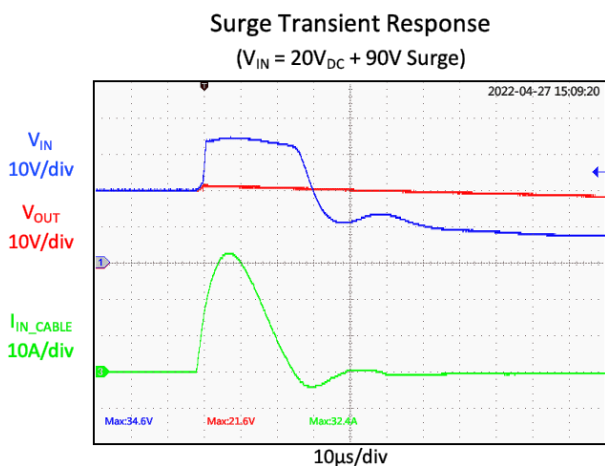
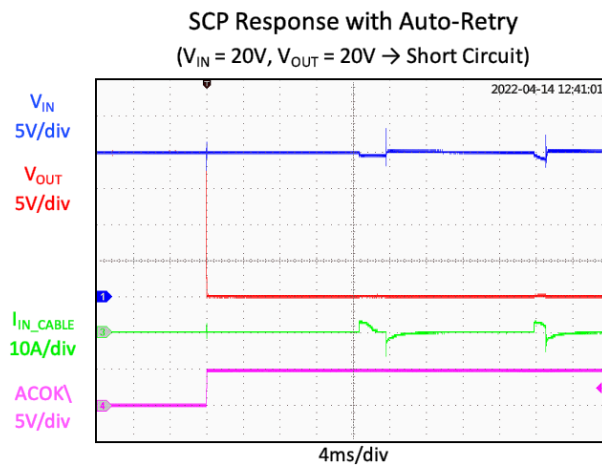
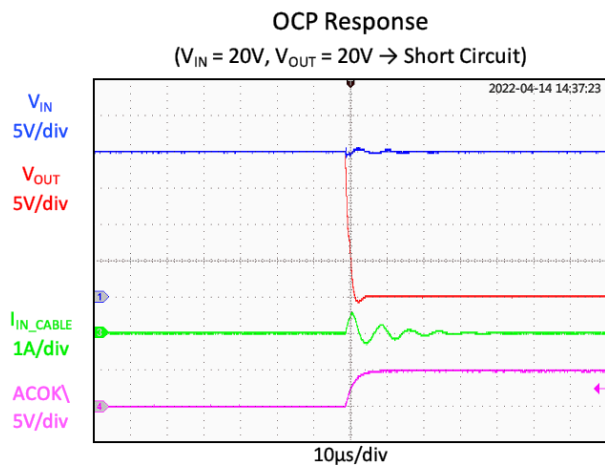
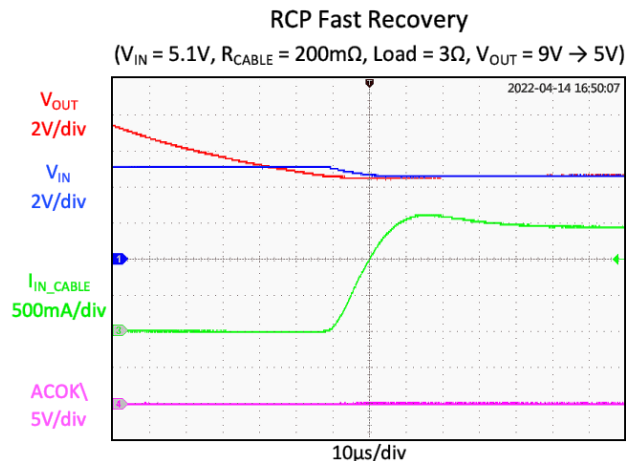
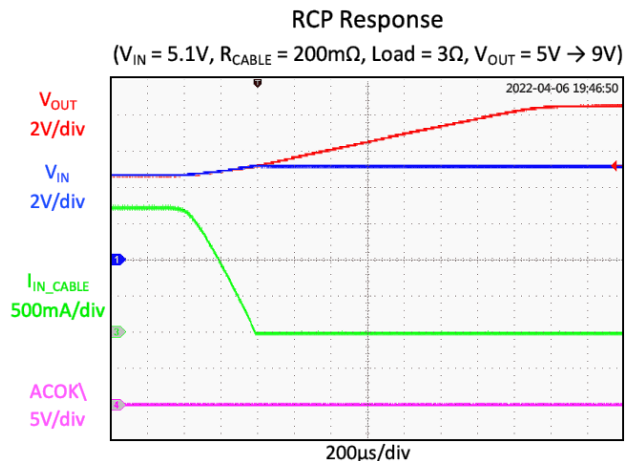
OVP Recovery
($V_{IN} = 28\text{V Short Removal} \rightarrow 15\text{V}$)



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Typical Characteristics (continued)

Unless otherwise noted, $T_A = +25^\circ\text{C}$ and $V_{IN} = 20\text{V}$.



Functional Block Diagram

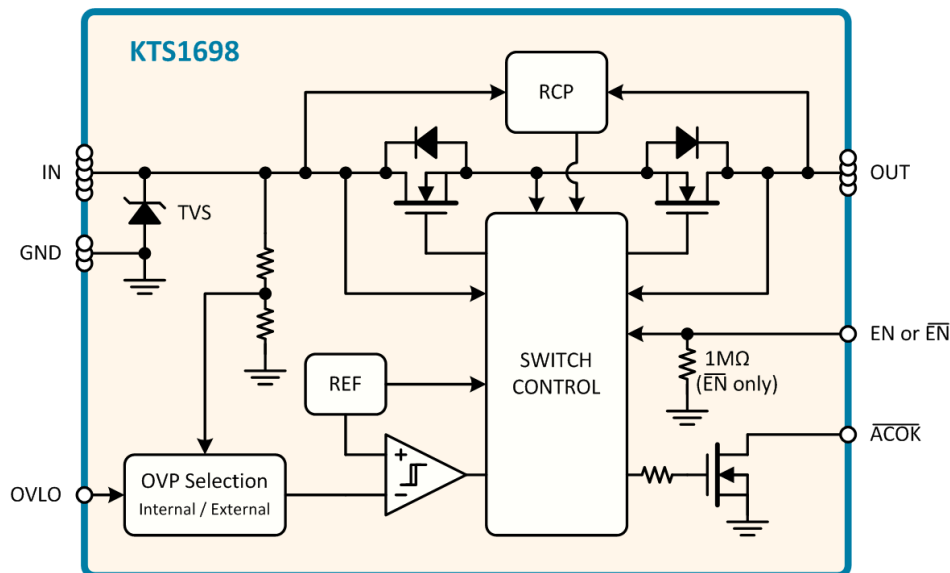


Figure 6. Functional Block Diagram

Functional Description

The KTS1698 is a slew-rate controlled, 25mΩ (typ) low resistance MOSFET switch intended to be inserted between a power source and a load to isolate and protect against abnormal voltage and current conditions. Featuring slew-rate controlled soft-start and soft-start current limit to prevent excessive large inrush current, the KTS1698 also features several additional protection functions. These include input over-voltage protection, “ideal diode” reverse-current protection with fast recovery, output short-circuit protection, over-current protection, over-temperature protection, and input transient voltage suppression for ±90V surge, ±8kV contact ESD, and ±15kV air-gap ESD protections.

Operating from a wide input voltage range of 3V to 23V, the KTS1698 is optimized for USB Type-C Power Delivery (PD) current-sink applications that require essential protection and enhanced system reliability. While in the OFF state, the KTS1698 blocks voltages of up to 29V on the IN and OUT pins and prevents current flow. While in the ON state, the KTS1698 withstands voltages of up to 29V on the IN and OUT pins, passes valid input voltages and current from IN to OUT, and blocks reverse current from OUT to IN. Due to the ideal-diode behavior, two or more KTS1698 parts connected in “diode-OR” configuration can be used in parallel to support systems that may be charged or powered from multiple ports.

Enable Input

The KTS1698A has \overline{EN} active-low input logic with internal 1MΩ pull-down. The KTS1698B has EN active-high input logic. When disabled, the power switch is off and the IC is placed into low-power shutdown mode. When enabled, the protection circuits and the power switch are on. An 18ms de-bounce timer deploys before device turn-on and the soft-start ramp.

Under-Voltage Lockout (UVLO)

When $V_{IN} < V_{UVLO}$, the power switch is disabled. Once V_{IN} exceeds V_{UVLO} , the power switch is controlled by the enable pin and fault detection circuits.

Soft-Start (SS)

The internal soft-start function allows the KTS1698 to charge a total output capacitance of over 1000µF to 5V without excessive in-rush current. Soft-start controls the output voltage slew-rate ramp time. Use the below formula to calculate the current required to charge C_{OUT}:

$$I_{IN_SS} = I_{LOAD} + C_{OUT} \left(\frac{V_{IN}}{t_R} \right)$$

where t_R = 2.3ms. In either case, the soft-start time is somewhat fast to reduce power dissipation in the KTS1698 during soft-start.

Note that in addition to the soft-start voltage ramp, the soft-start current limit is 2.6A (typ.) to prevent excessive heat when starting into an output short-circuit condition or a large total output capacitance. This current limit is turned off after 7ms. After an additional 3ms delay, if V_{OUT} is near V_{IN}, the \overline{ACOK} flag indicates a power good condition.

Over-Voltage Protection (OVP)

When logically enabled, the switch is normally on. However, if V_{IN} > V_{OVP}, the power switch is disabled due to an OVP fault. Once V_{IN} drops below V_{OVP}, no other fault is detected, and the enable logic is still valid, the power switch is re-enabled via the soft-start debounce and ramp time.

The OVLO pin is used to adjust the over-voltage threshold externally. The default internal over-voltage threshold is 23V when the OVLO pin is tied to GND. Biasing the OVLO pin with a resistive voltage divider adjusts the over voltage threshold from 4V to 23V as in the below formula:

$$V_{OVP} = V_{OVLO} \left(1 + \frac{R1}{R2} \right)$$

where V_{OVLO} = 1.227V. Connect R1 from IN to OVLO. Connect R2 from OVLO to ground.

“Ideal Diode” Reverse-Current Protection (RCP)

The KTS1698 offers reverse-current protection regardless of the enable logic level. When disabled, all current flow is blocked. When enabled, the RCP acts as a voltage droop regulator. Whenever the voltage on V_{OUT} is higher than V_{IN} minus 20mV, the RCP circuit reduces the MOSFET gate drive to try and maintain the regulated 20mV droop, thereby acting as an “ideal diode” with V_f = 20mV. See Figure 7. This control method blocks all reverse current. The RCP circuit makes it possible to connect two or more USB charging ports to a single battery charger IC input in a “diode-OR” configuration with autonomous reverse-current blocking. The KTS1698 includes a 15µs “fast recovery” when V_{OUT} falls back down below the “ideal diode” droop regulation point.

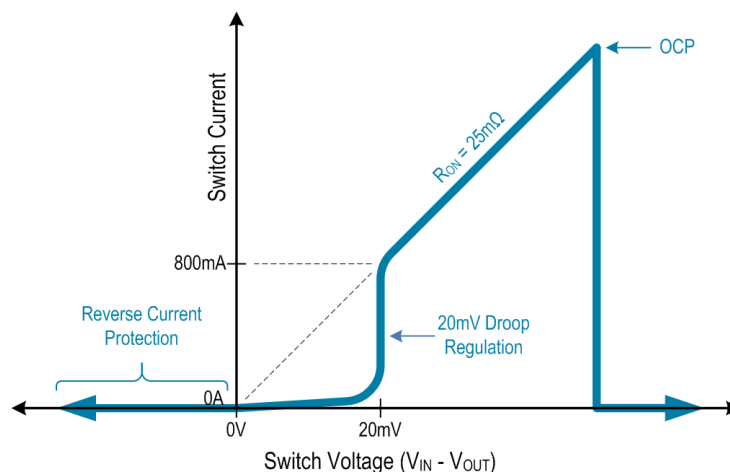


Figure 7. “Ideal Diode” Reverse-Current Protection V-I Curve

Over-Current Protection (OCP)

The KTS1698 includes output over-current protection (OCP) at 13A that protects the IC from damage when an over-current or short-circuit event suddenly appears. The OCP circuit quickly disables the power switch, so the current becomes zero. After an OCP event, if no other fault is detected, and the enable logic is still valid, the power switch is re-enabled via the soft-start debounce and ramp time.

Short-Circuit Protection (SCP)

The KTS1698 includes output short-circuit protection (SCP). If an SCP event occurs while the KTS1698 is already enabled and working, OCP is the first line of defense and responds very quickly. In this case, the current from C_{IN} through the switch to C_{OUT} increases very rapidly. For SCP events that do not reach OCP, if V_{OUT} droops significantly below V_{IN} , it is also detected as a soft-short event. In case of auto-retry or simply starting into a pre-existing SCP condition, the KTS1698 furthermore includes hard and soft SCP detection during soft-start if V_{OUT} is not ramping up. The KTS1698 remains undamaged during continuous SCP events.

Over-Temperature Protection (OTP)

When device junction temperature exceeds 150°C, the OTP circuit disables the power switch. Once the device junction temperature decreases below 130°C, if no other fault is detected, and the enable logic is still valid, the power switch is re-enabled via the soft-start debounce and ramp time.

Transient Voltage Suppression (TVS)

The KTS1698 integrates an active clamp transient voltage suppressor (TVS) from IN to GND. The TVS circuit provides protection to the KTS1698 and downstream circuits for IEC surge and ESD events. The protection is always active, whether the KTS1698 is enabled or disabled, powered or unpowered.

Auto-Retry

For all fault conditions that cause the switch to open, the KTS1698 will auto-retry via the soft-start debounce and ramp time. If any fault or the same fault is detected again, the switch will open again, and auto-retry will repeat. This continues until the fault is removed (normal operation), or the device is logically disabled via the \overline{EN} or EN pin, or V_{IN} is removed (UVLO).

\overline{ACOK} Output Flag

The \overline{ACOK} output is an open-drain output that requires an external pull-up resistor with recommended value in the 10k Ω to 200k Ω range. Connect \overline{ACOK} to GND or leave floating if unused. The \overline{ACOK} pin indicates the fault status. When there is no fault (UVLO, OVP, OCP, SCP, and OTP are not triggered) and the power switch is ON, then the \overline{ACOK} flag is pulled low to indicate the power is good. Otherwise, the \overline{ACOK} flag is high impedance. RCP is not classified as a fault condition.

Applications Information

Input Capacitor C_{IN} Selection

For most applications, connect a $1\mu\text{F}$ to $10\mu\text{F}$ ceramic capacitor as close as possible to the device from IN to GND to minimize the effect of parasitic trace inductance. 35V or 50V rated capacitors with X5R or better dielectric are recommended. For optimal surge and ESD performance, $10\mu\text{F}$ is preferred.

Output Capacitor C_{OUT} Selection

For most applications, connect from $10\mu\text{F}$ to $1000\mu\text{F}$ total capacitance to the output. Typical applications use $30\mu\text{F}$ to $100\mu\text{F}$ as needed for system load-transients. At minimum, connect a $10\mu\text{F}$ ceramic capacitor as close as possible to the device from OUT to GND to minimize the effect of parasitic trace inductance. 25V rated capacitors with X5R or better dielectric are recommended. Lower voltage ratings are acceptable when using the OVLO pin to set a lower over-voltage protection threshold.

Recommended PCB Layout

Good PCB thermal design is required to support heavy load currents. The KTS1698 EVB is designed with similar layout as Figure 8, but it extends the fill area for the IN, OUT, and GND copper planes to about 4 square inches total area for increased thermal performance. Due to the number of bumps on IN and OUT, these two planes are especially important and should not be ignored. Adding back-side and/or buried-layer fill area with thermal vias also helps significantly.

Other than thermal concerns, the PCB layout for the KTS1698 is quite simple. Place the input and output capacitors near the IC. Connect the capacitor ground terminals together and to the GND pins using the top-side copper layer. Route the control signals on buried layers. For internally set 23V OVP, directly connect the OVLO pin to the adjacent GND pins (as shown in Figure 8).

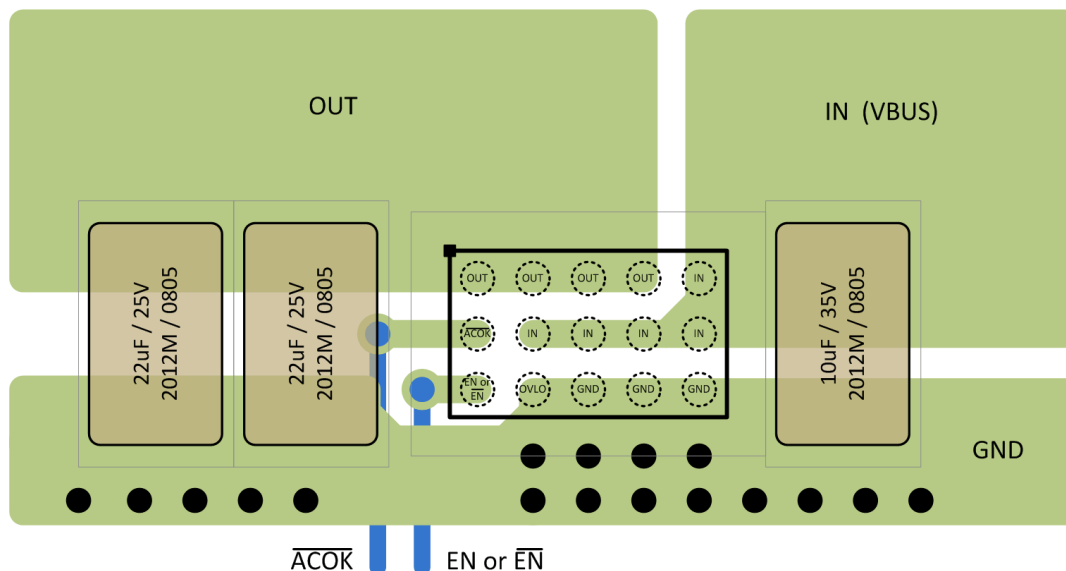


Figure 8. Recommended PCB Layout