USB Type-C Port Protector for CC and SBU Pins

Features

- Overvoltage Protection (OVP)
  - 24VDC Tolerance on CC1/2, SBU1/2
    - Robust 27V overshoot clamping
  - CC1/2 OVP = 5.8V
  - SBU1/2 OVP = 4.8V
  - Ultra-Fast 15ns Response Time
- IEC61000-4-5 Surge Protection
  - ±80V Surge Tolerance on CC1/2
  - ±35V Surge Tolerance on SBU1/2
- IEC61000-4-2 ESD Protection
  - ±15kV air gap on CC1/2, SBU1/2
  - ±8kV contact on CC1/2, SBU1/2
- ±2kV HBM on all pins (JEDEC JS-001-2017)
- Moisture Detection Compatible
  - Over 10MΩ to ground on CC1/2, SBU1/2
- CC Switches:
  - 1.25A, 330mΩ, 370pF, 17MHz
  - Automatic 5.1kΩ dead battery pull-down
- SBU Switches:
  - 4Ω, 27pF, 235MHz
  - Reverse current blocking when disabled
- 2.5V to 5.5V Operating Supply Voltage Range
- -40°C to 85°C Operating Temperature Range
- Pb-free 20 bump WLCSP (0.4mm pitch)

Brief Description

The KTU1101 provides ESD, surge, and overvoltage protection (OVP) for USB Type-C ports CC and SBU signal pins. ESD protection meets IEC61000-4-2 standards, eliminating the need for external TVS diodes. Surge protection meets IEC61000-4-5 standards, increasing immunity from power surges such as lightning strikes on the power lines while the USB cable is connected. Overvoltage protection (OVP) eliminates system damage due to physical or moisture-related shorts between the signal pins and VBUS at elevated PD voltage levels.

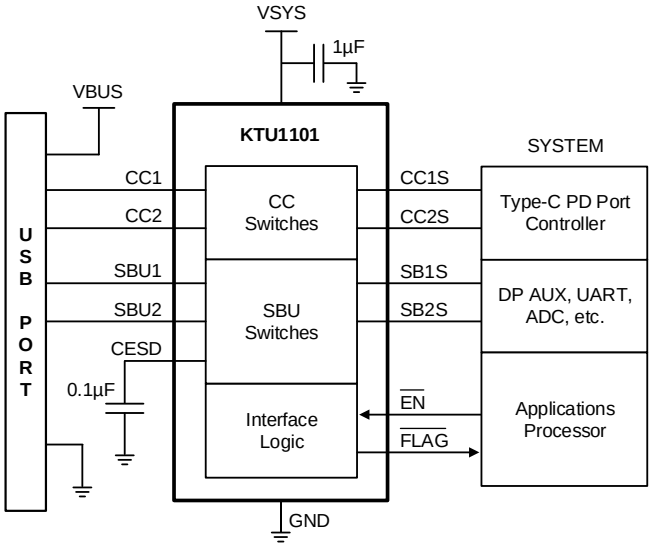
The SBU switches have low on-capacitance for passing high-speed signals. The CC1/2 switches have low on-resistance for passing V_{CONN} power up to 1.25A for CC power delivery communications. During dead battery conditions, internal 5.1kΩ resistors automatically pull down on CC1/2 to ensure that the up-stream source provides 5V to VBUS.

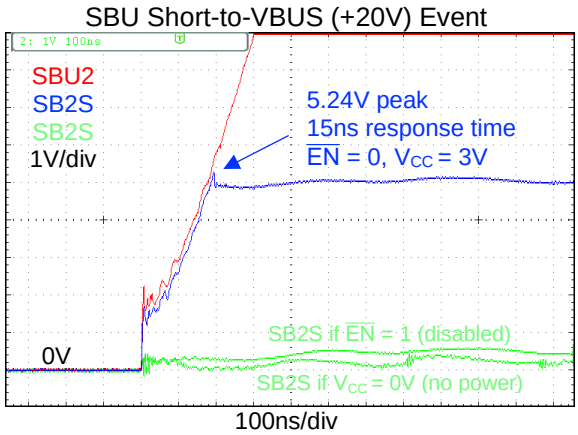
The KTU1101 is packaged in RoHS and Green compliant 1.7mm x 2.1mm wafer-level chip-scale package (WLCSP).

Applications

- Smartphones, Tablets, Notebooks, Monitors, TVs
- Accessories, AI/BT Loudspeakers, IoT
- Any USB Type-C port

Typical Application





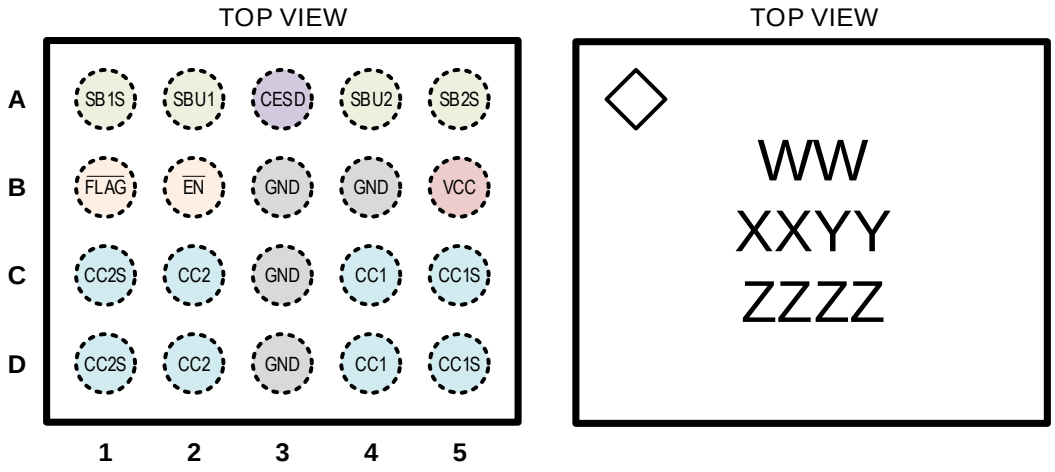
Conditions: SBU2 = 25mΩ short to +20V
SB2S (SB2S) = open, no load

Pin Descriptions

Pin #	Name	Function
B5	VCC	Device Supply Input – connect to a 2.5V to 5.5V source.
B3, B4, C3, D3	GND	Ground
C4, D4	CC1	Connector side of CC1 switch
C2, D2	CC2	Connector side of CC2 switch
C5, D5	CC1S	System side of CC1 switch
C1, D1	CC2S	System side of CC2 switch
A2	SBU1	Connector side of SBU1 switch
A4	SBU2	Connector side of SBU2 switch
A1	SB1S	System side of SBU1 switch
A5	SB2S	System side of SBU2 switch
A3	CESD	Capacitor connection for ESD/surge protection for SBU1 and SBU2 inputs.
B2	$\overline{EN}$	Active low enable input – drive $\overline{EN}$ to logic low level to enable the device. Drive $\overline{EN}$ to logic high level to disable the device and place all the switches in a high impedance state.
B1	$\overline{FLAG}$	Active low fault flag output to alert system to an OVP fault condition

Pinout Diagram

WLCSP45-20



20-Bump 1.71mm x 2.05mm x 0.620mm
WLCSP Package, 0.4mm pitch

Top Mark
MC = Device ID Code
XX = Date Code, YY = Assembly Code
ZZZZ = Serial Number

Absolute Maximum Ratings[1]

(T_A = 25°C unless otherwise noted)

Symbol	Description	Value	Units
V_{CC}	VCC to GND	-0.3 to 6	V
V_{IO}	CC1, CC2, SBU1, SBU2 to GND	-0.3 to 24	V
	CC1S, CC2S, SB1S, SB2S to GND	-0.3 to 8	V
	$\overline{EN}$, $\overline{FLAG}$ to GND	-0.3 to 6	V
I_{IO}	CCn to CCnS Continuous Current	±1.25	A
	CCn to CCnS Peak Current (2.5ms)	±2.0	A
	SBUn to SBnS, Continuous Current	±400	mA
V_{CESD}	CESD to GND	-0.3 to 22	V
T_J	Operating Temperature Range	-40 to 150	°C
T_S	Storage Temperature Range	-65 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	260	°C

ESD and Surge Ratings[2]

Symbol	Description	Value	Units
V_{ESD_HBM}	JEDEC JS-001-2017 ESD Human Body Model (all pins)	±2	kV
V_{ESD_CDM}	JESD22-C101-C ESD CDM Model (all pins)	±1	kV
V_{ESD_CD}	IEC61000-4-2 ESD Contact Discharge (CC1, CC2, SBU1, SBU2)	±8	kV
V_{ESD_AGD}	IEC61000-4-2 ESD Air-Gap Discharge (CC1, CC2, SBU1, SBU2)	±15	kV
V_{SURGE}	IEC61000-4-5 Surge (CC1, CC2 to GND)	±80	V
	IEC61000-4-5 Surge (SBU1, SBU2 to GND)	±35	V

Thermal Capabilities[3]

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance – Junction to Ambient	50	°C/W
P_D	Maximum Power Dissipation at 25°C	2	W
$\Delta P_D/\Delta_T$	Derating Factor Above T_A = 25°C	-20	mW/°C

Ordering Information

Part Number	Marking[4]	Operating Temperature	Package
KTU1101EVF-TR	MCXXYYZZZZ	-40°C to +85°C	WLCSP45-20

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
2. ESD and Surge Ratings conform to JEDEC and IEC industry standards. Some pins may actually have higher performance.
3. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.
4. “MC” is the device ID. “XXYY” is the date code and assembly code. “ZZZZ” is the serial number.

Electrical Characteristics[5]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C and V_{CC} = 2.5V to 5.5V. Typical values are specified at T_A = +25°C with V_{CC} = 3.0V.

Symbol	Description	Conditions	Min	Typ	Max	Units
Supply Specifications						
V_{CC}	Supply Operating Range		2.5		5.5	V
V_{UVLO}	Under-Voltage Lockout Threshold	Rising threshold	2.2	2.3	2.45	V
		Hysteresis		100		mV
I_{CC}	Supply Current	Enabled, V_{CC} = 3.0V, $V_{\overline{EN}}$ = 0V		55	80	µA
		Shutdown, V_{CC} = 3.0V, $V_{\overline{EN}}$ = V_{CC}		0.1	1	µA
Logic Specifications						
V_{IH}	Input Logic High ($\overline{EN}$)		1.0			V
V_{IL}	Input Logic Low ($\overline{EN}$)				0.4	V
I_{I_LK}	Input Logic Leakage ($\overline{EN}$)	T_A = +25°C, V_I = 0V or V_{CC}	-1	±0.01	1	µA
V_{OL}	Output Logic Low ($\overline{FLAG}$)	I_{OSINK} = 1mA		0.1	0.4	V
I_{O_LK}	Output Logic Leakage ($\overline{FLAG}$)	T_A = +25°C, V_O = high-Z or V_{CC}		0.01	1	µA
$t_{\overline{FLAG}}$	$\overline{FLAG}$ Response Time	Activation		80		ns
		Recovery		80		ns
Thermal Shutdown Specifications						
T_{J_SHDN}	IC Junction Thermal Shutdown	T_J rising		150		°C
		Hysteresis		20		°C

(continued next page)

5. Device is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

Electrical Characteristics (continued)[5]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C and V_{CC} = 2.5V to 5.5V. Typical values are specified at T_A = +25°C with V_{CC} = 3.0V.

Symbol	Description	Conditions	Min	Typ	Max	Units
CC Switch Specifications						
$V_{CC1/2}$	Switch Voltage Operating Range		-0.3		5.5	V
V_{OVP_CC}	OVP Threshold	Rising threshold	5.55	5.8	6.1	V
		Hysteresis		100		mV
R_{ON_CC}	On-Resistance	Value, $V_{CC1/2}$ = 0V to V_{CC}		330	500	mΩ
		Flatness, $V_{CC1/2}$ = 0V to V_{CC}		0.2		mΩ
		Matching, $V_{CC1/2}$ = 0V to V_{CC}		0.16		mΩ
C_{ON_CC}	On-Capacitance			370		pF
BW_{ON_CC}	On-Bandwidth	R_S = R_L = 50Ω, $V_{CC1/2}$ = 0dBm		17		MHz
		Intended CC PD data rate		300		kbps
$R_{CC1/2\_GND}$	Resistance to GND	$V_{CC1/2} \leq V_{CC}$, T_A = +25°C	10	12.8		MΩ
I_{CCLK}	Switch Off Leakage Current	V_{CC} = 0V, $V_{CC1/2}$ = 5.5V, $V_{CC1/2S}$ = 0V, T_A = +25°C, measure current out of CC1/2S		0.01	1	µA
R_{DB}	Dead Battery Pull-Down Resistance	$V_{CC} < V_{UVLO}$, $\overline{EN}$ = 0, $V_{CC1/2}$ = 2.6V	4.1	5.1	6.1	kΩ
		$V_{CC} > V_{UVLO}$, $\overline{EN}$ = 1, $V_{CC1/2}$ = 2.6V	4.1	5.1	6.1	kΩ
$V_{CC1/2\_DB}$	Dead Battery Threshold Voltage	$V_{CC} < V_{UVLO}$, $I_{CC1/2}$ = 80µA	0.5	0.82	1.2	V
t_{ON_CC}	Switch Turn-On Time	V_{CC} rising > V_{UVLO}, $\overline{EN}$ = 0		100		µs
		V_{CC} = 3.0V, $V_{\overline{EN}}$ falling < V_{IL}		75		µs
t_{OFF_CC}	Switch Turn-Off Time	V_{CC} falling < V_{UVLO}, $\overline{EN}$ = 0		1		µs
		V_{CC} = 3.0V, $V_{\overline{EN}}$ rising > V_{IH}		0.1		µs
$t_{OVP\_CC\_R}$	OVP Rising Response Time	V_{CC} = 3.0V, CC1/2 = +80Vsurge, CC1/2S = 5.1kΩ to GND, T_A = +25°C		15		ns
$t_{OVP\_CC\_F}$	OVP Falling Debounce Time			25		µs

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Electrical Characteristics (continued)[5]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C and V_{CC} = 2.5V to 5.5V. Typical values are specified at T_A = +25°C with V_{CC} = 3.0V.

Symbol	Description	Conditions	Min	Typ	Max	Units
SBU Switch Specifications						
$V_{SBU1/2}$	Switch Voltage Operating Range		-0.3		4.5	V
V_{OVP_SBU}	OVP Threshold	Rising threshold	4.65	4.8	4.95	V
		Hysteresis		100		mV
R_{ON_SBU}	On-Resistance	Value, $V_{SBU1/2}$ = 0V to V_{CC}		4	10	Ω
		Flatness, $V_{SBU1/2}$ = 0V to V_{CC}		2.4		mΩ
		Matching, $V_{SBU1/2}$ = 0V to V_{CC}		0.8		mΩ
C_{ON_SBU}	On-Capacitance			27		pF
BW_{ON_SBU}	On-Bandwidth	R_S = R_L = 50Ω, $V_{SBU1/2}$ = 0dBm		235		MHz
		Intended DP1.1 AUX data rate		1		Mbps
$R_{SBU1/2\_GND}$	Resistance to GND	$V_{SBU1/2} \leq V_{CC}$, T_A = +25°C	10	12.8		MΩ
I_{SBULK}	Switch Off Leakage Current	V_{CC} = 0V, $V_{SBU1/2}$ = 4.5V, $V_{SB1/2S}$ = 0V, T_A = +25°C, measure current out of SB1/2S		0.01	1	µA
I_{SBULK_RB}	Switch OFF Reverse Blocking Leakage Current	V_{CC} = 0V, $V_{SBU1/2}$ = 0V, $V_{SB1/2S}$ = 4.5V, T_A = +25°C, measure current into SB1/2S		0.01	1	µA
t_{ON_SBU}	Switch Turn-On Time	V_{CC} rising > V_{UVLO}, $\overline{EN}$ = 0		60		µs
		V_{CC} = 3.0V, $V_{\overline{EN}}$ falling < V_{IL}		45		µs
t_{OFF_SBU}	Switch Turn-Off Time	V_{CC} falling < V_{UVLO}, $\overline{EN}$ = 0		1		µs
		V_{CC} = 3.0V, $V_{\overline{EN}}$ rising > V_{IH}		0.1		µs
$t_{OVP\_SBU\_R}$	OVP Response Time	V_{CC} = 3.0V, initial $V_{SBU1/2}$ = 3.3V, SBU1/2 = +35Vsurge, SB1/2S = 100kΩ to GND, T_A = +25°C		15		ns
$t_{OVP\_SBU\_F}$	OVP Falling Debounce Time			25		µs

Timing Diagrams

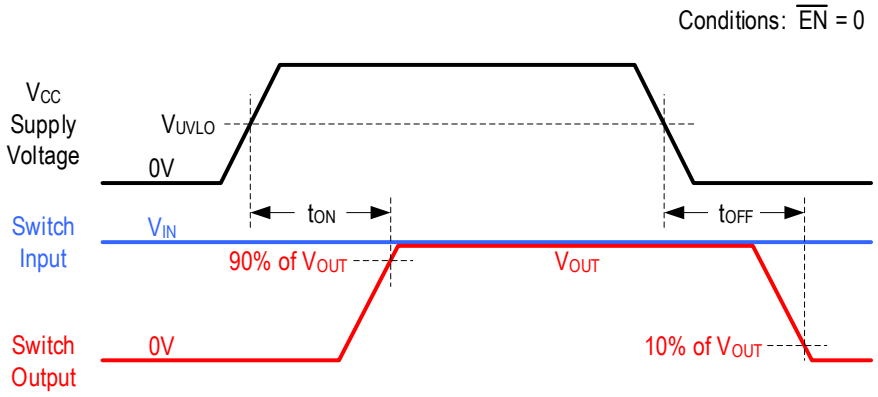


Figure 1. Switch Enable/Disable (via V_{CC} rising/falling) Timing Diagram

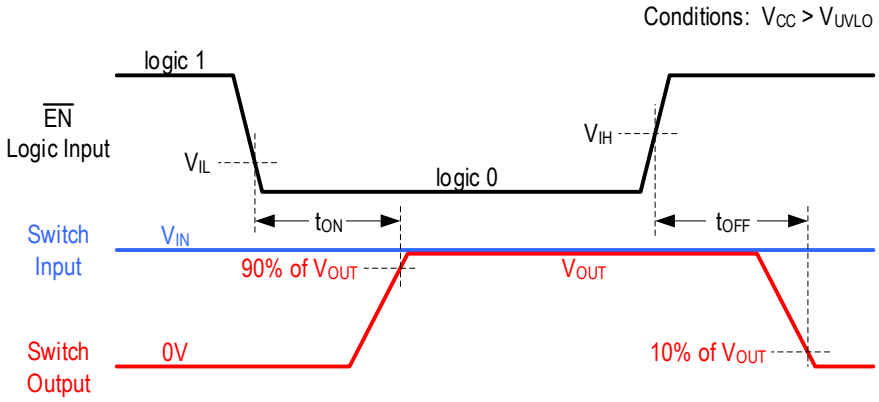


Figure 2. Switch Enable/Disable (via $\overline{EN}$ falling/rising) Timing Diagram

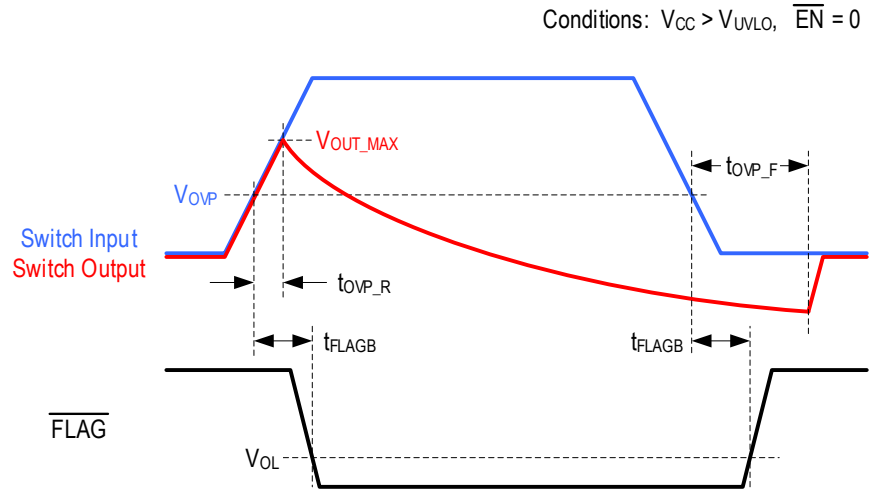
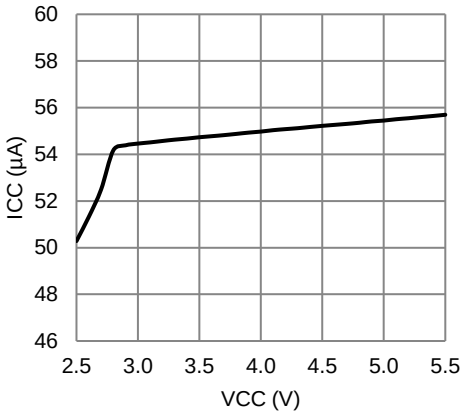


Figure 3. OVP Fault Protection Timing Diagram

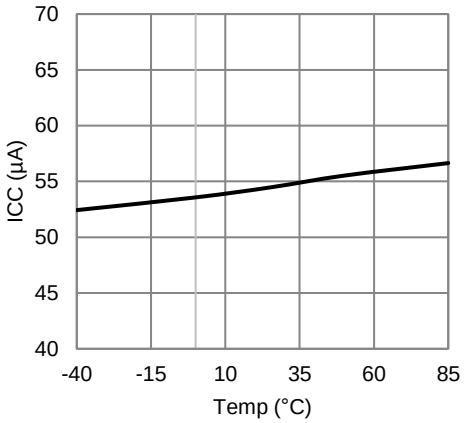
Typical Characteristics (continued)

VCC = 3V, $V_{\overline{EN}}$ = 0V, C_{VCC} = 1µF, C_{ESD} = 0.1µF, T_{AMB} = 25°C unless otherwise specified.

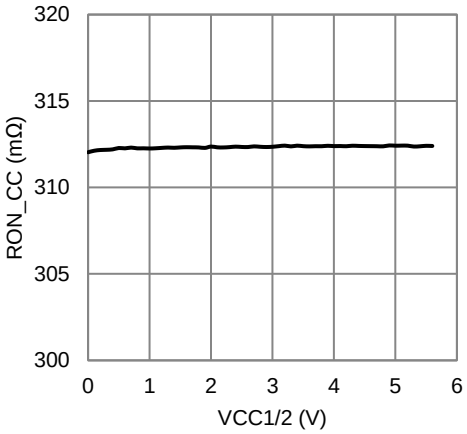
Supply Current vs. VCC Supply Voltage



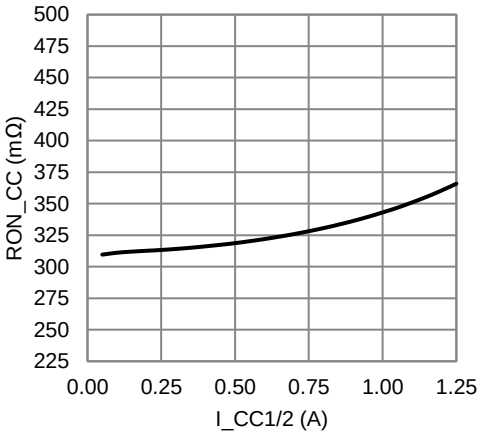
Supply Current vs. Temperature



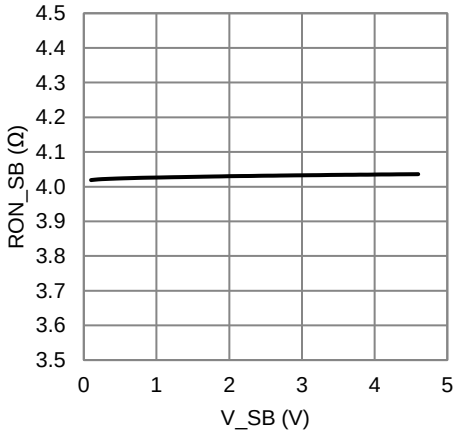
CC Switch Ron vs. Switch Voltage ($I_{CC1/2S}$ = 200mA)



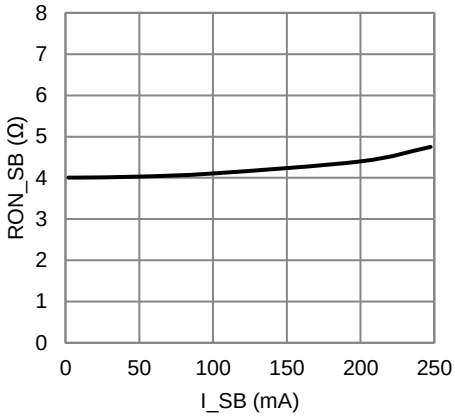
CC Switch Ron vs. Switch Current



SBU Switch Ron vs. Switch Voltage ($I_{SB1/2S}$ = 100mA)



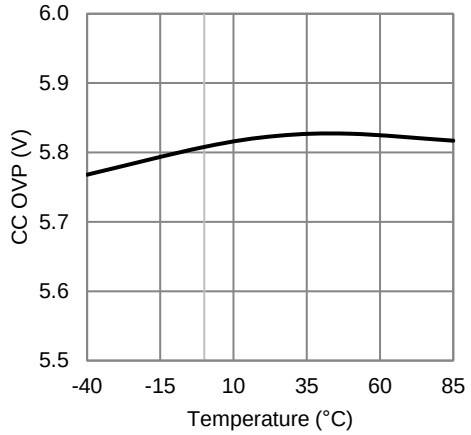
SBU Switch Ron vs. Switch Current



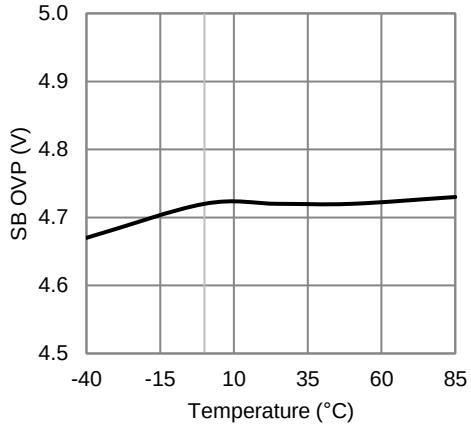
Typical Characteristics (continued)

VCC = 3V, $V_{\overline{EN}}$ = 0V, C_{VCC} = 1µF, C_{ESD} = 0.1µF, T_{AMB} = 25°C unless otherwise specified.

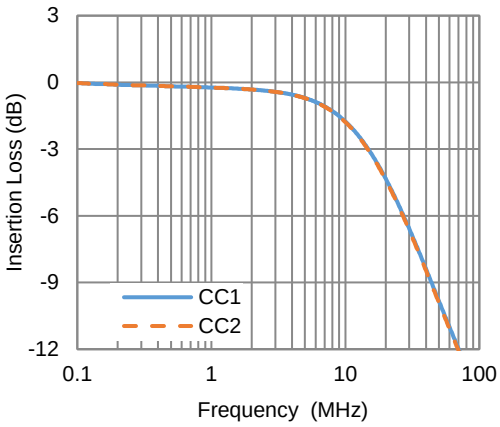
CC Switch OVP vs. Temperature



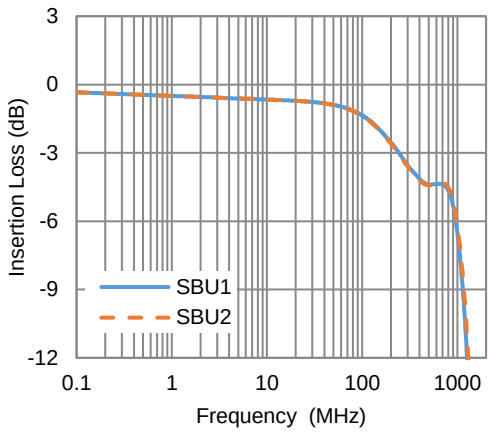
SB Switch OVP vs. Temperature



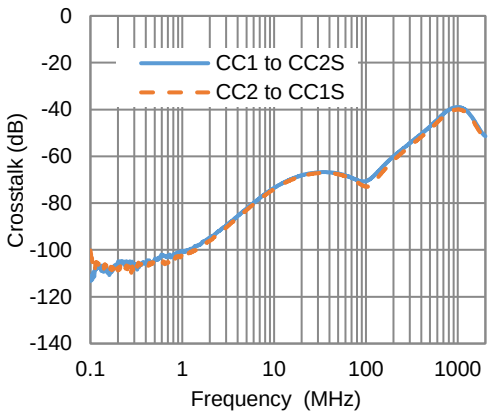
CC Switch Bandwidth



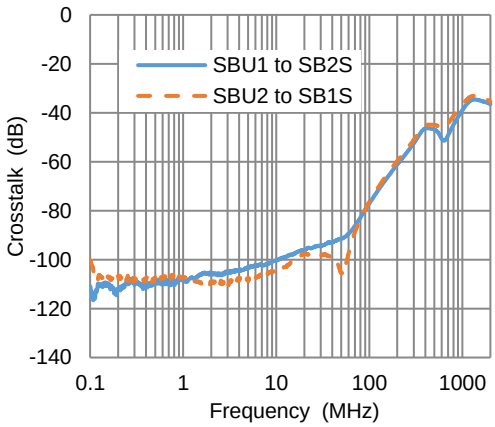
SBU Switch Bandwidth



CC Switch Crosstalk



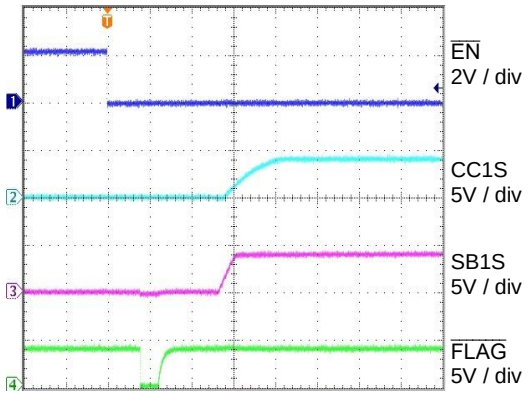
SBU Switch Crosstalk



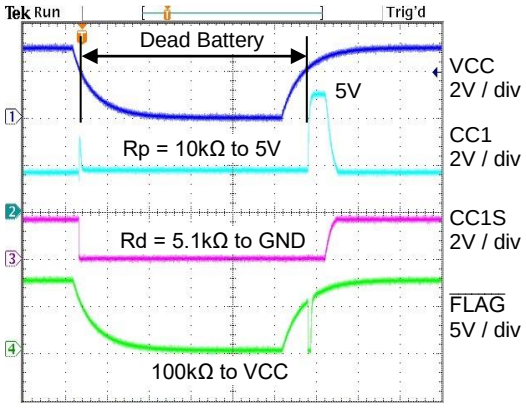
Typical Characteristics (continued)

VCC = 3V, $V_{\overline{EN}}$ = 0V, C_{VCC} = 1µF, C_{ESD} = 0.1µF, T_{AMB} = 25°C unless otherwise specified.

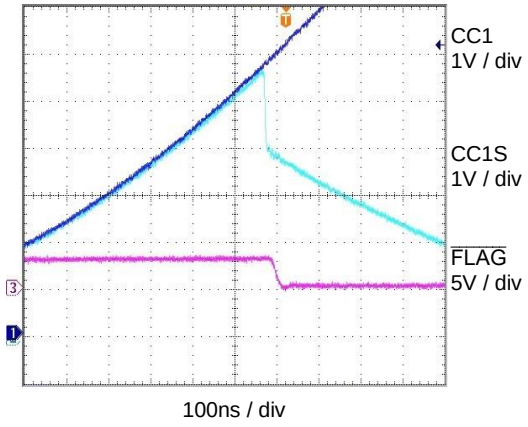
Switch Turn On (Enable)



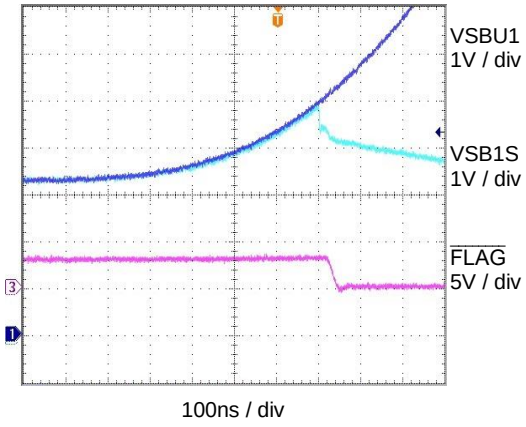
Dead Battery – Activation and Recovery



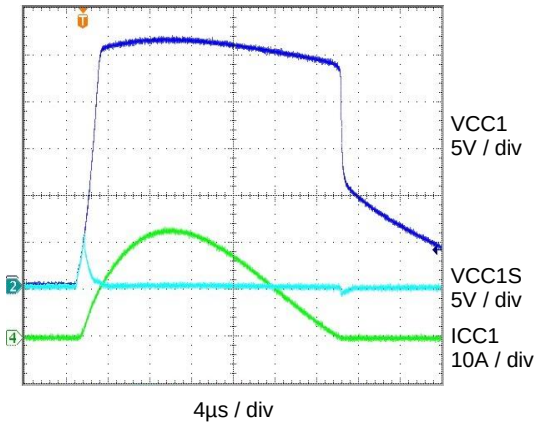
CC OVP Transient



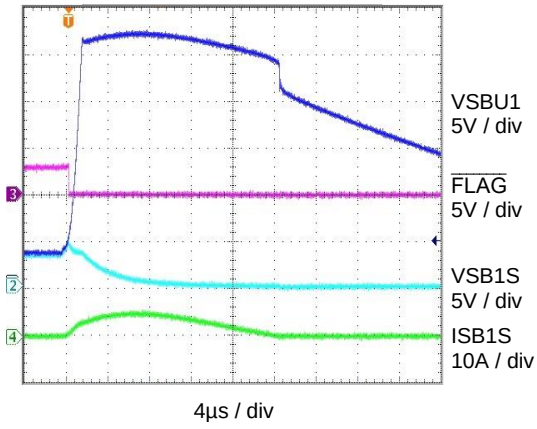
SBU OVP Transient



Surge +80V CC



Surge +35V SBU



Functional Block Diagram

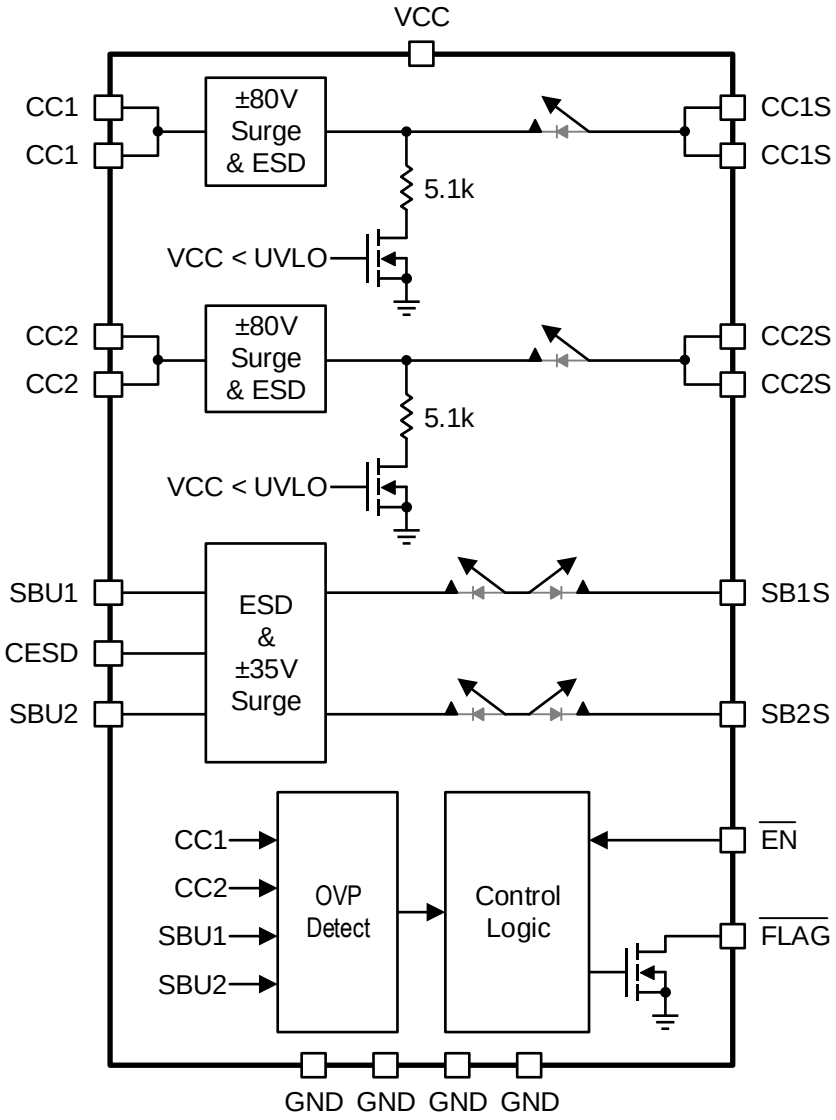


Figure 4. Functional Block Diagram

Functional Description

The KTU1101 is designed to provide overvoltage protection (OVP) switches for USB Type-C port CC and SBU signal pins, with protection from voltage surges and electro-static discharge (ESD). Fault conditions can occur at the input port receptacle due to mechanical shorts of the CC and SBU pins to VBUS PD levels up to 24V. The KTU1101 provides these functions along with an IC enable control and an open drain fault flag to alert the system controller to a fault event.

The CC1/2 protection switches have a low on-resistance value that is typically 300mΩ. This low on-resistance allows the CC1/2 switches to pass V_{CONN} power up to 1.25A without excess voltage drop or power dissipation issues. The typical 370pF switch capacitance provides a typical signal bandwidth of 17Mhz, which is more than required for the USB PD data rate of 300kbps.

The SBU1/2 protection switches are designed to accommodate high data rate SBU functions with a low switch on-capacitance that is typically 27pF or better with an effective switch bandwidth of 235MHz. This bandwidth can support DP1.1 AUX applications at 1Mbps and is capable of data rates up to 50Mbps. The SBU1/2 switches are reverse current blocking when disabled to protect the system controller in the event of an SBU port pin short circuit condition.

The IC also has a dead battery function for CC1/2 USB Type-C operation which presents internal 5.1KΩ pull-downs in the event of a dead battery. To aid in moisture detection within the USB Type-C receptacle, the CC1/2 and SBU1/2 switches have over 10MΩ resistance to ground in normal operation. Refer to the IC application information section for dead battery and moisture detection features.

Overvoltage Protection (OVP)

Overvoltage events can occur on the CC and SBU signal lines caused by a short to VBUS with voltages that can range up to the full USB PD 20V level. Overvoltage events can also be induced by faulty external adaptors or USB devices connected to the USB Type-C input. To guard against such events, both the CC1/2 and SBU1/2 switches are overvoltage tolerant up to 24VDC and include 27V surge clamps.

When enabled, the KTU1101 continuously monitors the voltage level present on the CC1/2 and SBU1/2 signal lines. If the voltage on either CC1/2 exceeds 5.8V (nominal) or if SBU1/2 exceeds 4.8V (nominal), the IC control shuts down (turns off) all switches to protect the downstream system from the overvoltage event. CC1/2 and SBU1/2 switches typically respond to an OVP event in 15ns. Switch operation automatically resumes when the applied CC1/2 voltage drops below 5.7 or the SBU1/2 voltage drops below 4.7V, as there is a 100mV OVP threshold hysteresis for both pairs of signal switches. In additional to the OVP function, the SBU switches also provide reverse current blocking when the device is disabled during an OVP event.

ESD and Surge Protection

The KTU1101 ESD protection is compliant to IEC61000-4-2 levels, providing CC1/2 and SBU1/2 air gap protection up to ±15kV and contact protection up to ±8kV. The KTU1101 is also ±2kV HBM compliant to JEDEC JS-001-2017 standards. The CC1/2 input is able to stand off ESD events up to the stated specifications. The SBU1/2 high bandwidth devices utilize an ESD support capacitor to allow these inputs to meet ESD requirements. A 50V rated 0.1µF ceramic capacitor is placed between the CESD pin and ground for this function.

In addition to ESD protection, the KTU1101 also has input surge protection compliant to IEC61000-4-5 specifications for both the CC1/2 and SBU1/2 input lines. The CC1/2 input pins can stand off input surge events up to ±80V. The SBU1/2 high bandwidth inputs can stand off surge events up to ±35V.

Fault Reporting

Should an OVP, surge or over temperature event occur causing the device to open the protection switches, an active-low, open-drain MOSFET fault flag ($\overline{FLAG}$) will be asserted to alert the system controller to the fault event. Both the fault flag assertion time and the recovery time after a fault is cleared are typically 80ns.

IC Protection

In addition to ESD, surge and OVP protection, the KTU1101 also includes internal thermal monitoring/shutdown and input supply under voltage lockout features. The IC will automatically shut down if the internal die temperature exceeds 150°C (nominal). There is 20°C of hysteresis, allowing the IC to automatically restart and resume operation when the internal die temperature cools to a level below 130°C (nominal).

IC Enable

The KTU1101 is on/off controlled by an active low enable signal applied to the $\overline{EN}$ input. Refer to Table 1 for IC enable versus switch state logic.

Table 1. Control Logic Table

IC Power	$\overline{EN}$	Conditions	Switch On/Off Status		Input Resistance to GND		$\overline{FLAG}$
			CC1/2	SBU1/2	CC1/2	SBU1/2	
$V_{CC} > V_{UVLO}$	0	No Faults	ON	ON	>10MΩ	>10MΩ	High-Z
	0	$V_{CC1/2} > V_{OVP\_CC}$	OFF	OFF	>10MΩ	>10MΩ	Active Low
	0	$V_{SBU1/2} > V_{OVP\_SBU}$	OFF	OFF	>10MΩ	>10MΩ	Active Low
	0	$T_J > T_{J\_SHDN}$	OFF	OFF	>10MΩ	>10MΩ	Active Low
	1	$V_{CC1/2}$ = 2.6V	OFF	OFF	5.1kΩ	>10MΩ	High-Z
$V_{CC} < V_{UVLO}$	X	$V_{CC1/2}$ = 2.6V	OFF	OFF	5.1kΩ	>10MΩ	High-Z

Application Information

For typical USB Type-C CC and SBU input port protection applications, only two external components are required for the KTU1101 to provide protection functions.

Input Supply and Bypass Capacitor Selection

Place a 1.0µF/10V ceramic capacitor between the VCC pin and ground. X5R or X7R dielectric ceramic capacitors are preferred for input supply bypassing applications as they maintain better capacitance value and tolerances over operating voltage and temperature ranges when compared to lower cost Y5V dielectric type ceramic capacitors.

ESD Capacitor

The high speed / high bandwidth SBU1/2 switches utilize an ESD support capacitor to meet ESD protection requirements. The ESD support capacitor should be placed between the CESD pin and ground. The SBU1/2 inputs can have as much as 35V applied during a surge event. The ESD support capacitor used for this circuit function should have a voltage rating that exceeds 35V. A 0.1µF/50V X5R or X7R dielectric ceramic capacitor is recommended for this application.

Dead Battery Detection / Operation

USB Type-C specification allows the host and peripheral device to charge internal batteries through the Type-C port receptacle. Dead battery detection is an important feature that allows a device to be charged when its internal battery supply is depleted. Another scenario for dead battery support is when the CC1/2 or SBU1/2 switches are shut down due to an OVP or other fault condition or via the $\overline{EN}$ pin. Automatic 5.1kΩ dead battery pull-down resistors on the CC1/2 inputs signal to a connected upstream USB current source PD host or wall adapter to allow charging through the USB Type-C port VBUS. When an applied adapter senses a 5.1kΩ pull down on CC1/2, 5V should be applied to the VBUS line to enable charging. For this reason, the KTU1101 contains an automatic dead battery sub-circuit -- see Figure 5. The CC1/2 pin impedance to ground is 5.1kΩ when the device is disabled ($\overline{EN}$ = 1) or when the IC is shut down by the UVLO function due to a dead battery. When the IC is enabled under regular operation conditions, the CC1/2 impedance to ground is switched to over 10MΩ to support normal CC line functions. Refer to Table 1 control logic for CC1/2 line-states versus operation conditions.

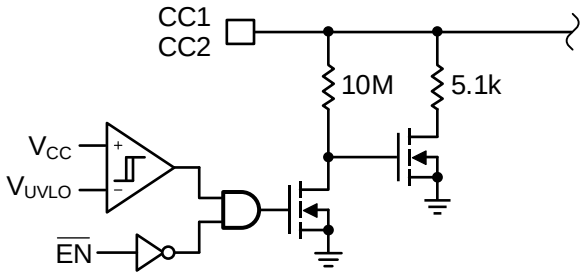


Figure 5. Simplified Schematic for Dead Battery Automatic 5.1kΩ Pull-Down Sub-Circuit

Moisture Testing

In systems that perform moisture detection on the USB port, it is typical to apply a test current through the KTU1101 and out of the connector-side pins. Moisture presents itself as a resistance path from the connector-side pins to ground. The threshold for moisture detection is usually less than 1MΩ of external leakage resistance to ground. To simplify moisture detection, the KTU1101 features over 10MΩ internal impedance from the connector-side pins to ground. However, it is important to keep in mind that KTU1101's internal impedance reduces when the voltage on the connector-side pins (CC1/2, SBU1/2) is greater than the device supply voltage (VCC). Therefore, it is important to use a weak test current for a suitably low moisture detection threshold. An alternate solution is to use a pullup resistor to a voltage source, for example, 30kΩ pull-up to 2.7V.

Fault Flag Operation

The KTU1101 fault flag will alert the system controller to an OVP, surge or IC over temperature fault. The fault flag circuit is an open-drain MOSFET output that connects the $\overline{\text{FLAG}}$ pin to ground when there is an active fault condition. Refer to the IC functional block diagram for internal fault flag circuit connections. Common system controllers can typically be configured to place a logic pull up on the fault flag input signal, in these cases the $\overline{\text{FLAG}}$ output can be connected directly to the controller I/O. If a logic pull-up termination is not available, the $\overline{\text{FLAG}}$ output may be manually pulled-up high to a logic level voltage supply through a 10kΩ or greater value resistor.

PCB Layout Guidelines

Good PCB layout is important to maintain USB CC and SBU signal integrity and optimize KTU1101 protection features. The following guidelines are recommended for best system performance:

1. Multi-layer printed circuits boards are recommended for hi-speed data communication applications. Best USB CC and SBU signal quality is realized with 4 layer or greater PCB assemblies. A multilayer board minimizes the board material thickness between the signal trace layer and adjacent ground plane layer, which aids in maintaining consistent trace impedance for high-frequency signals.
2. The KTU1101 IC package should be placed as close as possible to the USB Type-C connector to maximize ESD, surge and OVP protection for the system.
3. The use of data trace vias should be minimized or ideally avoided altogether as they introduce impedance discontinuities at high frequencies and compromise SBU signal quality.
4. If CC inputs are to be used in V_{CONN} applications, size the trace widths wide enough for the high current capacity requirements for this function. The KTU1101 is designed to support up to 1.25A through the CC1/2 switches.
5. If signal traces require turns or bends, do not use 90° turns. To maintain good high frequency performance, avoid sharp PCB trace turns, use rounded arcs or bends at 45° angles at a maximum.
6. All signal traces should be routed directly over ground planes placed on the next PCB layer. To maintain best PCB trace impedance characteristic and minimize electro-magnetic interference (EMI), the ground plane layer should have no breaks under the signal trace layer. The ground plane layer should be referenced back to the system power source ground at one single point to avoid stray current paths through the ground plane.