High Efficiency 3-CH LED Backlight Driver with Dual LCD Bias Power

Features

➢ **Backlight LED Driver**
- Wide input range: 2.9V~5.5V
- High efficiency step-up LED driver with 3-Ch current sinks, up to 32V boost voltage.
  - Up to 30mA/Ch in backlight mode
  - ±0.7% current matching at 20mA
  - ±2.2% current accuracy at 20mA
- I^2C/PWM dual dimming control scheme
  - High resolution I^2C 11-bit linear or exponential dimming
  - Wide range PWM dimming
    - 100Hz to 100kHz frequency
    - 0.2% to 100% duty cycle at 20kHz
- Programmable current sink turn on/off ramp time/shape and transition ramp up/down time
- Selectable boost switching frequency 1.0MHz or 500kHz with Auto-Frequency Mode supported
- Programmable input PWM hysteresis to minimize jitter at low PWM duty cycle
- Programmable OVP and current limitation
- LED open/short protection

➢ **LCD Panel Bias**
- Wide input range: 2.9V~5.5V
- Programmable dual Bias output regulator using a single inductor
- Programmable ramp time for OUTP and OUTN
- Charge pump PFM mode at light load
- LCD Bias efficiency up to 90%
- Wide dual output voltage range ±4.0V to ±6.3V (50mV/step) and output current up to 150mA
- I_{REG_OUT} up to 300mA at V_{REG_OUT} = 6.0 V, V_{IN} ≥ 3.0 V
- Active output discharge function
- Current limitation and short protection

➢ **Others**
- System level input UVLO
- Thermal shutdown protection
- Low shutdown current <1µA
- Flexible I^2C interface
- Pb-free Packages: WLCSP-24
- RoHS and Green compliant
- -40°C to +85°C Temperature Range

Applications

- Smartphone/Tablet Backlight

Brief Description

KTZ8863A is the ideal power solution for LED backlighting and LCD bias power of small and medium size panels. It integrates a step-up converter for LED backlighting, a step-up converter with LDO and inverting charge pump for LCD bias power, resulting in a simpler and smaller solution with fewer external components. High switching frequency allows the use of a smaller inductor and capacitor. Its input operating range is from 2.9V to 5.5V, accommodating 1-cell lithium ion batteries or 5V supply.

The LED driver's three regulated current sinks can regulate up to 30mA with its maximum boost output voltage up to 32V. 11-bit linear or exponential I_{LED} resolution can be obtained over I^2C or PWM diming. For additional flexibility, PWM dimming offers wide range frequency and duty cycle to support Content Adaptive Brightness Control (CABC).

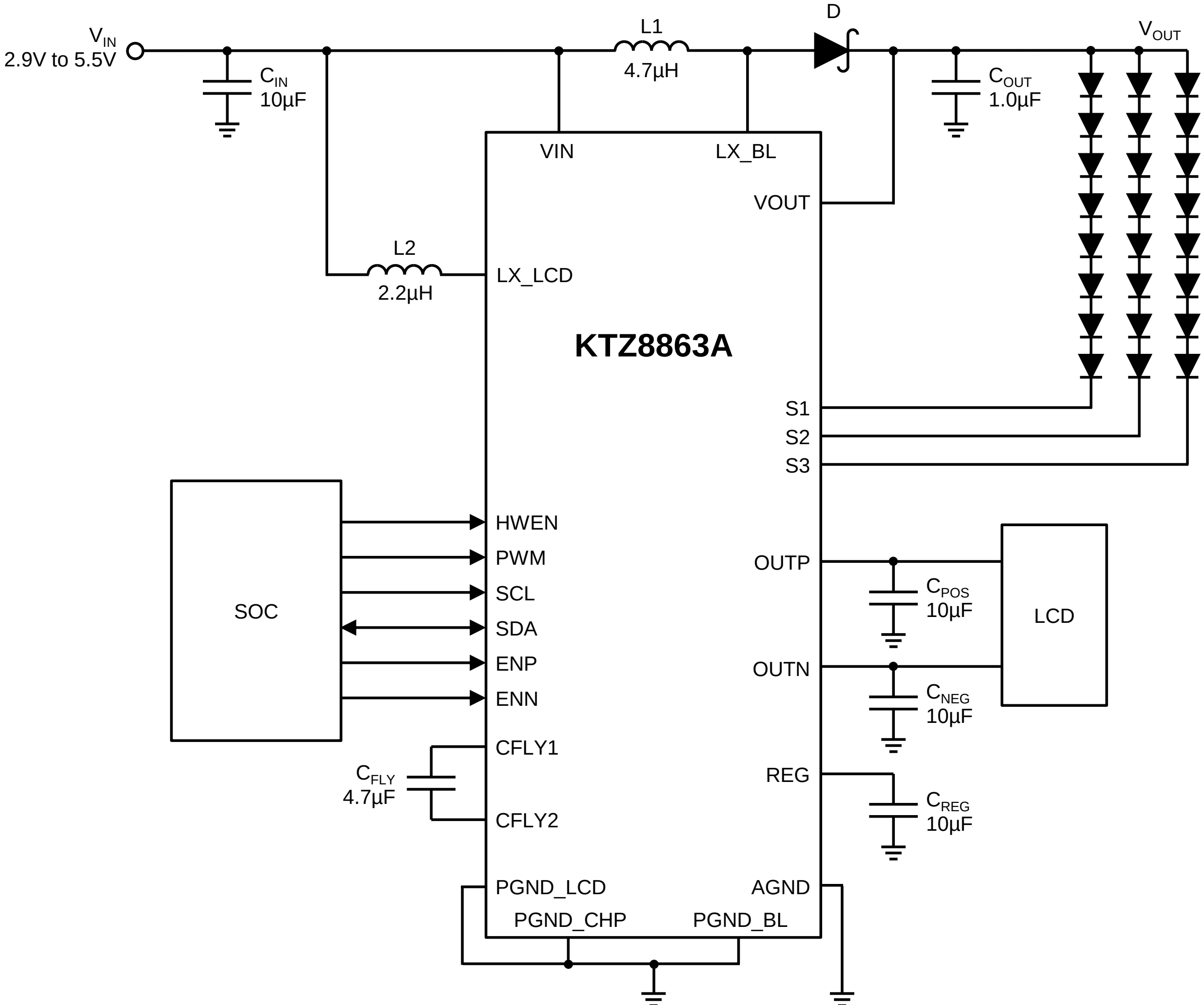
The LCD bias power section includes a step-up converter, LDO and an inverting Charge Pump to generate dual outputs OUTP and OUTN, whose voltages can be programmed via an I^2C interface. By integrating synchronous rectification MOSFETs for the step-up converter and charge pump, the KTZ8863A maximizes conversion efficiency up to 90%.

Various protection features are built into KTZ8863A, including inductor current limit protection, output short circuit protection, output over-voltage protection, LED fault (open or short) protection and thermal shutdown protection.

KTZ8863A is equipped with I^2C interface for various controls and status monitor.

KTZ8863A is available in a RoHS and Green compliant 24-ball 1.72mm x 2.45mm WLCSP.

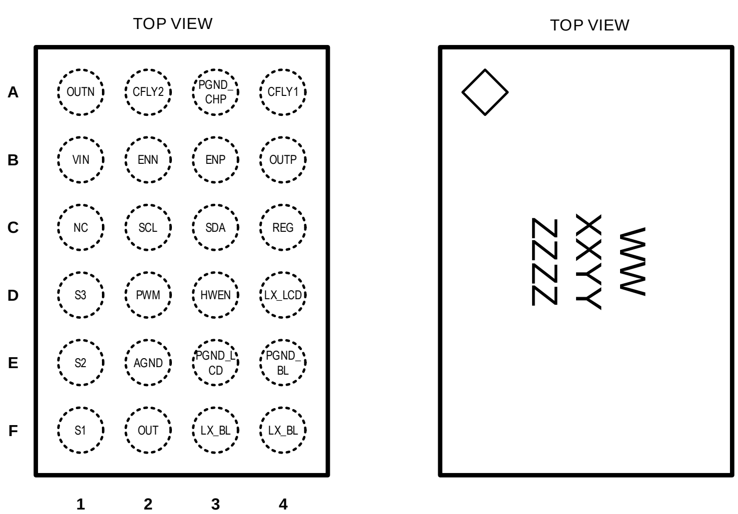
Typical Application



Pin Descriptions

Pin #	Name	Function
A1	OUTN	Charge pump output pin of the negative power. Bypass with a 10µF ceramic capacitor to PGND_CHP.
A2	CFLY2	Negative charge pump flying capacitor negative connection.
A3	PGND_CHP	Power ground for negative charge pump.
A4	CFLY1	Negative charge pump flying capacitor pin positive connection.
B1	VIN	Input supply pin for the IC, bypass with a 10µF ceramic capacitor to GND.
B2	ENN	Enable pin for negative power (OUTN), 300KΩ pull down resistor to GND
B3	ENP	Enable pin for positive power (OUTP), 300KΩ pull down resistor to GND
B4	OUTP	LDO output pin of the positive power, bypass with a 10µF ceramic capacitor.
C1	NC	No connection, leave this pin floating.
C2	SCL	Clock of the I²C interface.
C3	SDA	Bi-directional data pin of the I²C interface.
C4	REG	LCD-Bias Boost converter output pin, bypass a 10µF ceramic capacitor to PGND_LCD
D1	S3	Regulated output current sink #3.
D2	PWM	PWM dimming input pin, 300kΩ pull-down resistor at this pin to GND.
D3	HWEN	Active high hardware enable pin, 400kΩ pull-down resistor to GND.
D4	LX_LCD	Switching node of the LCD Bias boost converter.
E1	S2	Regulated output current sink #2.
E2	AGND	Analog ground pin.
E3	PGND_LCD	Power ground for LCD Bias power supply boost converter.
E4	PGND_BL	Power Ground for LED boost converter.
F1	S1	Regulated output current sink #1.
F2	VOUT	Output voltage sense pin of the step-up converter.
F3, F4	LX_BL	Switching pin of the LED step-up converter.

WLCSP46-24



24-Bump 1.72mm x 2.45mm x 0.62mm
WLCSP Package
Top Mark
WW = Device ID Code, XX = Date Code
YY = Assembly Code, ZZZZ = Serial Number

Absolute Maximum Ratings[1]

(T_A = 25°C unless otherwise noted)

Symbol	Description	Value	Units
VIN	Input Voltage	-0.3 to 6	V
LX_BL, VOUT	LED Backlight driver switching node and output node	-0.3 to 35	V
S1, S2, S3	LED Backlight driver current sink	-0.3 to 32	V
HWEN, SCL, SDA, PWM, ENP, ENN	Control Pins	-0.3 to VIN+0.3	V
LX_LCD, CFLY1, OUTP, REG	LCD Bias power positive voltage and switching node	-0.3 to 7	V
OUTN, CFLY2	LCD Bias power negative output voltage and switching node	-7 to 0.3	V
T_J	Junction Operating Temperature Range	-40 to 150	°C
T_S	Storage Temperature Range	-65 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	300	°C
ESD	HBM Electrical Static Discharge	2.0	kV

ESD Ratings

Symbol	Description	Value	Units
VESD	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000	V
	Charge device model (CDM), per JEDEC specification JESD22-C101	±500	V

Thermal Capabilities[2]

Symbol	Description	Value	Units
θ_{JA}	Thermal Resistance – Junction to Ambient	70.3	°C/W
P_D	Maximum Power Dissipation at $T_A \le 25°C$	1778	mW
$\Delta P_D/\Delta T$	Derating Factor Above T_A = 25°C	-14.22	mW/°C

Ordering Information

Part Number	Marking[3]	Operating Temperature	Package
KTZ8863AEJAA-TR	PSXXYYZZZZ	-40°C to +85°C	WLCSP-24

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
2. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.
3. "WWXXYYZZZZ" is the date code, assembly code and serial number.

Electrical Characteristics[4]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C, while *Typ* values are specified at room temperature (25°C). V_{IN} = 3.6V.

Symbol	Description	Conditions	Min	Typ	Max	Units
IC Supply						
V_{IN}	Input operating range		2.9		5.5	V
UVLO	Input under voltage lockout	Rising edge		2.45	2.65	V
$UVLO_{HYST}$	UVLO hysteresis			0.05		V
I_Q	IC standby current	HWEN = V_{IN}, LCD Boost disabled, LED Boost and Current Sink disabled.		1	7	µA
I_{LCD_EN}	Bias power no load current	LED Boost and Current Sink disabled. OUTP, OUTN enabled with no load.		1.1	1.3	mA
I_{SHDN}	IC shutdown V_{IN} current	HWEN = 0, ENP = ENN = GND		1	3	µA
Boost Converter for LED Backlight						
$R_{DS(ON)}$	NMOS on-resistance	I_{SW} = 250mA		0.2		Ω
I_{LIM}	Peak NMOS current limit	Reg 0x11[1:0]=00, T_A = 25°C	1.02	1.2	1.38	A
F_{SW}	Oscillator frequency	Reg 0x03[7]=0, T_A = 25°C	0.45	0.5	0.55	MHz
		Reg 0x03[7]=1, default, T_A = 25°C	0.9	1.0	1.1	MHz
EFF_{LEDBST}	Boost Efficiency	V_{IN} = 3.6V, I_{LED} = 5mA/ch, 3P6S LEDS, Typical application circuit.		87		%
D_{MAX}	Maximum duty cycle	FSW = 1MHz		94		%
V_{OVP}	OVP threshold	Reg 0x02[7:5]=011, T_A = 25°C	27.8	29	30.2	V
		Reg 0x02[7:5]=010, T_A = 25°C	23.9	25	26.1	V
		Reg 0x02[7:5]=001, default, T_A = 25°C	20.1	21	21.9	V
		Reg 0x02[7:5]=000, T_A = 25°C	16.2	17	17.8	V
	OVP hysteresis			2		V
Current Sink for LED Backlight						
I_{SINK_ACC}	Output current accuracy	Current setting = 30mA, T_A = 25°C	-2.0		2.0	%
		Current setting = 20mA, T_A = 25°C	-2.2		2.2	%
		Current setting = 1mA, T_A = 25°C	-3.0		3.0	%
I_{SINK_MATCH}	Output current matching[5]	Current setting = 30mA, T_A = 25°C	-0.7		0.7	%
		Current setting = 20mA, T_A = 25°C	-0.7		0.7	%
		Current setting = 1mA, T_A = 25°C	-1.5		1.5	%
V_{HR}	Current sink head room voltage			0.45		V
I_{LED_MIN}	Minimum LED current per string	Linear or Exponential mapping		60		µA
I_{STEP}	LED step size	Exponential Mode		0.3		%
		Linear Mode		14.63		µA
V_{SOV}	Current sink over voltage threshold			6		V
T_{FAULT}	Current sink fault delay			59		ms

4. KTZ8863A is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

5. The current matching among channels is defined as $|I_{SINK}-I_{AVG}|_{MAX}/I_{AVG}$.

Electrical Characteristics[4]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C, while *Typ* values are specified at room temperature (25°C). V_{IN} = 3.6V.

Symbol	Description	Conditions	Min	Typ	Max	Units
Boost Converter for LCD Power Bias						
V_{REG}	LCD boost output voltage range		4		6.6	V
	LCD boost output voltage step size			50		mv
I_{REG_LIM}	Peak current limit			1.0		A
F_{SW}	Oscillator frequency	Continuous Mode		2.0		MHz
EFF_{LCDBST}	Efficiency	VIN = 3.6 V, VREG_OUT = 5.9 V, 6mA < I_O < 160mA, Typical application circuit		90		%
R_{ON_HS}	High side FET on resistance	VIN = 3.6V		340		mΩ
R_{ON_LS}	Low side FET on resistance	VIN = 3.6V		200		mΩ
V_{REG_PP}	LCD boost output ripple	Io = 5mA and 50mA, Co = 10µF		50		mV
D_{MAX}	Maximum duty cycle		80	86		%
OUTP-Positive Output						
OUTP	Positive output voltage range		4.0		6.3	V
	Output voltage step size			50		mV
	Output voltage accuracy	V_{OUTP} = 5.5V, no load	-1.5		+1.5	%
I_{OUTP_MAX}	Maximum output current limit		150			mA
I_{OUTP_LIM}	Positive output current limit			180		mA
VOUTP_LOREG	VOUTP LDO load regulation	0 ≤ Io ≤ IOUTP_MAX		50		mV
VOUTP_DO	VOUTP LDO dropout voltage				160	mV
TOUTP_SS	Startup time	Co = 10µF, VOUTP = 5.75V, VPOS_RAMP = 2b'01		456		µs
RPD_OUTP	Output pulldown resistor in shutdown		40	70	100	Ω
OUTN-Negative Output						
OUTN	Negative output voltage range		-6.3		-4.0	V
	Output voltage step size			50		mV
	Output voltage accuracy	V_{OUTN} = -5.4V, no load	-1.5		+1.5	%
I_{OUTN_MAX}	Maximum output current limit		150			mA
EFF_{CHP}	Inverting charge pump efficiency	V_{REG} = 5.7 V, V_{OUTN} = –5.4V, I_{OUTN} > –5mA		85		%
V_{OUTN_PP}	Inverting charge pump output ripple	Io = 0mA, Co = 10µF		60		mV
T_{OUTN_SS}	Startup time	Co = 10µF, V_{OUTN} = -5.75V, VNEG_RAMP = 4b'0001		912		µs
R_{PD_OUTN}	Output pulldown resistor in shutdown			22	35	Ω

Electrical Characteristics[4]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C, while *Typ* values are specified at room temperature (25°C). V_{IN} = 3.6V.

Symbol	Description	Conditions	Min	Typ	Max	Units
PWM INPUT						
f_{PWM_INPUT}	PWM input frequency		0.1		100	kHz
t_{MIN_ON}	Minimum pulse ON time			150		ns
t_{MIN_OFF}	Minimum pulse OFF time			150		ns
PWM_{RES}	PWM input resolution	100Hz < f_{PWM} < 10KHz		11		bit
I²C-Compatible Voltage Specifications (SCL, SDA, ENP, ENN, PWM, HWEN)						
V_{IL}	Input Logic Low Threshold				0.4	V
V_{IH}	Input Logic High Threshold		1.2			V
V_{OL}	SDA Output Logic Low	I_{SDA} = 3mA			0.4	V
RPD_{HWEN}	Pulldown resistance on HWEN pin			300		KΩ
RPD_{PWM}	Pulldown resistance on PWM pin			300		KΩ
RPD_{ENP}	Pulldown resistance on ENP pin			300		KΩ
RPD_{ENN}	Pulldown resistance on ENN pin			300		KΩ
I²C-Compatible Timing Specifications (SCL, SDA), see Figure 1						
t_1	SCL clock period		2.5			µs
t_2	Data in setup time to SCL high		100			ns
t_3	Data out stable after SCL low		0			ns
t_4	SDA low setup time to SCL low (Start)		100			ns
t_5	SDA high hold time after SCL high (Stop)		100			ns
Thermal Shutdown						
T_{J-TH}	IC thermal shutdown threshold			150		°C
	IC thermal shutdown hysteresis			15		°C

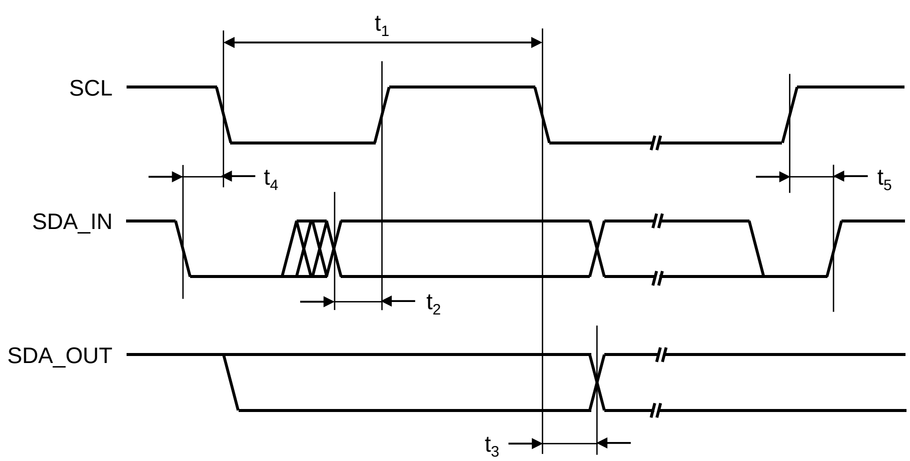


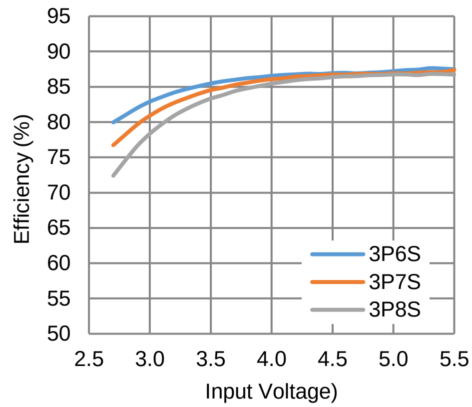
Figure 1. I²C Compatible Interface Timing

Typical Characteristics

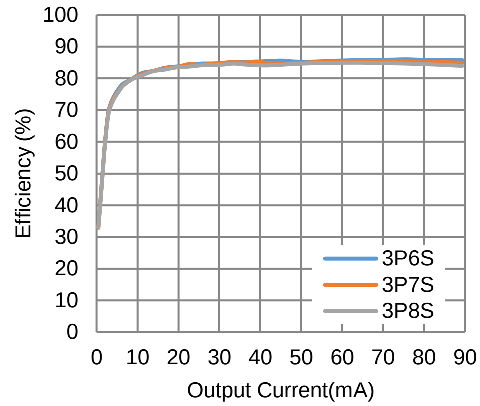
LED Backlight

V_{IN} = 3.6V, 3P7S LEDs, I_{LED} = 30mA, L = 4.7µH (TDK VLF504012MT-4R7M-CA), C_{IN} = 10µF, C_{OUT} = 1µF, I^2C register default settings, Temp = 25°C unless otherwise specified.

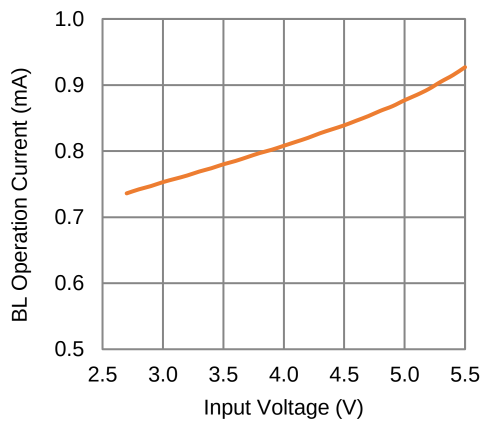
LED Driver Efficiency vs. VIN
(I_{LED} = 30mA)



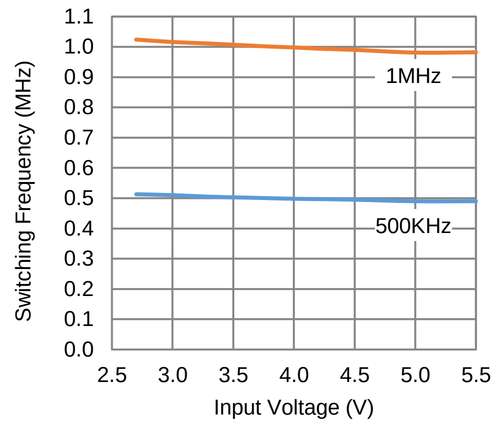
LED Driver Efficiency vs. IOUT



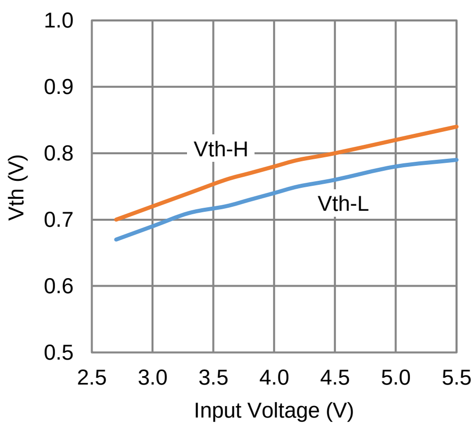
Operating Current (Switching)



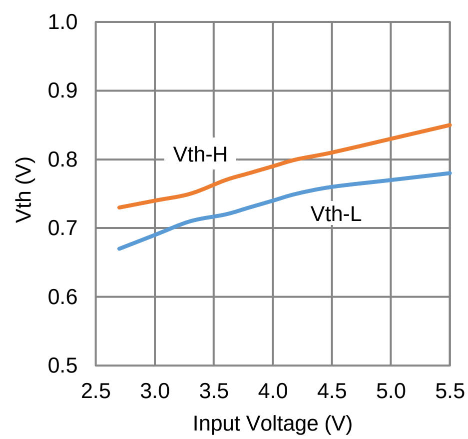
Switching Frequency vs. VIN



HWEN Logic Threshold Voltage



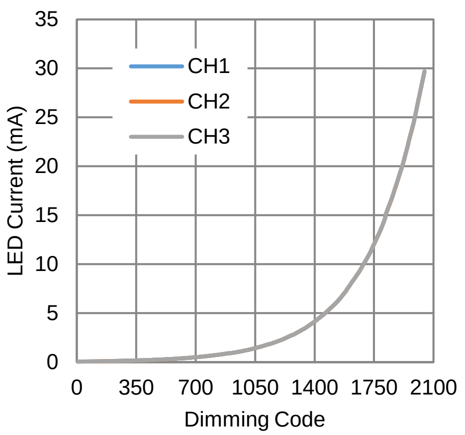
PWM Logic Threshold Voltage



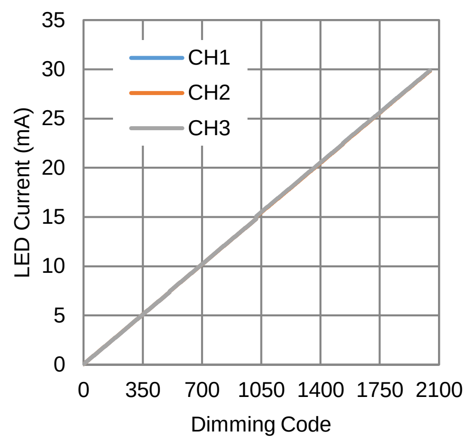
Typical Characteristics

V_{IN} = 3.6V, 3P7S LEDs, I_{LED} = 30mA, L = 4.7µH (TDK VLF504012MT-4R7M-CA), C_{IN} = 10µF, C_{OUT} = 1µF, I²C register default settings, Temp = 25°C unless otherwise specified.

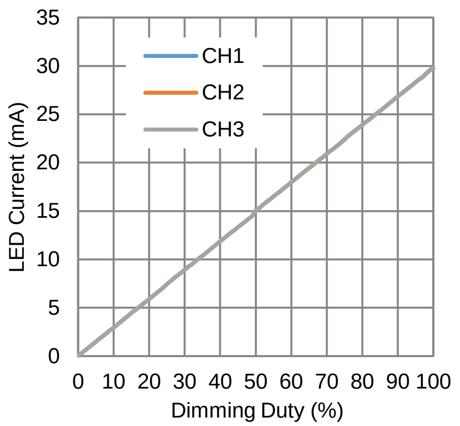
LED Current vs. Current Ratio Code
(11 bits, Exponential)



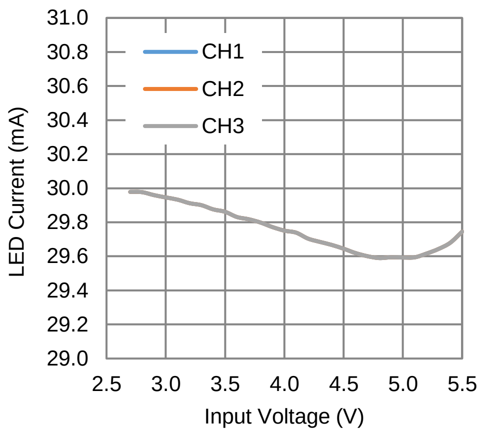
LED Current vs. Current Ratio Code
(11 bits, Linear)



LED Current vs. PWM Duty Cycle (20kHz)



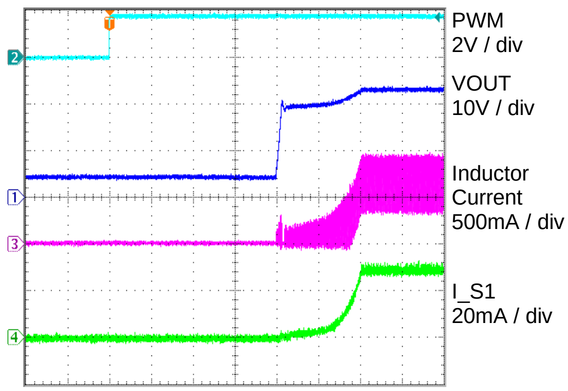
LED Current Line Regulation



Typical Characteristics

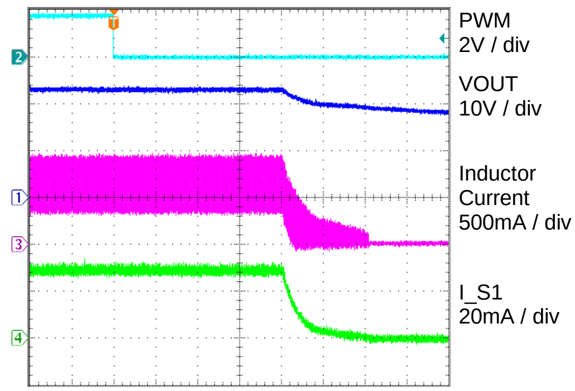
V_{IN} = 3.6V, 3P7S LEDs, I_{LED} = 30mA, L = 4.7µH (TDK VLF504012MT-4R7M-CA), C_{IN} = 10µF, C_{OUT} = 1µF, I²C register default settings, Temp = 25°C unless otherwise specified.

Turn On by PWM



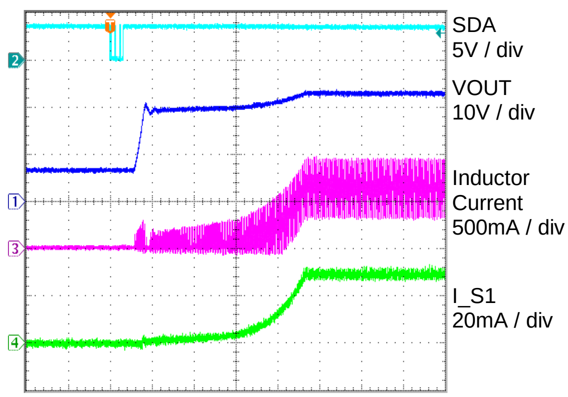
4ms / div

Turn Off by PWM



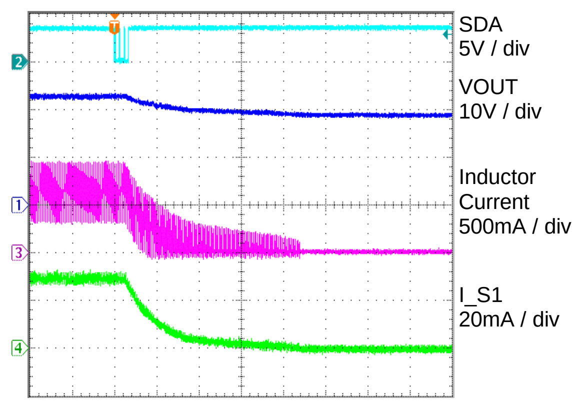
4ms / div

Turn On by I²C



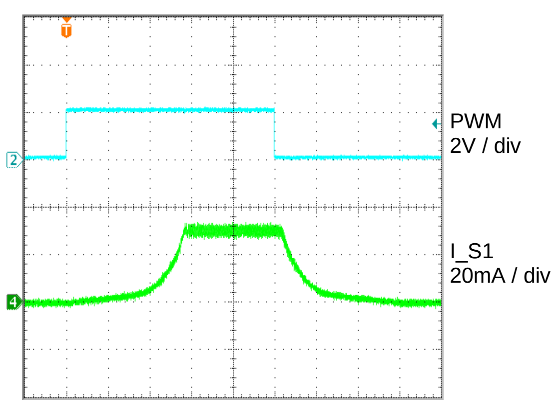
2ms / div

Turn Off by I²C



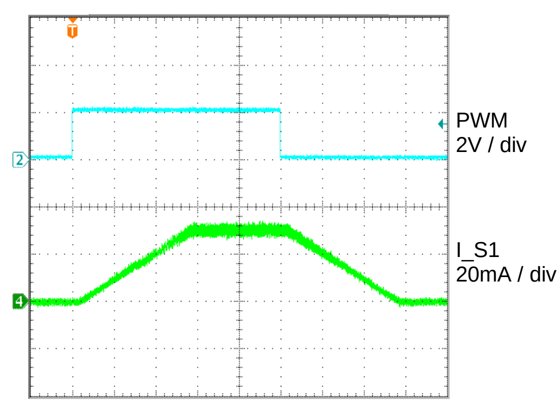
2ms / div

Ramp Up/Down Exponential (256ms)



100ms / div

Ramp Up/Down Linear (256ms)

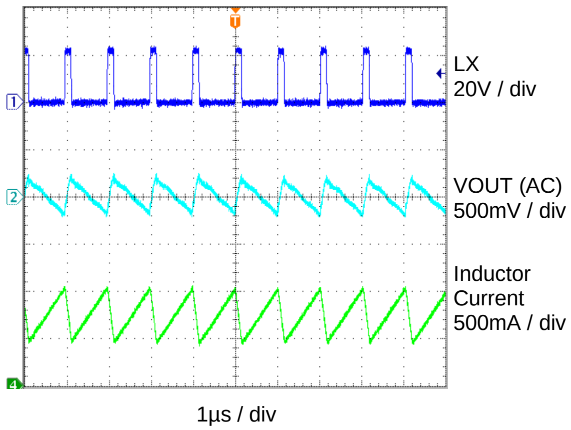


100ms / div

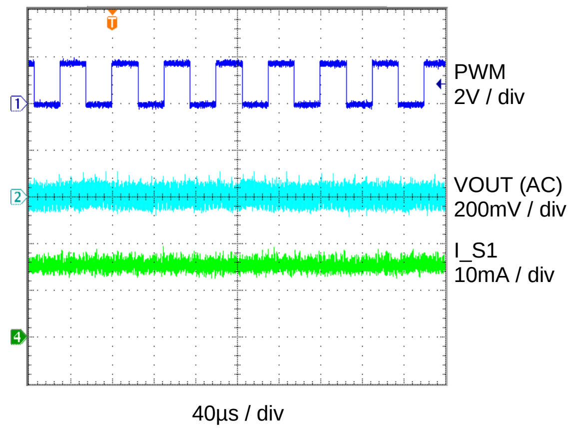
Typical Characteristics

V_{IN} = 3.6V, 3P7S LEDs, I_{LED} = 30mA, L = 4.7µH (TDK VLF504012MT-4R7M-CA), C_{IN} = 10µF, C_{OUT} = 1µF, I^2C register default settings, Temp = 25°C unless otherwise specified.

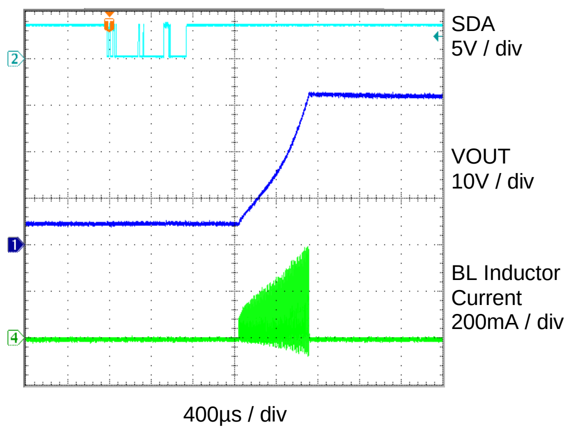
Steady State Switching



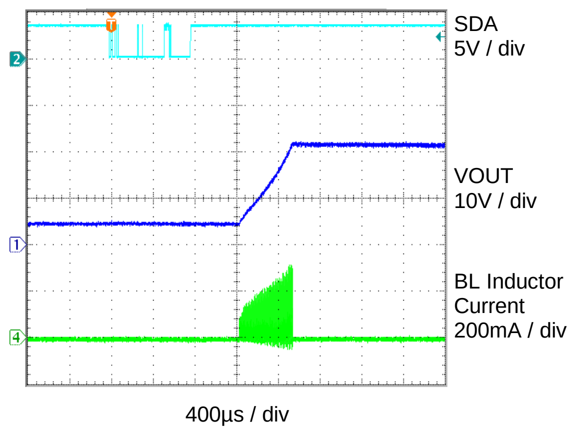
PWM Dimming (20kHz)



Turn On with LED Open (OVP = 32V)



Turn On with LED Open (OVP = 21V)

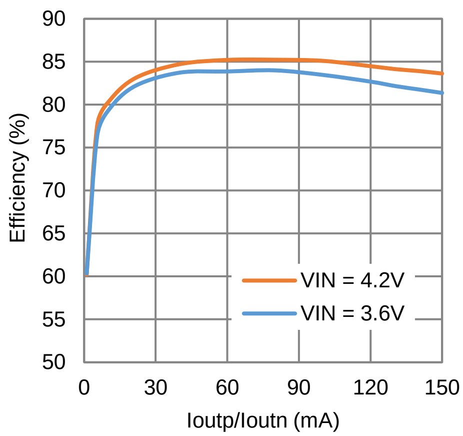


Typical Characteristics

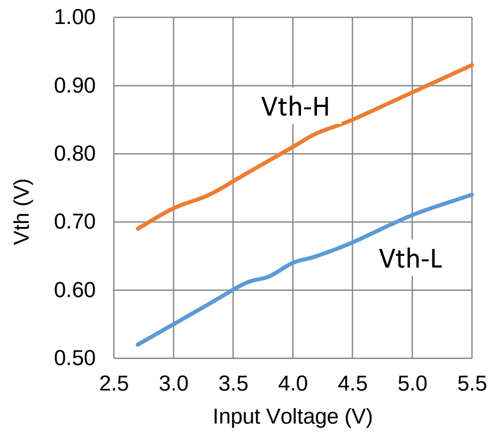
LCD Bias

V_{IN} = 3.6V, L = 2.2µH (TOKO DFE201612P-2R2M=P2), C_{IN} = C_{REG} = C_{POS} = C_{NEG} = C_{FLY} = 10µF, I_{POS} = -I_{NEG} = 40mA, T_A = 25°C, unless otherwise specified. Default setting V_{POS}/V_{NEG} = ±5.5V, V_{REG} = 5.8V.

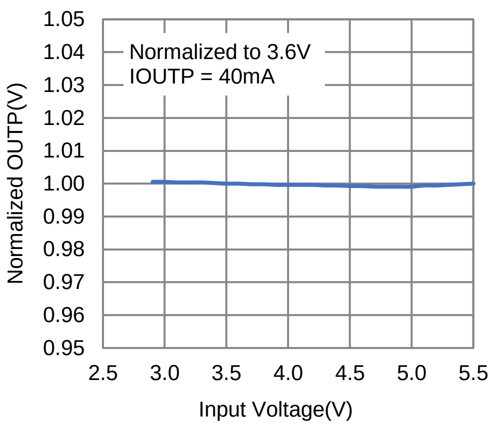
Efficiency vs. Output Current



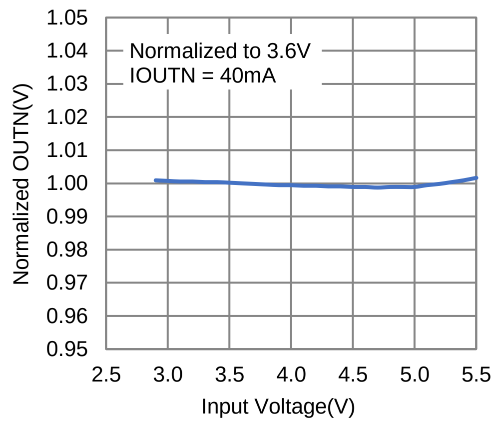
ENP/ENN Logic Threshold Voltage



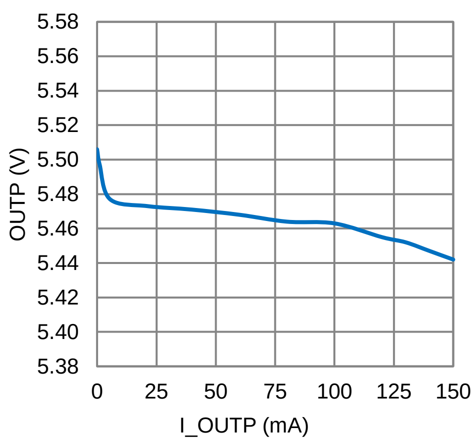
OUTP Line Regulation



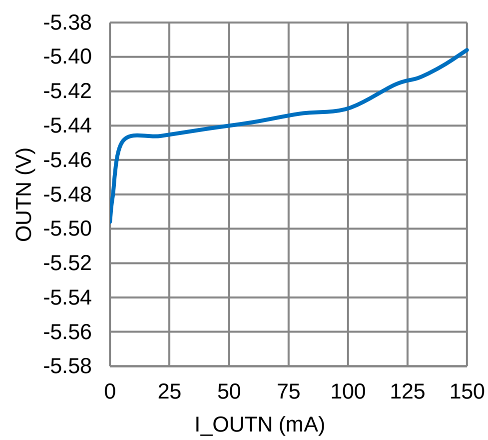
OUTN Line Regulation



OUTP Load Regulation



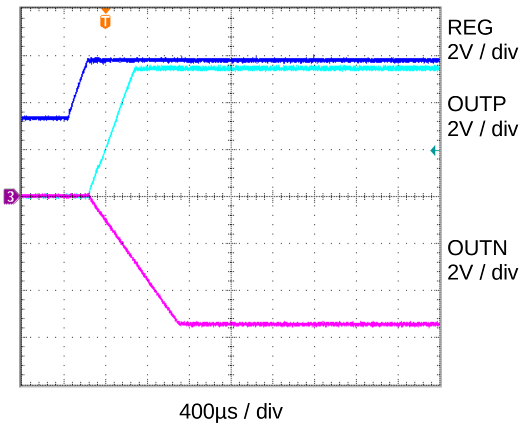
OUTN Load Regulation



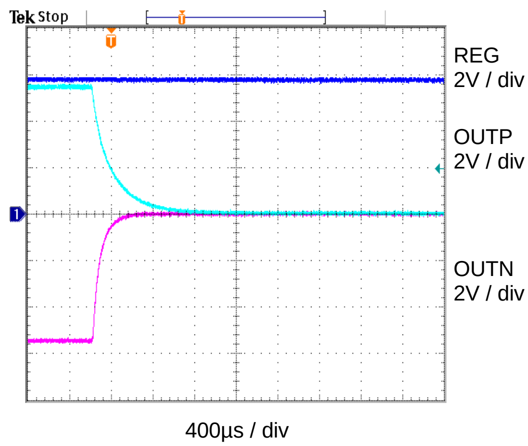
Typical Characteristics

V_{IN} = 3.6V, L = 2.2µH (TOKO DFE201612P-2R2M=P2), C_{IN} = C_{REG} = C_{POS} = C_{NEG} = C_{FLY} = 10µF, I_{POS} = -I_{NEG} = 40mA, T_A = 25°C, unless otherwise specified. Default setting V_{POS}/V_{NEG} = ±5.5V, V_{REG} = 5.8V.

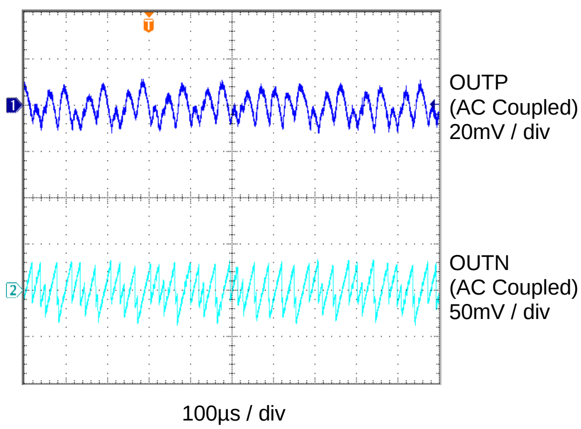
Power-up (No Load)



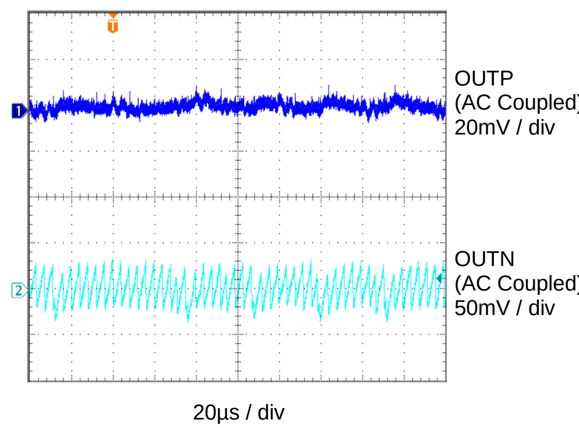
Power-down (No Load)



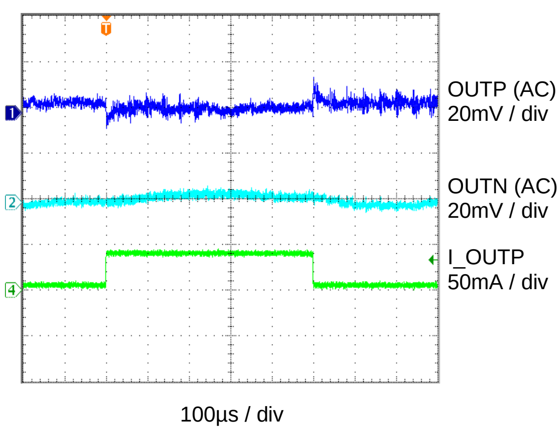
Steady-state Operation
(IPOS = -INEG = 5mA)



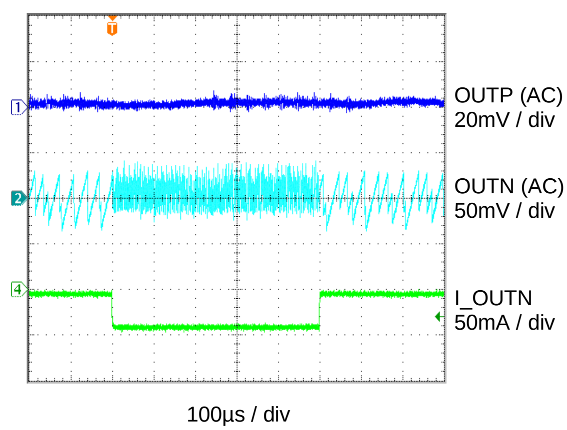
Steady-state Operation
(IPOS = -INEG = 40mA)



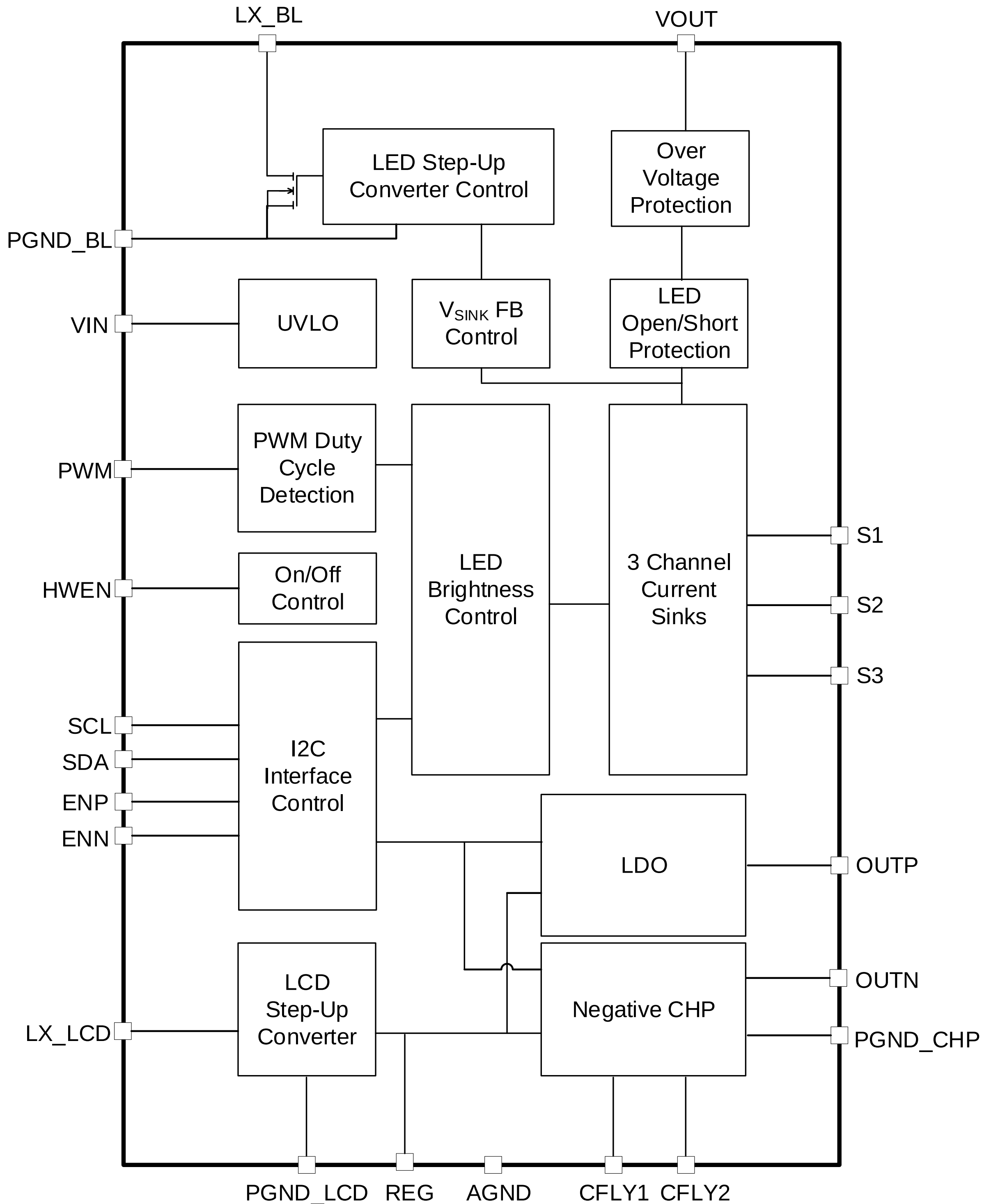
Load Transient
(5mA to 40mA Step Load) (OUTN = No Load)



Load Transient
(5mA to 40mA Step Load) (OUTP = No Load)



Functional Block Diagram



Functional Description

Overview

KTZ8863A is the ideal power solution for LED backlighting and LCD bias power of small and medium size panels. It integrates a step-up converter for LED backlighting, a step-up converter with LDO and inverting charge pump for LCD bias power, resulting in a simpler and smaller solution with fewer external components. High switching frequency allows the use of a smaller inductor and capacitor. Its operating input ranges from 2.9V to 5.5V, accommodating 1-cell lithium ion batteries or 5V supply.

The LED driver's three regulated current sinks can regulate up to 30mA in backlight mode with its maximum boost output voltage up to 32V. 11bit linear or exponential I_{LED} resolution can be obtained over I^2C or PWM diming. For additional flexibility, PWM dimming offers wide range frequency and duty cycle to support Content Adaptive Brightness Control (CABC).

The LCD bias power includes a step-up converter, LDO and an Inverting Charge Pump to generate dual outputs, OUTP and OUTN, whose voltages can be programmed via an I^2C interface. By integrating synchronous rectification MOSFETs for the step-up converter and charge pump, the KTZ8863A maximizes conversion efficiency up to 90%.

Various protection features are built into KTZ8863A, including inductor current limit protection, output short circuit protection, output over-voltage protection, LED fault (open or short) protection and thermal shutdown protection. KTZ8863A is equipped with I^2C interface for various controls and status monitor.

Hardware Enable & Standby Mode

KTZ8863A has a logic input HWEN pin to enable/disable the device. When HWEN is set low, the device goes into shutdown mode, all I^2C registers are reset to default, and the I^2C interface is disabled. Under this condition, the device does not respond to any I^2C command. Even when SCL/SDA's pull up voltage is much less than VIN voltage, it will not cause any extra leakage current.

When HWEN is set high, the device goes into standby mode, the I^2C interface is enabled, and the device can respond to I^2C command. Under this condition, if SCL/SDA's pull up voltage is much less than VIN voltage, it can cause a small leakage current from VIN. For example, if VIN = 4.2V and SCL/SDA's pull up voltage is 1.8V, there will be around 6.8µA additional leakage current from VIN in this standby mode.

Based on HWEN's connection, there are two kinds of power-up sequences as below

- If HWEN is tied to VIN, once VIN goes above around 2.0V, HWEN should stay high for at least T_{I2C_RESET} = 150µs time before any I^2C command can be accepted.
- If HWEN is driven by a GPIO, once HWEN goes from low to high, HWEN should stay high for at least T_{I2C_RESET} = 150µs time before receiving any I^2C command.

Either HWEN input or I^2C command can be used to turn off the part, but there are some differences.

- If setting HWEN input low to turn off the part, the I_{LED} will be turned off immediately without any ramp down control. After that, the I^2C interface is disabled.
- If using an I^2C command to turn off backlight while keeping HWEN high, the I_{LED} will have ramp down control. After the LED current ramp down is finished, the I^2C interface is still alive waiting for new command.

Backlight Boost

A step-up converter is used to generate high voltage for driving LED string. An adaptive control method automatically adjusts output voltage by monitoring the headroom voltage of current sinks. In this way, KTZ8863A can offer much better efficiency. KTZ8863A Backlight Boost has three switching frequency 1.0MHz, 500kHz, and 250kHz, selected by setting register 0x03 bit [7] in combination with auto-frequency register 0x06 and 0x07.

Backlight Current Sink Setting

Each current sink can be enabled or disabled by register 0x08 bits [2:0]. They can be enabled by writing the backlight enable bit to HIGH in register 0x08 bit [4] after correctly setting of LED configuration and brightness. If certain current is not used, connect its output to GND. During the startup, KTZ8863A will automatically detect and disable the corresponding channel.

When PWM dimming is enabled and a non-zero PWM duty cycle is detected, the KTZ8863A multiplies the duty cycle with I²C brightness settings. Figure 2 and Figure 3 describe the start-up timing for operation with I²C controlled current and with PWM controlled current.

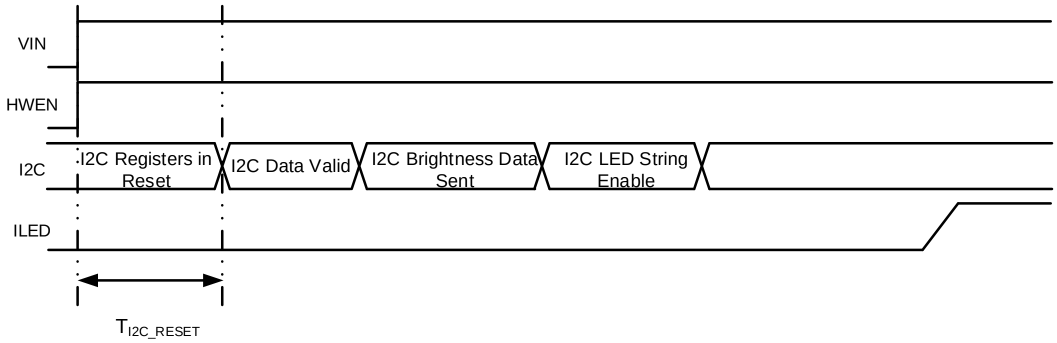


Figure 2. Enable of KTZ8863A via I²C

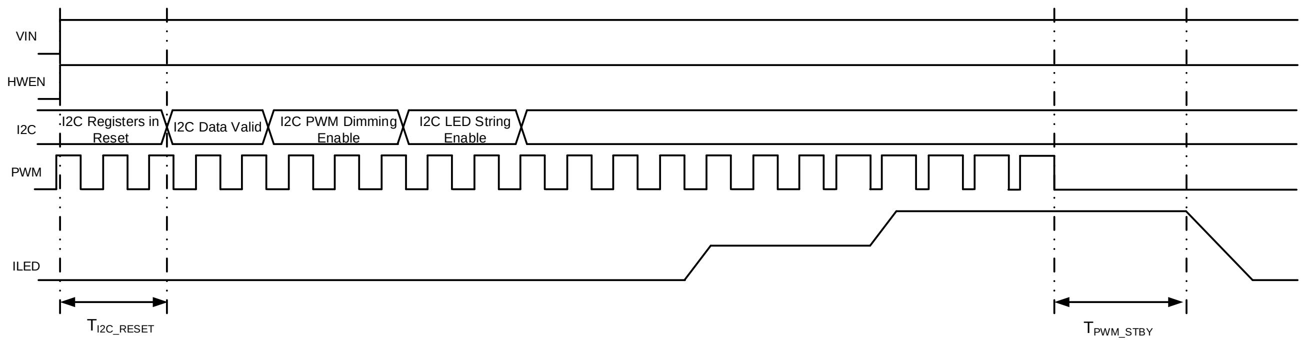


Figure 3. Enable of KTZ8863A via PWM

Operating Mode Description

The KTZ8863A backlight can operate in different mode, see Table 1 as below

Table 1. Backlight Operating Modes

HWEN	BL_EN 0x08[4]	PWM INPUT	I2C BRIGHTNESS 0X05[7:0] 0X04[2:0]	CURRENT SINKs ENABLEs 0x08[2:0]	PWM_EN 0x02[0]	FEEDBACK DISABLEs 0x10[5:3]	MAPPING MODE 0x02[3]	ACTION
0	X	X	X	X	X	X	X	Shutdown
1	0	X	X	X	X	X	X	Standby[6]
1	1	X	0x000	000	X	X	X	Standby[6]
1	1	X	≥0x001	≥001	0	<111	0 = Exp. Mode 1 = Lin. Mode	-Backlight boost enabled -Selected current sink(s) enabled -I²C control only
1	1	Duty = 0	X	≥001	1	<111	X	Standby[6]
1	1	Duty > 0	≥0x001	≥001	1	<111	0 = Exp. Mode 1 = Lin. Mode	-Backlight boost enabled -Selected current sink(s) enabled -I²C × PWM
1	1	Duty > 0	≥0x001	≥001	1	111	0 = Exp. Mode 1 = Lin. Mode	-Backlight boost disabled -Selected current sink(s) enabled -I²C × PWM

6. Standby implies the backlight boost and current sinks are shut down. Register writes are still possible. Shutdown implies that the device is in reset and no I2C communication is possible.

Backlight LED Current

The LED current is always a DC current (not PWM). It can be programmed for either exponential mapping mode or linear mapping mode by Register 0x02 bit [3]. These two modes determine the transfer characteristic of dimming code to LED current. It also has 11-bit control, including the 8-bit MSBs from register 0x05 bits [7:0] and the 3-bit LSBs from register 0x04 bits [2:0]. If only 8-bit dimming is needed, the 3-bit LSBs should be kept as '111' while the 8-bit MSBs are programmed. If 11-bit dimming ratio is needed, the 3-bit LSBs should be programmed first, then the 8-bit MSBs are programmed. Only programming the 3-bit LSBs doesn't change the current ratio until the 8-bit MSBs are programmed.

In linear mapping 8-bit dimming mode, the LED current per channel can be calculated as:

$$I_{LED\_BL} = I_{LED\_FS} * D_{PWM} * \left(\frac{3}{2050} + \frac{Code * 8 + 7}{2050}\right), \qquad (Code = 0\sim255)$$

where I_{LED_FS} is the backlight full-scale LED current which is programmed by 0x15 bits [7:3], ranges from 5.2mA to 30mA with 0.8mA step, D_{PWM} is the input PWM duty cycle if PWM dimming is enabled, otherwise $D_{PWM} = 1$.

In linear mapping 11-bit dimming mode, the LED current per channel can be calculated as:

$$I_{LED\_BL} = I_{LED\_FS} * D_{PWM} * \left(\frac{3}{2050} + \frac{Code}{2050}\right), \qquad (Code = 1\sim2047)$$

For linear mapping 11-bit dimming's Code 0, current sink and boost converter will be disabled, LED will be turned off.

In exponential mapping 8-bit dimming mode, the LED current per channel can be calculated as:

$$I_{LED\_BL} = I_{LED\_FS} * D_{PWM} * \frac{1.003040572^{(Code*8+7)}}{500} \quad (Code = 0\sim255)$$

In exponential mapping 11-bit dimming mode, the LED current per channel can be calculated as:

$$I_{LED\_BL} = I_{LED\_FS} * D_{PWM} * \frac{1.003040572^{Code}}{500} \quad (Code = 1\sim2047)$$

For exponential mapping 11-bit dimming's Code 0, current sink and boost converter will be disabled, LED will be turned off.

Backlight Brightness Control Mode

KTZ8863A has two brightness control mode, I^2C Only Mode and I^2C x PWM Mode, see Figure 4. In I^2C Only Mode, register 0x02's bit [0] PWM_ENABLE should be set to "0", the LED brightness is controlled by registers 0x04 and 0x05. In I^2C x PWM Mode, register 0x02's bit [0] PWM_ENABLE should be set to "1", the LED brightness will be controlled by I^2C code and PWM duty together.

If the LED current is changed from one value to the other by I^2C dimming Register 0x04 and Register 0x05, the ramp time can help LED current transit smoothly from one brightness level to next one. Ramp time can be adjusted from 1µs to 640ms via 0x03's bits [6:3]. Ramp time applies both to ramp up and ramp down, it remains same regardless the amount of change in brightness.

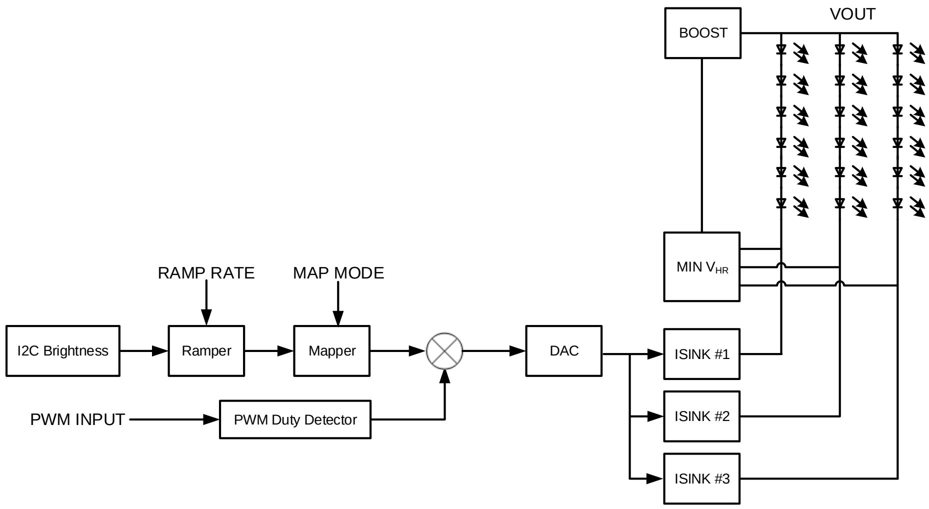


Figure 4. I²C and PWM Dimming Scheme

Backlight PWM Dimming

In backlight I²C x PWM Mode, the input PWM duty cycle is converted internally to produce a DC output sink current (not pulsing). When PWM is enabled, it can be programmed as either active high or active low by register 0x02's bit [2], with active high as default. When PWM dimming is enabled, KTZ8863A uses internal 20MHz sampling clock to detect the PWM duty cycle. It is recommended to have the minimum PWM on time as 0.1µs. For the example of 20kHz dimming frequency, the PWM duty cycle range can be 0.2%~100%. The PWM dimming frequency range can be as wide as 100Hz to 100kHz.

PWM Dimming Step Response and Timeout

If the LED current is changed from one value to the other by PWM dimming duty cycle, the transition ramp up/down time can be programmed by Register 0x15 bits [2:0]. For this transition ramp, its slope is fixed, so the final transition ramp time is dependent on the change amount of the PWM duty cycle.

The KTZ8863A PWM timeout feature turns off the boost output when the PWM is enabled and there is no PWM pulse detected.

PWM to Digital Code Readback

In PWM x I²C control mode, registers 0x12 and 0x13 contain the PWM duty cycle to the 11-bit code conversion information. Register 0x12 contains the 8 LSBs of the brightness code and register 0x13 the 3 MSBs. They are suggested to be read out in successive way to make sure the PWM duty result is correct. Too long delay between reading them may cause incorrect returned result, since input PWM duty may change during the delay time. To translate this reading to the actual LED current setting of the KTZ8863A, convert it to the corresponding duty cycle and multiply it by the brightness level setting in the brightness registers (0x04 and 0x05).

Backlight PWM Hysteresis

In backlight mode, if PWM dimming frequency is high and PWM dimming duty cycle is low, even the internal fast 20MHz sampling clock's sampling error can be sufficient to cause the output LED current jitter. KTZ8863A implements PWM hysteresis control to minimize the jitter. It can be programmed by register 0x03 bits [2:0]. The input PWM duty cycle is converted to an internal 11-bit digital value, this PWM hysteresis decides how many LSBs of this 11-bit digital value is changed before the output LED current can follow the change. When PWM duty cycle changes in the same direction, no hysteresis exists. Only when the PWM duty cycle's change starts to go in different direction, does the hysteresis starts to take effect, and only when the change is larger or equal to the number of LSBs programmed, the output LED current starts to follow the change. Table 2 shows the relationship between the minimum LSB(s) and the PWM duty cycle hysteresis. Table 3 summarizes register 0x03 bits [2:0]'s minimum setting to prevent jitter under different input PWM frequency conditions. The drawback of setting PWM hysteresis too high is that the output current becomes less accurate due to the hysteresis.

Table 2. PWM Hysteresis

PWM Register 0x03 Bits [2:0]	Minimum LSB(s)	PWM Duty Cycle Hysteresis
000	0	0/2047 = 0%
001	2	2/2047 = 0.10%
010	4	4/2047 = 0.20%
011	6	6/2047 = 0.29%
100	8	8/2047 = 0.39%
101	10	10/2047 = 0.48%
110	12	12/2047 = 0.59%
111	14	14/2047 = 0.68%

Table 3. Register 0x03 Bits [2:0]'s Minimum Setting

PWM Dimming Frequency (kHz)	Sampling Error	Register 0x03 Bits [1:0]'s Minimum Setting to Prevent Jitter
0.1	0.0005%	001
1	0.005%	001
5	0.025%	001
10	0.05%	001
20	0.1%	010
40	0.2%	011
100	0.5%	110

Turn On/Off Ramp

When backlight mode is enabled from standby mode or disabled to standby mode, the LED current waveform's turn on/off time is controlled by Turn On/Off Ramp Register 0x14 bits [7:4] and bits [3:0] respectively. The 16 options range from 512µs to 16384ms, with 8ms as default. The shape of the turn on/off ramp in backlight mode can also be programmed as exponential or linear through the Register 0x8 bit [5], with exponential as default.

Auto Frequency Mode

KTZ8863A can automatically adjust the backlight boost switching frequency based on the programmed LED current for optimizing the conversion efficiency. Auto-Frequency Mode is configured by AUTOF_LOW 0x06 and AUTOF_HIGH 0x07. 0x06 sets the low threshold between 250KHz and 500KHz, while 0x07 sets the high threshold between 500KHz and 1MHz. Both 0x06 and 0x07 take an 8-bit code which is compared against the 8 MSB of the brightness register 0x05. For 250kHz, it can only access by auto frequency mode and max duty ratio is 50%. Table 4 details the boundaries for this mode.

Table 4. Auto Switching Frequency Operation

Brightness Code MSBs (Register 0x05[7:0])	Boost Switching Frequency
≤ Auto Frequency Low Threshold (register 0x06)	250KHz
> Auto Frequency Low Threshold (register 0x06) & ≤ Auto Frequency High Threshold (register 0x07)	500KHz
> Auto Frequency High Threshold (register 0x07)	1MHz

By writing any non-zero code into 0x06 or 0x07 will enable Auto-Frequency Mode. Writing "0" into both 0x06 and 0x07 will disable Auto-Frequency Mode, the switching frequency will follow register 0x03 bit [7]) across the entire LED current range. Table 5 provides a guideline for selecting the auto frequency high/low threshold at V_{IN} = 3.7V. The actual setting must be verified in the application and optimized for the desired input voltage.

Table 5. Auto Frequency Threshold Setting Example

Condition (Vf = 3.3V@I_{LED} = 30mA)	Inductor (µH)	Recommend Auto Frequency High Threshold	Recommend Auto Frequency Low Threshold
2 × 4 LEDs	10	0x65 (12mA)	0x43 (8mA)
2 × 5 LEDs	10	0x5C (11mA)	0x42 (7.9mA)
2 × 6 LEDs	10	0x54 (10mA)	0x3F (7.5mA)
2 × 7 LEDs	10	0x4F (9.4mA)	0x36 (6.5mA)
2 × 8 LEDs	10	0x65 (12mA)	0x3F (7.5mA)
3 × 4 LEDs	10	0x4C (9mA)	0x2A (5.1mA)
3 × 5 LEDs	10	0x43 (8mA)	0x28 (4.8mA)
3 × 6 LEDs	10	0x3B (7mA)	0x27 (4.7mA)
3 × 7 LEDs	10	0x35 (6.4mA)	0x26 (4.6mA)
3 × 8 LEDs	10	0x43 (8mA)	0x25 (4.5mA)

LED Fault Protection

Each current sink is protected against LED short or open conditions. The outcome of LED short event depends on the setting of LED_SHORT_MODE bit in register 0x10. If it is '1' and LED short circuit condition arises, the current sink continues to regulate until V_{SINK} > V_{SOV}. When any sink node voltage goes above V_{SOV} (6V) for more than 59ms (typ.), LED_SHORT flag will be set in 0x0F and that channel's current sink will be turned off, and the other channel(s) will continue to work if they don't trigger this fault condition. If it is '0', the LED_SHORT flag will be set in 0x0F when V_{SINK} > V_{SOV} more than 59ms(typ.) is detected, but KTZ8863A will keep working as usual without turning off the shorted channel's current sink until it reaches thermal shutdown.

In case of an LED failing open, the current sink voltage of the failed string will go close to ground and dominate the boost converter control loop. As a result, the output voltage will increase until it reaches the over-voltage threshold set by register 0x02. Once an OVP event has been detected, the boost will stop switching and the BL_OVP flag will be set in register 0x0F. The outcome of OVP event depends on the setting of OVP_MODE bit in register 0x02. If OVP_MODE is set to 0, the LED open channel will not be disabled, as soon as V_{BL_OUT} falls below the backlight OVP threshold, the KTZ8863A begins switching again, so that V_{BL_OUT} will be kept close to OVP threshold. Once the opened channel resumes to connected later, its LED current will resume and V_{BL_OUT} will go back to normal level. If OVP_MODE is set to 1, once the over-voltage incident is triggered, the BL_OVP flag is set in register 0x0F. Any of the enabled current sink headroom voltage drops below 150mV will be disabled. Then the output voltage of the boost converter will go back to normal level. During the entire process, the rest of the LED string (healthy LED string) would continue in normal operation. Even if the opened channel is reconnected later, its LED current will not resume until toggling HWEN or sending software reset command or resetting backlight mode.

In case where all LED channels are open, once the output voltage of the boost converter reaches the over-voltage threshold, all the current sinks will be disabled internally and the boost converter will stop switching. User needs to restart the IC by toggling HWEN or sending software reset command or resetting backlight mode.

Backlight Over Current Protection

The KTZ8863A has 4 different OCP thresholds (1200mA, 1500mA, 1800mA, and 2100mA) chosen by register 0x11 bits [1:0]. It is a cycle-by-cycle current limit by detecting low side power FET current. Once the threshold is trigged, the low side power FET will be turned off immediately for the rest of the switching cycle time. If enough overcurrent threshold events occur, the BL_OCP Flag (register 0x0F, bit [0]) will be set.

LCD Bias Boost Converter

REG pin is the output of a high efficiency boost which is used to generate OUTP and OUTN power rails. REG boost ranges from 4V to 6.6V with 50mV step size. OUTP is generated by an LDO whose input is REG pin. OUTP ranges from 4V to 6.3V with 50mV step size and supports up to 150mA output current. OUTN is generated by an inverting Charge Pump whose input is REG pin. OUTN ranges from -6.3V to -4V with 50mV step size and support up to 150mA output current. Refer 0x0C, 0x0D, 0x0E for the settings of REG, OUTP and OUTN.

For proper operation, REG voltage is suggested to be $REG = MAX(OUTP, |OUTN|) + V_{HR}$, where $V_{HR} \geq 200mV$ for lower currents and $V_{HR} \geq 300mV$ for higher currents.

OUTP and OUTN voltage settings can be changed while they are enabled, but user must re-write 0x09 to get new settings taking effect. The REG voltage changes immediately upon a register write. The LCD Bias outputs can be turned on/off either by ENP and ENN pins or by 0x09 register bits [2:1]. EXT_EN bit in 0x09 is used to select on/off is controlled by external pins or internal register bits. Refer to Table 6 for detail information.

Table 6. LCD Bias Power Operating Mode

HWEN	ENN	ENP	LCD_EN_MODE 0x09[7]	OUTP_EN 0x09[2]	OUTN_EN 0x09[1]	EXT_EN 0x09[0]	ACTION
0	X	X	X	X	X	X	Device shutdown
1	0	0	0	X	X	1	Standby[7]
1	X	X	1	0	0	0	Standby[7]
1	0	1	1	X	X	1	VPOS enabled via external input
1	1	0	1	X	X	1	VNEG enabled via external input
1	1	1	1	X	X	1	VPOS and VNEG enabled via external Input
1	X	X	1	1	0	0	VPOS enabled via I²C
1	X	X	1	0	1	0	VNEG enabled via I²C
1	X	X	1	1	1	0	VPOS and VNEG enabled via I²C

Fast Discharge

KTZ8863A has internal switch resistance for discharging OUTP and OUTN when device is shutdown. The OUTP discharge function is enabled with register 0x09 bit [4] and the OUTN discharge is enabled with register 0x09 bit [3].

OUTP Short Circuit Protection

If output current of OUTP is bigger than 180mA (typical), the OUTP_SHORT flag will be set in register 0x0F. A I²C readback is required to clear the flag. The outcome of an OUTP_SHORT detection depends on the setting of register 0x0A bits [7:6], including report-only flag, shutdown OUTP/OUTN, and shutdown OUTP/OUTN and backlight. KTZ8863A provides four level short circuit detection filter: 100µs, 500µs, 1ms, and 2ms by register 0x0B bits [3:2] to avoid false trigger problems.

OUTN Short Circuit Protection

OUTN_SHORT flag will be set in register 0x0F if OUTN is found shorted to ground. A I²C readback of register 0x0F is required to clear the flag. The outcome of an OUTN_SHORT detection depends on the setting of register 0x0A bits [7:6], including report-only flag, shutdown OUTP/OUTN, and shutdown OUTP/OUTN and backlight. KTZ8863A provides four level short circuit detection filter options: 100µs, 500µs, 1ms, and 2ms by register 0x0B bits [1:0] to avoid false trigger problems.

Soft Reset

All the I²C registers can be reset to their default settings by writing ‘1’ to the SOFTWARE_RESET bit in Register 0x08, this bit will be reset to ‘0’ automatically after the software reset.

UVLO

Under voltage lock-out (UVLO) featured is included to monitor the input voltage VIN. Once VIN drops below UVLO falling threshold, the current sinks are disabled and the boost converters stop switching. After VIN increases above UVLO rising threshold, the boost converters and the current sinks will resume to their previous setting.

7. Standby implies that OUTP and OUTN are either high impedance or being internally pulled low via the active pulldown, and that the LCD boost is off. Shutdown implies that the device is in reset and no I²C communication is possible.

Thermal Shutdown

The KTZ8863A has Thermal Shutdown Protection which will turn off the backlight boost, all current sinks, LCD bias boost, inverting charge pump, and the LDO when the die temperature reaches or exceeds 150°C (typ). The I^2C access is still available during Thermal Shutdown event, but TSD flag will be set in register 0x0F, this bit is real time reflection of TSD. When TSD is gone, the bit will be reset back to 0 automatically.

Device Functional Modes

Shutdown: The KTZ8863A is in shutdown when the HWEN pin is low.

Standby: After the HWEN pin is set high the KTZ8863A goes into standby mode. In standby mode, I^2C writes are allowed but references, bias currents, the oscillator, LCD powers, and backlight are all disabled to keep the quiescent supply current low.

Normal mode: Both main blocks of the KTZ8863A are independently controlled. For enabling each of the blocks in all available modes.

Application Information

I²C Serial Data Bus

KTZ8863A supports the I²C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the bus is called a master, whereas the devices controlled by the master are known as slaves. A master device must generate the serial clock (SCL), control bus access and generate START and STOP conditions to control the bus. KTZ8863A operates as a slave on the I²C bus. Within the bus specifications a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. KTZ8863A works in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined in Figure 5:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy

Both data and clock lines remain HIGH.

Start Data Transfer

A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop Data Transfer

A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data Valid

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Setup and hold times must also be taken into account.

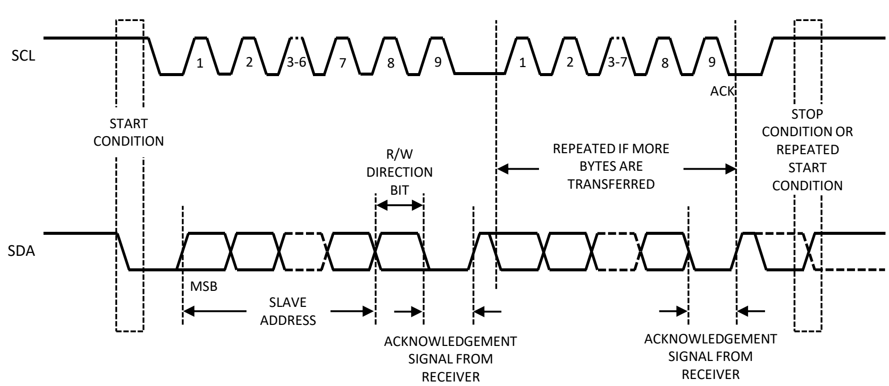


Figure 5. Data Transfer on I²C Serial Bus

KTZ8863A 7-bit slave device address is 0010001 binary (0x11h).

There are two kinds of I²C data transfer cycles: write cycle and read cycle.

I²C Write Cycle

For I²C write cycle, data is transferred from a master to a slave. The first byte transmitted is the 7-bit slave address plus one bit of ‘0’ for write. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first. Figure 6 shows the sequence of the I²C write cycle.

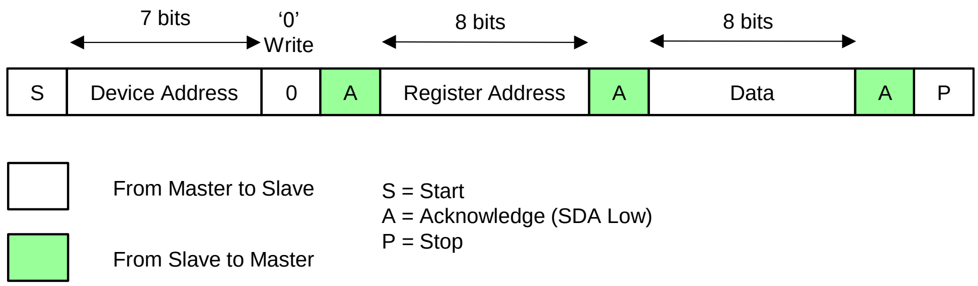


Figure 6. I²C Write Cycle

I²C Write Cycle Steps:

- Master generates start condition.
- Master sends 7-bit slave address (0010001 for KTZ8863A) and 1-bit data direction ‘0’ for write.
- Slave sends acknowledge if the slave address is matched.
- Master sends 8-bit register address.
- Slave sends acknowledge.
- Master sends 8-bit data for that addressed register.
- Slave sends acknowledge.
- If master sends more data bytes, the register address will be incremented by one after each acknowledge.
- Master generate stop condition to finish the write cycle.

I²C Read Cycle

For I²C read cycle, data is transferred from a slave to a master. But to start the read cycle, master needs to write the register address first to define which register data to read. Figure 7 shows the steps of the I²C read cycle.

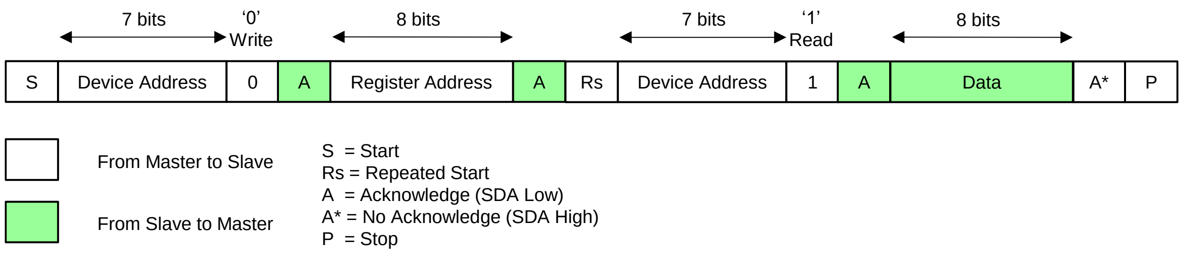


Figure 7. I²C Read Cycle

I²C Read Cycle Steps:

- Master generates start condition.
- Master sends 7-bit slave address (0010001 for KTZ8863A) and 1-bit data direction ‘0’ for write.
- Slave sends acknowledge if the slave address is matched.
- Master sends 8-bit register address.
- Slave sends acknowledge.
- Master generates repeated start condition.
- Master sends 7-bit slave address (0010001 for KTZ8863A) and 1-bit data direction ‘1’ for read.
- Slave sends acknowledge if the slave address is matched.
- Slave sends the data byte of that addressed register.
- If master sends acknowledge, the register address will be incremented by one after each acknowledge and the slave will continue to send the data for the updated addressed register.

- If master sends no acknowledge, the slave will stop sending the data.
- Master generate stop condition to finish the read cycle.

I²C Register Map

Table 7 summarizes KTZ8863A's 21 I²C registers, their read/write settings and default values. They can be reset to default values by VIN power on reset, toggling HWEN or I²C software reset.

Table 7. I²C Register Map

Register Name	Address (Hex)	R/W	Default Value
REV	0x01	R	xxxxxx10
BL_CFG1	0x02	R/W	0x28
BL_CFG2	0x03	R/W	0x8D
BL_BRT_LSB	0x04	R/W	0x07
BL_BRT_MSB	0x05	R/W	0xFF
BL_AUTOF_LOW	0x06	R/W	0x00
BL_AUTOF_HIGH	0x07	R/W	0x00
BL_EN	0x08	R/W	0x00
LCD_BIAS_CFG1	0x09	R/W	0x18
LCD_BIAS_CFG2	0x0A	R	0x11
LCD_BIAS_CFG3	0x0B	R/W	0x00
LCD_BOOST_CFG	0x0C	R/W	0x28
OUTP_CFG	0x0D	R/W	0x1E
OUTN_CFG	0x0E	R/W	0x1C
FLAG	0x0F	R	0x00
BL_OPTION1	0x10	R/W	0x06
BL_OPTION2	0x11	R/W	0x35
PWM2DIG_LSBs	0x12	R	0x00
PWM2DIG_MSBs	0x13	R	0x00
TURN_ON/OFF_RAMP	0x14	R/W	0x44
PWM_UP/DOWN_RAMP and IFS	0x15	R/W	0XF8

Table 8. REV Register

ADDRESS	MODE		RESET VALUE: 0x12
0x01	R		
BIT	NAME	POR	DESCRIPTION
7:2	DEV Revision	xxxxxx	Die Revision Identification
1:0	VENDOR	10	

Table 9. BL_CFG1 Register

ADDRESS	MODE		RESET VALUE: 0x28
0x02	R/W		
BIT	**NAME**	**POR**	**DESCRIPTION**
7:5	BL_OVP	001	Backlight OVP 000: 17V 001: 21V 010: 25V 011: 29V 100: 19V 101: 23V 110: 27V 111 = 32V
4	OVP_MODE	0	0: OVP is report only 1: OVP will turn off the fault string that cause OVP event.
3	BLED_MAP	1	0: Exponential 1: Linear
2	PWM_CONFIG	0	0: Active high 1: Active low
1	RSVD	0	
0	PWM_ENABLE	0	0: PWM disabled 1: PWM enabled

Note: When Backlight Current Mapping setting is changed, the LED current change will not take effect until Register 0x05 is programmed.

Table 10. BL_CFG2 Register

ADDRESS	MODE		RESET VALUE: 0x8D
0x03	R/W		
BIT	**NAME**	**POR**	**DESCRIPTION**
7	BL_FREQ_FREQ	1	Sets the backlight boost switch frequency 0: 500kHz 1: 1.0MHz (Default)
6:3	LED CURRENT RAMP	0001	Controls backlight LED ramping time. The transient time is a constant time that the backlight takes to transition from an existing programmed code to a new programmed code. 0000 : 1µs 0001 : 2ms(Default) 0010 : 4ms 0011 : 8ms 0100 : 16ms 0101 : 32ms 0110 : 64ms 0111 : 128ms 1000 : 192ms 1001 : 256ms 1010 : 320ms 1011 : 384ms 1100 : 448ms 1101 : 512ms 1110 : 576ms 1111 : 640ms
2:0	PWM_HYST	101	Sets the minimum change in PWM input duty cycle that results in a change of backlight LED brightness level 000 : 0 LSB 001: 2 LSBs 010: 4 LSBs 011: 6 LSBs 100: 8 LSBs 101: 10 LSBs(Default) 110: 12 LSBs 111: 14 LSBs

1. For LED CURRENT RAMP Time in the table, all the ramp times are fixed when current ramps from one level to the other except "0000" setting. For "0000" setting, the ramp slope is 1µs/step, the final ramp time is proportional to the 11-bit current steps.

Table 11. BL_BRT_LSB Register

ADDRESS	MODE		RESET VALUE: 0x07
0x04	R/W		
BIT	NAME	POR	DESCRIPTION
7:3	RSVD	00000	
2:0	BRT[2:0]	111	3-bit brightness code LSBs

Table 12. BL_BRT_MSB Register

ADDRESS	MODE		RESET VALUE: 0xFF
0x05	R/W		
BIT	NAME	POR	DESCRIPTION
7:0	BRT[7:0]	11111111	11-bit brightness code MSBs

Note:
1. If only using 8-bit current ratio, keep the 3-bit LSBs as '111' and only program the 8-bit MSBs.
2. If using 11-bit current ratio, the 3-bit LSBs should be programmed first, then the 8-bit MSBs can be programmed to take effect. Even if only the 3-bit LSBs need to be changed, the 8-bit MSB should always be programmed to make the 3-bit LSBs change taking effect.
3. For 11-bit program code 11'b00000000000, both boost converter and current sinks are turned off.

Table 13. BL_AUTOF_LOW Register

ADDRESS	MODE		RESET VALUE: 0x00
0x06	R/W		
BIT	NAME	POR	DESCRIPTION
7:0	AFLT	00000000	Compared against 8 MSB's of Brightness Code (register 0x05)

Table 14. BL_AUTOF_HIGH Register

ADDRESS	MODE		RESET VALUE: 0x00
0x07	R/W		
BIT	NAME	POR	DESCRIPTION
7:0	AFHT	00000000	Compared against 8 MSB's of Brightness Code (register 0x05)

Table 15. BL_EN Register

ADDRESS	MODE		RESET VALUE: 0x00
0x08	R/W		
BIT	NAME	POR	DESCRIPTION
7	SOFTWARE_RESET	0	0 = No reset 1 = Device reset (automatically returns to 0 after reset)
6	RSVD	0	
5	RAMP_SHAPE	0	0: Exponential 1: Linear
4	BL_EN	0	0 = BL disabled 1 = BL enabled
3	RSVD	0	Must be written as 0
2	LED3_EN	0	0 = Current sink 3 disabled 1 = Current sink 3 enabled
1	LED2_EN	0	0 = Current sink 2 disabled 1 = Current sink 2 enabled
0	LED1_EN	0	0 = Current sink 1 disabled 1 = Current sink 1 enabled

Note: Writing software reset bit to '1' will reset all I^2C registers to their default values, then this bit will be internally reset back to '0'.

Table 16. LCD_CFG1 Register

ADDRESS	MODE		RESET VALUE: 0x18
0x09	R/W		
BIT	NAME	POR	DESCRIPTION
7	LCD_EN	0	0 = Bias supply off (I^2C and external) 1 = Normal mode
6:5	RSVD	00	
4	OUTP_DISCH	1	0 = No pulldown on OUTP 1 = Pulldown on OUTP when in shutdown
3	OUTN_DISCH	1	0 = No pulldown on OUTN 1 = Pulldown on OUTN when in shutdown
2	OUTP_EN	0	0 = OUTP disabled 1 = OUTP enabled
1	OUTN_EN	0	0 = OUTN disabled 1 = OUTN enabled
0	EXT_EN	0	Activates external enables (ENP and ENN) 0 = External enables are disabled. OUTP and OUTN can only be enabled via bit OUTP_EN and OUTN_EN, respectively.(Default) 1 = External enables are enabled. OUTP and OUTN can only be enabled via pin ENP and ENN, respectively.

Table 17. LCD_CFG2 Register

ADDRESS	MODE		RESET VALUE: 0x11
0x0A	R/W		
BIT	NAME	POR	DESCRIPTION
7:6	BIAS_SHORT_MODE	00	0X = Flag only 10 = Flag + shutdown VPOS/VNEG 11 = Flag + shutdown VPOS/VNEG/Backlight
5:4	VPOS_RAMP	01	VPOS ramp time, low to high: 00 = 228µs 01 = 456µs 10 = 684µs 11 = 912µs
3:0	VNEG_RAMP	0001	VNEG ramp time, high to low: 0000 = 456µs 0001 = 912µs 0010 = 1368µs 0011 = 1824µs 0100 = 2280µs 0101 = 2736µs 0110 = 3192µs 0111 = 3648µs 1000 = 4104µs 1001 = 4560µs 1010 = 5016µs 1011 = 5472µs 1100 = 5928µs 1101 = 6384µs 1110 = 6840µs 1111 = 7296µs

Note:
1. For VPOS_RAMP time, it is fixed slew rate ramp strategy, the ramp time value is given by assuming OUTP = 5.75V. If OUTP is set 5.5V and VPOS_RAMP = 01, then actual ramp time will be 456*5.5/5.75 = 436µs.
2. For VNEG_RAMP time, it is fixed slew rate ramp strategy, the ramp time value is given by assuming OUTN = -5.75V. If OUTN is set -5.5V and VNEG_RAMP = 0001, then actual ramp time will be 912*5.5/5.75 = 872µs.

Table 18. LCD_CFG3 Register

ADDRESS	MODE		RESET VALUE: 0x00
0x0B	R/W		
BIT	NAME	POR	DESCRIPTION
7:4	RSVD	0000	
3:2	VPOS_SC_FILT	00	OUTP short circuit filter timer 00 = 2ms 01 = 1ms 10 = 500µs 11 = 100µs
1:0	VNEG_SC_FILT	00	OUTN short circuit filter timer 00 = 2ms 01 = 1ms 10 = 500µs 11 = 100µs

Table 19. LCD_BOOST_CFG Register

ADDRESS	MODE		RESET VALUE: 0x28
0x0C	R/W		
BIT	NAME	POR	DESCRIPTION
7:6	RSVD	00	
5:0	REG	101000	REG voltage (50-mV steps): REG = 4V + (Code × 50mV) 000000 : 4V 000001 : 4.05V : 101000 : 6V (Default) : >=110100 = 6.6V

Table 20. OUTP_CFG Register

ADDRESS	MODE		RESET VALUE: 0x1E
0x0D	R/W		
BIT	NAME	POR	DESCRIPTION
7:6	RSVD	00	
5:0	OUTP	011110	OUTP voltage (50mV steps): VPOS = 4V + (Code × 50mV), 6.3V max 000000 : 4V 000001 : 4.05V : 011110 : 5.5V (Default) : >=101110 : 6.3V

Note: Writing to Register 0x0D will not take effect immediately, until Register 0x09 is written again.

Table 21. OUTN_CFG Register

ADDRESS	MODE		RESET VALUE: 0x1C
0x0E	R/W		
BIT	NAME	POR	DESCRIPTION
7:6	RSVD	00	
5:0	OUTN	011100	VNEG voltage (–50mV steps): VNEG = -4 V - (Code × 50mV), -6.3V min 000000 = –4 V 000001 = –4.05V : 011100 = -5.4V (Default) : >=101110 = –6.3V

Note: Writing to Register 0x0E will not take effect immediately, until Register 0x09 is written again.

Table 22. FLAG Register

ADDRESS	MODE		RESET VALUE: 0x00
0x0F	R		
BIT	NAME	POR	DESCRIPTION
7	LED_SHORT	0	0 = Normal operation 1 = LED short protection trigged.
6	TSD	0	0 = Normal operation 1 = Thermal shutdown triggered (die temperature > 140°C)
5	RSVD	0	
4	RSVD	0	
3	OUTP_SHORT	0	0 = Normal operation 1 = OUTP output has hit the overcurrent threshold
2	OUTN_SHORT	0	0 = Normal operation 1 = OUTN > 0.9 × V_{OUTN_target}
1	BL_OVP	0	0 = Normal operation 1 = Backlight boost output > OVP threshold
0	BL_OCP	0	0 = Normal operation 1 = Backlight boost switch current > OCP threshold

Note:
1. TSD is real-time results.
2. LED_SHORT, OUTP_SHORT, OUTN_SHORT, BL_OVP and BL_OCP are latched results; OUTP_SHORT, OUTN_SHORT, BL_OVP and BL_OCP can be reset by reading back 0x0F.
3. All the status bits can be reset by VIN power on reset, software reset or toggling HWEN.

Table 23. BL_OPTION1 Register

ADDRESS	MODE		RESET VALUE: 0x06
0x10	R/W		
BIT	NAME	POR	DESCRIPTION
7	LED_SHORT_MODE	0	0 = Will keep all strings on. 1 = Will turn off the fault string while keep health strings keep on.
6	RSVD	0	Must be written as 0
5	LED3_FB_DISABLE	0	0 = Feedback enabled 1 = Feedback disabled
4	LED2_FB_DISABLE	0	0 = Feedback enabled 1 = Feedback disabled
3	LED1_FB_DISABLE	0	0 = Feedback enabled 1 = Feedback disabled
2:0	RSVD	110	

Note: If all LED1~LED3 disabled, Boost stops switching.

Table 24. BL_OPTION2 Register

ADDRESS	MODE		RESET VALUE: 0x35
0x11	R/W		
BIT	NAME	POR	DESCRIPTION
7:6	BL_L_SELECT	00	00 = 4.7μH 01 = 10μH 10 = 15μH 11 = 15μH
5:4	RSVD	11	
3:2	RSVD	01	
1:0	BL_CURRENT_LIMIT	01	00 = 1.2A 01 = 1.5A 10 = 1.8A 11 = 2.1A

Table 25. PWM2DIG_LSBs Register

ADDRESS	MODE		RESET VALUE: 0x00
0x12	R		
BIT	NAME	POR	DESCRIPTION
7:0	PWM_TO_DIG	00000000	11-bit PWM-to-digital conversion code LSBs

Table 26. PWM2DIG_MSBs Register

ADDRESS	MODE		RESET VALUE: 0x00
0x13	R		
BIT	NAME	POR	DESCRIPTION
7:3	RSVD	00000	
2:0	PWM_TO_DIG	000	11-bit PWM-to-digital conversion code MSBs

Note: 0x12 and 0x13 are suggested to be read out in successive way to make sure the PWM duty result is correct. Too long delay between reading them may cause incorrect returned result, since input PWM may change during the delay time.

Table 27. TURN_ON/OFF_RAMP Register

ADDRESS	MODE		RESET VALUE: 0x44
0x14	R/W		
BIT	NAME	POR	DESCRIPTION
7:4	RAMP_ON_TIME	0100	On Ramp Time 0000 : 512µs 0001 : 1ms 0010 : 2ms 0011 : 4ms 0100 : 8ms (Default) 0101 : 16ms 0110 : 32ms 0111 : 64ms 1000 : 128ms 1001 : 256ms 1010 : 512ms 1011 : 1024ms 1100 : 2048ms 1101 : 4096ms 1110 : 8192ms 1111 : 16384ms
3:0	RAMP_OFF_TIME	0100	Off Ramp Time 0000 : 512µs 0001 : 1ms 0010 : 2ms 0011 : 4ms 0100 : 8ms (Default) 0101 : 16ms 0110 : 32ms 0111 : 64ms 1000 : 128ms 1001 : 256ms 1010 : 512ms 1011 : 1024ms 1100 : 2048ms 1101 : 4096ms 1110 : 8192ms 1111 : 16384ms

Table 28. PWM_UP/DOWN_RAMP Register

ADDRESS	MODE		RESET VALUE: 0xF8
0x15	R/W		
BIT	NAME	POR	DESCRIPTION
7:3	IFS	**11111**	Backlight Full-scale LED Current ILED_FS ILED_FS = 5.2+Code*0.8mA 11111 : 30mA (Default) …. 10100 : 21.2mA 10011 : 20.4mA 10010: 19.6mA .... 00010 : 6.8mA 00001 : 6.0mA 00000 : 5.2mA
2:0	PWM_RAMP_TIME	000	PWM Duty Cycle Transition Ramp Time 000 : 2ms (Default) 001 : 4ms 010 : 8ms 011 : 16ms 100 : 32ms 101 : 64ms 110 : 128ms 111 : 256ms The time in the table is defined as the time to change between 0% PWM duty cycle and 100% PWM duty cycle. The final PWM duty cycle transition time is the multiplication of the time in the table and the difference of the PWM duty cycle change.

Note: The PWM Dimming Transition Ramp Time in the table is defined as the time to change between minimum PWM duty cycle and the maximum PWM duty cycle. The final transition time is the multiplication of the time in the table and the change of the PWM duty cycle.

Capacitor Selection

Small size ceramic capacitors with low ESR are ideal for all applications. A 10µF input capacitor and a 1µF~2.2µF output capacitor are suggested. The voltage rating of these capacitors should exceed the maximum possible voltage at the corresponding pins, and these capacitors should be as close as possible to the IC. Table 29 shows the recommended capacitor vendors.

Table 29. Recommended Capacitor Vendors

Manufacturer	Website
Murata	www.murata.com
AVX	www.avx.com
Taiyo Yuden	www.t-yuden.com

Inductor Selection

An inductor of 4.7µH to 10µH with low DCR can be selected for the boost converter. To decide the current rating of the inductor required for the application, the following equation can be used to estimate the peak inductor current I_{PEAK} in continuous conduction mode (CCM):

$$I_{PEAK} = \frac{V_{OUT(MAX)} \times I_{OUT(MAX)}}{V_{IN(MIN)} \times \eta} + \frac{V_{IN(MIN)}}{2L \times F_{SW}} \times \left(1 - \frac{V_{IN(MIN)}}{V_{OUT(MAX)}}\right)$$

where $V_{OUT(MAX)}$ is the maximum output voltage, $V_{IN(MIN)}$ is the minimum input voltage, $I_{OUT(MAX)}$ is the maximum output current, F_{SW} is the boost converter's switching frequency, L is the inductor value, η is the boost converter's efficiency under that condition. Table 30 shows recommended inductors under different application conditions.

Table 30. Recommended Inductors

Application	Inductor Part Number	Value (µH)	DCR (mΩ)	Saturation Current (A)	Dimensions (mm)	Manufacturer
3P7S (Max. 30mA/Ch)	VLF504012MT-4R7M-CA	4.7	120 max	1.83	5.0 x 4.0 x 1.2	Murata
3P9S (Max. 30mA/Ch)	SRP5030T-100M	10	128 max	2.75	5.7 x 5.2 x 2.8	Bourns

Schottky Diode Selection

Using a schottky diode is recommended because of its low forward voltage drop and fast reverse recovery time. The average current rating of the schottky diode should exceed the maximum output current, and its peak current rating should exceed the peak inductor current. Its voltage rating should also exceed the OVP setting. Table 31 shows the recommended schottky diode.

Table 31. Recommended Schottky Diode

Application	Schottky Diode Part Number	Forward Voltage (V)	Forward Current (A)	Reverse Voltage (V)	Manufacturer
All	PMEG4010B	0.54	1	40	NXP

Capacitor Selection for Dual Output Bias

Small size ceramic capacitors with low ESR are ideal for all applications. A 10µF output capacitor at REG are suggested. Higher capacitor values can be used to improve the load transient response. The voltage rating of these capacitors should exceed the maximum possible voltage at the corresponding pins, and these capacitors should be as close as possible to the IC.

Flying Capacitor Selection for Bias

The charge pump needs an external flying capacitor. The minimum value for smartphone application is 4.7µF and 10µF for tablet application. Special care must be taken while choosing the flying capacitor as it will directly impact the output voltage accuracy and load regulation performance.

Inductor Selection for Dual Output Bias

An inductor in the range of 2.2µH to 10µH with low DCR can be selected for the boost converter. To estimate the inductance required for applications, calculate the maximum input average current as the following

$$I_{IN(MAX)} = \frac{V_{OUT} \cdot I_{OUT(MAX)}}{V_{IN} \cdot \eta}$$

Where, η is the converter efficiency and can be approximated as 90% for the typical case. In order to have smaller current ripple (to improve efficiency and minimize output voltage ripple), larger inductance will be required. If inductor ripple current needs to be less than 40% of the average input current, then

$$\Delta I_L = \frac{V_{IN} \cdot D \cdot T_S}{L} \le 40\% \cdot \frac{V_{OUT} \cdot I_{OUT(MAX)}}{V_{IN} \cdot \eta}$$

Where duty cycle can be estimated as

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

Then

$$\Delta I_L = \frac{V_{IN} \cdot (V_{OUT} - V_{IN}) \cdot T_S}{L \cdot V_{OUT}} \le 40\% \cdot \frac{V_{OUT} \cdot I_{OUT(MAX)}}{V_{IN} \cdot \eta}$$

Therefore, the inductance can be calculated as

$$L \ge \frac{V_{IN}^2 \cdot (V_{OUT} - V_{IN}) \cdot \eta}{40\% \cdot V_{OUT}^2 \cdot I_{OUT(MAX)} \cdot f_S}$$

Where, f_S is the switching frequency of the boost converter.

Table 32. Recommended Inductor Part Numbers

Value (μH)	Manufacturer	Inductor Part Number	DCR (Ω)	Saturation Current (A)	EIA Size
2.2	Toko	DFE201612P-2R2M	0.12	1.5	2 x 1.6 x 1.0mm
4.7	Murata	LQH3NPN4R7MJRL	0.12	1.18	3 x 3 x 1.1mm

Recommended PCB Layout

PCB layout is very important for high frequency switching regulators in order to keep the loop stable and minimize noise. The input capacitor (C_{IN}) should be very close to the IC's VIN pin and PGND pin in order to get the best decoupling. The path between the inductor, LX pin, schottky diode and the output capacitor (C_{OUT}) should be kept as short as possible to minimize noise and ringing. To reduce power loss, the trace through the inductor, LX pin, schottky diode and C_{OUT} should be as short and wide as possible. Both input and output capacitors' GND terminals should be connected together on the PCB top layer and on the bottom layer GND plane.

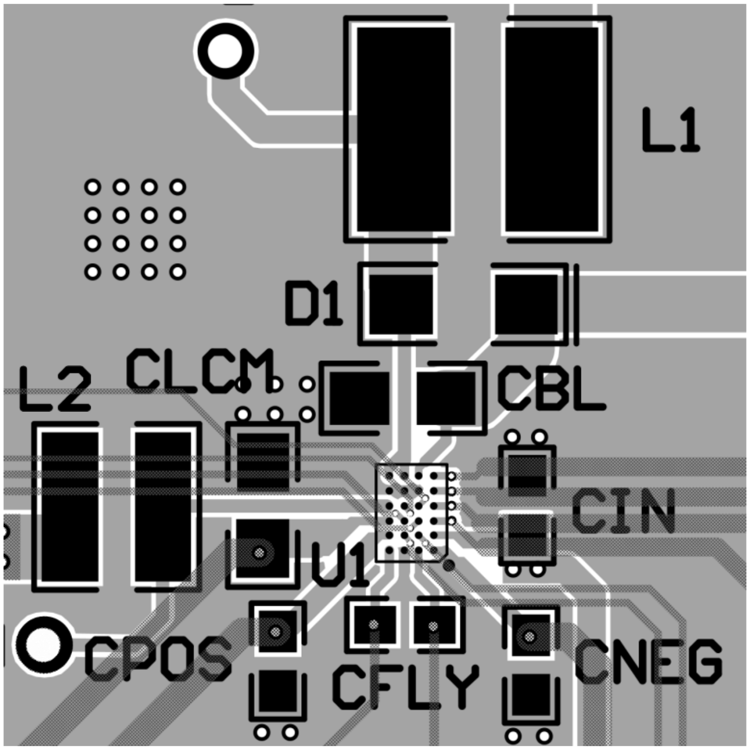


Figure 8. Recommended PCB Layout