

## Single and dual isolated 5 V low drop linear voltage regulators for automotive application




SO-8



### Features

Symbol	Parameter	Values
$V_S$	Max DC supply voltage	40 V
$\Delta V_O$	Max output voltage tolerance	$\pm 2\%$
$V_{dp}$	Max dropout voltage	500 mV
$I_O$	Output current	50 mA <sup>(1)</sup> 2x50 mA <sup>(2)</sup>
$I_{qn}$	Quiescent current	50 $\mu$ A <sup>(3)</sup>

1. For L5050S - single output. Up to 100 mA as pulsed current
2. For L5050SD - dual output. Up to 2x100 mA as pulsed current.
3. Typical value valid for each single output with  $E_n = LOW$ .

- AEC-Q100 qualified 
- Operating DC supply voltage range 5.6 V to 40 V
- Low dropout voltage
- Low quiescent current consumption
- Up to 100 mA and 2x100 mA as pulsed current
- Precision output voltage 5 V  $\pm 2\%$
- Dual electrically isolated voltage regulators (only for L5050SD)
- Enable input for enabling/disabling the voltage regulator
- Thermal shutdown and short circuit protection
- Wide temperature range ( $T_j = -40\text{ }^\circ\text{C}$  to  $150\text{ }^\circ\text{C}$ )

### Description

L5050 is a 5 V low dropout linear voltage regulator suitable for automotive applications, available in single (L5050S) or dual isolated (L5050SD) linear output voltage in a SO-8 package. The LDO delivers up to 50 mA (2x50 mA for the dual version) of DC load current and consumes as low as 5  $\mu$ A (per each output in L5050SD) of quiescent current with device disabled. High output voltage accuracy ( $\pm 2\%$ ) is kept over wide temperature range, line and load variation. The L5050S is able to deliver up to 100 mA (as pulsed current) and L5050SD up to 100 mA (as pulsed current); duration of current is linked to thermal settings (such as PCB type, ambient temperature). Enable features (two enables for the dual version) allow enabling or disabling each output. The maximum input voltage is 40 V. The regulator output current is internally limited and the device is protected against short circuit, overload and over temperature conditions. In addition, only low value ceramic capacitor on output is required for stability.

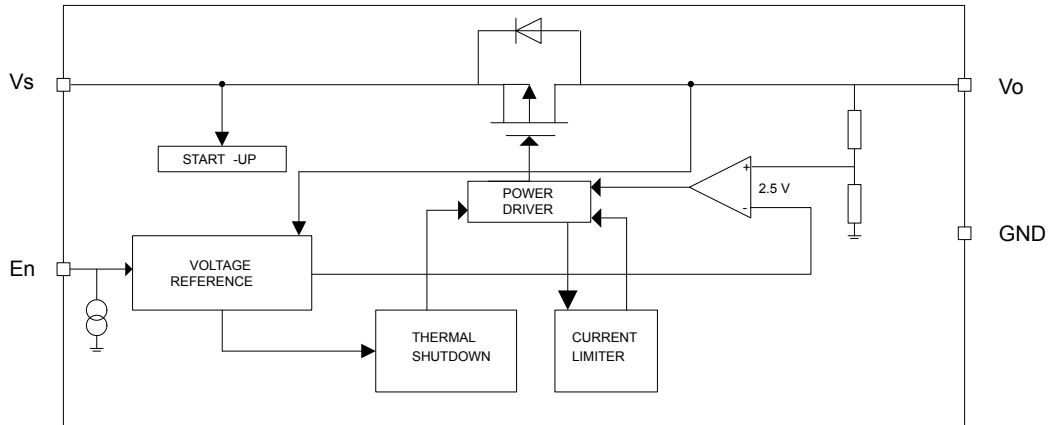
#### Product status link

[L5050](#)

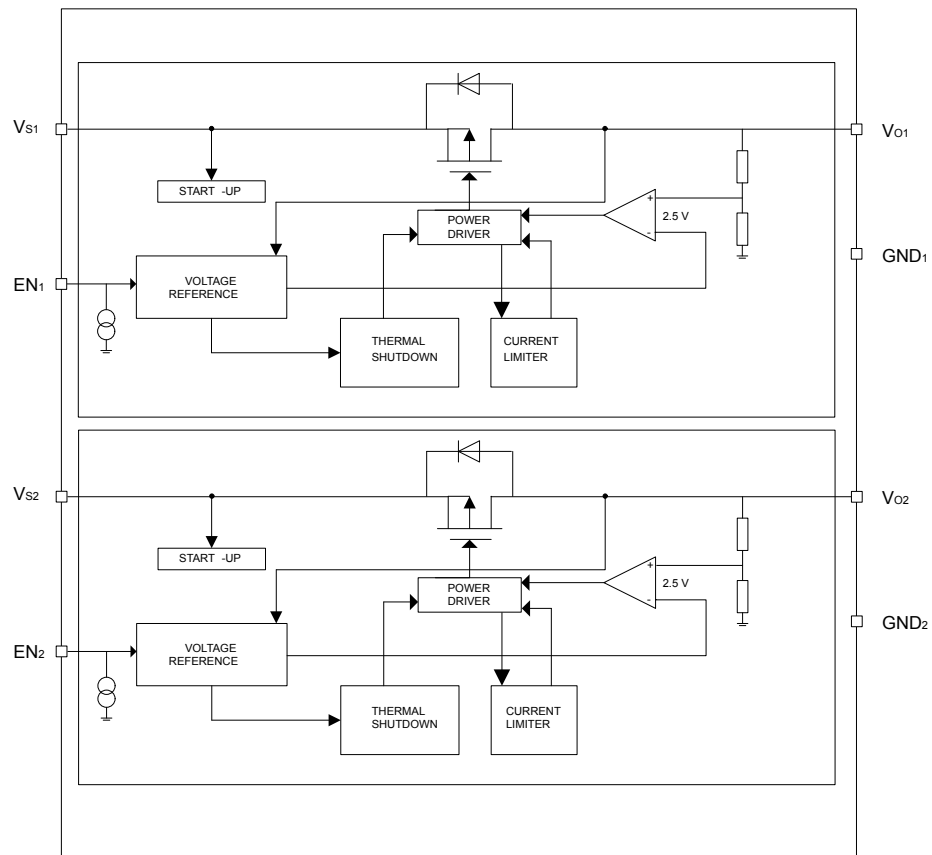
#### Product summary

Order code	L5050STR, L5050SDTR
Package	SO-8
Packing	Tape and reel

# 1 Block diagram and pins description

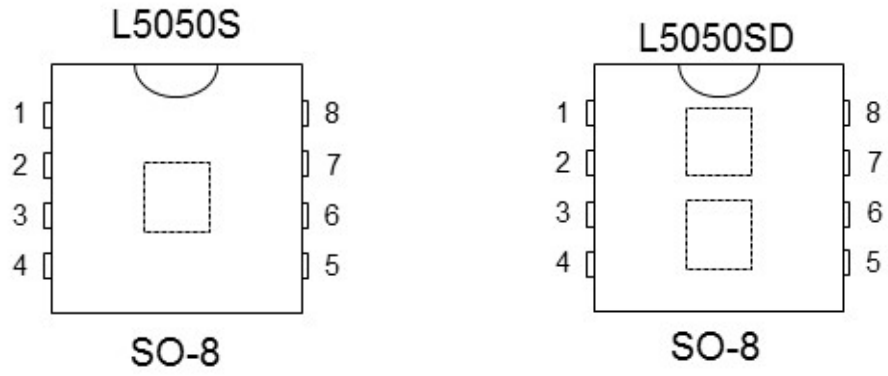
**Figure 1. Functional block diagram - L5050S**

**Table 1. L5050S pins description**

Pin name	Pin number	Function
N.C.	1	-
GND	2	Ground reference for regulator
Vo	3	5 V regulated output. Block to GND with a ceramic capacitor ( $\geq 220$ nF for regulator stability)
N.C.	4	-
N.C.	5	-
V <sub>S</sub>	6	Supply voltage, block directly to GND on the IC with a capacitor.
En	7	Enable pin for regulator: high signal to switch the regulator on
N.C.	8	-

**Figure 2. Functional block diagram - L5050SD**

**Table 2. L5050SD pins description**

Pin name	Pin number	Function
GND1	1	Ground reference for regulator 1
Vo1	2	5 V regulated output 1. Block to GND1 with a ceramic capacitor ( $\geq 220$ nF for regulator stability)
GND2	3	Ground reference for regulator 2
Vo2	4	5 V regulated output 2. Block to GND2 with a ceramic capacitor ( $\geq 220$ nF for regulator stability)
VS2	5	Supply voltage 2, block directly to GND2 on the IC with a capacitor
En2	6	Enable pin for regulator 2: <ul style="list-style-type: none"> <li>high signal to switch the regulator on</li> </ul>
VS1	7	Supply voltage 1, block directly to GND1 on the IC with a capacitor.
En1	8	Enable pin for regulator 1: <ul style="list-style-type: none"> <li>high signal to switch the regulator on</li> </ul>

Figure 3. Pins configuration



## 2 Electrical specifications

### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in the [Table 3](#): absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality documents.

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_s$	DC supply voltage	-0.3 to 40	V
$I_s$	Input current	internally limited	
$V_o$	DC output voltage	-0.3 to 6	V
$I_o$	DC output current	internally limited	
$V_{En}$	Enable input	-0.3 to 40	
$T_J$	Junction operating temperature	-40 to 150	°C
$V_{ESD\ HBM}$	ESD HBM voltage level (HBM-MIL STD 883C)	±2	kV
$V_{ESD\ CDM}$	ESD CDM voltage level (CDM)	±750 <sup>(1)</sup>	V

1. ±500 V for En1 and En2 (only for L5050SD).

**Table 4. Thermal data**

Item	Symbol	Parameter	Value <sup>(1)</sup>		Unit
			L5050S	L5050SD	
A.022	$R_{thJL}$	Thermal resistance, junction-to-lead	60.6	60.6	°C/W
A.001	$R_{thJA}$	Thermal resistance, junction-to-ambient	96	94	°C/W

1. PCB: single layer; FR4 area = 77 mm x 86 mm; PCB thickness = 1.6 mm; Cu thickness = 70 μm (front side), Cu area = 2 cm<sup>2</sup>.

## 2.2 Electrical characteristics

Values specified in this section are for  $V_S = 5.6 \text{ V}$  to  $31 \text{ V}$ ,  $T_J = -40 \text{ }^\circ\text{C}$  to  $+150 \text{ }^\circ\text{C}$ , unless otherwise stated.

**Table 5. General**

Item	Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A.002	$V_o$	$V_o$	Output voltage	$V_S = 5.6$ to $31 \text{ V}$ ; $I_o = 5$ to $50 \text{ mA}$	4.9	5	5.1	V
A.020	$V_o$	$V_o$	Output voltage	$V_S = 5.6$ to $31 \text{ V}$ ; $I_o = 100 \text{ mA}$	4.85	5	5.15	V
A.003	$V_o$	$I_{\text{short}}$	Short circuit current	$V_S = 5.6$ to $31 \text{ V}$	200	380	550	mA
				$V_S = 10.5 \text{ V}$	200	370	450	
A.004	$V_o$	$I_{\text{lim}}^{(1)}$	Output current limitation	$V_S = 10.5 \text{ V}$	110	225	450	mA
A.005	$V_S, V_o$	$V_{\text{line}}$	Line regulation voltage	$V_S = 5.6$ to $18 \text{ V}$ ; $I_o = 5$ to $50 \text{ mA}$			50	mV
A.021	$V_S, V_o$	$V_{\text{line}}$	Line regulation voltage	$V_S = 5.6$ to $18 \text{ V}$ ; $I_o = 100 \text{ mA}$			60	mV
A.006	$V_o$	$V_{\text{load}}$	Load regulation voltage	$I_o = 5$ to $100 \text{ mA}$ , $V_S = 5.6$ to $31 \text{ V}$			55	mV
A.007	$V_S, V_o$	$V_{\text{dp}}$	Drop voltage	$I_o = 100 \text{ mA}$			500	mV
A.008	$V_S, V_o$	SVR	Ripple rejection	$f_r = 100 \text{ Hz}^{(2)}$		60		dB
A.009	$V_o$	$I_{\text{oth\_H}}$	Normal consumption mode output current		4			mA
A.010	$V_o$	$I_{\text{oth\_L}}$	Very low consumption mode output current				0.1	mA
A.011	$V_S, V_o$	$I_{\text{qn}}$	Current consumption with regulator disabled $I_{\text{qn}} = I_{V_S} - I_o$	$V_S = 13.5 \text{ V}$ , $E_n = \text{low}$		5	10	$\mu\text{A}$
A.012	$V_S, V_o$	$I_{\text{qn\_1}}$	Current consumption with regulator enabled $I_{\text{qn\_1}} = I_{V_S} - I_o$	$I_o = 0.1 \text{ mA}$ to $0.3 \text{ mA}$ ; $E_n = \text{high}$		50	70	$\mu\text{A}$
A.013	$V_S, V_o$	$I_{\text{qn\_100}}$	Current consumption with regulator enabled $I_{\text{qn\_100}} = I_{V_S} - I_o$	$I_o = I_{\text{oth\_H}}$ to $100 \text{ mA}$ ; $E_n = \text{high}$		2	4.2	mA
A.014		$T_w$	Thermal protection temperature <sup>(3)</sup>		150		190	$^\circ\text{C}$
A.015		$T_{w\_hy}$	Thermal protection temperature hysteresis			10		$^\circ\text{C}$

1. Measured output current when the output voltage has dropped 200 mV from its nominal value obtained at  $V_S = 10.5 \text{ V}$  and  $I_o = 25 \text{ mA}$ .

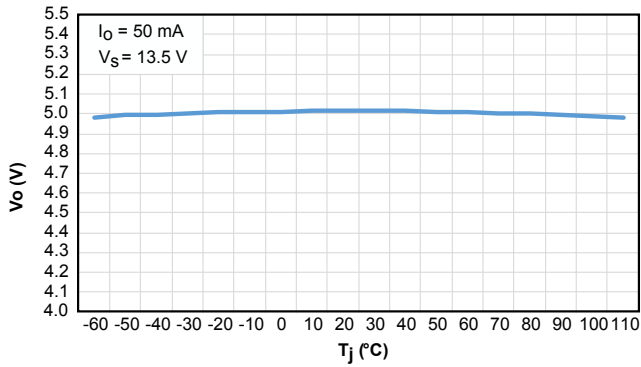
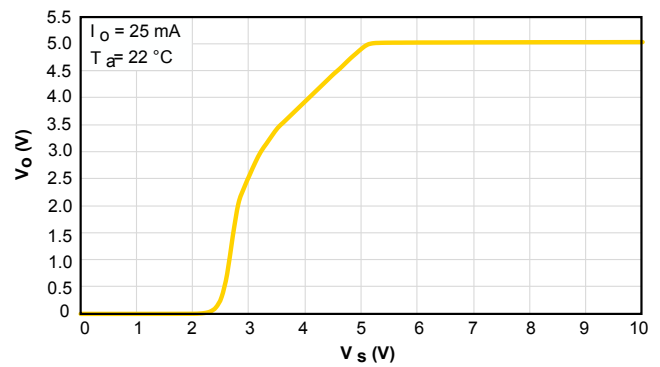
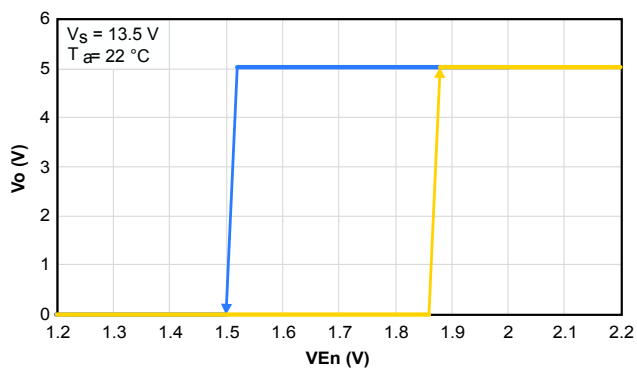
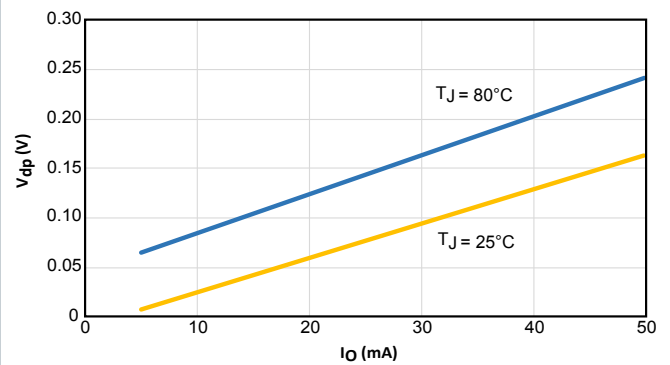
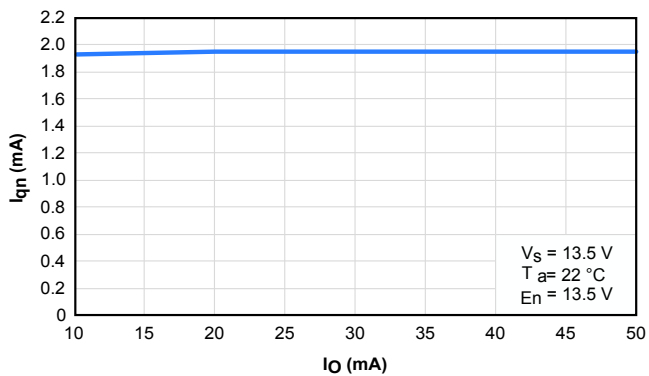
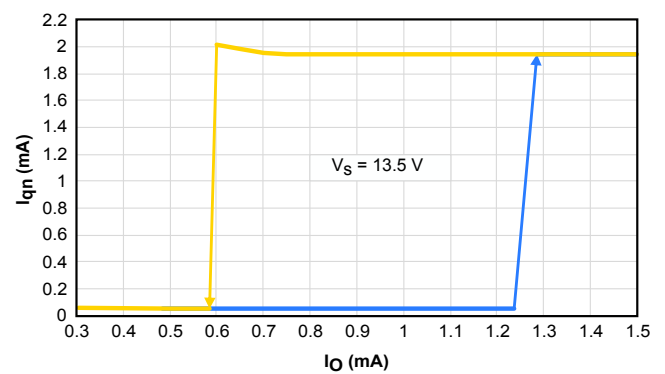
2. Guaranteed by design.

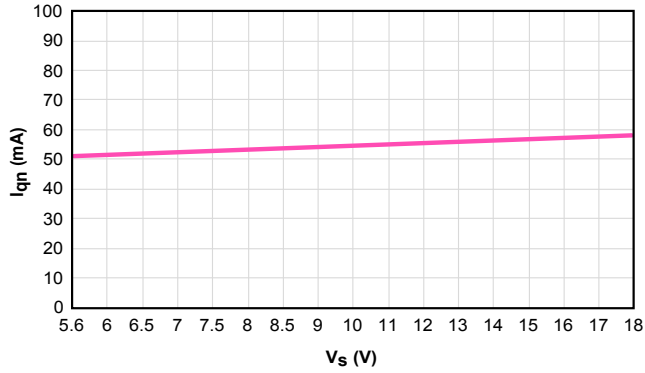
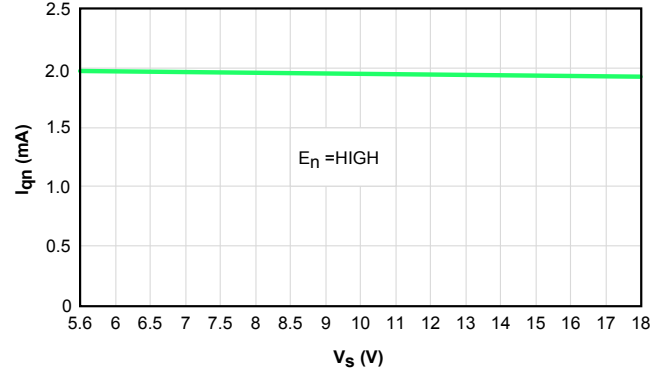
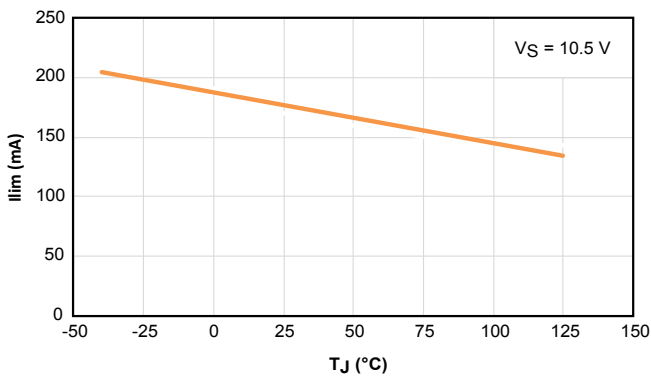
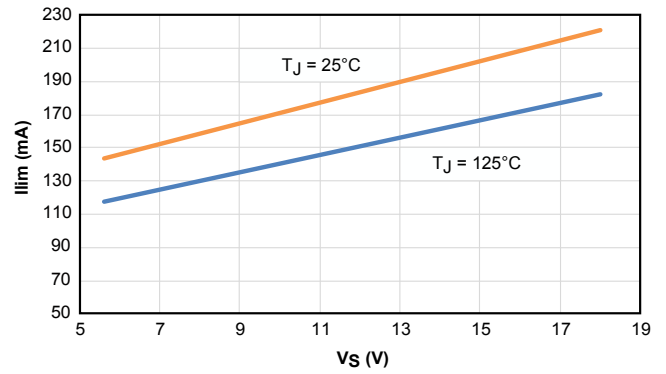
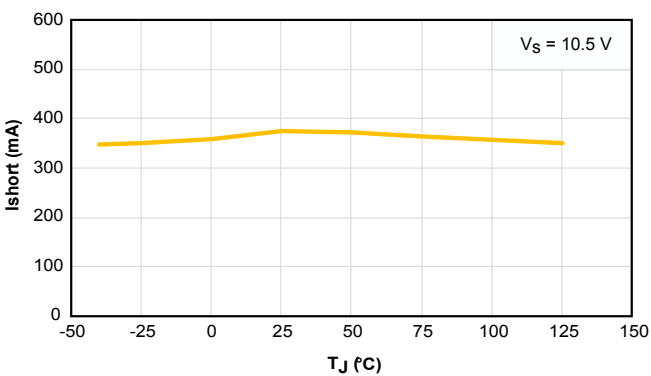
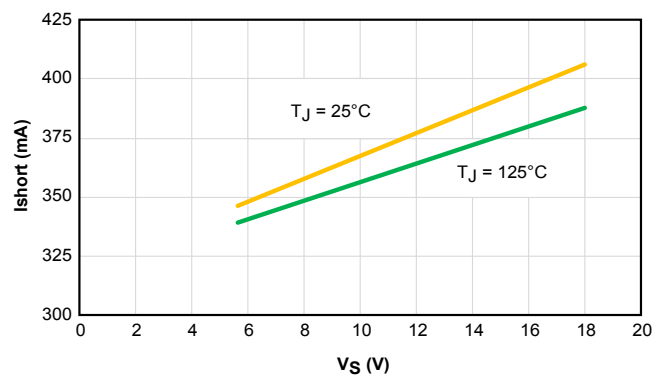
3. Thermal protection is guaranteed by design and characterization.

**Table 6. Enable**

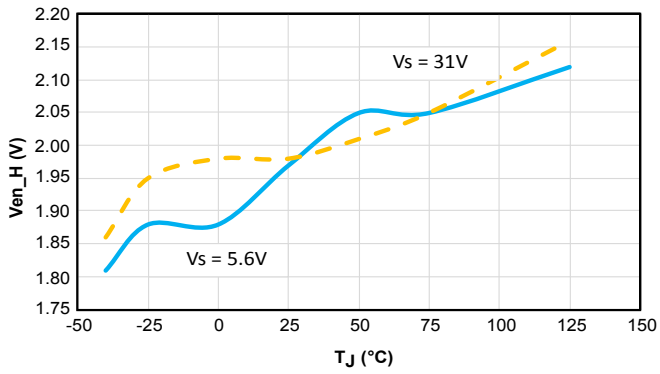
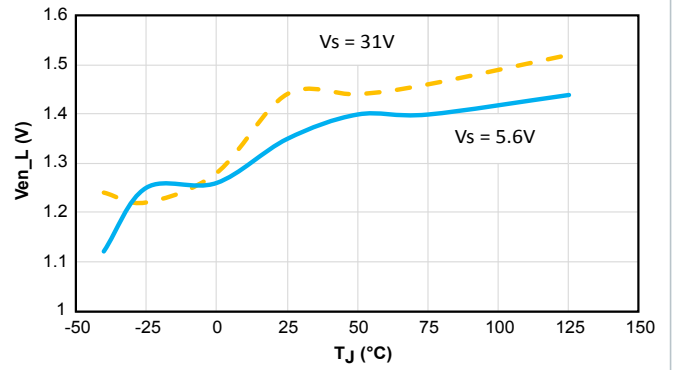
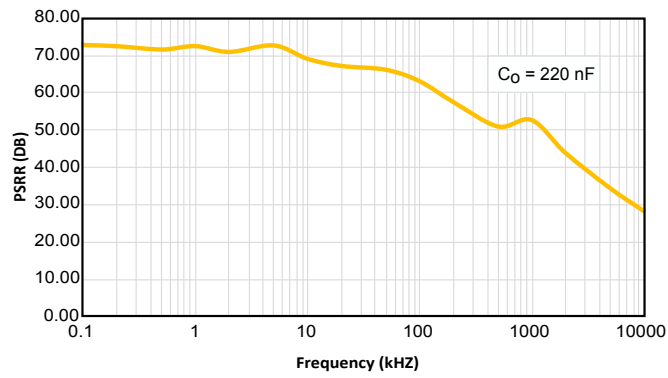
Item	Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A.016	En	$V_{\text{En\_low}}$	En input low voltage				1	V
A.017	En	$V_{\text{En\_high}}$	En input high voltage		3			V
A.018	En	$V_{\text{En\_hyst}}$	En input hysteresis			800		mV
A.019	En	$I_{\text{leak}}$	Pull down current	$V_{\text{En}} = 5 \text{ V}$		3	10	$\mu\text{A}$

### 2.3 Electrical characteristics curves

**Figure 4. Output voltage vs  $T_J$** 

**Figure 5. Output voltage vs  $V_s$** 

**Figure 6. Output voltage vs  $V_{En}$** 

**Figure 7. Drop voltage vs output current**

**Figure 8. Current consumption vs output current**

**Figure 9. Current consumption vs output current (at light load condition)**


**Figure 10. Current consumption vs input voltage ( $I_o = 0.15$  mA)**

**Figure 11. Current consumption vs input voltage ( $I_o = 50$  mA)**

**Figure 12. Current limitation vs  $T_J$** 

**Figure 13. Current limitation vs input voltage**

**Figure 14. Short-circuit current vs  $T_J$** 

**Figure 15. Short-circuit current vs input voltage**




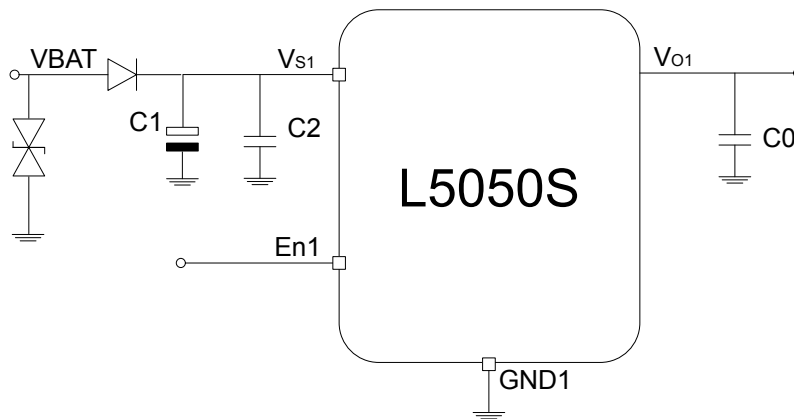
**Figure 16.  $V_{En\_high}$  vs  $T_J$** 

**Figure 17.  $V_{En\_low}$  vs  $T_J$** 

**Figure 18. PSRR**


### 3 Protection features

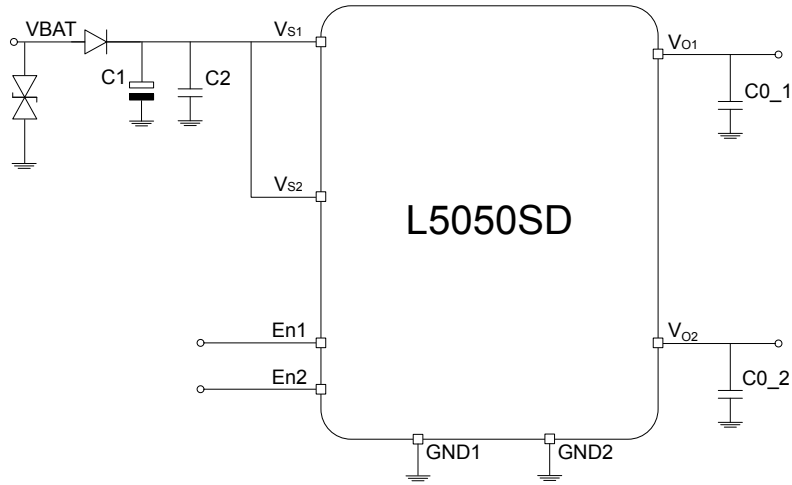
#### 3.1 Voltage regulator

Voltage regulator uses a p-channel MOS transistor as a regulating element. With that structure, a very low dropout voltage at current up to 100 mA is obtained. The output voltage is regulated up to transient input supply voltage of 40 V. The high-precision of the output voltages ( $\pm 2\%$ ) is obtained with a pre-trimmed reference voltage. The voltage regulator automatically adapts its own quiescent current to the output current level. In light load conditions, the quiescent current goes down to 50  $\mu\text{A}$  only in low consumption mode (for each regulating element in L5050SD). This procedure features a certain hysteresis on the output current (see [Figure 9. Current consumption vs output current \(at light load condition\)](#)). Short-circuit protection to GND and a thermal shutdown are provided.

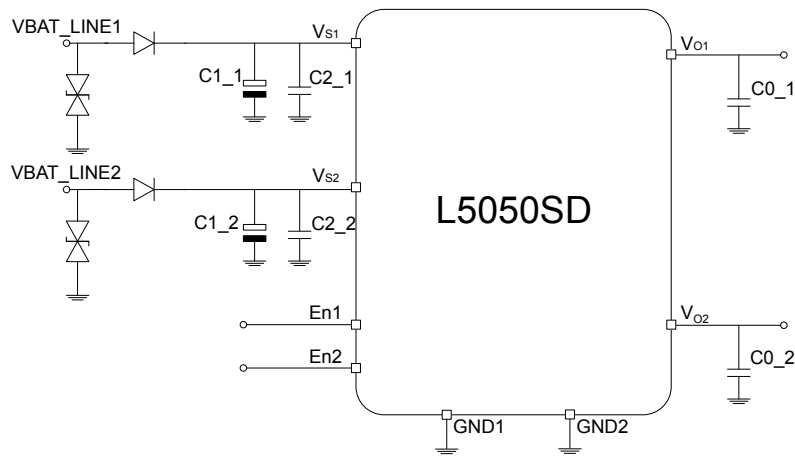
Figure 19. Application schematic - L5050S



**Figure 20. Application schematic - L5050SD - common input voltage**

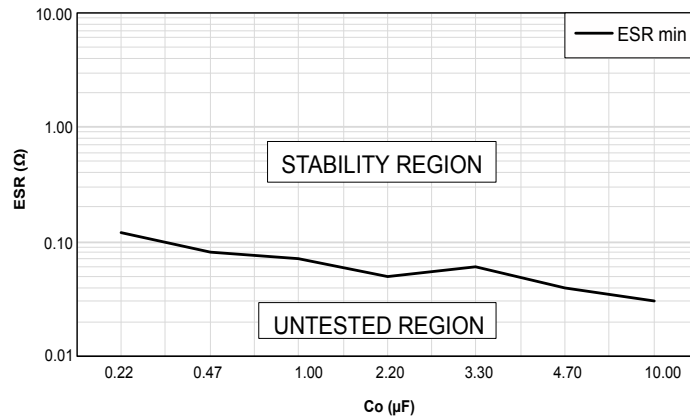


**Figure 21. Application schematic - L5050SD - double supply line for the input voltages**

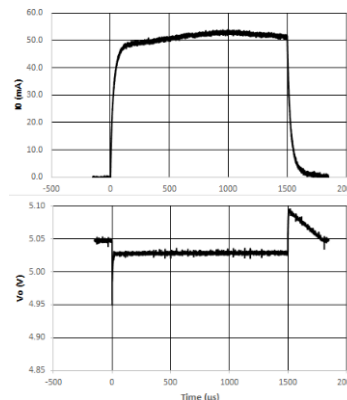


The input capacitor C1 is necessary as backup supply for short battery voltage interruption, which may occur on the line. Its value, should be chosen according to the relevant application requirement. The second input capacitor  $C2 \geq 220 \text{ nF}$  is needed when the C1 is too distant from the VS pin and it compensates smooth line disturbances. The C0 ceramic capacitor, connected to the output pin, is for bypassing to GND the high-frequency noise and it guarantees stability even during sudden line and load variations. Suggested value is  $C0 = 220 \text{ nF}$  with  $\text{ESR} \geq 100 \text{ m}\Omega$ . Stability region is reported in the figure below.

**Figure 22. Stability region**



**Figure 23. Maximum load variation response**

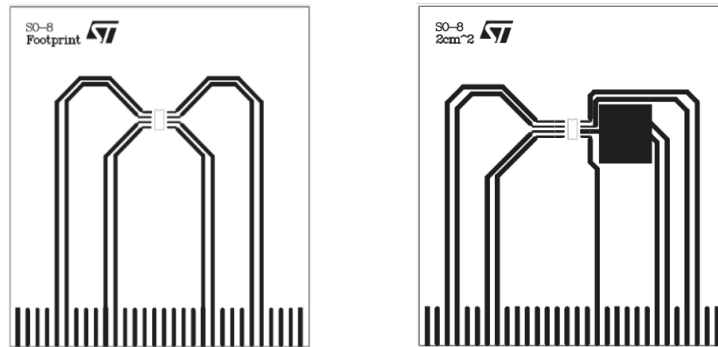


### 3.2 Enable

L5050 features enable input (two enable input pins for the L5050SD, one for each voltage regulator). A high voltage level at the enable input pin switches the regulator element ON. In standby mode, with the enable input pin low, the regulator output is disabled and the current consumption of the corresponding regulator (quiescent current) is typically  $5 \mu\text{A}$ .

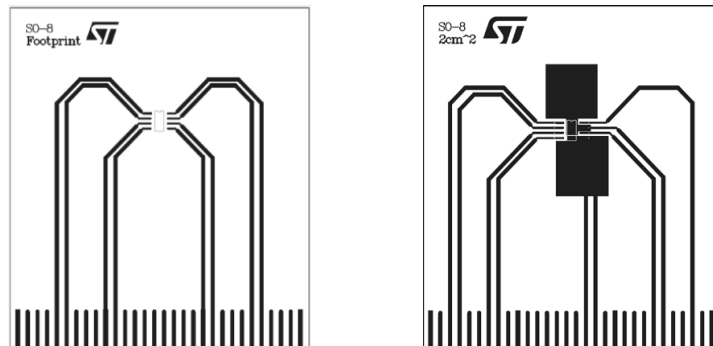
## 4 Package and PCB thermal data

Figure 24. SO-8 PC board for L5050S



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB: single layer; FR4 area = 77 mm x 86 mm; PCB thickness = 1.6 mm; Cu thickness = 70  $\mu\text{m}$  (front side), Cu area = 2  $\text{cm}^2$  for L5050S (picture on the right)).

Figure 25. SO-8 PC board for L5050SD



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB: single layer; FR4 area = 77 mm x 86 mm; PCB thickness = 1.6 mm; Cu thickness = 70  $\mu\text{m}$  (front side); Cu area = 2  $\text{cm}^2$  for L5050SD (picture on the right)).

Figure 26. Rthj-amb vs PCB copper area in open box free air condition

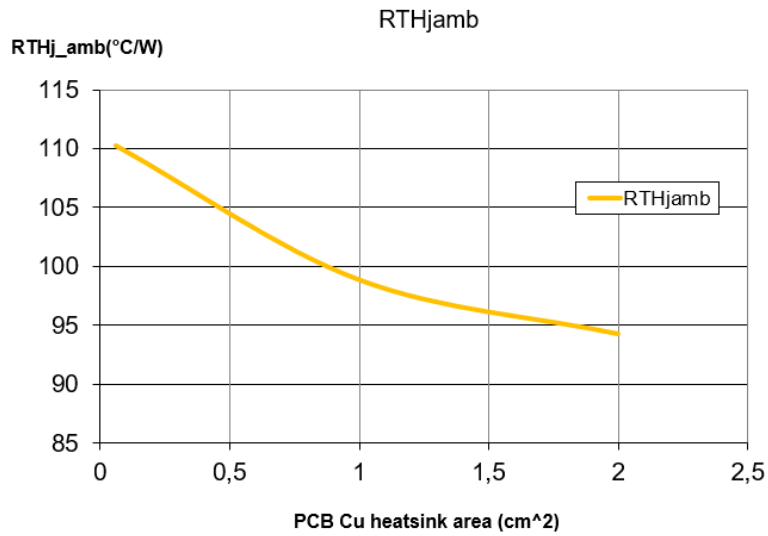


Figure 27. SO-8 thermal impedance junction ambient single pulse (L5050S)

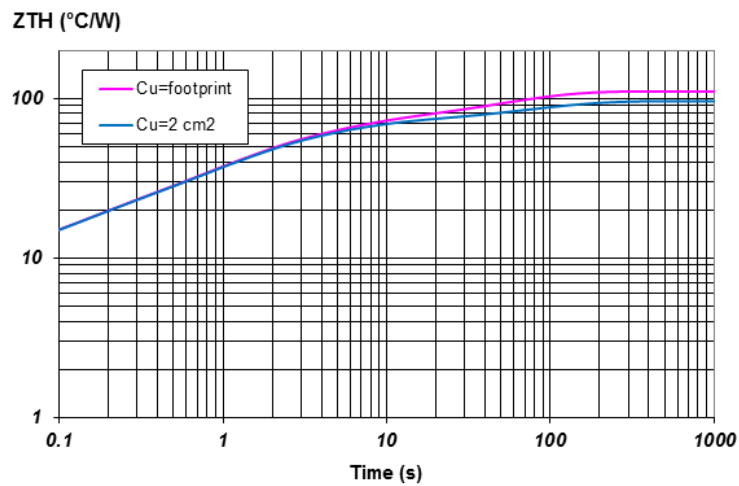
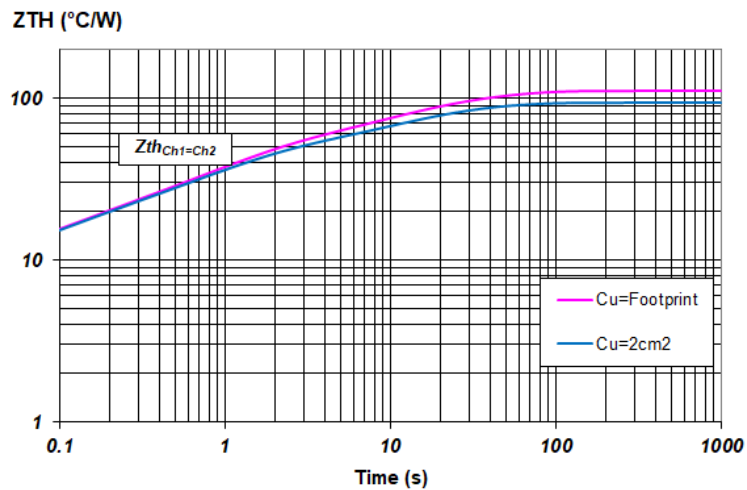


Figure 28. SO-8 thermal impedance junction ambient single pulse (one channel on for L5050SD)

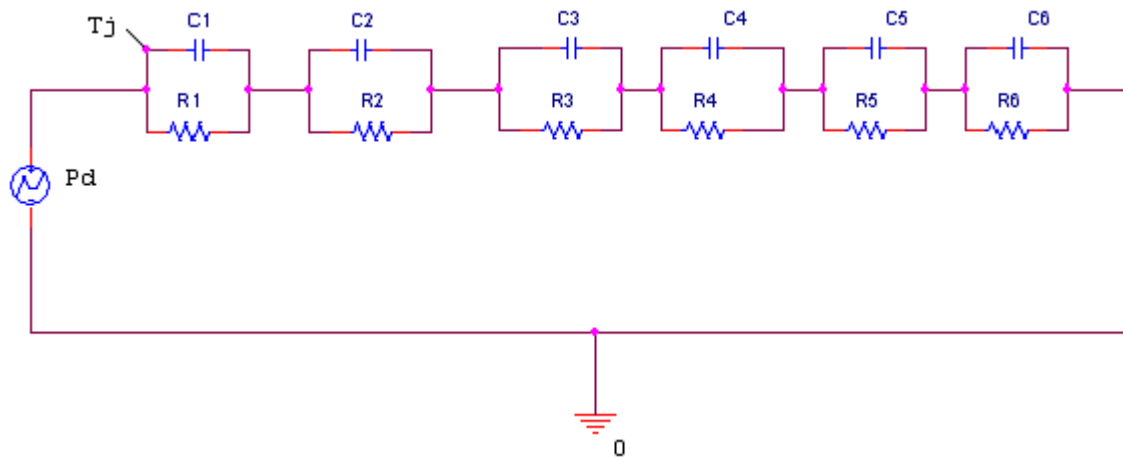


**Equation 1:** pulse calculation formula

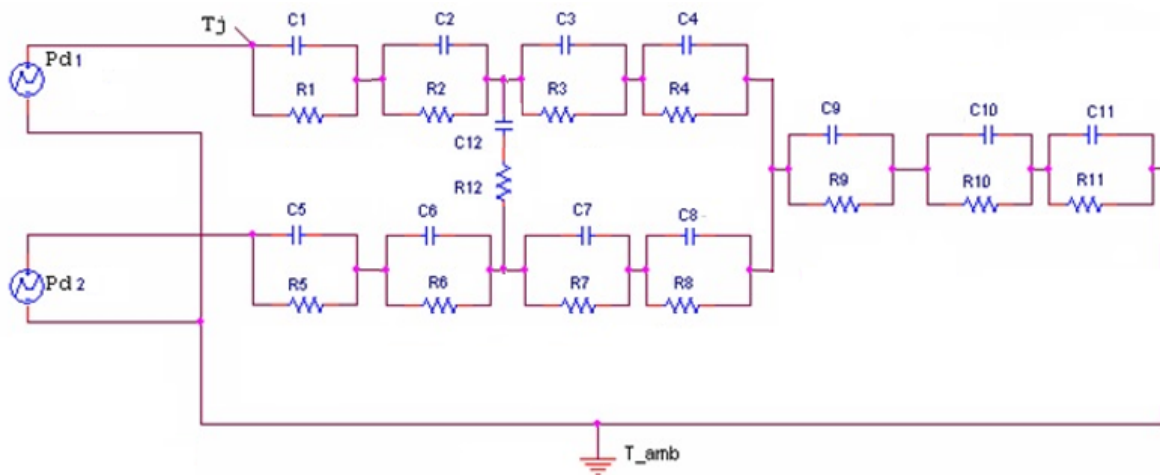
$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = tp/T$

**Figure 29.** L5050S thermal fitting model of a V<sub>reg</sub> in SO-8



**Figure 30.** L5050SD Thermal fitting model of a V<sub>reg</sub> in SO-8



**Table 7. L5050S SO-8 thermal parameter**

Area/island (cm <sup>2</sup> )	FP	2
R1 (°C/W)	3.2	
R2 (°C/W)	4.2	
R3 (°C/W)	7.9	
R4 (°C/W)	26.5	
R5 (°C/W)	27	
R6 (°C/W)	41.6	27.1
C1 (W·s/°C)	0.00001	
C1 (W·s/°C)	0.0015	
C3 (W·s/°C)	0.014	
C4 (W·s/°C)	0.04	
C5 (W·s/°C)	0.165	
C6 (W·s/°C)	1.4	3

**Table 8. L5050SD SO-8 thermal parameter**

Area/island (cm <sup>2</sup> )	FP	2
R1 - R5 (°C/W)	3.2	
R2 - R6 (°C/W)	4.2	
R3 - R7 (°C/W)	7.9	
R4 - R8 (°C/W)	8	
R9 (°C/W)	26	24
R10(°C/W)	28	23
R11 (°C/W)	33	24
R12 (°C/W)	50	50
C1 - C5 (W·s/°C)	0.00001	
C1 - C6 (W·s/°C)	0.0015	
C3 - C7 (W·s/°C)	0.014	
C4 - C8 (W·s/°C)	0.06	
C9 (W·s/°C)	0.05	
C10 (W·s/°C)	0.35	0.45
C11 (W·s/°C)	1	1.2
C12 (W·s/°C)	0.1	0.1

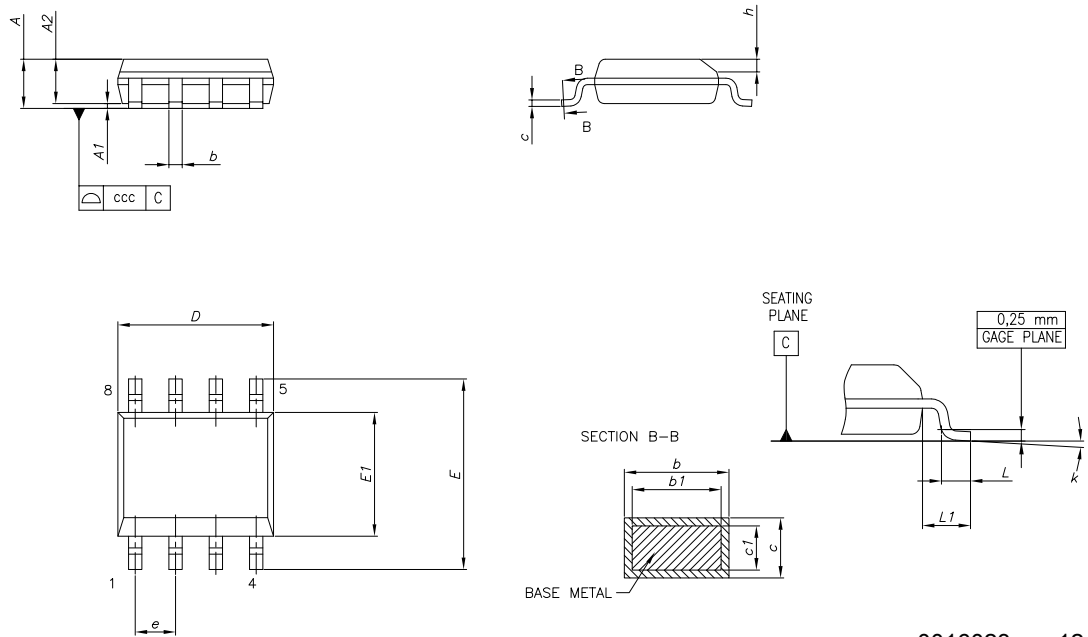


## 5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 5.1 SO-8 package information

Figure 31. SO-8 package outline

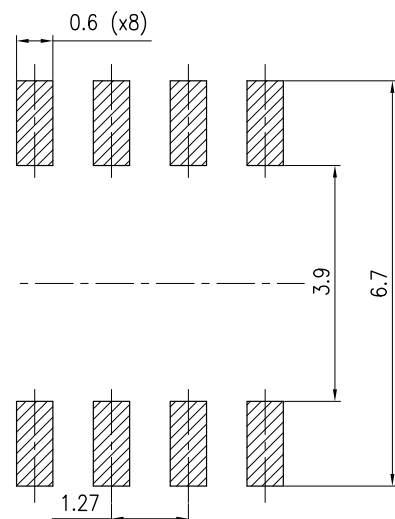


0016023\_rev12

Table 9. SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

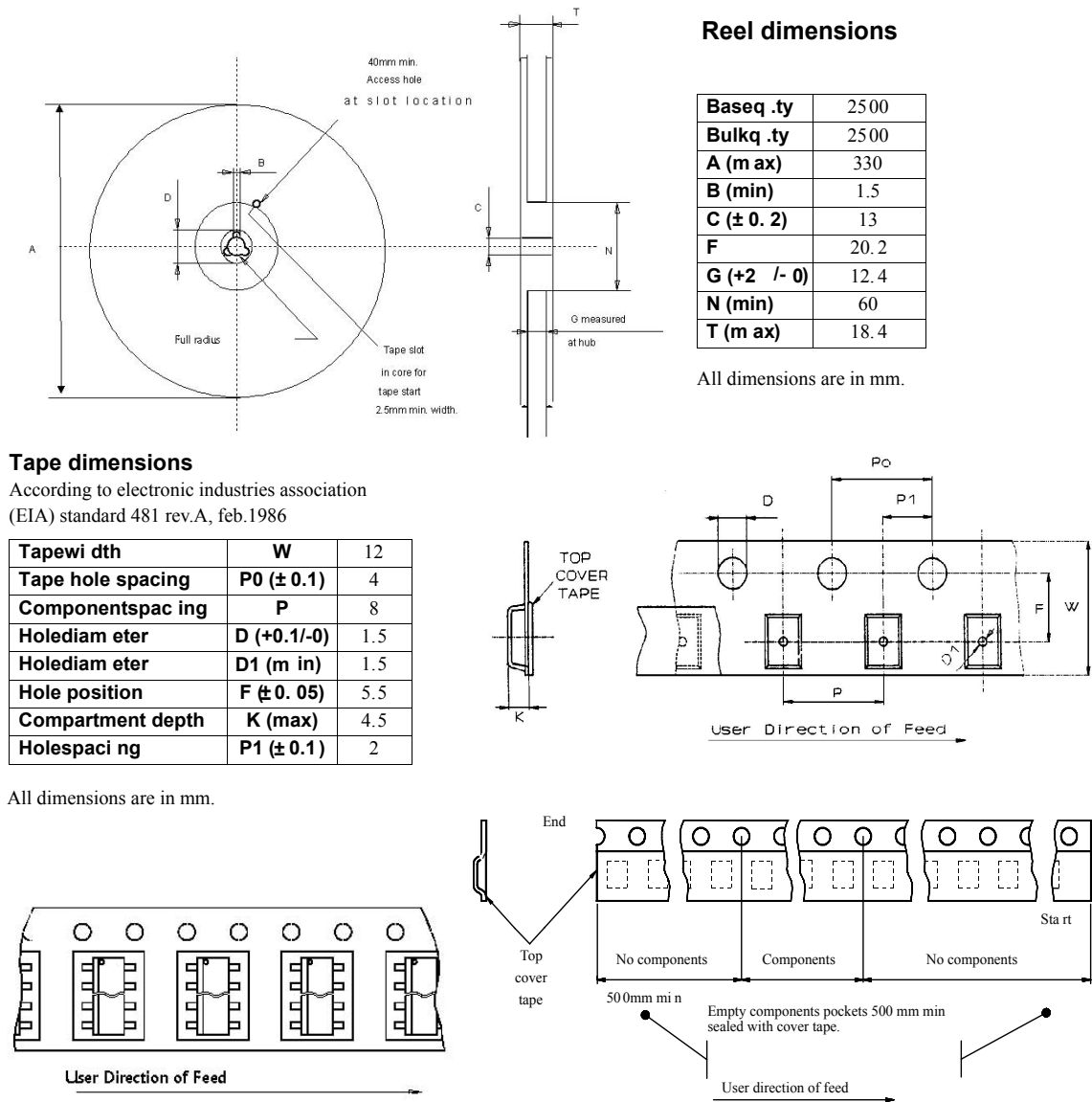
Figure 32. SO-8 recommended footprint (dimensions are in mm)



0016023\_Rev12

## 5.2 SO-8 packaging information

Figure 33. SO-8 tape and reel shipment (suffix "TR")



## Revision history

**Table 10. Document revision history**

Date	Version	Changes
19-Apr-2021	1	Initial release.
11-May-2022	2	<p>Updated features and description in cover page.</p> <p>Updated Table 4. Thermal data, Table 5. General , Section 4 Package and PCB thermal data and Figure 28. SO-8 thermal impedance junction ambient single pulse (one channel on for L5050SD).</p> <p>Minor text changes.</p>

## Contents

<b>1</b>	<b>Block diagram and pins description.....</b>	<b>2</b>
<b>2</b>	<b>Electrical specifications .....</b>	<b>5</b>
2.1	Absolute maximum ratings.....	5
2.2	Electrical characteristics.....	6
2.3	Electrical characteristics curves .....	7
<b>3</b>	<b>Protection features .....</b>	<b>10</b>
3.1	Voltage regulator .....	10
3.2	Enable .....	12
<b>4</b>	<b>Package and PCB thermal data .....</b>	<b>13</b>
<b>5</b>	<b>Package information.....</b>	<b>17</b>
5.1	SO-8 package information .....	17
5.2	SO-8 packaging information .....	19
	<b>Revision history .....</b>	<b>20</b>

## List of tables

<b>Table 1.</b>	L5050S pins description . . . . .	2
<b>Table 2.</b>	L5050SD pins description . . . . .	3
<b>Table 3.</b>	Absolute maximum ratings . . . . .	5
<b>Table 4.</b>	Thermal data . . . . .	5
<b>Table 5.</b>	General . . . . .	6
<b>Table 6.</b>	Enable . . . . .	6
<b>Table 7.</b>	L5050S SO-8 thermal parameter . . . . .	16
<b>Table 8.</b>	L5050SD SO-8 thermal parameter . . . . .	16
<b>Table 9.</b>	SO-8 mechanical data . . . . .	18
<b>Table 10.</b>	Document revision history . . . . .	20

## List of figures

<b>Figure 1.</b>	Functional block diagram - L5050S	2
<b>Figure 2.</b>	Functional block diagram - L5050SD	3
<b>Figure 3.</b>	Pins configuration	4
<b>Figure 4.</b>	Output voltage vs $T_J$	7
<b>Figure 5.</b>	Output voltage vs $V_s$	7
<b>Figure 6.</b>	Output voltage vs $V_{en}$	7
<b>Figure 7.</b>	Drop voltage vs output current	7
<b>Figure 8.</b>	Current consumption vs output current	7
<b>Figure 9.</b>	Current consumption vs output current (at light load condition)	7
<b>Figure 10.</b>	Current consumption vs input voltage ( $I_o = 0.15$ mA)	8
<b>Figure 11.</b>	Current consumption vs input voltage ( $I_o = 50$ mA)	8
<b>Figure 12.</b>	Current limitation vs $T_J$	8
<b>Figure 13.</b>	Current limitation vs input voltage	8
<b>Figure 14.</b>	Short-circuit current vs $T_J$	8
<b>Figure 15.</b>	Short-circuit current vs input voltage	8
<b>Figure 16.</b>	$V_{En\_high}$ vs $T_J$	9
<b>Figure 17.</b>	$V_{En\_low}$ vs $T_J$	9
<b>Figure 18.</b>	PSRR	9
<b>Figure 19.</b>	Application schematic - L5050S	10
<b>Figure 20.</b>	Application schematic - L5050SD - common input voltage	11
<b>Figure 21.</b>	Application schematic - L5050SD - double supply line for the input voltages	11
<b>Figure 22.</b>	Stability region	12
<b>Figure 23.</b>	Maximum load variation response	12
<b>Figure 24.</b>	SO-8 PC board for L5050S	13
<b>Figure 25.</b>	SO-8 PC board for L5050SD	13
<b>Figure 26.</b>	$R_{thj-amb}$ vs PCB copper area in open box free air condition	14
<b>Figure 27.</b>	SO-8 thermal impedance junction ambient single pulse (L5050S)	14
<b>Figure 28.</b>	SO-8 thermal impedance junction ambient single pulse (one channel on for L5050SD)	14
<b>Figure 29.</b>	L5050S thermal fitting model of a $V_{reg}$ in SO-8	15
<b>Figure 30.</b>	L5050SD Thermal fitting model of a $V_{reg}$ in SO-8	15
<b>Figure 31.</b>	SO-8 package outline	17
<b>Figure 32.</b>	SO-8 recommended footprint (dimensions are in mm)	18
<b>Figure 33.</b>	SO-8 tape and reel shipment (suffix "TR")	19