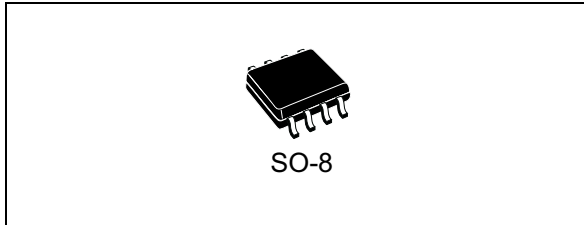


High voltage high and low-side driver

Datasheet - production data



Features

- High voltage rail up to 600 V
- dV/dt immunity ± 50 V/ns over full temperature range
- Driver current capability:
 - 290 mA source
 - 430 mA sink
- Switching times 75/35 ns rise/fall with 1 nF load
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Integrated bootstrap diode
- Internal 320 ns deadtime
- Interlocking function
- Compact and simplified layout
- Bill of material reduction
- Flexible, easy and fast design

Applications

- Home appliances
- Industrial applications and drives
- Motor drivers DC, AC, PMDC and PMAC motors systems
- HVAC
- Factory automation
- Power supply systems
- Compressors
- Fans
- Lighting applications

Description

The L6399 is a high voltage device manufactured using BCD™ “offline” technology. It is a single-chip half bridge gate driver for N-channel power MOSFETs or IGBTs.

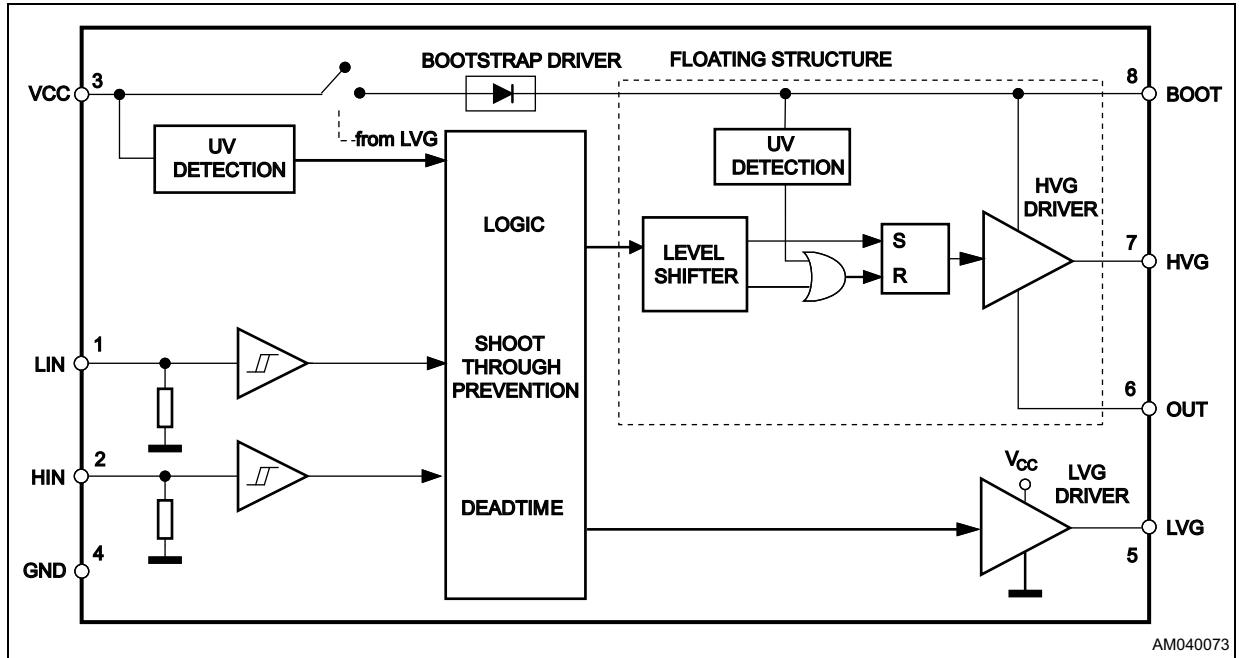
The high-side (floating) section is designed to withstand a voltage rail up to 600 V. The logic inputs are CMOS/TTL compatible down to 3.3 V for easy microcontroller/DSP interfacing.

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1 Block diagram

Figure 1. Block diagram



2 Electrical data

2.1 Absolute maximum ratings

Table 1. Absolute maximum rating

| Symbol | Parameter | Value | | Unit |
|-----------------------|--|------------------------|-------------------------|------|
| | | Min. | Max. | |
| V _{CC} | Supply voltage | -0.3 | 21 | V |
| V _{OUT} | Output voltage | V _{BOOT} - 21 | V _{BOOT} + 0.3 | V |
| V _{BOOT} | Bootstrap voltage | -0.3 | 620 | V |
| V _{hvg} | High-side gate output voltage | V _{OUT} - 0.3 | V _{BOOT} + 0.3 | V |
| V _{lvg} | Low-side gate output voltage | -0.3 | V _{CC} + 0.3 | V |
| V _i | Logic input voltage | -0.3 | 15 | V |
| dV _{OUT} /dt | Allowed output slew rate | - | 50 | V/ns |
| P _{tot} | Total power dissipation (T _A = 25 °C) | - | 800 | mW |
| T _J | Junction temperature | - | 150 | °C |
| T _{stg} | Storage temperature | -50 | 150 | °C |
| ESD | Human body model | 2 | | kV |

2.2 Recommended operating conditions

Table 2. Recommended operating conditions

| Symbol | Pin | Parameter | Test condition | Min. | Max. | Unit |
|--------------------------------|-------|-------------------------|-------------------------------------|---------------------|------|------|
| V _{CC} | 3 | Supply voltage | - | 10 | 20 | V |
| V _{BO} ⁽¹⁾ | 8 - 6 | Floating supply voltage | - | 9.8 | 20 | V |
| V _{OUT} | 6 | Output voltage | - | - 11 ⁽²⁾ | 580 | V |
| f _{sw} | - | Switching frequency | HVG, LVG load C _L = 1 nF | - | 800 | kHz |
| T _J | - | Junction temperature | - | -40 | 125 | °C |

1. V_{BO} = V_{BOOT} - V_{OUT}.

2. LVG off. V_{CC} = 10 V
Logic is operational if V_{BOOT} > 5 V.

2.3 Thermal data

Table 3. Thermal data

| Symbol | Parameter | SO-8 | Unit |
|---------------------|--|------|------|
| R _{th(JA)} | Thermal resistance junction to ambient | 150 | °C/W |

3 Pin connection

Figure 2. Pin connection (top view)

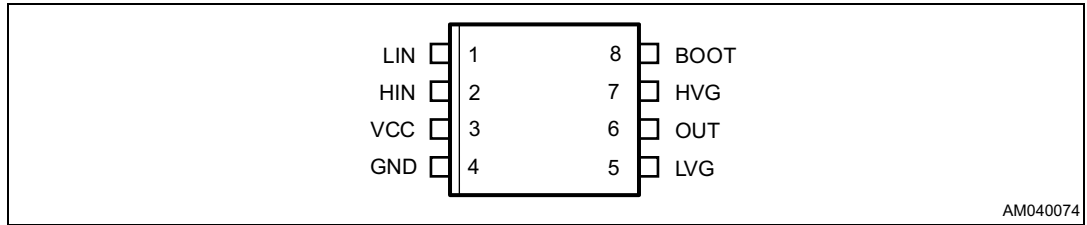


Table 4. Pin description

| Pin no. | Pin name | Type | Function |
|---------|--------------------|------|--|
| 1 | LIN | I | Low-side driver logic input (active high) |
| 2 | HIN | I | High-side driver logic input (active high) |
| 3 | VCC | P | Lower section supply voltage |
| 4 | GND | P | Ground |
| 5 | LVG ⁽¹⁾ | O | Low-side driver output |
| 6 | OUT | P | High-side (floating) common voltage |
| 7 | HVG ⁽¹⁾ | O | High-side driver output |
| 8 | BOOT | P | Bootstrapped supply voltage |

1. The circuit guarantees less than 1 V on the LVG and HVG pins (at $I_{\text{sink}} = 10 \text{ mA}$), with $V_{\text{CC}} > 3 \text{ V}$. This allows omitting the "bleeder" resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low.

4 Electrical characteristics

4.1 AC operation

Table 5. AC operation electrical characteristics ($V_{CC} = 15\text{ V}$; $T_J = +25\text{ °C}$)

| Symbol | Pin | Parameter | Test condition | | Min. | Typ. | Max. | Unit |
|-----------|------|--|--|-------------------------------------|------|------|------|------|
| t_{on} | 1, 2 | High/low-side driver turn-on propagation delay ⁽¹⁾ | $V_{OUT} = 0\text{ V}$ $V_{BOOT} = V_{CC}$ $C_L = 1\text{ nF}$ | $V_{IN} = 0\text{ to }3.3\text{ V}$ | 50 | 125 | 200 | ns |
| t_{off} | 5, 7 | High/low side driver turn-off propagation delay ⁽¹⁾ | | $V_{IN} = 3.3\text{ to }0\text{ V}$ | 50 | 125 | 200 | ns |
| DT | - | Deadtime ⁽²⁾ | $C_L = 1\text{ nF}$ | - | 225 | 320 | 415 | ns |
| t_r | 5, 7 | Rise time ⁽¹⁾ | $C_L = 1\text{ nF}$ | - | - | 75 | 120 | ns |
| t_f | | Fall time ⁽¹⁾ | $C_L = 1\text{ nF}$ | - | - | 35 | 70 | ns |

1. See [Figure 3](#)

2. See [Figure 4](#).

4.2 DC operation

Table 6. DC operation electrical characteristics ($V_{CC} = 15\text{ V}$; $T_J = +25\text{ °C}$)

| Symbol | Pin | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|--|------|---|--|------|------|------|------------------|
| Low supply voltage section⁽¹⁾ | | | | | | | |
| V_{CC_hys} | 3 | V_{CC} UV hysteresis | - | 1.2 | 1.5 | 1.8 | V |
| V_{CC_thON} | | V_{CC} UV turn-ON threshold | - | 9 | 9.5 | 10 | V |
| V_{CC_thOFF} | | V_{CC} UV turn-OFF threshold | - | 7.6 | 8 | 8.4 | V |
| I_{QCCU} | | Undervoltage quiescent supply current | $V_{CC} = 7\text{ V}$ $LIN = HIN = GND$ | - | 170 | 330 | μA |
| I_{QCC} | | Quiescent current | $V_{CC} = 15\text{ V}$ $LIN = HIN = GND$ | - | 380 | 440 | μA |
| Bootstrapped supply voltage section⁽¹⁾ | | | | | | | |
| V_{BO_hys} | 8 | V_{BO} UV hysteresis | - | 0.8 | 1 | 1.2 | V |
| V_{BO_thON} | | V_{BO} UV turn-ON threshold | - | 8.2 | 9 | 9.8 | V |
| V_{BO_thOFF} | | V_{BO} UV turn-OFF threshold | - | 7.3 | 8 | 8.7 | V |
| I_{QBOU} | | Undervoltage V_{BO} quiescent current | $V_{BO} = 7\text{ V}$, $LIN = GND$; $HIN = 5\text{ V}$ | - | 30 | 140 | μA |
| I_{QBO} | | V_{BO} quiescent current | $V_{BO} = 15\text{ V}$, $LIN = GND$; $HIN = 5\text{ V}$ | - | 190 | 240 | μA |
| I_{LK} | - | High voltage leakage current | $V_{hvg} = V_{OUT} = V_{BOOT} = 600\text{ V}$ | - | - | 10 | μA |
| $R_{DS(on)}$ | - | Bootstrap driver on resistance ⁽²⁾ | LVG ON | - | 120 | - | Ω |
| Driving buffers section | | | | | | | |
| I_{SO} | 5, 7 | High/low-side source short-circuit current | $V_{IN} = V_{ih}$ ($t_p < 10\text{ }\mu\text{s}$) | 200 | 290 | - | mA |
| I_{SI} | | High/low side sink short-circuit current | $V_{IN} = V_{il}$ ($t_p < 10\text{ }\mu\text{s}$) | 250 | 430 | - | mA |
| Logic inputs | | | | | | | |
| V_{il} | 1, 2 | Low level logic threshold voltage | - | 0.8 | - | 1.1 | V |
| V_{ih} | | High level logic threshold voltage | - | 1.9 | - | 2.25 | V |
| I_{INI} | | LIN/HIN logic "0" input bias current | $V_{IN} = 0\text{ V}$ | - | - | 1 | μA |
| I_{HINh} | 2 | HIN High logic level input current | $V_{IN} = 15\text{ V}$ | 110 | 175 | 260 | μA |
| R_{PD-HIN} | | HIN pull-down resistor | $V_{IN} = 15\text{ V}$ | 57 | 85 | 137 | $\text{k}\Omega$ |
| I_{LINh} | 1 | LIN High logic level input current | $V_{IN} = 15\text{ V}$ | 10 | 40 | 100 | μA |
| R_{PD-LIN} | | LIN pull-down resistor | $V_{IN} = 15\text{ V}$ | 150 | 375 | 1500 | $\text{k}\Omega$ |

1. $V_{BO} = V_{BOOT} - V_{OUT}$.

2. $R_{DS(on)}$ is tested in the following way: $R_{DS(on)} = [(V_{CC} - V_{BOOT1}) - (V_{CC} - V_{BOOT2})] / [I_1(V_{CC}, V_{BOOT1}) - I_2(V_{CC}, V_{BOOT2})]$ where I_1 is the pin 8 current when $V_{BOOT} = V_{BOOT1}$, I_2 when $V_{BOOT} = V_{BOOT2}$.

5 Timing and waveform definitions

Figure 3. Propagation delay timing definition

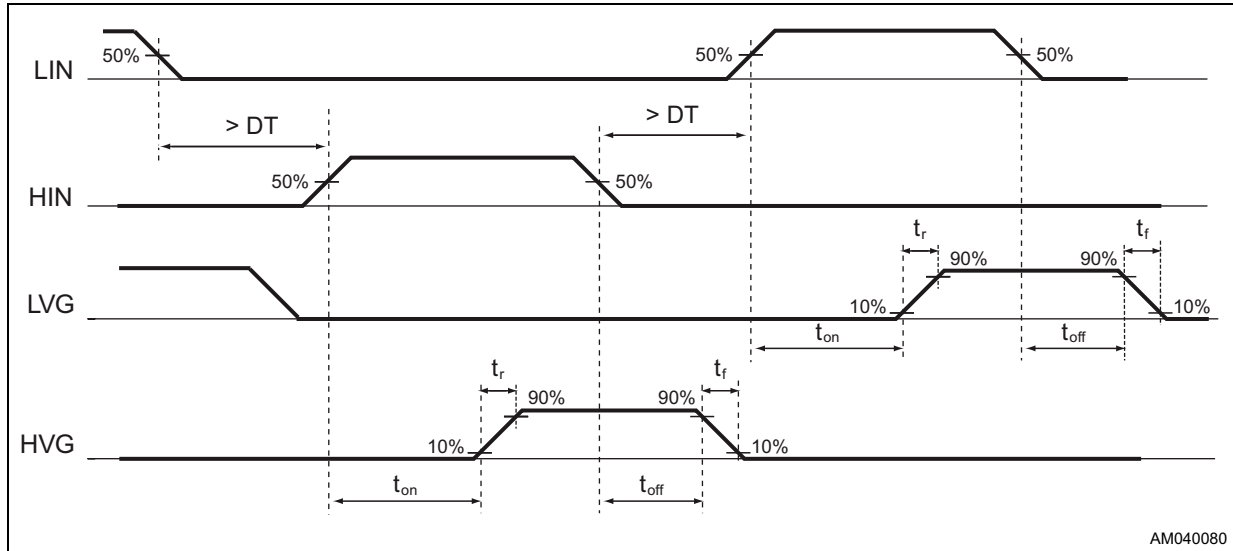


Figure 4. Deadtime and interlocking timing definition

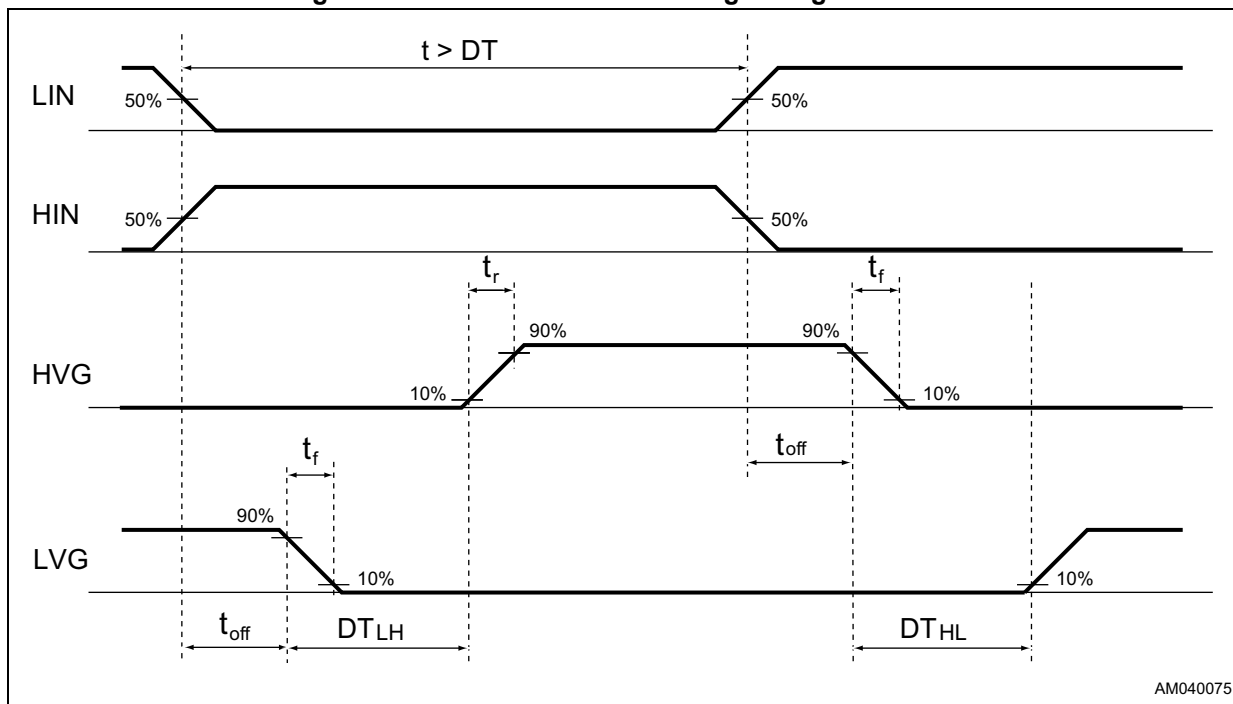
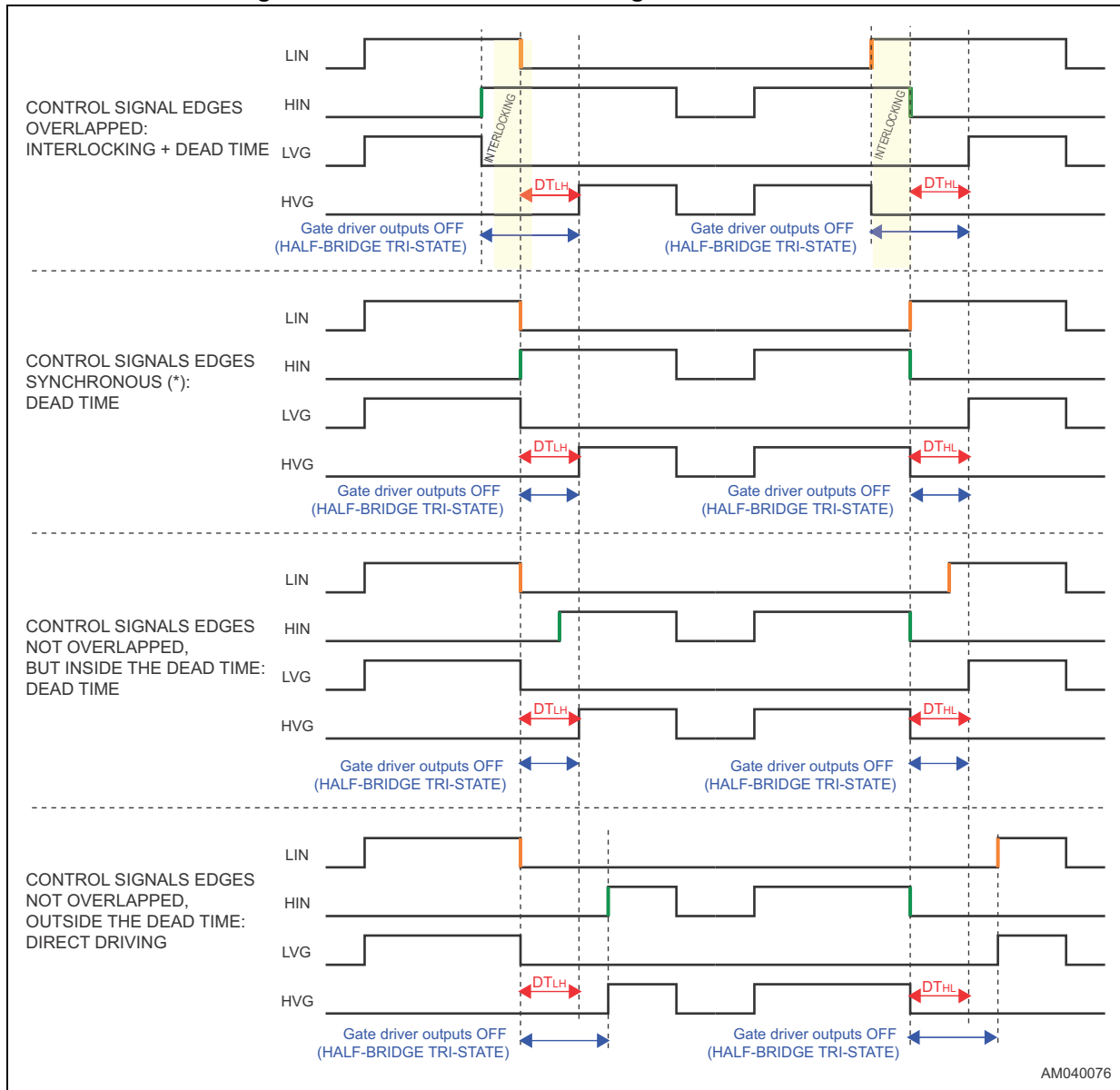


Figure 5. Deadtime and interlocking waveform definitions



6 Input logic

Table 7. Truth table

| Input | | Output | |
|-------|-----|------------------|------------------|
| LIN | HIN | LVG | HVG |
| L | L | L | L |
| L | H | L | H |
| H | L | H | L |
| H | H | L ⁽¹⁾ | L ⁽¹⁾ |

1. Interlocking function.

Input logic is provided with interlocking circuitry which prevents the two outputs (LVG, HVG) being active at the same time when both the logic input pins (LIN, HIN) are at a high logic level. In addition, to prevent cross-conduction of the external MOSFETs, after each output is turned off, the other output cannot be turned on before a certain amount of time (DT) (see [Figure 4: Deadtime and interlocking timing definition](#) and [Figure 5: Deadtime and interlocking waveform definitions](#)).

7 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode (*Figure 6*). In the L6399 device a patented integrated structure replaces the external diode. It is realized by a high voltage DMOS, driven synchronously with the low-side driver (LVG), with a diode in series, as shown in *Figure 7*. An internal charge pump (*Figure 7*) provides the DMOS driving voltage.

C_{BOOT} selection and charging

To choose the proper C_{BOOT} value the external MOS can be seen as an equivalent capacitor. This capacitor C_{EXT} is related to the MOS total gate charge:

Equation 1

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors C_{EXT} and C_{BOOT} is proportional to the cyclical voltage loss. It has to be:

Equation 2

$$C_{BOOT} \gg \gg C_{EXT}$$

E.g.: if Q_{gate} is 30 nC and V_{gate} is 10 V, C_{EXT} is 3 nF. With $C_{BOOT} = 100$ nF the drop would be 300 mV.

If HVG has to be supplied for a long time, the C_{BOOT} selection has to take into account also the leakage and quiescent losses.

E.g.: HVG steady state consumption is lower than 190 μ A, so if HVG T_{ON} is 5 ms, C_{BOOT} has to supply C_{EXT} with 1 μ C. This charge on a 1 μ F capacitor means a voltage drop of 1 V.

The internal bootstrap driver gives a great advantage: the external fast recovery diode can be avoided (it usually has a high leakage current).

This internal diode can work only if V_{OUT} is close to GND (or lower) and in the meanwhile the LVG is on. The charging time (T_{charge}) of the C_{BOOT} is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the equivalent resistance of the internal diode R_{DSon} (typical value: 120 Ω). At low frequency this drop can be neglected. Anyway increasing the frequency it must be taken in to account.

The following equation is useful to compute the drop on the bootstrap DMOS:

Equation 3

$$V_{drop} = I_{charge} \cdot R_{BOOT} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}} \cdot R_{DSon}$$

where Q_{gate} is the gate charge of the external power MOS.

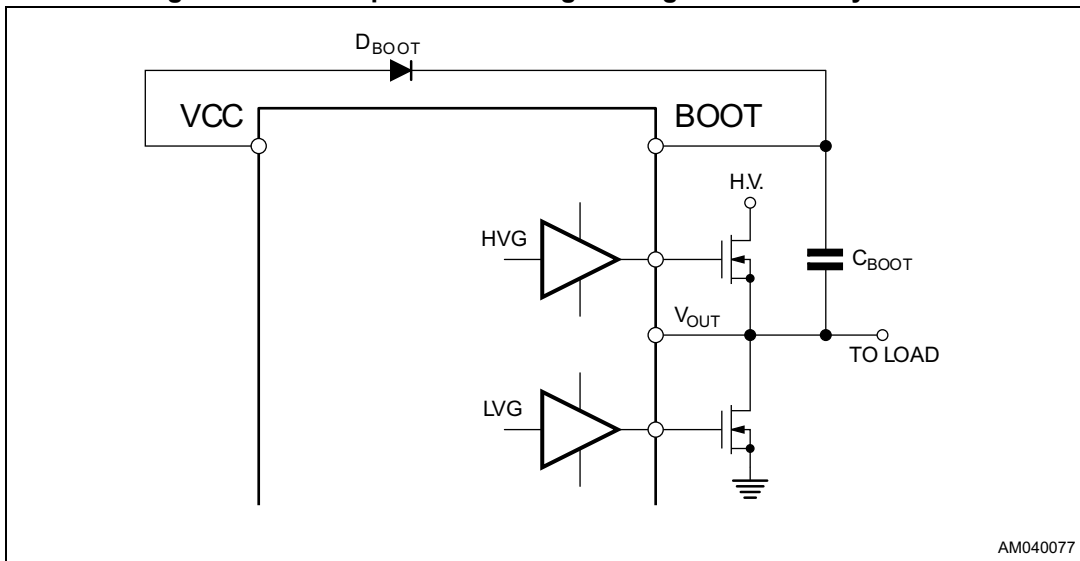
For example: using a power MOS with a total gate charge of 30 nC the drop on the bootstrap diode is about 1 V, if the T_{charge} is 5 μs . In fact:

Equation 4

$$V_{drop} = \frac{30nC}{5\mu s} \cdot 120\Omega \sim 0.72V$$

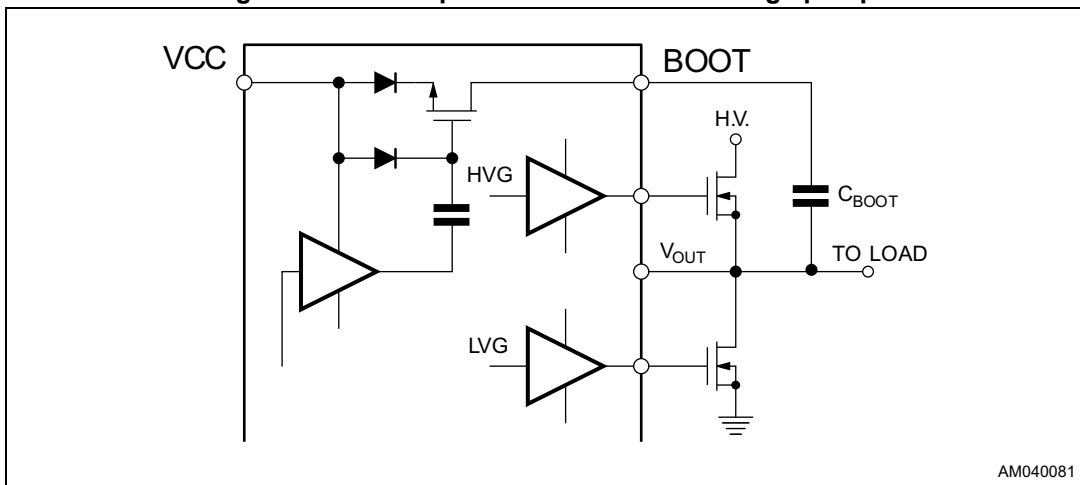
V_{drop} has to be taken into account when the voltage drop on C_{BOOT} is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

Figure 6. Bootstrap driver with high voltage fast recovery diode



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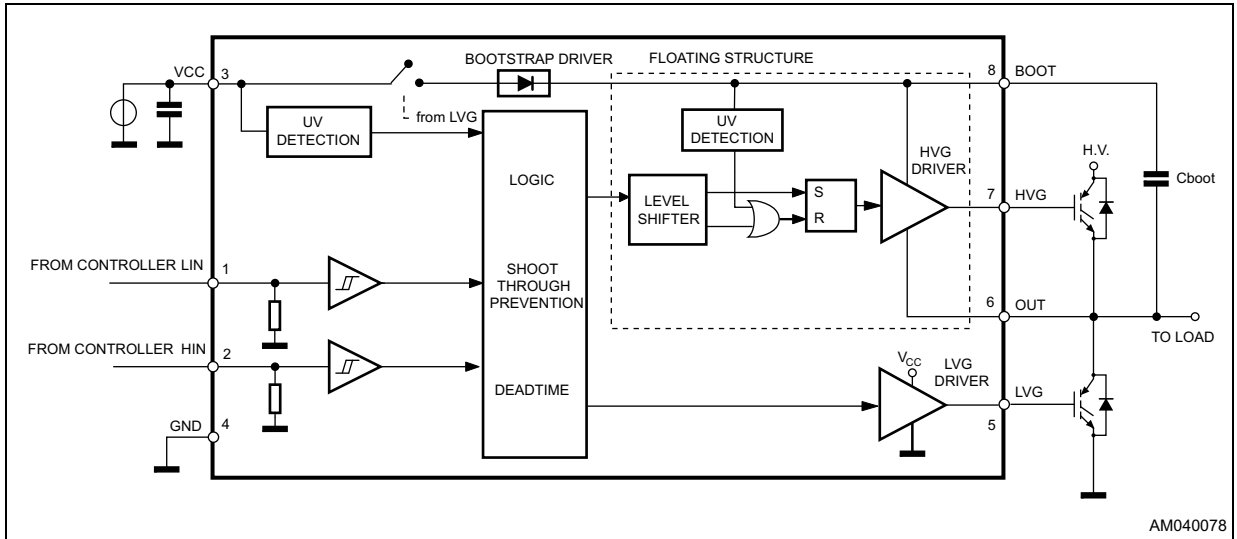
Figure 7. Bootstrap driver with internal charge pump



AM040081

8 Typical application diagram

Figure 8. Typical application schematic



9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 SO-8 package information

Figure 9. SO-8 package outline

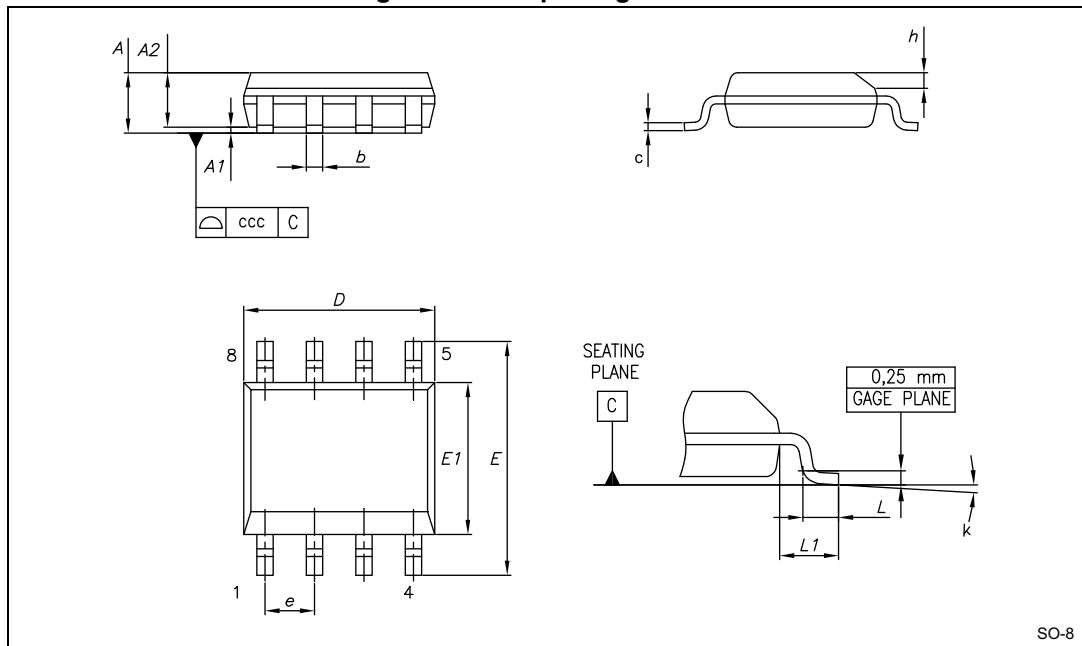
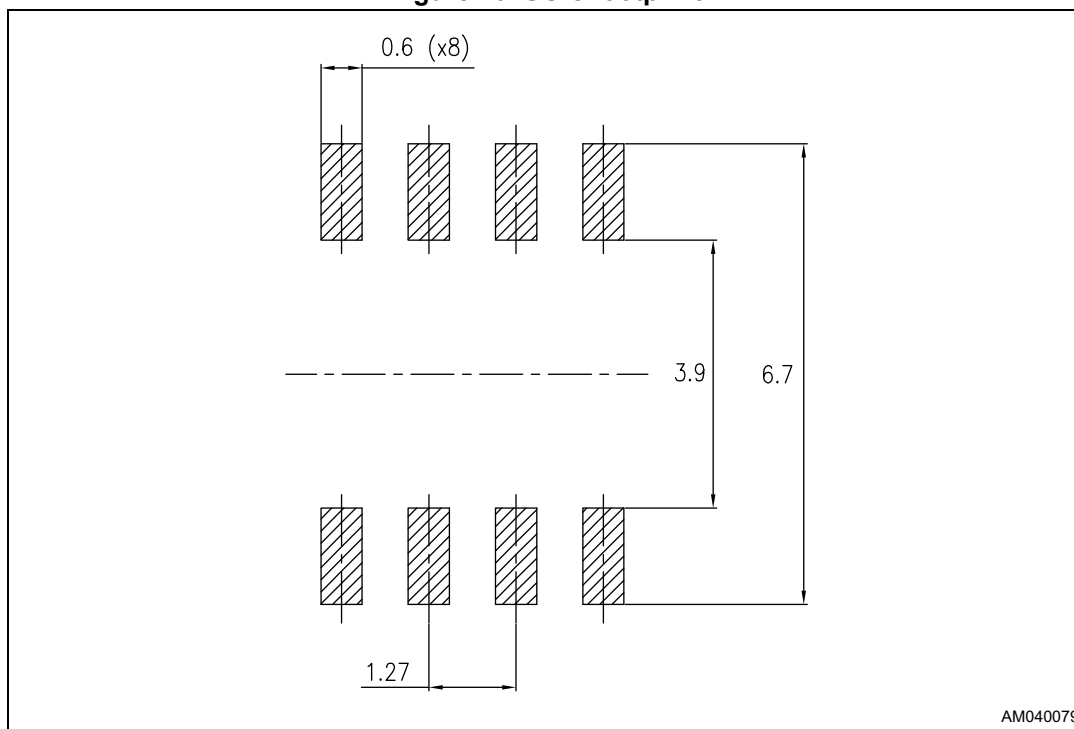


Table 8. SO-8 package mechanical data

| Symbol | Dimensions (mm) | | | Note |
|--------|------------------|------|------|------|
| | Min. | Typ. | Max. | |
| A | - | - | 1.75 | - |
| A1 | 0.10 | - | 0.25 | - |
| A2 | 1.25 | - | - | - |
| b | 0.28 | - | 0.48 | - |
| c | 0.17 | - | 0.23 | - |
| D | 4.80 | 4.90 | 5.00 | (1) |
| E | 5.80 | 6.00 | 6.20 | - |
| E1 | 3.80 | 3.90 | 4.00 | (2) |
| e | - | 1.27 | - | - |
| h | 0.25 | - | 0.50 | - |
| L | 0.40 | - | 1.27 | - |
| L1 | - | 1.04 | - | - |
| k | 0 | - | 8 | (3) |
| ccc | - | - | 0.10 | - |

1. The dimension "D" does not include the mold flash, protrusions or gate burrs. The mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both sides).
2. The dimension "E1" does not include the interlead flash or protrusions. The interlead flash or protrusions shall not exceed 0.25 mm per side.
3. Degrees.

Figure 10. SO-8 footprint



AM040079

10 Order codes

Table 9. Order codes

| Order codes | Package | Packaging |
|-------------|---------|---------------|
| L6399D | SO-8 | Tube |
| L6399DTR | SO-8 | Tape and reel |

11 Revision history

Table 10. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 03-Mar-2017 | 1 | Initial release. |
| 27-Mar-2017 | 2 | Updated document status to: Datasheet - production data on page 1 . |