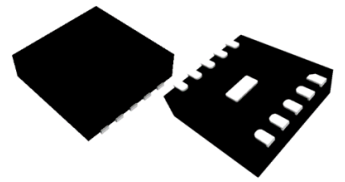
L7983

Datasheet

60 V, 300 mA synchronous step-down switching regulator with 10 µA quiescent current



DFN10 3 x 3

Maturity status link
L7983

Features

- 3.5 V to 60 V operating input voltage
- Fixed output voltage (3.3 V and 5 V) or adjustable from 0.85 V to V_{IN}
- 300 mA DC output current
- Dynamic low consumption mode to low noise mode selection
- 10 µA operating quiescent current (L7983PU33R, V_{IN} > 24 V, LCM)
- 2.3 µA shutdown current
- 200 kHz to 2.2 MHz programmable switching frequency
- Optional spread spectrum (dithering)
- Internal soft-start
- Enable / adjustable UVLO threshold
- Synchronization to external clock
- Internal compensation network
- Internal current limiting
- Overvoltage protection
- Output voltage sequencing
- Thermal shutdown

Applications

- Designed for 12 V, 24 V and 48 V buses
- Battery powered applications
- Decentralized intelligent nodes
- Fail safe system
- Sensors and low noise applications (LNM)

Description

The L7983 device is a step-down monolithic switching regulator able to deliver up to 300 mA DC based on peak current mode architecture.

The output voltage adjustability ranges from 0.85 V to V_{IN}. The wide input voltage range and adjustable UVLO threshold meet the specification for the 12 V, 24 V and 48 V industrial bus standards.

The “Low Consumption Mode” (LCM) is designed for applications active during idle mode, so it maximizes the efficiency at light load with controlled output voltage ripple. The “Low Noise Mode” (LNM) makes the switching frequency constant overload current range, meeting the low noise application specification. The L7983 supports dynamic LCM to LNM transition.

The soft-start time is internally fixed and the output voltage supervisor manages the reset phase for any digital load (microcontroller, FPGA, etc.).

The internal compensation network features high noise immunity, simple design and saves on the component cost.

The RST open collector output can also implement output voltage sequencing during the power-up phase.

The synchronous rectification, designed for high efficiency at medium - heavy load, and the high switching frequency capability make the size of the application compact.

Pulse-by-pulse current sensing on both power elements implements an effective constant current protection.

1 Application schematic and block diagram

1.1 Application circuit

Figure 1. Typical application circuit

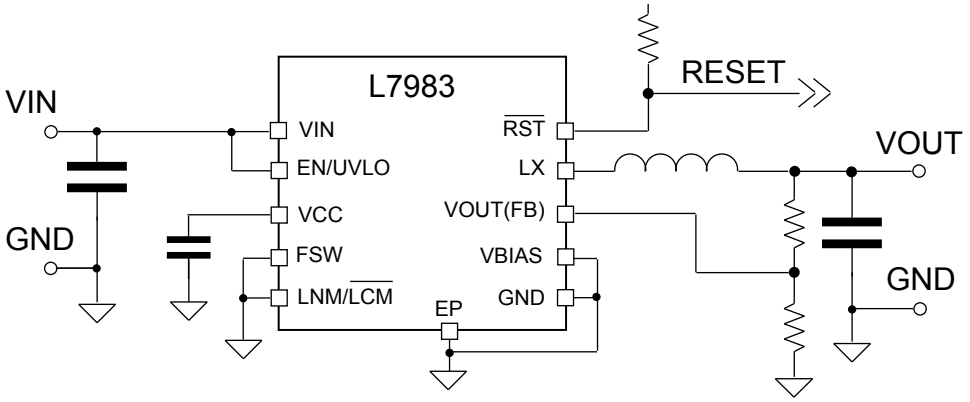
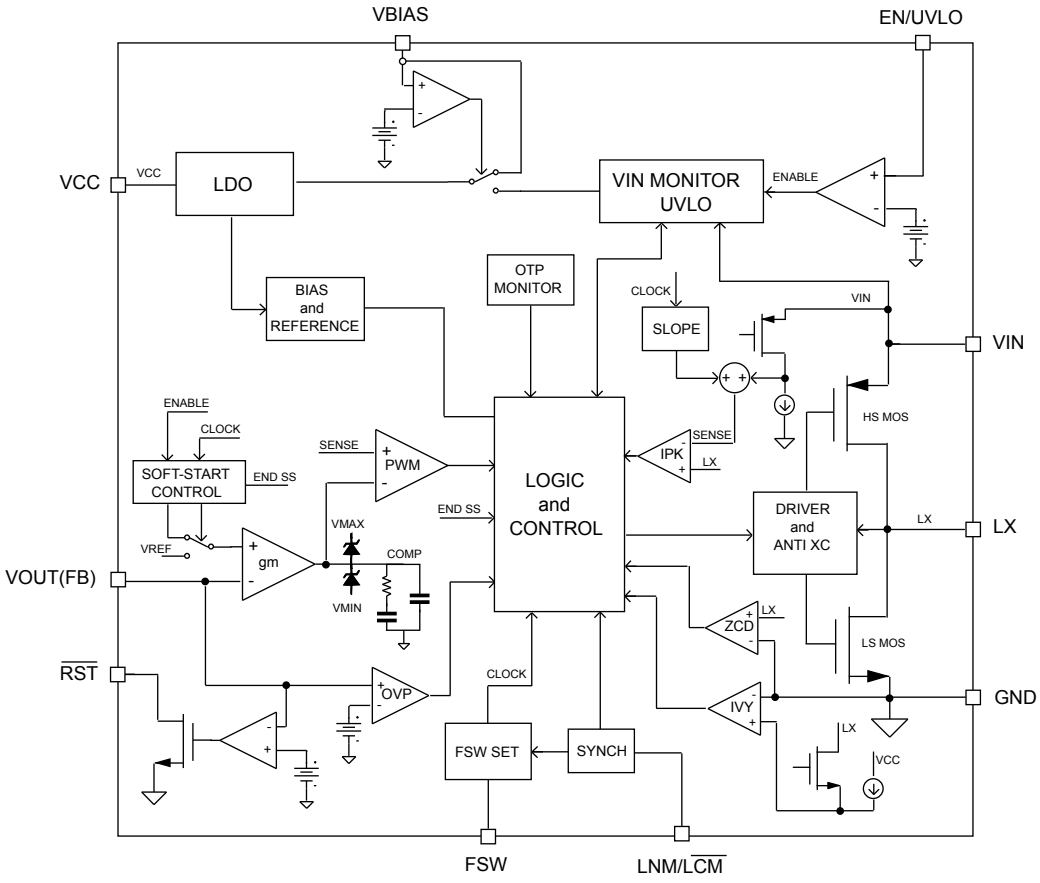


Figure 2. Block diagram



2 Pin settings

Figure 3. **Pin connection (top view)**

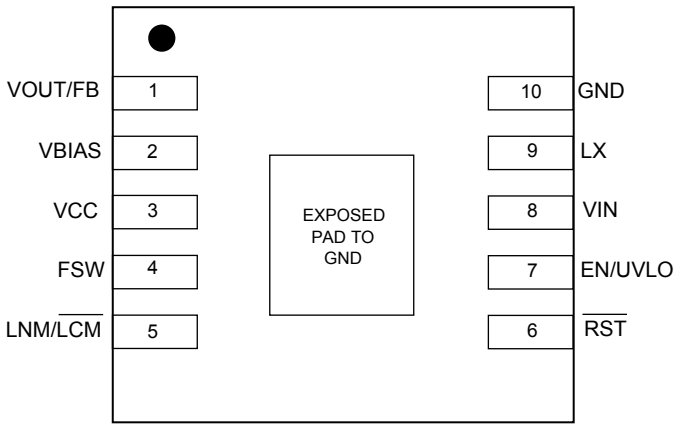


Table 1. **Pin description**

N°	Pin	Description
1	VOUT/FB	Output voltage sensing. This pin operates as VOUT or FB accordingly with selected part number: • VOUT is output voltage sensing with selected internal voltage divider. • FB is output voltage sensing with external resistor divider.
2	VBIAS	Input supply of the integrated LDO. Typically connected to the regulated output voltage or an auxiliary rail to increase the efficiency at light load. Connect to GND if not used or bypass with a 100 nF ceramic capacitor if supplied by the output voltage or by an auxiliary rail.
3	VCC	Output of the integrated LDO that supplies the embedded analog circuitry. Connect a ceramic capacitor (470 nF typ.) to filter internal voltage reference.
4	FSW	Switching frequency programming pin. Connect an external resistor to VCC or GND.
5	LNM/$\overline{\text{LCM}}$	Dynamic pin selection between Low Consumption Mode (LCM, active low) and Low Noise Mode operation (LNM, active high). This pin can also be used for synchronization with an external clock (clock-in function).
6	$\overline{\text{RST}}$	Active low open collector output for output monitoring and power-up reset sequencing. RST is driven in low impedance when the output voltage is out of regulation and released once the output voltage becomes valid.
7	EN/UVLO	Active high enable pin, VIN compatible. It can be exploited with an external resistor divider to adjust the input undervoltage lockout (UVLO).
8	VIN	DC input voltage
9	LX	Switching node
10	GND	Ground
--	E.P.	Exposed pad must be connected to GND

3 Absolute maximum ratings

Stressing the device above the ratings listed in Table 2 may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute maximum ratings

Symbol	Description	Min.	Max.	Unit
VIN	See Table 1	-0.3	63	V
V_{CC}		-0.3	VIN + 0.3 or max. 3.6	V
EN/UVLO		-0.3	VIN + 0.3	V
$\overline{RST}$				V
LX		-0.3	VIN + 0.3	V
VBIAS		-0.3	VIN + 0.3 or max. 14	V
VOUT/FB		-0.3	5.5	V
LNM/$\overline{LCM}$				V
FSW		-0.3	VCC + 0.3	V
I_{HS}, I_{LS}	High-side / low-side RMS switch current		0.3	A
T_J	Operating temperature range	-40	150	°C
T_{STG}	Storage temperature range	-65	150	
T_{LEAD}	Lead temperature (soldering 10 sec.)		260	

3.1 Thermal characteristics

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient (device soldered on a standard demonstration board)	50	°C/W

3.2 ESD protection

Table 4. ESD performance

Symbol	Test conditions	Value	Unit
ESD	HBM	2	kV
	CDM	500	V

3.3 Operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
V_{IN}	Power supply voltage	3.5		60	V
V_{BIAS}		0		14	V

4 Electrical characteristics

T_J = 25 °C, V_{IN} = 24 V, $V_{EN/UVLO}$ = V_{IN}, LNM selected, f_{SW} = 1 MHz unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Turn on and power section characteristics						
V_{INH}	V_{IN} turn-on	VIN rising	2.6	2.8	3.0	V
V_{INL}	V_{IN} turn-off	VIN falling	2.5	2.7	2.9	
		Hysteresis		0.1		
$V_{WAKEUPH}$	Wake-up ON threshold	V_{EN} rising			0.7	V
$V_{WAKEUPL}$	Wake-up OFF threshold	V_{EN} falling	0.2			
V_{ENH}	Enable ON threshold	V_{EN} rising	1.1	1.2	1.3	
V_{ENL}	Enable OFF threshold	V_{EN} falling	0.9	1.0	1.1	
		Hysteresis		0.2		
I_{PK}	Peak current limit	Duty cycle < 20% (1)	0.42	0.47	0.52	A
		Duty cycle = 100%, closed loop operation (1)	0.35	0.39	0.43	
I_{VY}	Valley current limit	(1)	0.43	0.52	0.61	
I_{SKIP}	Skip current limit	(1)		0.08		
I_{NEG}	Reverse current limit	LNM selected, VFB = 0.9 V (1)		- 0.15		
HS R_{DSON}	HS MOS ON resistance	I_{LX} = 0.2 A		1.9	2.5	Ω
LS R_{DSON}	LS MOS ON resistance	I_{LX} = 0.2 A		0.85	1.2	
f_{SW}	Selected switching frequency	R_{FSW} = 5.6 kΩ	450	500	550	kHz
		R_{FSW} = 0 Ω	900	1000	1100	
		R_{FSW} = 56 kΩ	1980	2200	2420	
D	Duty cycle		0		100	%
$t_{ON\ MIN}$	Minimum HS MOS on-time			60		ns
t_{SS}	Internal soft-start time		1.3	2	2.7	ms
VCC and VBIAS						
V_{CC}	LDO output voltage	VBIAS = GND	2.9	3.3	3.6	V
		VBIAS = 5 V	2.9	3.3	3.6	
SWO	Switchover threshold	VBIAS increasing		3.2		V
		Hysteresis		0.075		V
Power consumption						
I_{SHTDWN}	Shutdown current from VIN	$V_{EN/UVLO}$ = GND		2.3	3.2	µA
I_{QVIN}	Quiescent current from VIN, LCM (refer to Section 5.5 VCC and switchover)	VBIAS = 5 V, VOUT = 1.05 * V_{REF} (2)		3	6	
		VBIAS = GND, VOUT = 1.05 * V_{REF} (2)		35	50	
	Quiescent current from VIN, LNM	VBIAS = 5 V, VOUT = 1.05 * V_{REF}		170	205	
		VBIAS = GND, VOUT = 1.05 * V_{REF}		1300	1500	

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{QVBIAS}	Quiescent current from VBIAS	LCM, VBIAS = 5 V, VOUT = 1.05 * V_{REF} (2)		37	50	µA
		LNM, VBIAS = 5 V, VOUT = 1.05 * V_{REF}		1200	1400	
Voltage reference and OVP						
V_{REF}	Voltage feedback, L7983PUR	T_J = 25 °C	0.844	0.850	0.856	V
		-40 °C ≤ T_J ≤ 125 °C (3)	0.840	0.850	0.860	
	Voltage feedback, L7983PU33R	T_J = 25 °C	3.267	3.300	3.333	
		-40 °C ≤ T_J ≤ 125 °C (3)	3.250	3.300	3.350	
	Voltage feedback, L7983PU50R	T_J = 25 °C	4.950	5.000	5.050	
		-40 °C ≤ T_J ≤ 125 °C (3)	4.925	5.000	5.075	
V_{OVP}	Overvoltage trip (V_{OUT}/V_{REF})		115	120	125	%
$V_{OVP,HYST}$	Overvoltage hysteresis			2		%
Synchronization (clock-in) and LNM/LCM						
f_{CLKIN}	Synchronization range		180		2400	kHz
V_{CLKINH}	CLKIN allowed high level		2		5	V
V_{CLKINL}	CLKIN allowed low level		0		1.3	V
V_{LNM}	LNM selection level		2		5	V
V_{LCM}	LCM selection level		0		1.3	V
$T_{LNM/LCM}$	Minimum allowed delay between LNM to LCM or LCM to LNM dynamic selection			14		µs
Reset						
V_{RSTTHR}	RST release threshold (V_{OUT}/V_{REF})	T_J = 25 °C	90	92	94	%
		-40 °C ≤ T_J ≤ 125 °C (3)	88		96	
$V_{RSTHYST}$	RST hysteresis			2		
T_{RSTDLY}	Delay from V_{RSTTHR} threshold detection and RST pin release			2.0		ms
V_{RSTLOW}	RST open collector output	V_{OUT}/V_{REF} = 80%, 4 mA sinking current		0.3	0.4	V
		2 < V_{IN} < V_{INH}, 4 mA sinking current		0.5	0.8	
I_{RSTLKG}	RST leakage current	V_{IN} = 60 V, V_{OUT}/V_{REF} = 110%			0.2	µA
Thermal shutdown						
T_{SHDWN}	Thermal shutdown threshold	(4)		165		°C
T_{HYS}	Thermal shutdown hysteresis	(4)		30		

1. *Parameter tested in static condition during testing phase. Parameter value may change over dynamic application condition.*
2. *LCM enables SLEEP mode at light load.*
3. *Specifications in the -40 to +125 °C temperature range are assured by characterization and statistical correlation.*
4. *Not tested in production.*

5 Functional description

The L7983 device is a monolithic step-down (“buck”) DC-DC voltage regulator based on a peak current mode, constant frequency architecture, with integrated control loop compensation network.

The main internal blocks are shown in Figure 2 and can be summarized as follows:

- Power section, including high-side and low-side power MOSFETs, gate driver and current sensing
- Control loop blocks, including the trans-conductor (gm), the PWM comparator and the slope generator
- The control logic for low noise mode (LNM) or low consumption mode (LCM) operation selection and synchronization to external clock
- The frequency programming circuitry for device configuration
- Input voltage monitor and enable circuit with soft-start management and RST output signal for sequencing programming
- The low drop-out linear regulator (LDO) and switchover block to improve the power conversion efficiency. The fault management, including the overcurrent (OCP), the overvoltage (OVP) and overtemperature (OTP) protection

5.1 Power section

The L7983 integrates both power MOSFETs for synchronous operation; one P-channel (high-side, HS) and one N-channel (low-side, LS), optimized for fast switching transition and high efficiency over the entire load range. The power stage is designed to deliver a continuous output current up to 0.3 A.

The HS MOSFET source is connected to the VIN pin, the LS MOSFET source is connected to the GND pin (power ground). The HS MOSFET drain and LS MOSFET drain are connected together and to the LX pin (see Figure 2).

The L7983 embodies an anti-shoot-through and adaptive deadtime control to minimize low-side body diode conduction time and consequently reduce power losses. This feature is implemented by comparing LX with HS and LS gate driving voltage.

- Following the HS turn-off, the LS MOSFET is suddenly switched on as soon as the voltage at the LX pin drops
- Following the LS turn-off, the HS MOSFET is suddenly switched on as soon as the gate driving voltage of LS drops

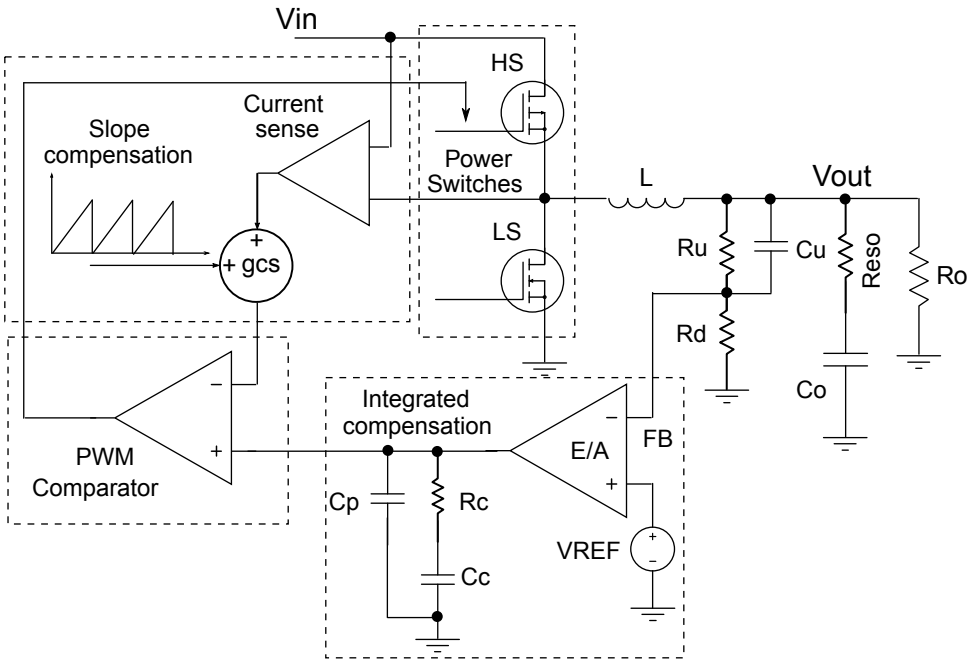
If the current flowing in the inductor is negative (i.e. from VOUT to VIN), the voltage on the LX pin can’t drop after HS MOS turn-off. A watchdog controller is implemented to allow the LS MOSFET to turn on even in this case, allowing the negative current of the inductor to flow to ground. This mechanism allows the system to regulate even if the current is negative (if LNM mode is enabled).

5.2 Control loop and voltage programming

The L7983 is based on a constant frequency peak current mode architecture.

Thanks to integrated compensation network and slope generation, no additional external components are necessary for loop stabilization.

Figure 4. Control loop block diagram



Refer to Section 5.7 for further details on power components design.

For the adjustable version (L7983PUR), the output voltage can be programmed through an external resistor divider, from 0.85 V up to VIN.

The design equation is:

$$V_{OUT} = 0.85 \cdot \left(1 + \frac{R_U}{R_D}\right) \quad (1)$$

For the fixed version (L7983PU33R or L7983PU50R), the output voltage programming is achieved by simply shorting the VOUT(FB) pin to the output capacitor.

Figure 5. **Output voltage programming - adjustable version**

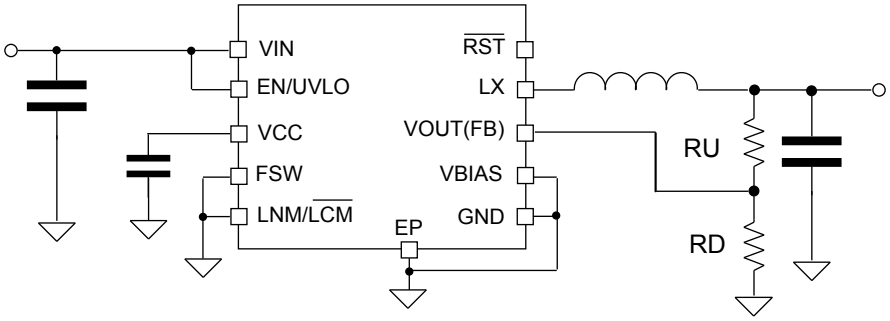
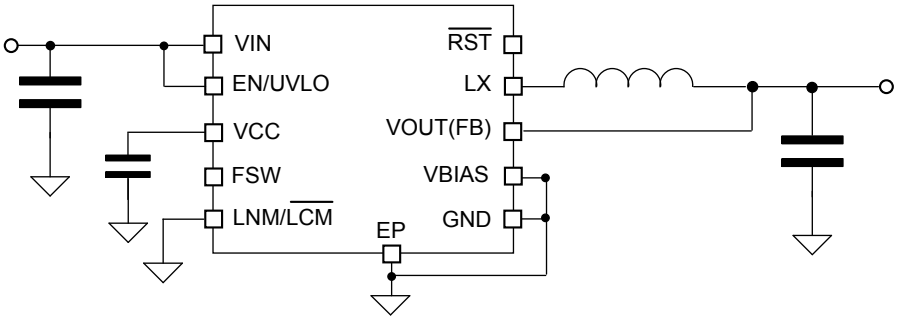


Figure 6. **Output voltage programming - fixed version**

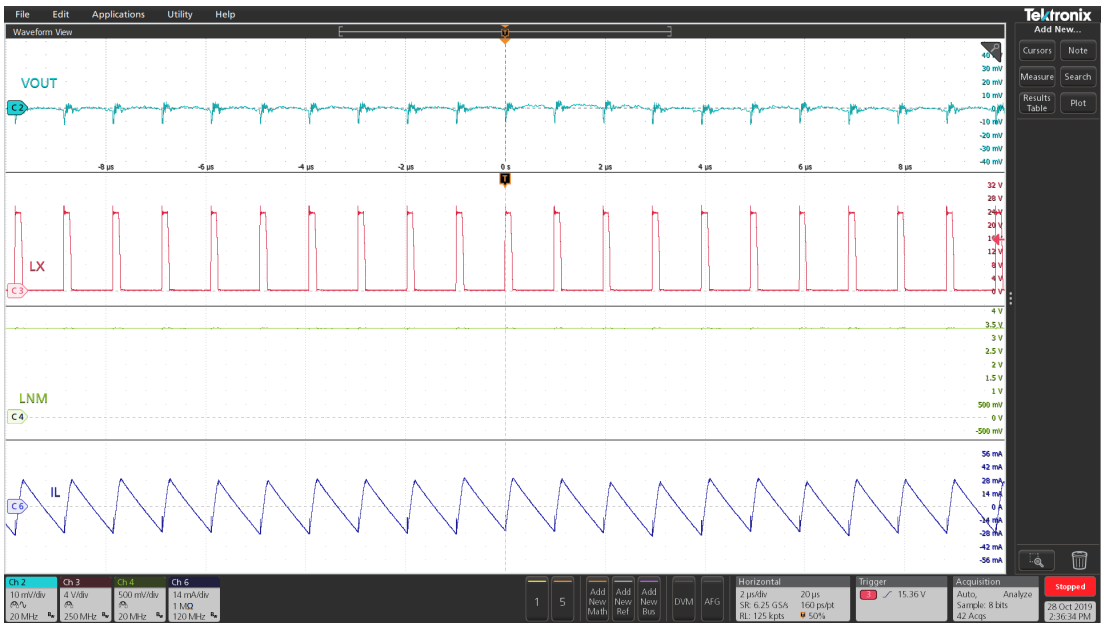


5.2.1 LNM/LCM selection and synchronization

Depending on the low-side power MOSFET management, the inductor current can be allowed to reverse or not. The choice can be performed during device operation by acting on the LNM/LCM pin.

When the low-noise mode (LNM) operation is selected, by forcing high pin LNM/LCM, the inductor current can reverse. In this way a constant switching frequency is achieved, so limiting the output voltage ripple and providing a prompt transient response.

Figure 7. LNM selected, no load



If the LNM/LCM pin is forced low, the low-consumption mode (LCM) is activated, with the aim of maximizing the light load efficiency. When LCM is selected, the high-side MOSFET is turned on as soon as the FB pin is sensed lower than V_{REFLCM}, i.e. V_{REF} reference voltage increased by 2% typ.:

$$V_{REFLCM} = V_{REF} \cdot 1{,}02(typ.) \quad (2)$$

In LCM mode the HS MOS is turned on until ISKIP current is reached, then it is turned-off. The low-side MOSFET is then turned on until one of the following conditions occurs:

- The sensed inductor current drops to zero
- The switching period (programmed through the FSW pin) has expired and the FB pin is still lower than the voltage reference. In this case a new switching cycle is performed.

In LCM working mode the regulator switching frequency is load-dependent (i.e. LX pulses can be skipped) with greater advantage to power conversion efficiency at light load.

The following waveforms are showing the switching activity in LCM working mode and different load.

Figure 8. **LCM selected, no load**

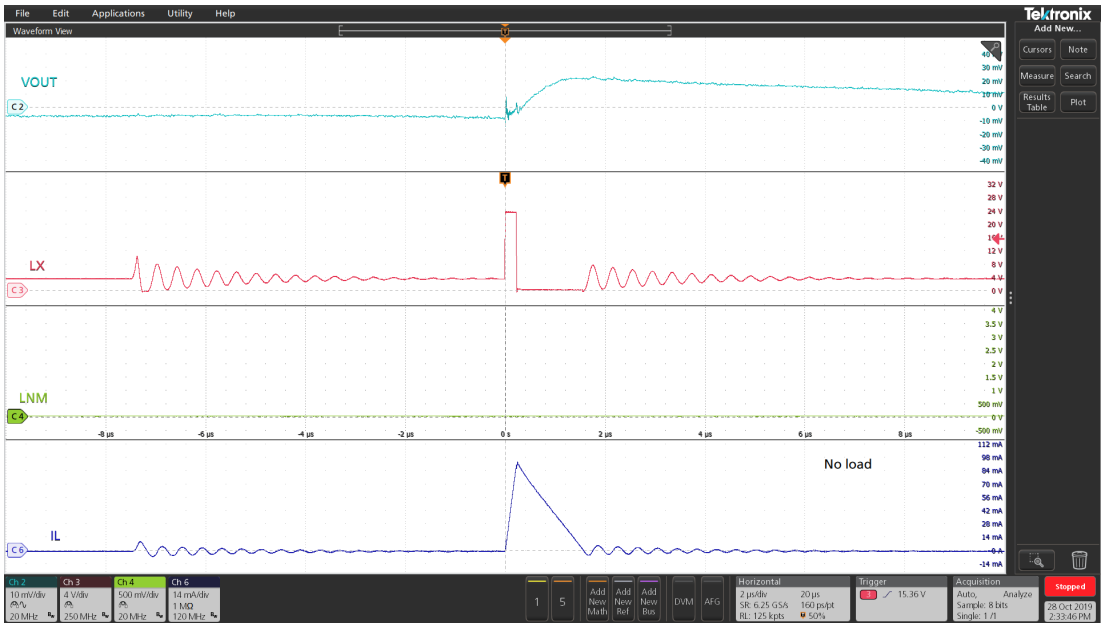


Figure 9. **LCM selected, 10 mA load**

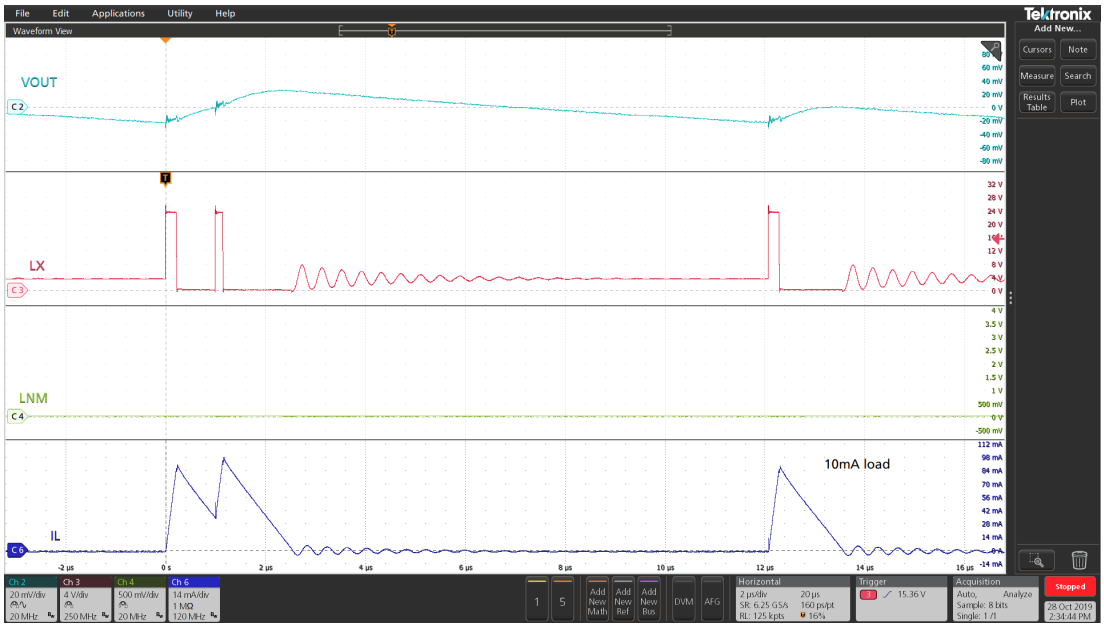
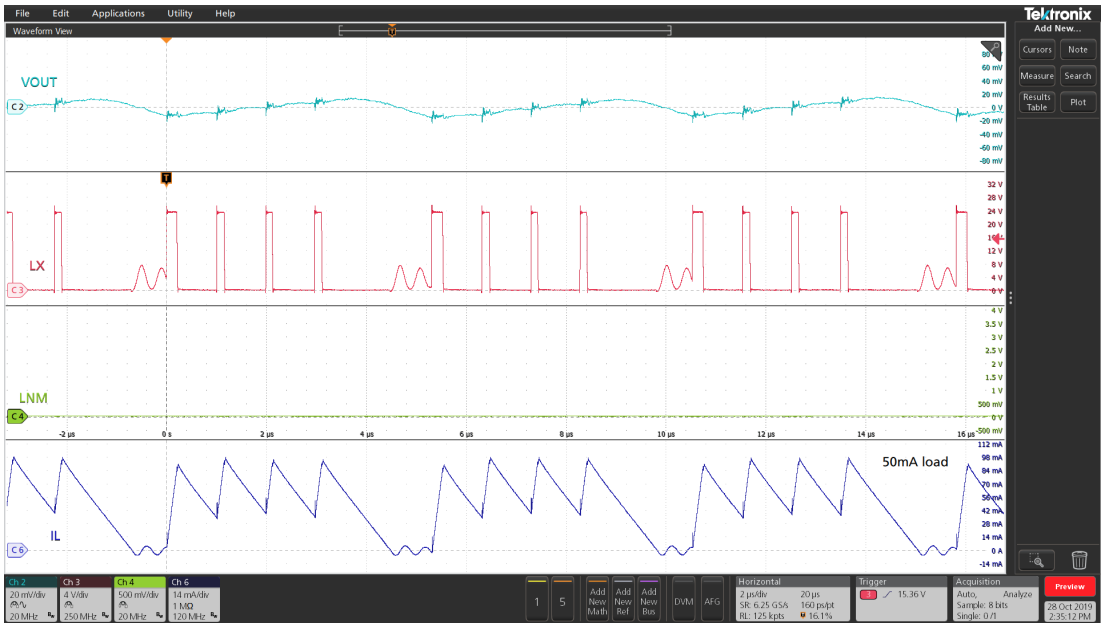


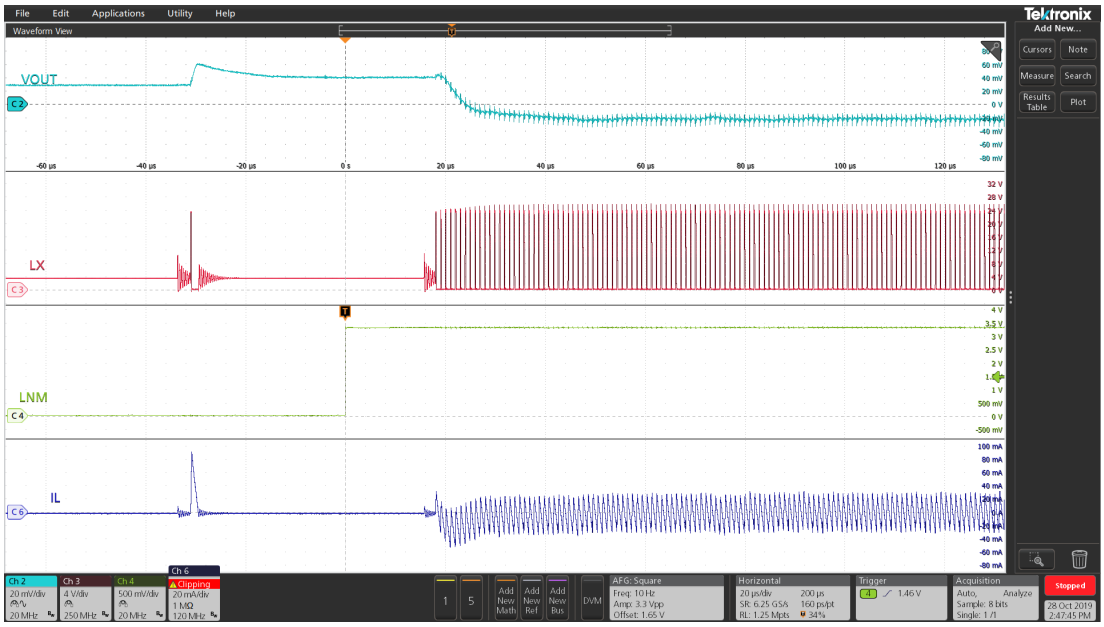
Figure 10. **LCM selected, 50 mA load**



If an external clock is applied on the LNM/LCM pin, the L7983 switching activity is synchronized to the applied clock and the LNM operation is enabled. The external clock must meet the electrical requirements summarized in Table 7. In case no external clock is detected on LNM/LCM for $T_{LNM/LCM}$ (14 µs typ.), the free running clock programmed on pin FSW through RFSW resistor is restored as switching frequency. Refer to Section 5.3 Switching frequency programming and dithering.

$T_{LNM/LCM}$ is also the typical delay between LNM to LCM and the opposite transition.

Figure 11. **LCM to LNM transition, no load**



5.3 Switching frequency programming and dithering

The L7983 has one programming pin, FSW (pin 4), which is used to set the regulator free running switching frequency.

The switching frequency programming feature is performed by selecting the proper 1% accuracy resistor, to be mounted between pin 4 and ground or VCC, as summarized in the following table. The pinstrapping is active only before the soft-start phase to minimize the IC consumption.

Refer also to Figure 1 for reference schematic.

Table 7. FSW pin programming resistor

	Dithering enabled				Dithering disabled			
#	RVCC [kΩ]	RGND [kΩ]	Fsw [kHz] (1)		#	RVCC [kΩ]	RGND [kΩ]	Fsw [kHz] (1)
1	0	--	1000		**1**	--	0	1000
2	1,8	--	200		**2**	--	1,8	200
3	3,3	--	400		**3**	--	3,3	400
4	5,6	--	500		**4**	--	5,6	500
5	10	--	700		**5**	--	10	700
6	18	--	1500		**6**	--	18	1500
7	33	--	2000		**7**	--	33	2000
8	56	--	2200		**8**	--	56	2200

1. *Typical value. Refer to Table 6 for details.*

The dithering function, enabled by connecting the proper R_{FSW} resistor to VCC, is intended to reduce the DC-DC electromagnetic emissions, with small impact on output voltage ripple.

Figure 12. RVCC = 0 Ω, dithering enabled, no load

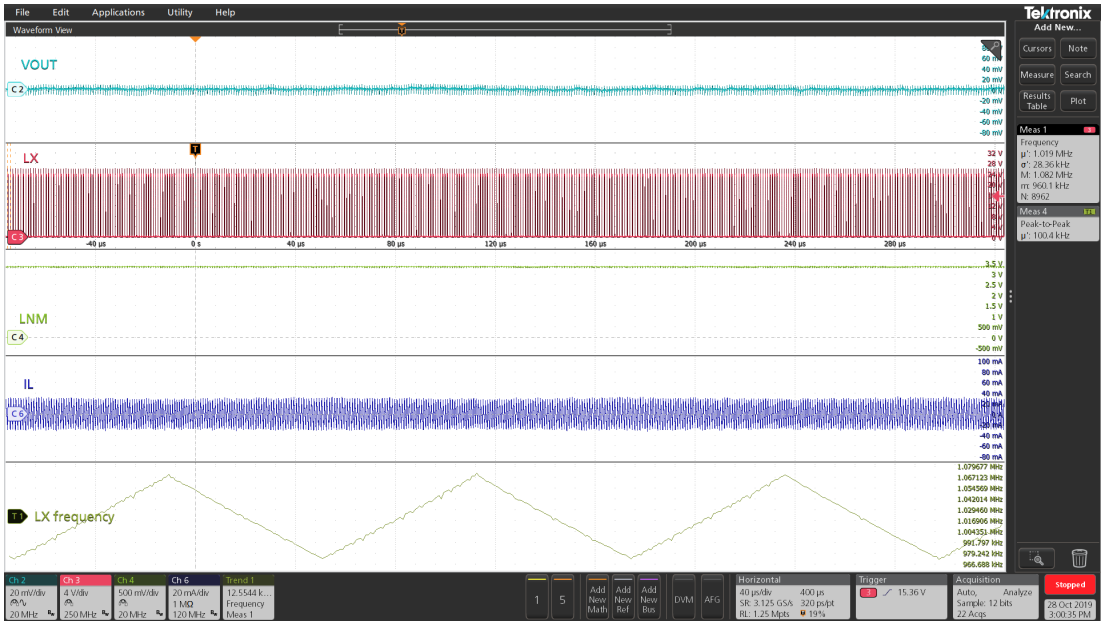
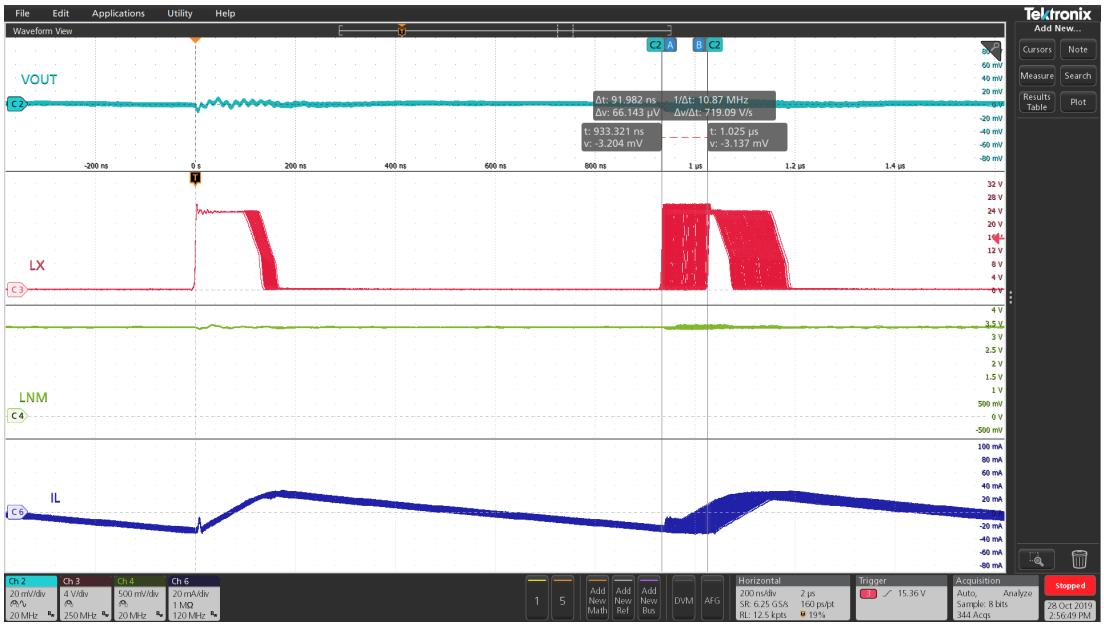


Figure 13. RVCC = 0 Ω, dithering enabled, no load. Detail



The internal dithering circuitry changes the switching frequency in the range of ± 5% of the nominal value. The device updates the frequency every clock period by fixed steps:

- Ramps up in 63 steps from minimum to maximum switching frequency
- Ramps down in 63 steps from maximum to minimum switching frequency

The resulting frequency modulation is almost triangular, with a frequency of:

$$F_{Dith} = \frac{F_{SW}}{126} \quad (3)$$

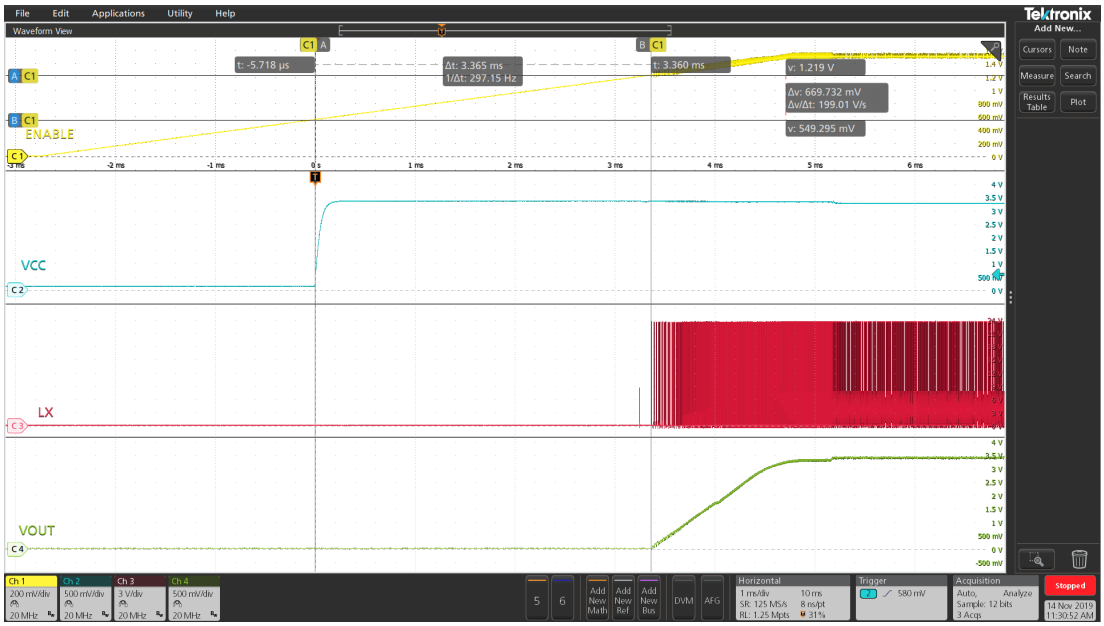
5.4 Enable and Reset

In order to maximize both the EN threshold accuracy and the current consumption, the device implements two different enable thresholds:

- The wake-up threshold, $V_{WAKEUPH}$ = 0.5 V typ.
- The start-up threshold, V_{ENH} = 1.2 V typ.

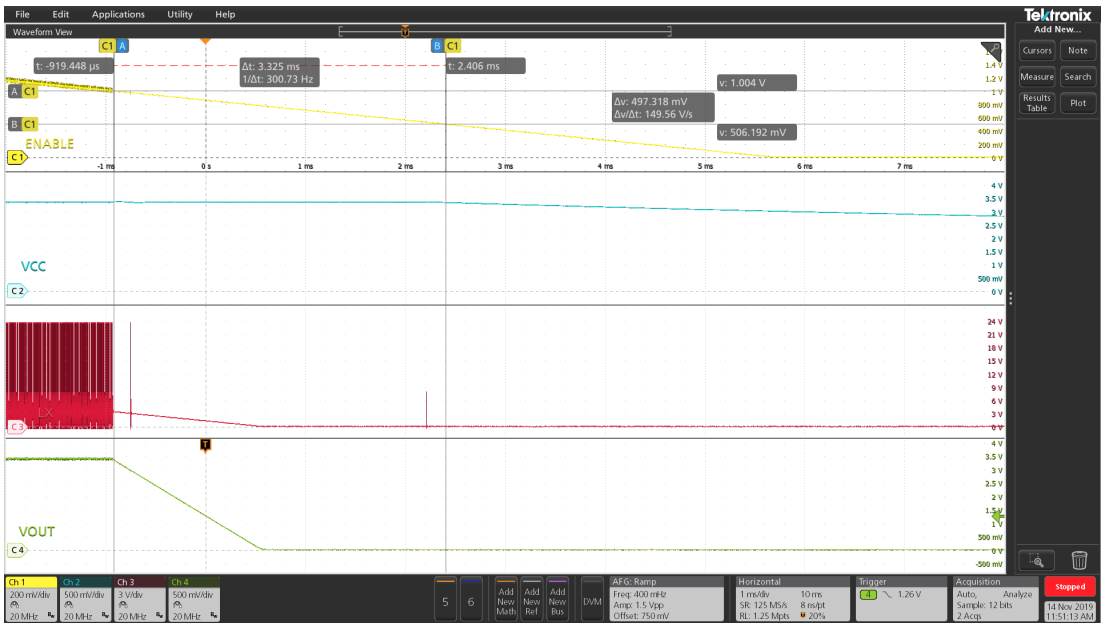
As soon as the EN pin is detected above $V_{WAKEUPH}$ and VIN voltage is higher than V_{INH}, the regulator turns on the internal circuitry and waits for the V_{ENH} before starting the switching activity. When this occurs, the internal voltage reference is increased by about 2 ms (typ.) in order to limit the inrush current and perform a smooth output capacitor charge.

Figure 14. Turn-on example



If the EN pin is forced lower than V_{ENL} the switching activity is stopped. The L7983 can further reduce the input current as soon as EN is forced lower than the $V_{WAKEUPL}$ threshold. When this occurs the input current is reduced to I_{SHTDWN} = 2.3 µA (typ.).

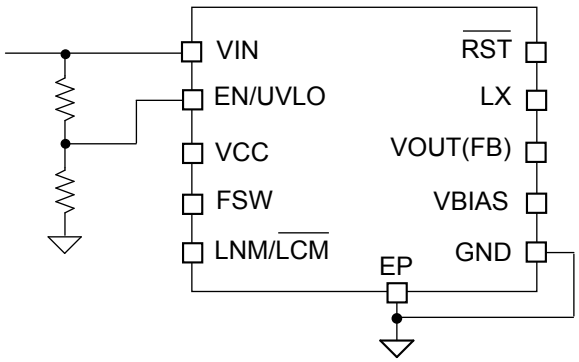
Figure 15. Turn-off example



A divider from VIN can be used to program the input voltage threshold for controlled power-up, as shown in Figure 16.

The EN pin is VIN compatible.

Figure 16. Input voltage turn-on threshold programming



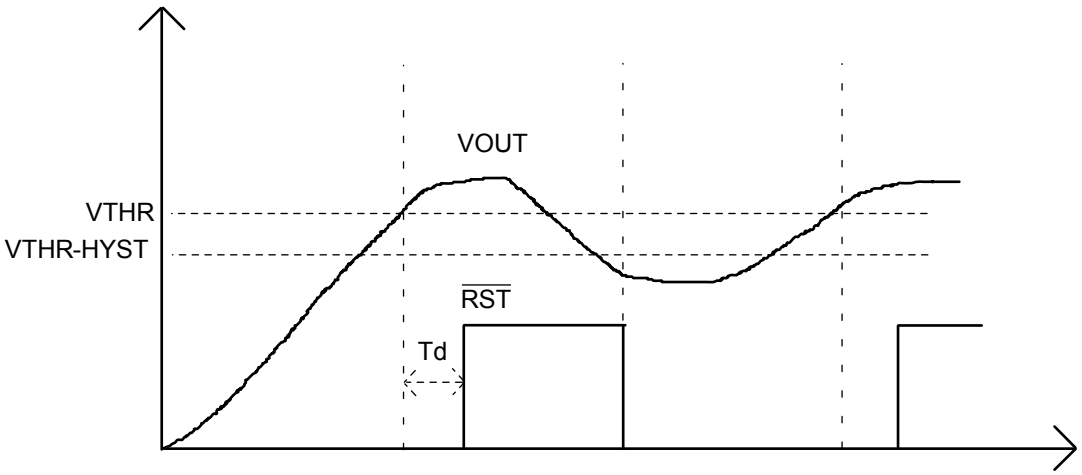
During the soft-start, the L7983 is not allowed to sink current from the output, also if LNM operation is selected. This feature is intended to guarantee the proper power-up also in case of output voltage pre-bias condition.

Following the L7983 turn-on, if the output voltage (sensed through the VOUT(FB) pin) is detected higher than the V_{RSTTHR} threshold, the RST pin is left floating.

During the operation, the RST pin is asserted low if the output voltage is found lower than the V_{RSTTHR} - $V_{RSTHYST}$ threshold, i.e. a typical 2% hysteresis is implemented.

In case of overvoltage detection (OVP), the RST pin is asserted low. A 2% hysteresis (typ.) is required before releasing RST.

Figure 17. Output voltage and RST behavior



A built-in 2 ms typ. delay is always implemented before releasing RST.

5.5 VCC and switchover

The internal LDO (low drop-out) linear regulator is turned on when VIN is higher than the V_{INH} threshold and EN pin is detected above $V_{WAKEUPH}$. The output voltage is available on pin VCC, which must be properly bypassed to GND by 470 nF ceramic capacitor. No external load is expected on VCC pin.

The switchover function is enabled in case VBIAS is detected higher than the SWO threshold (refer to Table 7). When this occurs, the internal LDO power supply is switched from VIN to VBIAS, so increasing the power conversion efficiency. This is the typical case when VBIAS is connected to the regulator output.

If the programmed output voltage is lower than the SWO threshold and no auxiliary rail lower than VIN is available, VBIAS must be connected to GND (refer to Figure 29, Figure 35 and Figure 41 for no load input current in typical application conditions).

5.6 Fault management

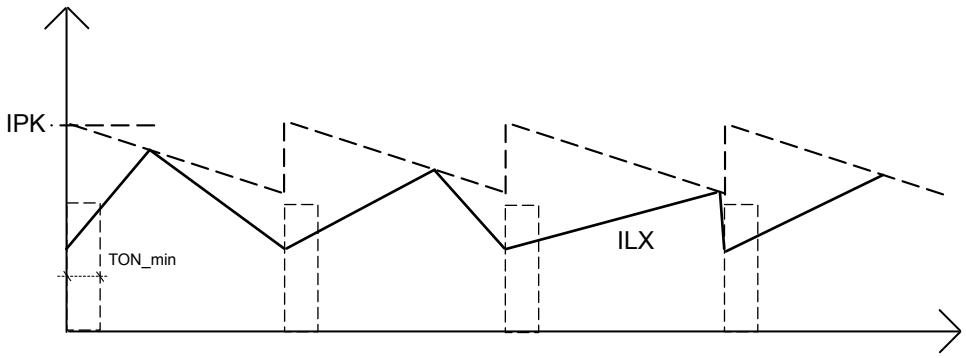
The L7983 fault management is continuously monitoring the inductor current, the output voltage and the device junction temperature.

Furthermore, thanks to the input UVLO (undervoltage lock-out) circuitry, the switching activity is guaranteed only with the proper VIN level. All the protections are auto-recovery.

5.6.1 Overcurrent protection (OCP)

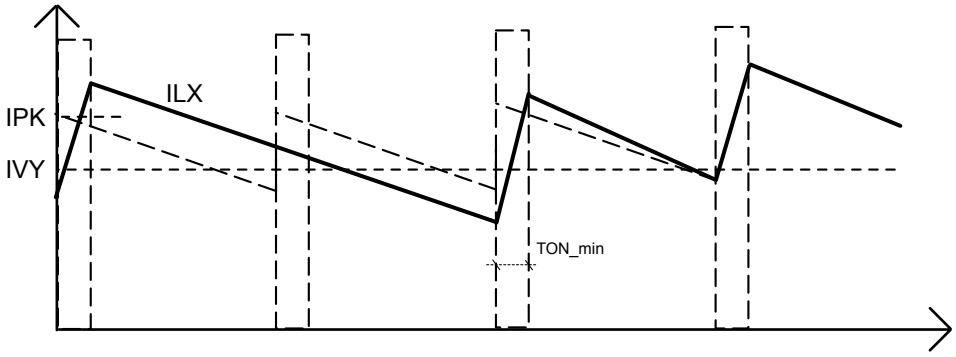
In normal operation the HS MOS is turned off when the sensed current is equal to programmed current (refer to Figure 2). The maximum available current is limited by the internal OCP (overcurrent protection) comparator, cycle by cycle. The IPK threshold is gradually reduced during the switching period by slope contribution, as shown in Figure 18.

Figure 18. Peak current limit



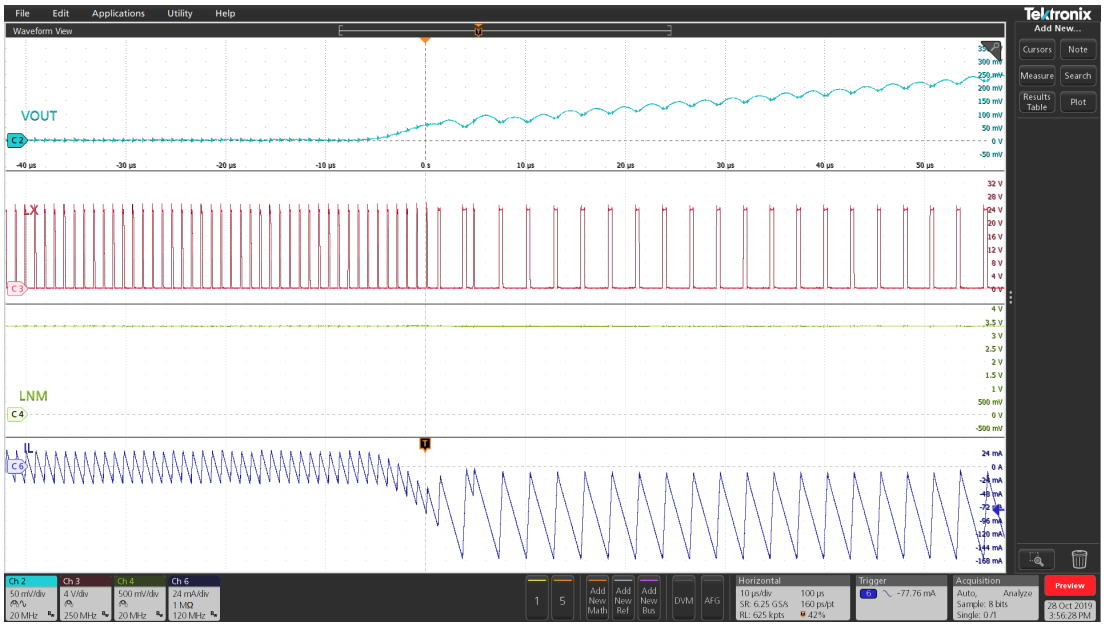
The inductor current is also monitored during LS MOS on-time. This feature, also known as “valley current limitation”, is effective in case of current runaway due to HS MOS minimum on-time limitation and very low VOUT / VIN ratio. This protection can avoid the HS MOS turn-on if the inductor current, sensed during LS MOS on-time, is higher than the IVY threshold (Figure 19).

Figure 19. Valley current limit



In LNM mode, the L7983 can sink current from the output. However, to protect the power components, a negative current limit is implemented. If the sensed current is found lower than the I_{NEG} threshold, the low-side MOS is promptly turned off and the high-side one is turned on until the inductor is discharged. When this occurs, the LS MOS is allowed to turn on again.

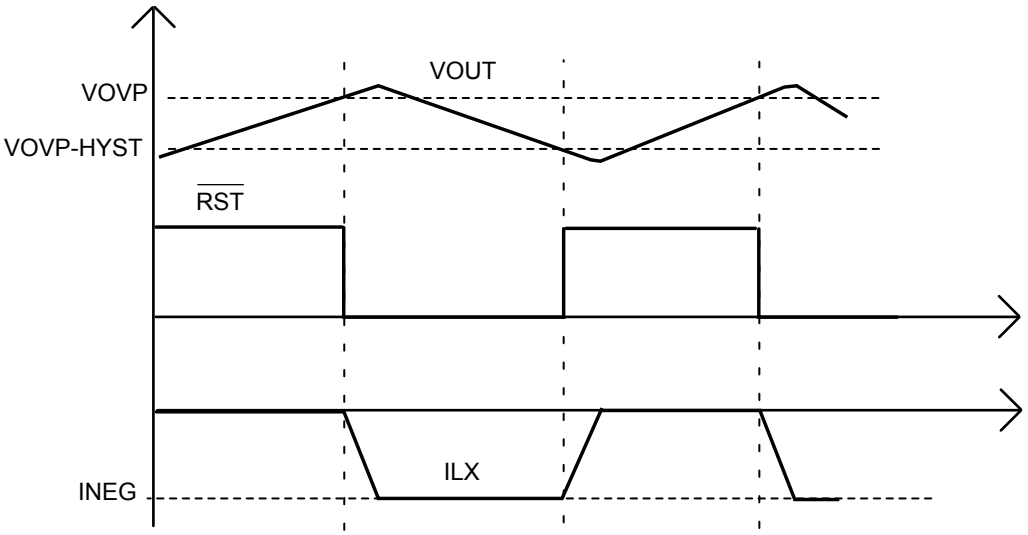
Figure 20. Negative current limit example



5.6.2 Overvoltage protection (OVP)

In case the VOUT(FB) pin is detected above the VOVP threshold, the output overvoltage protection is triggered. When this occurs, the RST pin is forced low and the L7983 actively discharges the output voltage by sinking current (refer to Section 5.6.1 Overcurrent protection (OCP)).

Figure 21. Overvoltage protection



As soon as the OVP cause is removed, the proper switching activity is restored and RST output is released, with the delay and threshold described in Section 5.4 .

5.6.3 Overtemperature protection (OTP)

If the device junction temperature increases above T_{SHDWN} (165 °C typ.) the switching activity is inhibited until a temperature drop of T_{HYS} (30 °C typ.) is detected.

When the switching activity is resumed, a soft-start is implemented. The OTP protection is always active.

5.7 Application design guidelines

5.7.1 Input capacitor selection

The input capacitor must be rated for the maximum input operating voltage and the maximum expected RMS input current.

Since the step-down converters' input current is a sequence of pulses from 0A to IOUT, the input capacitor must absorb the equivalent RMS current which can be up to the load current divided by two (worst case, with duty cycle of 50%). For this reason, the quality of these capacitors must be very high to minimize the power dissipation generated by the internal ESR, thereby improving system reliability and efficiency.

The RMS input current (flowing through the input capacitor) is roughly estimated by:

$$I_{CIN,RMS} \cong I_{OUT} \cdot \sqrt{D \cdot (1-D)} \quad (4)$$

Considering D = V_{OUT} / V_{IN} the theoretical DC-DC conversion ratio, the above equation provides a maximum value equal to I_{OUT} / 2 when D = 0.5.

The amount of the input voltage ripple can be roughly estimated by Eq. (5).

$$V_{IN,PP} = \frac{D \cdot (1-D) \cdot I_{OUT}}{C_{IN} \cdot F_{SW}} + R_{ES,IN} \cdot I_{OUT} \quad (5)$$

In case of MLCC ceramic input capacitors, the equivalent series resistance ($R_{ES,IN}$) is almost negligible.

The suggested component is a ceramic MLCC capacitor with value 1 µF or higher, with adequate voltage rating (100 V typ.), placed as close as possible to the V_{IN} and GND pins.

Very fast V_{IN} transitions must be avoided to guarantee the proper operation. Additional input voltage filtering must be implemented in case of expected V_{IN} transitions faster than 0.1 V/µs.

5.7.2 Inductor selection

In low consumption mode (LCM) the light load operation is implemented with constant current pulses (I_{SKIP} = 80 mA typ., as described in Section 5.2.1). In LCM, to achieve a smooth transition from discontinuous to continuous operation, i.e. from pulse skipping to constant frequency working mode, the inductor should be selected assuming a target current ripple close to I_{SKIP}.

$$L = \frac{V_{OUT} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{I_{SKIP} \cdot F_{SW}} \quad (6)$$

In low noise mode (LNM) the inductance value is typically selected in order to keep the current ripple in the range 20% - 40% of the maximum DC output current. However, in order to prevent the sub-harmonic instability in the peak current mode control loop, a fixed slope compensation mechanism is implemented in L7983 by adding a current ramp to the sensed current (see Figure 4). This approach is effective if the inductor current ripple, in the expected input voltage range, is comparable with the above-mentioned added slope.

In conclusion, Eq. (6) is the reference design equation for inductor selection, independent of selected working mode (LNM or LCM).

5.7.3 Output capacitor selection

In LNM working mode, the current in the output capacitor has a triangular waveform which generates a voltage ripple across it. This ripple is due to the capacitive component (charge and discharge of the output capacitor) and the resistive component (due to the voltage drop across its ESR). The output capacitor must be selected in order to have a voltage ripple compliant with the application requirements.

The amount of the voltage ripple can be estimated starting from the current ripple obtained by the inductor selection. Assuming ΔI_L is the inductor current ripple, the output voltage ripple is roughly estimated by Eq. (7).

$$\Delta V_{OUT,PP,LNM} \approx \Delta I_L \cdot R_{ES,OUT} + \frac{\Delta I_L}{8 \cdot F_{SW} \cdot C_{OUT}} \quad (7)$$

The ESR contribution is usually negligible in case of multi-layer ceramic capacitor (MLCC), which is the most common choice for the L7983 typical solution. Neglecting the ESR contribution, the minimum value of the output capacitor to guarantee the target output voltage ripple specification in LNM is estimated by:

$$C_{OUT,LNM} \geq \frac{\Delta I_L}{8 \cdot F_{SW} \cdot \Delta V_{OUT,PP,LNM}} \quad (8)$$

In case of light load and LCM working mode, the theoretical output voltage ripple is estimated by:

$$\Delta V_{OUT,PP,LCM} = \frac{L \cdot I_{SKIP}^2}{2 \cdot C_{OUT}} \cdot \frac{V_{IN}}{V_{OUT} \cdot (V_{IN} - V_{OUT})} \quad (9)$$

The output capacitor selection is important also to guarantee the control loop stability.

A minimum capacitance value is necessary to limit the system bandwidth, F_{BW}. A reasonable limit for F_{BW} is the minimum between $F_{SW}/8$ and 150 kHz, which provides the following design equation:

$$C_{OUT,BW} \geq \frac{0.8\,A}{F_{BW,MAX} \cdot V_{OUT}} \quad (10)$$

In the peak current mode architecture, working in LNM, there is a close relationship between the programmed inductor peak current and the error amplifier input error (i.e. the difference between the output voltage sensed on the FB pin and the internal reference voltage, V_{REF}).

During a load transient, ΔI_{OUT}, the theoretical loop response depends on output capacitor and designed system bandwidth:

$$\Delta V_{OUT,LTR} \approx \frac{\Delta I_{OUT}}{2\pi \cdot F_{BW} \cdot C_{OUT}} \quad (11)$$

The L7983 implements a fixed integrated compensation network so the output capacitor selection, as highlighted by Eq. (10), directly impacts the system bandwidth and, at the end, also the expected load transient performance as described by Eq. (11).

The above listed design suggestions are summarized in Table 8 below which considers the most common voltage conversions.

Table 8. Reference applications – V_{IN} = 24 V, C_{IN} = 1 µF, CVCC = 470 nF

V_{OUT} [V]	F_{SW} [kHz]	L [µH]	C_{OUT} [µF]	R_{FSW} [kΩ]	R_U [kΩ]	R_D [kΩ]	Note
1.5	200	100	22	1.8	43	56	VBIAS = GND
	500	33	10	5.6			
	1000	22	4.7	0			
3.3	200	220	10	1.8	180	62	L7983PU33R to avoid R_U and R_D. VBIAS = VOUT
	500	68	4.7	5.6			
	1000	47	2.2	0			
	1500	22	2.2	18			
5	200	330	6.8	1.8	300	62	L7983PU50R to avoid R_U and R_D. VBIAS = VOUT
	500	100	3.3	5.6			
	1000	47	2.2	0			
	2200	22	2.2	56			
12	200	330	3.3	1.8	510	39	VBIAS = VOUT
	500	150	2.2	5.6			
	1000	68	1	0			
	2200	33	1	56			

5.7.4 Layout considerations

The PCB layout of the switching DC-DC regulators minimizes the noise injected in high impedance nodes and interference generated by the high current switching loops.

In a step-down converter, the input loop (including the input capacitor, the DC-DC regulator and ground connection) is the most critical one due to high value pulsed currents flowing through it. In order to minimize the EMI, this loop must be as short as possible with an adequate input capacitor placed very close to L7983 VIN and GND (pin 8 and 10 respectively).

The feedback pin (FB) connection to the external resistor divider is a high impedance node, so the interference can be minimized by placing the routing of the feedback node as far as possible from the high current paths. To reduce the pick-up noise, the resistor divider must be placed very close to the device.

Thanks to the exposed pad of the device, the ground plane helps to reduce the junction to ambient thermal resistance, so a wide ground plane enhances the thermal performance of the converter, allowing the high-power conversion.

Refer to Section 6 Evaluation board for an example of the PCB layout.

5.7.5 Thermal considerations

The thermal design prevents the thermal shutdown of the device if junction temperature goes above 165 °C (typ.).

The three different sources of losses within the device are:

- Conduction losses due to the non-negligible RDS(on) of the integrated power switches; these are equal to

$$P_{COND} = R_{HS,ON} \cdot D \cdot I_{OUT}^2 + R_{LS,ON} \cdot (1 - D) \cdot I_{OUT}^2 \quad (12)$$

where D is the duty cycle of the application and $R_{HS,ON}$ and $R_{LS,ON}$ are the maximum resistance overtemperature of the power switches. Note that the duty cycle is theoretically given by the ratio between VOUT and VIN but actually it is higher in order to compensate the losses of the regulator, so the conduction losses increase compared with the ideal case;

- Switching losses due to power MOSFETs turn-ON and OFF; these can be calculated as:

$$P_{SW} = V_{IN} \cdot I_{OUT} \cdot \frac{(T_{RISE} + T_{FALL})}{2} \cdot F_{SW} = V_{IN} \cdot I_{OUT} \cdot T_{TR} \cdot F_{SW} \quad (13)$$

where T_{RISE} and T_{FALL} are the overlap times of the voltage across the high-side power switch (VDS) and the current flowing into it during turn-ON and turn-OFF phases. T_{TR} is the equivalent switching time. For this device the typical value for the equivalent switching time is 10 ns.

- Quiescent current losses, calculated as follows:

$$P_Q = V_{IN} \cdot I_{QVIN} + V_{BIAS} \cdot I_{QVBIAS} \quad (14)$$

where I_{QVIN} and I_{QVBIAS} are the L7983 quiescent currents in case of separate bias supply.

If VBIAS = V_{OUT} the L7983 power conversion efficiency η_{L7983} must be included in the previous equation:

$$P_Q|_{VBIAS = VOUT} = V_{IN} \cdot \left(I_{QVIN, VBIAS = 3.3V} + \frac{1}{\eta_{L7983}} \cdot \frac{V_{BIAS}}{V_{IN}} \cdot I_{QVBIAS,\ VBIAS = 3.3V} \right) \quad (15)$$

If the switch-over feature is not used the total quiescent current losses are represented by:

$$P_Q|_{VBIAS = GND} = V_{IN} \cdot I_{QVIN, VBIAS = GND} \quad (16)$$

The L7983 total power losses are given by:

$$P_{LOSS} = P_{COND} + P_{SW} + P_Q \quad (17)$$

The junction temperature T_J can be estimated with the following equation:

$$T_J = T_A + P_{LOSS} \cdot R_{TH,JA} \quad (18)$$

where T_A is the ambient temperature. $R_{TH,JA}$ is the equivalent thermal resistance junction to ambient of the device; it can be calculated as the parallel of many paths of heat conduction from the junctions to the ambient. For this device the path through the exposed pad is the one conducting the largest amount of heat. The $R_{TH.JA}$ measured on the demonstration board described in the following section is about 50 °C/W.

6 Evaluation board

6.1 Schematic and PCB layout

Figure 22. **Evaluation board schematic**

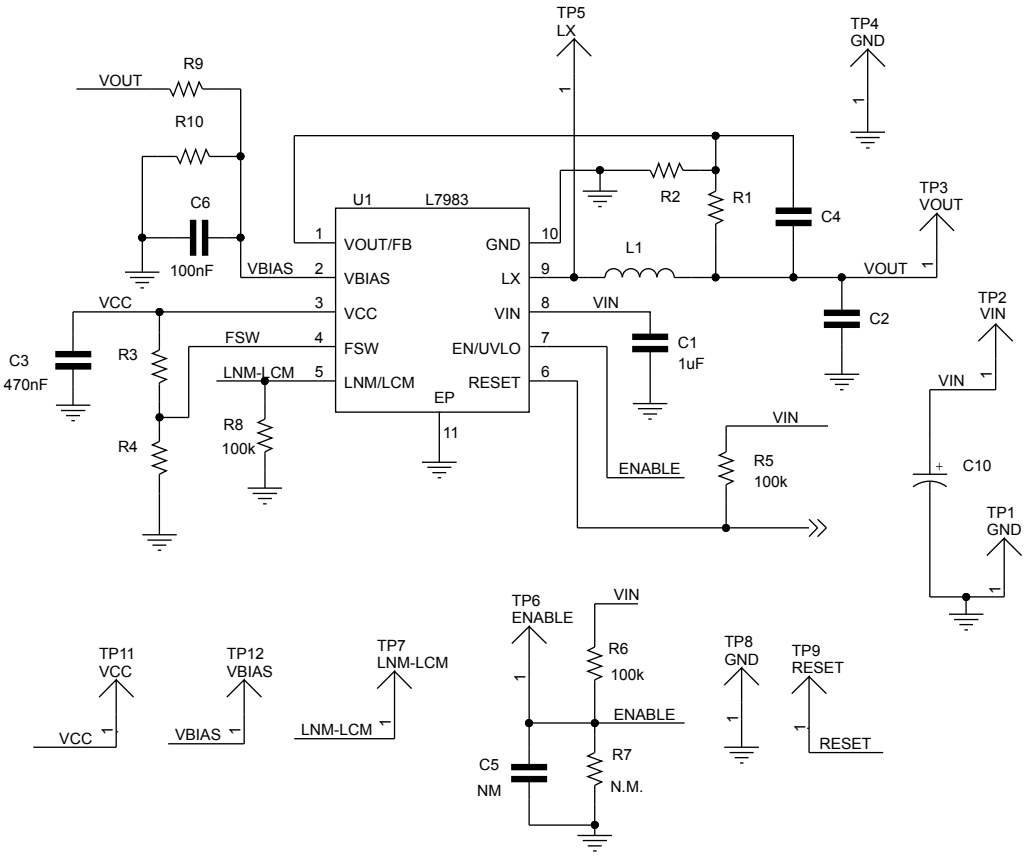


Figure 23. PCB layout (Top)

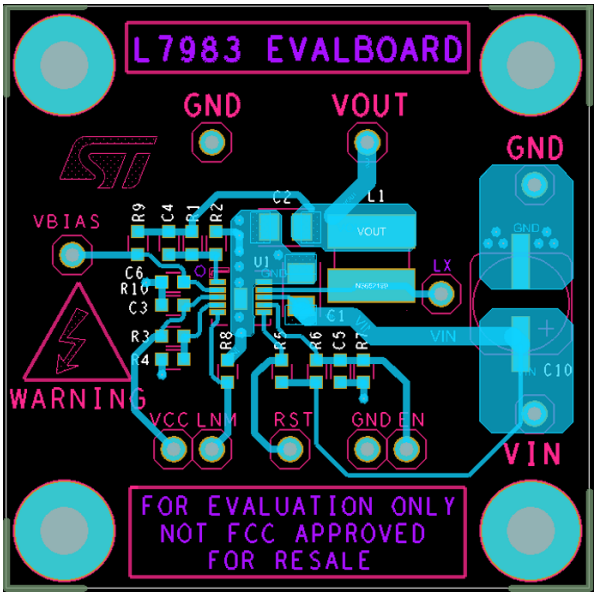
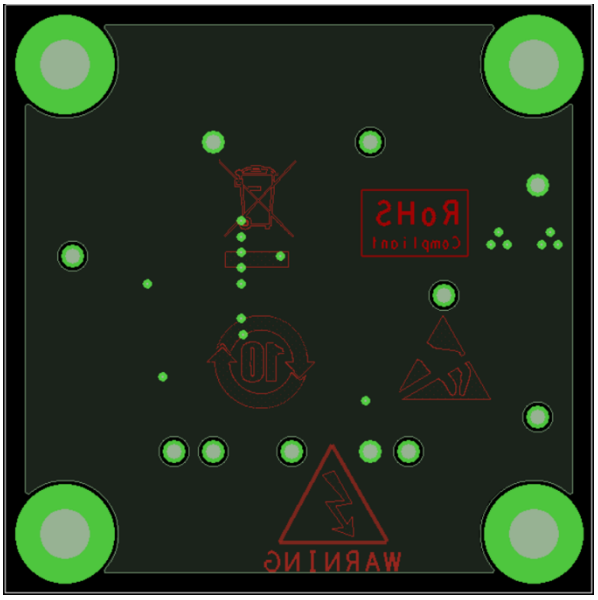


Figure 24. PCB layout (Bottom)



6.2 L7983PUR - Evaluation board

In this section the L7983PUR (adjustable VOUT) evaluation board is described.
The board schematic is shown in Figure 22 and the PCB layout is depicted in Figure 23 and Figure 24.
The main features are:

- Programmed VOUT = 12 V
- Max. IOUT = 300 mA
- Selected FSW = 1 MHz
- VBIAS = VOUT (switch-over enabled)

Table 9. L7983PUR evaluation board component list (BOM)

Reference	Part	Package	Details	Manufacturer P/N
C1	1 µF	1206	X7R/100V/10%	TDK C3216X7R2A105K
C2	1 µF	1206	X7R/100V/10%	TDK C3216X7R2A105K
C3	470 nF	0603	X7R/16V/10%	
C4, C5, C10	N.M.			
C6	100 nF	0603	X7R/16V/10%	
L1	68 µH	4x4 mm	0.46 A sat/ 950 mΩ	COILCRAFT LPS4018-683M
R1	510 kΩ	0603	1% tolerance	
R2	39 kΩ	0603	1% tolerance	
R3, R7	N.M.			
R4, R9, R10	0	0603		
R5, R6, R8	100 kΩ	0603	1% tolerance	
U1	L7983	DFN10_3x3		STM L7983PUR

Figure 25. 12 V efficiency (LCM)

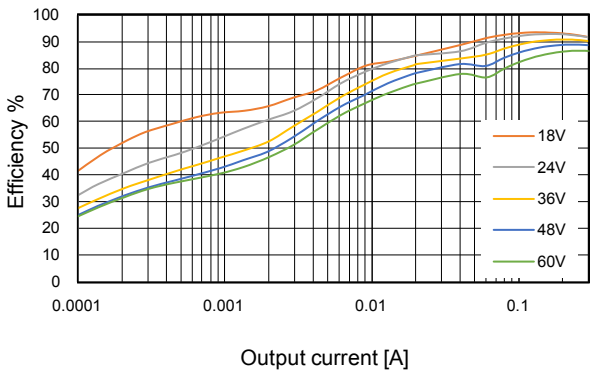


Figure 26. 12 V load regulation (LCM)

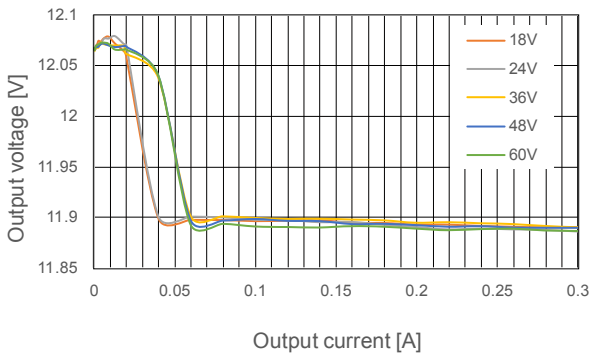


Figure 27. 12 V efficiency (LNM)

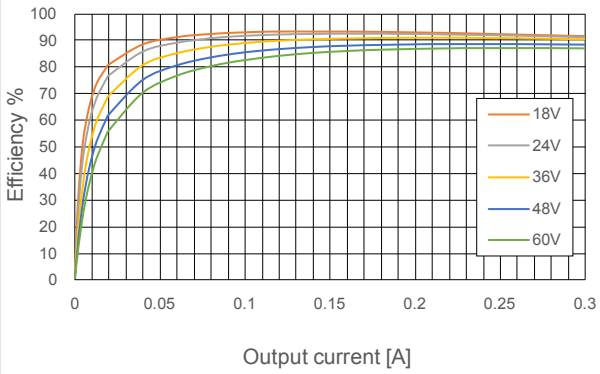


Figure 28. 12 V load regulation (LNM)

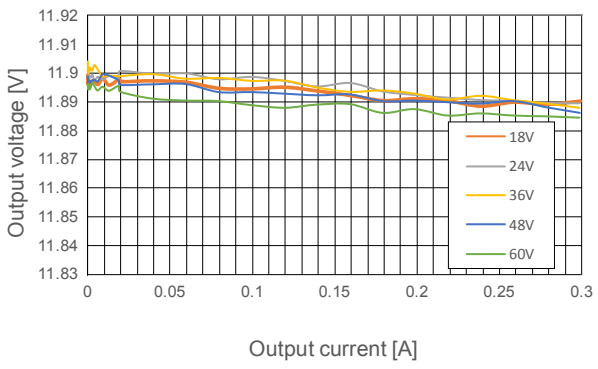


Figure 29. 12 V input current - LCM

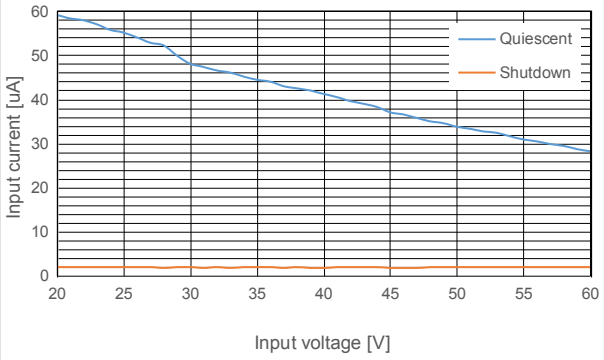
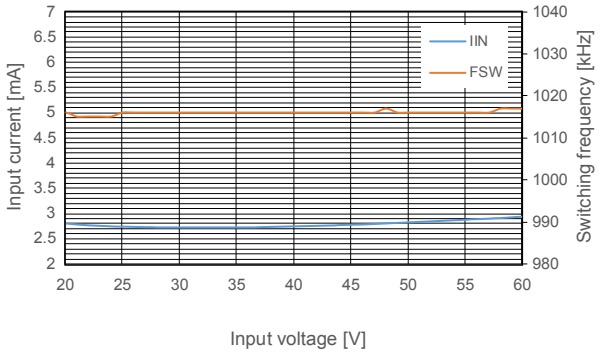


Figure 30. 12 V input current and FSW - LNM



6.3 L7983PU33R - Evaluation board

In this section the L7983PU33R (VOUT=3.3 V fixed) evaluation board is described.
The board schematic is shown in Figure 22 and the PCB layout is depicted in Figure 23 and Figure 24.
The main features are:

- Programmed VOUT = 3.3 V (fixed)
- Max. IOUT = 300 mA
- Selected FSW = 1 MHz
- VBIAS = VOUT (switch-over enabled)

Table 10. L7983PU33R evaluation board component list (BOM)

Reference	Part	Package	Details	Manufacturer P/N
C1	1 µF	1206	X7R/100V/10%	TDK C3216X7R2A105K
C2	2.2 µF	0805	X7R/16V/10%	TDK C2012X7R1C225K
C3	470 nF	0603	X7R/16V/10%	
C4, C5, C10	N.M.			
C6	100 nF	0603	X7R/16V/10%	
L1	47 µH	4x4 mm	0.56 A sat/ 650 mΩ	COILCRAFT LPS4018-473M
R1, R4, R9	0 Ω	0603		
R2, R3, R7, R10	N.M.			
R5, R6, R8	100 kΩ	0603	1% tolerance	
U1	L7983	DFN10_3x3		STM L7983PU33R

Figure 31. 3.3 V fix efficiency (LCM)

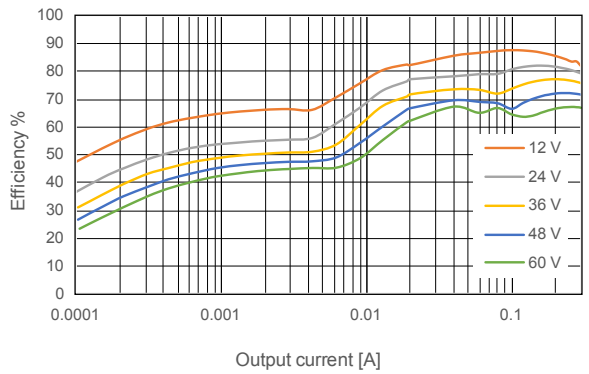


Figure 32. 3.3 V fix load regulation (LCM)

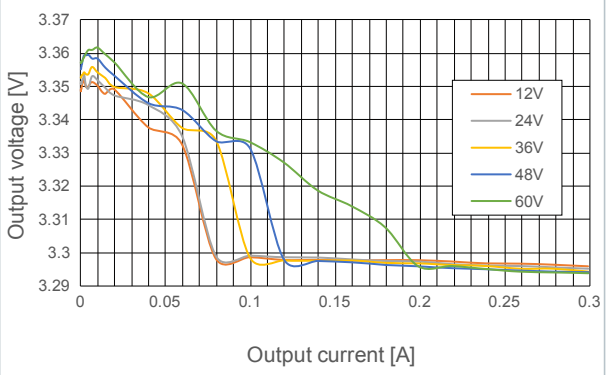


Figure 33. 3.3 V fix efficiency (LNM)

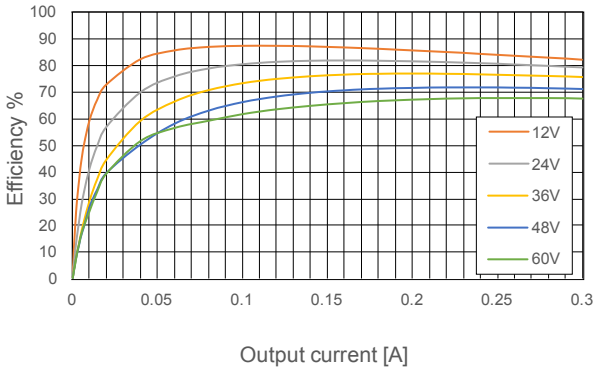


Figure 34. 3.3 V fix load regulation (LNM)

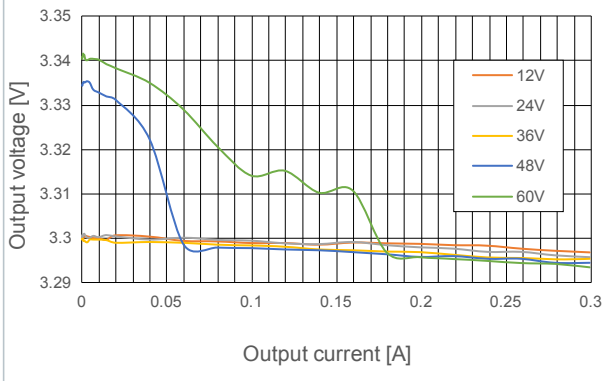


Figure 35. 3.3 V fix input current, no load (LCM)

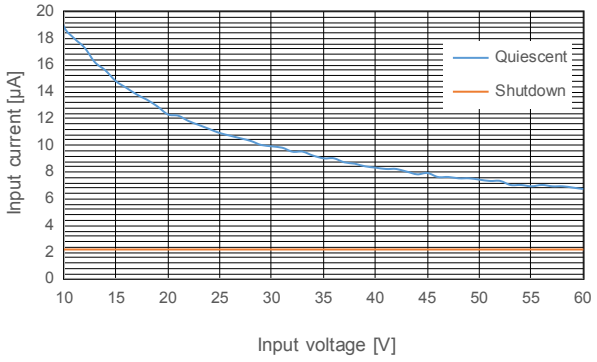
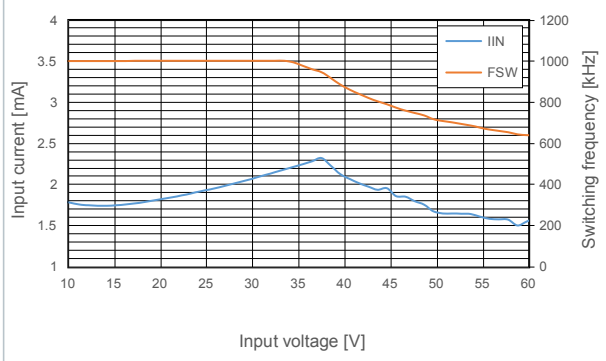


Figure 36. 3.3 V fix input current, no load (LNM)



6.4 L7983PU50R - Evaluation board

In this section the L7983PU50R (VOUT = 5 V fixed) evaluation board is described.
The board schematic is shown in Figure 22 and the PCB layout is depicted in Figure 23 and Figure 24.
The main features are:

- Programmed VOUT = 5 V (fixed)
- Max. IOUT = 300 mA
- Selected FSW = 1 MHz
- VBIAS = VOUT (switch-over enabled)

Table 11. L7983PU50R evaluation board component list (BOM)

Reference	Part	Package	Details	Manufacturer P/N
C1	1 µF	1206	X7R/100V/10%	TDK C3216X7R2A105K
C2	2.2 µF	0805	X7R/16V/10%	TDK C2012X7R1C225K
C3	470 nF	0603	X7R/16V/10%	
C4, C5, C10	N.M.			
C6	100 nF	0603	X7R/16V/10%	
L1	47 µH	4x4 mm	0.56 A sat/ 650 mΩ	COILCRAFT LPS4018-473M
R1, R4, R9	0 Ω	0603		
R2, R3, R7, R10	N.M.			
R5, R6, R8	100 kΩ	0603	1% tolerance	
U1	L7983	DFN10_3x3		STM L7983PU50R

Figure 37. 5 V fix efficiency (LCM)

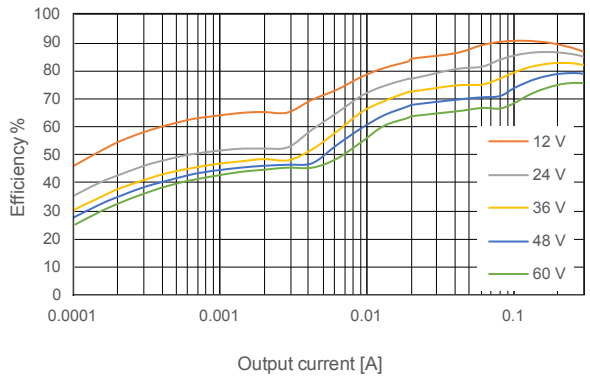


Figure 38. 5 V fix load regulation (LCM)

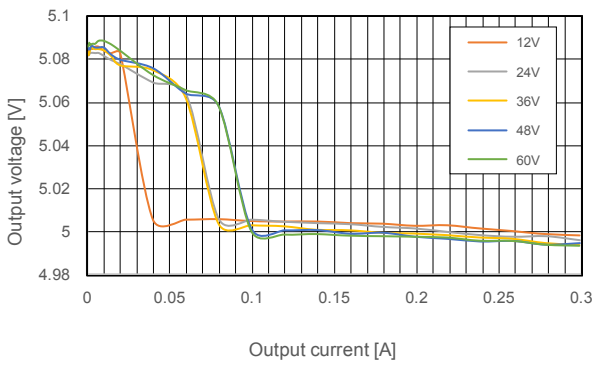


Figure 39. 5 V fix efficiency (LNM)

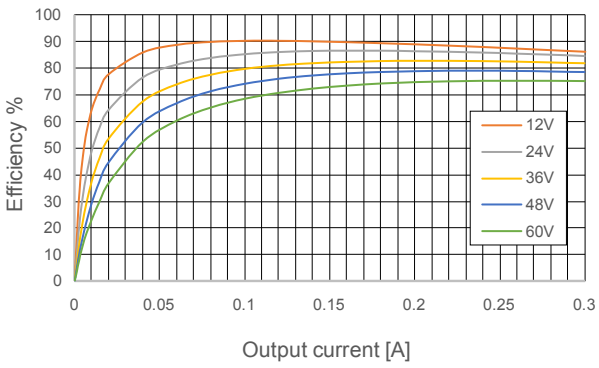


Figure 40. 5 V fix load regulation (LNM)

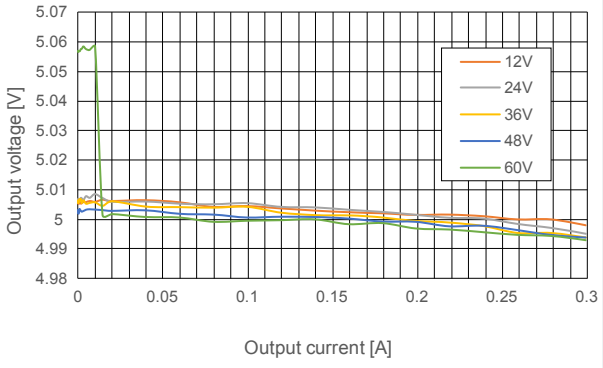


Figure 41. 5 V fix input current, no load (LCM)

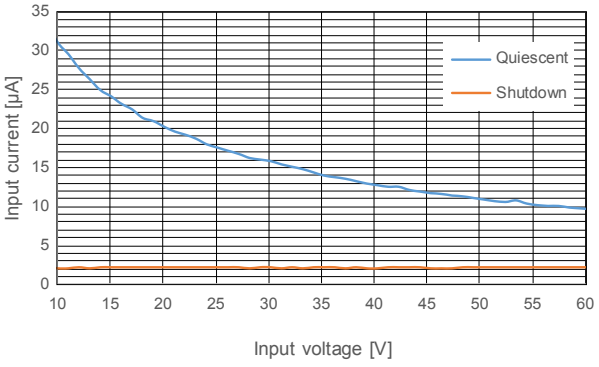
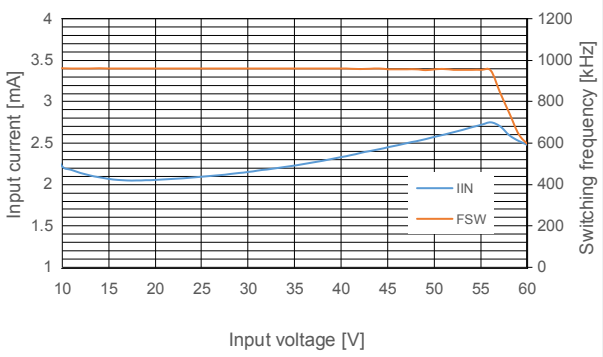


Figure 42. 5 V fix input current, no load (LNM)



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 DFN10 (3 x 3 x 0.8 mm) package information

Figure 43. **DFN10 (3 x 3 x 0.8 mm) package outline**

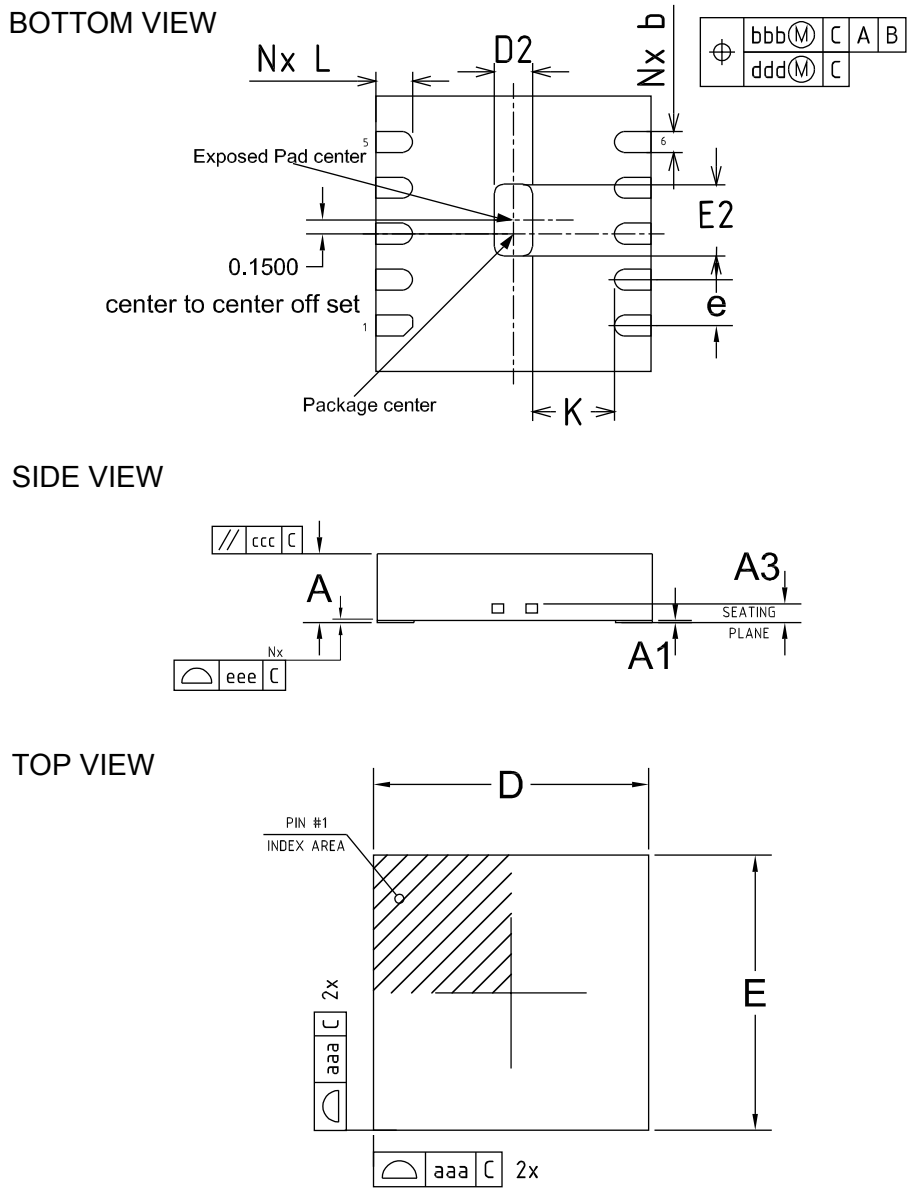
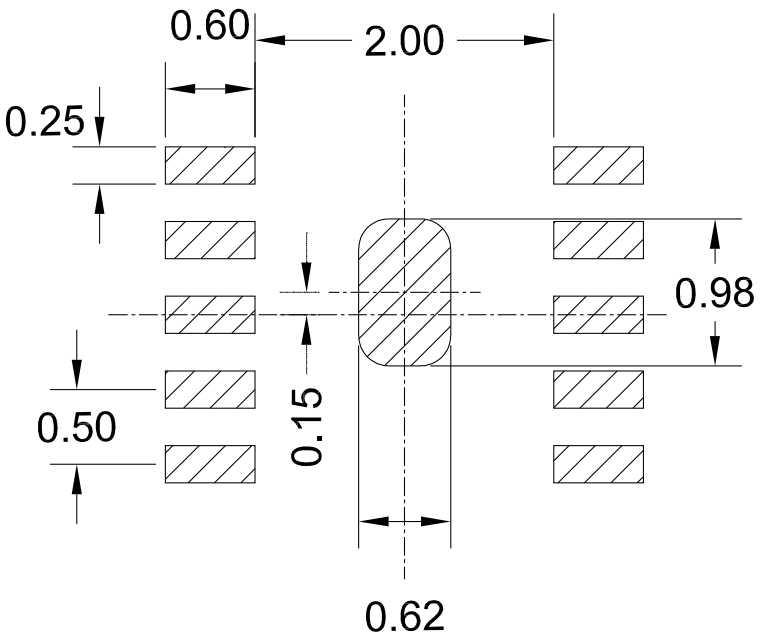


Table 12. **DFN10 (3 x 3 x 0.8 mm) mechanical data**

SYMBOL	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.0	0.02	0.05
A3		0.20 Ref.	
b	0.16	0.23	0.28
D		3.00 BSC	
D2	0.27	0.42	0.52
e		0.50 BSC	
E		3.0 BSC	
E2	0.63	0.78	0.88
L	0.30	0.40	0.50
K	0.20		
N		10	
NE		5	

Figure 44. **DFN10 (3 x 3 x 0.8 mm) recommended footprint**



8 Ordering information

Table 13. **Order codes**

Part numbers	Output voltage	Package	Packaging
L7983PUR	Adjustable	DFN10	Tape and reel
L7983PU33R	Fixed 3.3 V		
L7983PU50R	Fixed 5.0 V		

Revision history

Table 14. **Document revision history**

Date	Revision	Changes
01-Oct-2020	1	Initial release.

Contents

List of tables

List of figures