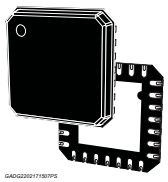
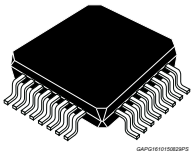
L9663

Automotive PSI5 Transceiver IC

Datasheet - production data



VFQFPN28



TQFP32
(Exposed pad down)

Features

- AEC-Q100 qualified
- 2-channel PSI5 transceiver compatible with rev. 1.3 and rev. 2.x
- Manchester coded digital data transmission
- High data transmission speed of 125 kbps (optional 83.3 kbps and 189 kbps)
- High EMC robustness and low emission
- Bootstrap circuits for sync pulses
- Current limitation and voltage clamp on interface pins
- Integrated charge pump stage for pre-regulation with spread spectrum approach
- Integrated FLL module for high accuracy timing control
- Reverse voltage protection structure
- Short to ground tolerant with ±1.5 V ground shift
- 32-bit SPI interface with address multiplexing
- Operating voltage: V_B = 4.8 V (5.2 V for sync pulses with 3.5 V step) to 35 V
- Ambient temperature range: -40°C to 140 °C
- Package: VFQFPN28 or TQFP32EP

Description

The Peripheral Sensor Interface (PSI5) is an interface for automotive sensor applications. PSI5 is an open standard based on existing sensor interfaces for peripheral sensors and offers a universal and flexible solution for multiple sensor applications.

The PSI5 interface allows asynchronous or synchronous operations and different bus modes. The device is compatible with both v1.3 and v2.x PSI5 revisions (limitations are specified inside this document). It operates with a wide range of sensor supply current and variable data word length (8 to 28 bit).

The sensors are connected to the ECU using the same line for power supply and data transmission. The transceiver IC provides a pre-regulated voltage to the sensors and reads in the transmitted sensor data.

The PSI5 interface allows either point to point connection or bussed mode.

Table 1. Device summary

Order code	Package	Packing
L9663	TQFP32 (Exposed pad)	Tray
L9663-TR		Tape & Reel
L9663-1	VFQFPN28	Tray
L9663-TR-1		Tape & Reel

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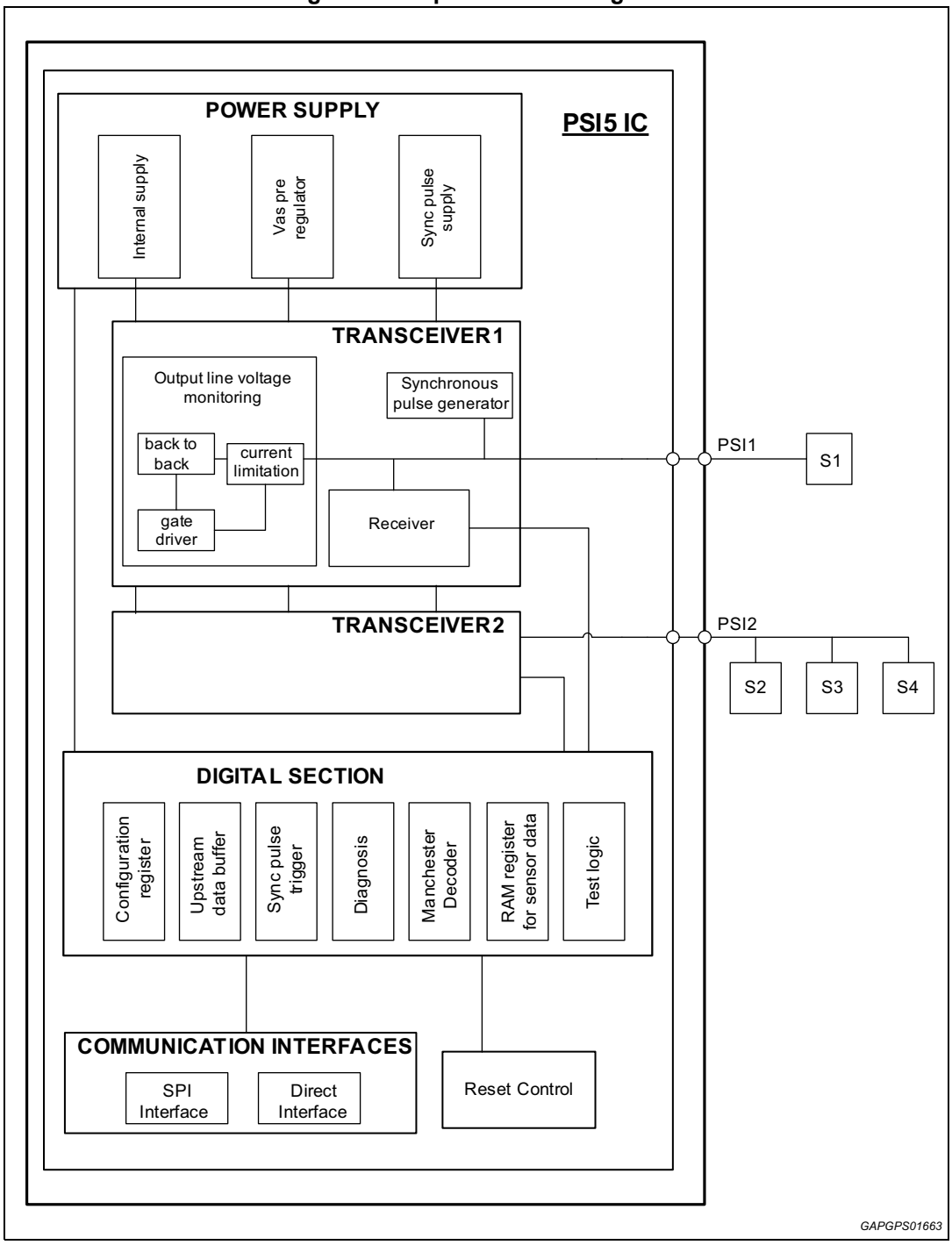
Figure 1. Simplified block diagram



1.2 Main functionality

The transceiver IC can be used in two different modes (Mode 1 or Mode 2)[a] . The system configuration called Mode 1 performs the decoding effort of sensor signals in the IC. The system configuration called Mode 2 is a front-end to a PSI5 decoder contained in an external device (typically a µC with a dedicated module).

The transceiver IC can monitor all internally generated relevant voltages, such as V_{SYNCx} V_{AS} and V_PSIx.

The PSI5 interfaces inside the IC are supplied by a separate input pin VAS. If only asynchronous mode is required, the VAS voltage is sufficient for the sensor power supply. When synchronous mode is required, a higher voltage than VAS is needed in order to generate the synchronous pulses. This voltage VSYNCx is generated by a dedicated bootstrap circuit for each channel.

For direct supply from battery, the transceiver IC includes a V_{AS} pre-regulator supplied by VASSUP-pin: the pre-regulator can drive an external FET to regulate the VAS voltage to 7.6 V or 5.3 V. In case of low voltage level at VASSUP, an integrated charge pump is implemented, with supply from VASSUP.

The internal analog and digital circuits are supplied by VB. The external voltage on VDD pin is used to supply the digital output pins; VDD pin can be used to switch the digital outputs from 5 V output level (default) to 3.3 V output level.

The PSI5 transceiver is functional in the whole V_{DD}, VB, VASSUP and V_{AS} power supply range.

The internal voltage supplies (V_{SYNCx}) are automatically activated by the transceiver IC depending on the operating mode whenever they are needed.

Each transceiver interface can be activated and deactivated by an SPI command. At start-up, the interfaces are off by default.

The communication interface block includes two different interfaces. In mode 1, SPI is used for data transfer. In mode 2, the direct interface is used. The data from and to the sensors will be transmitted bit-wise between the transceiver IC and the µC. The data evaluation and error handling for frame errors will be done in the PSI5 controller which is integrated in the µC.

Transceiver 1 and 2 supply the sensors and generate the synchronous pulses for synchronous data transfer (if required) from the sensors to the transceiver and for data transfer from the ECU to the sensors.

A data transfer from the ECU to the sensors can be performed:

- by using sync pulses with different duration (PSI5 2.x standard)
- by masking of sync pulses (PSI5 1.3 and 2.x standard)

The sync pulse trigger can be generated by an SPI command, by a dedicated pin (for connection to the Synchronous Pulse Output Block included in the microcontroller) or by an integrated automatic timer.

a. Mode 1 and Mode 2 are two system architectures which relate on the way L9663 communicates with the microcontroller. Depending on the chosen architecture, the µC must configure the IC with the correct setup.

The Transceivers 1 and 2 limit the current and the PSIx voltage (PSI5-requirement when VAS is too high because of failure in the VAS power supply, less than 11 V in data transmission or less than 16.5 V in sync pulse).

The current modulated signal received from sensor is detected and digitally converted. This sensor data will then either be:

- First Manchester decoded by the Manchester Decoder block with mark space error correction and then transferred to the "receive data buffer" module (Mode 1). The data from the new sensor frames will be saved in a buffer and then will be transferred to the µC via SPI.
- Transferred directly to the µC (Mode 2). In this case the output of the transceiver is a Manchester-coded signal without error correction that falls under microcontroller responsibility.

1.3 VQFPN28 pins description

Figure 2. VQFPN28 pins connection diagram (top view)

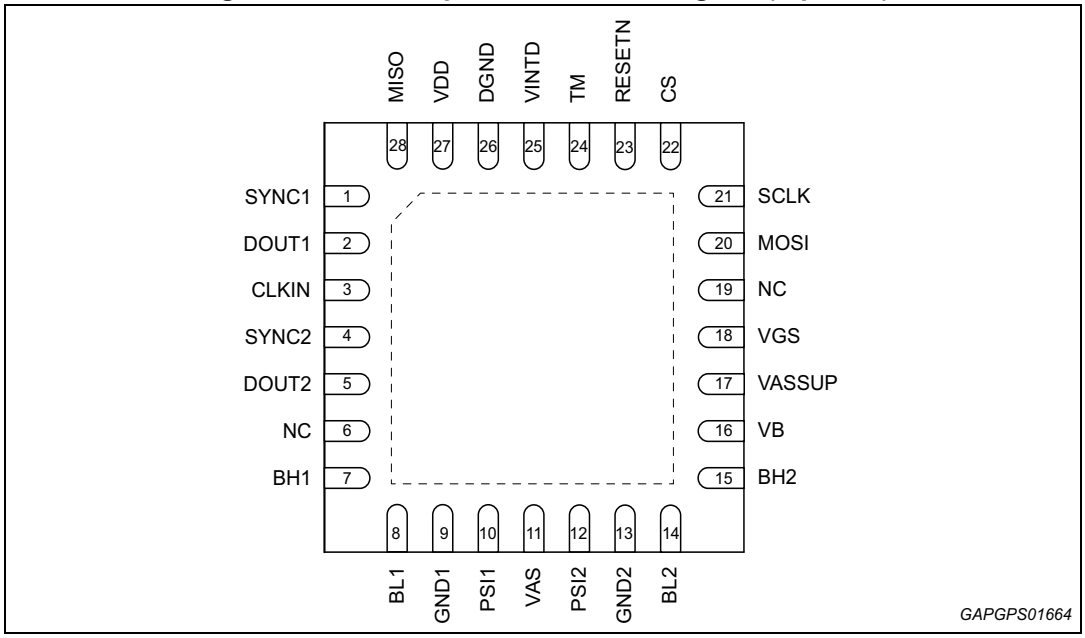


Table 2. VQFPN28 pin-out

Pin	Name	Description	Pin type	
1	SYNC1	Direct interface sync pulse trigger 1	I	local
2	DOUT1	Direct interface 1/Interrupt 1	O	local
3	CLKIN	External clock input	I	local
4	SYNC2	Direct Interface sync pulse trigger 2	I	local
5	DOUT2	Direct interface 2/Interrupt 2	O	local
6	NC(1)	-	-	-
7	BH1	Bootstrap capacitor pin 1 or SYNC voltage supply (from ECU), transceiver 1	I/O	local
8	BL1	Bootstrap capacitor pin 2, transceiver 1	I/O	local
9	GND1	Ground return for PSI5 interface (analog ground and substrate ground)	supply	local
10	PSI1	PSI5 Interface 1	I/O	global
11	V_{AS}	PSI5 Interface pre-regulated voltage supply	supply	local
12	PSI2	PSI5 Interface 2	I/O	global
13	GND2	Ground return for PSI5 interface (analog ground and substrate ground)	supply	local
14	BL2	Bootstrap capacitor pin 2, transceiver 2	I/O	local
15	BH2	Bootstrap capacitor pin 1 or SYNC voltage supply (from ECU), transceiver 2	I/O	local

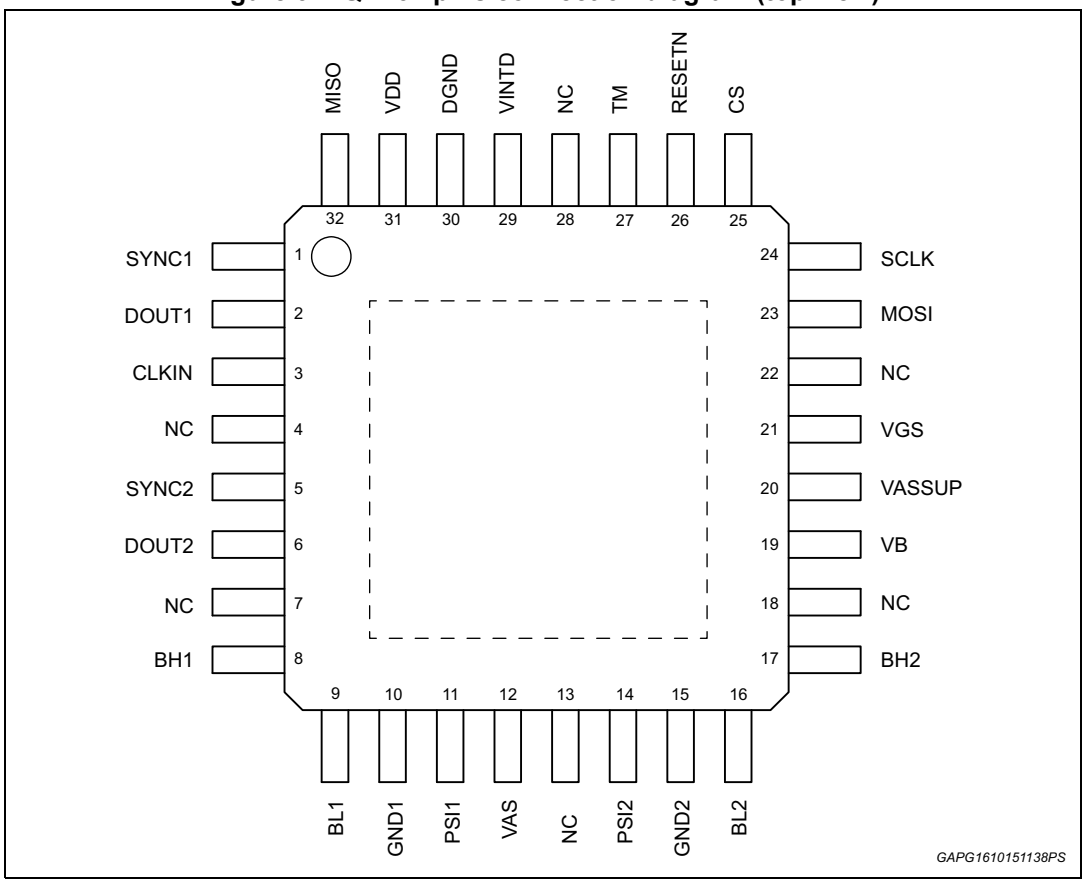
Table 2. VQFPN28 pin-out (continued)

Pin	Name	Description	Pin type	
16	V_B	Input voltage supply	supply	global
17	V_{ASSUP}	VAS pre-regulator and charge pump voltage supply	supply	global
18	V_{GS}	Gate driver for V_{AS} pre-regulator	I/O	local
19	NC(2)	-	-	-
20	MOSI	SPI input	I	local
21	SCLK	SPI Clock	I	local
22	CS	SPI Chip Select	I	local
23	RESETN	Reset	I	local
24	TM	Test-mode pin(3)	I	local
25	V_{INTD}	Internal digital supply voltage	supply	local
26	DGND	Digital ground	supply	local
27	V_{DD}	Digital I/O supply	supply	local
28	MISO	SPI output	O	local

1. Not connected internally, must be left open.
2. Not connected internally, it can be connected to GND externally.
3. It must be connected to GND, for safety reasons.

1.4 TQFP32 pins description

Figure 3. TQFP32 pins connection diagram (top view)



Note: The exposed pad is electrically shorted to the substrate and to pins GND1 and GND2. These three nodes have to be kept shorted on the application.

Table 3. TQFP32 pin-out

Pin	Name	Description	Pin type	
1	SYNC1	Direct interface sync pulse trigger 1	I	local
2	DOUT1	Direct interface 1/Interrupt 1	O	local
3	CLKIN	External clock input	I	local
4	NC(2)	-	-	-
5	SYNC2	Direct Interface sync pulse trigger 2	I	local
6	DOUT2	Direct interface 2/Interrupt 2	O	local
7	NC(1)	-	-	-
8	BH1	Bootstrap capacitor pin 1 or SYNC voltage supply (from ECU), transceiver 1	I/O	local
9	BL1	Bootstrap capacitor pin 2, transceiver 1	I/O	local

Table 3. TQFP32 pin-out (continued)

Pin	Name	Description	Pin type	
10	GND1	Ground return for PSI5 interface (analog ground and substrate ground)	supply	local
11	PSI1	PSI5 Interface 1	I/O	global
12	V_{AS}	PSI5 Interface pre-regulated voltage supply	supply	local
13	NC(2)	-	-	-
14	PSI2	PSI5 Interface 2	I/O	global
15	GND2	Ground return for PSI5 interface (analog ground and substrate ground)	supply	local
16	BL2	Bootstrap capacitor pin 2, transceiver 2	I/O	local
17	BH2	Bootstrap capacitor pin 1 or SYNC voltage supply (from ECU), transceiver 2	I/O	local
18	NC(1)	-	-	-
19	V_B	Input voltage supply	supply	global
20	V_{ASSUP}	VAS pre-regulator and charge pump voltage supply	supply	global
21	V_{GS}	Gate driver for V_{AS} pre-regulator	I/O	local
22	NC(2)	-	-	-
23	MOSI	SPI input	I	local
24	SCLK	SPI Clock	I	local
25	CS	SPI Chip Select	I	local
26	RESETN	Reset	I	local
27	TM	Test-mode pin(3)	I	local
28	NC(2)	-	-	-
29	V_{INTD}	Internal digital supply voltage	supply	local
30	DGND	Digital ground	supply	local
31	V_{DD}	Digital I/O supply	supply	local
32	MISO	SPI output	O	local

1. Not connected internally, must be left open.
2. Not connected internally, it can be left open or connected to GND externally.
3. It must be connected to GND, for safety reasons.

1.5 Maximum ratings

Within the maximum ratings, no damage to the component shall occur. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

All maximum ratings can occur at the same time.

All analog voltages are related to the potential at substrate ground (GND1 and GND2, internally shorted), all digital voltages are related to DGND.

Operative voltage conditions are specified in *Section 6*.

Table 4. Pin maximum ratings

Symbol	Description	Min	Max	Unit
Power supply				
V_B, V_{ASSUP}	Input voltage range	-0.3	40	V
V_{AS}	Pre-regulated voltage range	-0.3	40	V
V_{DD}	Supply voltage range for digital I/O pins	-0.3	6.5	V
V_{INTD}	Internal digital supply voltage	-0.3	4.6	V
BHx, BLx	Voltage range of bootstrap capacitor or SYNC voltage supply (from ECU)	-0.3	40	V
Other pins				
PSI1, PSI2	Voltage of sensor interface	-1.5	40	V
V_{GS}	Pre-regulator gate voltage range	-0.3	40	V
RESETN	Reset input pin range	-0.3	6.5	V
TM	Test mode input pin range	-0.3	6.5	V
CLKIN	Clock input pin range	-0.3	6.5	V
CS, SCLK, MOSI	SPI communication pin range	-0.3	6.5	V
MISO	SPI communication pin range	-0.3	V_{DD}+0.3≤6.5	V
D_{OUT1}, D_{OUT2}	Direct interface pin range	-0.3	V_{DD}+0.3≤6.5	V
SYNC1, SYNC2	Sync pulse trigger input range	-0.3	6.5	V
ESD robustness				
-	ESD according to Human Body Model (HBM), Q100-002 for pins PSIx, VB, VASSUP; (100 pF/1.5 kΩ)	±4000	-	V
-	ESD according to Human Body Model (HBM), Q100-002 for all other pins; (100 pF/1,5 kΩ)	±2000	-	V
-	ESD according to Charged Device Model (CDM), Q100-011 Corner pins	±750	-	V
-	ESD according to Charged Device Model (CDM), Q100-011 Non-corner pins	±500	-	V

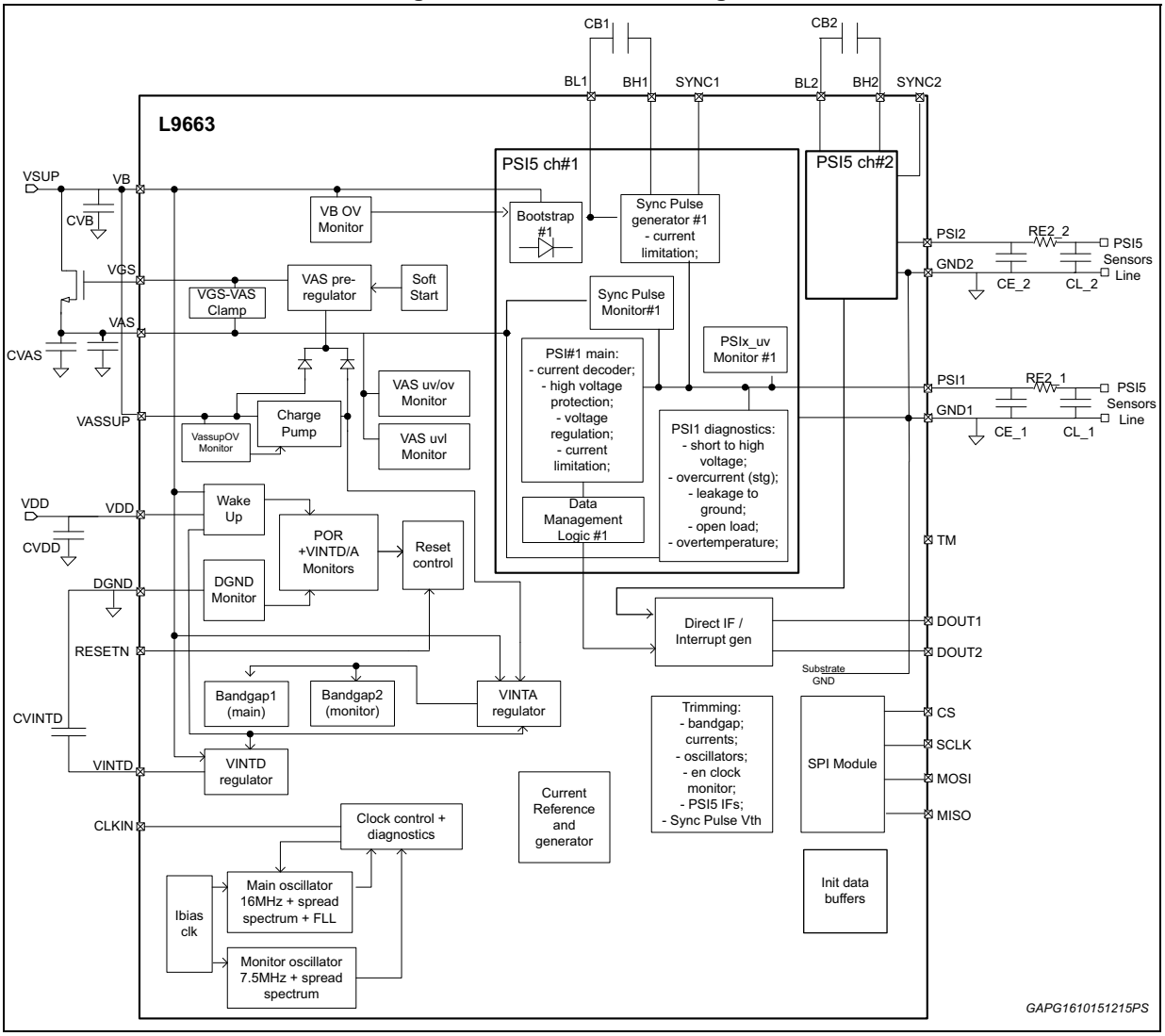
Table 4. Pin maximum ratings (continued)

Symbol	Description	Min	Max	Unit
Temperature				
T_a	Ambient operating temperature range	-40	140	°C
T_j	Junction operating temperature range	-40	175	°C
Rthja	Package thermal resistance (on PCB JEDEC 2s2p)		45	°C/W

The device offers a high level of flexibility on power supply configuration. The calculated maximum power dissipation can reach 1.6 W considering the worst case configuration.

1.6 Detailed block diagram

Figure 4. Detailed block diagram



The high supply voltage of the IC can be a battery or a regulated voltage provided by the ECU.

To reduce disturbances on the voltage supply which might have a negative influence on the PSIx interface and therefore lead to bit errors, a PI filter can be employed in the supply line.

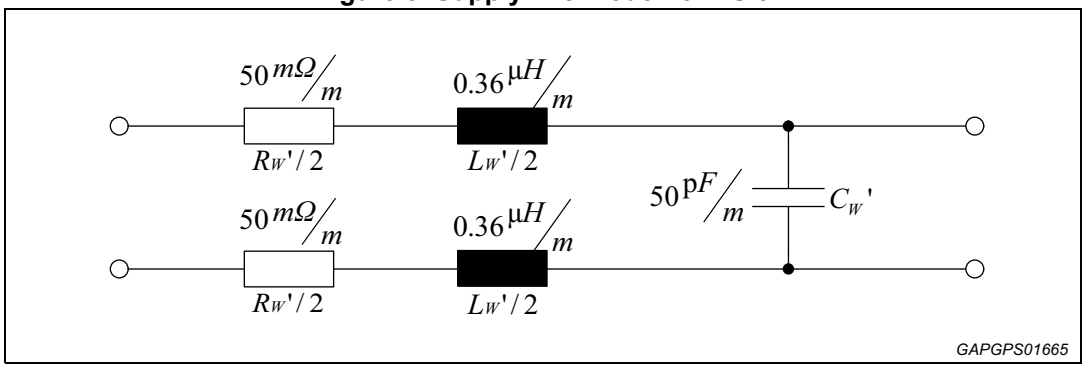
Possible power supply configurations[b] are:

- VB, VASSUP connected to VSUP, VAS and V_{SYNCx} generated by the IC with external components (as in the above figure);
- VAS, VB, VASSUP connected to VSUP, V_{SYNCx} generated by bootstrap, no external MOS, VGS pin open;
- VB, VASSUP, BH1, BH2 connected to VSUP, no external capacitors CBx, VAS generated by IC pre-regulator and external MOS;
- VB connected to VSUP, VASSUP connected to 0V (charge pump off), VAS supplied by an external source and VSYNCx generated by the IC with external components.

The values of the external components RE2_x, CE_x and CL_x are specified in PSI5 standard.

The assumed line model for the PSI5 interface on which the transceiver IC operates is as follows:

Figure 5. Supply line model for PSI5



b. The high supply voltage VSUP must be in the correct operative range of connected pins.

1.7 Power up sequence

When VDD is higher than the startup threshold and VB is available the IC is switched on.

To reduce disturbances on its voltage supply, the transceiver IC does a staggered startup of its internal voltage supplies.

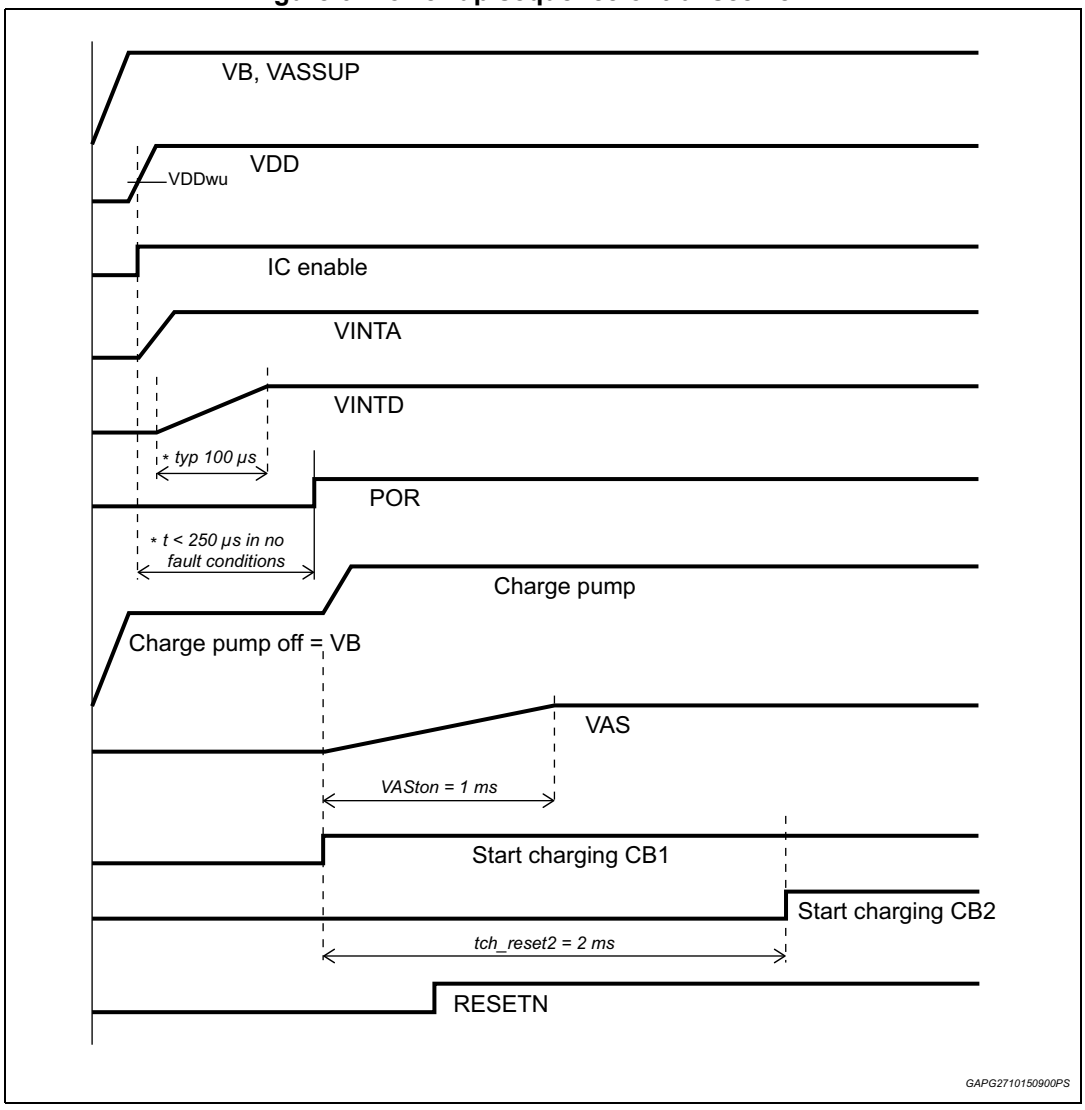
While RESETN is low, the PSIx lines are deactivated to reduce power consumption and to increase system safety.

The transceiver IC can be configured to operate in the standard current mode (4 mA up to 19 mA) or in the extended current mode (4 mA up to 35 mA). Moreover, both channels can be configured to allow the extension to a maximum quiescent current of 45 mA, only in case of asynchronous mode.

The synchronous sensors send data only after a synchronous pulse is triggered via the dedicated pin or by SPI.

The following figure shows a power-up example.

Figure 6. Power-up sequence of transceiver IC

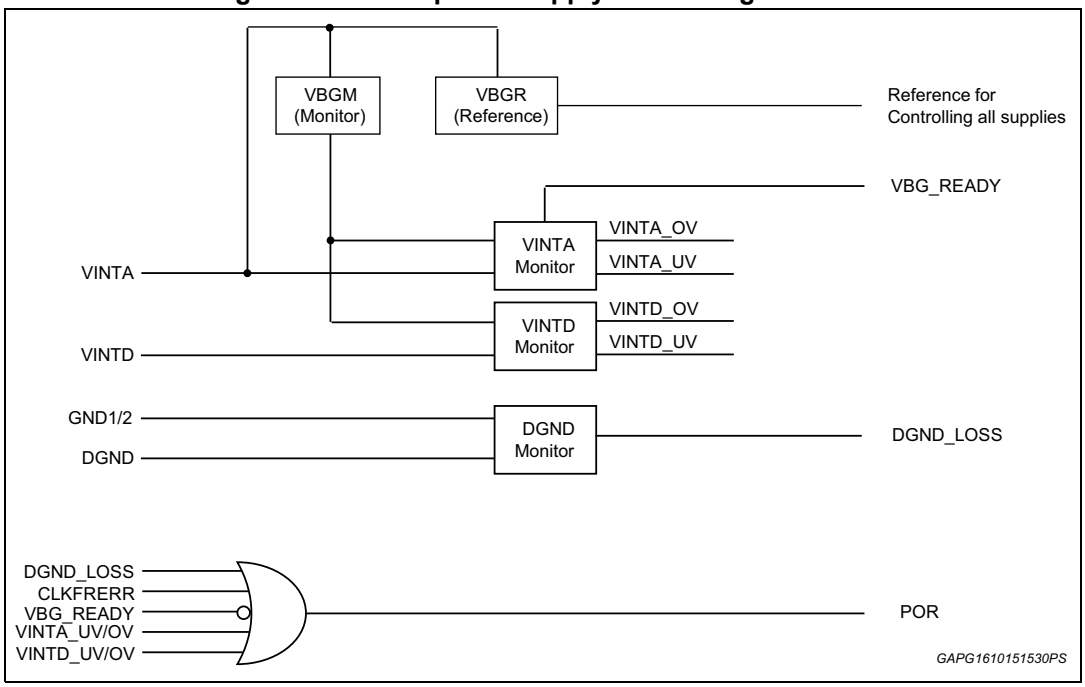


2 Power supply

2.1 Internal supply

The internal analog and digital part is supplied by the supply voltage VB. The necessary power supply for the internal digital and analog parts is generated internally by the transceiver IC. The generated voltage is monitored. In case of under/over voltage, the transceiver IC performs a power on reset (POR).

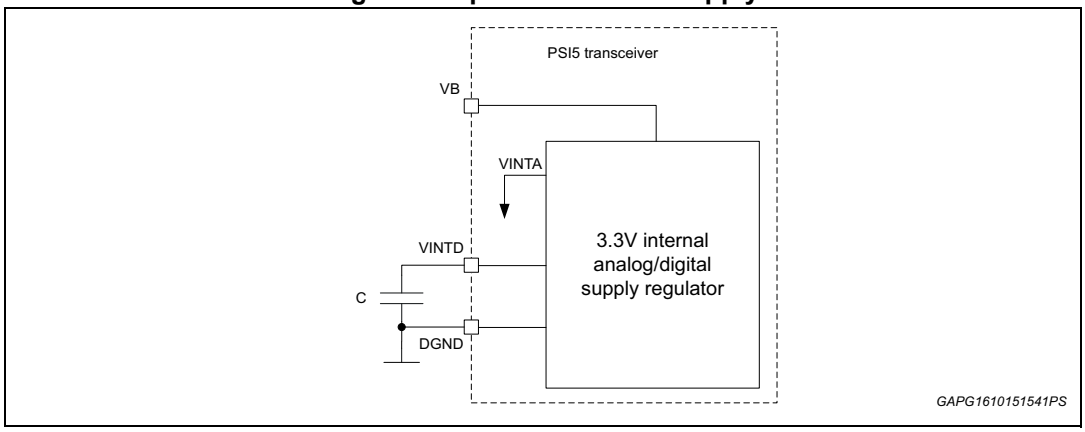
Figure 7. Internal power supply and reset generation



Basic features:

- Voltage regulator
- Under / Over voltage monitoring
- Reset generation of the IC in case of under / over voltage

Figure 8. Input structure of supply



A ceramic capacitor with a typical capacitance of 100 nF is required as a blocking capacitor close to the pins V_{DD} and VB.

The internal supply voltages V_{INTD} (supply voltage for digital part) and V_{INTA} (supply voltage for analog part) are monitored for under voltage and over voltage to prevent the transceiver IC from malfunction. The reference for the voltage monitoring is a bandgap voltage, supplied by V_{INTA}. The device integrates two separated instances of bandgap voltage regulators; one of these bandgaps is used as voltage reference for the internal regulators, while the other one is used for monitoring the voltage levels. In case of under or over voltage, the transceiver IC is set into reset: outside reset thresholds full functionality is granted.

The functionality of the digital part only depends on the voltages on V_{INTD}. In order to improve noise emissions and stability of the regulator, the digital supply line needs an external decoupling 100 nF ceramic capacitor to be connected between V_{INTD} and DGND and close to them.

DGND ground line is protected against ground loss scenarios. In case DGND line would be at least $DGND_{OPEN}$ above the reference ground lines GND1/2, a POR is asserted.

The transceiver IC returns to normal operation with full functionality as soon as the POR is released.

2.2 V_{AS} supply and pre-regulator

The V_{AS} pre-regulator sets the V_{AS} voltage if no regulated voltage with the necessary value is available in the ECU.

The pre-regulator is designed for two different regulated voltages at V_{AS}: 5.3 V or 7.6 V, selectable by a SPI command. The supply of external FET can be chosen at application level according to the required voltage at VAS pin.

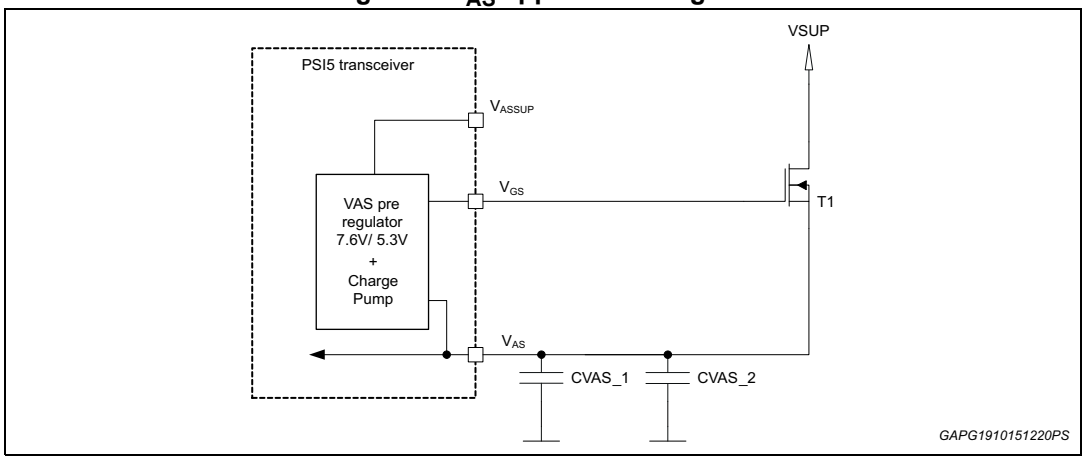
Two possible applications are:

- V_{AS} typical of 5.3 V; external FET supplied by ECU internal voltage, typically 6 V .
- V_{AS} typical of 7.6 V; external FET directly supplied from battery, from 8 V to 35 V.

Basic features:

- Gate control for an external n-ch FET transistor with integrated charge pump stage
- Gate control is switched on if no power on reset condition is present
- Configurable output voltage: either 5.3 V or 7.6 V.

Figure 9. V_{AS} application diagram



When POR is active, the V_{GS} output pin is driven low to keep external N-ch switched off. The V_{AS} pre-regulator is automatically activated with a soft start at POR and automatically switched off, after a filter time, if V_{AS} falls below V_{VASU_off}. It can be later controlled off or on by means of a dedicated VAS_EN bit. To protect the external component from exceeding maximum allowed gate to source voltage if VAS is shorted to ground by a fault, an internal passive clamp is implemented on V_{GS}.

The integrated charge pump, supplied by VASSUP, assures proper voltage regulation in case of low voltage conditions. It is automatically switched off in case the voltage on V_{ASSUP} is high enough to allow proper regulation.

If the pre-regulator is not needed, the VAS_EN bit can be set to '0' to switch off the pre-regulator itself. The pin V_{GS} can be left open, and the V_{AS} pin directly connected to the regulated voltage in the ECU.

The pre-regulator is active independently of RESETN input pin if the supply voltage of the internal analog/digital circuits is available.

2.3 Voltage supply for synchronous pulse generation V_{SYNCx}

To use synchronous PSI5 sensors and for ECU-to-sensor communication, the transceiver IC needs to generate synchronization pulses. These require a voltage which is higher than V_{AS}.

This module generates the necessary voltage V_{SYNCx} by two bootstrap circuits. Two capacitors with two transceiver IC pins each are used as external components of this module.

The bootstrap blocks start pre-charging the external capacitors after POR (with a 2 ms time gap between the first and second block).

The bootstrap circuits are enabled by default, activated by internal logic with timing sync pulses dependent, and can be disabled later on through a dedicated SPI command. The bootstrap block can recharge the capacitor so that subsequent sync pulses are allowed with a minimum period of 200 µs.

A useful option is the possibility to connect the BHx pin directly to a high voltage rail. In this configuration, VB has also to be connected to the same high voltage rail and the bootstrap

circuit can be bypassed by disabling it through the dedicated SPI command (bit 12 of CH1_CR2, CH2_CR2, writable during PROG phase).

The bootstrap blocks are automatically switched off in case the voltage on VB is high enough to allow proper regulation. In this case both CBx capacitors should be omitted.

The V_{SYNCx} voltage can supply a 2.5 V minimum sync pulse as per PSI5 v2.x low power mode down to V_B = 4.8 V and a 3.5 V minimum sync pulse down to V_B = 5.2 V, with a maximum quiescent current level of 35mA and down to minimum 200 µs period between sync pulses. The block is protected against reverse feeding to V_B.

The bootstrap module is fully functional while V_B and V_{DD} are all inside their specified voltage ranges.

2.4 Power supply for PSI5 sensor line

Basic features:

- Reverse voltage protection structure
- Voltage limitation and current limitation for PSIx input/output
- Protection against negative voltages on PSIx transceiver pin due to ground shifts
- Disconnection of PSIx from V_{AS} in failure cases

The PSI5 transceiver IC is supplied directly from the pin V_{AS}. It includes blocks with the following functionalities:

- Reverse voltage protection structure and gate driver block for
  - Voltage clamp on PSIx in case of V_{AS} fault
  - Backward voltage supply blocking mechanism from PSIx to V_{AS}
  - Sensor supply by switching V_{AS} to the PSIx pin
  - Disconnection of PSIx from the VAS if required or in failure cases
- Under voltage detection block to implement cross coupling test between the two channels (see *Section 3.7.5* and *4.2*)
- Receiver block for Sensor Data receive (see *Section 3.1* for details).

The reverse voltage protection structure is also used to switch off the PSIx transceiver channel, if:

- the local junction temperature exceeds its maximum rating and the channel is in overcurrent
- an overcurrent condition on PSIx is detected (STG)
- a short to battery is detected
- it is requested via SPI or RESETN pin.

In case of short to battery on the PSIx lines, there is no interference to any other IC pin/supply including SPI.

The two interfaces can be enabled by SPI command, and the enable has effect only if VAS under voltage signals are not asserted.

If an over temperature condition (OT) occurs, the interface that is also in overcurrent condition is switched off and a failure bit is set. The fault bit is latched and cleared only when a SPI switch off command is sent for confirmation on the line that was automatically switched off. The shutoff of one interface does not affect the second interface.

If an overcurrent condition on PSIx is detected, the current limitation is active and after a filter time t_{filt} a fault bit is set and the interface is shut off. In order to switch on again, the interface must be first switched off by SPI and then switched on, as for over temperature.

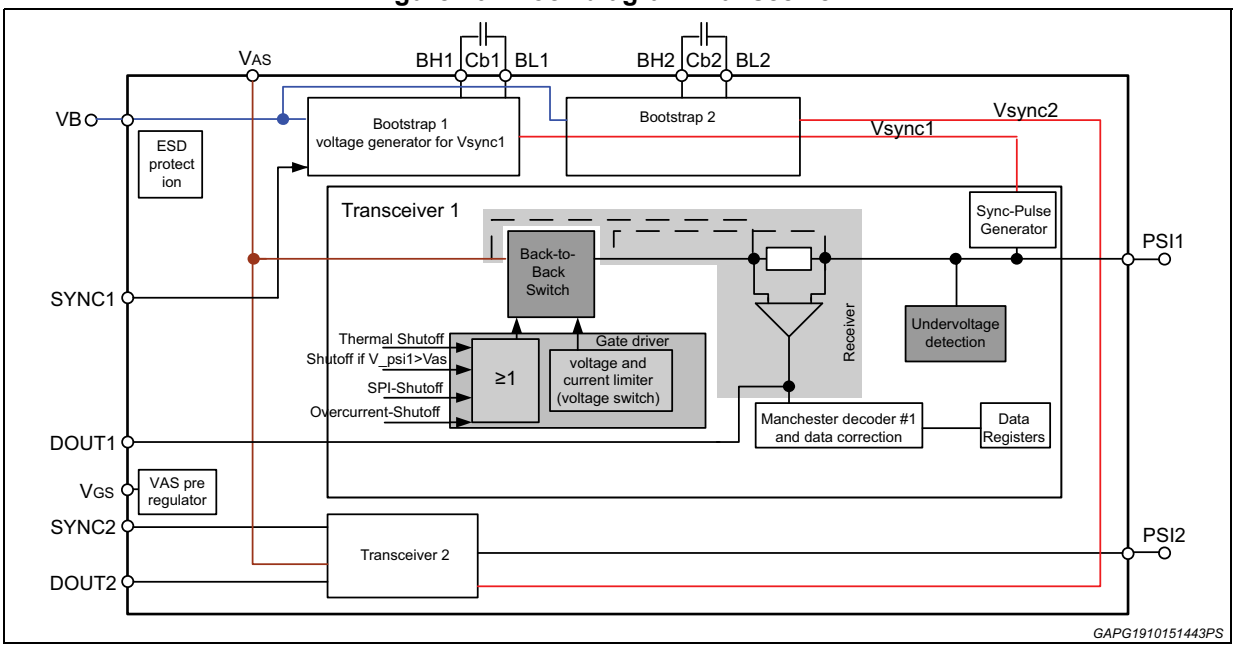
The channels' switch off by overcurrent can be disabled if the corresponding bits STG_MASK for every channel are set in the SPI registers.

During start up, a configurable blanking time is implemented (128 µs/5 ms/10 ms, see BLANKING_SEL bits in SPI register); during this time current limitation is active, even though the interface will not shut off for overcurrent, thermal shutdown is always active, the PSI5 receiver is disabled, and some fault flags are masked (short to battery, under voltage, leakage to ground).

The quiescent current is monitored for minimum and maximum value, depending on the range selected by SPI (CH1_CR1, QC_SEL bits). In failure case the corresponding bit in the diagnostic register is set (SR2).

The voltage at PSIx is compared with VAS to monitor short to battery condition: if an over voltage occurs PSIx is disconnected from VAS and the corresponding bit in diagnostic register is set (STBx in SR2), In over voltage condition also low quiescent current bit is set (OLx in SR2) after a transient time.

Figure 10. Block diagram Transceiver 1



2.5 Frequency references

The device comes with an integrated accurate oscillator, used for any of the internal circuitry, with no need of external connections or components. The nominal clock frequency is 16 MHz with a ±5% accuracy.

Should the application need some more accurate timing reference, a discrete pin CLKIN is provided. An external clock reference can be connected to this pin. The PSI5 transceiver IC offers an integrated FLL module that tracks this input to provide a high accurate clock reference (±1%). This feature can be used especially if accurate timeslot control needs to be achieved.

External signal on CLKIN can be configured as follows (see CLKIN_CFG bits in GCR1 SPI register):

- 1 MHz square signal
- 4 MHz square signal
- No signal (Not connected pin)

Pin CLKIN can be grounded when not used. The pin input circuit implements a pull-down structure.

The FLL module tracking the CLKIN signal is off by default.

The PSI5 transceiver IC implements a safety function for monitoring the device clock reference, both in case it is derived from the CLKIN signal through the FLL module or internally generated. In the first condition the monitoring is always activated, while in the second condition it can be enabled by programming in ST (storing a '1' in a dedicated OTP[c] bit) and another oscillator generator is used for monitoring.[d]

When the CLKIN_CFG is set, the FLL tries to close the LOOP and a mask counter of T_CKMSK (16 ms MAX) is used to count the maximum transient time.

During this time, regardless of the CLK frequency the CKER_DETECT is masked, i.e the device doesn't detect a clock error.

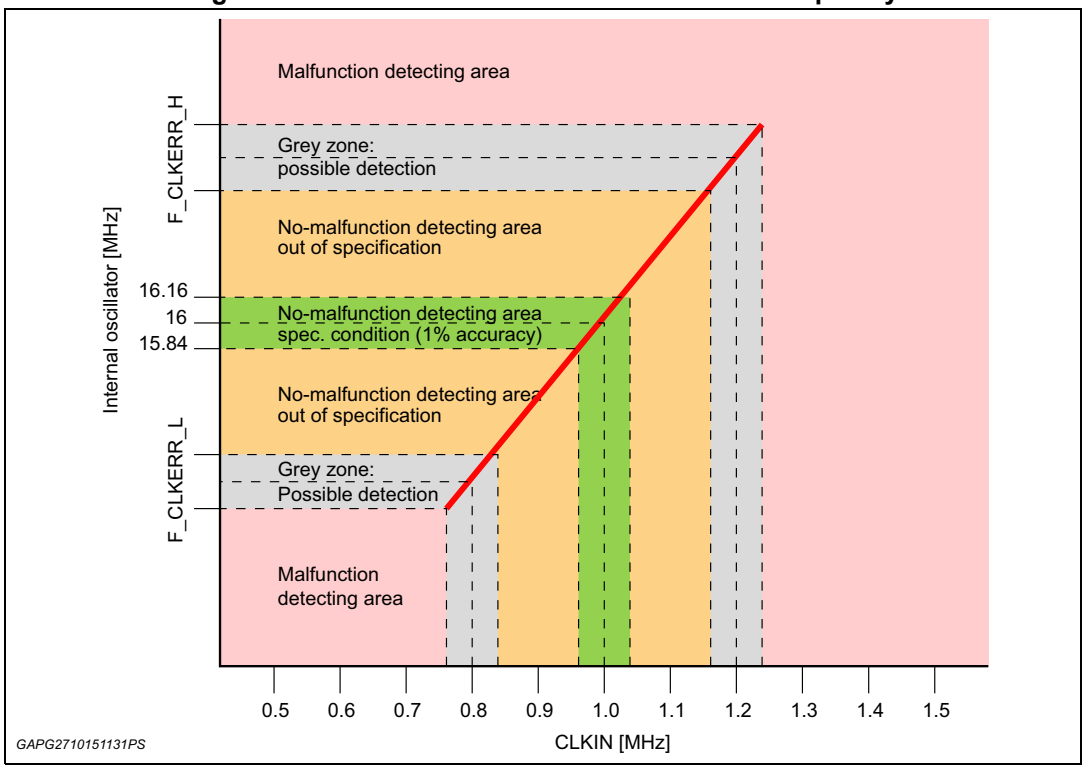
After this time, if the CLKIN frequency is in the correct range, the loop is closed and the CLK frequency is inside the 1% tolerance; if the CLKIN frequency is outside the malfunction detecting range, a clock error is detected after a detection time T_CKERD, the device is reset and the CLK_FLT is set so that the µC can read the reset source.

The T_CKERD and the transient during detection time depend on the CLKIN frequency behavior; the figure below shows the behavior of the internal oscillator as function of the external one.

c. One Time Programmable bit: it can be programmed by ST only.

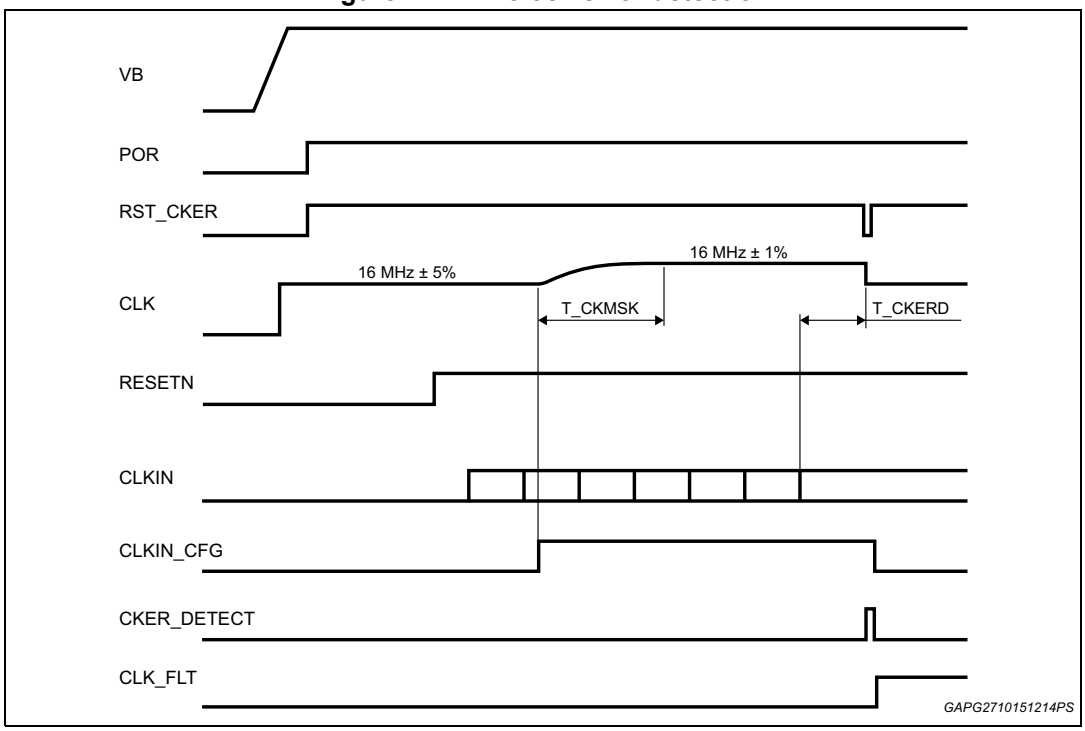
d. For clock error detection by internal monitor oscillator see errata n.3367, *Section 7: Errata*.

Figure 11. Internal oscillator vs external clock frequency



If the CLKIN is stuck the device behavior is shown in the figure below: in this case during the detection time the tolerance is still inside the 1% tolerance until the device enters reset (T_CKERD max 260 µs).

Figure 12. FLL clock error detection



2.6 Reset handling

Four different sources are considered in resetting the IC:

- POR (Power On Reset, see *Section 2.1*)
- RESETN pin
- SW_RESET
- CKER_DETECT

All these sources of reset, when asserted, will switch off the PSIx lines and reset to default value the device registers (including those registers for configuration).

Additionally to the hardware resets (by pin/POR), a reset can also be initiated by software (SW_RESET).

The command SW_RESET initiates a soft reset-sequence if all of the following conditions are fulfilled (see also the DCR register in SPI section):

- unlocked state: it means that if the UNLOCK command is not received the command SW_RESET has no effect;
- The command SW_RESET is sent in the next SPI communication of the unlock command.

A SW_RESET initiates soft reset-sequence and resets all digital parts of the device, except POR and RST flag that is set in SR3 register.

3 Satellite interface

3.1 Receiver with digital sampling and filtering

This module has the following features:

- The output current signal is mirrored and converted to the digital domain
- Automatic synchronization on entire PSI5 frames
- Fast DAC digital conversion of sensed currents with digital filtering
- Static DC current set point tracking of PSI5 quiescent current.
- Tracking of modulated PSI5 current signal

The quiescent current tracking can be configured to work in two ways (reg. ADVSET1, ADVSET3, bits FREEZE_DIS): continuous mode tracking or tracking between consecutive frames till the first edge of a new frame is recognized. In the second case, the quiescent current is frozen till the end of the frame.

To recognize the PSI5 current signal level the receiver compares the digitally converted and filtered current with a threshold. This threshold can be fixed or dynamic, depending on the configuration selected by SPI (reg. ADVSET).

In fixed threshold mode the user must program the right delta current threshold, according to the application requirements. The threshold is obtained as tracked quiescent current plus the programmed threshold.

In dynamic threshold mode, the threshold is dynamically adapted considering the PSI5 current input signal.

For detailed explanation on all the possible configurations refer to ADVSET registers section.

Depending on the selected configuration, the threshold for the sensor signal can be permanently tracked, separately for each PSI5 interface. The IC is designed to compensate erratic changes of the quiescent current in the bus according to PSI5 standard requirements.

The v2.x standard low power mode is not supported with dynamic threshold mode.

Micro cuts up to 10µs do not affect the DC current tracking in a way that more than one frame will be lost.

The PSI5 Receiver is designed to operate at:

- 83.3 Kbps typical (slow mode)
- 125 Kbps typical (standard mode)
- 189 Kbps typical (fast mode).

3.2 Manchester decoder and error detection

Basic features:

- Detection of start bits "00"
- Synchronization with sensor to ECU frame
- Manchester decoding according to PSI5 specification (v 1.3 or v 2.x, depending on the chosen configuration)

The Manchester decoder takes the bit stream which the receiver has as its output and decodes the incoming data frames from this bit stream.

It can be programmed to measure the period of start bits sent by the sensors and double-check the timing of the following data bits with respect to the synchronization given by the start bits or to validate the data bits according to the PSI5 protocol baud rate configured by the microcontroller. The tolerance for timing checks is 20%: in case of timing error a Manchester error is reported.

A Manchester Decoder Error occurs if one or more of the following are true:

- Start bit error outside of selected operating range
- Data length error or stop bit error
- Bit time error (a data bit edge is not received inside the expected time window)
- Timing violation on slot when standard timeslot monitor is enabled

In case a Manchester error is detected the corresponding error code is set [v. Error codes table, *Section 3.3.2*].

3.3 Receive block

This block includes the buffer for incoming sensor data and diagnostic results. It includes:

- PSI5 receive registers
- Sensor data buffer
- Interrupt generation for the microcontroller

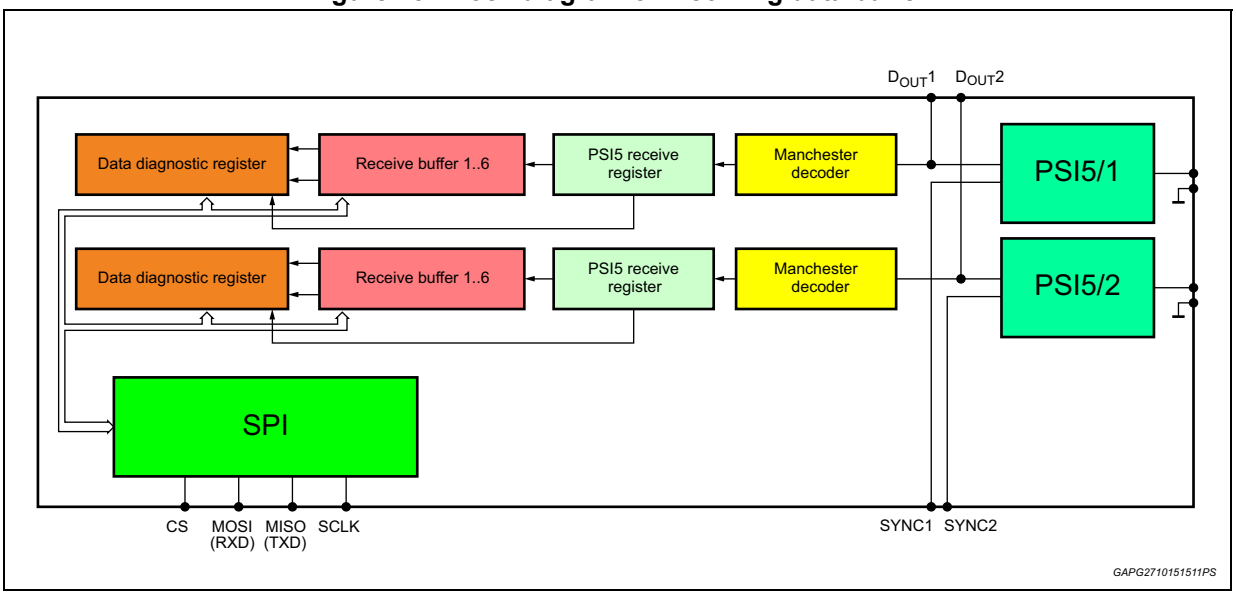
3.3.1 PSI5 receive register

This module includes the sensor data storage and diagnostic.

Basic features:

- Storage of Sensor data
- Error handling

Figure 13. Block diagram of incoming data buffer



PSI5 Receive Register

The transceiver IC has a PSI5 Receive Register for each PSI5 transceiver.

Each PSI5 Receive Register can store up to 28Bit data and up to 3Bit error check (CRC or parity) for each of the incoming frames. According to the PSI5 powertrain substandard, up to 6 frames can be sent between two synchronous pulses. For every frame, a frame configuration register is available which defines:

- Data Region 8 … 28 bit
- CRC or Parity Bit (3 or 1 bit)

Depending on the desired configuration (SPI bit CRC_CK of GCR1 register), the parity/CRC bits handling can be done in the following ways:

- Parity/CRC bits are generated by the sensor; the transceiver IC simply passes data+parity/CRC bits to the µC via SPI and the µC performs parity/CRC check
- Parity/CRC bits are calculated by the transceiver IC and in case of a correct parity bit/checksum, the payload of the frame is stored in the receive buffer; otherwise, if the CRC calculation shows a wrong result, the Parity Error code is stored.

The SPI register bit CRC_CK is valid for all sensors of both interfaces.

After all bits have been received the data will be transmitted into the corresponding part of the receive buffer.

Each PSI5 data frame consists of a total p bits containing:

- two start bits (S1 and S2),
- one parity bit (P) with even parity or alternatively 3 CRC bits (C0, C1, C2), and
- a data region (D0 … D[k-1]) with k = 8…28 bit.

The total length of a PSI5 frame is p=k+3 data bits (in case of frames with parity bit) or p=k+5 data bits (in case of frames with CRC).

Data bits are transmitted LSB first. The parity or CRC check bits cover the bits of the entire data region.

Figure 14. PSI5 v1.3 frame

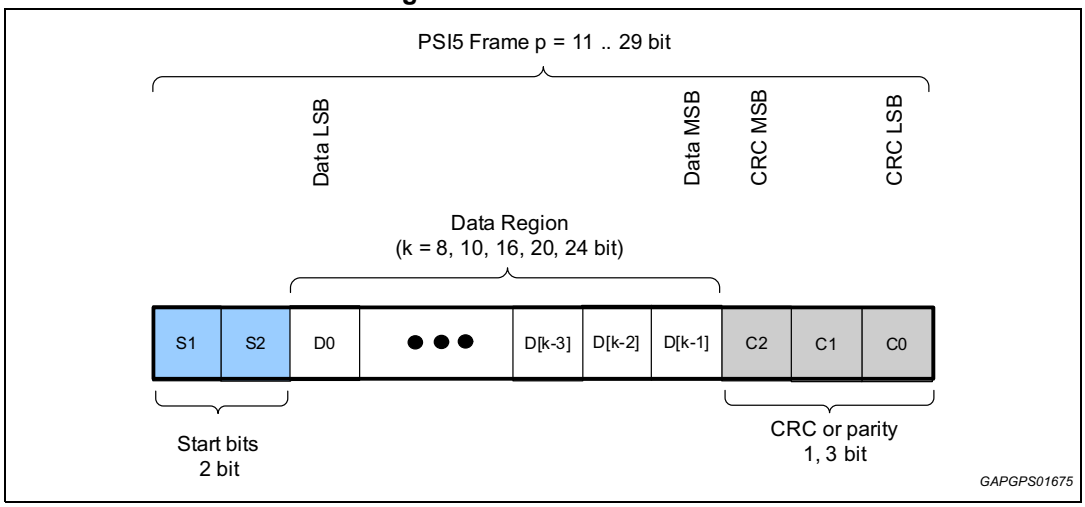
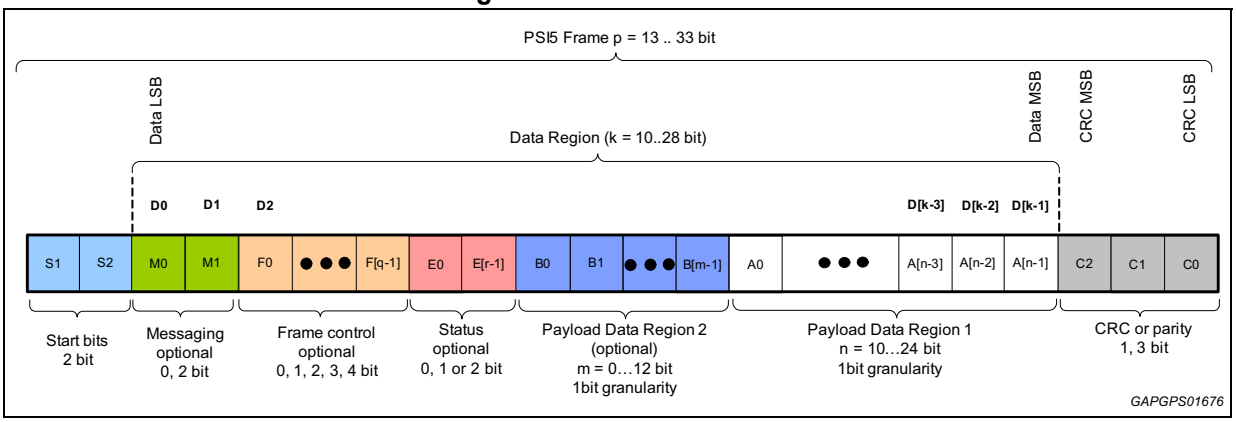


Figure 15. PSI5 v2.0 frame



In case of PSI5 v2.x, the length of the data region can vary between k = 10 … 28 bits, with 1-bit granularity. The data region can be split into the following fields and regions:

- Signal payload region 1 with data bits A0 … A[n-1] (scalable n = 10…24 with 1-bit granularity)
- Signal payload region 2 with data bits B0 … B[m-1] (scalable m = 0…12 with 1-bit granularity)
- Sensor status E0.. E[r-1] (optional r = 0, 1 or 2 bit)
  - This optional status bit can be used to show that the data of the current frame are faulty.
- Frame control, type of frame F0, …F[q-1] (optional q = 0, 1, 2, 3 or 4 bit)
  - This frame control can be used to number the frames which are sent after a sync pulse.
- Serial (slow) messaging channel (optional) M0, M1 (optional 0 or 2 bit)

Time slot monitoring

The time slot monitoring is active only in synchronous mode.

The time slot monitoring is required to check if the sensors connected to the transceiver work properly in terms of timing, i.e. if they are sending data frames within their defined time slot.

Basic features:

- 3 configurable modes
- Failure bit

During a synchronous pulse period (T_{SYNC}), a maximum number of 6 frames can be configured. Each frame has its own time slot, to be configured through dedicated configuration registers. The registers contain the reference time needed to check if the sensor data is transmitted during the defined time slot.

The resolution of time slots is 1 µs. The time slot monitoring timings are applied starting from the internal sync pulse trigger. This internal trigger falls t_{d_SPI} (or t_{d_SYNC}, depending on sync pulse trigger configuration) after the external one (via SPI or SYNC pin).

Three different configurations for the time slot monitoring are available:

- Standard configuration: monitoring the correct start and end time of a unique frame within a time slot
- Simple configuration: monitoring only the end time of a frame within a time slot
- No monitoring configuration: monitoring is disabled and data are stored in successive slots.

The time slot monitoring can be activated/deactivated separately for each interface (registers CHx_CR1, bits TSMx_SEL).

In case of standard configuration, the IC accepts as valid frame in a timeslot only a frame which starts and ends within its timeslot; if more than one valid frame is received within its timeslot, only the last one received is kept.

On the other side, in case frames span across slots, the frame is discarded and the error code 1FC (timing violation) is stored in the correspondent buffer; in this case the decoder is reset at every slot start. After this reset if a frame was being decoded, a slot error is set in the previous slot but no slot error is set. Then the Manchester FSM after reset checks again

for two valid start bits and so a new incoming frame can be stored without error in the new timeslot.

In the simple configuration, the last valid message which ends in a timeslot is stored in the buffer of the slot (so if a frame is currently stored in a timeslot and an incoming frame ends in this timeslot, the old data are overwritten). In this mode slot error is never set.

It is also possible to disable the time slot monitoring and in this case, no timing check is done: the first frame is assigned to the first buffer, the second to the second, and so on. This means that the buffer index is incremented every time a frame is received both valid and invalid (Manchester communication error).

After reset, the default mode for the time slot monitoring is "monitoring disabled".

3.3.2 Sensor data buffer

To avoid loss of data, a data buffer for each PSI5 transceiver is necessary. While the data buffer is being read by SPI, at the beginning of the sensor data transfer the data register is cleared and a new data frame can be accepted.

The incoming PSI5 sensor data, together with CRC and SID/GBIT (if selected) are written into a receive buffer, which is large enough to hold the data of one sync pulse cycle (i.e. up to six sensors). In order to avoid data-mixing between different cycle times the data must be fetched by the µC before the next transmission cycle starts.

The figure below shows how sensor buffers are updated in synchronous mode.

At t_0 the buffers contain no data; then a sync pulse is sent and data are received and stored in each register during the cycle time; so at t1/t2 the buffers contain sensors data of the current cycle time.

Figure 16. Sensor buffer in synchronous mode diagram

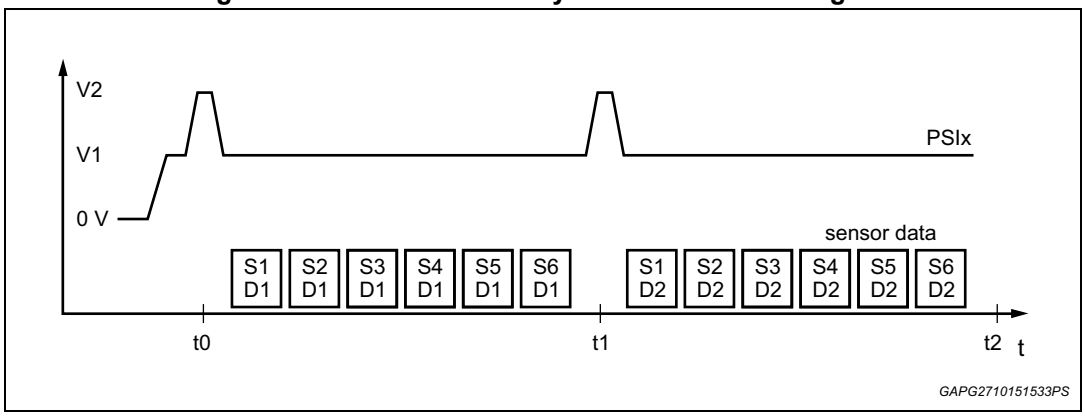


Table 5. Time (t0-t2) vs SensorData

Time/Sensor	t0	t1	t2
SensorData1	Buffer Empty	D11	D12
SensorData2	Buffer Empty	D21	D22
SensorData3	Buffer Empty	D31	D32
SensorData4	Buffer Empty	D41	D42

Table 5. Time (t0-t2) vs SensorData (continued)

Time/Sensor	t0	t1	t2
SensorData5	Buffer Empty	D51	D52
SensorData6	Buffer Empty	D61	D62

In case of sensor or channel fault conditions, the following codes are sent in the first 10 bits of the data field. The lower 10 bits are filled with '0'.

Table 6. Error codes in sensor communication

Error Code	Definition
1FC	Manchester error (non-valid start bits, incorrect number of bits received, timing violation)
1F8	Parity / CRC error(1)
1F1	Physical layer error (short to ground, leakage to GND, over-temperature, open load)
1F0	Data buffer empty
1F2	Short to battery
1F9	Sync pulse error

1. Used only in case the CRC check computation is assigned to the IC (CRC_CK bit set to 1); otherwise the sensor data will be written in the buffer.

If more than one data is present, the faults are handled with this priority scale:

Table 7. Faults priority

Priority	Data	Fault type	Code
1 (highest)	Valid data	-	-
2	Over Temperature	channel	1F1
3	Short To Ground	channel	1F1
4	Short To Battery	channel	1F2
5	Leakage To Ground	channel	1F1
6	Open Load	channel	1F1
7	Manchester Error	Sensor related	1FC
8	CRC/Parity Error	Sensor related	1F8
9	Sync Pulse under voltage (both Slow Vsync detection and sync UV faults)	channel	1F9
10	Data Buffer Empty	Sensor related	1F0

In synchronous communication mode each sensor (time slot) has its own range in the data buffer. The buffer range content is overwritten if new data arrives before the old data has been read out.

If a channel fault occurs, the content of every sensor buffer is affected regardless of the moment inside the timeslots cycle in which the fault occurs. This value will be held until the fault is cleared (reading the appropriate bit in the Status Register) or a fault with higher priority occurs.

In asynchronous communication mode a six stages FIFO is implemented: the newest data is always in the data buffer range corresponding to sensor no. 1, the oldest data is in the data buffer range corresponding to sensor no. 6. When the buffer is full, the FIFO shifts the incoming data to keep always the newest data. As soon as the first data is read by SPI, the FIFO will be locked to writing, until it is emptied[e]. This situation is reported through SPI bit FIFO_LCK.

Figure 17. Sensor buffer in asynchronous mode diagram

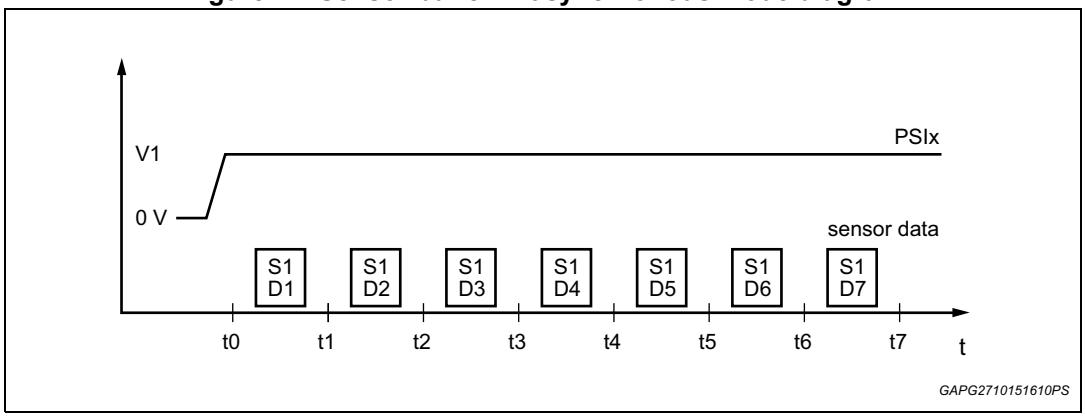


Table 8. Time (t0-t7) vs SensorData

Time/Sensor	t0	t1	t2	t3	t4	t5	t6	t7
SensorData1	Buffer Empty	D1	D2	D3	D4	D5	D6	D7
SensorData2	Buffer Empty	Buffer Empty	D1	D2	D3	D4	D5	D6
SensorData3	Buffer Empty	Buffer Empty	Buffer Empty	D1	D2	D3	D4	D5
SensorData4	Buffer Empty	Buffer Empty	Buffer Empty	Buffer Empty	D1	D2	D3	D4
SensorData5	Buffer Empty	Buffer Empty	Buffer Empty	Buffer Empty	Buffer Empty	D1	D2	D3
SensorData6	Buffer Empty	Buffer Empty	Buffer Empty	Buffer Empty	Buffer Empty	Buffer Empty	D1	D2

If a fault occurs and FIFO is unlocked, the correspondent code is written in the FIFO buffer at the current position; if more than one fault occurs at the same time the fault with the highest priority is written in the FIFO.

In both synchronous and asynchronous mode, when a valid data is read, the buffer empty code 1F0 is written in the buffer.

e. For the lock of the FIFO see errata n.1526, *Section 7: Errata*.

As safety feature, the IC always checks that after a valid data read the code 1F0 is written in the buffer.

If this check fails a Buffer Empty Fault is latched (BEx bits in SR2 register) and it's cleared after SPI read. Buffer empty fault asserts also Global Status Bit.

In order to allow the µC to test this feature a test of buffer empty check is implemented (see *Section 3.7.3* and STSR register for details).

3.3.3 Interrupt generator

The microcontroller interrupt module describes the function of the interrupt pins to generate a microcontroller interrupt if the data buffers are filled with sensor data.

Basic features:

- Configurable interrupt pins
- Interrupt generation when data buffer is full

The interrupt pins generate an interrupt for the microcontroller if the receive buffer corresponding to a transceiver interface is filled completely: the interrupt pin is then reset when the receive buffer is empty.

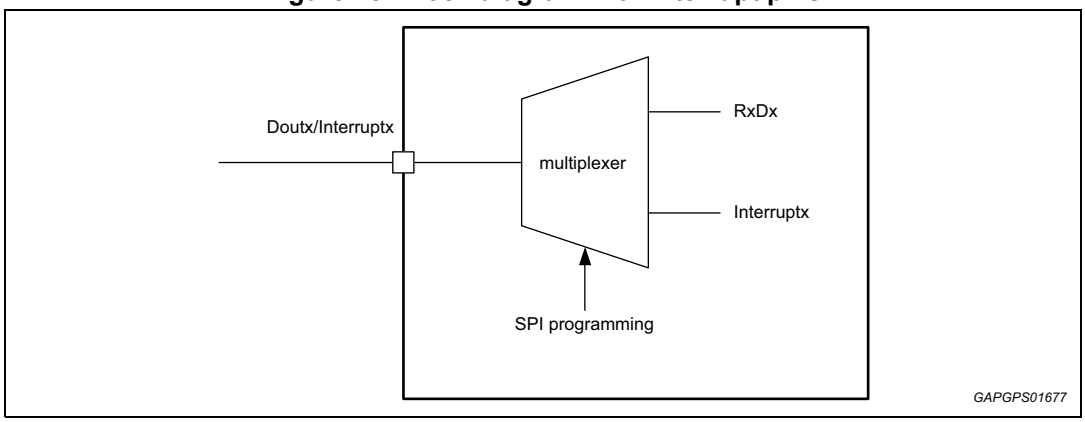
Asynchronous operation:

The interrupt pin is set to high when the number of received data since the last reading of register is as large as the size of the receive buffer. The interrupt pin is set to low when all the buffers are empty.

Synchronous operation:

The interrupt pin is set to high when all the buffers configured by SPI are full. The interrupt pin is set to low when all the buffers are empty.

Figure 18. Block diagram with interrupt pins



After reset, the output pin is configured as DOUTx.

3.3.4 Automatic storage of sensor initialization data

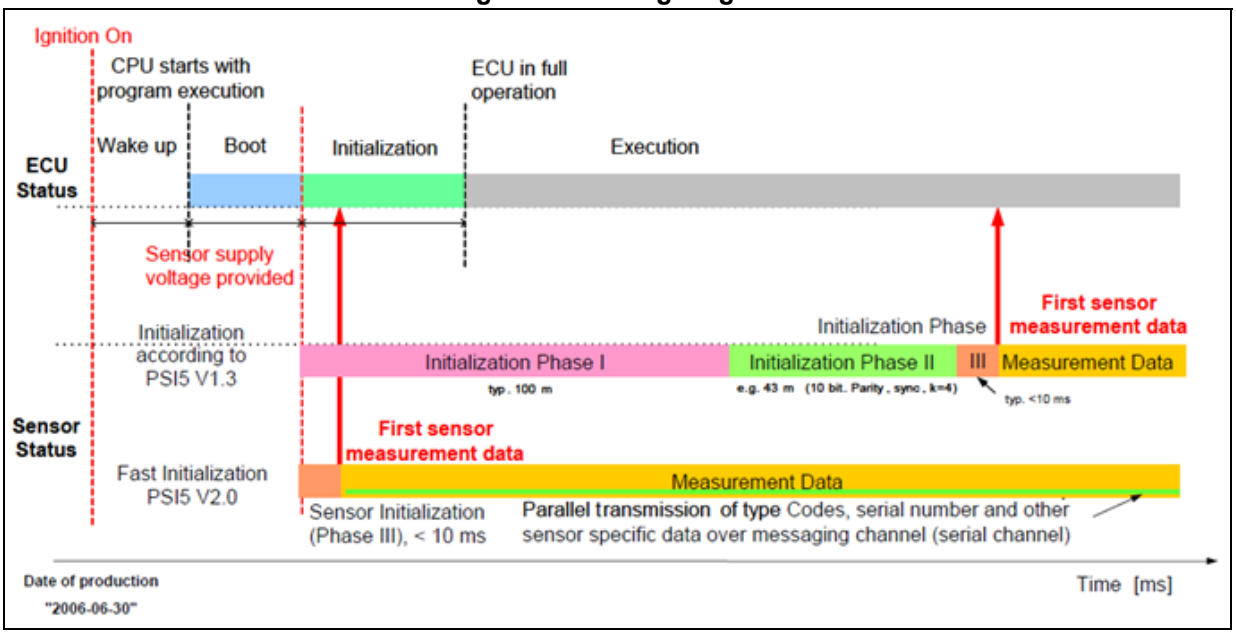
If the sensor uses a data range initialization procedure and the PSI5 payload is 20 bit with 3 frame control bits, 1 status bit, 16 bit data, the device can be configured so that the initialization data is stored in the transceiver IC and can be read via SPI.

In case of serial messaging method, the data must be extracted at application layer.

Basic features:

- Registers for initialization data (up to 8 init data buffer by 16 word available)
- Automatic detection of init data
- Reading via SPI

Figure 19. Timing diagram



After the activation of an interface, the transceiver IC can check for incoming sensor initialization data on that interface and store the data for further processing. This behavior is triggered by the configuration bit READ_INIT_DATA on that channel.

If the bit is set, an internal FSM checks for IDn and data blocks Dn in the incoming payload data on that interface and stores data in the init buffer id (init_buf_id) of the corresponding frame id at address n-1 in the following format:

RegAddr	15 (MSB) 10	9 6	5 0 (LSB)
n-1	additional data from blockid message (6 bits --- 0 bits)	data block (4 bits)	additional data from data message (6 bits --- 0 bits)

The frame control bits allow using up to 8 init data buffers when automatic storage of init data is activated and both interfaces are used (READ_INIT_DATA1 = READ_INIT_DATA2 = 1). In case only one interface is active, the IC can store up to 6 init data on that interface.

As specified in PSI5, data nibbles D2 and D3 contain the number of datablock expected for the all init procedure for each particular frame id; when all the init data are received for the engaged sensors (i.e. for the sensors which had sent at least one correct data blocks) on both the interfaces, the init_data_rdy is set and the µC can read all the init data by SPI. During reset, the incoming data buffer is cleared and the counters for each initialization data block are set to "00".

The interface can be configured both in asynchronous and synchronous mode (in the second case, the number of bits must be the same for all the timeslots). The accepted configuration for init data is based on 20 total bits, as follows:

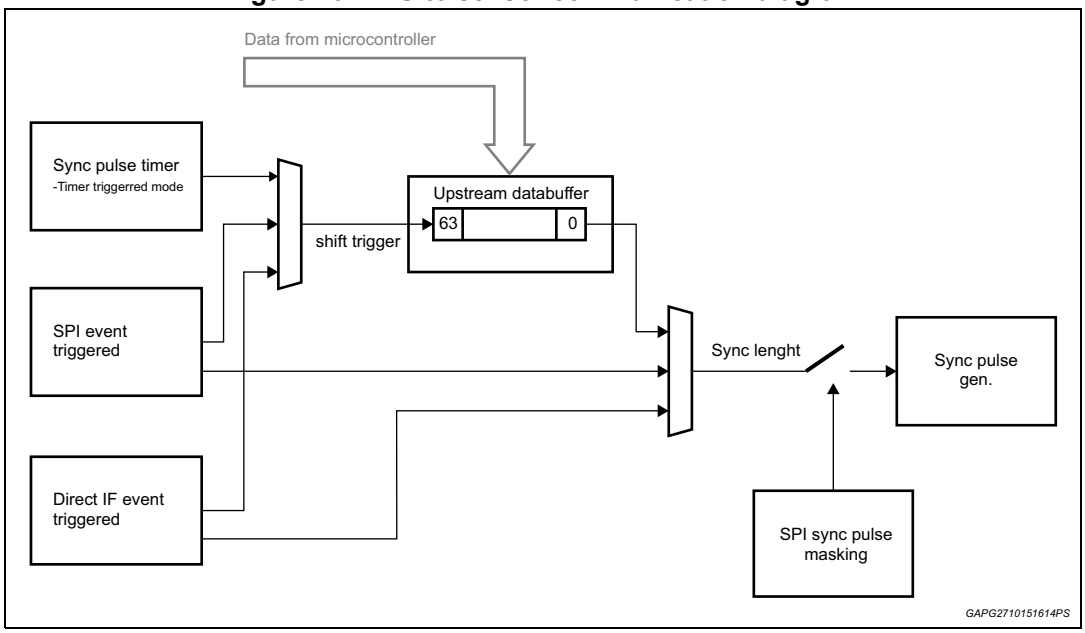
- 16 data bits
- 1 status bit
- 3 frame control

3.4 Upstream data buffer

Basic features:

- Adapts the signals delivered by Sync Pulse Timer block in order to make possible a bidirectional communication ECU to sensor
- Generates the trigger signal necessary for an event triggered sync pulse
- Provides the Sync Pulse Trigger signal to the Sync Pulse Generator

Figure 20. ECU to sensor communication diagram



The synchronization bits in the ECU to sensor communication must be programmed in the upstream data buffer by the microcontroller.

The upstream data buffer has 64 bits. The clock for the register is the output of the Sync Pulse Timer together with the trigger commands via SPI. After each request for a sync pulse, the register is shifted by one and the last bit is fed into the sync pulse trigger generator.

Depending on the data length, only a part of the upstream data buffer is used. After the writing of the relevant part of the buffer, the µC writes the upstream data confirm bit in the UDBCR register (bit UDBx_RDY). After this confirmation, the trigger source can start the communication. If these data are sent, the upstream data buffer is ready for new data. This is indicated by the SPI flag UDBx_BUSY='0'. If new data is written to the buffer while UDBx_BUSY is still '1', the write command is ignored and the error flag UDBx_FLT is set.

Besides if a new trigger is sent while the buffer is busy, again the command is ignored and the fault bit is set.

The buffer register can be reset by writing 0x00FF for channel 1 (respectively 0xFF00 for channel 2) to the SPI register DCR. After such a reset, the module will flag that it is ready for new data.

The behaviour of the sync pulse trigger generator then depends on the configuration of the transceiver IC:

- In PSI5 1.3 and 2.x mode (tooth gap method), it will mask out (i.e. ignore) the incoming sync pulse trigger if the bit is '0'. The resulting gap is defined to be a '0' in the ECU-to-sensor communication.
- In PSI5 2.x mode (pulse length method), it will generate a long sync pulse if the bit is '1' and a standard sync pulse otherwise.

The transceiver IC provides a transparent interface for ECU-to-sensor communication. This means that any data in the upstream data buffer will directly be transmitted onto the PSIx interface. The CRC calculation and data layer handling are done by the microcontroller.

3.5 Trigger pulse generator for synchronous pulses

This module generates the trigger signals for the transceiver interfaces. It has the following sub-modules:

- SPI-programmable sync pulse timer
- SPI command triggering
- 2 pins named SYNC1, SYNC2

The module contains the sync pulse trigger generators (one for each transceiver).

Basic features:

- Generates the sync pulse trigger at the configured time intervals
- Generates the sync pulse trigger upon the corresponding command via SPI or discrete SYNCx pins.

The trigger pulse generator generates the trigger signal which the sync pulse generator uses as its input.

The trigger pulse generator has five different configurations, which can be properly selected via SPI command:

- Triggering via SPI without upstream data buffer. The microcontroller sends the corresponding SPI command for a sync pulse. The sync pulse trigger generator then internally generates the appropriate sync pulses, based on the specific SPI command sent.
- Triggering via SPI with upstream data buffer. The microcontroller sends the corresponding SPI command for a sync pulse. Then the sync pulse trigger generator internally generates the appropriate sync pulses, depending on the value in the upstream data buffer.
- Triggering via SYNCx pins without upstream data buffer (tooth gap method only). When the SYNCx pin is triggered, the sync pulse trigger generator internally generates the appropriate sync pulses, based on the trigger received on the input pin.

- Triggering via SYNCx pins with upstream data buffer. When the SYNCx pin is triggered, the sync pulse trigger generator internally generates the appropriate sync pulses, depending on the value in the upstream data buffer.
- Triggering via trigger pulse timer: the transceiver IC automatically generates the sync pulses at fixed time intervals, depending on the value in the upstream data buffer.

The default configuration at startup is to use the triggering via SYNCx pins without upstream data buffer.

If the triggering with upstream data buffer is used and there aren't data to be sent to the sensor, a short pulse is sent.

The switch matrix is configurable by an SPI command. It determines whether the sync pulses are triggered via SPI by the trigger generator (transceiver IC in mode 1) or by the external trigger pins (transceiver IC in mode 2).

If the trigger pulse timer is used to generate the sync pulse trigger, the interval between two pulses on interface x is configured by the SPI register SYNC Pulse Timer (SPT). It's possible also to program the delay between interface 1 and interface 2 sync pulses through the SYNC_DELAY_PSI1_PSI2 bits in ADVSET2 register. In case the sync pulse trigger comes from SPI commands or SYNCx pins, the programmed pulse timer still has the functionality of a filtering time with respect to those triggering commands.

If full flexibility for the sync pulse interval is required, use direct triggering either via SPI or direct interface.

3.6 Synchronous pulse generator

The Synchronous Pulse Generator is designed to generate synchronous pulses conform to PSI5 rev. 1.3 (min V_{t2} = 3.5 V) as well PSI5 rev. 2.x (min V_{t2} = 2.5 V).

The sync pulse is granted according to PSI5 standard with the I_{base} current range up to 35 mA.

If the pulse trigger generation is configured with an external trigger and without the upstream data buffer, the external source must manage the encoding via SPI CHCNT register (for tooth gap and pulse width methods) or via PIN (tooth gap method only), for what concerns the duration of the sync pulse (i.e. ECU to sensor communication), otherwise the IC manages the encoding (tooth gap or pulse width methods, specified in register GCR1, bit PSIx_TGAP_PW).

An automatic hardware based slew rate control (SRC) ensures PSI5 compliant slew rates for the rising and falling edge of the sync pulse for an overall capacitive bus load of 15 to 107 nF. The Sync Pulse is shaped like raised cosine instead of trapezoidal to reduce EMC emission.

During the duration of the sync pulse, the corresponding PSI5 receiver is frozen to avoid erroneous data detection.

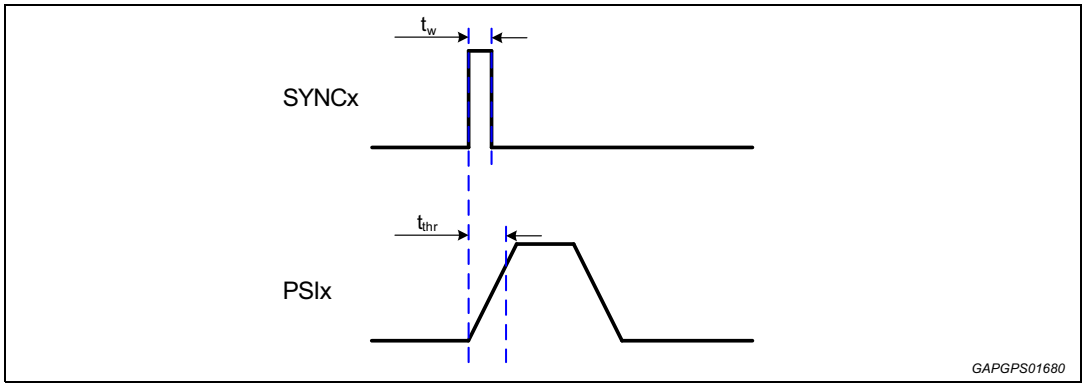
VDD, VAS and VB and other supply voltages are protected against reverse feeding from the sync pulse.

The pulse length at PSIx will be generated using the Sync Pulse Trigger Generator.

In case of trigger by pin without UDB, the Sync Pulse Generator starts the sync pulse with the positive edge of the trigger signal, after SYNCx pin filter. The duration of the sync pulse

is compliant to PSI5 standard (short pulse only) if the duration of the trigger is shorter than 5µs.[f]

Figure 21. Short (in case 1 µs < t_w < 5 µs) Sync Pulse trigger, compliant to PSI5 standard



3.7 Safety concepts

The IC design is optimized concerning functional safety requirements, thanks to the following implementations.

3.7.1 Voltage monitoring check

Internal and external voltage critical monitoring structures are automatically tested run-time while the device is operated. This feature covers the voltage monitors on:

- VINTA/D (under/over voltage monitoring)
- GNDD loss
- VAS (under/over voltage monitoring)
- VASSUP over voltage for charge pump disable
- VB over voltage for bootstrap disable
- PSIx under voltage
- PSIx over-temperature

The tests automatically running can highlight a condition of real fault on the application or a fault within the IC.

3.7.2 Sensor data consistency

Sensor data handling implements a particular safe concept intended to work with the SPI formats related to passive restraint application (i.e. 10-bit to 16-bit payloads): SID bits and G bit.

A 5-bit code (SID) can be used to identify sensor data. The external MCU can program a SID via SPI to be associated to each time slot of a physical interface. When the MCU performs a sensor data read operation via SPI, the L9663 returns the SID code to the MCU, along with the requested sensor data, for the MCU to check.

f. For sync pulse triggering via pin see errata n.1822, *Section 7: Errata*.

If the SID is used, a diagnostic bit (G bit) is also present in the SPI frame sent to the MCU. This bit signals the occurrence of specific faults, namely an under voltage on the VAS supply, or a parity check fault on a critical register[g] .

The data register containing SID bits and PSI5 sensor data is written with one single access: data from the Manchester decoder is identified with reference to the time slot counter and written in the same access when the information of the transmitting sensor is written.

Each failure case, CRC checksum and SID identification mismatch, can be forced via test SPI commands through STS and STSR register after a special "self test" mode is entered through an SPI command (see *DCR (PROG)* register for details).

3.7.3 Buffer empty check

As described in *Section 3.3.2*, the IC always checks that, after a valid data read, the code 1F0 is written in the buffer.

This feature is the "Buffer Empty check", implemented for safety: if the check fails a Buffer Empty Fault is asserted and latched (BEx bits in SR2 register) and it is cleared after reading through SPI.

In order to allow the µC to test this feature at startup or during normal operation, a Test of buffer empty check is provided in the STSR register (bit0).

If this bit is set, after a read operation the old data is left in the buffer; in this way a buffer empty fault is set and the µC can test the safety feature.

3.7.4 DOUTx path check

DOUTx paths can be checked against fault conditions through dedicated test SPI register (STS register).

In order to test the input structures of the connected microcontroller, the L9663 features a DOUTx test mode that allows test patterns to be applied on the two outputs DOUT1-DOUT2. The test mode can be entered via SPI and the test patterns can also be controlled via SPI commands. Test patterns can be composed only of static high or low signals, which can be selected via SPI. For failsafe reasons only one channel at a time can be switched into test mode.

Table 9. Doutx test mode bit value

Bit	Name	Description
10	DOUTTP	Test Pattern: 1: Static output set to high on DOUTx, for which test mode is enabled 0: Static output set to low on DOUTx, for which test mode is enabled
9:5	DOUTSEL	Dout Test Mode Selection Bits: 10101: DOUT Test Mode Enabled for DOUT1 Output 10110: DOUT Test Mode Enabled for DOUT2 Output All other bit patterns: DOUT Test Mode Disabled

g. The fault "clock error" is not included in the G bit because in this case the device enters immediately reset state, if the bit REACTTIME of ADVSET2 register is '0' (default).

3.7.5 Cross coupling test

An automatic hardware based cross-coupling test (XCT) for the PSI interfaces is implemented and can be triggered by SPI command (Self-Test Setting (STS) Register). Aim of the test is to monitor the status of PSIx interfaces both in master and slave mode; slave mode simply checks that when PSIx are switched off the under voltage flag is set, while master mode implements a Finite State Machine able to schedule several steps (see description below).

- XCT test both in master and slave mode is triggered only if both PSIx interfaces are off. In case one of the PSI-IFs is already switched on, starting of a XCT will not be possible and in this case the XCT results register will be reset.
- Once XCT test is running, commands to switch the channel on or disable VAS regulator are ignored by the device.
- Once XCT test is running, it cannot be interrupted or stopped by any SPI instruction except by stop bit within "Abort cross-coupling test" command: in this case, only in master mode, an "abort" flag will be set (XCT_ABT bit).
- While XCT test is running a "busy" flag will be asserted (XCT_RUN bit).
- Once XCT test is finished a "done" flag will be asserted (XCT_COMPL).
- Flag "busy" is only asserted while XCT test both master and slave mode is ongoing while "done", "abort", XCTx_R, STB, XCT_STG results are cleared when read via SPI or when a new XCT start request occurs (both valid or invalid). Please note that XCT_STG bits are mapped in bits 0 and bit 8 of SR2 register. These bits normally are real time bits but, as soon as a Master XCT test is completed (and the XCT_COMPL flag is asserted) the bits 0 and 8 contain the results of the XCT test and keep this value until results are cleared by reading or by new test start)

Slave Mode (PSIx switched off)

- A pulldown current (I_{XCT}) is turned ON for both channels for a 512 µs time in order to be sure to discharge PSI5 lines
- Once PSI5 line is supposed to be discharged (512 µs time elapsed), pull-down current is switched off on each channel
- Check psi1_uv=psi2_uv='1':
  - Xcoupling_slave PSI1 ok if psi1_uv='1' (test failed otherwise)
  - Xcoupling_slave PSI2 ok if psi2_uv='1' (test failed otherwise)

Master Mode

- Short to battery test
  - Enable PSI1 channel
  - Wait for a 512 µs time in order to reach steady state condition (short to ground and overcurrent masked in this phase)
  - Check psi1_stb='0': in case psi1_stb='1' the fault flag is asserted and the channel 1 is not involved in the following tests
  - Switch off PSI1 channel and switch on I_{XCT} pull down current for a 128 µs time on PSI1 interface
  - Once PSI5 line is supposed to be discharged (128 µs time elapsed), pull-down current is switched OFF
  - Enable PSI2 channel
  - Repeat the above flow for PSI2 channel
- X coupling test phase 1 (only if channel 1 was not excluded in previous short to battery test)
  - Enable PSI1 channel, PSI2 channel switched off
  - Wait for 512 µs time in order to reach steady state condition and allow PSI under voltage filter time to elapse (short to ground and overcurrent masked in this phase)
  - Check psi1_uv='0' and psi2_uv='1': in case of psi1_uv='1' a short to GND on PSI1 is detected while in case psi2_uv='0' a cross coupling is detected and XCT2_R bit is set [(h)]
  - Switch off PSI1 channel and switch on I_{XCT} pull down current for a 128 µs time
  - Once PSI5 line is supposed to be discharged (128 µs time elapsed), pull-down current is switched off.
- X coupling test phase 2 (only if channel 2 was not excluded in previous short to battery test)
  - Enable PSI2 channel, PSI1 channel switched off
  - Wait for 512us time in order to reach steady state condition and allow PSI under voltage filter time to expire (short to ground and overcurrent masked in this phase)
  - Check psi2_uv='0' and psi1_uv='1': in case of psi2_uv='1' a short to GND on PSI2 is detected while in case psi1_uv='0' a cross coupling is detected and XCT1_R bit is set
  - Switch off PSI2 channel and switch on I_{XCT} pull down current for a 128 µs time
  - Once PSI5 line is supposed to be discharged (128 µs time elapsed), pull-down current is switched off

Short to battery test in master mode is executed in two phases for the two channels to avoid enabling simultaneously PSIx interfaces and avoid overloading ECU supply line.

Cross coupling test in master mode stops automatically when the time required by this test is elapsed. Cross coupling test in slave mode can be stopped with "Abort cross coupling test" command; only in this case, the flag "cross-coupling test aborted" is not set, because this is not a faulty condition.

h. Cross coupling test flags swapped in master mode, see errata n.1830, *Section 7: Errata*.

4 Diagnosis

The PSIx output voltage is monitored to detect and protect against failures:

- Under voltage on PSI5x outputs
- Short to ground (STG)
- Leakage to ground (LTG)
- Open load (OL)
- Short to battery (STB)
- Short between channels (through cross coupling test) and to protect the transceiver IC in case of negative voltages or excessive voltage on the PSIx outputs.

This module consists of the following sub modules:

- PSIx output voltage clamping circuit
- PSIx short circuit detection and current limitation
- PSIx reverse voltage monitoring
- PSIx under voltage monitoring
- VAS under voltage monitoring
- Sync pulse voltage monitoring

4.1 PSIx output voltage clamping circuit

The clamping circuit allows control of the maximum voltage level on the PSIx output, despite a possible over voltage fault on the VAS line.

The Transceivers clamp the PSIx voltage to less than 11 V in data transmission or less than 16.5 V in sync pulse with a 50 mA typical sink current.

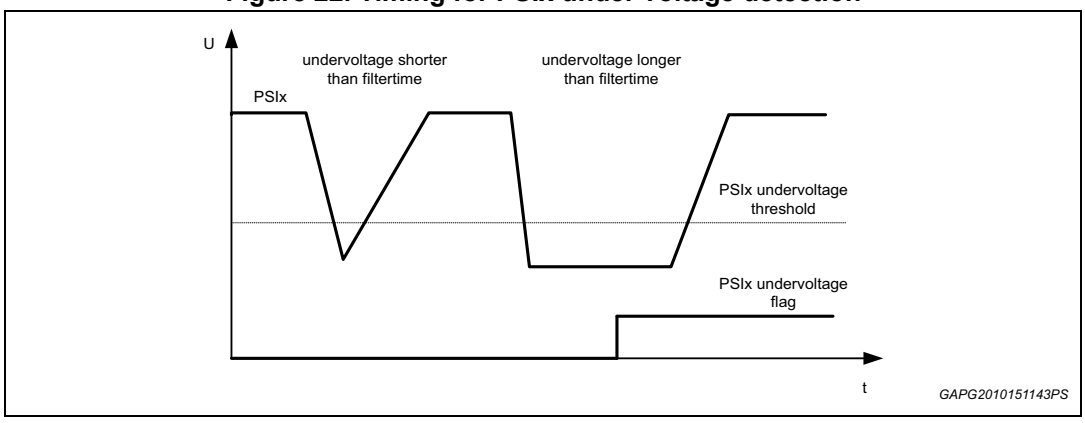
4.2 PSIx output under voltage monitoring

The under voltage monitoring detects a low voltage level of the sensor supply line PSIx.

Basic features:

- Under voltage monitoring with filter time

Figure 22. Timing for PSIx under voltage detection



The PSIx lines (sensor supply lines) are monitored for under voltage if the PSIx line is switched on.

The current status of the under voltage comparators is shown in the SPI register SR2.

The logical state of the voltage comparator is debounced internally by a filter.

While any reset is active (POR, RESETN or SW_RESET), the PSIx lines are switched off. After reset is released, the failure bits are reset and the voltage supply at PSIx lines kept off.

4.3 PSIx short circuit detection

The short circuit monitoring detects a short of the sensor supply line PSIx to GND, limits the current to ISTG (max 130mA) for tIfilt and then switches off the affected PSIx line.

Basic features:

- Short to ground circuit monitoring with filter time
- Automatic deactivation of the PSIx line in case of a short to GND
- Readable via SPI

The PSIx lines (sensor supply lines) are monitored to detect a short circuit to GND if the PSIx line is switched on. In this case, the corresponding fault SPI bit STGx in SR2 register is set to '1' and the PSIx line is switched off (the status of the interfaces is reported in SR3 register). The fault bit is latched and cleared only when a SPI switch off command for confirmation is sent on the line that was under short to ground condition. The current status (on/off) of the PSI interfaces can be read via SPI.

The line can be switched on again by switching off and on via SPI.

The logical state of the short to ground monitoring is debounced internally by a filter. The monitoring is deactivated during a configurable blanking time after startup of the interface.

This time is selectable through BLANKING_SEL parameter in SPI register ADVSET1 (default value is 128 µs)

During reset is active, the PSIx lines are switched off. After reset is released, the failure bits are reset and the voltage supply at PSIx lines can be switched on by SPI command. It is possible to reset the transceiver IC by sending an SPI command (SW Reset).

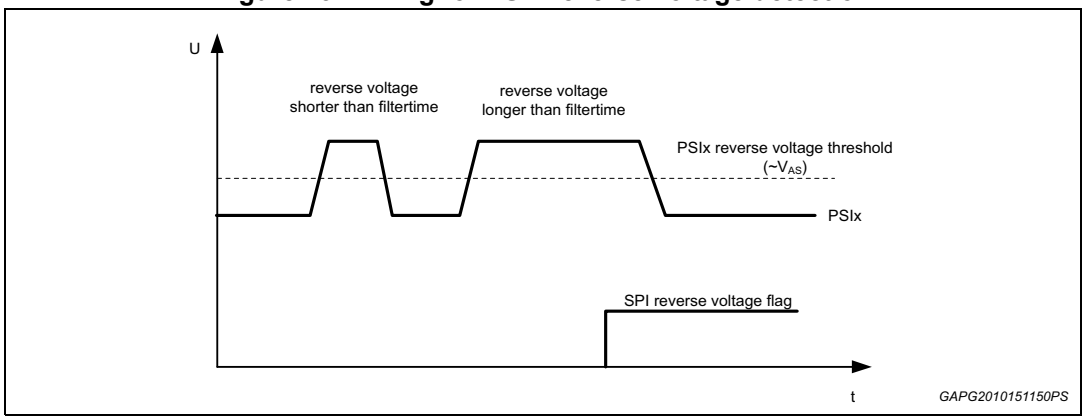
4.4 PSIx reverse voltage monitoring

The PSIx sensor supply lines are monitored to detect a short circuit to battery if the PSIx line is switched on.

Basic features:

- Reverse voltage monitoring with respect to VAS (or VBH during sync pulse) voltage with filter time
- Readable via SPI

Figure 23. Timing for PSIx reverse voltage detection



In case of a detected failure, a failure bit STBx in SR2 register is set to '1' (latched and cleared upon reading via SPI).

After reset, the failure bit is reset to '0'

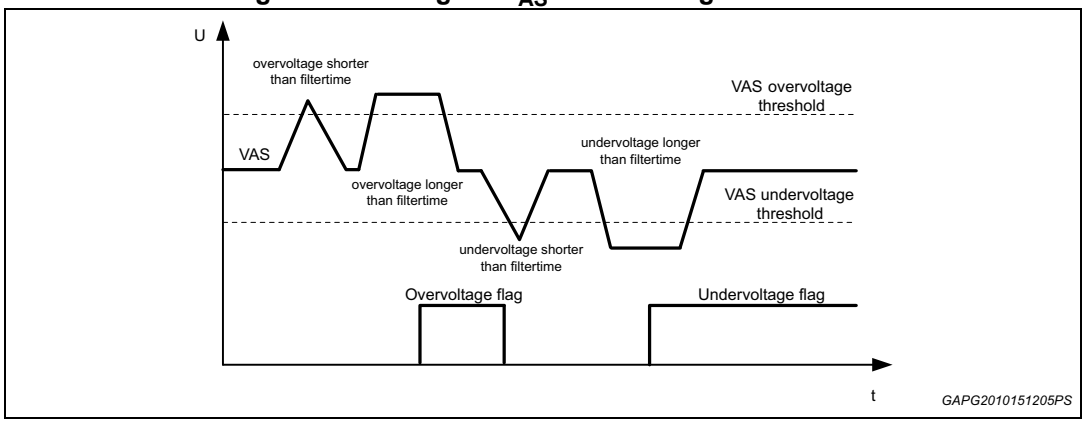
4.5 V_{AS} under/over voltage monitoring

The VAS voltage is monitored for under voltage and over voltage.

Basic features:

- Under voltage comparator with filter time
- Over voltage comparator with filter time
- Readable via SPI

Figure 24. Timing for V_{AS} under voltage detection



If the V_{AS} voltage is lower than the under voltage threshold for longer than the filter time, the SPI bit VAS_UV in SR1 reg is set to '1' and it is latched and cleared upon read.

If the V_{AS} voltage is higher than the over voltage threshold for longer than the filter time, the SPI bit VAS_OV in SR1 reg is set to '1' (NOT latched). In addition to that, in case of further lower under voltage condition (V_{VASU_off}), VAS is switched off to protect the external n-channel FET component from high current flow when external pin is shorted to ground. The fault bit VAS_UVL (SR1) is latched and gets cleared only when a SPI switch off command for confirmation is sent. The current status (on/off) can be read via SPI (SR3).

The regulator can be switched on again by switching off and on via SPI.

When POR is de-asserted, under voltage is masked for the time needed by soft start circuit to switch on the regulator (1 ms).

During reset, the under/over voltage bits are set to 0.

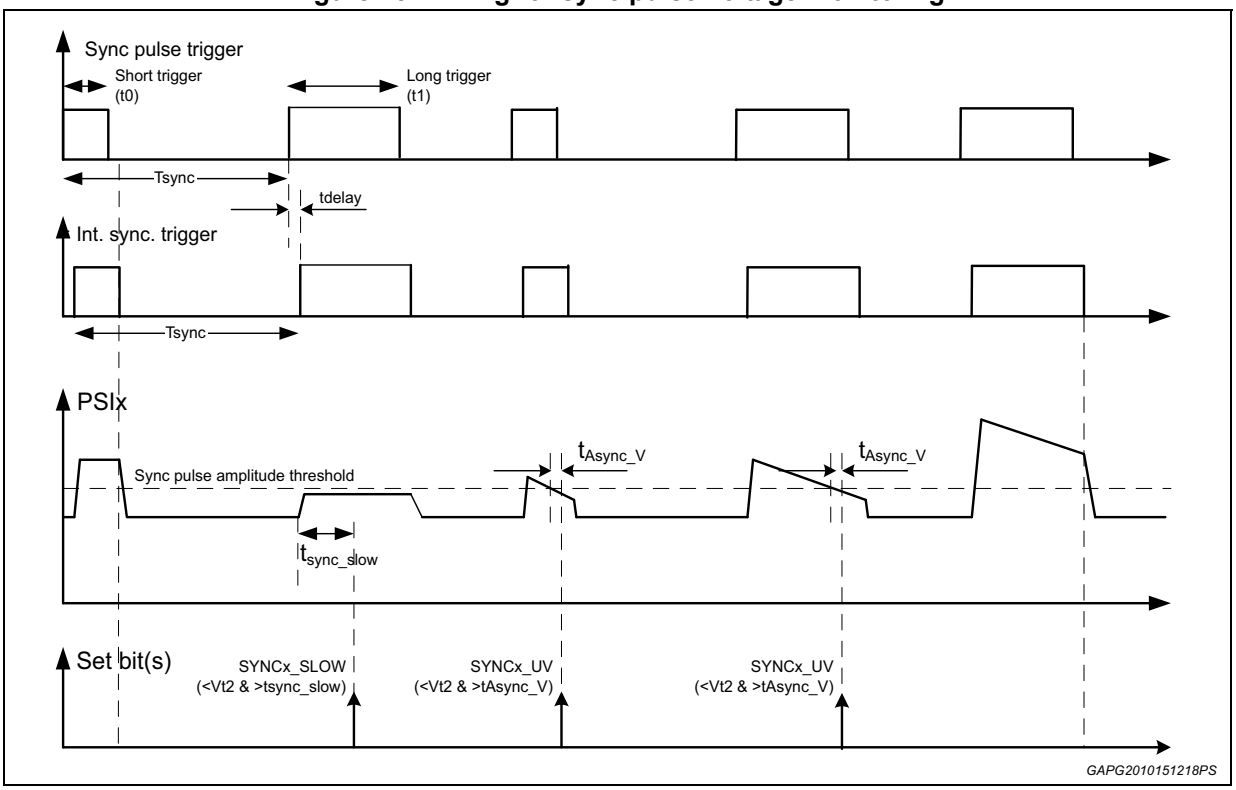
4.6 Monitoring of Synchronous Pulse amplitude

To detect possible communication problems due to sync pulses which do not conform to the standard, this module monitors the parameters of the sync pulse and registers any deviation from the standard.

Basic features:

- Comparator
- Evaluation block
- Flag readable via SPI

Figure 25. Timing for sync pulse voltage monitoring



The sync pulses[i] are monitored for under voltage, duration and rising edge transient speed. The circuit evaluates the output voltage versus internal sync trigger signal and sets the corresponding bit(s) in Status Register 1 (SR1):

- Bit SYNCx_SLOW if a delayed sync pulse or pulse with Vt2< 2.5V /3.5V was generated (slow Vsync rising time)
- Bit SYNCx_UV if the sync pulse amplitude goes below 2.5V/3.5V for a time longer than the specified filtering time (spec parameter tAsync_V).

STB is detected by the over voltage monitoring (see *Section 4.4*).

i. For sync pulse triggering via pin see errata n.1822, *Section 7: Errata*

5 Communication interface

As interface to the microcontroller, either the SPI interface or the direct interface shall be used.

The following pins are used for SPI communication:

- MOSI
- MISO
- SCLK
- CS

5.1 Device registers

The following registers are available for writing configuration data and reading information data. Registers can be of 4 different types:

- WO: writeable only
- RO: readable only
- R/W: both readable and writeable
- RC : readable and cleared upon reading

Device configuration registers are marked with "PROG". These registers can only be written before the microcontroller sends an EOP (End Of Programming) command through the Direct Command Register (DCR).

The registers which have a special safety importance contain a parity bit (PAR) which must be written by the µC with an odd parity. A periodic check (every 150 us) is done and if a parity error is found on one of these registers the GBIT is set.

GCR1 (PROG) General Configuration Register 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PAR	DIS_ADD_MUX	PSI2_EXT_UDB	PSI2_TRIG_SEL		PSI2_TGAP_PW	PSI1_EXT_UDB	PSI1_TRIG_SEL		PSI1_TGAP_PW	RESERVED	CLKIN_CFG		SIDG_EN	CRC_CK	VAS_SEL
Default value:															
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W															

Address: 000001

Type: R/W

Description:

[15] PAR: Register parity
Odd parity bit for register bits [15:0]

[14] DIS_ADD_MUX: SPI address multiplexing disable
0: address multiplexing enabled
1: address multiplexing disabled

[13] PSI2_EXT_UDB: SYNC pulse generation for PSI5 interface 2
0: the trigger on SYNC2 pin or the SPI command determine the SYNC pulse length
1: the contents of UDB2 determine the SYNC pulse length (always true if timer enabled bit[12:11]=10)

[12:11] PSI2_TRIG_SEL: SYNC pulse trigger source for PSI5 interface 2
00: SYNC pulse generated by SYNC2 pin
11: SYNC pulse generated by SYNC2 pin
01: SYNC pulse generated by SPI command
10: automatic SYNC pulse generation

[10] PSI2_TGAP_PW: SYNC pulse method for PSI5 interface 2
This bit takes effect only in case bit [13] = 1
0: tooth gap method
1: pulse width method

[9] PSI1_EXT_UDB: SYNC pulse generation for PSI5 interface 1
0: the trigger on SYNC1 pin or the SPI command determine the SYNC pulse length
1: the contents of UDB1 determine the SYNC pulse length(always true if timer enabled bit[8:7]=11)

[8:7] PSI1_TRIG_SEL: SYNC pulse trigger source for PSI5 interface 1
00: SYNC pulse generated by SYNC1 pin
11: SYNC pulse generated by SYNC1 pin
01: SYNC pulse generated by SPI command
10: automatic SYNC pulse generation

[6] PSI1_TGAP_PW: SYNC pulse method for PSI5 interface 1
This bit takes effect only in case bit [9]=1
0: tooth gap method
1: pulse width method

[5] RESERVED

[4:3] CLKIN_CFG: Clock input configuration
00: no external clock used
11: no external clock used
01: 1MHz external clock
10: 4MHz external clock

[2] SIDG_EN: SID and Gbit
This bit takes effect only in case of payload of 10 or 16 bits
0: SID bits and G bit not used
1: SID bits and G bit used

[1] CRC_CK: CRC / parity check on sensor data
0: the CRC bits on SPI MISO are those from the sensor
1: the CRC bits on SPI MISO are calculated by the transceiver

[0] VAS_SEL: VAS voltage regulator output
0: 5.3 V
1: 7.6 V

CHCNT Channel Control

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	VAS_EN	SPI_SYNC_TRIG2		RESERVED	MASK_SYNC2	PSI2_EN	SPI_SYNC_TRIG1		RESERVED	MASK_SYNC1	PSI1_EN
Default value:															
0	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0
R/W															

Address: 000010

Type: R/W

Description:

[15:11] RESERVED

[10] PVAS_EN: Enable / disable VAS regulator
0: disabled
1: enabled

[9:8] SPI_SYNC_TRIG2: SPI SYNC pulse trigger for PSI5 interface 2
00, 11: no SYNC pulse generated
01: short SYNC pulse
10: long SYNC pulse
Notes:
if interface 2 is off, these bits are ignored and no sync pulse is generated bits are evaluated only once, after writing;
If upstream data buffer is used, both codes "01" and "10" are equivalent. Information on sync pulse length is provided by the UDB

[7] RESERVED

[6] MASK_SYNC2: SYNC pulse enable / disable for PSI5 interface 2
0: SYNC pulse disabled
1: SYNC pulse enabled (if in synchronous mode, otherwise ignored)

[5] PSI2_EN: Enable PSI5 interface 2
0: interface off
1: interface on

[4:3] SPI_SYNC_TRIG1: SPI SYNC pulse trigger for PSI5 interface 100: no external clock used
00: no SYNC pulse generated
11: no SYNC pulse generated
01: short SYNC pulse
10: long SYNC pulse
Notes:
if interface 1 is off, these bits are ignored and no sync pulse is generated.
if interface 1 is on, these bits are evaluated only once, after writing;
If upstream data buffer is used, both codes "01" and "10" are equivalent. Information on sync pulse length is provided by the UDB

[2] RESERVED

[1] MASK_SYNC1: SYNC pulse enable / disable for PSI5 interface 1
0: SYNC pulse disabled
1: SYNC pulse enabled (if in synchronous mode, otherwise ignored)

[0] PSI1_EN: Enable PSI5 interface 1
0: interface off
1: interface on

NOPR No Operation Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Default value:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W															

Address: 000011

Type: R/W

Description:

Write into this register to perform no operation and read the Global Status Bits.

SR1 Status Register 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XCT_COMPL	XCT_ABT	XCT_RUN	SPI_FLT	OTP_CRC_ERR	VAS_UV	VAS_OV	VAS_UVL	SYNC2_TOUT	UDB2_FLT	SYNC2_SLOW	SYNC2_UV	SYNC1_TOUT	UDB1_FLT	SYNC1_SLOW	SYNC1_UV
Default value:															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
RC															

Address: 000100

Type: RC (latched and cleared on read, except if otherwise specified)

Description:

[15] XCT_COMPL: Cross-coupling test completed

[14] XCT_ABT: Cross-coupling test aborted

[13] XCT_RUN: Cross-coupling test running [realtime]

[12] SPI_FLT: SPI fault (CRC error, clock cycles, wrong H/L read operation on sensor data, register address not valid)

[11] OTP_CRC_ERR: Error from OTP trimming bits [realtime]

[10] VAS_UV: Under voltage detected on VAS. Latched bit

[9] VAS_OV: Over voltage detected on VAS [realtime]

[8] VAS_UVL: Under voltage detected on VAS. When below VVASU_off, VAS is switched off. Latched bit. Cleared upon VAS_EN='0' confirmation from MCU

[7] SYNC2_TOUT: Exceeded tw timeout of 100 µs on SYNC2 pin during sync pulse (sync pulse driven by pin source)

[6] UDB2_FLT: Write operation on Upstream Data Buffer 2 occurred while buffer is busy (i.e. UDB2_BUSY=1)

[5] SYNC2_SLOW: No SYNC pulse generated, delayed SYNC pulse or SYNC voltage < 2.5V/3.5V on PSI5 interface 2

[4] SYNC2_UV: SYNC pulse < 2.5V/3.5V for a time longer than specified on PSI5 interface 2

[3] SYNC1_TOUT: Exceeded tw timeout of 100 µs on SYNC1 pin during sync pulse (sync pulse driven by pin source)

[2] UDB1_FLT: Write operation on Upstream Data Buffer 1 occurred while buffer is not empty (i.e. UDB1_BUSY=1)

[1] SYNC1_SLOW: No SYNC pulse generated, delayed SYNC pulse or SYNC voltage < 2.5V/3.5V on PSI5 interface 1

[0] SYNC1_UV: SYNC pulse < 2.5V/3.5V for a time longer than specified on PSI5 interface 1

SR2 Status Register 2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XCT2_R	BE2	OL2	STB2	LKG2	STG2	OT2	UV2/XCT_STG2	XCT1_R	BE1	OL1	STB1	LKG1	STG1	OT1	UV1/XCT_STG1
Default value:															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
RC															

Address: 000101

Type: RC (latched and cleared on read, except if otherwise specified)

Description:

[15] XCT2_R(1): Result of cross-coupling test on PSI5 interface 2

[14] BE2: Buffer empty fault on PSI5 interface 2

[13] OL2: Open load on PSI5 interface 2

[12] STB2Short to VBAT on PSI5 interface 2
Masked towards FSR2 status bit during cross coupling test

[11] LKG2: Leakage to GND on PSI5 interface 2

[10] STG2: Short to GND on PSI5 interface 2
Cleared upon PSI2_EN='0' confirmation from MCU

[9] OT2: Over temperature on PSI5 interface 2
Cleared upon PSI2_EN='0' confirmation from MCU

[8] UV2/XCT_STG2: Under voltage on PSI5 interface 2
Masked towards FSR2 status bit during cross coupling test
[real time bit except when XCT test is used]

[7] XCT1_R: Result of cross-coupling test on PSI5 interface 1

[6] BE1: Buffer empty fault on PSI5 interface 1

[5] OL1: Open load on PSI5 interface 1

[4] STB1: Short to VBAT on PSI5 interface 1
Masked towards FSR2 status bit during cross coupling test

[3] LKG1: Leakage to GND on PSI5 interface 1

[2] STG1: Short to GND on PSI5 interface 1
Cleared upon PSI1_EN='0' confirmation from MCU

[1] OT1: Over temperature on PSI5 interface 2
Cleared upon PSI1_EN='0' confirmation from MCU

[0] UV1/XCT_STG1: Under voltage on PSI5 interface 1
Masked towards FSR2 status bit during cross coupling test
[real time bit except when XCT test is used]

1. Cross coupling test flags swapped in master mode, see errata n.1830, *Section 7: Errata*.

SR3 Status Register 3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS_EN	INITDATA_RDY	VAS_ON	FIFO_LCK	RESERVED	RESERVED	SYNC2_STAT	UDB2_BUSY	PSI2_ON	RESERVED	SYNC1_STAT	UDB1_BUSY	PSI1_ON	RESERVED	CLK_FLT	RST
Default value:															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R															

Address: 000110

Type: R (except if otherwise specified)

Description:

[15] STS_EN: Enable self test status
0: disabled: STS/STSR register not WR (depending on PROG state STS will not be enabled)
1: enabled: STS/STSR register WR

[14] INITDATA_RDY: Initialization data ready
0: not ready
1: ready

[13] VAS_ON: VAS regulator status
0: disabled
1: enabled

[12] FIFO_LCK: FIFO locked status
Note:
This bit is set to '1' when first data is read after FIFO has been filled up
Cleared to '0' as soon as FIFO gets emptied

[11:10] RESERVED

[9] SYNC2_STAT: SYNC2 pin status
0: SYNC2 pin is low
1: SYNC2 pin is high for more than pin filter time.
It can be used to detect short condition on this pin.
Cleared upon read.

[8] UDB2_BUSY: Upstream data buffer 2 is busy with data to be sent
Not cleared upon read
0: not busy
1: busy

[7] PSI2_ON: PSI 2 interface status
0: disabled
1: enabled

[6] RESERVED

[5] SYNC1_STAT: SYNC1 pin status
0: SYNC1 pin is low,
1: SYNC1 pin is high for more than pin filter time.
It can be used to detect short condition on this pin.
Cleared upon read.

[4] UDB1_BUSY: Upstream data buffer 1 is busy with data to be sent
0: not busy
1: busy

[3] PSI1_ON: PSI 1 interface status
0: disabled
1: enabled

[2] RESERVED

[1] CLK_FLT:
0: no CLK fault
1: reset by internal CLK fault
Cleared upon read.

[0] RST: Reset occurred via internal POR, SW reset (via SPI) or HW reset (via RESET pin)
0: no reset
1: reset occurred
Cleared upon read.

UDBCR Upstream Data Buffer Configuration Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	UDB2_RDY	UDB2_NOB						RESERVED	UDB1_RDY	UDB1_NOB					
Default value:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W															

Address: 000111

Type: R/W

Description:

[15] RESERVED

[14] UDB2_RDY: Upstream data confirmation.
0: NOP.
1: UDB2 data are ready for sending, and are sent based on the trigger source.
Note:
This bit is used only once, after writing

[13:8] UDB2_NOB: Number of bits in UDB2 to be sent on the PSI5 interface 2.
000000: 1 bit
000001: 2 bits
…
111111: 64 bits

[7] RESERVED

[6] UDB1_RDY: Upstream data confirmation.
0: NOP.
1: UDB1 data are ready for sending and are sent based on the trigger source.
Note:
This bit is used only once, after writing.

[5:0] UDB1_NOB: Number of bits in UDB1 to be sent on the PSI5 interface 1
000000: 1 bit
000001: 2 bits
…
111111: 64 bits

UDB1_X (X = 1…4) Upstream Data Buffer 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UDB1_X															
Default value:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W															

Address: 001000 (UDB1_1) .. 001011 (UDB1_4)

Type: R/W

Description:

[15:0] UDB1_X (X = 1…4)

The Upstream Data Buffer 1 (4x 16 bits = 64 bits) contains the bits to be sent to sensors as SYNC pulses on the PSI5 interface 1. The Upstream Data Buffer 1 is formed by the concatenation of UDB1_1, UDB1_2, UDB1_3 and UDB1_4:UDB1_1 (bits [63:48]), UDB1_2 (bits [47:32]), UDB1_3 (bits [31:16]), UDB1_4 (bits [15:0]). Data are sent on the interface with LSB first.

If the upstream data buffer is empty (UDBx_BUSY flag is set to '0'), when the trigger source (SPI, SYNCx pin or timer) is active, a short sync pulse is generated on the interface by default (independently from tooth gap or pulse width method selection).

UDB2_X (X = 1…4) Upstream Data Buffer 2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UDB2_X															
Default value:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W															

Address: 001100 (UDB2_1) .. 001111 (UDB2_4)

Type: R/W

Description:

[15:0] UDB2_X (X = 1…4)

The Upstream Data Buffer 2 (4x 16 bits = 64 bits) contains the bits to be sent to sensors as SYNC pulses on the PSI5 interface 2. The Upstream Data Buffer 2 is formed by the concatenation of UDB2_1, UDB2_2, UDB2_3 and UDB2_4: UDB2_1 (bits [63:48]), UDB2_2 (bits [47:32]), UDB2_3 (bits [31:16]), UDB2_4 (bits [15:0]). Data are sent on the interface with LSB first.

If the upstream data buffer is empty (UDBx_BUSY flag is set to '0'), when the trigger source (SPI, SYNCx pin or timer) is active, a short sync pulse is generated on the interface by default (independently from tooth gap or pulse width method selection).

SPT (PROG) SYNC Pulse Timer

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPT1								SPT2							
Default value:															
0	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1
R/W															

Address: 010000

Type: R/W

Description:

[15:8] SPT1 Sync pulse timer 1:
Period for automatic SYNC pulse generation on PSI5 interface 2 (if automatic SYNC pulse generation is selected).
Minimum allowed period (if SYNC pulse trigger is generated by PIN or SPI).
00000000: 200 µs
…
00001001: 488 µs (default)
…
11111111: 8360 µs

Steps of 32 µs.

[7:0] SPT2 Sync pulse timer 2:
Period for automatic SYNC pulse generation on PSI5 interface 1 (if automatic SYNC pulse generation is selected)
Minimum allowed period (if SYNC pulse trigger is generated by PIN or SPI).
00000000: 200 µs
…
00001001: 488 µs (default)
…
11111111: 8360 µs

Steps of 32 µs.

CH1_CR1 (PROG) Channel 1 Configuration Register 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PAR	RESERVED	VT2_SYNC1_SEL	DOUT1_SEL	TSM1_SEL		QC1_SEL		READ_INIT_DATA1	NOTS1			RESERVED	BR1		SYNC1_EN
Default value:															
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
R/W															

Address: 010001

Type: R/W

Description:

[15] PAR: Register parity
Odd parity bit for register bits [15:0]

[14] RESERVED

[13] VT2_SYNC1_SEL: Sync pulse voltage selector for channel 1
0: 2.5 V (PSI5 ver. 2.x common and low power mode)
1: 3.5 V (PSI5 ver. 2.x common mode only, and PSI5 ver. 1.3)

[12] DOUT1_SE: Configuration of DOUT1 pin
0: DOUT1 transmits PSI5 data
1: DOUT1 is an interrupt output

[11:10] TSM1_SEL: Time slot monitoring on PSI5 channel 1
00: monitoring disabled
11: monitoring disabled
01: standard monitoring enabled
10: simple monitoring enabled

[9:8] QC1_SEL: Quiescent current limit on PSI5 interface 1
00: standard current (19 mA)
01: extended current (35 mA)
11: extended current (35 mA)
10: extended current (45 mA)

[7] READ_INIT_DATA1: Read sensor initialization data on ch 1
0: init data not stored
1:init data stored in dedicated buffer

[6:4] NOTS1: Number of time slots on PSI5 interface 1
001: 1 time slot
…
110: 6 time slots
others: default (3 slots)

[3] RESERVED

[2:1] BR1: Baud rate of PSI5 interface 1
00: 125 kb/s
11: 125 kb/s
01: 189 kb/s
10: 83.3 kb/s

[0] SYNC1_EN: Asynchronous or synchronous mode on PSI5 interface 1
0: asynchronous mode (SYNC pulse disabled, FIFO data buffer)
1: synchronous mode

CH1_CR2 (PROG) Channel 1 Configuration Register 2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	CH1_BT1_DIS1	CH1_CRCP2	CH1_NOB2					CH1_CRCP1	CH1_NOB1				
Default value:															
0	0	0	0	0	1	0	1	0	0	0	1	0	1	0	0
R/W															

Address: 010010

Type: R/W

Description:

[15:13] RESERVED

[12] CH1_BT1_DIS1: Bootstrap ch1 disable
0: enabled
1: disabled

[11] CH1_CRCP2: Parity or CRC in time slot 2
0: CRC
1: parity

[10:6] CH1_NOB2: Number of data bits in time slot 2
01000: 8 data bits
…
11100: 28 data bits
others: default (20 bit)

[5] CH1_CRCP1: Parity or CRC in time slot 1
0: CRC
1: parity

[4:0] CH1_NOB1: Number of data bits in time slot 1
01000: 8 data bits
…
11100: 28 data bits
others: default (20 bit)

Settings programmed for time slot 1 are automatically applied to the other time slots in case at least one of the following conditions in CH1_CR1 register is verified:
– READ_INIT_DATA1='1'
– TSM1_SEL="10" (simple configuration)
– SYNC1_EN='0' (asynchronous mode)
Although the settings of time slot 1 are automatically applied by the logic to other time slots, these are not written in the corresponding configuration registers. In order to avoid not up-to-date readout of the time slot configuration by SPI and to prevent from wrong SPI errors in case of mismatches in the number of SPI transfers (refer to *Section 5.2.4* case 2), it is recommended to confirm the time slot 1 configuration also for the other times slots.

CH1_CR3 (PROG) Channel 1 Configuration Register 3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	CH1_CRCP4	CH1_NOB4					CH1_CRCP3	CH1_NOB3				
Default value:															
0	0	0	0	0	1	0	1	0	0	0	1	0	1	0	0
R/W															

Address: 010011

Type: R/W

Description:

[15:12] RESERVED

[11] CH1_CRCP4: Parity or CRC in time slot 4
0: CRC
1: parity

[10:6] CH1_NOB4: Number of data bits in time slot 4
01000: 8 data bits
…
11100: 28 data bits
others: default (20 bit)

[5] CH1_CRCP3: Parity or CRC in time slot 3
0: CRC
1: parity

[4:0] CH1_NOB3: Number of data bits in time slot 3
01000: 8 data bits
…
11100: 28 data bits
others: default (20 bit)

CH1_CR4 (PROG) Channel 1 Configuration Register 4

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	CH1_CRCP6	CH1_NOB6					CH1_CRCP5	CH1_NOB5				
Default value:															
0	0	0	0	0	1	0	1	0	0	0	1	0	1	0	0
R/W															

Address: 010100

Type: R/W

Description:

[15:12] RESERVED

[11] CH1_CRCP6: Parity or CRC in time slot 6
0: CRC
1: parity

[10:6] CH1_NOB6: Number of data bits in time slot 6
01000: 8 data bits
…
11100: 28 data bits
others: default (20 bit)

[5] CH1_CRCP5: Parity or CRC in time slot 5
0: CRC
1: parity

[4:0] CH1_NOB5: Number of data bits in time slot 5
01000: 8 data bits
…
11100: 28 data bits
others: default (20 bit)

SID1 (PROG) SID1 Configuration Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	SID1_3					SID1_2					SID1_1				
Default value:															
0	0	1	0	1	1	0	1	0	1	0	0	1	0	0	1
R/W															

Address: 010101

Type: R/W

Description:

[15] RESERVED

[14:10] SID1_3: SID bits for time slot 3 of PSI5 interface 1

[9:5] SID1_2: SID bits for time slot 2 of PSI5 interface 1

[4:0] SID1_1: SID bits for time slot 1 of PSI5 interface 1

SID2 (PROG) SID2 Configuration Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	SID1_6					SID1_5					SID1_4				
Default value:															
0	0	1	1	1	0	0	1	1	0	1	0	1	1	0	0
R/W															

Address: 010110

Type: R/W

Description:

[15] RESERVED

[14:10] SID1_6: SID bits for time slot 6 of PSI5 interface 1

[9:5] SID1_5: SID bits for time slot 5 of PSI5 interface 1

[4:0] SID1_5: SID bits for time slot 4 of PSI5 interface 1

TSM1_ESn, n=1…6 (PROG) Time Slot Monitoring Channel 1, Earliest Start of Slot n

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PAR	RESERVED			ST_CH1_n											
Default value:															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W															

Address: 010111 (TSM1_ES1) .. 011100 (TSM1_ES6)

Type: R/W

Description: default values: TSM1_TES1=0x002c , TSM1_TES2=0x00b5, TSM1 _TES3=0x8149, TSM1_ES4,5,6= 0x8000.

[15] PAR: Odd parity bit for register bits [15:0]

[14:12] RESERVED

[11:0] ST_CH1_n: Start time of time slot n on PSI5 channel 1
The start time for the given time slot after the sync pulse trigger
Steps of 1 µs

TSM1_END (PROG) Time Slot Monitoring Channel 1, End of last Slot

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PAR	RESERVED			ET_CH1_n											
Default value:															
1	0	0	0	0	0	0	1	1	1	1	0	1	1	0	0
R/W															

Address: 011101

Type: R/W

Description: default value:

[15] PAR: Odd parity bit for register bits [15:0]

[14:12] RESERVED

[11:0] ET_CH1_n: End time of time slot on PSI5 channel 1
The end time of the last given slot after the sync pulse trigger
Steps of 1 µs

DCR (PROG) Direct Command Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DCR															
Default value:															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
WO															

Address: 011110

Type: WO

Description: A write operation on this register carries out specific actions, depending on the bits written.

1) In order to perform a software reset of the L9663, the hexadecimal value 0x5555 ("unlock reset" command) has first to be written into this register, followed by the hexadecimal value 0xA5A5 ("reset" command) in the next SPI cycle. If this condition is not met, no software reset will occur.

2) In order to reset the UDB1 (Upstream Data Buffer 1) for ECU-to-sensor communication on the PSI5 channel 1, 0x00FF has to be written to this register. This also resets the UDB1_RDY bit in the UDBCR register to 0.

3) In order to reset the UDB2 (Upstream Data Buffer 2) for ECU-to-sensor communication on the PSI5 channel 2, 0xFF00 has to be written to this register. This also resets the UDB2_RDY bit in the UDBCR register to 0.

4) Writing the hexadecimal value 0x1111 into this register locks the configuration registers (EOP, End Of Programming), i.e. it is no longer possible to write the configuration registers (marked with PROG). The PROG bit in the SPI Status bits is '0' after the EOP command has been sent. This bit is reset to '1' at device reset (POR, RESETN, SW_RESET or clock error).

5) If value 0x9999 is written into this register the writing of STS or STSR registers is allowed. This is intended to grant a safety enabler for writing these couple of registers. If value 0x9999 is written in PROG phase, then both STS and STSR registers are allowed to be written, otherwise only STSR is allowed. To disable writing these two registers, value 0x9090 has to be written here. The status of the configuration (STS and STSR registers writeable or not) is shown with the STS_EN bit in the SR3 register.

CH2_CR1 (PROG) Channel 2 Configuration Register 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PAR	RESERVED	VT2_SYNC2_SEL	DOUT2_SEL	TSM2_SEL		QC2_SEL		READ_INIT_DATA2	NOTS2			RESERVED	BR2		SYNC2_EN
Default value:															
0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
R/W															

Address: 011111

Type: R/W

Description:

[15] PAR: Odd parity bit for register bits [15:0]

[14] RESERVED

[13] VT2_SYNC2_SEL: Sync pulse voltage selector for channel 2
0: 2.5 V (PSI5 ver. 2.x common and low power mode)
1: 3.5 V (PSI5 ver. 2.x common mode only, and PSI5 ver. 1.3)

[12] DOUT2_SEL: Configuration of DOUT2 pin
0: DOUT1 transmits PSI5 data
1: DOUT1 is an interrupt output

[11:10] TSM2_SEL: Time slot monitoring on PSI5 channel 2
00: monitoring disabled
11: monitoring disabled
01: standard monitoring enabled
10: simple monitoring enabled

[9:8] QC2_SEL: Quiescent current limit (extended+ current) on PSI5 interface 2
00: standard current (19 mA)
01: extended current (35 mA)
11: extended current (35 mA)
10: extended+ current (45 mA)

[7] READ_INIT_DATA2: Read sensor initialization data on ch 2
0: init data not stored
1:init data stored in dedicated buffer.

[6:4] NOTS2: Number of time slots on PSI5 interface 2
001: 1 time slot
…
110: 6 time slots
others: default (3 slots)

[3] RESERVED

[2:1] BR2: Baud rate of PSI5 interface 2
00: 125 kb/s
11: 125 kb/s
01: 189 kb/s
10: 83.3 kb/s

[0] SYNC2_EN: Asynchronous or synchronous mode on PSI5 interface 2
0: asynchronous mode (SYNC pulse disabled, FIFO data buffer)
1: synchronous mode

CH2_CR2 (PROG) Channel 2 Configuration Register 2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	CH2_BT_DIS2	CH2_CRCP2	CH2_NOB2					CH2_CRCP1	CH2_NOB1				
Default value:															
0	0	0	0	0	1	0	1	0	0	0	1	0	1	0	0
R/W															

Address: 100000

Type: R/W

Description:

[15:13] RESERVED

[12] CH2_BT_DIS2: Bootstrap ch2 disable
0: enabled
1: disabled

[11] CH2_CRCP2: Parity or CRC in time slot 2
0: CRC
1: parity

[10:6] CH2_NOB2: Number of data bits in time slot 2
01000: 8 data bits
…
11100: 28 data bits
others: default (20 bit)

[5] CH2_CRCP1: Parity or CRC in time slot 1
0: CRC
1: parity

[4:0] CH2_NOB1: Number of data bits in time slot 1
01000: 8 data bits
…
11100: 28 data bits
others: default (20 bit)

Settings programmed for time slot 1 are automatically applied to the other time slots in case at least one of the following conditions in CH2_CR2 register is verified:
– READ_INIT_DATA2 = '1'
– TSM2_SEL = ‘10’ (simple configuration)
– SYNC2_EN = '0' (asynchronous mode)
Although the settings of time slot 1 are automatically applied by the logic to other time slots, these are not written in the corresponding configuration registers. In order to avoid not up-to-date readout of the time slot configuration by SPI and to prevent from wrong SPI errors in case of mismatches in the number of SPI transfers (refer to *Section 5.2.4* case 2), it is recommended to confirm the time slot 1 configuration also for the other times slots.

CH2_CR3 (PROG) Channel 2 Configuration Register 3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	CH2_CRCP4	CH2_NOB4					CH2_CRCP3	CH2_NOB3				
Default value:															
0	0	0	0	0	1	0	1	0	0	0	1	0	1	0	0
R/W															

Address: 100001

Type: R/W

Description:

[15:12] RESERVED
[11] CH2_CRCP4: Parity or CRC in time slot 4
0: CRC
1: parity
[10:6] CH2_NOB4: Number of data bits in time slot 4
01000: 8 data bits
…
11100: 28 data bits
others: default (20 bit)
[5] CH2_CRCP3: Parity or CRC in time slot 3
0: CRC
1: parity
[4:0] CH2_NOB3: Number of data bits in time slot 3
01000: 8 data bits
…
11100: 28 data bits
others: default (20 bit)

CH2_CR4 (PROG) Channel 2 Configuration Register 4

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	CH2_CRCP6	CH2_NOB6					CH2_CRCP5	CH2_NOB5				
Default value:															
0	0	0	0	0	1	0	1	0	0	0	1	0	1	0	0
R/W															

Address: 100010

Type: R/W

Description:

[15:12] RESERVED

[11] CH2_CRCP6: Parity or CRC in time slot 6
0: CRC
1: parity

[10:6] CH2_NOB6: Number of data bits in time slot 6
01000: 8 data bits
…
11100: 28 data bits
others: default (20 bit)

[5] CH2_CRCP5: Parity or CRC in time slot 5
0: CRC
1: parity

[4:0] CH2_NOB5: Number of data bits in time slot 5
01000: 8 data bits
…
11100: 28 data bits
others: default (20 bit)

SID3 (PROG) SID3 Configuration Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	SID_CH2_S3						SID_CH2_S2					SID_CH2_S1			
Default value:															
0	1	0	0	1	1	1	0	0	1	0	1	0	0	0	1
R/W															

Address: 100011

Type: R/W

Description:

[15] RESERVED

[14:10] SID_CH2_S3: SID bits for time slot 3 of PSI5 interface 2

[9:5] SID_CH2_S2: SID bits for time slot 2 of PSI5 interface 2

[4:0] SID_CH2_S1: SID bits for time slot 1 of PSI5 interface 2

SID4 (PROG) SID4 Configuration Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	SID_CH2_S6						SID_CH2_S5					SID_CH2_S4			
Default value:															
0	1	0	1	1	0	1	0	1	0	1	1	0	1	0	0
R/W															

Address: 100100

Type: R/W

Description:

[15] RESERVED

[14:10] SID_CH2_S6: SID bits for time slot 6 of PSI5 interface 2

[9:5] SID_CH2_S5: SID bits for time slot 5 of PSI5 interface 2

[4:0] SID_CH2_S4: SID bits for time slot 4 of PSI5 interface 2

TSM2_ESn, n=1…6 (PROG) Time Slot Monitoring Channel 2, Earliest Start of Slot n

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PAR	RESERVED			ST_CH2_n											
Default value:															
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W															

Address: 100101 (TSM1_ES1) .. 101010 (TSM1_ES6)

Type: R/W

Description: default values: TSM2_TES1=0x002c, TSM2_TES2=0x00b5, TSM2 _TES3=0x8149, TSM2_ES4,5,6= 0x8000.

[15] PAR: Odd parity bit for register bits [15:0]

[14:12] RESERVED

[11:0] ST_CH2_n: Start time of time slot n on PSI5 channel 2
The start time for the given time slot after the sync pulse trigger
Steps of 1 µs

TSM2_END (PROG) Time Slot Monitoring Channel 2, End of last Slot

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PAR	RESERVED			ET_CH2_n											
Default value:															
1	0	0	0	0	0	0	1	1	1	1	0	1	1	0	0
R/W															

Address: 101011

Type: R/W

Description:

[15] PAR: Odd parity bit for register bits [15:0]

[14:12] RESERVED

[11:0] ET_CH2_n: End time of time slot on PSI5 channel 2
The end time of the last given slot after the sync pulse trigger
Steps of 1 µs

STS (PROG) Self-Test Setting - prog time

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FCRCM	RESERVED				DOUTTP	DOUTSEL					RESERVED				
Default value:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W															

Address: 101100

Type: R/W

Description:

[15] FCRCM: Force CRC mismatch on MISO
0: NOP
1: the least significant bit of CRC is inverted

[14:11] RESERVED

[10] DOUTTP
Value ('0' or '1') to be output on DOUTx pin

[9:5] DOUTSEL: DOUTx channel activation
10101: DOUT1
10110: DOUT2
others: ignored

[4:0] RESERVED

STRS Self-Test Setting - run time

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	FSIDM	FTSIDM	RESERVED							ACCT	SCCT		RESERVED		TBEC
Default value:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W															

Address: 101101

Type: R/W

Description:

[15] RESERVED

[14] FSIDM: Force SID mismatch

0: NOP

1: the behavior of the MUX which selects SID, CRC/parity and Number of bits, is changed according to the following table:

slot1 <-->slot2

slot3<-->slot4

slot6<-->slot5

[13] FTSIDM: Force TSID mismatch

0: NOP

1: the behavior of MUX that selects sensor data (and SID) for each time slot is modified in this way:

– slot2 sensor data -> slot1 sensor data

– slot4 sensor data ->slot3 sensor data

– slot6 sensor data ->slot5 sensor data

Sensor data of time slots 1, 3 and 5 keep a buffer empty value.

[12:6] RESERVED

[5] ACCT: Abort cross-coupling test

0: NOP

1: Stop cross-coupling test immediately

[4:3] SCCT: Start cross-coupling test

11: ignored

00: ignored

01: start cross-coupling test in master mode

10: start cross-coupling test in slave mode

[2:1] RESERVED

[0] TBEC: Test buffer empty check

0 : after a read operation 1F0 is written into the buffer (normal operation)

1 : after a read operation old data are left In the buffer

ADVSET1 (PROG) Advanced Settings 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STG_MASK	FIXED_THR_SEL				RESERVED	TRACKING_SEL	BLANKING_SEL		DATA_FILT_SEL				FREEZE_DIS	RESERVED	FIXED_THR
Default value:															
0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0
R/W															

Address: 101110

Type: R/W

Description: Advanced settings for interface 1

[15] STG_MASK: Short to ground does not switch off channel
0: short to ground switches off the channel after filter time
1: short to ground does NOT switch off the channel

[14:11] FIXED_THR_SEL: Fixed threshold setting for PSI5 channel 1
Ibase + 5.5mA + (15-5.5)/16*bits[14:11]mA (1)

[10] RESERVED

[9] TRACKING_SEL
0: Standard threshold tracking algorithm (default, recommended)
1: Fast tracking algorithm

[8:7] BLANKING_SEL: Blanking time selector at sensor startup:
00/11 : 128 µs
01 : 5 ms
10: 10 ms

[6:3] DATA_FILT_SEL: Deglitch filter adjust
Baud rate = 189K: filter time = (16 + <DATA_FILT_SEL>) * Tosc
Baud rate = 125K or 83.3K: filter time = (24 + <DATA_FILT_SEL>) * Tosc
Note:Tosc is the period of the 16 MHz oscillator

[2] FREEZE_DIS: Freezing of base current tracking after start bits are detected
0: frozen
1: not frozen

[1] RESERVED

[0] FIXED_THR: Adaptive / fixed threshold
0: adaptive threshold
1: fixed threshold

1. The selectable threshold is in the range: Ibase+5.5 mA to Ibase+14.4 mA

ADVSET2 (PROG) Advanced Settings 2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REACTTIME	RESERVED		BITTIME_H_DET2	PERIOD_M_DIS2	STBIT_DC_CK_DIS2	STBITERR_RST_CNT2	RESERVED		BITTIME_H_DET1	PERIOD_M_DIS1	STBIT_DC_CK_DIS1	STBITERR_RST_CNT1	SYNC_DELAY_PSI1_PSI2		
Default value:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W															

Address: 101111

Type: R/W

Description: Advanced settings for interface 2

[15] REACTTIME: Reaction time for FLL module reset after error detection
0: 0ms
1: 20ms

[14:13] RESERVED

[12] BITTIME_H_DET2: Manchester decoder Bit time error detect on PSI2
0: bittime too high error is not detected as error
1: bittime too high error is detected as error

[11] PERIOD_M_DIS2: Disable bit time Period measurement for frame decoding on PSI2
0: measurement of start bits period enabled
1: measurement of start bits period disabled

[10] STBIT_DC_CK_DIS2: Duty cycle check (DC>0.25) on start bits
0: duty cycle check enabled
1: duty cycle check disabled

[9] STBITERR_RST_CNT2: Manchester decoder Bit counter reset upon start bit error
0: start bit error does not reset the counter
1: start bit error resets the counter

[8:7] RESERVED

[6] BITTIME_H_DET1: Manchester decoder Bit time error detect on PSI1
0: bittime too high error is not detected as error
1: bittime too high error is detected as error

[5] PERIOD_M_DIS1: Disable bittime Period measurement for frame decoding on PSI1
0: measurement of start bits period enabled
1: measurement of start bits period disabled

[4] STBIT_DC_CK_DIS1: Duty cycle check (DC>0.25) on start bits
0: duty cycle check enabled
1: duty cycle check disabled

[3] STBITERR_RST_CNT1: Manchester decoder Bit counter reset upon start bit error
0: start bit error does not reset the counter
1: start bit error resets the counter

[2:0] SYNC_DELAY_PSI1_PSI2: SYNC pulse time delay between PSI5 interface 1 and 2 in case of automatic SYNC pulse generation
This bit takes effect only in case of automatic generation on both interfaces
000: no delay
001 - 111: 2µs/LSB

ADVSET3 (PROG) Advanced Settings 3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STG_MASK	FIXED_THR_SEL				RESERVED	TRACKING_SEL	BLANKING_SEL		DATA_FILT_SEL				FREEZE_DIS	RESERVED	FIXED_THR
Default value:															
0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0
R/W															

Address: 110000

Type: R/W

Description: Advanced settings for interface 3

[15] STG_MASK: Short to ground does not switch off channel
0: short to ground switches off the channel after filter time
1: short to ground does NOT switch off the channel

[14:11] FIXED_THR_SEL: Fixed threshold setting for PSI5 channel 2
Ibase + 5.5mA + (15-5.5)/16*bits[14:11]mA (1)

[10] RESERVED

[9] TRACKING_SEL:
0: Standard threshold tracking algorithm (default, recommended)
1: Fast tracking algorithm

[8:7] BLANKING_SEL: Blanking time selector at sensor startup:
00 : 128 µs
11: 128 µs
01: 5 ms
10: 10 ms

[6:3] DATA_FILT_SEL: Deglitch filter adjust
Baud rate = 189K: filter time = (16 + <DATA_FILT_SEL>) * Tosc
Baud rate = 125K or 83.3K: filter time = (24 + <DATA_FILT_SEL>) * Tosc
Note: Tosc is the period of the 16 MHz oscillator

[2] FREEZE_DIS: Freezing of base current tracking after start bits are detected
0: frozen
1: not frozen

[1] RESERVED

[0] FIXED_THR: Adaptive / fixed threshold
0: adaptive threshold
1: fixed threshold

1. The selectable threshold is in the range: Ibase+5.5 mA to Ibase+14.4 mA.

ADVRD1 Advanced Read 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						BASE1									
Default value:															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W															

Address: 110010

Type: RO

Description:

[15:10] RESERVED

[9:0] BASE1: Base current level on PSI5 channel 1

ADVRD2 Advanced Read 2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						DELTA1									
Default value:															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
RO															

Address: 110011

Type: RO

Description:

[15:10] RESERVED

[9:0] DELTA1: Delta current level I(threshold) - I(base) on PSI5 channel 1

ADVRD3 Advanced Read 3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						THRESH1									
Default value:															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
RO															

Address: 110100

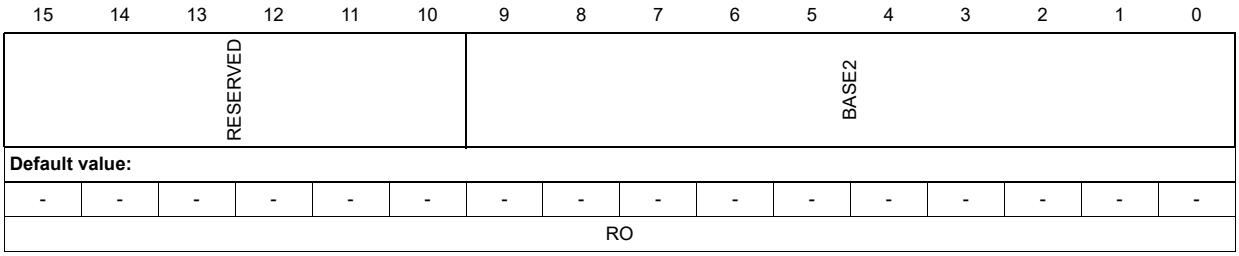
Type: RO

Description:

[15:10] RESERVED

[9:0] THRESH1: Threshold current level on PSI5 channel 1 (absolute value)

ADVRD4 Advanced Read 4



Address: 110101

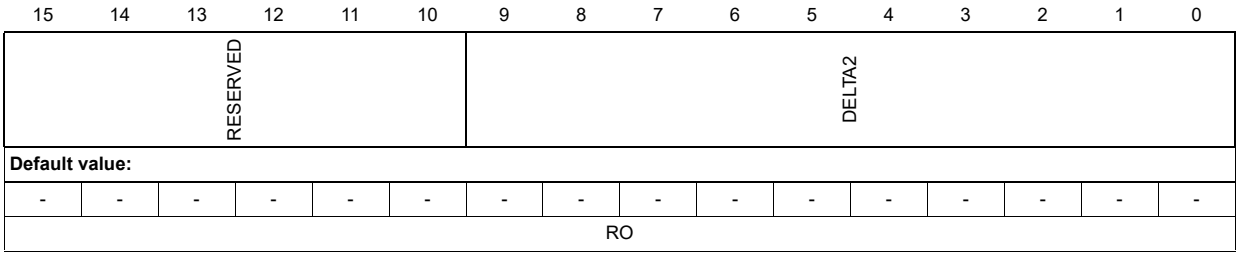
Type: RO

Description:

[15:10] RESERVED

[9:0] BASE2: Base current level on PSI5 channel 2

ADVRD5 Advanced Read 5



Address: 110110

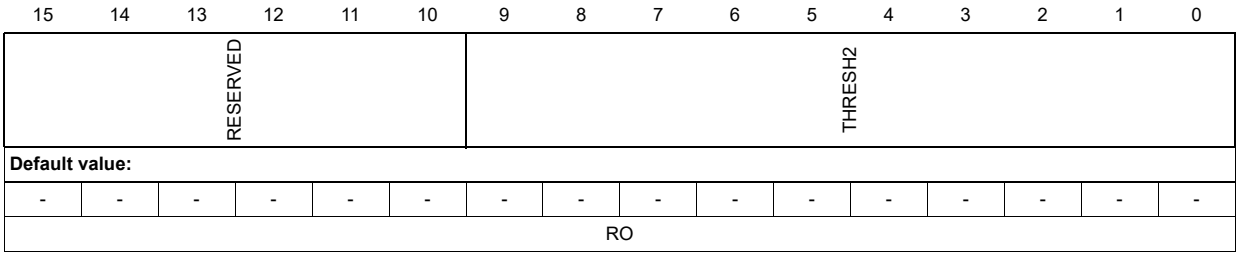
Type: RO

Description:

[15:10] RESERVED

[9:0] DELTA2: Delta current level I(threshold) - I(base) on PSI5 channel 2

ADVRD6 Advanced Read 6



Address: 110111

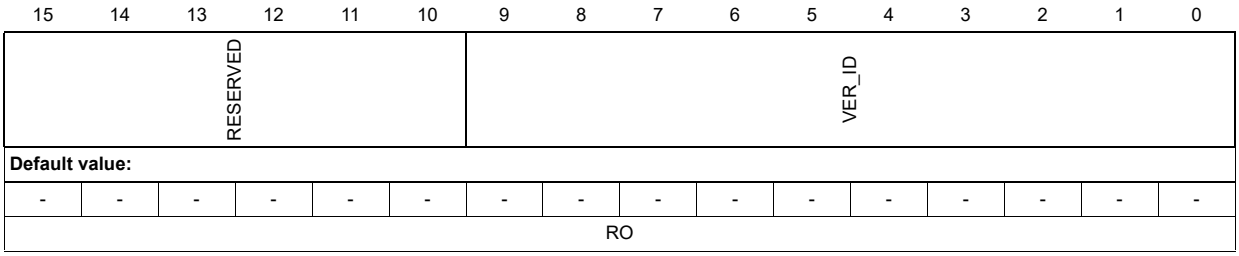
Type: RO

Description:

[15:10] RESERVED

[9:0] THRESH2: Threshold current level on PSI5 channel 2 (absolute value)

DEVID Device Version ID



Address: 111000

Type: RO

Description:

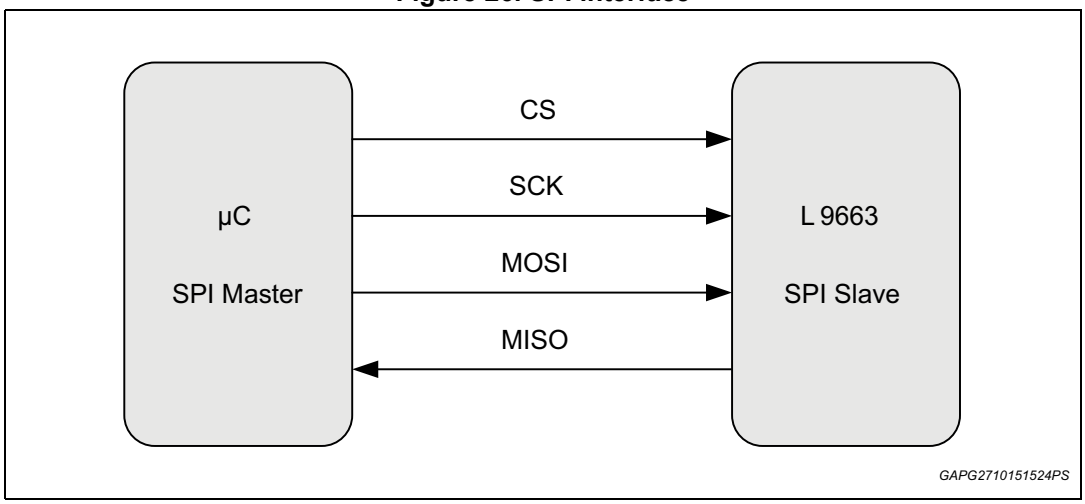
[15:10] RESERVED

[9:0] VER_ID: Device Version ID
Static value for silicon version.
b<9:6>: ST reserved
b<5:3>: mask set reference "000"=A,"001"=B,…
b<2:0>: mask set revision "000"=A,"001"=B,…

5.2 SPI interface

5.2.1 Physical layer and signal description

Figure 26. SPI interface



Chip Select (CS)

The communication interface is deselected when this input signal is logically high. A falling edge on CS enables and starts the communication, while a rising edge finishes the communication and the command is executed if a valid frame has been sent. During communication start and stop, the Serial Clock (SCLK) has to be logically low. The MISO line is in high impedance when CS is high.

In order to considerably reduce the number of CS lines and pins on the system, while still allowing connecting different devices, an address multiplexing approach is implemented in the device with cabled address "00".

This means that if CS is low the device is not selected unless the MOSI bits 31 and 30 of the frame matches the device address.

This feature can be disabled by SW, writing a dedicated SPI bit.

The default state after reset (sw, hw or by internal clock fault) is in the address multiplexing mode.

Serial Clock (SCLK)

This SCLK provides the clock of the SPI. Data present on the MOSI line is latched on the falling edge of Serial Clock (SCLK) into the internal shift registers, while data from the internal shift registers are shifted out on the MISO line on the rising edge.

MOSI

This input is used to transfer data serially into the device. Data is latched on the falling edge of Serial Clock (SCLK).

MISO

This output signal is used to transfer data serially out of the device. Data is shifted out on the rising edge of Serial Clock (SCLK). MISO is in high impedance under POR condition.

5.2.2 Clock and data characteristics

A microcontroller with its SPI peripheral running in the following mode can drive the SPI:

CPOL = '0' and CPHA = '1'.

The communication frame starts with the falling edge of the CS (Communication Start). SCLK has to be low.

The MOSI data are then latched on all following falling SCLK edges into the internal shift registers.

After Communication Start, the MISO will leave tri-state and shift the MSB of the output data on MISO. On all following rising SCLK edges data are shifted out through the internal shift registers to MISO.

The communication frame is finished with the rising edge of CS. If a valid communication took place (e.g. correct number of SCLK cycles), the operation requested will be performed (Write or Clear operation).

5.2.3 Frame definition

Global status bits (standard mode)

31	30	29	28	27	26
SPIE	FSR1	FSR2	RSTB	PROG	GSB

Global status bits (address multiplexing mode)

31	30	29	28	27	26
-	-	-	RSTB	PROG	GSB

Type: R

Bit Description

[31] SPIE: SPI error
The SPIE bit is a logical OR combination of errors related to wrong SPI communication (wrong SCLK count, wrong CRC, wrong SPI operation). It is also reported as SR1[12] bit and it is automatically cleared when this register is read.

[30] FSR1: Fault status register 1 flag
The FSR1 bit is set to '1' if at least one of the bits SR1[11:0] is active.

[29] FSR2: Fault status register 2 flag
The FSR2 bit is set to '1' if at least one of the bits SR2[14:8] or SR2[6:0] is active.

[28] RSTB: Reset bit
The RSTB bit indicates a device reset (POR, RESETN or SW_RESET). In case this bit is set, all internal Control Registers are set to their default values and kept in that state until the bit is cleared after a read access on SR3 register and the fault is not present anymore.

[27] PROG: End of programming
The EOP bit indicates the end of the device programming phase (PROG registers).

[26] GSB: Global Status Bit
The GSB bit is a logical OR combination of Bit 31 to Bit 27 and buffer empty error bit. This stands also for address multiplexing mode.

The global status bits are shifted out on the MISO line on every SPI access. They provide information about the current device status.

5.2.4 Communication frames

In the following frames, all fields are written with MSB at left side and 'X' represents a "don't care" value.

The bit RW is used to select the operation type on the internal register: read (RW=0), write (RW=1).

CRC on MOSI is calculated over bits 31:5, with "000" appended after LSB.

CRC on MISO instead, depends on the setting of GCR1[1]:

a) CRC calculated from the sensor.

b) CRC calculated over MISO bits 26:3, with "000" appended after LSB.

CRC generation is based on the same calculation scheme used for PSI5 sensor data (generator polynomial g(x)=1+x+x3, initialization value "111") with MSB passed first.

In case the IC receives a not valid register address on MOSI, the address bit are recognized as invalid address; in this case the two last bit on MISO (i.e. CRC[1:0]) are intentionally corrupted, inverting their values (NOT operator).

The same action is also performed either in case of access to a not valid register (address > 59) or in case of:

- slot error when PSI5 data SPI frame.
- write access to read only registers.
- Frame L-H wrong sequence.

Figure 27. Operation on internal register (with upstream data buffer)

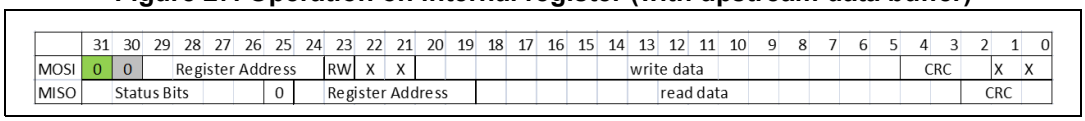
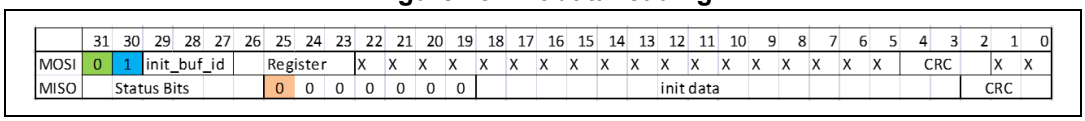


Figure 28. Init data reading



Sensor data Reading:

Timeslot coding: Timeslot1=001, …, timeslot6=110

SID and Gbit are supported only for 10 - 16 bit and enabled by 1 single configuration bit = GCR1(2)

Two kinds of transfer are possible:

1. No SID, payload ≤ 20 bit; SID and GBIT, payload ≤ 16 bit: one transfer needed
2. No SID, payload > 20 bit: two transfers are needed.

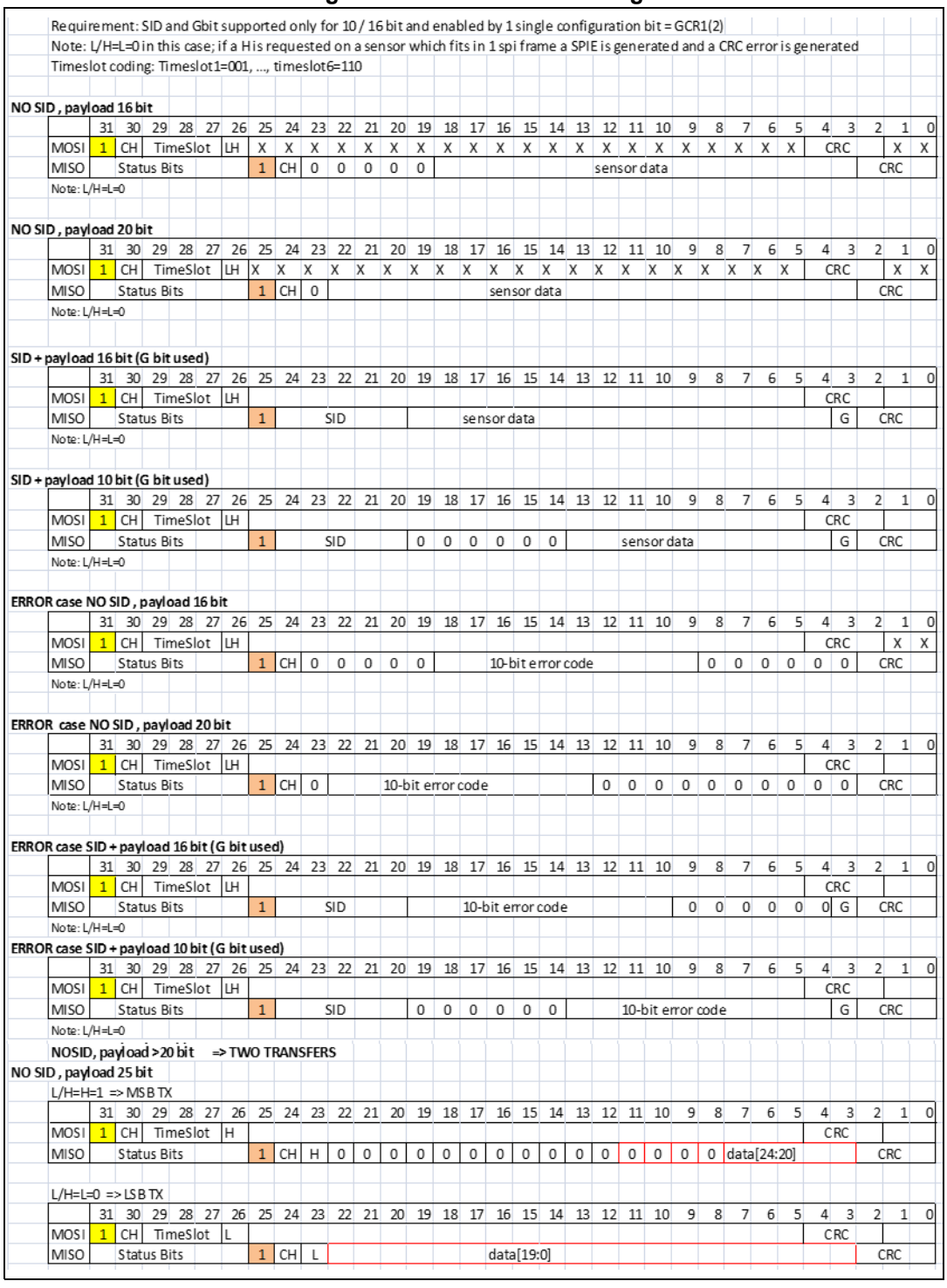
In case 1) the L/H bit must be L (0).

In case 2) the device expects a sequence H - L on the L/H bit to transmit first the MSB part of the data and then the LSB.

To guarantee a safe communication with two SPI transfers:

- if CRC is the one from the sensor (GCR1(1)=0) , CRC is the same on both transfers and it's the one from the sensor;
- if CRC is calculated on SPI (GCR1(1)=1), CRC is calculated over bits 26:3 in each frame.

Figure 29. Sensor data reading



In case of sensor fault conditions, error codes are sent in the first 10 bits of the data field (see *Table 6 on page 31*). The lower 10 bits are filled with '0'.

SPI error handling

The SPI message from the external microcontroller is monitored. The following errors are detected:

- the CRC on the MOSI line is not correct;
- incorrect SPI operation (e.g. an attempt to write a read-only register);
- the number of SPI clock cycles is not equal to 32.

In case any of the above-mentioned errors is detected, the MOSI message is rejected, the SPI failure bit in the SR1 register is set and the SPIE status bit in the next MISO message is set to '1'.

5.3 Direct interface

The direct interface has the following features:

- DOUTx output for Manchester-coded sensor data
- SYNCx input for synchronous pulse voltage trigger
- Deglitch filter for SYNCx input of PSI5 transceiver

The reference voltage for the threshold levels of DOUTx pins is VDD.

The direct interface is only used in transceiver IC mode 2 (data decoding in the µC).

To use direct mode slot monitor should be disabled on the channel.

In order to have good device functionality all registers, except the ones listed below, must be configured if default values do not match the application.(j)

The registers that do not need a configuration are the following: SIDx, TSMx_ESy, TSMx_END.

Optional configuration: SPT (if sync pulse period is smaller than 500 µs), ADVSET1/2/3 if a particular set of tracking is required, UDBCR, UDBx_y to use tooth gap method, DCR, STS, STSR.

j. Registers needing a configuration: CHCNT, CHx_CR1, CHx_CR2, CHx_CR3, CHx_CR4, GCR1.

6 Electrical characteristics

Table 10. Operating conditions

Symbol	Parameter / Condition[1]	Min	Typ	Max	Unit
V_{VB}	VB input voltage	4.8	–	35	V
V_{VASSUP}	VASSUP input voltage (in case V_{AS} pre-regulator is used)	4.8	–	35	V
V_{VDD}	VDD input voltage	3	–	6	V
T_j	Junction temperature	-40	–	175	°C

1. Unless otherwise specified.

Table 11. VINTx internal supply

Symbol	Parameter / Condition	Min	Typ	Max	Unit
VDDwu_H	VDD voltage level for power up	2.3	2.5	2.7	V
VDDwu_L	VDD voltage level for power down	1.5	1.8	2.3	V
VINTDuv	VINTD under voltage threshold	2.7	–	2.9	V
VINTDov	VINTD over voltage threshold	3.47	–	3.66	V
VINTAuv	VINTA under voltage threshold	2.97	–	3.13	V
VINTAov	VINTA over voltage threshold	3.47	–	3.66	V
$DGND_{OPEN}$	DGND ground loss threshold GND1 = GND2 = 0	100	200	300	mV
T_{POR}	Filter time for power on reset output (vintx ov/uv, dgnd open)	5	–	45	µs
T_{WAKE}	Start-up time in no fault conditions (from VDD=3V to internal power on reset set to ‘1’) (Design info)	–	–	250	µs
$I_{limVINTD}$	V_{INTD} current limitation	80	–	150	mA
C_{VINTD}	V_{INTD} filter capacitance (Test info)	60	100	140	nF

Table 12. V_{AS} supply

Symbol	Parameter / Condition	Min	Typ	Max	Unit
V_{AS}	Supply voltage V_{AS} normal operation (Test info)	4.3	–	16	V
$V_{AS,rip}$	Max. voltage ripple on V_{AS} (1) (Test info)	-1.5	–	1	V
$SR\_V_{AS,rip}$	Slew rate of the voltage ripple on V_{AS} (Test info)	–	–	50	mV/µs
$I\_V_{AS,eff}$	Effective current for V_{AS}: (Design info) 2 * 60 mA (effective for 45 mA supply current; 30mA data current) + 5mA current for all included Transceiver blocks supplied from V_{AS}.	–	–	125	mA
$I\_V_{AS,peak}$	Dynamic current for V_{AS}: (Design info) 1 * 75 mA (45 mA supply current; 30mA data current) + 130 mA (STG on 2nd IF) + 5 mA current for all included Transceiver blocks supplied from V_{AS}.	–	–	210	mA

1. This voltage ripple, that will anyhow not exceed minimum V_{AS} voltage value, does not lead to corrupted data reception.

Table 13. V_{AS} external MOS

Symbol	Parameter / Condition(1)	Min	Typ	Max	Unit
V_{gs_ext}	Gate to Source voltage (Test info)	-20	–	20	V
V_{gsth_ext}	Gate threshold voltage, with $V_{DS} = V_{GS}$, I_D = 250 µA (Test info)	1	–	2.5	V
V_{gl_ext}	Gate leakage current at V_{GS} = 20 V, V_{DS} = 0 V (Test info)	-10	–	10	µA
R_{dson_ext}	Drain to Source on state resistance at V_{GS} = 4.5 V, ID = 2.6 A (Test info)	–	–	150	mΩ
C_{iss_ext}	Input Capacitance at V_{GS}=0V, V_{DS}=25V f=1MHz (Test info)	–	–	1100	pF
C_{oss_ext}	Output Capacitance at V_{GS}=0V, V_{DS}=25V f=1MHz (Test info)	–	–	170	pF
td_{on_ext}	Turn on delay time at VDS=30V, VGS=4.5V, ID=2.6A, RG=16Ω (Test info)	–	–	20	ns

1. Main parameters for choice of external component.

Table 14. V_{AS} pre regulator

Symbol	Parameter / Condition	Min	Typ	Max	Unit
V_{AS5DC}	Regulated V_{AS} voltage 5.3 V output selection V_{SUP} ≥ 5.8 V (supply of external NFET) VASSUP ≥ 5.3 V Static load condition: 4 mA ≤ Iload ≤ 210 mA	-2.5%	5.3	+2%	V
V_{AS7DC}	Regulated V_{AS} voltage 7.6 V output selection V_{SUP} > 8 V (supply of external NFET) VASSUP ≥ 7.6V Static load condition 4 mA ≤Iload ≤210 mA	-4%	7.6	4%	V
V_{AS5LS}	Maximum ripple on V_{AS} output in load step condition 5.3 V output selection V_{SUPR} ≥ 5.8 V (supply of external NFET) VASSUP ≥ 5.3 V Transient load: 0 mA to 210 mA and 210 mA to 0 mA in 0.5 µs	-5%	VAS5DC	+5%	V
V_{AS7LS}	Maximum ripple on V_{AS} output in load step condition 7.6 V output selection V_{SUP} > 8V (supply of external NFET) VASSUP ≥ 7.6 V Transient load: 0 mA to 210 mA and 210 mA to 0 mA in 0.5 µs	-5%	VAS7DC	5%	V
V_{AS}	Maximum ripple voltage on the transceiver during current modulation (dI/dt = ±60mA/ µs)	–	–	|2|	%
V_{VGS_RPD}	V_{GS} passive pull-down clamping structure (device off) Test condition: Isink = 100 µA	–	–	1.5	V
I_{VGS_IPD}	V_{GS} active pull-down current (regulator disabled, VAS_EN=0, device on)	–	1	1.2	mA
–	V_{GS} to V_{AS} passive clamp (V_{AS} shorted to ground, regulator switched on)	8	12	16	V
C2	Decoupling capacitor (Test info)	1.7	4.7	6.3	µF
ESR_{C2}	ESR of decoupling capacitor (Test info)	0	–	0.2	Ω
VASSUPuv	VASSUP under voltage threshold for enabling of internal charge pump	11.8	–	13	V
VASton	VAS startup timing after VAS_EN='1' (on by default at POR release)	–	–	1	ms

Table 15. V_{SYNCx}

Symbol	Parameter / Condition	Min	Typ	Max	Unit
$V_{CBclamp}$	Voltage limitation on CB V(BHx)-V(BLx)	–	–	8	V
V_{CBov}	VB over voltage threshold for bootstrap disabling	18	–	21	V
t_{ch_ini}	Initial time interval necessary to charge CB = 10µF from 0V to 4V@V_B = 4.8V	–	–	2	ms
t_{ch}	Recharge time for bootstrap capacitor min. sync pulse amplitude = 2.5 V; all sync pulses are long (for logical 1, pulse width); V_B = 5.2 V.	–	–	130	µs
t_{ch_reset1}	Start of CB1 charging after release of internal POR	–	–	1	µs
t_{ch_reset2}	Delay between start of CB2 charging with respect to start of CB1 charging (staggered charging)	–	2	–	ms
V_B	V_B voltage for full functionality	5.2	–	35	V
V_B	V_B voltage for full functionality (low power mode)	4.8	–	5	V
CBx	Capacitor value	5	10	15	µF

Table 16. PSI5 output supply

Symbol	Parameter / Condition	Min	Typ	Max	Unit
I_{PSIx}	Interface quiescent current (standard current)	-19	–	-4	mA
I_{PSIx}	Interface quiescent current (extended current)	-35	–	-4	mA
I_{PSIx}	Interface quiescent current (extended+ current)	-45	–	-4	mA
$V_{PSIx,max}$	Max. output voltage excluding sync. pulse (internal regulation, VAS=16V)	–	–	11	V
$V_{PSIxsync,max}$	Max. output voltage including sync. pulse (internal regulation, VAS=16V)	–	–	16.5	V
I_{STG}	Static short to ground current limitation for each transceiver output PSIx	-130	–	-80	mA
t_{Ifilt}	Filter time for current limitation detection	128	–	–	µs
t_{Iblank}	Blanking time on current limitation detection (active at PSIx output start-up in addition to the filter time) Selectable by SPI: 128 µs/5ms/10ms	128	–	–	µs
R_{INT}	Internal resistance of complete path (from input pin V_{AS} to output pin PSIx, Iload=<75mA) VAS from	4	–	8.5	W
T_{OT}	Over temperature detection	175	–	200	°C

Table 16. PSI5 output supply (continued)

Symbol	Parameter / Condition	Min	Typ	Max	Unit
I_{LTG_std}	Leakage to ground detection (standard current)	-9%	-23	+13%	mA
I_{LTG_ext}	Leakage to ground detection (extended current)	-9%	-42	+9%	mA
I_{LTG_ext+}	Leakage to ground detection (extended+ current)	-9%	-54	+9%	mA
I_{OL}	Open load detection	-4	-2.5	-1	mA
V_{STB}	Short to battery reverse voltage detection	10	–	100	mV
t_{STB}	Short to battery reverse voltage filter time	6	10	19.5	µs
I_{STB}	Static reverse current into PSIx pin $V_{PSIx} > V_{AS}$	–	–	20	mA
I_{BO}	Base current Default value of receiver	-9%	15	+9%	mA
I_{PSIxTH}	Trigger point for signal current threshold (fixed threshold mode, assuming a nominal programming of IBO + 6 mA for low power mode, see ADVSETx(FIXED_THR_SEL))	I_{BO} + 5.14	I_{BO} + 6	I_{BO} + 6.86	mA
	Trigger point for signal current threshold (fixed threshold mode, assuming a nominal programming of IBO + 12mA for common mode, see ADVSETx(FIXED_THR_SEL))	I_{BO} + 10.29	I_{BO} + 12	I_{BO} + 13.71	
V_{PSIxU}	PSIx under voltage monitoring threshold	3.1	3.3	3.5	V
t_{PSIxU}	PSIx under voltage monitoring filter time	200	–	–	µs
I_{XCT}	PSIx pull down current for cross coupling test	25	32	39	mA

Table 17. PSI5 receiver

Symbol	Parameter / Condition	Min	Typ	Max	Unit
f_{slow}	PSI5 baud rate (slow)	-	83.3	-	kbps
f_{std}	PSI5 baud rate (standard)	-	125		kbps
f_{fast}	PSI5 baud rate (fast)	-	189	-	kbps
	Data frame length (without overhead)(1)	8/10	-	28	bit

1. Also 8 bit compatibility according to PSI5 v1.3.

Figure 30. Sync generator

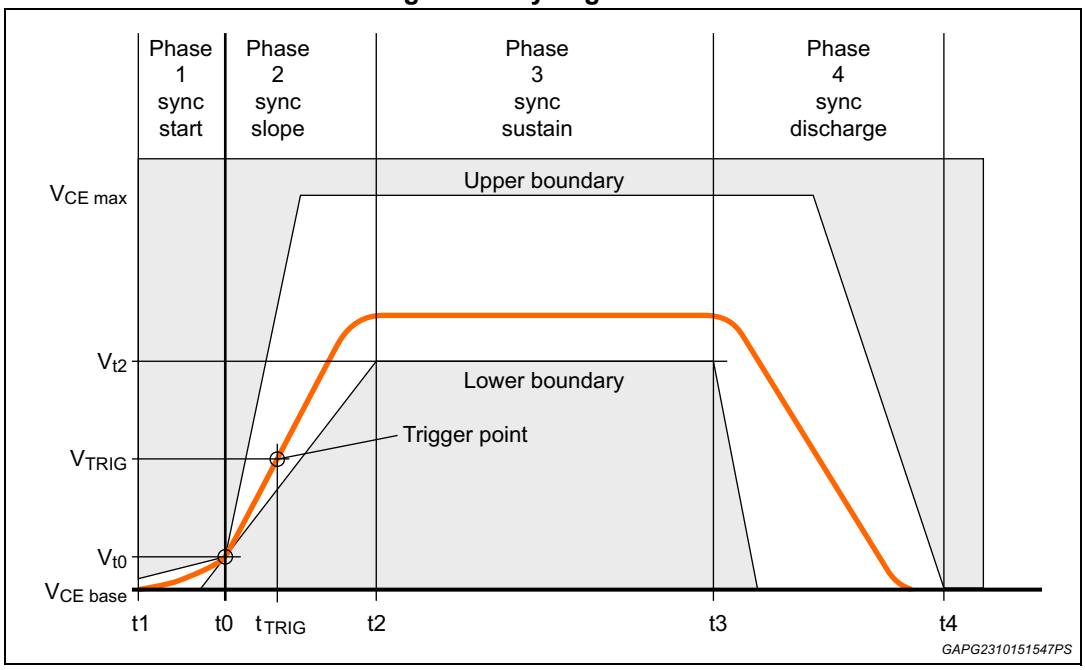


Table 18. Sync generator

Symbol	Parameter / Condition	Min	Typ	Max	Unit
t_w	Trigger signal duration to generate a short Sync Pulse (std PSI5) (1)	1	-	5	µs
V_{t2}	Voltage increase of sync pulse normal operation (Ibase ≤ 35 mA, VB ≥ 4.8 V)	2.5	-	-	V
V_{t2}	Voltage increase of sync pulse normal operation (Ibase ≤ 35 mA, VB ≥ 5.2 V	2.5/3.5	-	-	V
SR_{rise}	Slew rate of rising sync slope	0.43	-	1.5	V/µs
SR_{fall}	Slew rate of falling sync slope	-1.5	-	-	V/µs
t_0	Reference time (@ 0.5 V on top of VCEbase)	-	0	-	µs
t_1	Sync signal earliest start Delta current less than 2 mA	-3.25	-	-	µs
t_2	Sync signal sustain start (@ Vt2)	-	-	7	µs
t_3	Sync signal sustain time (short/long pulse)	16/43	-	-	µs
t_{sync_slow}	Slow Vsync detection time	10	-	14	µs
t_4	Discharge time limit (short/long pulse)	-	-	35/62	µs
$t_{Slot\ 1\ Start}$	Start of first sensor data word (short/long pulse)	44/71	-	-	µs

Table 18. Sync generator (continued)

Symbol	Parameter / Condition	Min	Typ	Max	Unit
I_{Limit}	Static current limitation for each transceiver output PSIx (only for sync pulse generator)	-280	-	-110	mA
t_{d_SPI}	Delay between end of SPI trigger command and start of sync pulse (t1)	-	-	2.2	µs
t_{d_SYNC}	Delay between SYNC pin command filtered ($t_{deglitch}$ not included) and start of sync pulse (t1)	-	-	1	µs

1. Only the short sync pulse can be triggered by PIN (tw ≤5 µs), see errata 1822, *Section 7*.

Table 19. Reset

Symbol	Parameter / Condition	Min	Typ	Max	Unit
$V_{RESETN\_THR\_High}$	Input high threshold of RESETN pin	-	-	2	V
$V_{RESETN\_THR\_Low}$	Input low threshold of RESETN pin	1	-	-	V
V_{RESETN_HYS}	Hysteresis of RESETN pin thresholds	100	150	-	mV
I_{RESETN}	Input Pull-Down current source	30	45	60	µA
t_{RESETN}	Reset detection filter time	1-	-	4	µs

Table 20. VAS under/over voltage monitoring

Symbol	Parameter / Condition	Min	Typ	Max	Unit
V_{VASU_low}	V_{AS} under voltage monitoring threshold (low voltage mode)	4.5	-	4.85	V
V_{VASU_inc}	V_{AS} under voltage monitoring threshold (increased voltage mode)	6.5	-	6.95	V
V_{VASO_low}	VAS over voltage monitoring threshold (low voltage mode)	6.5	-	6.95	V
V_{VASO_inc}	VAS over voltage monitoring threshold (increased voltage mode)	8.2	-	8.8	V
V_{VASU_off}	V_{AS} low under voltage monitoring threshold (both increased and low voltage modes) When below this threshold, V_{AS} is switched off	1	-	1.4	V
t_{VASU}	V_{AS} under/over voltage monitoring filter time	3	-	4	µs
$t_{VASblk1}$	V_{AS} under voltage switch-off blanking time (at V_{AS} activation)	-	1	-	ms
$t_{VASuoff2}$	V_{AS} automatic switch-off filter time (after V_{AS} activation)	9	-	12	µs

Table 21. Synchronous pulse amplitude monitoring

Symbol	Parameter / Condition	Min	Typ	Max	Unit
V_{Async_l}	Sync pulse amplitude under voltage monitoring threshold (if VT2_SYNCx_SEL bit is set to 0) (1)	2.4	-	2.8	V
V_{AsyncU}	Sync pulse amplitude under voltage monitoring threshold (if VT2_SYNCx_SEL bit is set to 1)	3.5	-	3.85	V
t_{Async_V}	Filter time for insufficient sync pulse amplitude	-	2	-	µs

1. The sync pulse amplitude and the diagnostic threshold voltage level are referred to the inputs of the difference amplifier, i.e. V_{Async} = V(PSIx-VAS).

Table 22. Time slot monitoring

Symbol	Parameter / Condition	Min	Typ	Max	Unit
t_{TSM}	Resolution of the time slots	-	1	-	µs
	Required register size for each time slot	-	12	-	bit

Table 23. Digital I/O

Symbol	Parameter / Condition	Min	Typ	Max	Unit
V_{in_High}	Input high threshold	-	-	2	V
V_{in_Low}	Input low threshold	0.8	-	-	V
V_{in_HYS}	Hysteresis	100	150	-	mV
I_{in_pu}	Input pull up current (pins CS, MOSI, SCLK)	-30	-45	-60	µA
I_{in_pd}	Input pull down current (pins SYNC1, SYNC2, CLKIN)	30	45	60	µA
V_{out_High}	Output high level (I_{source} = 2 mA)	V_{DD}-0.4	-	V_{DD}	V
V_{out_Low}	Output low level (I_{sink} = 2 mA)	-	-	0.4	V

Table 24. Frequency references

Symbol	Parameter / Condition	Min	Typ	Max	Unit
f_{CLK}	Internal oscillator frequency (FLL disabled)	15.2	16	16.8	MHz
f_{CLK}	Internal oscillator frequency (FLL enabled, normal CLKIN frequency)	15.84	16	16.16	MHz
$f_{CLKIN\text{-}normal}$	Normal CLKIN input frequency (1MHz or 4MHz) (Test info)	-0.5%	1 / 4	+0.5%	MHz
t_{T_CKMSK}	FLL Mask time	-	-	16	ms
t_{T_CKERD}	Clock error detection time (if FLL is enabled and CLKIN is stuck)	-	-	260	µs
$t_{reaction}$	Clock error reaction time (if bit REACTTIME=1)	-	20	-	ms

Table 24. Frequency references (continued)

Symbol	Parameter / Condition	Min	Typ	Max	Unit
f_{CLKERR_H}	High frequency error detection by FLL (clock error, FLL enabled)	17	-	21.7	MHz
f_{CLKERR_L}	Low frequency error detection by FLL (clock error, FLL enabled)	10.9	-	14	MHz

6.1 SPI interface

Figure 31. SPI communication timing diagram

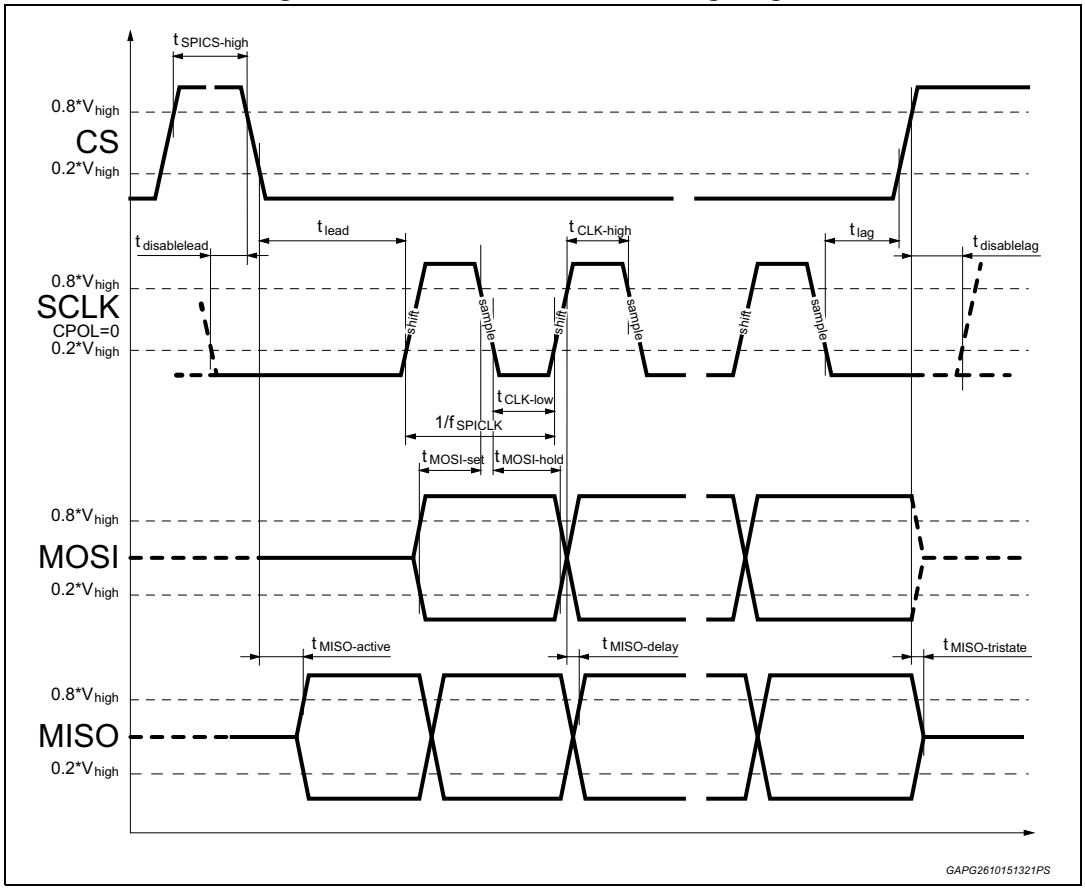


Table 25. SPI communication timing

Symbol	Parameter / Condition	Min	Typ	Max	Unit
f_{SPICLK}	SCLK frequency	-	10	-	MHz
$t_{CLK-high/low}$	SCLK high/low time	30	-	-	ns
t_{lead}	CS to SCLK delay	180	-	-	ns
t_{lag}	SCLK to CS delay	45	-	-	ns
$t_{disablelead}$	SCLK disable lead time	10	-	-	ns
$t_{disablelag}$	SCLK disable lag time	10	-	-	ns
$t_{MOSI-set}$	MOSI to SCLK delay	10	-	-	ns
$t_{MOSI-hold}$	SCLK to MOSI delay	10	-	-	ns
$t_{MISO-delay}$	SCLK to MISO delay, $C_L \leq 90$ pF	-	-	30	ns
$t_{MISO-delay}$	SCLK to MISO delay, C_L = 25 pF (Design info)	-	-	21	ns
$t_{MISO-delay}$	SCLK to MISO delay, C_L = 200 pF (Design info)	-	-	75	ns
$t_{MISO-active}$	CS to MISO active delay, $C_L \leq 90$ pF	-	-	30	ns
$t_{MISO-tristate}$	CS to MISO tristate delay, $C_L \leq 90$ pF	-	-	30	ns
$t_{SPICS-high}$	CS high time	200	-	-	ns
$I_{MISO\_tristate}$	MISO leakage current	-10	-	10	µA

Table 26. Direct interface

Symbol	Parameter / Condition	Min	Typ	Max	Unit
$V_{SYNCx-H}$	SYNCx high threshold	-	-	2	V
$V_{SYNCx-L}$	SYNCx low threshold	0.8	-	-	V
ΔV_{SYNCx}	SYNCx Hysteresis	100	150	-	mV
$t_{deglitch}$	Deglitch filter for SYNCx path	-	500	-	ns
VD_{out-L}	DOUTx Low level (Isink=2mA)	-	-	0.4	V
VD_{out-H}	DOUTx High level (Isource=2mA)	V_{DD}-0.45	-	-	V
$t_{DOUTx-delay}$	DOUTx output buffer delay, $C_L \leq 50$pF (Design info)	-	-	90	ns
-	DOUTx rising and falling edge delay difference, $C_L \leq 50$pF	-50	-	+50	ns
$t_{Latency\_DOUTx\_HF\_IIR}$	Latency time between receiving sensor data @ PSIx pin and reaching threshold high level of DOUTx pin (trigger point: 80% of PSIx modulated current, @189kBps, deglitch filter with default value).	-	-	3.05	µs

Table 26. Direct interface (continued)

Symbol	Parameter / Condition	Min	Typ	Max	Unit
$t_{Latency\_ DOUTx\_MF\_IIR}$	Latency time between receiving sensor data @ PSIx pin and reaching threshold high level of DOUTx pin (trigger point: 80% of PSIx modulated current, @125kBps or 83.3kBps, deglitch filter with default value.	-	-	3.6	µs
$t_{deglitch}$	Additional delay on DOUTx for deglitch filter configuration by SPI (DATA_FILT_SEL bits with value from “0000” to “1111”)	-	-	1	µs
$t_{Latency\_Jitter\_ DOUTx}$	Latency jitter between receiving sensor data @ PSIx pin and reaching threshold high level of DOUTx pin (trigger point: 80% of PSIx amplitude)	-	-	176	ns

7 Errata

Table 27. Errata

BugID#	Category / Function	Issue Description
1526	Asynchronous Mode	FIFO_LOCK could still stay set even after clearing of the data buffer registers of the 2 PSI5 channels. Assuming a low data rate from sensor compared to SPI readout, the proposed workaround is to read both FIFOs in the following sequence: – Ch 1, slot 6 – Ch 2, slot 6 – Ch 1, slot 5 – Ch 2, slot 5 – … – Ch 2, slot 1 Afterwards, if the FIFO_LOCK bit is still high, the following read commands are needed: – Ch 1, slot 1 – Ch 2, slot 1
1822	Sync Pulse	If the IC is configured to control the sync pulse length via pin (PSIx_EXT_UDB=0 and PSIx_TRIG_SEL=00/11, x=1 or 2) the generated sync pulse could be not compliant with the PSI5 standard, depending on the trigger pulse duration tw. – 1µs ≤ tw ≤ 5µs ≥ a short pulse is generated, PSI5 standard compliant; ≥ Correct short pulse – tw > 5µs ≥ the pulse could be not compliant with PSI5 standard, two consecutive pulses could be generated instead of a single pulse. ≥ Wrong pulse
1830	Cross coupling test	XCTRSLT1/2 fault flags are swapped in master mode
3367	Clock monitor by internal oscillator	The internal clock monitor (disabled by default) is not accurate enough: fCLKERR_H/L thresholds overlap the main oscillator operating range. This function is disabled by default, it can be enabled by ST only (burning a dedicated OTP bit). If enabled it could detect false errors. => Activation is forbidden.

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of *ECOPACK* packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

8.1 TQFP32 (7x7x1.0 mm exp. pad down) package information

Figure 32. TQFP32 (7x7x1.0 mm exp. pad down) package outline

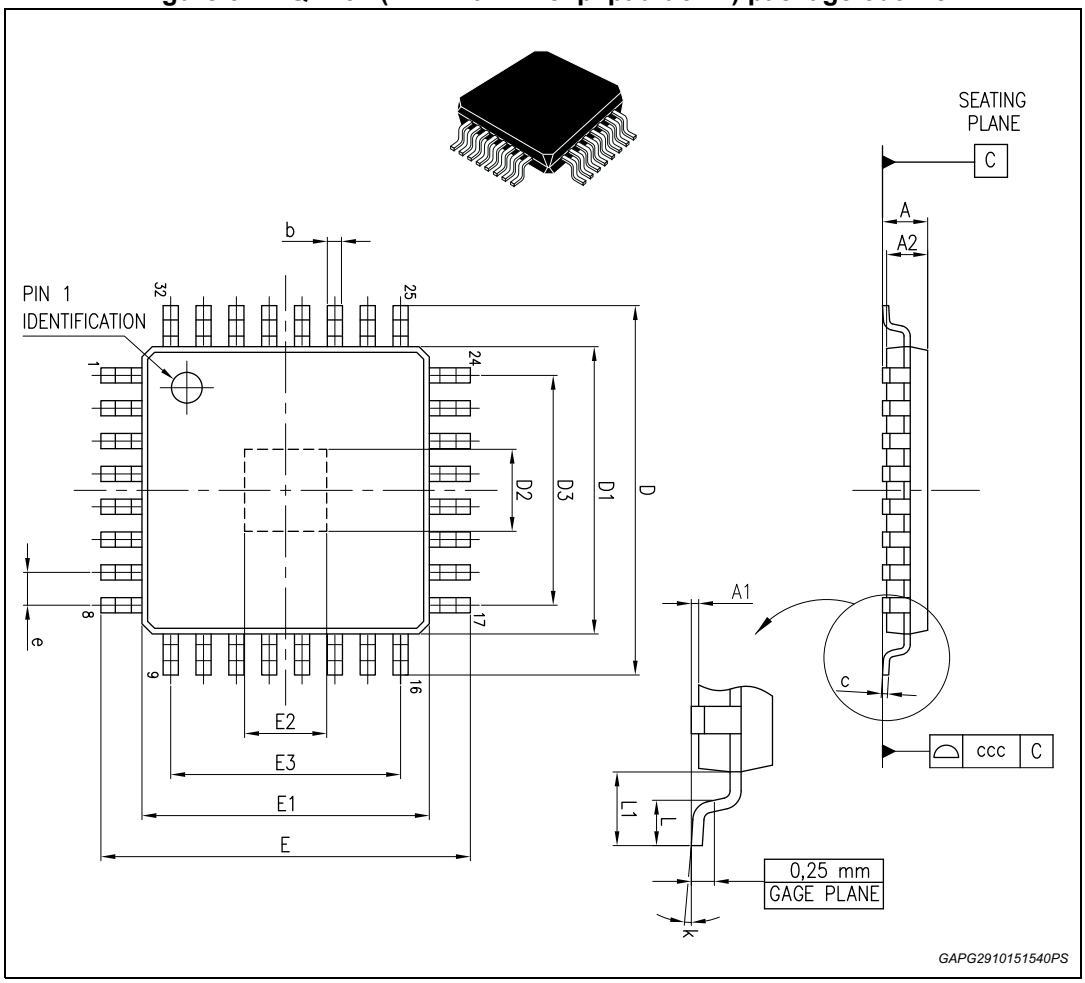


Table 28. TQFP32 (7x7x1.0 mm exp. pad down) package mechanical data

Ref	Dimensions (mm)		
	Min.	Typ.	Max.
A	-	-	1.2
A1	0.05	-	0.15
A2	0.95	1	1.05
b	0.3	0.37	0.45
c	0.09	-	0.2
D	8.8	9	9.2
D1	6.8	7	7.2
D2	2	-	-
D3	-	5.6	-
E	8.8	9	9.2
E1	6.8	7	7.2
E2	2	-	-
E3	-	5.6	-
e	-	0.8	-
L	0.45	0.6	0.75
L1	-	1	-
k	-	3.5	7
ccc	-	-	0.1

8.2 VFQFPN-28 (5x5x1.0 mm) package information

Figure 33. VFQFPN-28 (5x5x1.0 mm) package outline

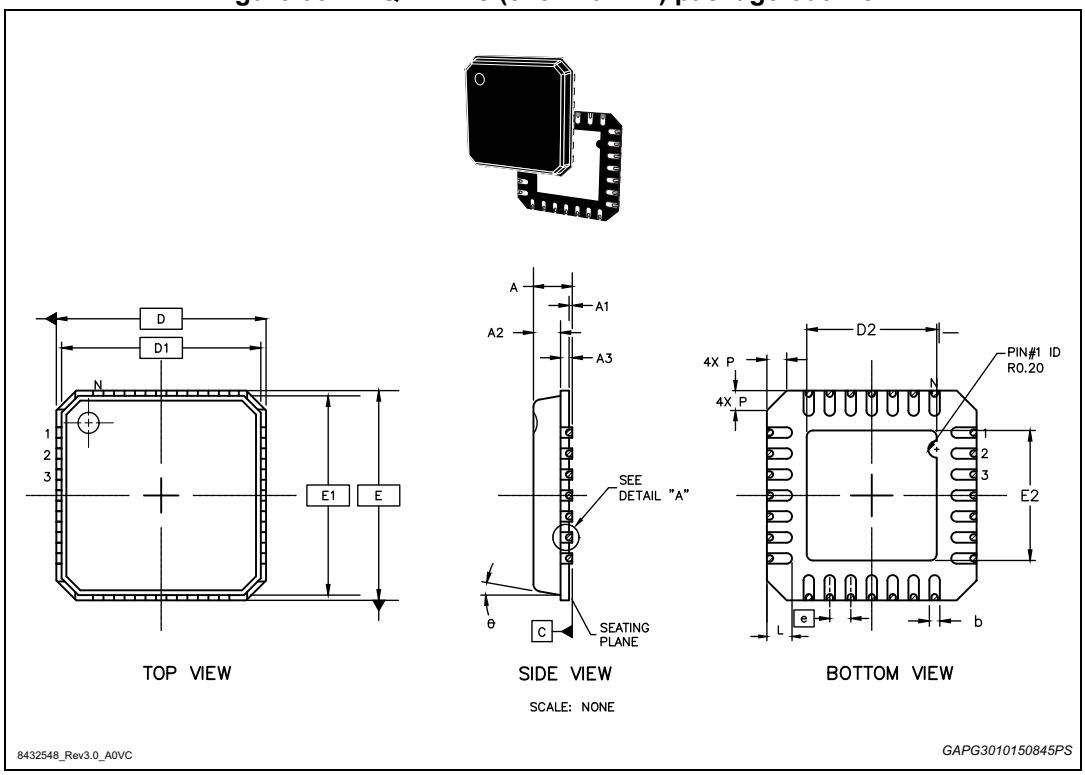


Table 29. VFQFPN-28 (5x5x1.0 mm) package mechanical data

Ref	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80	-	1.00
A1	-	0.02	0.05
A2	-	0.65	0.75
A3	-	0.20	-
b	0.18	0.25	0.3
D	5.00 (BSC)		
D1	4.75 (BSC)		
D2	3.1 (BSC)		
e	0.5 (BSC)		
E	5.00 (BSC)		
E1	4.75 (BSC)		
E2	3.1 (BSC)		
P	-	-	0.60

Table 29. VFQFPN-28 (5x5x1.0 mm) package mechanical data (continued)

Ref	Dimensions (mm)		
	Min.	Typ.	Max.
L	0.30	0.40	0.50
N	28 (pins)		

9 Revision history

Table 30. Document revision history

Date	Revision	Changes
19-Jan-2016	1	Initial release.
06-Feb-2017	2	In cover page update document title and added AECQ100 qualified in Features section. Updated: – *Section 3.5: Trigger pulse generator for synchronous pulses*; – *CH1_CR2 (PROG) on page 61*;; – *TSM1_ESn, n=1…6 (PROG) on page 65*; – *TSM1_END (PROG) on page 65*; – *CH2_CR2 (PROG) on page 68*; – *TSM2_ESn, n=1…6 (PROG) on page 72*; – *TSM2_END (PROG) on page 72*; – *ADVSET1 (PROG) on page 75*; – Corrected errors in the pargraphs '**MOSI**' and '**MISO**' in the *Section 5.2.1: Physical layer and signal description* at page 81 and 82; – *Section 5.2.4: Communication frames*; – Mininimun value of the VASSUPuv parameter on *Table 14: V_{AS} pre regulator on page 90*; – Min. and Max. value of t_{STB} and I_{XCT} parametersin *Table 16: PSI5 output supply*; – Min value of V_{Async_I} parameter in*Table 21: Synchronous pulse amplitude monitoring*; – In *Table 24: Frequency references* removed $f_{CLKMONERR\_H}$ and $f_{CLKMONERR\_L}$ parameters and updated Min and Max value of f_{CLKERR_H} and f_{CLKERR_L} parameters; – In *Table 26: Direct interface* corrected the maximum value of $t_{Latency\_Jitter\_DOUTx}$ parameter.
08-Mar-2017	3	Updated: – Feature and Description in cover page; – Registers: *NOPR*, *UDBCR*, *CH1_CR1 (PROG)*, *CH1_CR3 (PROG)*, *CH1_CR4 (PROG)*, *SID1 (PROG)*, *SID2 (PROG)*, *SID3 (PROG)*, *SID4 (PROG)*, *STRS*, *ADVSET3 (PROG)*; – *Section 5.2.1: Physical layer and signal description*; – *Table 26: Direct interface*; – *Table 27: Errata*; – *Section 8.2: VFQFPN-28 (5x5x1.0 mm) package information on page 102*.
21-Mar-2019	4	Updated: – *CH1_CR4 (PROG)*; – *Section 5.2.4: Communication frames*.
09-Jul-2019	5	Minor text changes in *Section 5.2.3: Frame definition*