L9691

Datasheet

Automotive chip for advanced airbag applications

TQFP128 exposed pad down
(14x14x1.0 mm)

Product status link
L9691

Product summary		
Order code	Package	Packing
L9691-TR	TQFP128EP 14x14x1.0 mm	Tape and reel

Features

- AEC-Q100 qualified
- Single chip and master/slave configurations
- Boost regulator for energy reserve
  - 2 MHz operation
  - Output voltage 24 V/33 V ±6%, user-selectable, peak inductor current regulation
  - Capacitor value and ESR diagnostics
- Boost regulator for low voltage system operation
  - 2 MHz operation
  - Output voltage, 10 V ±8%, 870 mA max
- Buck regulator for remote sensor
  - 2 MHz operation
  - Output voltage, 6.5 V/8 V ±4%, 700 mA max
- Buck regulator for micro controller unit
  - 2 MHz operation
  - Output voltage, 3.3 V ±3%, 450 mA max
- Remote sensor interface and SYNC pulse supply voltage inputs and monitorings
- Linear regulator with external power PNP transistor, 5 V ±5%, 135 mA max
- Integrated energy reserve crossover switch with switch active output indicator, configured as input for slave mode operation
- Battery voltage monitor and shutdown with wake-up control
- System voltage diagnostics with integrated ADCs
- Squib/LEA deployment drivers
  - 16 channel HSD/LSD for squib load
  - 2 over 16 channels supporting LEA load
  - 2 channel couples supporting common-return connection
  - 18 V deployment voltage
  - Low, high and automatic dynamic deployment current profiles
  - R measure, STB, STG and leakage diagnostics
  - High and low side driver FET tests
  - LEA presence diagnostics
- Two isolated high side safing FET regulators and diagnostics
- Eight channel PSI-5 v2.3 remote sensor interface
- Three channel general purpose low side drivers with 0-100% PWM control
- Twelve channel hall-effect, resistive or switch sensor interface
- User-programmable safing logic and rolling average algorithm
- E2E arming procedure through global SPI
- Temporal watchdog timer
- End-of-life disposal interface
- Temperature sensor
- 32 bit global SPI bus interface

- 32 bit remote sensor SPI bus interface, SafeSPI v1.0 compatible
- LIN v2.2A interface with OCS message decoding capability
- 5.4 V min operating voltage at VIN battery input for start-up
- Full ISO 26262 compliant, ASIL-D systems ready
- Packaging 128 pin

Description

The L9691 is an advanced airbag system chip solution targeted for the global airbag market.

High frequency power supply design optimizes system cost by using smaller and less expensive external components. All switching regulators operate at 2 MHz and all buck converters have integrated synchronous rectifiers.

The reserve capacitor is electrically isolated from the boost regulator by integrated switches and external resistors, controlling in-rush current. A capacitor discharge switch is integrated to discharge the capacitor at shutdown.

Low quiescent current permits the device to be directly connected to battery. In this mode, device start-up and shutdown are controlled through the wake-up input pin (actually, shutdown needs also dedicated SPI command too). The power supply and crossover function are controlled automatically through the internal state machine.

For systems with high feature content, two L9691 devices can be used in a master/slave configuration.

The L9691 provides two fully isolated deployment voltage regulators, using the external safing FETs as power elements in the regulator loop. Deployment voltage is set to a nominal 18 V value to further optimize system cost.

Integrated safing logic uses a rolling average algorithm and decodes all sensor information within the system remote sensor SPI bus. Number of samples and thresholds are user-programmable. An alternative safing function permits arming from an external source through the global SPI bus (E2E communication).

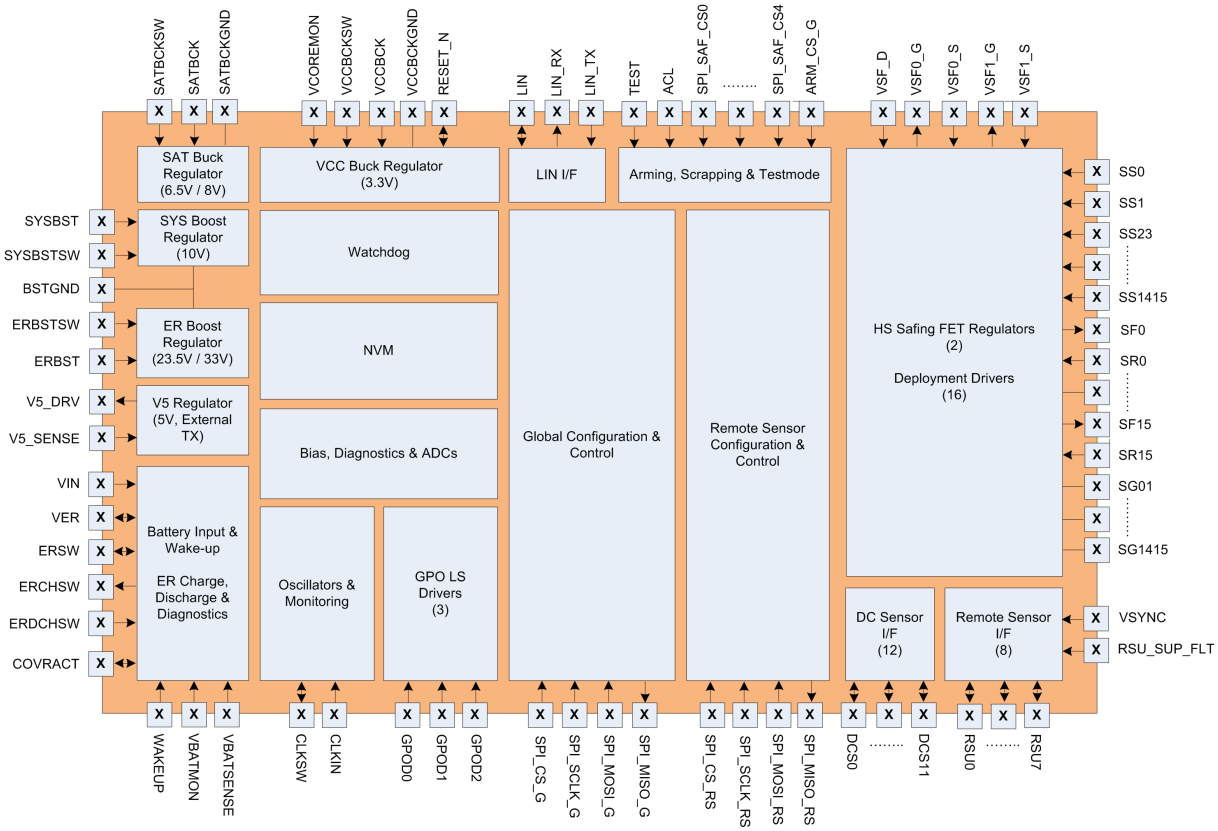
Dual SPI interfaces separate device global functions and remote sensors. LIN interface is available, providing OCS message decoding for passenger loop inhibition.

1 Block diagram and pin description

1.1 Block diagram

The L9691 IC is an application specific standard component for airbag system chip. Its main functions include power management, deployment drivers (supporting both squib and low-energy actuator loads), deployment voltage regulators, remote sensor interfaces (supporting PSI-5 satellite sensors), diagnostics, deployment arming, hall-effect/switch sensor interfaces, general purpose output low-side drivers, watchdog, LIN interface. A simplified block diagram for this IC is shown in the Figure 1.

Figure 1. Block diagram



1.2 Pin description

Figure 2. **Device pinout**

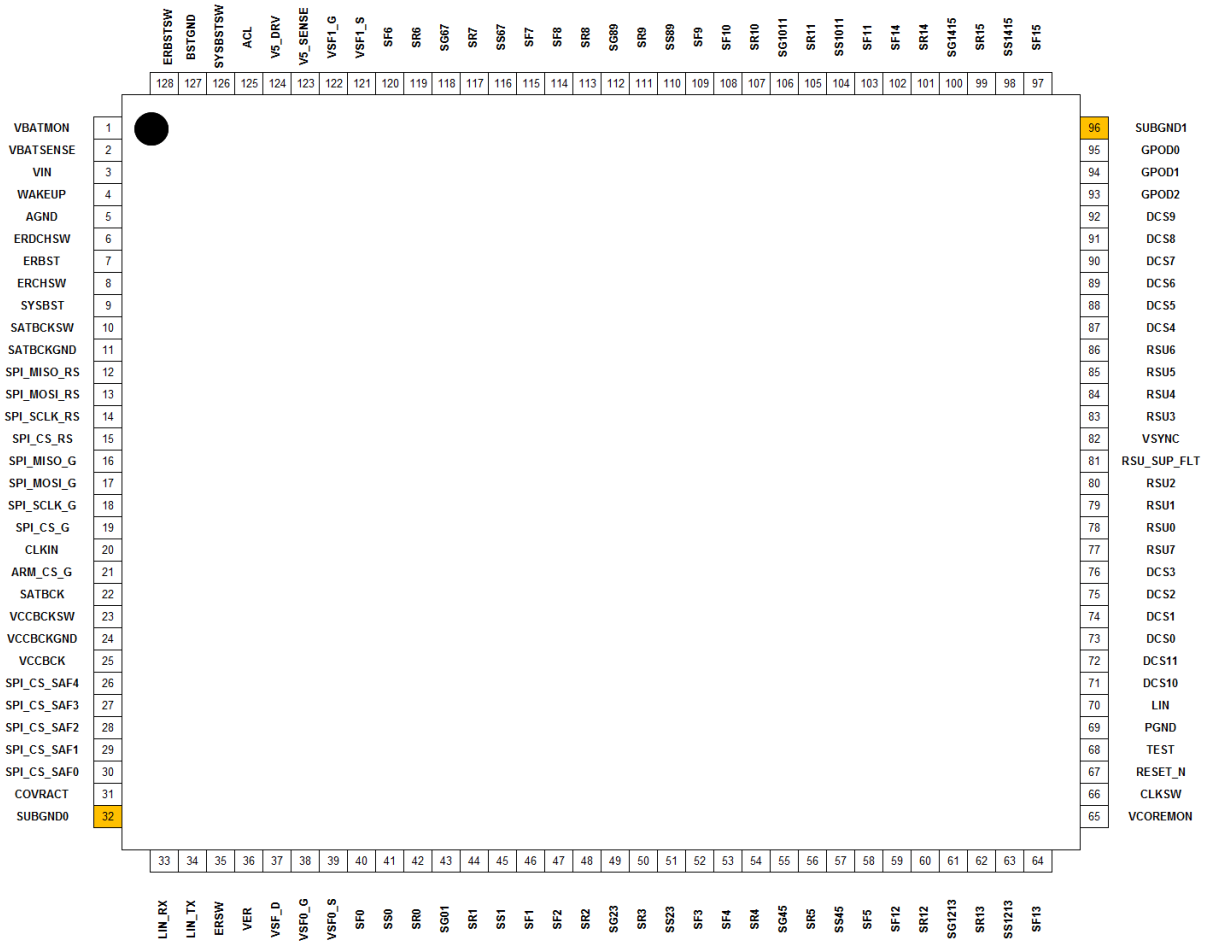


Table 1. **Pin function**

Pin #	Pin name	Description	I/O type	Class
1	VBATMON	Battery monitor for wake up	I	Global
2	VBATSENSE	Battery sense input	I	Global
3	VIN	Battery input voltage	S	Global
4	WAKEUP	Wake-up control input	I	Global
5	AGND	Analog ground	S	Local
6	ERDCHSW	Energy reserve discharge path	O	Local
7	ERBST	Energy reserve boost output voltage	S	Local
8	ERCHSW	Energy reserve charge path	O	Local
9	SYSBST	System boost output voltage	S	Local
10	SATBCKSW	Satellite buck switching output	O	Local
11	SATBCKGND	Satellite buck ground	S	Local
12	SPI_MISO_RS	Remote sensor SPI data out/snooping input	I/O	Local
13	SPI_MOSI_RS	Remote sensor SPI data in	I	Local

Pin #	Pin name	Description	I/O type	Class
14	SPI_SCLK_RS	Remote sensor SPI clock	I	Local
15	SPI_CS_RS	Remote sensor SPI chip select	I	Local
16	CLKIN	External clock input	I	Local
17	SPI_MOSI_G	Global SPI data in	I	Local
18	SPI_SCLK_G	Global SPI clock	I	Local
19	SPI_CS_G	Global SPI chip select	I	Local
20	SPI_MISO_G	Global SPI data out/snooping input	I/O	Local
21	ARM_CS_G	Arm status capture input (on global SPI)	I	Local
22	SATBCK	Satellite buck output voltage	S	Local
23	VCCBCKSW	VCC buck switching output	O	Local
24	VCCBCKGND	VCC buck ground	S	Local
25	VCCBCK	VCC buck output voltage	S	Local
26	SPI_CS_SAF4	SPI safing sensor chip select 4	I	Local
27	SPI_CS_SAF3	SPI safing sensor chip select 3	I	Local
28	SPI_CS_SAF2	SPI safing sensor chip select 2	I	Local
29	SPI_CS_SAF1	SPI safing sensor chip select 1	I	Local
30	SPI_CS_SAF0	SPI safing sensor chip select 0	I	Local
31	COVRACT	Crossover switch control input/output	I/O	Local
32	SUBGND0	Substrate ground 0 (fused with lead frame)	S	Local
33	LIN_RX	LIN bus receive data out	I/O	Local
34	LIN_TX	LIN bus transmit data in	I	Local
35	VER	Energy reserve voltage	I	Local
36	ERSW	Energy reserve switch input/output	I/O	Local
37	VSF_D	Safing FET drain sense/force	O	Local
38	VSF0_G	Safing FET regulator 0 gate output	O	Local
39	VSF0_S	Safing FET regulator 0 source input	I	Local
40	SF0	Squib high-side channel 0	O	Global
41	SS0	Squib high-side supply channel 0	S	Local
42	SR0	Squib low-side channel 0	O	Global
43	SG01	Squib low-side ground channel 0 and 1	S	Local
44	SR1	Squib low-side channel 1	O	Global
45	SS1	Squib high-side supply channel 1	S	Local
46	SF1	Squib high-side channel 1	O	Global
47	SF2	Squib high-side channel 2	O	Global
48	SR2	Squib low-side channel 2	O	Global
49	SG23	Squib low-side ground channel 2 and 3	S	Local
50	SR3	Squib low-side channel 3	O	Global
51	SS23	Squib high-side supply channel 2 and 3	S	Local
52	SF3	Squib high-side channel 3	O	Global
53	SF4	Squib high-side channel 4	O	Global
54	SR4	Squib low-side channel 4	O	Global

Pin #	Pin name	Description	I/O type	Class
55	SG45	Squib low-side ground channel 4 and 5	S	Local
56	SR5	Squib low-side channel 5	O	Global
57	SS45	Squib high-side supply channel 4 and 5	S	Local
58	SF5	Squib high-side channel 5	O	Global
59	SF12	Squib high-side channel 12	O	Global
60	SR12	Squib low-side channel 12	O	Global
61	SG1213	Squib low-side ground channel 12 and 13	S	Local
62	SR13	Squib low-side channel 13	O	Global
63	SS1213	Squib high-side supply channel 12 and 13	S	Local
64	SF13	Squib high-side channel 13	O	Global
65	VCOREMON	MCU core voltage monitoring input	I	Local
66	CLKSW	Switching regulator sync input/output	I/O	Local
67	RESET_N	Reset input/output	I/O	Local
68	TEST	Test-mode, watchdog disable input and ISRC check	I/O	Local
69	PGND	Power ground for LIN, GPOs and RSU	S	Local
70	LIN	LIN bus	I/O	Global
71	DCS10	DC sensor interface channel 10	O	Global
72	DCS11	DC sensor interface channel 11	O	Global
73	DCS0	DC sensor interface channel 0	O	Global
74	DCS1	DC sensor interface channel 1	O	Global
75	DCS2	DC sensor interface channel 2	O	Global
76	DCS3	DC sensor interface channel 3	O	Global
77	RSU7	Remote sensor interface channel 7	O	Global
78	RSU0	Remote sensor interface channel 0	O	Global
79	RSU1	Remote sensor interface channel 1	O	Global
80	RSU2	Remote sensor interface channel 2	O	Global
81	RSU_SUP_FLT	RSU filtered supply input	S	Local
82	VSYNC	RSU SYNC pulse supply input	S	Local
83	RSU3	Remote sensor interface channel 3	O	Global
84	RSU4	Remote sensor interface channel 4	O	Global
85	RSU5	Remote sensor interface channel 5	O	Global
86	RSU6	Remote sensor interface channel 6	O	Global
87	DCS4	DC sensor interface channel 4	O	Global
88	DCS5	DC sensor interface channel 5	O	Global
89	DCS6	DC sensor interface channel 6	O	Global
90	DCS7	DC sensor interface channel 7	O	Global
91	DCS8	DC sensor interface channel 8	O	Global
92	DCS9	DC sensor interface channel 9	O	Global
93	GPOD2	General purpose drain output channel 2	O	Global
94	GPOD1	General purpose drain output channel 1	O	Global
95	GPOD0	General purpose drain output channel 0	O	Global

Pin #	Pin name	Description	I/O type	Class
96	SUBGND1	Substrate ground 1 (fused with lead frame)	S	Local
97	SF15	Squib high-side channel 15	O	Global
98	SS1415	Squib high-side supply channel 14 and 15	S	Local
99	SR15	Squib low-side channel 15	O	Global
100	SG1415	Squib low-side ground channel 14 and 15	S	Local
101	SR14	Squib low-side channel 14	O	Global
102	SF14	Squib high-side channel 14	O	Global
103	SF11	Squib high-side channel 11	O	Global
104	SS1011	Squib high-side supply channel 10 and 11	S	Local
105	SR11	Squib low-side channel 11	O	Global
106	SG1011	Squib low-side ground channel 10 and 11	S	Local
107	SR10	Squib low-side channel 10	O	Global
108	SF10	Squib high-side channel 10	O	Global
109	SF9	Squib high-side channel 9	O	Global
110	SS89	Squib high-side supply channel 8 and 9	S	Local
111	SR9	Squib low-side channel 9	O	Global
112	SG89	Squib low-side ground channel 8 and 9	S	Local
113	SR8	Squib low-side channel 8	O	Global
114	SF8	Squib high-side channel 8	O	Global
115	SF7	Squib/LEA high-side channel 7	O	Global
116	SS67	Squib/LEA high-side supply channel 6 and 7	S	Local
117	SR7	Squib/LEA low-side channel 7	O	Global
118	SG67	Squib/LEA low-side ground channel 6 and 7	S	Local
119	SR6	Squib/LEA low-side channel 6	O	Global
120	SF6	Squib/LEA high-side channel 6	O	Global
121	VSF1_S	Safing FET regulator 1 source input	I	Local
122	VSF1_G	Safing FET regulator 1 gate output	O	Local
123	V5_SENSE	V5 regulator sense input	I	Local
124	V5_DRV	V5 regulator drive output	O	Local
125	ACL	End-of-life disposal control input	I	Global
126	SYSBSTSW	System boost switching output	O	Local
127	BSTGND	Boost regulator ground	S	Local
128	ERBSTSW	Energy reserve boost switching output	O	Local
-	Ex Pad Down	Substrate ground (backside)	S	Local

Legend: I = Input, O = Output, I/O = Input/Output, S = Supply or ground

2 Maximum ratings

2.1 Absolute maximum ratings

Maximum ratings are absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit.

All voltages are related to the potential at substrate ground (SUBGND0 and SUBGND1).

Table 2. Absolute maximum ratings

Symbol	Parameter	Min	Typ	Max	Unit
VBATMON	Battery monitor for wake up	-18(1)	-	40	V
VBATSENSE	Battery sense input	-18(1)	-	40	V
VIN	Battery input voltage	-1(2)	-	40	V
WAKEUP	Wake-up control input	-1	-	40	V
ERDCHSW	Energy reserve discharge path	-0.3	-	40	V
ERCHSW	Energy reserve charge path	-0.3	-	40	V
ERBST	Energy reserve boost output voltage	-0.3	-	40	V
AGND	Analog ground	-0.3	-	0.3	V
SYSBST	System boost output voltage	-0.3	-	40	V
SATBCKSW	Satellite buck switching output	-0.3	-	40	V
SATBCKGND	Satellite buck ground	-0.3	-	0.3	V
SPI_MISO_RS	Remote sensor SPI data out/snooping input	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
SPI_MOSI_RS	Remote sensor SPI data in	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
SPI_SCLK_RS	Remote sensor SPI clock	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
SPI_CS_RS	Remote sensor SPI chip select	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
SPI_MISO_G	Global SPI data out/snooping input	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
SPI_MOSI_G	Global SPI data in	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
SPI_SCLK_G	Global SPI clock	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
SPI_CS_G	Global SPI chip select	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
CLKIN	External clock input	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
ARM_CS_G	Arm status capture input (on global SPI)	-0.3	-	20(3)	V
SATBCK	Satellite buck output voltage	-0.3	-	20	V
VCCBCKSW	VCC buck switching output	-0.3	-	20	V
VCCBCKGND	VCC buck ground	-0.3	-	0.3	V
VCCBCK	VCC buck output voltage	-0.3	-	4.6	V
SPI_CS_SAF4	SPI safing sensor chip select 4	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
SPI_CS_SAF3	SPI safing sensor chip select 3	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
SPI_CS_SAF2	SPI safing sensor chip select 2	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
SPI_CS_SAF1	SPI safing sensor chip select 1	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
SPI_CS_SAF0	SPI safing sensor chip select 0	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
COVRACT	Crossover switch control input/ouput	-0.3	-	min (VCCBCK + 0.3, 4.6)	V

Symbol	Parameter	Min	Typ	Max	Unit
SUBGND0	Substrate ground 0 (fused with lead frame)	-0.3	-	0.3	V
LIN_RX	LIN bus receive data out	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
LIN_TX	LIN bus transmit data in	-0.3	-	40	V
ERSW	Crossover switch output	-0.3	-	40	V
VER	Energy reserve voltage	-0.3	-	40	V
VSF_D	Safing FET drain sense/force	-0.3	-	40	V
VSF0_G	Safing FET regulator 0 gate output	-0.3	-	40	V
VSF0_S	Safing FET regulator 0 source input	-0.3	-	40	V
SF0	Squib high-side channel 0	-1[4]	-	40	V
SS0	Squib high-side supply channel 0	-0.3	-	40	V
SR0	Squib low-side channel 0	-0.3	-	35	V
SG01	Squib low-side ground channel 0 and 1	-0.3	-	0.3	V
SR1	Squib low-side channel 1	-0.3	-	35	V
SS1	Squib high-side supply channel 1	-0.3	-	40	V
SF1	Squib high-side channel 1	-1[4]	-	40	V
SF2	Squib high-side channel 2	-1[4]	-	40	V
SR2	Squib low-side channel 2	-0.3	-	35	V
SG23	Squib low-side ground channel 2 and 3	-0.3	-	0.3	V
SR3	Squib low-side channel 3	-0.3	-	35	V
SS23	Squib high-side supply channel 2 and 3	-0.3	-	40	V
SF3	Squib high-side channel 3	-1[4]	-	40	V
SF4	Squib high-side channel 4	-1[4]	-	40	V
SR4	Squib low-side channel 4	-0.3	-	35	V
SG45	Squib low-side ground channel 4 and 5	-0.3	-	0.3	V
SR5	Squib low-side channel 5	-0.3	-	35	V
SS45	Squib high-side supply channel 4 and 5	-0.3	-	40	V
SF5	Squib high-side channel 5	-1[4]	-	40	V
SF6	Squib/LEA high-side channel 6	-1[4]	-	40	V
SR6	Squib/LEA low-side channel 6	-0.3	-	35	V
SG67	Squib/LEA low-side ground channel 6 and 7	-0.3	-	0.3	V
SR7	Squib/LEA low-side channel 7	-0.3	-	35	V
SS67	Squib/LEA high-side supply channel 6 and 7	-0.3	-	40	V
SF7	Squib/LEA high-side channel 7	-1[4]	-	40	V
VCOREMON	MCU core voltage monitoring input	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
CLKSW	Switching regulator sync input/output	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
RESET_N	Reset input/output	-0.3	-	min (VCCBCK + 0.3, 4.6)	V
TEST	Test-mode, watchdog disable input and ISRC check	-0.3	-	40	V
PGND	Power ground for LIN, GPOs and RSU	-0.3	-	0.3	V
LIN	LIN bus	-27[5]	-	40	V
DCS0	DC sensor interface channel 0	-2	-	40	V

Symbol	Parameter	Min	Typ	Max	Unit
DCS1	DC sensor interface channel 1	-2	-	40	V
DCS2	DC sensor interface channel 2	-2	-	40	V
DCS3	DC sensor interface channel 3	-2	-	40	V
DCS4	DC sensor interface channel 4	-2	-	40	V
DCS5	DC sensor interface channel 5	-2	-	40	V
RSU0	Remote sensor interface channel 0	-1	-	40	V
RSU1	Remote sensor interface channel 1	-1	-	40	V
RSU2	Remote sensor interface channel 2	-1	-	40	V
RSU3	Remote sensor interface channel 3	-1	-	40	V
RSU_SUP_FLT	RSU filtered supply input	-0.3	-	40	V
VSYNC	RSU SYNC pulse supply input	-0.3	-	40	V
RSU4	Remote sensor interface channel 4	-1	-	40	V
RSU5	Remote sensor interface channel 5	-1	-	40	V
RSU6	Remote sensor interface channel 6	-1	-	40	V
RSU7	Remote sensor interface channel 7	-1	-	40	V
DCS6	DC sensor interface channel 6	-2	-	40	V
DCS7	DC sensor interface channel 7	-2	-	40	V
DCS8	DC sensor interface channel 8	-2	-	40	V
DCS9	DC sensor interface channel 9	-2	-	40	V
DCS10	DC sensor interface channel 10	-2	-	40	V
DCS11	DC sensor interface channel 11	-2	-	40	V
GPOD2	General purpose drain output channel 2	-1	-	40	V
GPOD1	General purpose drain output channel 1	-1	-	40	V
GPOD0	General purpose drain output channel 0	-1	-	40	V
SUBGND1	Substrate ground 1 (fused with lead frame)	-0.3	-	0.3	V
SF15	Squib high-side channel 15	-1[(4)]	-	40	V
SS1415	Squib high-side supply channel 14 and 15	-0.3	-	40	V
SR15	Squib low-side channel 15	-0.3	-	35	V
SG1415	Squib low-side ground channel 14 and 15	-0.3	-	0.3	V
SR14	Squib low-side channel 14	-0.3	-	35	V
SF14	Squib high-side channel 14	-1[(4)]	-	40	V
SF13	Squib high-side channel 13	-1[(4)]	-	40	V
SS1213	Squib high-side supply channel 12 and 13	-0.3	-	40	V
SR13	Squib low-side channel 13	-0.3	-	35	V
SG1213	Squib low-side ground channel 12 and 13	-0.3	-	0.3	V
SR12	Squib low-side channel 12	-0.3	-	35	V
SF12	Squib high-side channel 12	-1[(4)]	-	40	V
SF11	Squib high-side channel 11	-1[(4)]	-	40	V
SS1011	Squib high-side supply channel 10 and 11	-0.3	-	40	V
SR11	Squib low-side channel 11	-0.3	-	35	V

Symbol	Parameter	Min	Typ	Max	Unit
SG1011	Squib low-side ground channel 10 and 11	-0.3	-	0.3	V
SR10	Squib low-side channel 10	-0.3	-	35	V
SF10	Squib high-side channel 10	-1(4)	-	40	V
SF9	Squib high-side channel 9	-1(4)	-	40	V
SS89	Squib high-side supply channel 8 and 9	-0.3	-	40	V
SR9	Squib low-side channel 9	-0.3	-	35	V
SG89	Squib low-side ground channel 8 and 9	-0.3	-	0.3	V
SR8	Squib low-side channel 8	-0.3	-	35	V
SF8	Squib high-side channel 8	-1(4)	-	40	V
VSF1_S	Safing FET regulator 1 source input	-0.3	-	40	V
VSF1_G	Safing FET regulator 1 gate output	-0.3	-	40	V
V5_SENSE	V5 regulator sense input	-0.3	-	40	V
V5_DRV	V5 regulator drive output	-0.3	-	40	V
ACL	End-of-life disposal control input	-0.3	-	40(6)	V
SYSBSTSW	System boost switching output	-0.3	-	40	V
BSTGND	Boost regulator ground	-0.3	-	0.3	V
ERBSTSW	Energy reserve boost switching output	-0.3	-	40	V
Ex Pad Down	Substrate ground (backside)	-0.3	-	0.3	V

1. *Or 20 mA for 10 ms during transient.*
2. *Valid in transient conditions only.*
3. *Set at 20 V for pin FMEA constraints.*
4. *In the case of deployment turn off the transient voltages on SS and SF pins can move away from each other until a maximum voltage of SS-SF < 45 V for a limited transient time (6.5 µs maximum) with no damage on device. Additionally in this time transient, in worst case load condition (maximum load inductance 56 µH) the peak energy that can be handled by the ESD protection on SF pin is 128 µJ within a maximum time of 6.5 µs.*
5. *Valid for T_J > 27 deg, otherwise -18 V.*
6. *Set at 40 V for pin FMEA constraints.*

2.2 ESD protection

Table 3. ESD protection

Symbol	Parameter	Min	Typ	Max	Unit
All pins	HBM	-2	-	2	kV
All pins	CDM (values for corner pins in brackets)	-500/(-750)	-	500/(750)	V
Global pins (except LIN)	HBM	-4	-	4	kV
LIN pin	HBM	-6	-	6	kV

2.3 Temperature ranges and thermal data

Table 4. Temperature ranges and thermal data

Symbol	Parameter	Min	Max	Unit
T_{AMB}	Operating temperature (ECU environment)	-40	105	°C
T_J	Operating junction temperature	-40	175	°C
T_{STG}	Storage temperature	-55	150	°C
$R_{TH\_J\_CASE}$	Thermal resistance junction to case	-	2	°C/W

3 Device overview

3.1 Main features

- Capability to operate in dual-chip mode in master/slave configuration, user-selectable via NVM programming
- Internal 16 MHz oscillator for timing generation
- Internal 10 MHz oscillator for monitoring
- Dedicated CLKIN pin to provide an external 4 MHz clock, 1% accurate, to improve timing accuracy (by FLL circuitry)
- Dedicated CLKSW pin to optimize switching regulator operation phases between master and slave devices (output when master, input when slave)
- Phase configuration for switching regulators time base, user-programmable via Global SPI
- Integrated temporal watchdog control
- RESET_N reset input/output pin (output with pull-up and pull-down capability when master, input with pull-down capability when slave)
- Internal NVM, used for trimming and device configuration, user-programmable via Global SPI

3.2 SPI interface

- One dedicated 32-bit SPI bus for global configuration and control
- One dedicated 32-bit SPI bus for remote sensor configuration and control, SafeSPI v1.0 compatible

3.3 Power supply and energy reserve management

- Integrated 2 MHz SYS boost regulator, 10 V ±8% nominal output
- Integrated 2 MHz energy reserve boost regulator, 33 V ±6% or 23.5 V ±6% nominal output, user-selectable via Global SPI
- Integrated energy reserve capacitor charge current-limited switch
- Integrated energy reserve capacitor discharge overcurrent-protected switch
- Integrated energy reserve crossover current-limited switch
- Crossover switch “active” signal (output when master, input when slave)
- Integrated 2 MHz synchronous SAT buck regulator, 8 V ±4% or 6.5 V ±4% nominal output, user-selectable via NVM programming
- Integrated 2 MHz synchronous VCC buck regulator, 3.3 V ±3% nominal output; 50% fixed duty-cycle mode (FDM), selectable via NVM programming
- External microcontroller core supply voltage monitoring (VCOREMON), user-selectable via NVM programming
- V5 linear regulator with external power PNP transistor, 5 V ±5% nominal output; possibility to disable via NVM programming
- Switching frequency selection via Global SPI
- Over and undervoltage status monitorings
- Open feedback diagnostic on VCC buck and V5 linear regulators
- Switching regulator ground loss detection and shutdown
- Boost external diode loss detection and voltage clamping
- Overtemperature detection and shutdown on all switching regulators, ER crossover switch and ER charge switch
- Energy reserve diagnostics, capacitor value and ESR

3.4 Safing FET regulator and diagnostics

- Dual integrated 18 V linear regulators for high-side safing FET source voltage, enabled via arming logic
- Safing FET connection integrity diagnostics
- Battery and energy reserve diode integrity diagnostics

3.5 Deployment drivers and diagnostics

- 16 high-side deployment drivers, 16 low side deployment drivers
- Low-energy actuator (LEA) support available on 2 channels (6 and 7)
- Common-return (CSRx) connection support available on 2 channel couples (2-3 and 4-5)
- Independently controlled high-side and low-side FETs
- User-programmable deployment options
  - Low current: 1.21 A minimum
  - High current: 1.76 A minimum
  - Programmable dwell time in 16 µs increments
  - Automatic dynamic deployment current profile
- Configurable deployment current monitor feature
- Deployment interruption in case of high-side short to ground and/or supply overvoltage
- Squib/LEA resistance measurement
- High and low-side FET tests
- Open and shorts diagnostics, including between loop drivers
- LEA diode presence/integrity diagnostics

3.6 Remote sensor interfaces

- 8 channel receiver, PSI-5 v2.3 compatible with SYNC pulse
- Dedicated supply input pins for both satellite and SYNC pulse operation
- Current limit with short circuit protection diagnostics
- Auto-adjusting current trip points for each channel
- Satellite data with parity and CRC, 10 bit, 16 bit and 20 bit messages, 125 k or 189 kbps
- Satellite message error detection

3.7 DC sensor interfaces

- 12 integrated interfaces with current sense capability
- Compatible with hall-effect, resistive and switch sensors
- Capability to perform 2 simultaneous measurements on two different channels (0-1-2-3-10-11 and 4-5-6-7-8-9 grouping)
- Current limit protected output
- Capability to inhibit passenger airbag loops via monitoring of 2 DC sensor channels (0 and 1)

3.8 LIN interface and decoder

- LIN specification v2.2A compliance and K-LINE ISO9141 compatibility
- Configurable integrated communication decoder for OCS message monitoring and passenger airbag loop inhibition

3.9 Arming logic

- User-configurable safing algorithms with 22 safing records
- 5 independent chip-select inputs for external sensor interface SPI snooping
- Independent chip-select input for master/slave device arming status SPI snooping (in master/slave configuration)
- Independent user-programmable thresholds
- Independent user-programmable latch timers
- 8 discrete and independent internal arming signals
- 8 discrete and independent arming result outputs
- Capability to receive arming request from global SPI communication using E2E protocol
- End-of-life interface

3.10 Passenger inhibit logic

- Passenger loop inhibition via internal monitoring of DC sensors and LIN OCS communication
- Capability to snoop master/slave device passenger inhibit status on global SPI (in master/slave configuration)
- Capability to snoop alternative microcontroller passenger inhibit status on global SPI

3.11 General purpose low-side outputs

- 3 low-side drivers
- ON-OFF mode and PWM 0-100% fine control
- Diagnostics for short circuit protection and open load detection
- Current limit protected

3.12 A/D converters

- One A/D converter dedicated to power-supply voltage and die average temperature monitoring, providing a 10 bit conversion via global SPI and with the capability to handle a queue of 4 conversion requests
- 2 A/D converters used to perform ER capacitor value (14 bit conversion, global SPI) and ESR (13 bit conversion, global SPI) measurement diagnostic
- One A/D converter dedicated to deployment and safing FET regulator circuitry voltage monitoring, providing a 10 bit conversion via global SPI and with the capability to handle one conversion request per time
- One A/D converter dedicated to deployment leakage current diagnostic, providing a 10 bit conversion of the measured leakage current via global SPI; this current A/D converter is shared among all 16 deployment channels
- 8 A/D converters dedicated to remote sensor interfaces, providing a 10 bit conversion of the sensor current value and used for sensor communication decoding; each RSU channel have a dedicated current A/D converter
- 2 A/D converters dedicated to DC sensor interfaces, one providing the voltage value (10 bit conversion) and the other one providing the current value (10 bit conversion); the 2 A/D converters are shared among all 12 DC sensor channels. Conversions are provided via global SPI, with the capability to handle a queue of 4 conversion requests; channel 0 and 1 voltage/current conversions can also be used internally by the passenger airbag inhibit feature

4 Main features

4.1 Power supply and power mode control

Power supply and power mode control section provides all voltage supplies which are required for a high feature airbag system; in order to provide a higher level of flexibility, two applicative scenarios are supported:

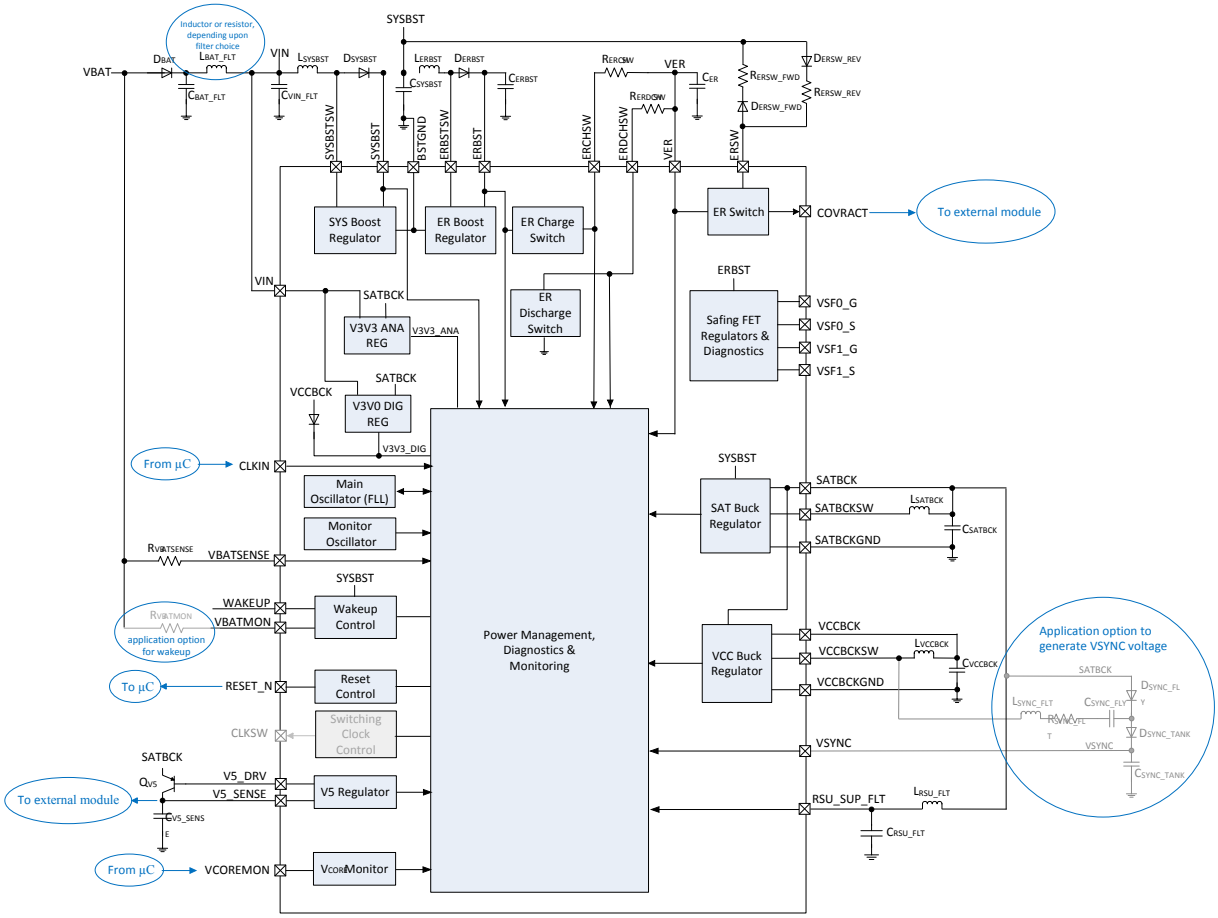
- Single-chip/master-only: only one system basis device is mounted on the ECU, providing power to all the external units, including additional expansion devices.
- Dual-chip/master-slave: two system basis devices are mounted on the ECU; this allows to double the overall power driving capability and to balance power dissipation between the 2 devices. By the way, from power mode control point of view, one of the 2 devices has to be configured as “master”, while the other has to be configured as “slave”: “master” device defines the power mode state of the “slave”, in particular when reset release and transition to energy reserve supply usage is decided (ER state).

In dual-chip scenario, there is no support for regulator double-driving output configurations: as an example, even if there are 2 buck regulators for microcontroller supply (one in the master, the other in the slave), the 2 outputs should not be connected to the same load, as there is no implemented mechanism to balance the 2 regulator output currents. Information that device is configured as master or slave is given via NVM programming; in single-chip scenario, device must be configured as master. “Master” is the default configuration setting.

4.1.1 Single chip/master-only scenario

A general block diagram of a typical single chip/master-only application scenario is shown in Figure 3.

Figure 3. Single chip/master-only block diagram



Here is a short description of the available features:

- Battery input pin (VIN): protected battery input, i.e. after reverse battery protection diode (D_{BAT}) and filter (L_{BAT_FLT} and C_{BAT_FLT}); its voltage is monitored to determine device power-up/down.
- Device wakeup input pin (WAKEUP): main source to trigger device power-up/down, whose operating range is compatible with protected battery voltage (VIN).
- Redundant device wakeup input pin (VBATMON): secondary source to trigger device power-up/down, whose operating range is compatible with unprotected battery voltage (VBAT); in standard application scenario, it can be connected to VBAT line through and external resistor ($R_{VBATMON}$).
- Battery monitor input pin (VBATSENSE): VBAT (unprotected battery) voltage monitor input; in standard application scenario, it can be connected to VBAT line through and external resistor ($R_{VBATSENSE}$).
- External clock input pin (CLKIN): digital input to be connected to an external 4 MHz clock source (normally provided by the ECU microcontroller), used to generate an accurate time base for the device; this is obtained by synchronizing CLKIN frequency value to the internal main oscillator one by a frequency-locked loop (FLL). An additional internal oscillator is provided as well to perform clock monitoring.
- System boost regulator (SYS boost): its purpose is to supply the whole device at 10 V nominal voltage when VIN is lower than a set voltage threshold value, sustaining ECU operation in low battery condition; regulator operates at 2 MHz and its circuit involves 3 device pins: SYSBST (output), SYSBSTSW (switching node) and BSTGND (switching power ground, shared with ER boost). When VIN is in a normal voltage operation range, SYS boost regulator is kept off and SYSBST pin voltage is (VIN-$V_{D\_SYSBST\_FWD}$), where $V_{D\_SYSBST\_FWD}$ is D_{SYSBST} diode forward voltage.
- Wakeup control circuit: it monitors both WAKEUP and VBATMON voltage values in order to initiate device startup phase; in order to guarantee correct operation even when VIN connection is lost (energy-reserve mode), circuit is supplied directly from SYS boost regulator output (SYSBST).
- Energy reserve boost regulator (ER boost): its main purpose is to provide a selectable 33 V/23.5 V voltage output, used to charge the energy reserve capacitor C_{ER}; regulator operates at 2 MHz and its circuit involves 3 device pins: ERBST (output), ERBSTSW (switching node) and BSTGND (switching power ground, shared with SYS boost). In a standard application scenario, ER boost is cascaded to SYS boost; regulator is enabled via Global SPI and it is also used to provide supply voltage to deployment safing FET regulator circuits.
- Energy reserve capacitor pin (VER): connected to energy reserve capacitor C_{ER}; ER cap provides an alternative supply path to the device, in case battery connection is lost or temporarily not available.
- Energy reserve charge circuit (ER charge): its main purpose is to provide a SPI-controllable low-ohmic path between ERBST and ERCHSW pins, allowing to charge the ER capacitor; in a standard application scenario, ERCHSW is connected to VER with an external resistor R_{ERCHSW}, used as a sense component for diagnostic purposes.
- Energy reserve discharge circuit (ER discharge): its main purpose is to provide a SPI-controllable low-ohmic path between ERDCHSW pin and ground, allowing to discharge the ER capacitor; in a standard application scenario, ERDCHSW is connected to VER with an external resistor $R_{ERDCHSW}$, used both as a current limiting component and as a sense component for diagnostic purposes.
- Energy reserve crossover switch circuit (ER switch): its main purpose is to provide a low-ohmic path between VER and ERSW pins; as VIN voltage supply path is lost, this circuit allows to supply SYSBST pin directly from the ER capacitor. In a standard application scenario, ERSW is connected to SYSBST through the external R_{ERSW_FWD}/R_{ERSW_REV} resistors and D_{ERSW_FWD}/D_{ERSW_REV} diodes, used both as current limiting components and as sense components for diagnostic purposes. ER crossover switch is back-to-back protected in off state and can be enabled via Global SPI too.
- Energy reserve crossover switch active output pin (COVRACT): its purpose is to provide a high logic level in case the ER switch has been enabled, transferring this information to external modules.
- Satellite buck regulator (SAT buck): its purpose is to provide a user-selectable 8 V/6.5 V voltage output via NVM programming, mainly used to supply remote sensor (satellite) interface supporting PSI-5 standard; regulator operates at 2 MHz with integrated synchronous rectifier and its circuit involves 3 device pins: SATBCK (output), SATBCKSW (switching node) and SATBCKGND (switching power ground). SAT buck input is internally connected to SYSBST pin.
- Remote sensor interface supply input pin (RSU_SUP_FLT): voltage input used to supply the internal remote sensor interface circuit; connection of this pin is mandatory as no internal supply path is present between SATBCK pin and the remote sensor interface. Suggested usage is to connect RSU_SUP_FLT to SATBCK externally on the ECU, adding a supply filter circuit (L_{RSU_FLT} and C_{RSU_FLT}).

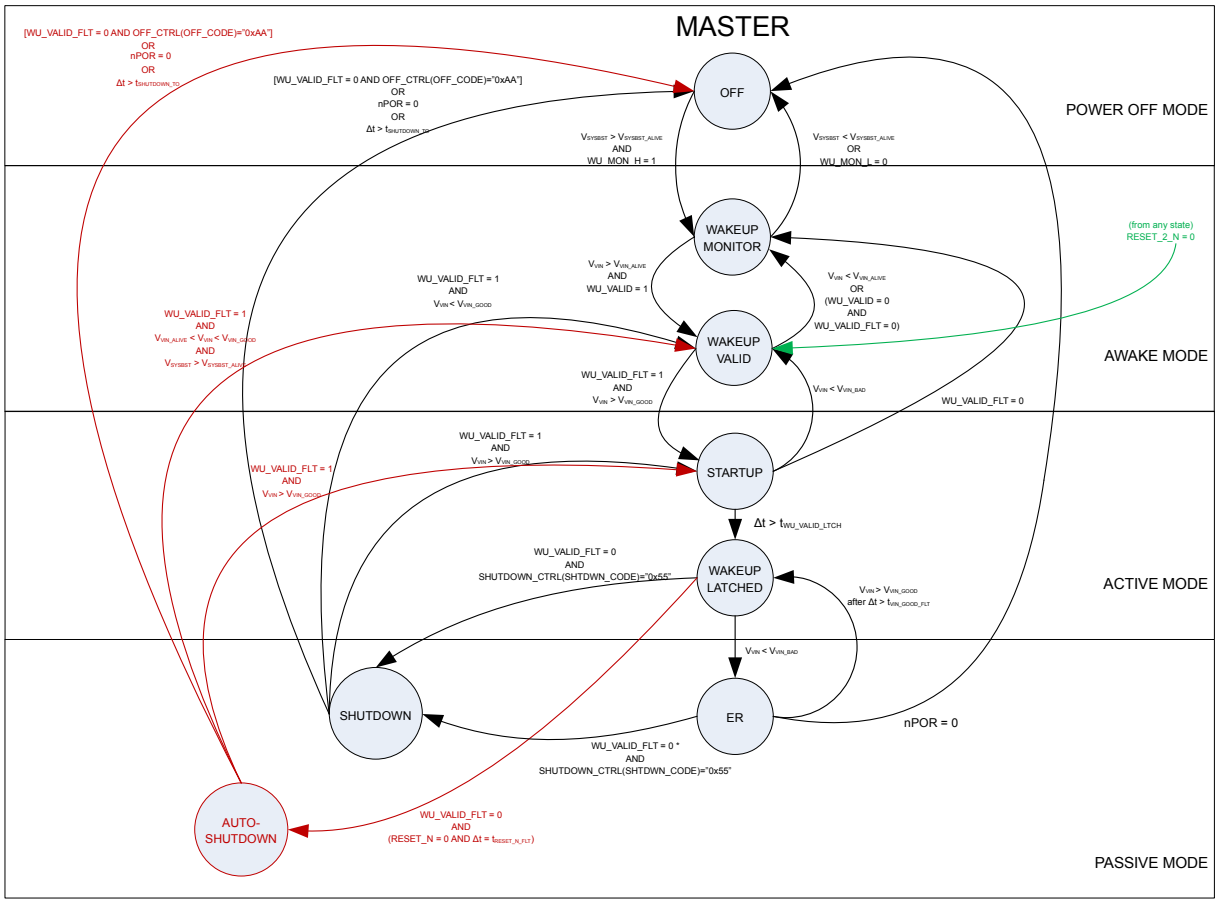
- SYNC pulse supply input pin (VSYNC): voltage input used to supply remote sensor interface SYNC pulse generator circuit; connection of this pin is mandatory as no device-internal supply path to SYNC pulse circuit. To ensure compliance to PSI-5 standard, it is suggested to generate VSYNC as a delta voltage drop with respect to RSU_SUP_FLT (for example a simple charge pump circuit duplicating SATBCK voltage, see Figure 3).
- Microcontroller supply buck regulator (VCC buck): its main purpose is to provide a 3.3 V voltage output, normally used to supply the ECU microcontroller core and I/Os; regulator operates at 2 MHz with integrated synchronous rectifier and its circuit involves 3 device pins: VCCBCK (output), VCCBCKSW (switching node) and VCCBCKGND (switching power ground). VCC buck input is internally connected to SATBCK pin; VCCBCK pin acts as supply line for the device digital I/Os, in order to guarantee voltage level coherence with the microcontroller.
- Microcontroller core supply voltage monitor input pin (VCOREMON): additional input to monitor the actual microcontroller core voltage (nominal expected value is 1.2 V), influencing VCC buck start-up behaviour; core monitor functionality is optional and can be enabled by writing the related configuration bit in NVM.
- Switching regulator clock synchronization output (CLKSW): digital output, used to synchronize the switching regulator time base of different devices in order to optimize the overall EME performance; this feature is used only in dual chip/master-slave scenario.
- Reset output pin (RESET_N): active-low digital reset signal, normally provided to microcontroller; pin driver has both pullup and pulldown capability.
- External module supply linear regulator (V5 regulator): its purpose is to provide a 5 V voltage output using an external PNP transistor as power element; this regulator is normally used to supply external modules on the ECU (for example CAN interface). Regulator circuit involves 2 device pins: V5_DRV (base driving output) and V5_SENSE (collector sense input, regulation output).
- Internal bias generation unit: it generates all voltage/current references and supply lines needed for correct device operation; this mainly includes bandgap circuits, bias current generators, and 2 fully integrated linear regulators, i.e. one for analog part supply (V3V3 ANA REG, 3.3 V nominal voltage), the other for digital part supply (V3V0 DIG REG, 3 V nominal voltage). This whole unit is supplied by VIN pin in device power-up first phase; at the end of it, V3V3 ANA REG regulator supply input is shifted to SAT buck, while digital part is directly supplied by VCC buck: this strategy allows to further improve device power dissipation performance.

All of the above circuits are controlled by the power mode control state machine.

4.1.2 Master power mode control

In case of single chip/master only application scenario, device is configured as master; as a consequence, its power mode control state machine follows the diagram showed in Figure 4. There are 4 main power modes, that is POWER OFF, AWAKE, ACTIVE and PASSIVE; each of these modes has a set of different states.

Figure 4. Power mode control state flow diagram for master IC



*Note: * (this condition can be disabled by NVM bit WU_WALID_FLT_SHTDW).*

Two general observations about the diagram:

- V_{SYSBST_ALIVE} and V_{IN_ALIVE} are not thresholds of a comparator: they represent the minimum voltage needed to supply the wake-up circuitry and the internal linear regulators respectively.
- The transitions with nPOR = 0 represent conditions that may happen normally in the device, without any fault; however, nPOR = 0 may drive transitions from ACTIVE mode to OFF mode in case of faults related to voltage regulators.

Here follows a detailed description of each mode and transition.

4.1.2.1 *POWER OFF mode*

In POWER OFF mode, all device regulators are disabled and system is kept in quiescent state; there is only one state defined for this mode, that is OFF. Device moves to AWAKE mode-WAKEUP MONITOR state, as soon as all of the following conditions are met:

- SYSBST pin voltage value is higher than V_{SYSBST_ALIVE}, that is the minimum needed supply voltage for wakeup circuitry correct operation
- Either of the two wakeup source input pins, that is WAKEUP and VBATMON, reach the minimum voltage value to start the basic operation of wakeup monitoring circuit; this happens if WU_MON_H = 1, where WU_MON_H is defined in the following way:

  WU_MON_H = (V_{WAKEUP} > $V_{WAKEUP\_MON\_H}$) OR ($V_{VBATMON}$ > $V_{VBATMON\_MON\_H}$)

In OFF state, VIN pin current is almost equal to zero (I_{VIN_OFF}), while SYSBST pin current is almost equal to zero (I_{SYSBST_OFF}) only when WU_MON_H = 0.

4.1.2.2 AWAKE mode

In AWAKE mode, device wakeup circuit becomes operative, starting to monitor WAKEUP/VBATMON voltages to check for a potential startup request.

There are two states defined for this mode:

- WAKEUP MONITOR: WAKEUP/VBATMON monitoring circuits are active, thus current drawn from SYSBST pin is $I_{SYSBST\_WU\_MON} > I_{SYSBST\_OFF}$; VIN pin current is $I_{VIN\_WU\_MON}$.

  Device moves to WAKEUP VALID state as soon as both of the following conditions are met:

  – VIN pin voltage value is higher than V_{VIN_ALIVE}, that is the minimum needed supply voltage for internal regulators correct operation

  – Either V_{WAKEUP} goes above $V_{WAKEUP\_VALID\_H}$ or $V_{VBATMON}$ goes above $V_{VBATMON\_VALID\_H}$, that is WU_VALID signal is set to 1

  Device falls back to POWER OFF mode-OFF state, if one or both of the following conditions are met:

  – SYSBST pin voltage falls below V_{SYSBST_ALIVE}

  – WU_MON_L = 0, where WU_MON_L is defined in the following way:

  WU_MON_L = ($V_{WAKEUP} > V_{WAKEUP\_MON\_L}$) OR ($V_{VBATMON} > V_{VBATMON\_MON\_L}$)

- WAKEUP VALID: internal voltage regulators (V3V3 ANA REG and V3V0 DIG REG) are enabled, digital part power-on reset (nPOR, active low) is released and NVM content download and CRC validation is performed; current drawn from VIN pin is increased to $I_{VIN\_WU\_VALID} > I_{VIN\_WU\_MON}$.

  Device moves to ACTIVE mode-STARTUP state, as soon as all of the following conditions are met:

  – VIN pin voltage value is higher than V_{VIN_GOOD}, that is the minimum needed supply voltage to allow correct operation of the whole power supply section

  – Either V_{WAKEUP} stays above $V_{WAKEUP\_VALID\_H}$ or $V_{VBATMON}$ stays above $V_{VBATMON\_VALID\_H}$ for a time longer than $t_{WU\_VALID\_FLT}$, that is WU_VALID_FLT signal is set to 1

  Device returns to WAKEUP MONITOR state in either of the following cases:

  – VIN pin voltage value goes lower than V_{VIN_ALIVE}

  – Both V_{WAKEUP} goes below $V_{WAKEUP\_VALID\_L}$ and $V_{VBATMON}$ goes below $V_{VBATMON\_VALID\_L}$ before either of the two sources has been validated, that is WU_VALID returns to 0 and WU_VALID_FLT is still 0

  – One or both wakeup sources have been already validated, but both of them disappear for a time longer than $t_{WU\_VALID\_FLT}$, that is starting from WU_VALID_FLT = 1, WU_VALID returns to 0 for a time longer then $t_{WU\_VALID\_FLT}$, thus WU_VALID_FLT is set to 0

4.1.2.3 ACTIVE mode

In ACTIVE mode, device power supply section becomes fully operative, following the implemented regulator power-up sequence. When VCC Buck exit from UV threshold, microcontroller reset will be released after RESET_N filter time expiration (t_{HOLD_RESET}).

There are two states defined for this mode:

- STARTUP: it is a transitory state, at the beginning of which regulator power-up sequence is started; device automatically moves to WAKEUP LATCHED state if it remains in STARTUP state for a time longer than $t_{WU\_VALID\_LTCH}$; device falls back to AWAKE mode-WAKEUP VALID state, if VIN pin voltage falls below V_{VIN_BAD} before $t_{WU\_VALID\_LTCH}$ counter expiration. However, device falls back to AWAKE mode-WAKEUP MONITOR state, if both wakeup sources disappear for a time longer than $t_{WU\_VALID\_FLT}$, that is WU_VALID_FLT is set back to 0, before $t_{WU\_VALID\_LTCH}$ counter expiration.
- WAKEUP LATCHED: once this state is reached, after completing power-up without any failure occurring on regulator circuits, device is ready to operate. No state change happens if only WU_VALID_FLT drops to 0, that is the wakeup condition is latched; device automatically moves to PASSIVE mode-ER state, as soon as VIN pin voltage falls below V_{VIN_BAD}; by this transition ER_STATE bit inside PWR_STATUS_1 register is set. Device can also move to PASSIVE mode, going in either of the following states:

  – SHUTDOWN state, if both WU_VALID_FLT = 0 (means after $t_{WU\_VALID\_FLT}$ since WAKE_UP_STATUS = 0) and SHUTDOWN_CTRL frame is received on Global SPI with SHTDWN_CODE = ”0x55”

  – AUTO-SHUTDOWN state (here ER discharge is automatically enabled), in case of failure during startup or microcontroller/SPI failure: this transition happens if WU_VALID_FLT = 0 and RESET_N is still 0 as $t_{RESET\_N\_FLT}$ filter time expires (due to WD_ERR_LATCHED or due to VCC Buck fault)

4.1.2.4 *PASSIVE mode*

In PASSIVE mode, device power supply section is reconfigured by enabling the ER switch; as a consequence, ER capacitor starts to supply the whole device through SYSBST pin (see Figure 3. Single chip/master-only block diagram) while SYS boost regulator is kept disabled; COVRACT pin output is set to high level.

There are three states defined for this mode:

- **ER**: as VIN pin voltage stays below V_{VIN_BAD} value (that is low or lost battery connection), device operation is guaranteed by ER capacitor supply; in this state, ER charge functionality is controlled by SPI. If device remains in ER state (that is battery voltage does not recover) for a time long enough to discharge all system capacitors, nPOR signal drops to 0, forcing device to go back to POWER OFF mode-OFF state.

  If, after blanking time $t_{VIN\_GOOD\_FLT}$, VIN pin voltage rises again above V_{VIN_GOOD} for a time longer than $t_{RISE\_VIN\_GOOD}$, device moves back to ACTIVE mode-WAKEUP_LATCHED state; ER_STATE bit inside PWR_STATUS_1 register is cleared upon SPI reading. However, if both WU_VALID_FLT drops to 0 (this condition can be disabled by NVM bit WU_WALID_FLT_SHTDW) and SHUTDOWN_CTRL frame is received on Global SPI with SHTDWN_CODE = ”0x55”, device moves to PASSIVE mode-SHUTDOWN state, that is SPI shutdown request.

- **SHUTDOWN**: following microcontroller SPI request, device starts to deplete the ER capacitor in order to perform shutdown; in this state, ER charge functionality is inhibited and both ER boost and safing FET regulators are kept disabled, but ER discharge circuit can be enabled in order to speed up ER capacitor discharge procedure. As device enters SHUTDOWN state, a permanence in SHUTDOWN state timer starts to count up ($t_{SHUTDOWN\_TO}$).

  If both WU_VALID_FLT is set again to 1 and VIN pin voltage is higher than V_{VIN_GOOD}, device interrupts shutdown and moves back to ACTIVE mode-STARTUP state; on the other hand, devices interrupts shutdown and moves back to AWAKE mode-WAKEUP_VALID state, if all of the following conditions are met:

  – WU_VALID_FLT is set again to 1
  – VIN pin voltage is lower than V_{VIN_GOOD} but it is still higher than V_{VIN_ALIVE}, thus keeping the internal voltage regulators correctly supplied
  – SYSBST pin voltage is higher than V_{SYSBST_ALIVE}, thus keeping wakeup monitor circuit correctly supplied

  Finally, device moves to POWER OFF mode-OFF state, in either of the following cases:

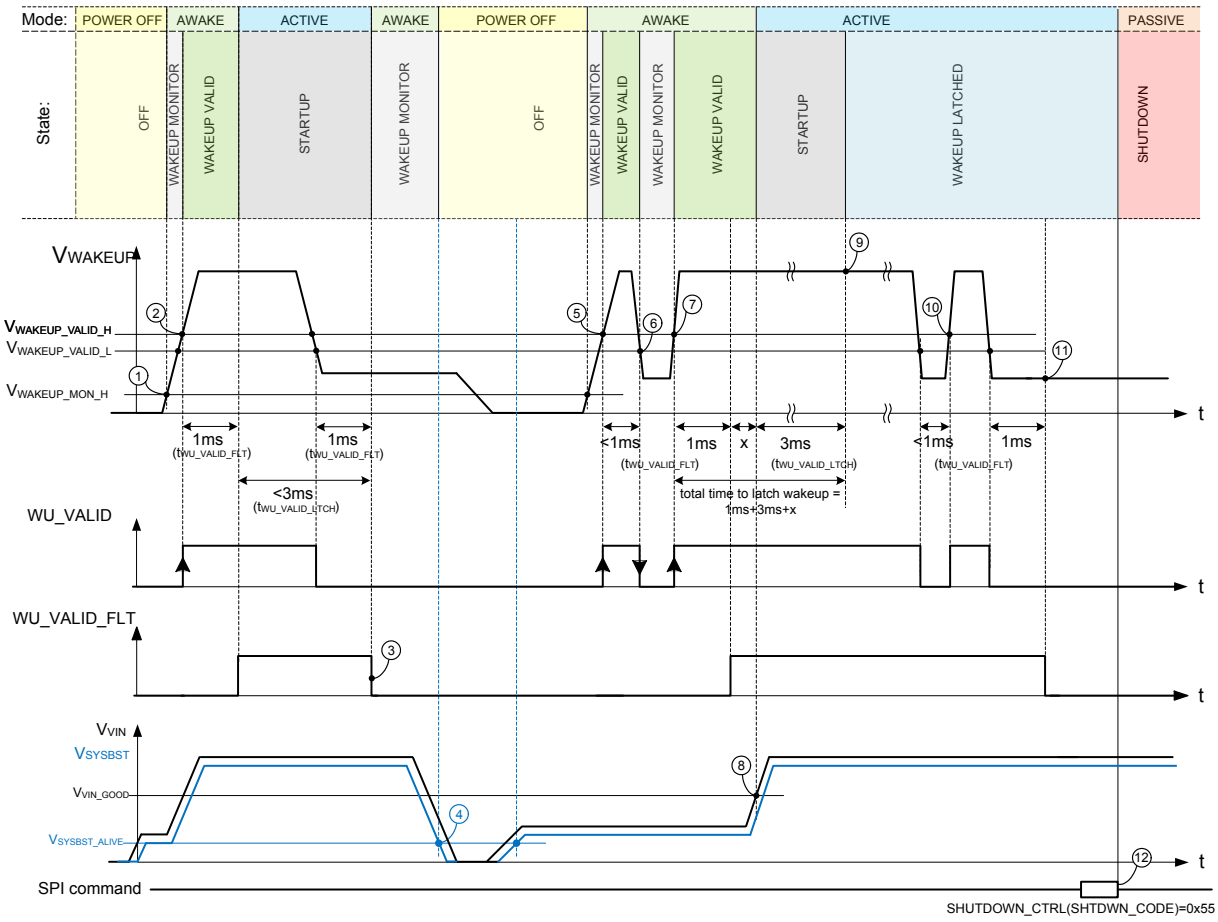
  – SPI OFF request: both WU_VALID_FLT = 0 and OFF_CTRL frame is received on Global SPI with OFF_CODE = ”0xAA”
  – Power-on reset: this happens in case device remains in SHUTDOWN state for a time long enough to discharge all system capacitors and nPOR signal drops to 0
  – Automatic transition to OFF state due to timeout, triggered by expiration of permanence in SHUTDOWN state timer ($t_{SHUTDOWN\_TO}$) before either of the two previous cases occur

- **AUTO-SHUTDOWN**: this state is equal to SHUTDOWN, with the additional feature of auto-enable of ER Discharge circuit.

4.1.2.5 *Wakeup source filter*

Figure 5 shows a timing diagram that explains WAKEUP pin voltage effect on power mode state change, including the description of WU_VALID and WU_VALID_FLT signals described in Section 4.1.2 Master power mode control; the same behavior applies to VBATMON pin.

Figure 5. WAKEUP filtering and latching



4.1.2.6 *Power mode status SPI reading*

An indication of present device power mode state is available on Global SPI by accessing DEVICE_STATUS register, PWR_MODE_STATE 2 bit field, with the following coding: 00 = AWAKE, 01 = ACTIVE, 10 = ER STATE, 11 = SHUTDOWN.

4.1.2.7 *Function disablement summary*

A summary of the device power modes is provided in the table below, indicating which functionality is kept disabled per each state. Note that, in STARTUP state, disable is related to device after RESET_N release (theoretically, many functions may be disabled even in WAKEUP_LATCHED state, in case RESET_N is still low).

Table 5. Disabled device functions by state

Function	POWER OFF	Mode						
		AWAKE		ACTIVE		PASSIVE		
	OFF	WAKEUP MONITOR	WAKEUP VALID	STARTUP	WAKEUP LATCHED	ER	SHUTDOWN	AUTO SHUTDOWN
Wakeup monitor	X	-	-	-	-	-	-	-
Internal regulators	X	X	-	-	-	-	-	-
SYS boost	X	X	X	-	-	X	X	X
ER boost	X	X	X	-	-	-	X	X
ER charge	X	X	X	-	-	-	X	X
ER discharge	X	X	X	-	-	-	-	-
ER switch	X	X	X	-	-	-	-	-
COVRACT Output(1)	X	X	X	X(2)	X(2)	-	-	-
SAT buck	X	X	X	-	-	-	-	-
VCC buck	X	X	X	-	-	-	-	-
V5 regulator	X	X	X	-	-	-	-	-
Safing FET regulators	X	X	X	-	-	-	-	-
Deployment drivers	X	X	X	-	-	-	-	-
Remote sensor I/F	X	X	X	-	-	-	-	-
Watchdog	X	X	X	-	-	-	-	-
NVM	X	X	-	-	-	-	-	-
Clock monitor	X	X	-	-	-	-	-	-
DC sensor I/F	X	X	X	-	-	-	-	-
GPO drivers	X	X	X	-	-	-	-	-
Arming logic	X	X	X	-	-	-	-	-
LIN I/F	X	X	X	-	-	-	-	-
RESET_N	X	X	X	-	-	-	-	-
ER cap diagnostic	X	X	X	-	-	X	X	X

1. *COVRACT output disabled means low logic level.*
2. *COVRACT is normally disabled, except during M/S connection self-test.*

4.1.3 Timing diagrams

Figure 6. Powerup sequence from OFF state to WAKEUP LATCHED state

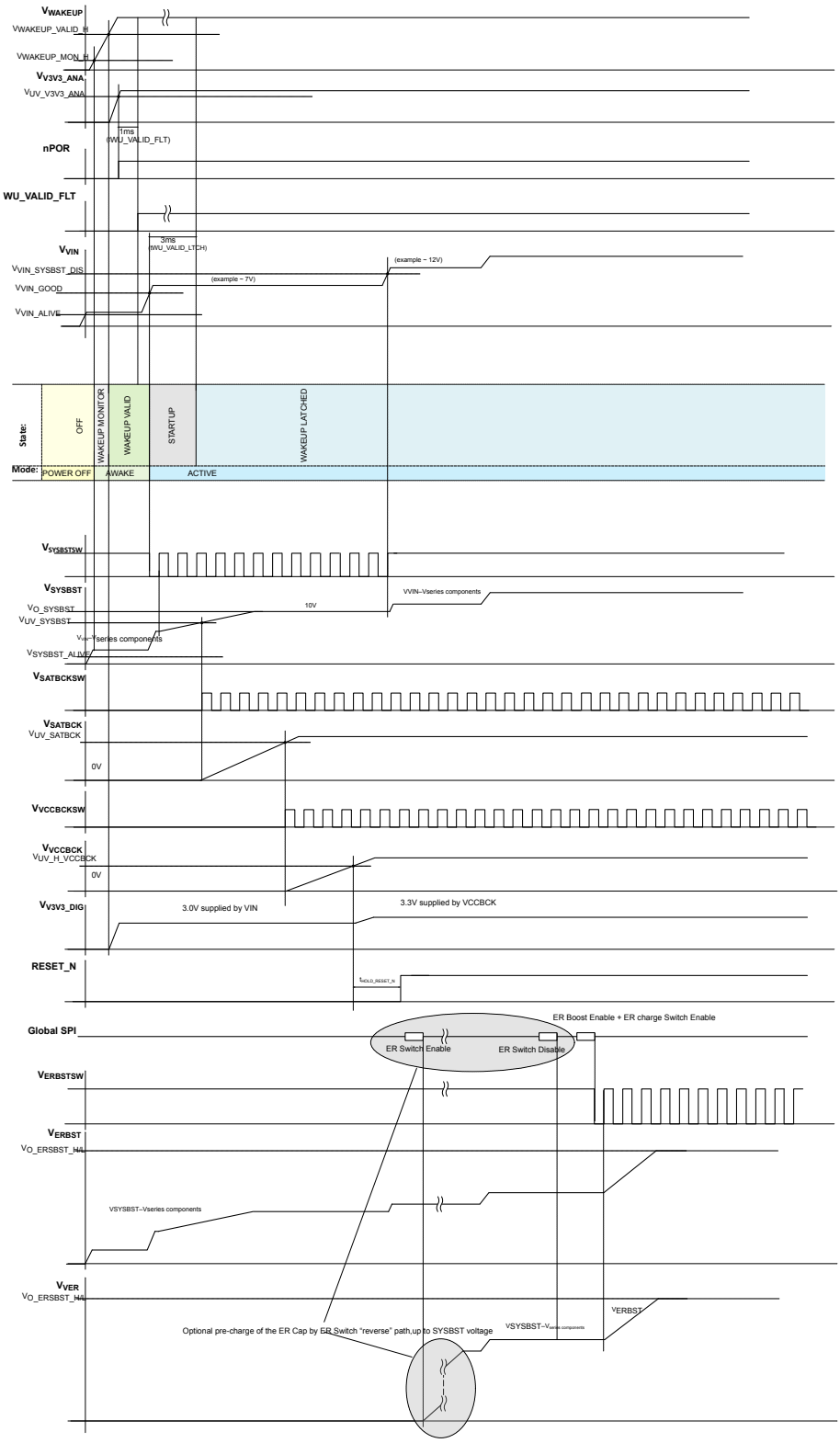


Figure 7. Powerdown sequence by SPI OFF CMD through SHUTDOWN state with ER discharge

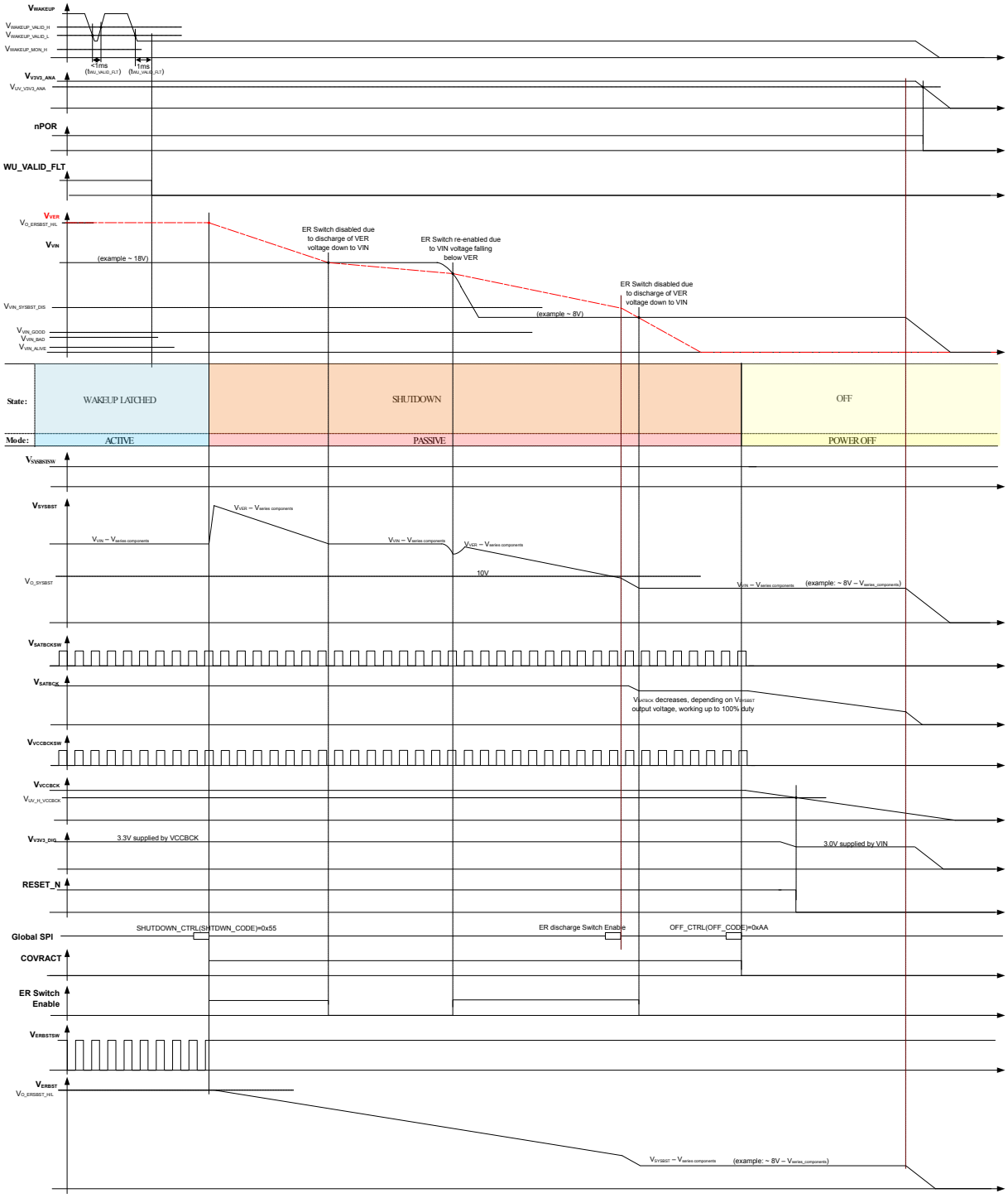
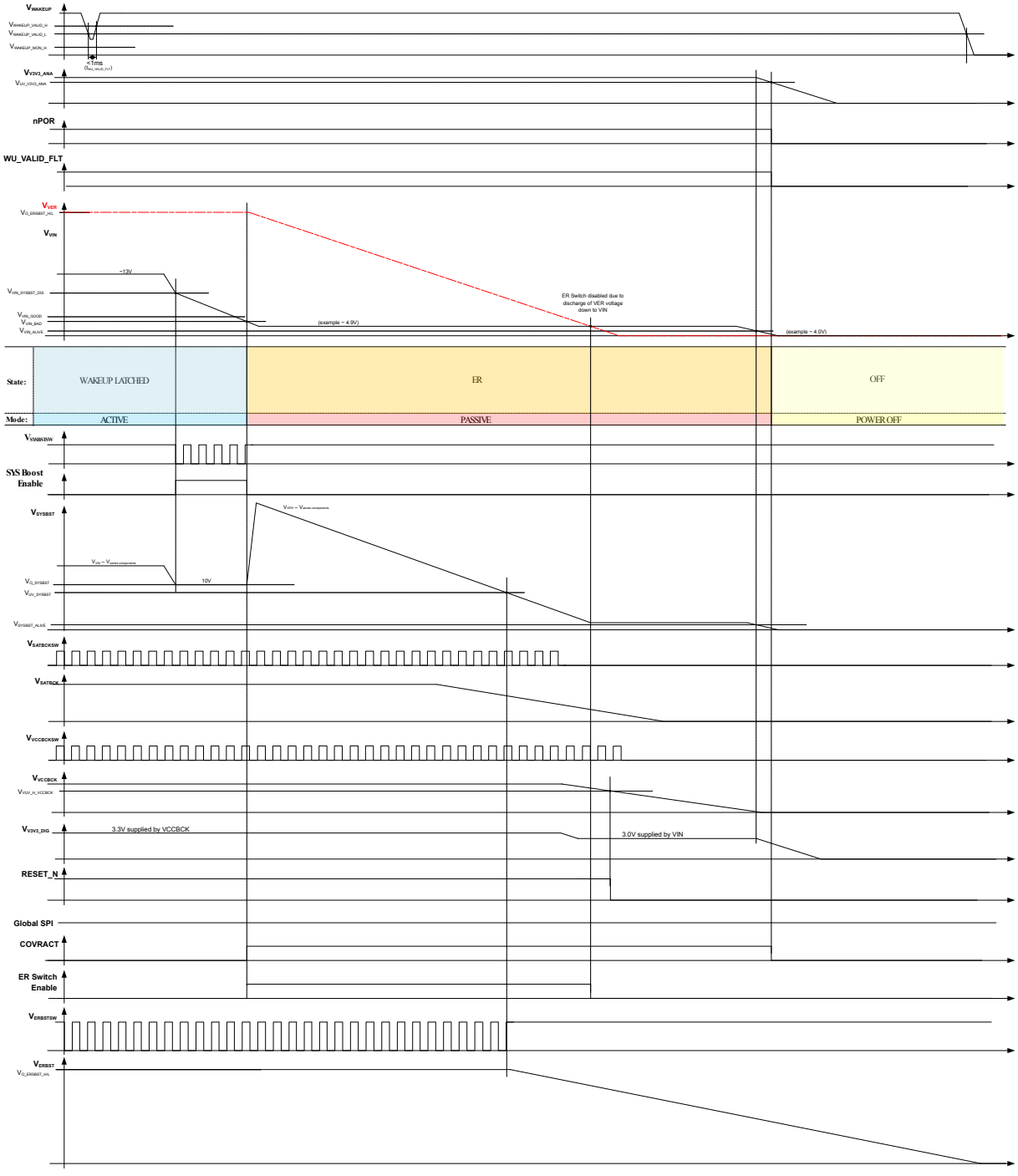


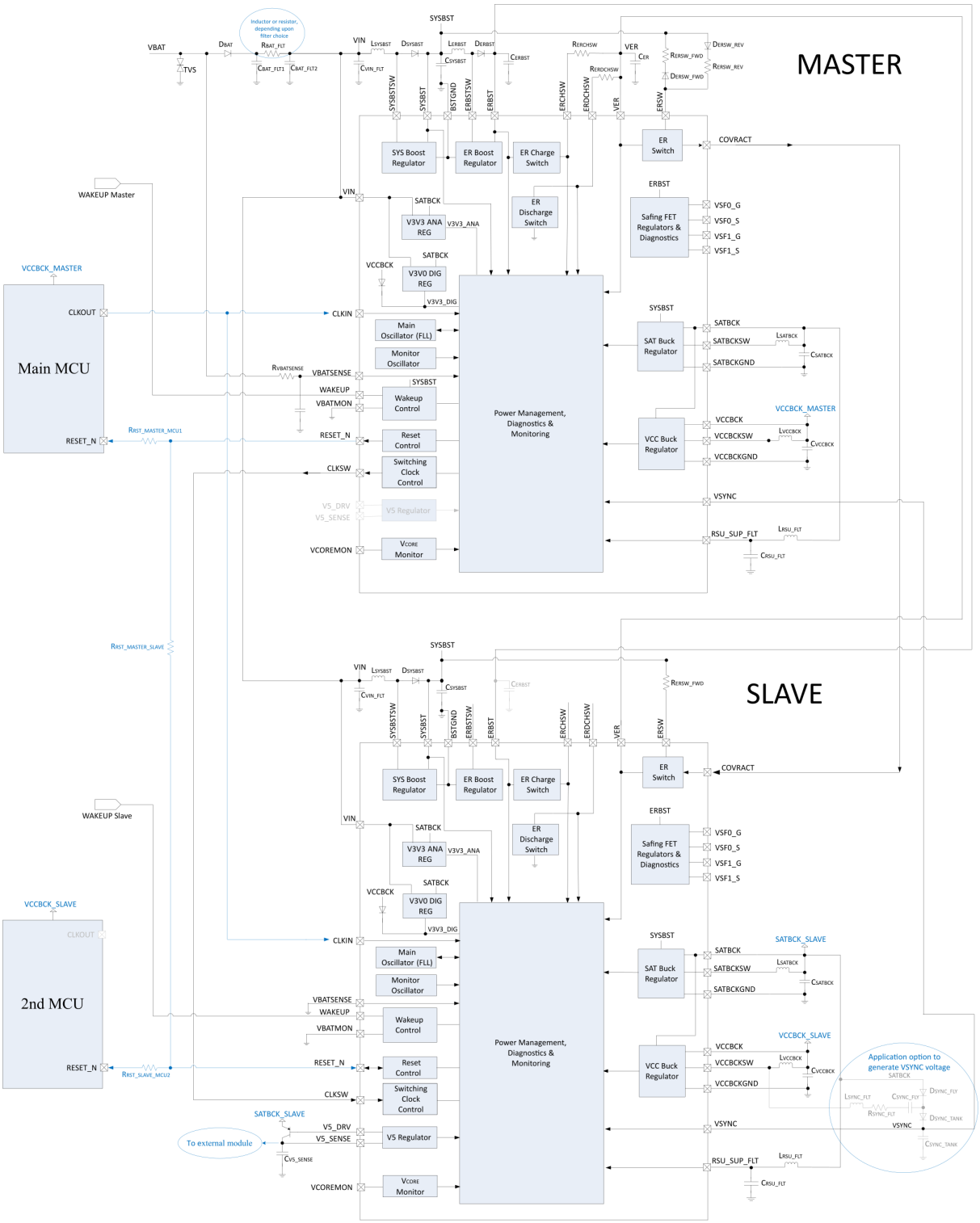
Figure 8. **Powerdown sequence by nPOR through ER state without battery**



4.1.4 Dual chip/master-slave scenario

An example of a dual chip/master-slave application scenario is shown in Figure 9, in which two microcontrollers are present, one connected to the master (primary micro) and one to the slave (secondary): this scenario is only one example of the various possible dual chip configurations; it has been chosen here to explain the operation of master and slave devices.

Figure 9. Example of dual chip/master-slave scenario



Master device offers the same functionalities described in Section 4.1.1 Single chip/master-only scenario; in the example shown in Figure 9, it has been decided to disable master V5 regulator.

Slave device offers the same functionalities described in Section 4.1.1 Single chip/master-only scenario, with the following exceptions:

- Energy reserve crossover switch active input pin (COVRACT): as COVRACT input is set to a digital high level, slave device moves to PASSIVE mode, ER state, and its own ER switch is activated. Moreover to check the COVRACT pin connection, in DIAG state (Master device), MCU can write the code 0x6 in COVRACT_MASTER_DIAG_START bit field in PWR_CTRL_0 SPI register, that generates a pulse of 1 us on COVRACT pin output in the Master device. The information is latched on COVRACT_SLAVE_STATUS bit in PWR_CTRL_0 SPI register.

  Finally MCU can read COVRACT_SLAVE_STATUS (Slave Device) and ER_SWITCH_SLAVE_STATUS in order to check if the pin and the switch work as expected.

  The register is clear on read.
- Reset input pin with pulldown capability (RESET_N): slave device RESET_N pin is an input pin with an internal active pulldown capability; thus, slave device is taken out of reset state when both its internal reset control logic is out of reset (that is internal pulldown is disabled) and its RESET_N pin voltage receives a digital high-level.
- Switching regulator clock synchronization input (CLKSW): digital input, driven by master CLKSW digital output and used to synchronize slave switching regulator time base to the master one.

In the example shown in Figure 9, both master and slave VIN pins are connected to the same battery line; in case of low battery condition, each device activates its own SYS boost regulator.

There is only one ER capacitor for both devices, that is VER pins are shorted together and connected to the ER capacitor on the ECU; however, ER boost regulator external components are mounted only for the master device, as well as the external resistors connected to ER charge and discharge circuits: this means that ER capacitor charge, discharge and diagnostic operations are handled only by the master device.

Slave device acts only as a user of the ER capacitor, thus the transition to PASSIVE mode-ER state is under full control of the master device through the COVRACT feature (see Figure 10. Power mode control state flow diagram for slave IC); slave ERSW pin is connected to slave SYSBST pin through a dedicated set of external resistors and diodes. Additionally, slave device ERBST pin is supplied by the master ER boost output, in order to guarantee slave safing FET regulator operation.

Both master and slave SAT buck regulators are available and used to provide power to the respective RSU_SUP_FLT remote sensor unit supply input; both master and slave VSYNC pins are supplied by a single external charge-pump circuit, whose operation is sustained by slave VCCBCKSW output (VSYNC generation from either master or slave IC is optional for the user); moreover, slave V5 regulator is used to supply an external optional module (for example CAN interface).

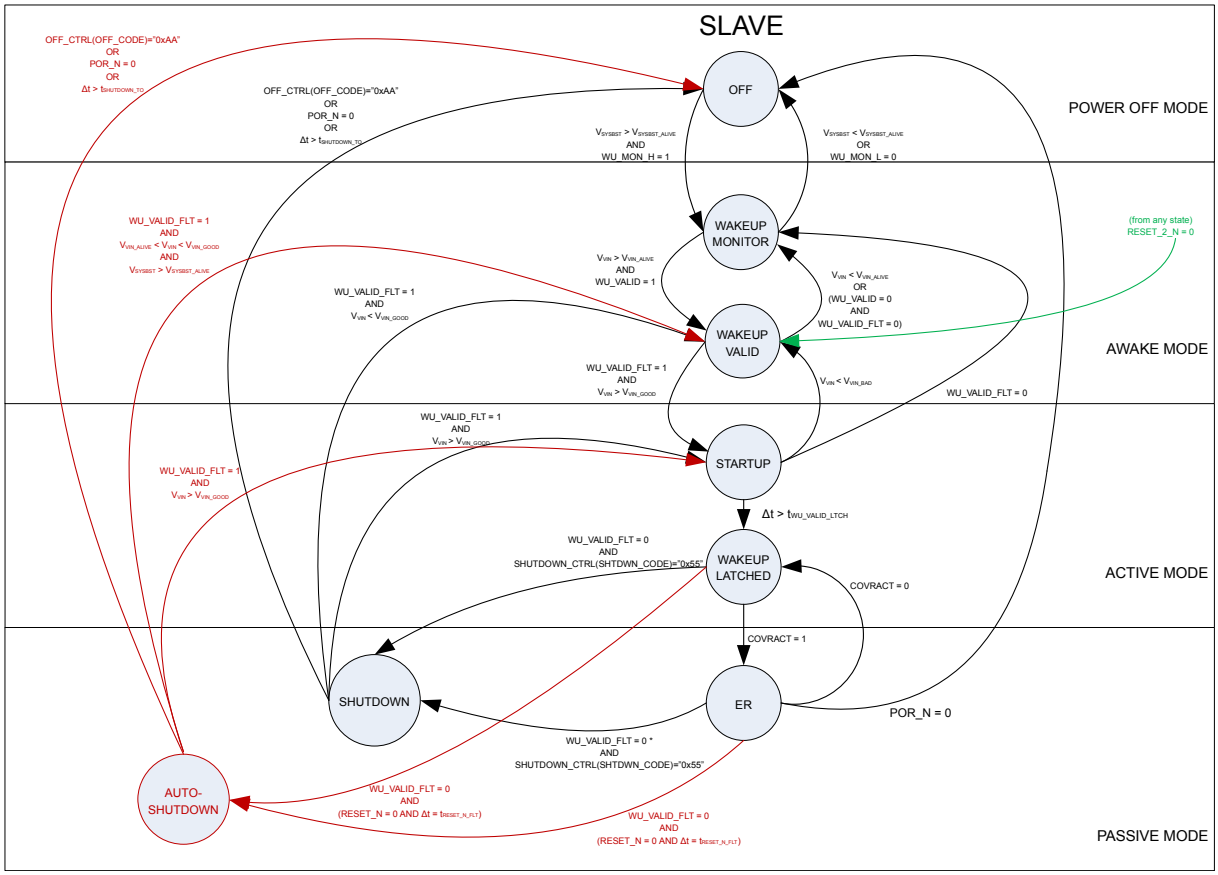
Master device is connected to the primary ECU microcontroller device, providing to it its own VCCBCK supply voltage and RESET_N output signal; slave device is connected to a secondary microcontroller device, providing to it its own VCCBCK supply voltage. Both secondary microcontroller reset and slave RESET_N pin are connected to the master/primary micro reset line through external decoupling resistors $R_{RST\_SLAVE\_MCU2}$ and $R_{RST\_MASTER\_SLAVE}$: as the master device RESET_N pin is the only one with pullup capability, the two microcontrollers and the slave device cannot go out-of-reset without the master consent; moreover, in case only the primary microcontroller is in auto-reset condition, the external decoupling resistor $R_{RST\_MASTER\_MCU1}$ lets master and slave devices (and secondary microcontroller) to be out of reset. Additionally, the primary microcontroller provides the CLKIN signal to both master and slave devices.

In another possible application scenario, only one VCC buck supplies both master and slave VCCBCK inputs, while the other VCCBCKSW is used only to generate VSYNC: user shall consider that, for the device sustaining VCC buck with dual chip load, other supply loads shall be reduced to stay within thermal budget.

4.1.5 Slave power mode control

In case of a dual chip/master-slave application scenario, master device operation follows the same power mode control state machine described in Section 4.1.2 Master power mode control; slave device follows a slightly different state machine, showed in Figure 10.

Figure 10. Power mode control state flow diagram for slave IC



*Note: * (this condition can be disabled by NVM bit WU_WALID_FLT_SHTDW).*

Slave state machine is composed by the same power modes and states of the master one, but some state transition conditions are different: main feature is that, once the device has entered in ACTIVE mode and wakeup has been validated, transition to/from PASSIVE mode are managed by COVRACT (configured as digital input); details follow in next paragraphs below.

4.1.5.1 *POWER OFF mode*

No difference compared to the master device; see Section 4.1.2.1 POWER OFF mode.

4.1.5.2 *AWAKE mode*

No difference compared to the master device; see Section 4.1.2.2 AWAKE mode.

4.1.5.3 *ACTIVE mode*

In ACTIVE mode, the device power supply section becomes fully operative, following the implemented regulator power-up sequence.

There are two states defined for this mode:

- STARTUP: same functionality as master device; see Section 4.1.2.3 ACTIVE mode.

- WAKEUP LATCHED: once this state is reached, after completing power-up without any failure occurring on regulator circuits, the device is ready to operate. Device automatically moves to PASSIVE mode-ER state, as soon as COVRACT goes to 1; by this transition ER_STATE bit inside PWR_STATUS_1 register is set. Device can also move to PASSIVE mode, going in either of the following states:
  - SHUTDOWN state, if both WU_VALID_FLT = 0 and SHUTDOWN_CTRL frame is received on global SPI with SHTDWN_CODE = ”0x55”.
  - AUTO-SHUTDOWN state (here ER discharge is automatically enabled), in case of failure during startup or microcontroller/SPI failure: this transition happens if WU_VALID_FLT = 0 and RESET_N is still 0 as $t_{RESET\_N\_FLT}$ filter time expires (due to master fault or VCC buck fault).

4.1.5.4 *PASSIVE mode*

In PASSIVE mode, the device power supply section is reconfigured by enabling the ER switch; as a consequence, the ER capacitor starts to supply the whole device through SYSBST, while SYS boost regulator is kept disabled.

There are three states defined for this mode:

- **ER**: as COVRACT = 1 (configured as input), device operation is guaranteed by ER capacitor supply; in this state, ER charge functionality is controlled by SPI (in case an ER capacitor is present also for the slave). If device remains in ER state (that is master device remains in PASSIVE mode) for a time long enough to discharge all system capacitors, nPOR signal drops to 0, forcing device to go back to POWER OFF mode-OFF state.

  If COVRACT falls again to 0, the device moves back to ACTIVE mode-WAKEUP_LATCHED state; ER_STATE bit inside PWR_STATUS_1 register is cleared upon SPI reading. However, the device can also move to PASSIVE mode, going in either of the following states:
  - SHUTDOWN state, if both WU_VALID_FLT = 0 (this condition can be disabled by NVM bit WU_WALID_FLT_SHTDW) and SHUTDOWN_CTRL frame is received on global SPI with SHTDWN_CODE = ”0x55”.
  - AUTO-SHUTDOWN state (here ER discharge is automatically enabled), in case of failure during startup or microcontroller/SPI failure: this transition happens if WU_VALID_FLT = 0 and RESET_N is still 0 as $t_{RESET\_N\_FLT}$ filter time expires (due to master fault or VCC buck fault).
- **SHUTDOWN**: following microcontroller SPI request, the device starts to deplete the ER capacitor in order to perform shutdown; in this state, ER charge functionality is inhibited (if requested also for the slave) and both ER boost (if enabled also for the slave) and safing FET regulators are kept disabled, but ER discharge circuit can be enabled in order to speed up ER capacitor discharge procedure. As the device enters SHUTDOWN state, a permanence in SHUTDOWN state timer starts to count up ($t_{SHUTDOWN\_TO}$).

  If both WU_VALID_FLT is set again to 1 and VIN pin voltage is higher than V_{VIN_GOOD}, the device interrupts shut down and moves back to ACTIVE mode-STARTUP state; on the other hand, devices interrupts shutdown and moves back to AWAKE mode-WAKEUP_VALID state, if all of the following conditions are met:
  - WU_VALID_FLT is set again to 1.
  - VIN pin voltage is lower than V_{VIN_GOOD} but it is still higher than V_{VIN_ALIVE}, thus keeping the internal voltage regulators correctly supplied.
  - SYSBST pin voltage is higher than V_{SYSBST_ALIVE}, thus keeping wakeup monitor circuit correctly supplied.

  Finally, the device moves to POWER OFF mode-OFF state, in either of the following cases:
  - SPI OFF request: OFF_CTRL frame is received on global SPI with OFF_CODE = ”0xAA”.
  - Power-on reset: this happens in case the device remains in SHUTDOWN state for a time long enough to discharge all system capacitors and nPOR signal drops to 0.
  - Automatic transition to OFF state due to timeout, triggered by expiration of permanence in SHUTDOWN state timer ($t_{SHUTDOWN\_TO}$) before either of the two previous cases occur.
- **AUTO-SHUTDOWN**: this state is equal to SHUTDOWN, with the additional feature of auto-enable of ER discharge circuit.

4.1.6 Master-slave timing diagrams

In the following figures, it is shown an example of the power-up/down sequence in a master-slave scenario with power mode wakeup control; refer to Figure 9. Example of dual chip/master-slave scenario for the related schematic.

Figure 11. Master-slave powerup sequence with power mode wakeup control

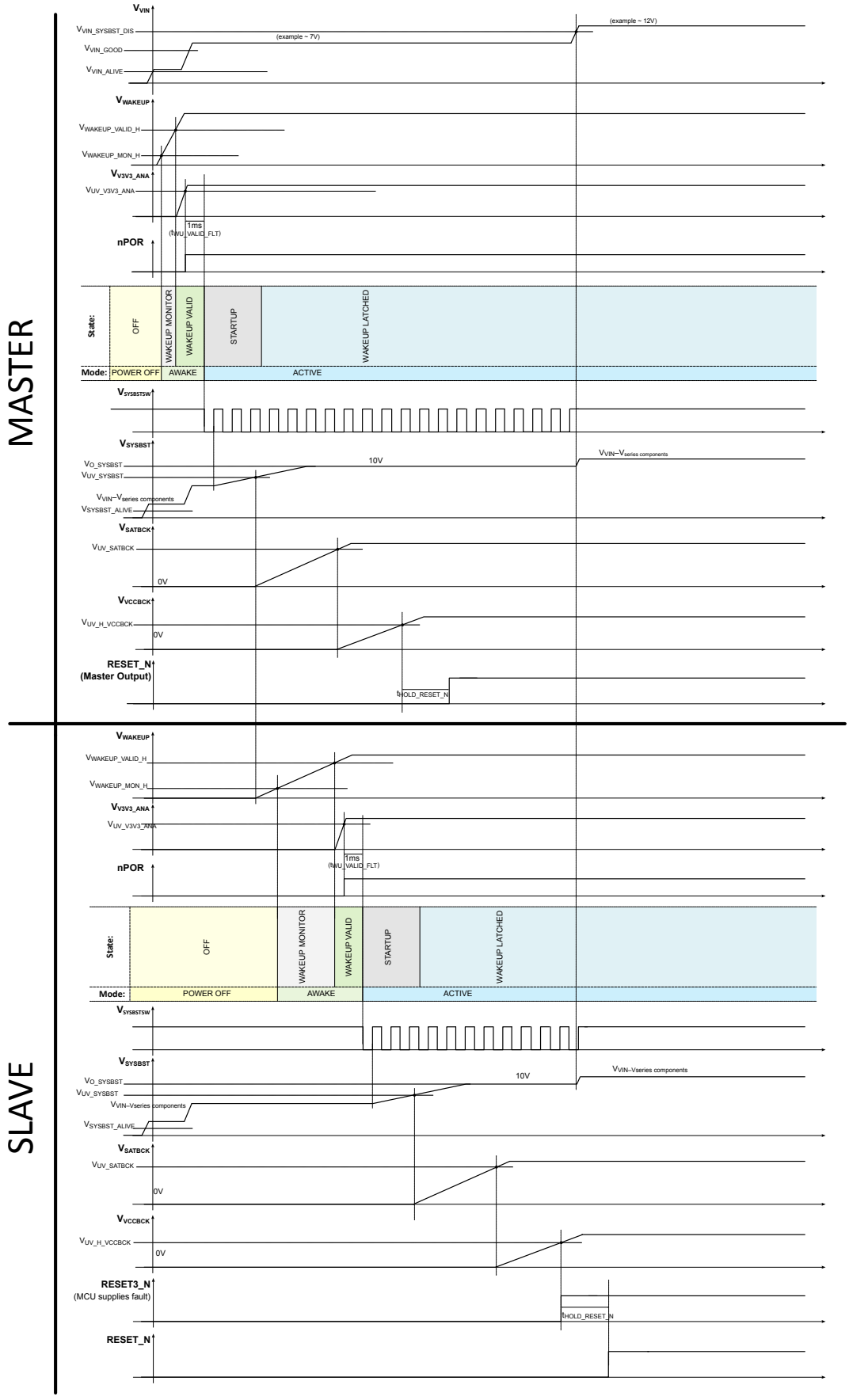
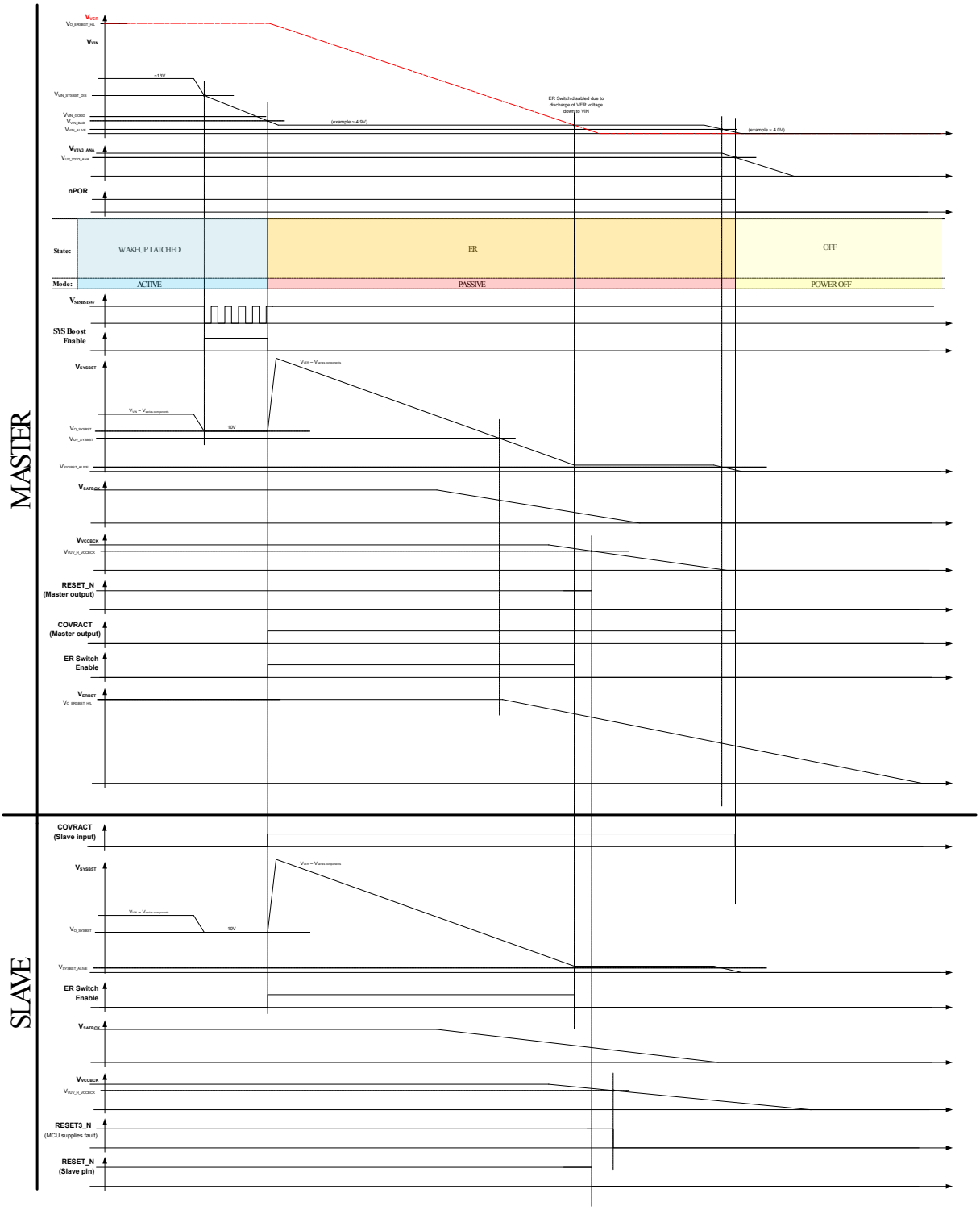


Figure 12. **Master-slave powerdown sequence via ER state**



4.2 IC operating control system

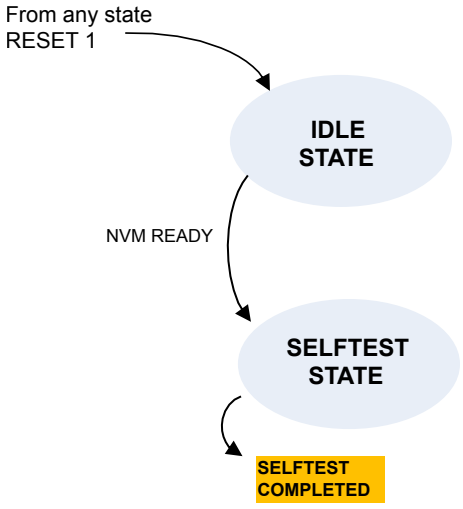
Operating states allow safe and predictable initialization, test, operation and final disposal of the part (scrapping). There are two state machines, the first one to handle NVM and SELFTEST after power up, the second one that handle the device operating states.

4.2.1 IC initialization state machine

The INIT state machine is composed by two main states:

- **IDLE STATE**: until the RESET 1 is not de-asserted, the device remains in this state. Upon RESET 1 is de-asserted, the NVM content is downloaded inside the trimming registers. Upon the download is completed NVM_READY is set to 1 and the NVM_USER_CRC_ERR and NVM_CRC_ERR will report the NVM CRC check status. The device transitions to SELFTEST state.
- **SELFTEST STATE**: here the analog, logic and memory bist start up as soon as the RESET 2 is released. The relative status can be checked respectively in DEVICE_STATUS register and in LBIST_CTRL register. Upon all the bist are completed the DEVICE_STATUS (SELFTEST_COMPLETED) is set. Both NVM download and BIST (logic and memory) run in parallel during power up phase, during the execution of logic BIST there will be an increased current consumption from VCCBCK pin (about 30 mA).

Figure 13. Initialization state machine



4.2.1.1 *Built-in self-test (BIST)*

The analog BIST (ABIST) is checked during startup phase and can be re-triggered at any time setting bit SPI_ANALOG_BIST_RETRIGGER. The involved comparators are:

- SG_LOSS_x
- SS_OV_x_y
- SATBCK_UV
- SYSBOOST_OV
- SYSBOOST_UV
- VIN_BAD
- VIN_GOOD
- FAST_SLOPE_VIN
- VIN_SYSBST_DIS
- VIN_OV
- VSYNC_UV
- VCOREMON_UV
- VCOREMON_OV
- VCCBCK_OV
- VCCBCK_UVL

- VCCBCK_UVH
- ERBOOST_OV
- ERBOOST_UV
- V5_SENSE_UV
- V5_SENSE_OV
- V5_SENSE_STG
- PGND_LOSS
- VCCBCKGND_LOSS
- SATBCKGND_LOSS
- BSTGND_LOSS
- ERDCHSW_OC
- GPO_OT_x
- RSU_OT_x
- SYSBST_OT
- ERBST_OT
- ERCHRSW_OT
- ERSW_OT
- VCCBCK_OT
- SATBCK_OT
- OT_LIN
- ACL

In order to be properly executed, ABIST should be run with monitored inputs at their nominal value; ABIST re-trigger can be requested by MCU in case previous condition cannot be met, to validate potential failures at start-up. The ABIST failure do not inhibit the device functionalities and it can be retriggered multiple times.

After the analog BIST, three Logic BIST (LBIST) run sequentially to check:

1. SAFING LOGIC
2. PSINH DC SENSOR & ACL LOGIC
3. E2E LOGIC

MCU can check the state in LBIST_CTRL register and can request every LBIST in DIAG state. The LBIST sequence is:

- MCU verify the SELFTEST_COMPLETE status bit.
- Once the SELFTEST_COMPLETE is true, the MCU can verify SELFTEST_ERR status bit.
- If the SELFTEST_ERR is true, MCU can trigger again LBIST to start.

In case of LBIST fault a dedicated flag is set. The whole logic BIST duration lasts for t_{LBIST}.

When the three LBIST are completed, the Memory BIST (MBIST) starts automatically and it will be completed in t_{MBIST}. MCU can check the MBIST status in LBIST_CTRL register and can request it on demand in DIAG state.

4.2.1.2 *Background monitoring*

Moreover, the device provides a background monitoring function for the following group register:

Safing configuration registers:

- 44 reg SAF_CONTROL_x
- 22 reg SAF_THRESHOLD_P_x
- 22 reg SAF_THRESHOLD_N_x
- 22 reg SAF_FOC_SEEDVAL
- 10 reg SAF_PROG_MASK_x
- 10 reg SAF_REQ_PROG_MASK_x
- 10 reg SAF_RESP_PROG_MASK_x
- 44 reg SAF_REQ_TARGET_MASK_x
- 44 reg SAF_RESP_TARGET_MASK_x
- 6 reg SAF_CS_CONFIG_x

Deployment/arming configuration registers:

- 8 reg LOOP_MATRIX_ARM_x
- 1 reg LOOP_MATRIX_PSHINH
- ARM_PSINH_MCU2_CTRL

LIN configuration registers (disable by NVM bit):

- 4 reg LIN_OCS_MASK_PTx
- 4 reg LIN_OCS_TGT1_PTx
- 4 reg LIN_OCS_TGT2_PTx
- LIN_CFG

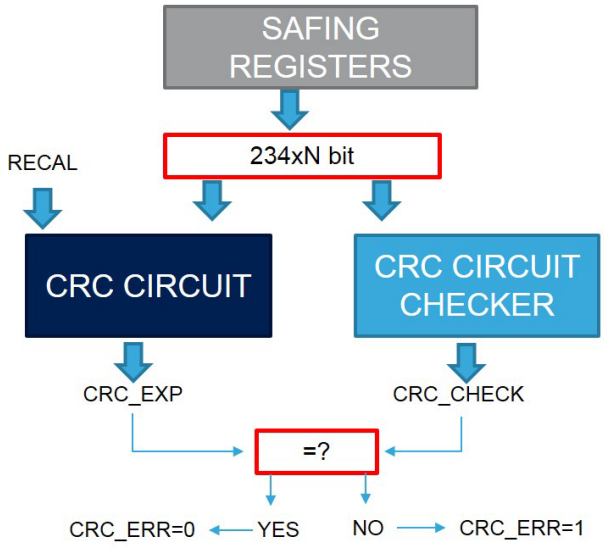
E2E configuration registers (disable by NVM bit):

- E2E_ARM_GLOBAL_CFG
- 3 reg E2E_ARM_DATA_ID_0x_CFG
- 15 reg E2E_ARM_DATA_ID_LIST_0x_CFG
- E2E_TX1_ARM_CFG
- 4 reg E2E_TX1_ARMxy_MAPPING_CFG
- E2E_TX2_ARM_CFG
- 4 reg E2E_TX2_ARMxy_MAPPING_CFG
- E2E_RX_ARM_CFG
- E2E_RX_ARM_CFG3
- 4 reg E2E_RX_ARMxy_MAPPING_CFG
- E2E_RX_ARM_DWELL_CFG

The background monitoring function works as following:

- The MCU will perform all device configurations (in DIAG state).
- The MCU will ignore the CRC fault flag during the process of configuring the device.
- The MCU will track all on going configuration. Once all configurations are complete, the MCU will request RECALC command from the device. The time to compute a CRC for every register is 2 µs.
- The MCU will verify no CRC fault is present.
- If a CRC fault is present the MCU will attempt to reconfigure and RECALC the CRC.
- When either CRC fault flag is clear (that means CRC_EXP = CRC_COMPUTED internally and MCU clears the flag), the MCU will request the device to enter SAFING state (configuration register cannot be written because write operation of that register are inhibited, so CRC_EXP is locked).
- If the CRC fault flag remains active, then the MCU will take appropriate actions to drive the system in a safe state.
- The MCU will monitor the CRC flags periodically for the remainder of the key cycle.

Figure 14. **Background monitoring concept**



4.2.2 IC safety state machine

Device operating states are shown in the state diagram in Figure 15. RESET_4 always forces the state machine to the INIT STATE from any safety state. The device can evolve in the following states:

- **INIT STATE**: in this state upon RESET_4 is de-asserted at the beginning of the ACTIVE mode, the microcontroller powers up. MCU can configure the registers watchdog timing thresholds. When the watchdog service begins or the watchdog overwrite command is set (for the device configured as a master) the devices switches to DIAG state. For slave device, SSM_CTRL(DIAG STATE) entry command is sufficient to enter into DIAG state.
- **DIAG STATE**: in this state, the system can initialize specific functions and execute specific diagnostic tests. Once the system leaves DIAG state, the only way to come back again here is a RESET_4. The state machine remains in this state until commanded to transition into the SAFING or SCRAP state by dedicated SPI commands on the global SPI bus.
- **SAFING STATE**: primary runtime state for the system. System monitors sensor data and enters into ARM_SAFE state if sensor data meets the criteria for arming. The device can also transition to SCRAP state if SPI scrap CMD sequence is received from MCU using the SAFING_SCRAP_CTRL register. In idle state, the MCU must perform a reading access to read SAFING_SCRAP_CNT (SAFING_SCRAP_FDBK field) at the same time as sent SAFING_SCRAP_CODE_A command. When MCU sent SAFING_SCRAP_CODE_A command, the device freezes the SAFING_SCRAP_CNT that is used as seed for comparison to the next states (see Figure 16).
- **ARM_SAF STATE**: device is armed and VSF regulator is enabled to allow deployment in this state. The state machine automatically returns to SAFING state when the arming condition is no longer valid.
- **SCRAP STATE**: the device no longer processes system sensor data (safing logic is disabled) but is monitoring for valid ACL signal on ACL pin and valid scrap key input on global SPI to enter into ARM_SCRAP state.
- **ARM SCRAP STATE**: the device is armed and VSF regulator is enabled to allow scrap deployment in this state. The state machine can return to SCRAP state if the invalid ACL signal or invalid scrap key is received from MCU.

Figure 15. **IC operating state diagram**

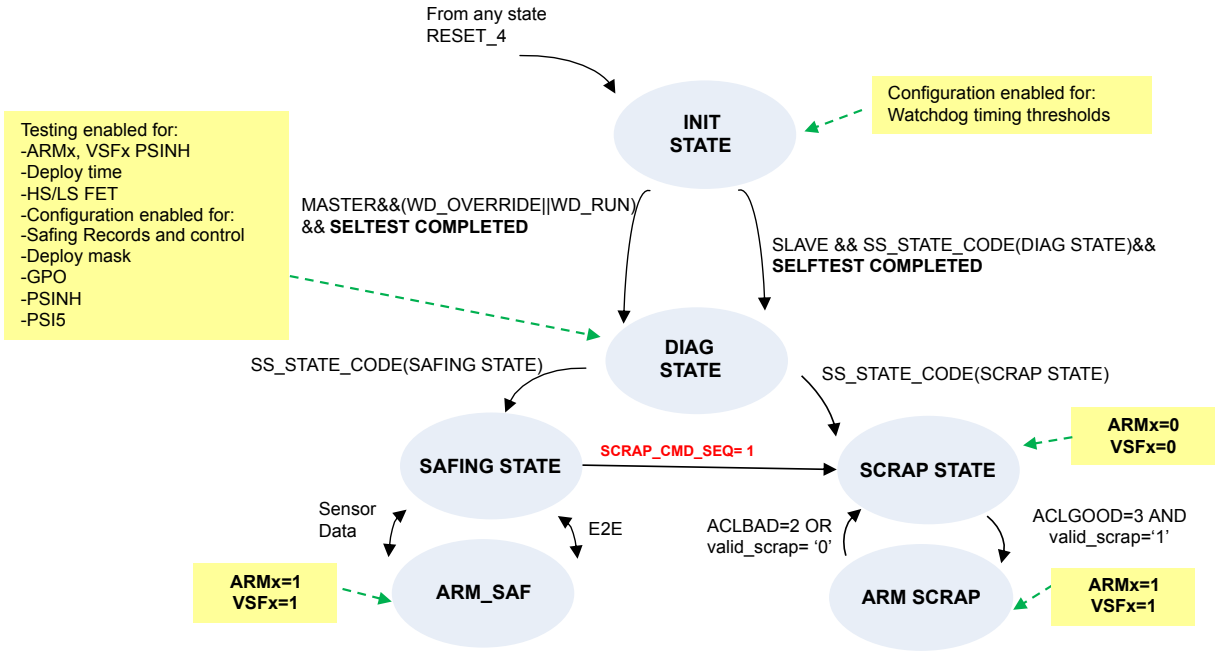
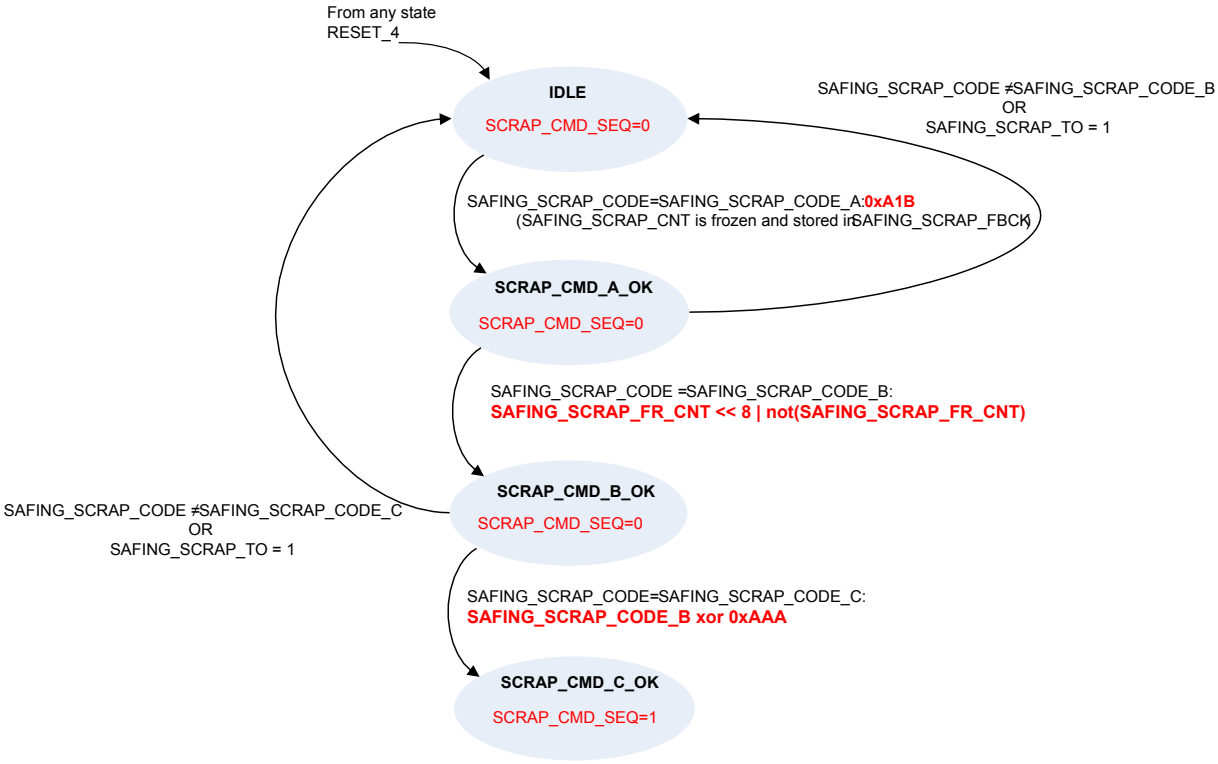


Figure 16. **SCRAP commands sequence**



4.3 Internal regulators and nPOR generation

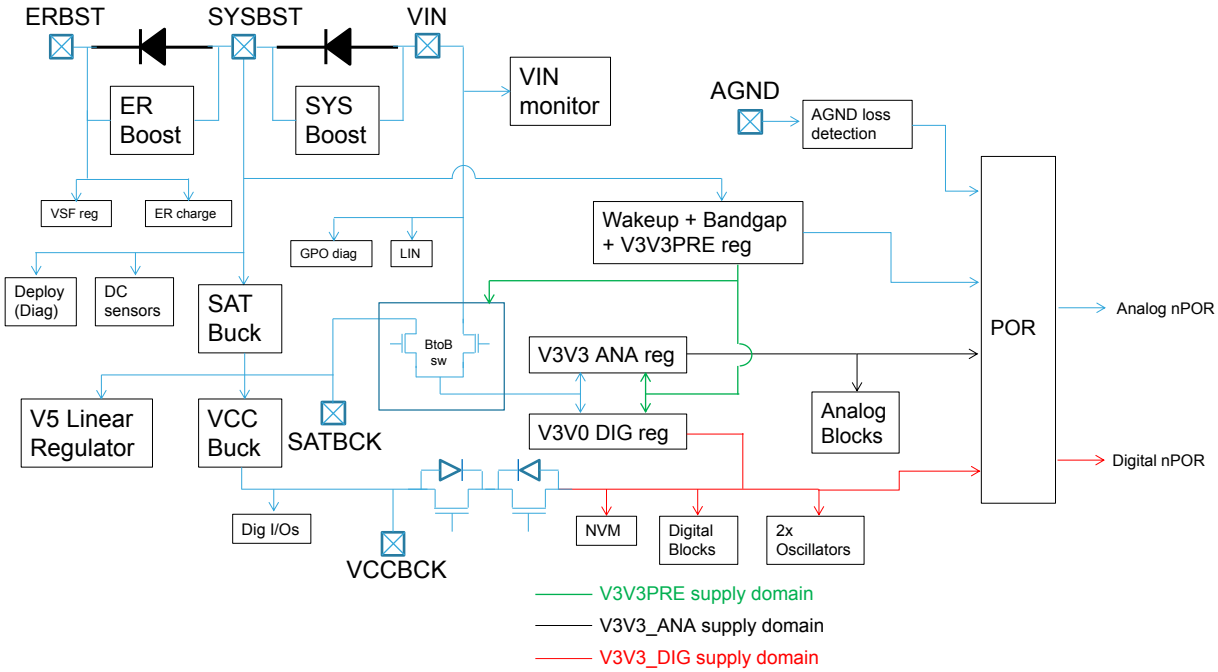
The L9691 has two low-voltage power domains, one for the analog circuits (V3V3_ANA) and one for the digital circuits (V3V3_DIG). The first one is provided by a linear internal regulator, V3V3 ANA reg, while the second one is supplied by the VCCBCK in steady state conditions; at power-up, when VCCBCK is not yet available, a second internal regulator, V3V0 DIG reg, is used to supply the digital circuits at 3.0 V, so that, as soon as VCCBCK is greater than 3 V, V3V3_DIG will be sourced by the buck and V3V0 DIG reg will be automatically turned-off by the control loop (that is it goes naturally in open loop, because its output voltage is pulled-up at a voltage value higher than regulation value), reducing the power dissipation. In the event that VCCBCK drops out of regulation (V_{VCCBCK} < 3 V), V3V3_DIG will revert back to V3V0_DIG_int to ensure continuity of digital operation.

None of these linear regulators require an external bypass capacitor (no external pin is connected to their output voltage).

In order to further reduce the internal power dissipation, the L9691 automatically switches the source for these internal regulators between VIN and SATBCK: both regulators are initially powered from VIN during startup and switch over to SATBCK when it achieves regulation (V_{SATBCK} > V_{UV_SATBCK}). In the event that SATBCK drops out of regulation (V_{SATBCK} < V_{UV_SATBCK}) and the device is not in PASSIVE mode, the input to the regulators revert back to VIN to ensure continuity of operation.

The two low-voltage power domains are monitored in order to generate a power-on reset (nPOR) in case of any fault on those supply lines. AGND connection is monitored as well and a loss of AGND will generate analog nPOR too. V3V3PRE reg is an internal linear regulator which provides supply for internal startup circuit, including wakeup, bandgap, V3V3 ANA reg and V3V0 DIG reg, POR, switches to select main supply for linear regulators between SATBCK and VIN.

Figure 17. Block diagram supply connections



4.4 Oscillators, FLL function and CLKSW usage

4.4.1 Oscillators and FLL function

The L9691 device integrates two trimmed oscillators: the main oscillator runs at 16 MHz typ (trimmed accuracy of ±5%), with the possibility to vary instantaneous frequency for spread spectrum capability, and it is used to provide clock to the internal synchronous logic and for the switching regulators operation (at a divided frequency of typ 2 MHz); the auxiliary oscillator runs at 10 MHz typ and is used to monitor the main oscillator. In the event of an internal oscillator fault, CLK_FREQ_ERR = 11 (CLK_CTRL Global SPI register) is set and RESET_2_N is asserted; bit is cleared upon SPI reading after fault has disappeared. In addition, in case of clock main or aux stuck at fault, CLK_STUCK_ERR (CLK_CTRL Global SPI register) will be set.

An accurate (±1%) 4 MHz external oscillator is provided by the MCU on CLKIN pin and can be used in the frequency locked loop circuit (FLL) to adjust run-time the average frequency of the main oscillator (the instantaneous frequency may vary according to the spread spectrum feature). The FLL function is enabled by using CLK_CTRL Global SPI register, SPI_FLL_EN bit and is locked after T_{FLL_LOCK} this bit is cleared (and so FLL is disabled) in either of the following cases:

- RESET_N = 0, that is MCU stops to send 4 MHz clock on CLKIN, so no FLL function is possible
- CLK_FREQ_ERR = 01: in this case, the fault is due to a problem on CLKIN, by opening the frequency loop the main oscillator will recover into the open loop accuracy (±5%), so the device digital functionality is kept alive and clock frequency error disappears: if FLL function is enabled, main clock frequency accuracy improves from ±5% to ±1% (not considering the loop error). Anyway, thresholds for clock monitor are defined in order to guarantee that no CLK_FREQ_ERR is asserted with FLL disabled (typ thresholds are ±15% around 16 MHz). On the other hand, if the fault is due to a problem on the main/monitor oscillator itself (CLK_FREQ_ERR = 11), no digital functionality is possible and so there is no reason to keep FLL enabled.

With FLL enabled, after a transient phase necessary for the loop to go in steady-state (tracking time with external oscillator), main oscillator frequency has a residual loop error of ±0.3%.

4.4.2 Frequencies and phases for switching regulators

In order to limit EME, it is needed to:

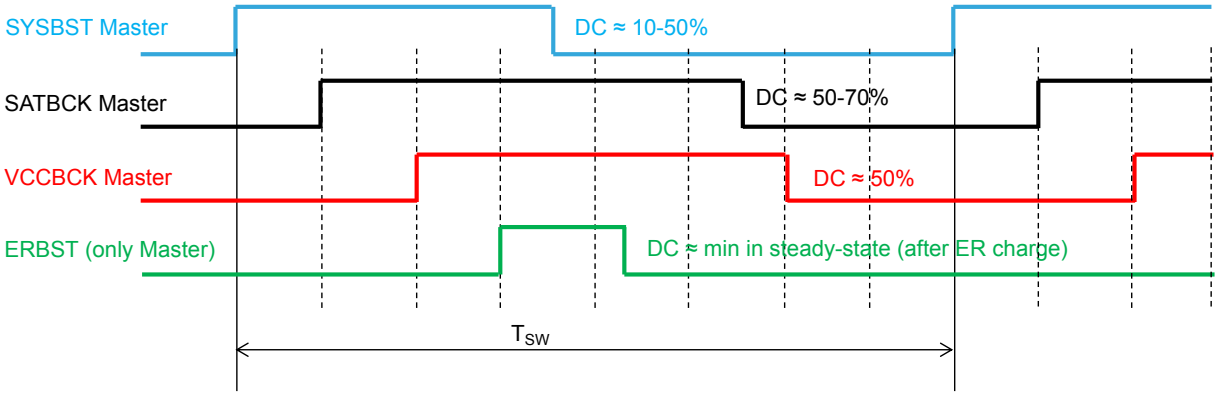
- Select appropriate phase among switching regulators (this applies for both single chip/master-only scenario and master-slave).
- Keep same clock frequencies between master and slave in a dual-chip scenario, to avoid beat frequency emissions: CLKSW pin is used for this purpose.

4.4.2.1 *Switching regulators phases*

A possible phase distribution in a single-chip scenario is shown in Figure 18, considering that:

- Switching period T_{SW} can be divided into 8 time slots (16 MHz/2 MHz).
- At least, turn-on time of main power-MOS (HS for buck) can be split into each of these slots.
- Turn-off time is decided by the control loop and it cannot be directly synchronized, but duty cycle can be estimated in order to distribute on-off switching in the period.

Figure 18. Switching regulators phases



For this purpose, each switching regulator phase can be SPI programmed by writing into register PWR_CTRL_1; each phase has a 3 bit resolution, so that it is possible to start each regulator into any of the 8 time slots. Note that these phases can be changed at any time in INIT and DIAG states; in all other states, these config registers are locked.

4.4.2.2 *Master-slave synchronization by CLKSW*

In order to align switching timebase frequencies between master and slave, first of all the FLL function shall be enabled on both devices, sharing the same accurate external clock provided by the MCU on CLKIN pin: in this way, after locking time, the two internal oscillators will have the same frequency, apart from the frequency loop error. In order to recover the residual frequency error and to control the phases between master and slave devices, a synchronization pulse is provided by the master every multiple N of switching timebase period T_{SW} (see Figure 19 and Figure 20 below); N is user programmable via global SPI (range: 1 to 31, 0 is invalid so the TSW keeps the last value), by writing into the bit CLKSW_PERIOD of the register CLK_CTRL.The phase delay φ between master and slave is user programmable via global SPI (range: 0 to 7), by writing into the bit SLAVE_PH_SEL of register PWR_CTRL_1.

Figure 19. **Delay between switching regulator phases**

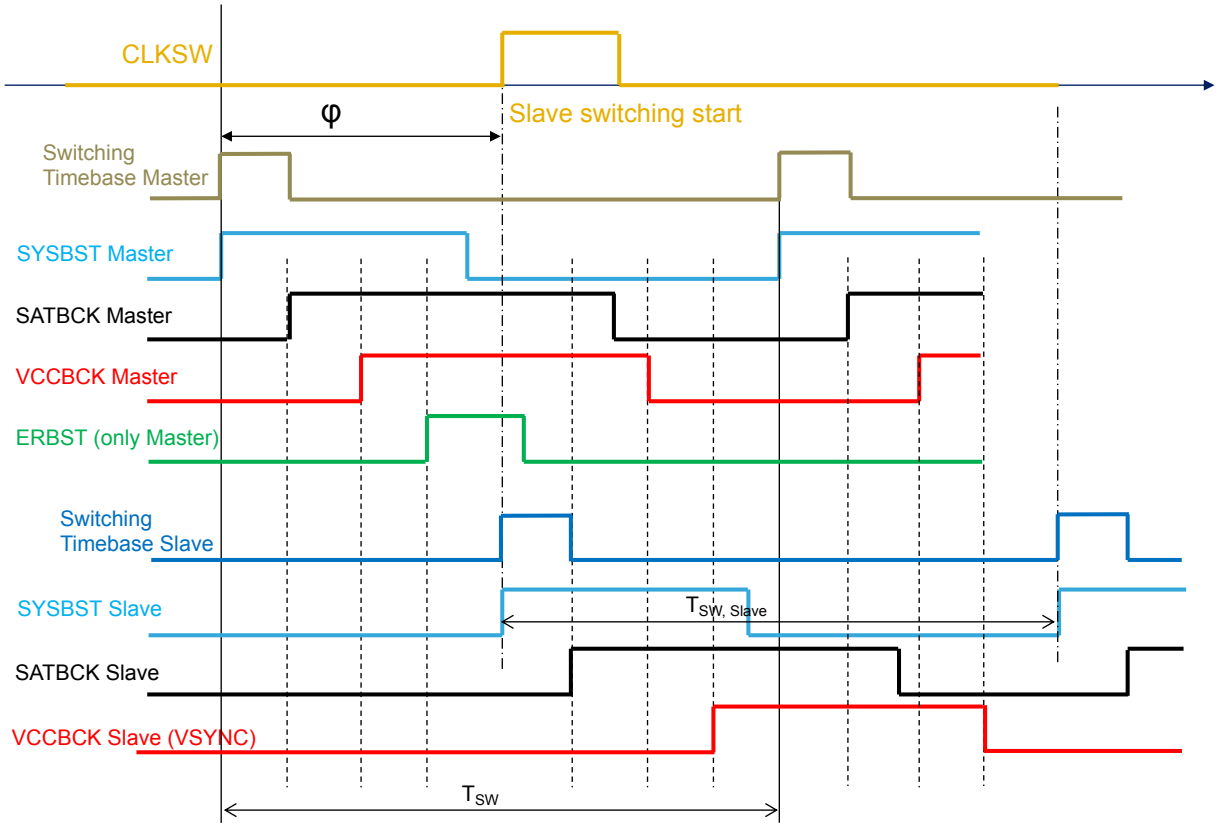
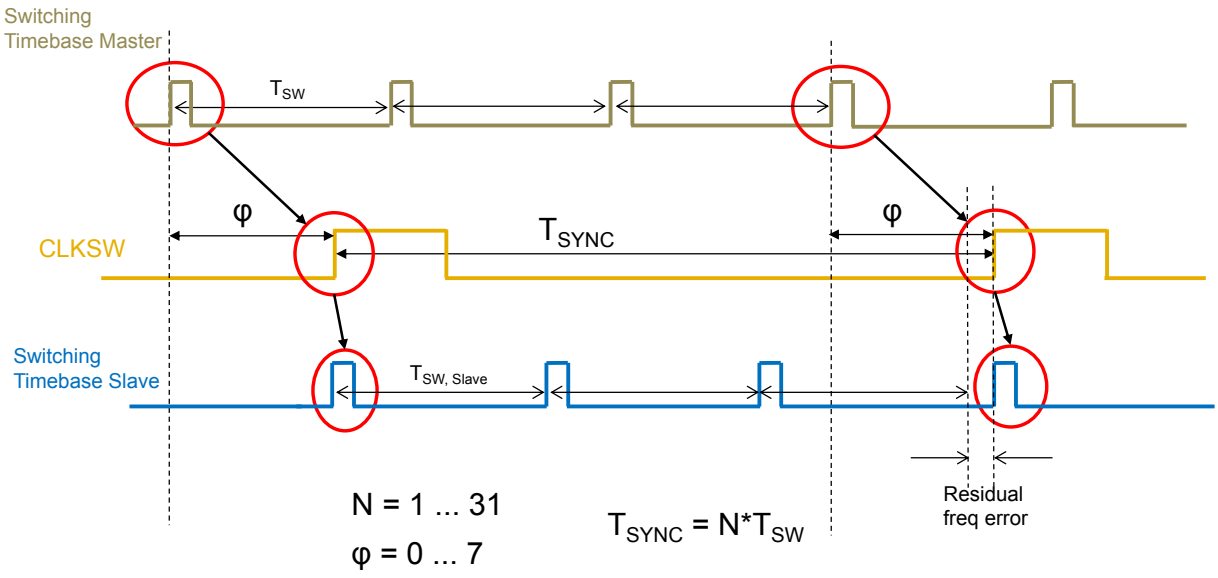


Figure 20. **CLKSW synchronization**



The switching regulators are enabled on both devices, following startup sequence, with default phases.

When RESET_N is released, the MCU can send SPI frames to select different phases for the regulators of each device, if needed: up to now, power MOS switching edge times can be controlled for each single device, but there is no control among master and slave.

After the MCU writes CLKSW_EN in CLK_CTRL register, the master starts to send the synchronization pulse, and the slave starts to use the synchronization pulse received on CLKIN pin, adjusting its switching timebase immediately (therefore, only one 2 MHz-period for slave switching regulators will be affected by this transition).

In case of frequency error or RESET_N = 0, the FLL function does not work, therefore the MCU stops sending the pulse to CLKIN and the slave will mask any signal detected on its CLKIN pin. If slave device loses CLKSW signal, it continues its switching functionality without any timebase update (as done during power-up phase); if no synchronization pulse is received on CLKSW within (N + 1)* $T_{SW, Slave}$, slave activates CLKSW masking and bit CLKSW_ERR into CLK_CTRL register will be set; switching functionality is guaranteed by slave internal counter.

4.5 Watchdog

The temporal watchdog ensures that the system software is operating correctly by requiring periodic service from the microcontroller at a programmable rate. This service (watchdog refresh) must occur within a SPI programmable time window, and if serviced too early or too late will enter an error state. If the device is in SLAVE mode, the device enters and will remain in WSM_Reset state (and WD_LO is set to '0'), where watchdog operation is under reset. The overall WD functionality is described in the state diagram shown in Figure 21 below.

Figure 21. Temporal watchdog state diagram

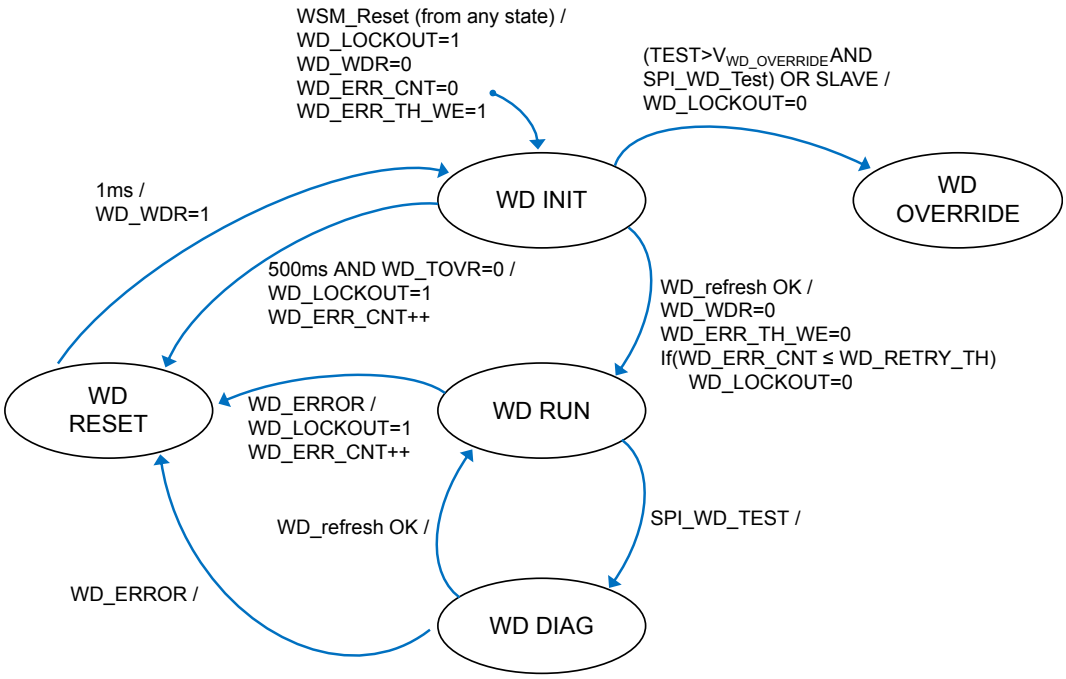


Table 6. Watchdog state description

State/Signal	Description
WD INITIAL	Default state entered from startup. While in this state, no watchdog service is required, and the IC may stay in this state indefinitely. For system safety, all arming signals are disabled during this state to prevent deployment.
WD RUN	Normal runtime state where WD service is required.
SLAVE	Signal or status bit to indicate MASTER or SLAVE configuration.
WD TEST	A special state used to test the watchdog function. Normally, this state will only be checked once per power cycle by the software, but there is no inherent restriction in the watchdog logic preventing periodic testing. This state allows testing of the watchdog, which can only be cleared via WSM reset. Deployment is inhibited when the WD state machine is in this state.
WD RESET	State entered when a WD_ERROR occurs. This is a timed-duration state that is automatically exited after 1 ms.
WD OVERRIDE	A special state used to disable watchdog functionality for development purposes. Other logic within the IC can use this state to emulate the WD RUN state without the need to service WD.

State/Signal	Description
WSM_Reset	Signal used to reset the WD state machine to the WD INITIAL state and all signals to their inactive values. It sets also WD RESET bit in DEVICE_STATUS register. WD state when the device is configured as slave.
WD_refresh OK	Signal that is asserted only if the watchdog is refreshed ('A' - 'B' or 'B' - 'A' seq.) within the WD time window.
WD_ERROR	Signal that is asserted if the watchdog refresh fails to occur during the WD time window.
WD_WDR	Watchdog reset - latched signal that is activated whenever a watchdog error is qualified. For WD, this occurs when WD service is required, but not received. This signal is SPI-readable.
WD_TM	Test mode - a signal that indicates that WD is being tested. This signal is SPI-readable.
WD_LOCKOUT	A latched signal activated if an unexpected WD error occurs. This signal is permanently latched when set (until WSM_RESET). When set, all arming signals are disabled, preventing deployment. This signal is SPI-readable.
SPI_WD_TEST	SPI command used to enter WD TEST state from WD RUN state, or to enter WD OVERRIDE state from INITIAL state if TEST pin voltage is greater than the threshold $V_{WD\_OVERRIDE}$. This command has no effect in other states.

4.5.1 Watchdog timer configuration

The watchdog timer can be configured for two different frequency modes:

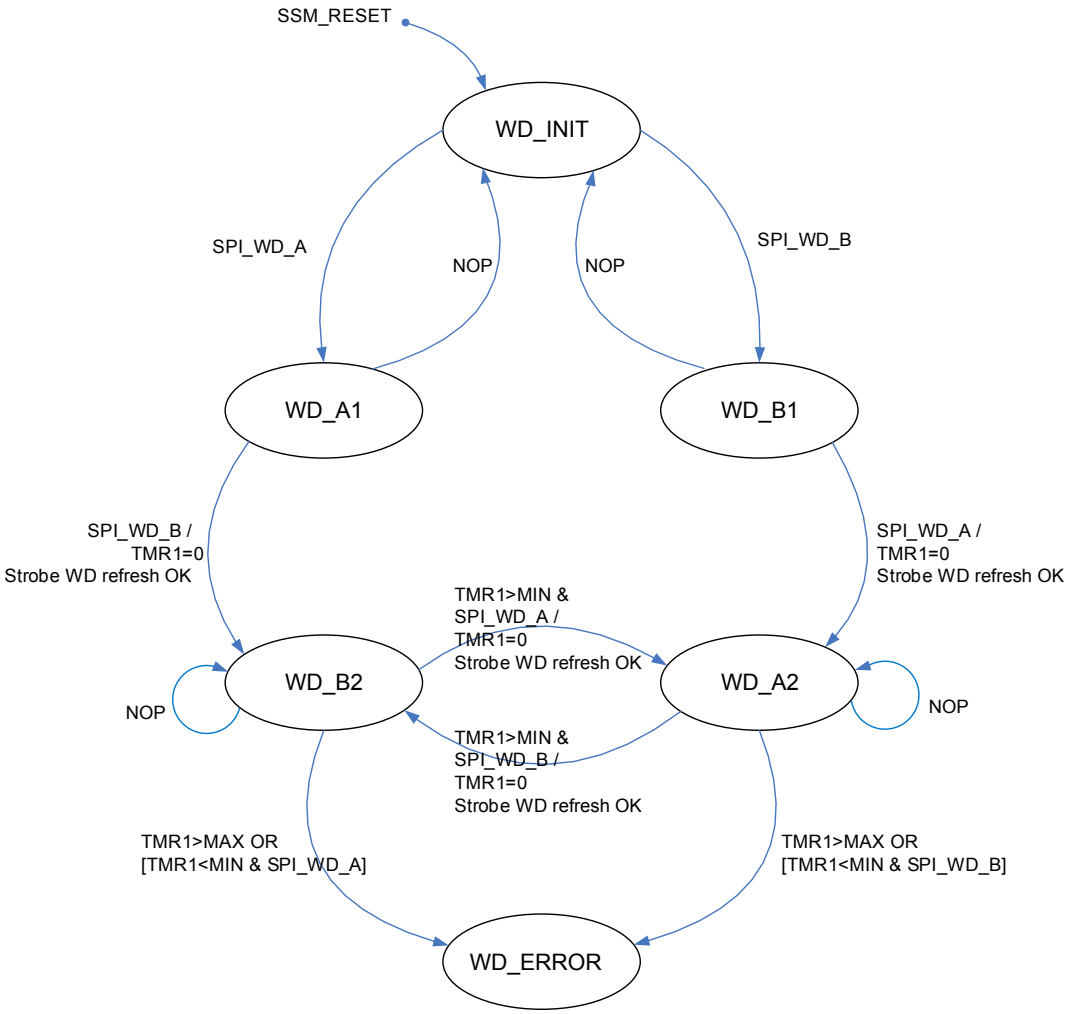
- Fast with maximum range of 2 ms and a resolution of 8 µs;
- Slow with maximum range of 16.3 ms and a resolution of 64 µs.

The watchdog window times are SPI programmable by setting the WD_CFG_0 register. Configuration is accepted only when the device is in the INIT state. Once the device enters in DIAG state, watchdog control is enabled, configuration is fixed and cannot be modified.

4.5.2 Watchdog timer operation

Watchdog state diagram operation is shown in Figure 22.

Figure 22. Watchdog timer refresh diagram



In the WD initial state, watchdog service must begin within the first 500 ms, or a SPI command with WD_TIMEOUT_DISABLE = 1 in the WD_CTRL_1 must be received to disable the timeout and keep the device in the INIT state indefinitely without watchdog service. To refresh the WD, the logic must receive a SPI command with the expected key value within the time window (WDTMIN + WDTDELTA) set in the WD_CFG_0 register. If the command is received too early or too late, the WD_ERROR signal will be asserted.

This error will not be asserted if an incorrect key value is received in the correct time window, allowing the MCU to repeatedly transmit the key value until the correct value is sent. Upon reception of the correct key within the window, the WD logic reset a new time window. This time is properly cleared upon writing code ‘A’ and code ‘B’ (‘A’ – ‘B’ or ‘B’ – ‘A’ sequences) to the WDCTL[1:0] bits in the WD_CTRL_0 register (other codes different from A or B are defined as NOP). The watchdog timer WD_TIMER can be read in the same register.

If WD_ERR_CNT > WD_RETRY_TH, WD_ERR_LATCHED signal is set to 1 and can be reset only by RESET_1_N. This function can be enabled by NVM. The configuration WD_RETRY_TH can be written only in INIT after power-up. If the device come back in INIT due to a RESET_N, it is not possible to update WD_RETRY_TH.

When the watchdog enters in WD TEST state, it needs a right A or B code to return in WD RUN state. If this doesn't occur, that is WD_ERROR signal is asserted, watchdog enters in WD RESET state and then in WD INITIAL state, latching WD_WDR bit in WD_STATUS Global SPI register.

4.5.3 Watchdog reset assertion timer

Upon watchdog reset, the watchdog logic will momentarily assert the RESET_N pin for t_{WDT_RST}. When the RESET pin is asserted by the watchdog reset assertion timer, stored faults are maintained and can be read by the microcontroller via SPI following the RESET period.

4.6 Reset control

The device provides reset logic to safely control system operation in the event of internal ECU failures. Several internal reset signals are generated depending on the type of failure detected. The list of internal resets is shown in Table 7.

Table 7. Reset list

LIST OF RESET	RST SOURCES
RESET_1_N	Digital POR
RESET_2_N	Digital POR Analog POR Freq err (not latched, internal oscillator)
RESET_3_N (WSM_RESET)	Dig POR Analog POR Freq err (not latched, internal oscillator) VCCBCK OV/UV CLKIN fault
RESET_4_N (SSM_RESET)	Dig POR Analog POR Freq err (not latched, internal oscillator) VCCBCK OV/UV CLKIN fault SW_RESET_CTRL(SOFT_RESET_CMD) WD RESET STATE WD_ERR_LATCHED RST_N_MASTER&&SLAVE

Four internal reset signals are generated by the device:

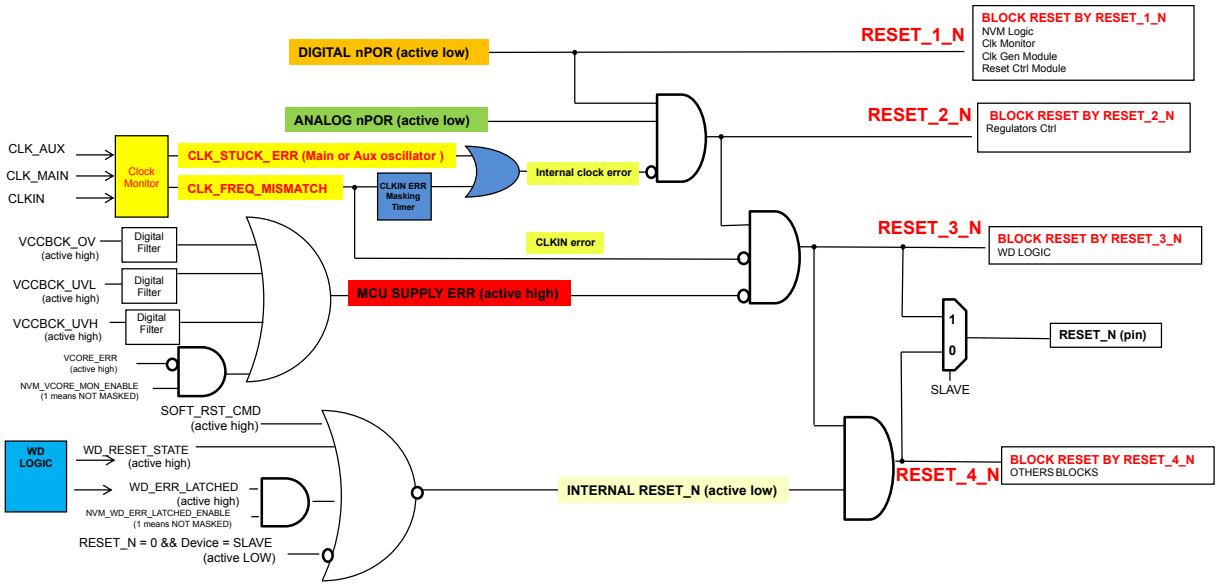
- RESET_1_N: this reset is asserted when a failure is detected in the internal digital supplies circuits. When active, all other resets are asserted.
- RESET_2_N: this reset is asserted when a failure is detected in the internal analog supplies or in case of clock monitor error detection (internal oscillator main or aux). When active, also RESET_3_N and RESET_4_N are asserted.
- RESET_3_N (WSM_RESET, watchdog state machine reset): this reset is generated when a failure is detected in the VCC supply or in case of CLKIN fault.

  In case of CLKIN fault, clock monitor detects a fault due to a frequency mismatch and the FLL is automatically disabled. This error is masked for 1 ms (CLKIN ERR masking timer) and RESET_3_N asserted for the same time. When the masking time expired, the RESET_3_N will be released. When active, also RESET_4_N is asserted.
- RESET_4_N (SSM_RESET, safety state machine reset): this reset is asserted when a failure is detected in watchdog logic or in case of SOFT_RESET_CMD is set (in case of SOFT_RESET_CMD, the RESET_N assertion is equal to t_{HOLD_RESET}) or in case of RESET_N_MASTER only in slave configuration.

  The RESET_4 drives RESET_N, the active-low signal driven on the output pin. The reset pin is output only with push-pull capability when the device is configured as master. When the device is configured as slave, the RESET_N pin is reconfigured as open drain with pull-down resistor and input capability.

The reset logic shall be controlled as shown in Figure 23:

Figure 23. Reset logic



4.7 Digital I/O

The digital pins of L9691 are described in Table 8. The drive strength of SPI_MISO_G and SPI_MISO_RS are configurable trough the field DIG_IO_SPEED in DEVICE_CTRL Global SPI register.

Table 8. Digital pins description

Pin	Type	Driving
SPI_MISO_RS	I/O	Push-pull buffer
SPI_MOSI_RS	I	Resistive pull-down 100 kΩ
SPI_SCLK_RS	I	Resistive pull-down 100 kΩ
SPI_CS_RS	I	Resistive pull-up 100 kΩ
SPI_MISO_G	I/O	Push-pull buffer
SPI_MOSI_G	I	Resistive pull-down 100 kΩ
SPI_SCLK_G	I	Resistive pull-down 100 kΩ
SPI_CS_G	I	Resistive pull-up 100 kΩ
CLKIN	I	Resistive pull-down 100 kΩ
ARM_CS_G	I	Resistive pull-up 100 kΩ
SPI_CS_SAF4	I	Resistive pull-up 100 kΩ
SPI_CS_SAF3	I	Resistive pull-up 100 kΩ
SPI_CS_SAF2	I	Resistive pull-up 100 kΩ
SPI_CS_SAF1	I	Resistive pull-up 100 kΩ
SPI_CS_SAF0	I	Resistive pull-up 100 kΩ
COVRACT	I/O	Resistive pull-down 100 kΩ + push-pull buffer
CLKSW	I/O	Resistive pull-down 100 kΩ + push-pull buffer
LIN_RX	I/O	Resistive pull-up 100 kΩ + push-pull buffer

Pin	Type	Driving
LIN_TX	I	Resistive pull-up 100 kΩ
RESET_N	I/O	Resistive pull-down 100 kΩ + push-pull buffer

4.8 Non volatile memory (NVM)

The device contents a 2 Kbits non volatile memory (NVM) that can be read and write using the control register of SPI. The NVM is divided internally in 16 sectors each of 128 bit (120 data bit and 8 CRC bit to cover that sector), but 1 sector can be programmed by user to configure the device.

By the reading instruction using the control register (NVM_READ_CTRL), the download data from the NVM area is stored in internal trimming registers. MCU can read the user trimming bits in NVM_BYTEx_STATUS. By the writing instruction using the control register (NVM_WRITE_CTRL), the data stored in the SPI data register (NVM_BYTEx_CFG) is uploaded to the NVM area and, when the operation is completed, a read operation starts automatically. The whole operation required about 12 ms. NVM area by customer can be written maximum 15 times, and in case of this limit is reached the NVM_WRITE_STATE is set to 1. When this bit is set, any NVM writing is not reliable.

The user sector is divided in:

- NVM_BYTE_x: 16 bits that can be configured by the user following the procedure subsequently described
- RESERVED BITS: 100 bits reserved
- UPLOAD COUNTER: 4 bits, a rewrite counter (default value 15) manages the number of rewrites on the user sector. The upload counter starts from 1111 and it is automatically decremented by writing command. As soon as the counter is equal to 0000 NVM_WRITE_STATE register is set. In this condition the NVM upload is still possible, but the data integrity is not guaranteed.
- CRC: 8 bits to cover the whole user sector. That CRC is computed automatically after that the writing is authorized and then is checked when the sector has been read. In case of CRC error DEVICE_STATUS(NVM_USER_CRC_ERROR) is set and the user bits are set to 0.

Figure 24. NVM user sector

The user trimming bits are:

- MASTER/SLAVE configuration: 000 = master, 111 = slave.
- VCOREMON enable: 0 = disable, 1 = enable.
- SATBCK value: 0- = 8 V, 1 = 6.5 V.
- VCCBCK FDM: 0 = disable, 1 = enable.
- E2E background CRC disable: 0 = enable, 1 = disable.
- LIN background CRC disable: 0 = enable, 1 = disable.
- WD_ERR_LATCHED enable: 0 = disable, 1 = enable.
- WU_WALID_FLT_SHTDW disable: 0 = enable, 1 = disable.
- SEL_STG_THRESH: 0 = $t_{FLT\_OCTH\_RSU\_LONG}$, 1 = $t_{FLT\_OCTH\_RSU\_SHORT}$.
- BASE_LPF_FREQ_CTRL.
- THRESH_HIST_EN: 0 = disable, 1 = enable.
- ISCR_SR_SEL: 0 = SR_{ISRCx_SLOW}, 1 = SR_{ISRCx_FAST}.
- ERBOOST_PLS_SKIP_BLK_SEL: 0 = 100 µs, 1 = 50 µs.
- ERBOOST_PLS_SKIP_DIS: 0 = enable, 1 = disable.

These bits can be configured using the NVM_BYTE01_CFG global SPI register.

At power-up all the NVM content is stored in trimming registers. The user trimming bits are equal to 0, so the device is set as master.

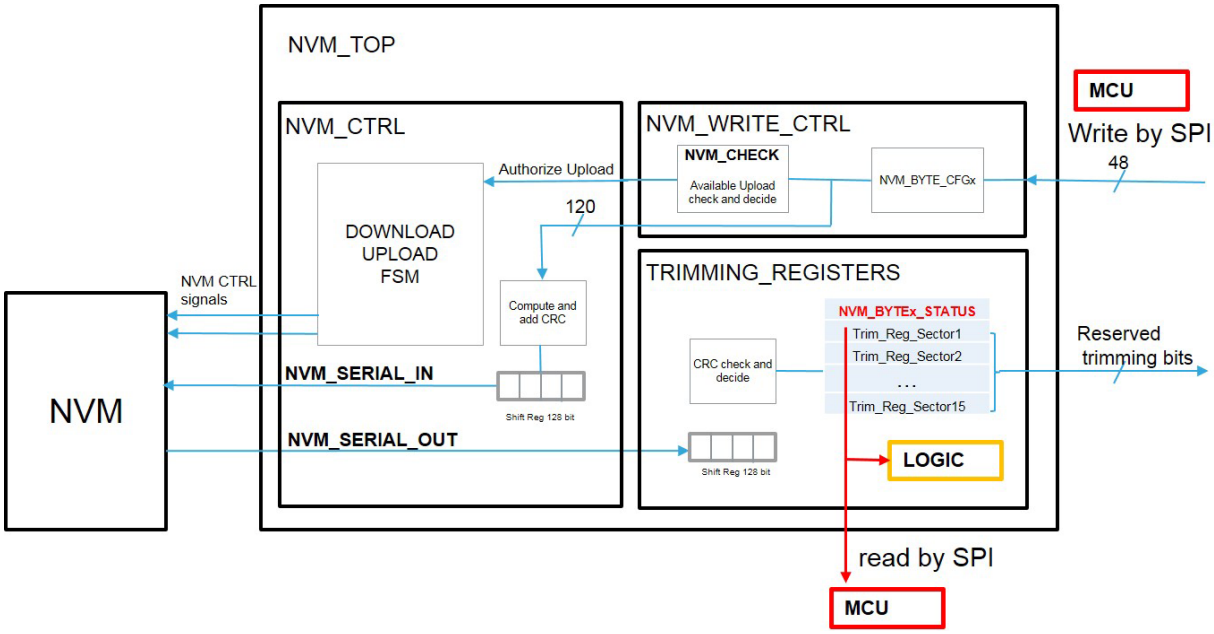
To program the user trimming bits, the procedure is the following:

1. MCU writes the configuration in NVM_BYTEx_CFG registers (48 bits → 3 SPI registers).
2. MCU sends NVM_WRITE_CTRL(WRITE_TO_NVM) command to initialize the write operation.
3. Before to authorize, the NVM_CHECK block checks the CRC error status (previous NVM reading). If some checks fail, authorize upload is not set, so the trimming data is not updated.
4. If check is ok, the upload is authorized and programming counter is decreased.
5. NVM_BYTE_CFGx along with the upload counter and reserved bits is ready to copy in the NVM.
6. The CRC (8 bits) is computed on the whole sector and then data is transferred inside the NVM.
7. When the NVM writing is completed, an automatic reading is executed in order to refresh trimming bits. MCU can check the applied configuration reading NVM_BYTEx_STATUS register.
8. The flag NVM_READY is 1 during the upload phase of NVM, which lasts about 10 ms (typ), and is reset to 0 during the download in the trimming registers of the new uploaded values. The download phase lasts about 650 µs (typ) and at the end NVM_READY is set back to 1.

The writing operation is possible only on all 16 bits (not single bit): MCU has to write again bits that have already programmed in a previous upload operation.

Moreover, it is possible to read the DIE_ID info stored in NVM by using NVN_DIE_ID_PTx SPI registers.

Figure 25. NVM control logic



5 Serial peripheral interface (SPI)

The L9691 uses two SPI interfaces: Global SPI and remote sensor SPI.

The global SPI interface provides general configuration, control, and status functions for the device.

The remote sensor SPI provides dedicated access to satellite interface (remote sensor data, status, and configuration registers) and is used by the MCU to communicate with digital sensors.

Both SPI interfaces have dedicated SCLK, MOSI and MISO interface pins and diagnostics for clock count checking, parity or CRC errors and incorrect register access. The IC maintains MISO in tri-state while CS is inactive.

The communications is controlled through SPI_CS_X, enabling and disabling communication. When SPI_CS_X is at logic high, all SPI communication I/O is tri-stated and no data is accepted. When SPI_CS_X is low, data is latched on the rising edge of SCLK_X and data is shifted on the falling edge (CPOL = 0, CPHA = 0). The SPI_MOSI_X pin receives serial data from the master with MSB first. Likewise for SPI_MISO_X, data is read MSB first, LSB last.

The sequential transfer delay (T_{NODATA}) occurs between each transfer frame. The device uses this delay to write data to a register and to confirm framing errors. Write and read are applied to the internal registers in the same clock cycle at the end of the frame, and in case of write access the next MISO will report the data contents before the write.

5.1 Global SPI protocol

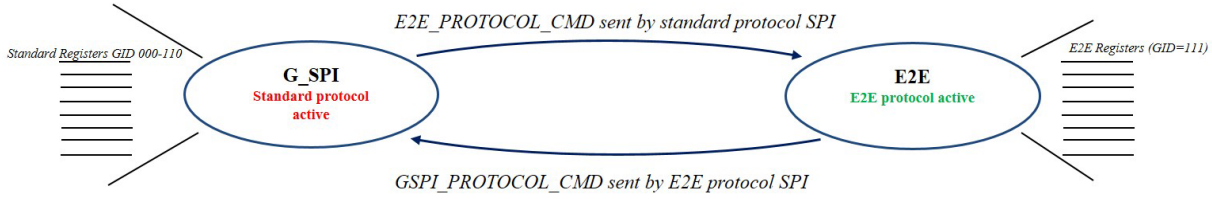
Global SPI interface is a 32-bit in-frame communication bus with a single CS and 1-bit odd parity. Both parity and clock cycle errors result in the GSW(SPI_FLT = 1), while attempts to access invalid or forbidden registers addresses does not set a fault, access is denied. There are two frame formats:

- Standard (in-frame response)
- E2E (end to end communication, out-of-frame response)

To change format, the following procedure is required:

- From standard to E2E: it is required E2E_PROTOCOL_CTRL(E2E_PROTOCOL_CMD) with standard access to activate E2E protocol. Response for this command will be the in-frame response for the E2E_PROTOCOL_CTRL command.
- From E2E to standard: it is required a GSPI_PROTOCOL_CTRL(GSPI_PROTOCOL_CMD) with E2E protocol to activate standard protocol. Response for this command will be returned on the first E2E MISO response after the next E2E protocol activation.

Figure 26. Change protocol diagram



5.1.1 Global standard SPI format

This format is available anytime and is used for general communication between the system µC and L9691. The IC SPI interface is composed by an input shift register, an output shift register and four control signals. SPI_MOSI_G is the data input to the input shift register. SPI_MISO_G is the data output from the output shift register. SPI_SCLK_G is the clock input used to shift data into the input shift register or out from the output one while SPI_CS_G is the active low chip select input. All SPI communications are executed in exact 32 bit increments. The general format of the 32 bit transmission for the SPI interface is shown in Table 9.

Table 9. Global standard SPI format, 32-bit in-frame protocol

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI_G	GID			RID						WID						WPAR	WRITE DATA															
MISO_G	GSW															RPAR	READ DATA															

Data sent to the IC consists of a target read register ID (GID and RID), a target write register ID (GID and WID), write data parity (WPAR) and 16 bits of data (WRITE). WRITE data is the data to be written to the target write register indicated by the write address. Data returned from the IC consists of a global status word (GSW), read data parity (RPAR) and 16 bits of data (READ). READ DATA is the contents of the target read register as indicated by the read address. The parity bits WPAR and RPAR cover all the 32 bits of the MOSI and MISO frames, respectively. Odd parity type is used.[end]

Table 10 and Table 11 describe the SPI_G bits:

Table 10. SPI_G field description

	Field	Description
SPI_G_MOSI		
[31:29]	GID	Global ID - appended to WID and RID to generate 9 bit address
[28:23]	RID	Read ID - address for in-frame register read operation
[22:17]	WID	Write ID - address for register write operation
[16]	WPAR	Write parity - odd parity on MOSI[31:0]
[15:0]	WRITE DATA	Write data to be written to address → GID and WID
SPI_G_MISO		
[31:17]	GSW	Global status word
[16]	RPAR	Read parity - odd parity on MISO[31:0]
[15:0]	READ DATA	Read data - in-frame data read from address → GID and RID

Table 11. SPI_G GSW field description

SPI_MISO_G	GSW	Name	Description
31	14	SPIFLT	SPI fault, set if previous SPI frame had wrong parity check or wrong number of bits: 0 = No fault 1 = Fault
30	13	NVM_ERR	NVM CRC error: 0 = CRC_CHECK is passed when the EEPROM is downloaded 1 = CRC_CHECK is NOT passed when the EEPROM is downloaded
29	12	BKG_MON_ERR	Background monitoring fault: 0 = No fault 1 = At least one test is failed
28	11	TM_PIN	State of TEST pin: 0 = TEST < $V_{WD\_DIS\_TH}$ 1 = TEST > $V_{WD\_DIS\_TH}$
27	10	ERSTATE	Set when power mode state machine is in ER state: 0 = Powermode state machine is not in ER state 1 = Powermode state machine is in ER state

SPI_MISO_G	GSW	Name	Description
26	9	POWERFLT	Fault present in PWR_STATUS_x register, logical OR between bits that report FAULT in power supply section: 0 = no fault 1 = fault
25	8	LBIST_FLT	Logic BIST fail: 0 = All the LBIST tests are ok 1 = At least one of LBIST test fails
24	7	MBIST_FLT	Memory BIST fail: 0 = MBIST passed 1 = MBIST failed
23	6	RAM_CRC_ERR	RAM_CRC_ERR: 0 = No RAM CRC error 1 = RAM CRC error
22	5	ER_DIAG_RUNNING	ERCAP DIAG RUNNING: 1 = ER cap diag is running
21	4	ADC_DEP_BUSY	Deployment ADC status: 1 = Dep ADC is busy and a new conversion request is rejected
20	3	SYSBST_DLOSS	0 = No SYSBST diode loss 1 = SYSBST diode loss
19	2	ERBST_DLOSS	0 = No ERBST diode loss 1 = ERBST diode loss
18	1	ERR_WID	Write address of previous SPI frame is not permitted in current operating phase: 0 = No error 1 = Error
17	0	ERR_RID	Read address received in the actual SPI frame is unused so data in the response is “don't care”: 0 = No error 1 = Error

The device checks the validity of the received write address and read address in the MOSI_G frame:

- ERR_WID: SPI write command with WID matching a writable register is received in an illegal state. The command is discarded and the ERR_WID bit will be flagged in the next global status word (GSW). The ERR_WID flag is not set in case WID is addressing a read/only register.
- ERR_RID: SPI read command contains an unused GID||RID address. The command is discarded and the ERR_RID bit will be flagged in the current global status word (GSW). The data field for the in-frame SPI response will be set to all 0’s.
- SPI_FLT: In case frame length long or short, or in case of parity error detected on MOSI frame, this flag is set. The SCLK input counts the number of received clocks and if the clock counter exceeds or counts fewer than 32 clocks, the received message is discarded and the SPI_FLT bit is flagged in the global status word (GSW). Any attempt to access to a register with forbidden access mode (read or write) is not leading to changes to the internal registers but the SPI_FLT bit is not set in this case. All global SPI commands containing a GID = ‘111’ while the standard protocol is active will be discarded and an ERR_RID will be generated.

5.1.2 Global standard SPI registers map

Note:

- *RO: READ ONLY*
- *RLR: READ LATCH UNTIL READ (clear on read)*
- *RW: READ/WRITE*
- *WO: WRITE ONLY (data read from WO registers/bits cannot necessarily be trusted except for ones indicated in register map description as "WO exception")*
- *RWL: CLEAR ON WRITE (the register is cleared writing '1' in the relative field)*

Table 12. SPI_G_MAP_intro

Register name	Address (HEX)	GID	Init	Diag	Safing	Scrap	Arming safing	Arming scraping
PWR_STATUS_0	0x001	000						
PWR_CTRL_0	0x002	000	x	x	x	x	x	x
PWR_CTRL_1	0x003	000	x	x	x	x	x	x
SHUTDOWN_CTRL	0x004	000	x	x	x	x	x	x
OFF_CTRL	0x005	000	x	x	x	x	x	x
DEVICE_STATUS	0x006	000						
DEVICE_CTRL	0x007	000	x	x				
NVM_WRITE_CTRL	0x008	000	x	x				
NVM_READ_CTRL	0x009	000	x	x				
NVM_BYTE01_CFG	0x00A	000	x	x				
NVM_BYTE01_STATUS	0x00B	000						
NVM_DIE_ID_PT1	0x00C	000						
NVM_DIE_ID_PT2	0x00D	000						
NVM_DIE_ID_PT3	0x00E	000						
NVM_DIE_ID_PT4	0x00F	000						
LBIST_CTRL	0x010	000	x	x				
CLK_CTRL	0x011	000	x	x				
PWR_STATUS_1	0x012	000						
PWR_STATUS_2	0x013	000						
WD_CFG_0	0x014	000	x					
WD_CTRL_0	0x015	000	x	x	x	x	x	x
WD_CFG_1	0x016	000	x					
WD_STATUS	0x017	000						
WD_CTRL_1	0x018	000	x	x	x	x	x	x
PWR_ADC_A	0x019	000	x	x	x	x	x	x
PWR_ADC_B	0x01A	000	x	x	x	x	x	x
PWR_ADC_C	0x01B	000	x	x	x	x	x	x
PWR_ADC_D	0x01C	000	x	x	x	x	x	x
ER_CAP_DIAG_ESR_STATUS	0x01D	000						
ER_CAP_DIAG_CAP_STATUS	0x01E	000						
ER_CAP_DIAG_STATUS_0	0x01F	000						
ER_CAP_DIAG_STATUS_1	0x020	000						

Register name	Address (HEX)	GID	Init	Diag	Safing	Scrap	Arming safing	Arming scraping
ER_CAP_DIAG_STATUS_2	0x021	000						
ER_CAP_DIAG_STATUS_3	0x022	000						
ER_CAP_DIAG_CTRL	0x023	000	x	x	x	x	x	x
SSM_CTRL	0x024	000	x	x	x	x	x	x
SAFING_SCRAP_CTRL	0x025	000	x	x	x	x	x	x
SCRAP_CTRL	0x026	000				x		x
ACL_PSINH_STATUS	0x027	000						
ARM_PSINH_INT_STATUS	0x028	000						
ARM_PSINH_EXT_STATUS	0x029	000						
ARM_E2E_STATUS	0x02A	000						
ARM_PSINH_MCU2_STATUS	0x02B	000						
MCU2_RESERVED_ADDRESS	0x02C	000						
ARM_PSINH_MCU2_CTRL	0x02D	000	x	x				
SW_RESET_CTRL	0x02E	000	x	x	x	x	x	x
E2E_PROTOCOL_CTRL	0x02F	000	x	x	x	x	x	x
SNOOPING_TEST_INT	0x030	000	x	x	x	x	x	x
SNOOPING_TEST_EXT	0x031	000						
E2E_CRC_CTRL	0x032	000	x	x				
DEVICE_ID	0x033	000						
NOP_GID_000	0x03F	000						
DCS_ENG0_CTRL	0x040	001	x	x	x	x	x	x
DCS_ENG1_CTRL1	0x041	001	x	x	x	x	x	x
DCS_DIAG_CFG	0x042	001	x	x	x	x	x	x
DCS_ADC_A	0x043	001	x	x	x	x	x	x
DCS_ADC_B	0x044	001	x	x	x	x	x	x
DCS_ADC_C	0x045	001	x	x	x	x	x	x
DCS_ADC_D	0x046	001	x	x	x	x	x	x
GPO0_CTRL	0x047	001	x	x	x	x	x	x
GPO1_CTRL	0x048	001	x	x	x	x	x	x
GPO2_CTRL	0x049	001	x	x	x	x	x	x
GPO0_CFG	0x04A	001	x	x	x	x	x	x
GPO1_CFG	0x04B	001	x	x	x	x	x	x
GPO2_CFG	0x04C	001	x	x	x	x	x	x
LIN_OCS_MASK_PT0	0x04D	001		x				
LIN_OCS_MASK_PT1	0x04E	001		x				
LIN_OCS_MASK_PT2	0x04F	001		x				
LIN_OCS_MASK_PT3	0x050	001		x				
LIN_OCS_TGT1_PT0	0x051	001		x				
LIN_OCS_TGT1_PT1	0x052	001		x				
LIN_OCS_TGT1_PT2	0x053	001		x				

Register name	Address (HEX)	GID	Init	Diag	Safing	Scrap	Arming safing	Arming scraping
LIN_OCS_TGT1_PT3	0x054	001		x				
LIN_OCS_TGT2_PT0	0x055	001		x				
LIN_OCS_TGT2_PT1	0x056	001		x				
LIN_OCS_TGT2_PT2	0x057	001		x				
LIN_OCS_TGT2_PT3	0x058	001		x				
LIN_STATUS	0x059	001						
LIN_CFG	0x05A	001		x				
LIN_CRC_CTRL	0x05B	001	x	x				
PSINH_DCS_CFG	0x05C	001		x	x	x	x	x
PSINH_DCS0_TH_HI_SAMPLES_CFG	0x05D	001		x	x	x	x	x
PSINH_DCS0_TH_LO_CFG	0x05E	001		x	x	x	x	x
PSINH_DCS1_TH_HI_SAMPLES_CFG	0x05F	001		x	x	x	x	x
PSINH_DCS1_TH_LO_CFG	0x060	001		x	x	x	x	x
SAF_EN_CTRL_PT1	0x061	001		x	x	x	x	x
SAF_EN_CTRL_PT2	0x062	001		x	x	x	x	x
SAF_NODATA_STATUS_PT1	0x063	001						
SAF_NODATA_STATUS_PT2	0x064	001						
SAF_REC_ARM_STATUS_PT1	0x065	001						
SAF_REC_ARM_STATUS_PT2	0x066	001						
SAF_EVC_CFG	0x067	001		x				
SAF_CS0_CFG	0x068	001		x				
SAF_CS1_CFG	0x069	001		x				
SAF_CS2_CFG	0x06A	001		x				
SAF_CS3_CFG	0x06B	001		x				
SAF_CS4_CFG	0x06C	001		x				
SAF_CSX_CFG	0x06D	001		x				
NOP_GID_001	0x07F	001						
DEP_AUTOPROF_CFG	0x080	010		x	x	x	x	x
DEP_DIAG_ADC_A	0x081	010	x	x	x	x	x	x
DEP_DIAG_ADC_B	0x082	010	x	x	x	x	x	x
DEP_DIAG_CTRL_A	0x083	010		x	x	x	x	x
DEP_DIAG_CTRL_B	0x084	010		x	x	x	x	x
DEP_DIAG_STATUS_0	0x085	010						
DEP_DIAG_STATUS_1	0x086	010						
SS_PD_CTRL	0x087	010	x	x	x	x	x	x
SR_SF_PD_CTRL	0x088	010	x	x	x	x	x	x
VSF0_CTRL	0x089	010		x	x	x	x	x
VSF1_CTRL	0x08A	010		x	x	x	x	x
DEP_CMT_H_CTRL	0x08B	010	x	x				
DEP_CMT_L_CTRL	0x08C	010	x	x				

Register name	Address (HEX)	GID	Init	Diag	Safing	Scrap	Arming safing	Arming scraping
DEP_DWELL_CTRL	0x08D	010	x	x				
DEP_CMT_0	0x08E	010						
DEP_CMT_1	0x08F	010						
DEP_CMT_2	0x090	010						
DEP_CMT_3	0x091	010						
DEP_CMT_4	0x092	010						
DEP_CMT_5	0x093	010						
DEP_CMT_6	0x094	010						
DEP_CMT_7	0x095	010						
DEP_CMT_8	0x096	010						
DEP_CMT_9	0x097	010						
DEP_CMT_10	0x098	010						
DEP_CMT_11	0x099	010						
DEP_CMT_12	0x09A	010						
DEP_CMT_13	0x09B	010						
DEP_CMT_14	0x09C	010						
DEP_CMT_15	0x09D	010						
DEP_CFG_A	0x09E	010		x				
DEP_CFG_B	0x09F	010		x				
DEP_CFG_C	0x0A0	010		x				
DEP_CFG_D	0x0A1	010		x				
DEP_PROF1_MATRIX_L0_7	0x0A2	010		x	x	x	x	x
DEP_PROF1_MATRIX_L8_15	0x0A3	010		x	x	x	x	x
DEP_CTRL	0x0A4	010	x	x	x	x		
DEP_CMD	0x0A5	010			x		x	x
DEP_CMD_N	0x0A6	010			x		x	x
DEP_EN_CTRL	0x0A7	010			x		x	x
DEP_DIS	0x0A8	010		x	x		x	
LOOP_MATRIX_ARM0	0x0A9	010		x				
LOOP_MATRIX_ARM1	0x0AA	010		x				
LOOP_MATRIX_ARM2	0x0AB	010		x				
LOOP_MATRIX_ARM3	0x0AC	010		x				
LOOP_MATRIX_ARM4	0x0AD	010		x				
LOOP_MATRIX_ARM5	0x0AE	010		x				
LOOP_MATRIX_ARM6	0x0AF	010		x				
LOOP_MATRIX_ARM7	0x0B0	010		x				
LOOP_MATRIX_PSINH	0x0B1	010		x				
DEP_STATUS_0_7	0x0B2	010						
DEP_STATUS_8_15	0x0B3	010						
DEP_DIAG_SG_LOSS	0x0B4	010						

Register name	Address (HEX)	GID	Init	Diag	Safing	Scrap	Arming safing	Arming scraping
DEP_DIAG_OC	0x0B5	010						
DEP_AUTO_SAFE_CTRL	0x0B6	010	x	x				
DEP_DIAG_SS_OV	0x0B7	010						
DEP_DIAG_CHECK	0x0B8	010		x				
DEP_CRC_CTRL	0x0B9	010	x	x				
DEP_DIAG_SS_OV_DIS	0x0BA	010		x				
NOP_GID_010	0x0BF	010						
SAF_REC0_CTRL_PT1	0x0C0	011		x				
SAF_REC0_CTRL_PT2	0x0C1	011		x				
SAF_REC1_CTRL_PT1	0x0C2	011		x				
SAF_REC1_CTRL_PT2	0x0C3	011		x				
SAF_REC2_CTRL_PT1	0x0C4	011		x				
SAF_REC2_CTRL_PT2	0x0C5	011		x				
SAF_REC3_CTRL_PT1	0x0C6	011		x				
SAF_REC3_CTRL_PT2	0x0C7	011		x				
SAF_REC4_CTRL_PT1	0x0C8	011		x				
SAF_REC4_CTRL_PT2	0x0C9	011		x				
SAF_REC5_CTRL_PT1	0x0CA	011		x				
SAF_REC5_CTRL_PT2	0x0CB	011		x				
SAF_REC6_CTRL_PT1	0x0CC	011		x				
SAF_REC6_CTRL_PT2	0x0CD	011		x				
SAF_REC7_CTRL_PT1	0x0CE	011		x				
SAF_REC7_CTRL_PT2	0x0CF	011		x				
SAF_REC8_CTRL_PT1	0x0D0	011		x				
SAF_REC8_CTRL_PT2	0x0D1	011		x				
SAF_REC9_CTRL_PT1	0x0D2	011		x				
SAF_REC9_CTRL_PT2	0x0D3	011		x				
SAF_REC10_CTRL_PT1	0x0D4	011		x				
SAF_REC10_CTRL_PT2	0x0D5	011		x				
SAF_REC11_CTRL_PT1	0x0D6	011		x				
SAF_REC11_CTRL_PT2	0x0D7	011		x				
SAF_REC12_CTRL_PT1	0x0D8	011		x				
SAF_REC12_CTRL_PT2	0x0D9	011		x				
SAF_REC13_CTRL_PT1	0x0DA	011		x				
SAF_REC13_CTRL_PT2	0x0DB	011		x				
SAF_REC14_CTRL_PT1	0x0DC	011		x				
SAF_REC14_CTRL_PT2	0x0DD	011		x				
SAF_REC15_CTRL_PT1	0x0DE	011		x				
SAF_REC15_CTRL_PT2	0x0DF	011		x				
SAF_REC16_CTRL_PT1	0x0E0	011		x				

Register name	Address (HEX)	GID	Init	Diag	Safing	Scrap	Arming safing	Arming scraping
SAF_REC16_CTRL_PT2	0x0E1	011		x				
SAF_REC17_CTRL_PT1	0x0E2	011		x				
SAF_REC17_CTRL_PT2	0x0E3	011		x				
SAF_REC18_CTRL_PT1	0x0E4	011		x				
SAF_REC18_CTRL_PT2	0x0E5	011		x				
SAF_REC19_CTRL_PT1	0x0E6	011		x				
SAF_REC19_CTRL_PT2	0x0E7	011		x				
SAF_REC20_CTRL_PT1	0x0E8	011		x				
SAF_REC20_CTRL_PT2	0x0E9	011		x				
SAF_REC21_CTRL_PT1	0x0EA	011		x				
SAF_REC21_CTRL_PT2	0x0EB	011		x				
SAF_THRESHOLD_P_0	0x0EC	011		x				
SAF_THRESHOLD_P_1	0x0ED	011		x				
SAF_THRESHOLD_P_2	0x0EE	011		x				
SAF_THRESHOLD_P_3	0x0EF	011		x				
SAF_THRESHOLD_P_4	0x0F0	011		x				
SAF_THRESHOLD_P_5	0x0F1	011		x				
SAF_THRESHOLD_P_6	0x0F2	011		x				
SAF_THRESHOLD_P_7	0x0F3	011		x				
SAF_THRESHOLD_P_8	0x0F4	011		x				
SAF_THRESHOLD_P_9	0x0F5	011		x				
SAF_THRESHOLD_P_10	0x0F6	011		x				
SAF_THRESHOLD_P_11	0x0F7	011		x				
SAF_THRESHOLD_P_12	0x0F8	011		x				
SAF_THRESHOLD_P_13	0x0F9	011		x				
SAF_THRESHOLD_P_14	0x0FA	011		x				
SAF_THRESHOLD_P_15	0x0FB	011		x				
SAF_THRESHOLD_P_16	0x0FC	011		x				
SAF_THRESHOLD_P_17	0x0FD	011		x				
SAF_THRESHOLD_P_18	0x0FE	011		x				
NOP_GID_011	0x0FF	011						
SAF_THRESHOLD_P_19	0x100	100		x				
SAF_THRESHOLD_P_20	0x101	100		x				
SAF_THRESHOLD_P_21	0x102	100		x				
SAF_THRESHOLD_N_0	0x103	100		x				
SAF_THRESHOLD_N_1	0x104	100		x				
SAF_THRESHOLD_N_2	0x105	100		x				
SAF_THRESHOLD_N_3	0x106	100		x				
SAF_THRESHOLD_N_4	0x107	100		x				
SAF_THRESHOLD_N_5	0x108	100		x				

Register name	Address (HEX)	GID	Init	Diag	Safing	Scrap	Arming safing	Arming scraping
SAF_THRESHOLD_N_6	0x109	100		x				
SAF_THRESHOLD_N_7	0x10A	100		x				
SAF_THRESHOLD_N_8	0x10B	100		x				
SAF_THRESHOLD_N_9	0x10C	100		x				
SAF_THRESHOLD_N_10	0x10D	100		x				
SAF_THRESHOLD_N_11	0x10E	100		x				
SAF_THRESHOLD_N_12	0x10F	100		x				
SAF_THRESHOLD_N_13	0x110	100		x				
SAF_THRESHOLD_N_14	0x111	100		x				
SAF_THRESHOLD_N_15	0x112	100		x				
SAF_THRESHOLD_N_16	0x113	100		x				
SAF_THRESHOLD_N_17	0x114	100		x				
SAF_THRESHOLD_N_18	0x115	100		x				
SAF_THRESHOLD_N_19	0x116	100		x				
SAF_THRESHOLD_N_20	0x117	100		x				
SAF_THRESHOLD_N_21	0x118	100		x				
SAF_FOC_SEEDVAL_0	0x119	100		x				
SAF_FOC_SEEDVAL_1	0x11A	100		x				
SAF_FOC_SEEDVAL_2	0x11B	100		x				
SAF_FOC_SEEDVAL_3	0x11C	100		x				
SAF_FOC_SEEDVAL_4	0x11D	100		x				
SAF_FOC_SEEDVAL_5	0x11E	100		x				
SAF_FOC_SEEDVAL_6	0x11F	100		x				
SAF_FOC_SEEDVAL_7	0x120	100		x				
SAF_FOC_SEEDVAL_8	0x121	100		x				
SAF_FOC_SEEDVAL_9	0x122	100		x				
SAF_FOC_SEEDVAL_10	0x123	100		x				
SAF_FOC_SEEDVAL_11	0x124	100		x				
SAF_FOC_SEEDVAL_12	0x125	100		x				
SAF_FOC_SEEDVAL_13	0x126	100		x				
SAF_FOC_SEEDVAL_14	0x127	100		x				
SAF_FOC_SEEDVAL_15	0x128	100		x				
SAF_FOC_SEEDVAL_16	0x129	100		x				
SAF_FOC_SEEDVAL_17	0x12A	100		x				
SAF_FOC_SEEDVAL_18	0x12B	100		x				
SAF_FOC_SEEDVAL_19	0x12C	100		x				
SAF_FOC_SEEDVAL_20	0x12D	100		x				
SAF_FOC_SEEDVAL_21	0x12E	100		x				
SAF_REQ_TARGET_0_PT1	0x12F	100		x				
SAF_REQ_TARGET_0_PT2	0x130	100		x				

Register name	Address (HEX)	GID	Init	Diag	Safing	Scrap	Arming safing	Arming scraping
SAF_REQ_TARGET_1_PT1	0x131	100		x				
SAF_REQ_TARGET_1_PT2	0x132	100		x				
SAF_REQ_TARGET_2_PT1	0x133	100		x				
SAF_REQ_TARGET_2_PT2	0x134	100		x				
SAF_REQ_TARGET_3_PT1	0x135	100		x				
SAF_REQ_TARGET_3_PT2	0x136	100		x				
SAF_REQ_TARGET_4_PT1	0x137	100		x				
SAF_REQ_TARGET_4_PT2	0x138	100		x				
SAF_REQ_TARGET_5_PT1	0x139	100		x				
SAF_REQ_TARGET_5_PT2	0x13A	100		x				
SAF_REQ_TARGET_6_PT1	0x13B	100		x				
SAF_REQ_TARGET_6_PT2	0x13C	100		x				
SAF_REQ_TARGET_7_PT1	0x13D	100		x				
SAF_REQ_TARGET_7_PT2	0x13E	100		x				
NOP_GID_100	0x13F	100						
SAF_REQ_TARGET_8_PT1	0x140	101		x				
SAF_REQ_TARGET_8_PT2	0x141	101		x				
SAF_REQ_TARGET_9_PT1	0x142	101		x				
SAF_REQ_TARGET_9_PT2	0x143	101		x				
SAF_REQ_TARGET_10_PT1	0x144	101		x				
SAF_REQ_TARGET_10_PT2	0x145	101		x				
SAF_REQ_TARGET_11_PT1	0x146	101		x				
SAF_REQ_TARGET_11_PT2	0x147	101		x				
SAF_REQ_TARGET_12_PT1	0x148	101		x				
SAF_REQ_TARGET_12_PT2	0x149	101		x				
SAF_REQ_TARGET_13_PT1	0x14A	101		x				
SAF_REQ_TARGET_13_PT2	0x14B	101		x				
SAF_REQ_TARGET_14_PT1	0x14C	101		x				
SAF_REQ_TARGET_14_PT2	0x14D	101		x				
SAF_REQ_TARGET_15_PT1	0x14E	101		x				
SAF_REQ_TARGET_15_PT2	0x14F	101		x				
SAF_REQ_TARGET_16_PT1	0x150	101		x				
SAF_REQ_TARGET_16_PT2	0x151	101		x				
SAF_REQ_TARGET_17_PT1	0x152	101		x				
SAF_REQ_TARGET_17_PT2	0x153	101		x				
SAF_REQ_TARGET_18_PT1	0x154	101		x				
SAF_REQ_TARGET_18_PT2	0x155	101		x				
SAF_REQ_TARGET_19_PT1	0x156	101		x				
SAF_REQ_TARGET_19_PT2	0x157	101		x				
SAF_REQ_TARGET_20_PT1	0x158	101		x				

Register name	Address (HEX)	GID	Init	Diag	Safing	Scrap	Arming safing	Arming scraping
SAF_REQ_TARGET_20_PT2	0x159	101		x				
SAF_REQ_TARGET_21_PT1	0x15A	101		x				
SAF_REQ_TARGET_21_PT2	0x15B	101		x				
SAF_DATA_MASK_CS0_PT1	0x15C	101		x				
SAF_DATA_MASK_CS0_PT2	0x15D	101		x				
SAF_DATA_MASK_CS1_PT1	0x15E	101		x				
SAF_DATA_MASK_CS1_PT2	0x15F	101		x				
SAF_DATA_MASK_CS2_PT1	0x160	101		x				
SAF_DATA_MASK_CS2_PT2	0x161	101		x				
SAF_DATA_MASK_CS3_PT1	0x162	101		x				
SAF_DATA_MASK_CS3_PT2	0x163	101		x				
SAF_DATA_MASK_CS4_PT1	0x164	101		x				
SAF_DATA_MASK_CS4_PT2	0x165	101		x				
SAF_REQ_MASK_CS0_PT1	0x166	101		x				
SAF_REQ_MASK_CS0_PT2	0x167	101		x				
SAF_REQ_MASK_CS1_PT1	0x168	101		x				
SAF_REQ_MASK_CS1_PT2	0x169	101		x				
SAF_REQ_MASK_CS2_PT1	0x16A	101		x				
SAF_REQ_MASK_CS2_PT2	0x16B	101		x				
SAF_REQ_MASK_CS3_PT1	0x16C	101		x				
SAF_REQ_MASK_CS3_PT2	0x16D	101		x				
SAF_REQ_MASK_CS4_PT1	0x16E	101		x				
SAF_REQ_MASK_CS4_PT2	0x16F	101		x				
SAF_RESP_MASK_CS0_PT1	0x170	101		x				
SAF_RESP_MASK_CS0_PT2	0x171	101		x				
SAF_RESP_MASK_CS1_PT1	0x172	101		x				
SAF_RESP_MASK_CS1_PT2	0x173	101		x				
SAF_RESP_MASK_CS2_PT1	0x174	101		x				
SAF_RESP_MASK_CS2_PT2	0x175	101		x				
SAF_RESP_MASK_CS3_PT1	0x176	101		x				
SAF_RESP_MASK_CS3_PT2	0x177	101		x				
SAF_RESP_MASK_CS4_PT1	0x178	101		x				
SAF_RESP_MASK_CS4_PT2	0x179	101		x				
NOP_GID_101	0x17F	101						
SAF_RESP_TARGET_0_PT1	0x180	110		x				
SAF_RESP_TARGET_0_PT2	0x181	110		x				
SAF_RESP_TARGET_1_PT1	0x182	110		x				
SAF_RESP_TARGET_1_PT2	0x183	110		x				
SAF_RESP_TARGET_2_PT1	0x184	110		x				
SAF_RESP_TARGET_2_PT2	0x185	110		x				

Register name	Address (HEX)	GID	Init	Diag	Safing	Scrap	Arming safing	Arming scraping
SAF_RESP_TARGET_3_PT1	0x186	110		x				
SAF_RESP_TARGET_3_PT2	0x187	110		x				
SAF_RESP_TARGET_4_PT1	0x188	110		x				
SAF_RESP_TARGET_4_PT2	0x189	110		x				
SAF_RESP_TARGET_5_PT1	0x18A	110		x				
SAF_RESP_TARGET_5_PT2	0x18B	110		x				
SAF_RESP_TARGET_6_PT1	0x18C	110		x				
SAF_RESP_TARGET_6_PT2	0x18D	110		x				
SAF_RESP_TARGET_7_PT1	0x18E	110		x				
SAF_RESP_TARGET_7_PT2	0x18F	110		x				
SAF_RESP_TARGET_8_PT1	0x190	110		x				
SAF_RESP_TARGET_8_PT2	0x191	110		x				
SAF_RESP_TARGET_9_PT1	0x192	110		x				
SAF_RESP_TARGET_9_PT2	0x193	110		x				
SAF_RESP_TARGET_10_PT1	0x194	110		x				
SAF_RESP_TARGET_10_PT2	0x195	110		x				
SAF_RESP_TARGET_11_PT1	0x196	110		x				
SAF_RESP_TARGET_11_PT2	0x197	110		x				
SAF_RESP_TARGET_12_PT1	0x198	110		x				
SAF_RESP_TARGET_12_PT2	0x199	110		x				
SAF_RESP_TARGET_13_PT1	0x19A	110		x				
SAF_RESP_TARGET_13_PT2	0x19B	110		x				
SAF_RESP_TARGET_14_PT1	0x19C	110		x				
SAF_RESP_TARGET_14_PT2	0x19D	110		x				
SAF_RESP_TARGET_15_PT1	0x19E	110		x				
SAF_RESP_TARGET_15_PT2	0x19F	110		x				
SAF_RESP_TARGET_16_PT1	0x1A0	110		x				
SAF_RESP_TARGET_16_PT2	0x1A1	110		x				
SAF_RESP_TARGET_17_PT1	0x1A2	110		x				
SAF_RESP_TARGET_17_PT2	0x1A3	110		x				
SAF_RESP_TARGET_18_PT1	0x1A4	110		x				
SAF_RESP_TARGET_18_PT2	0x1A5	110		x				
SAF_RESP_TARGET_19_PT1	0x1A6	110		x				
SAF_RESP_TARGET_19_PT2	0x1A7	110		x				
SAF_RESP_TARGET_20_PT1	0x1A8	110		x				
SAF_RESP_TARGET_20_PT2	0x1A9	110		x				
SAF_RESP_TARGET_21_PT1	0x1AA	110		x				
SAF_RESP_TARGET_21_PT2	0x1AB	110		x				
SAF_CRC_CTRL	0x1AD	110	x	x				
NOP_GID_110	0x1BF	110						

5.1.2.1 Main and power registers (GID = 000)

Table 13. **PWR_STATUS_0 - 0x001**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	2	0x0	x	Not used
SYS_BST_ON	RO	13	1	0x0	RESET_2	SysBoost state: 0 = OFF 1 = ON
PGND_LOSS	RLR	12	1	0x0	RESET_2	PGND ground loss latched flag: 0 = NO FAULT 1 = FAULT
ER_BST_PLS_SKIP	RLR	11	1	0x0	RESET_2	ER boost pulse skipping latched flag: 0 = NO FAULT 1 = FAULT
ER_BST_ON	RO	10	1	0x0	RESET_2	ERBST ON state: 0 = OFF 1 = ON
ERSW_OT	RLR	9	1	0x0	RESET_2	ER switch over temperature latched flag: 0 = NO FAULT 1 = FAULT
ERDCHSW_OC	RLR	8	1	0x0	RESET_2	ER discharge switch over current latched flag: 0 = NO FAULT 1 = FAULT
ERCHRSW_OT	RLR	7	1	0x0	RESET_2	ER charge switch over temperature latched flag: 0 = NO FAULT 1 = FAULT
ERBST_OT	RLR	6	1	0x0	RESET_2	ER boost over-temperature latched flag: 0 = NO FAULT 1 = FAULT
ERBOOST_OV	RLR	5	1	0x0	RESET_2	ER boost over-voltage latched flag: 0 = NO FAULT 1 = FAULT
ERBOOST_UV	RLR	4	1	0x0	RESET_2	ER boost under-voltage latched flag: 0 = NO FAULT 1 = FAULT
VSYSBOOST_OV	RLR	3	1	0x0	RESET_2	Sysboost over-voltage latched flag: 0 = NO FAULT 1 = FAULT
VSYSBOOST_UV	RLR	2	1	0x0	RESET_2	Sysboost under_voltage latched flag: 0 = NO FAULT 1 = FAULT
SYSBST_OT	RLR	1	1	0x0	RESET_2	Sysboost over-temperature latched flag: 0 = NO FAULT

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						1 = FAULT
BSTGND_LOSS	RLR	0	1	0x0	RESET_2	Boost GND_loss latched fault: 0 = NO FAULT 1 = FAULT

Table 14. PWR_CTRL_0 - 0x002

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
ERSWITCH_SLAVE_STATUS	RLR	15	1	0x0	RESET_4	ERSWITCH status for slave only: 0 = ERSWITCH is not set 1 = ERSWITCH is set and latched when COVRACT diagnostic command is issued
COVRACT_SLAVE_STATUS	RLR	14	1	0x0	RESET_4	COVRACT status for slave only: 0 = COVRACT is not set 1 = COVRACT is set and latched when COVRACT diagnostic command is issued
V5_REG_EN	RW	13	1	0x0	RESET_2	V5 linear regulator enable: 0 = Disable 1 = Enable
ER_SW_SLAVE_EN	RW	12	1	0x1	RESET_4	Inhibit ER_SWITCH, valid only for Slave during passive mode 0 = ER_Switch inhibited in passive mode 1 = ER_Switch not inhibited in passive mode
POWER_SUPPLY_ADC_MEAS_SAMPLE	RW	10	2	0x0	RESET_2	Sample number in power supply voltage measurement conversions: 00 = 4 samples 01 = 16 samples 10 = 8 samples 11 = 1 sample
ER_SW_CHG_DCHG_EN	RW	8	2	0x0	RESET_2	ER switch/charge/discharge enable: 00 = ALL OFF 01 = ER SWITCH ON 10 = ER CHARGE ON 11 = ER DISCHARGE ON
VCCBCK_FORCE_F_SLOPE	RW	7	1	0x0	RESET_2	VccBuck fast slope selection 0 = Fast slope activation depends on SysBoost voltage 1 = Fast slope is forced ON
SATBCK_FORCE_F_SLOPE	RW	6	1	0x0	RESET_2	SatBuck fast slope selection 0 = Fast slope activation depends on SysBoost voltage

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						1 = Fast slope is forced ON
COVRACT_MASTER_DIAG_START	WO	3	3	0x0	RESET_4	COVRACT diagnostic command for Master only: 0x0 = No action 0x6 = A pulse of 1 µs is generated on COVRACT pin output
ERBST_FORCE_F_SLOPE	RW	2	1	0x0	RESET_2	ER boost fast slope selection 0 = Fast slope activation depends on VIN voltage 1 = Fast slope is forced ON
ERBST_EN	RW	1	1	0x0	RESET_2	ER boost enable: 0 = OFF 1 = ON
ERBST_V_SEL	RW	0	1	0x0	RESET_2	ER boost voltage selection: 0 = 33 V 1 = 23 V

Table 15. PWR_CTRL_1 - 0x003

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SLAVE_PH_SEL	RW	13	3	0x1	RESET_2	Slave phase selection (62.5 ns of resolution): 000 = 0 ns 111 = 437.5 ns
VCCBCK_PH_SEL	RW	10	3	0x0	RESET_2	VCCBuck phase shifting selection (62.5 ns of resolution): 000 = 0 ns 111 = 437.5 ns
SATBCK_PH_SEL	RW	7	3	0x0	RESET_2	SatBuck phase shifting selection (62.5 ns of resolution): 000 = 0 ns 111 = 437.5 ns
SYBST_PH_SEL	RW	4	3	0x0	RESET_2	SyncBoost phase shifting selection (62.5 ns of resolution): 000 = 0 ns 111 = 437.5 ns
ERBST_PH_SEL	RW	1	3	0x0	RESET_2	ER boost phase shifting selection (62.5 ns of resolution): 000 = 0 ns 111 = 437.5 ns
SWREG_F_SEL	RW	0	1	0x0	RESET_2	Switching frequency select: 0 = 2 MHz 1 = 2.13 MHz

Table 16. **SHUTDOWN_CTRL - 0x004**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	8	8	0x0	x	Not used
SHTDWN_CODE	WO	0	8	0x0	RESET_1	Non-latched command 0x55 that allows transition into POWERMODE_SHUTDOWN state

Table 17. **OFF_CTRL - 0x005**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	8	8	0x0	x	Not used
OFF_CODE	WO	0	8	0x0	RESET_1	Non-latched command 0xAA that allows transition from POWERMODE SHUTDOWN to POWER OFF state

Table 18. **DEVICE_STATUS - 0x006**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SELFTEST_COMPLETED	RO	15	1	0x0	RESET_1	SELFTEST STATUS ANALOG BIST AND LOGIC BIST: 0 = NOT COMPLETED 1 = COMPLETED
NVM_WRITE_STATE	RO	14	1	0x0	RESET_1	NVM WRITE CYCLES STATE: 0 = Upload counter not equal to 0, it is possible to write NVM 1 = Upload counter equal to 0, maximum write cycles is reached
NVM_READY	RO	13	1	0x0	RESET_1	NVM READING STATUS: 0 = NOT COMPLETED 1 = COMPLETED
NVM_USER_CRC_ERR	RO	12	1	0x0	RESET_1	NVM USER SECTOR CRC error fault: 0 = NO FAULT 1 = FAULT
NVM_CRC_ERR	RO	11	1	0x0	RESET_1	NVM CRC error fault others sector (except USER sector): 0 = NO FAULT 1 = FAULT
SAFETY_ECHO_N	RLR	10	1	0x0	RESET_1	Safety echo status (active high): 1 = Is not asserted 0 = Is asserted
WD_RESET	RLR	9	1	0x0	RESET_1	WD reset detection flag: 0 = WD reset is not detected 1 = WD reset is detected
MCURST_FLAG	RLR	8	1	0x0	RESET_1	MCU reset detection flag: 0 = MCU reset is not detected 1 = MCU reset is detected

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
ANALOG_POR_FLAG	RLR	7	1	0x0	RESET_1	Analog Power on detection flag: 0 = Analog POR is not detected 1 = Analog POR is detected
UNUSED	RO	6	1	0x0	x	Not used
OPER_CTL_STATE	RO	3	3	0x0	RESET_2	Reports operating control state: 000 = Init 001 = Diag 010 = Saf 011 = Scrap 100 = Arm Saf 101 = Arm scrap other = Unused
TEST_MODE_STATE	RO	2	1	0x0	RESET_1	Report ST testmode state: 0 = Testmode not active 1 = Testmode active
PWR_MODE_STATE	RO	0	2	0x0	RESET_1	Reports power control state: 00 = Awake 01 = Active 10 = Er state 11 = Shutdown

Table 19. DEVICE_CTRL - 0x007

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SELFTEST_SAFETY_ECHO_ERR	RO	15	1	0x0	RESET_1	Safety echo bist error fault: 0 = NO FAULT 1 = FAULT
SNOOPING_TIMEOUT_DISABLE	RW	14	1	0x0	RESET_4	Disable 2 ms snooping timeout: 0 = Timeout enabled 1 = Timeout disabled
STAG_SYNC_PULSE_DLY	RW	13	1	0x0	RESET_1	SYNC pulse RSU staggering time: 0 = 10 µs 1 = 7 µs
SHUTDOWN_TIMEOUT_DISABLE	RW	12	1	0x0	RESET_1	Shutdown timeout disable 0 = tshutdown_to is enabled 1 = tshutdown_to is disabled
DIG_IO_SPEED	RW	11	1	0x0	RESET_1	DIG I/O speed configuration: 0 = Slow 1 = Fast
SELFTEST_ABIST_COMPLETED	RO	10	1	0x0	RESET_1	Analog bist status 0 = Running 1 = Completed

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SELFTEST_SAFETY_ECHO_COMPLETED	RO	9	1	0x0	RESET_1	Safety echo bist status 0 = Running 1 = Completed
SPI_ANALOG_BIST_RETRIGGER	WO	8	1	0x0	RESET_4	Restart selftest on analog comparators 0 = No effect 1 = Analog bist starts
SPI_SELFTEST_MASK	RW	7	1	0x0	RESET_4	Mask analog bist error result: 0 = Analog bist error is not masked 1 = Analog bist error is masked
SELFTEST_ABIST_ERR	RLR	6	1	0x0	RESET_1	Analog bist error fault: 0 = NO FAULT 1 = FAULT
CRC_MASK_RS_CS	RW	5	1	0x0	RESET_4	Disable snooping crc check protocol RS_CS: 0 = CRC check is enabled 1 = CRC check is disabled
CRC_MASK_SAF_CS4	RW	4	1	0x0	RESET_4	Disable snooping crc check protocol SAF_CS_4: 0 = CRC check is enabled 1 = CRC check is disabled
CRC_MASK_SAF_CS3	RW	3	1	0x0	RESET_4	Disable snooping crc check protocol SAF_CS_3: 0 = CRC check is enabled 1 = CRC check is disabled
CRC_MASK_SAF_CS2	RW	2	1	0x0	RESET_4	Disable snooping crc check protocol SAF_CS_2: 0 = CRC check is enabled 1 = CRC check is disabled
CRC_MASK_SAF_CS1	RW	1	1	0x0	RESET_4	Disable snooping crc check protocol SAF_CS_1: 0 = CRC check is enabled 1 = CRC check is disabled
CRC_MASK_SAF_CS0	RW	0	1	0x0	RESET_4	Disable snooping crc check protocol SAF_CS_0: 0 = CRC check is enabled 1 = CRC check is disabled

Table 20. NVM_WRITE_CTRL - 0x008

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	8	8	0x0	x	Not used
WRITE_TO_NVM	WO	0	8	0x0	RESET_1	Non-latched command 0x13 to write NVM

Table 21. **NVM_READ_CTRL - 0x009**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	8	8	0x0	x	Not used
READ_TO_NVM	WO	0	8	0x0	RESET_1	Non-latched command 0xEC that read data from NVM

Table 22. **NVM_BYTE01_CFG - 0x00A**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
ERBOOST_PLS_SKIP_BLK_SEL	RW	15	1	0x0	RESET_1	ERBST pulse skip blanking time: 0 = 100 µs nominal 1 = 50 µs nominal
ERBOOST_PLS_SKIP_DIS	RW	14	1	0x0	RESET_1	ERBST pulse skip selection: 0 = Enable 1 = Disable
ISCR_SR_SEL	RW	13	1	0x0	RESET_1	ISRC Slew rate selection: 0 = Slow 1 = Fast
THRESH_HIST_EN	RW	12	1	0x0	RESET_1	RSU threshold hysteresis enable of adaptive algorithm: 0 = No hysteresis 1 = ±4 mA hysteresis
BASE_LPF_FREQ_CTRL	RW	11	1	0x0	RESET_1	RSU base LPF sampling frequency control signal: 0 = Before deglitch filter 1 = After deglitch filter
SEL_STG_THRESH	RW	10	1	0x0	RESET_1	RSU over current detection deglitch filter time: 0 = Long 1 = Short
WD_ERR_LATCHED_ENABLE	RW	9	1	0x0	RESET_1	WD_ERR_LATCHED FEATURE ENABLE: 0 = When WD_ERR > WD_CNT_TH WD_ERR_LATCHED is not set 1 = When WD_ERR > WD_CNT_TH WD_ERR_LATCHED is set
WU_VALID_FLT_SHDW	RW	8	1	0x0	RESET_1	WU_VALID_FLT disable from ER to SHUTDOWN: 0 = WU_VALID_FLT equal to 0 needs to pass from ER to SHUTDOWN state 1 = WU_VALID_FLT is not necessary
LIN_CRC_CHECK_DISABLE	RW	7	1	0x0	RESET_1	LIN Background monitoring circuit disable 0 = Enable 1 = Disable
E2E_CRC_CHECK_DISABLE	RW	6	1	0x0	RESET_1	E2E background monitoring circuit disable 0 = Enable

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						1 = Disable
VCCBCK_FDM_EN	RW	5	1	0x0	RESET_1	VCCBCK FDM mode enable 0 = Disable 1 = Enable
SATBCK_SEL	RW	4	1	0x0	RESET_1	Satbuck voltage selection: 0 = 8 V 1 = 6.5 V
VCOREMON_ENABLE	RW	3	1	0x0	RESET_1	VCOREMON enable 0 = Disable 1 = Enable
MASTER_SLAVE_CONFIG	RW	0	3	0x0	RESET_1	Master slave configuration: 000 = Master 111 = Slave

Table 23. NVM_BYTE01_STATUS - 0x00B

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
NVM_ERBOOST_PLS_SKIP_BLK_SEL	RO	15	1	0x0	RESET_1	ERBST pulse skip blanking time: 0 = 100 µs nominal 1 = 50 µs nominal
NVM_ERBOOST_PLS_SKIP_DIS	RO	14	1	0x0	RESET_1	ERBST pulse skip selection: 0 = Enable 1 = Disable
NVM_ISCR_SR_SEL	RO	13	1	0x0	RESET_1	ISRC slew rate selection: 0 = Slow 1 = Fast
NVM_THRESH_HIST_EN	RO	12	1	0x0	RESET_1	RSU threshold hysteresis enable of adaptive algorithm: 0 = No hysteresis 1 = ±4 mA hysteresis
NVM_BASE_LPF_FREQ_CTRL	RO	11	1	0x0	RESET_1	RSU base LPF sampling frequency control signal: 0 = Before deglitch filter 1 = After deglitch filter
NVM_SEL_STG_THRESH	RO	10	1	0x0	RESET_1	RSU over current detection deglitch filter time: 0 = Long 1 = Short
NVM_WD_ERR_LATCHED_ENABLE	RO	9	1	0x0	RESET_1	WD_ERR_LATCHED FEATURE ENABLE: 0 = When WD_ERR > WD_CNT_TH WD_ERR_LATCHED is not set 1 = When WD_ERR > WD_CNT_TH WD_ERR_LATCHED is set

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
NVM_WU_VALID_FLT_SHDW	RO	8	1	0x0	RESET_1	WU_VALID_FLT disable from ER to SHUTDOWN: 0 = WU_VALID_FLT equal to 0 needs to pass from ER to SHUTDOWN state 1 = WU_VALID_FLT is not necessary
NVM_LIN_CRC_CHECK_DISABLE	RO	7	1	0x0	RESET_1	LIN Background monitoring circuit disable 0 = Enable 1 = Disable
NVM_E2E_CRC_CHECK_DISABLE	RO	6	1	0x0	RESET_1	E2E background monitoring circuit disable 0 = Enable 1 = Disable
NVM_VCCBCK_FDM_EN	RO	5	1	0x0	RESET_1	VCCBCK FDM mode enable 0 = Disable 1 = Enable
NVM_SATBCK_SEL	RO	4	1	0x0	RESET_1	Satbuck voltage selection: 0 = 8 V 1 = 6.5 V
NVM_VCOREMON_ENABLE	RO	3	1	0x0	RESET_1	VCOREMON enable 0 = Disable 1 = Enable
NVM_MASTER_SLAVE_CONFIG	RO	0	3	0x0	RESET_1	Master slave configuration: 000 = Master 111 = Slave

Table 24. NVM_DIE_ID_PT1 - 0x00C

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
EWS	RO	14	2	0x0	RESET_1	Identification of the device: 01 = L9691
Y_COORDINATE	RO	7	7	0x0	RESET_1	NVM_DIE_ID
X_COORDINATE	RO	0	7	0x0	RESET_1	NVM_DIE_ID

Table 25. NVM_DIE_ID_PT2 - 0x00D

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SEQUENTIAL_ID_PT1	RO	14	2	0x0	RESET_1	NVM_DIE_ID
Y_COORDINATE_OFFSET	RO	7	7	0x0	RESET_1	NVM_DIE_ID
X_COORDINATE_OFFSET	RO	0	7	0x0	RESET_1	NVM_DIE_ID

Table 26. **NVM_DIE_ID_PT3 - 0x00E**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SEQUENTIAL_ID_PT2	RO	0	16	0x0	RESET_1	NVM_DIE_ID

Table 27. **NVM_DIE_ID_PT4 - 0x00F**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	13	3	0x0	x	Not used
FAB	RO	10	3	0x0	RESET_1	NVM_DIE_ID
YEAR	RO	6	4	0x0	RESET_1	NVM_DIE_ID
WEEK	RO	0	6	0x0	RESET_1	NVM_DIE_ID

Table 28. **LBIST_CTRL - 0x010**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
LBIST_E2E_STATE	RO	14	2	0x0	RESET_1	LBIST E2E status: 00 = Not started 01 = Running 10 = Passed 11 = Fail
LBIST_PSINH_ACL_STATE	RO	12	2	0x0	RESET_1	LBIST PSINH ACL status: 00 = Not started 01 = Running 10 = Passed 11 = Fail
LBIST_SAFING_STATE	RO	10	2	0x0	RESET_1	LBIST SAFING status: 00 = Not started 01 = Running 10 = Passed 11 = Fail
MBIST_SAFING_RAM_STATE	RO	8	2	0x0	RESET_1	MBIST SAFING RAM status: 00 = Not started 01 = Running 10 = Passed 11 = Fail
UNUSED	RO	4	4	0x0	x	Not used
MBIST_SAFING_RAM_START	WO	3	1	0x0	RESET_1	Memory bist RAM inside moving average: 0 = No action 1 = MBIST start
LBIST_E2E_START	WO	2	1	0x0	RESET_1	LBIST E2E start command: 0 = No action 1 = MBIST start
LBIST_PSINH_ACL_START	WO	1	1	0x0	RESET_1	LBIST PSINH ACL start command: 0 = No action

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						1 = MBIST start
LBIST_SAFING_START	WO	0	1	0x0	RESET_1	LBIST SAFING start command: 0 = No action 1 = MBIST start

Table 29. **CLK_CTRL - 0x011**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
GND_LOSS_DEP_INH_EN	RW	15	1	0x0	RESET_1	0 = GND loss diagnostic not masked (same behavior as BA silicon) 1 = GND loss diagnostic masked when DEP_EN_CMD is set to 0xF0F0 (UNLOCK) and GND loss diagnostic un-masked when DEP_EN_CMD is set to 0x0F0F (LOCK). (comparators masked = VCCBCKGND_LOSS, SATBCKGND_LOSS, PGND_LOSS, BSTGND_LOSS, AGND_LOSS)
CLKSW_EN	RW	14	1	0x0	RESET_1	CLKSW output enable: 0 = Disable CLKSW output 1 = Enable CLKSW output
CLK_STUCK_ERR	RLR	13	1	0x0	RESET_1	CLK vs AUX CLK stuck error: 0 = No STUCK CLK error 1 = CLK_MAIN or CLK_AUX STUCK error
ERBOOST_SLOPE_SEL	RW	11	2	0x1	RESET_1	ER BOOST slope selection: 00 = 22 µH 01 = 33 µH 10 = 47-68 µH 11 = 100 µH
CLKSW_ERR	RLW	10	1	0x0	RESET_1	CLKSW error: 0 = No CLKSW error 1 = CLKSW error, CLKSW is not received by Slave (Write 1 to clear and to restart the CLKSW function)
CLKSW_PERIOD	RW	5	5	0x9	RESET_1	Value N to determine the switching phase refresh command defined as N*switching period (2 MHz): 00001 = 0.5 µs 00010 = 1 µs ... 01111 = 7.5 µs ... 11111 = 15.5 µs 00000 = Invalid configuration and the current value is not updated
CLK_FREQ_ERR	RLR	3	2	0x0	RESET_1	CLK vs AUX CLK frequency mismatch error: 00 = No CLK error 01 = CLKIN error

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						10 = Invalid 11 = CLK_MAIN or CLK_AUX error
FLL_LOOP_CLOSED	RO	2	1	0x0	RESET_1	FLL can close the loop after the enable: 0 = Do not close the FLL loop 1 = Close the FLL loop
SPI_FLL_EN	RW	1	1	0x0	RESET_4	Enable FLL: 0 = Disable FLL 1 = Enable FLL
MAIN_SS_DIS	RW	0	1	0x0	RESET_1	Main oscillator spread spectrum enable: 0 = Enable main oscillator spread spectrum 1 = Disable main oscillator spread spectrum

Table 30. PWR_STATUS_1 - 0x012

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	2	0x0	x	Not used
V5_SENSE_STG	RLR	13	1	0x0	RESET_2	V5V5 sense STG latched: 0 = NO FAULT 1 = FAULT
ER_STATE	RLR	12	1	0x0	RESET_2	ER STATE: 0 = Device not in ER state 1 = Device in ER state (VIN < VIN_BAD)
V5_SENSE_UV	RLR	11	1	0x0	RESET_2	V5V5 sense UV latched: 0 = NO FAULT 1 = FAULT
V5_SENSE_OV	RLR	10	1	0x0	RESET_2	V5V5 sense OV latched: 0 = NO FAULT 1 = FAULT
VCOREMON_UV	RLR	9	1	0x0	RESET_2	VCORE UV latched flag: 0 = NO FAULT 1 = FAULT
VCOREMON_OV	RLR	8	1	0x0	RESET_2	VCORE OV latched flag: 0 = NO FAULT 1 = FAULT
VCCBCK_OT	RLR	7	1	0x0	RESET_2	VCC buck OT latched flag: 0 = NO FAULT 1 = FAULT
VCCBCKGND_LOSS	RLR	6	1	0x0	RESET_2	VCC buck GND loss latched flag: 0 = NO FAULT 1 = FAULT
VCCBCK_UV_H	RLR	5	1	0x0	RESET_2	VCC buck UVH latched flag: 0 = NO FAULT 1 = FAULT

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
VCCBCK_UVL	RLR	4	1	0x0	RESET_2	VCC buck UVL latched flag: 0 = NO FAULT 1 = FAULT
VCCBCK_OV	RLR	3	1	0x0	RESET_2	VCC buck OV latched flag: 0 = NO FAULT 1 = FAULT
SATBCK_OT	RLR	2	1	0x0	RESET_2	Satbuck OT latched flag: 0 = NO FAULT 1 = FAULT
SATBCK_UV	RLR	1	1	0x0	RESET_2	Satbuck UV latched flag: 0 = NO FAULT 1 = FAULT
SATBCKGND_LOSS	RLR	0	1	0x0	RESET_2	Satbuck GND loss latched flag: 0 = NO FAULT 1 = FAULT

Table 31. PWR_STATUS_2 - 0x013

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
COVRACT_PIN_STATE	RO	15	1	0x0	RESET_2	Echo of COVRACT pin: 0 = LOW 1 = HIGH
V5_SENSE_ERR	RO	14	1	0x0	RESET_2	0 = V5_SENSE in range (V5_SENSE_UV < V5_SENSE < V5_SENSE_OV) 1 = V5_SENSE out of range (V5_SENSE < V5_SENSE_UV, or V5_SENSE > V5_SENSE_OV)
VCORE_ERR	RO	13	1	0x0	RESET_2	0 = VCOREMON in range (VCORE_UV < VCOREMON < VCORE_OV) 1 = VCOREMON out of range (VCOREMON < VCORE_UV, or VCOREMON > VCORE_OV)
VIN_BAD_STATUS	RO	12	1	0x0	RESET_2	VIN_BAD status: 1 = VIN < VIN_BAD 0 = VIN > VIN_BAD
VIN_GOOD_STATUS	RO	11	1	0x0	RESET_2	VIN_GOOD status: 0 = VIN < VIN_GOOD 1 = VIN > VIN_GOOD
VBAT_MON_STATUS	RO	10	1	0x0	RESET_2	VBAT_MON status: 0 = VBATMON < $V_{BATMON\_VALID\_L}$ 1 = VBATMON > $V_{BATMON\_VALID\_H}$
WAKE_UP_STATUS	RO	9	1	0x0	RESET_2	WAKE_UP status: 0 = Wake-up < $V_{WAKEUP\_VALID\_L}$ 1 = Wake-up > $V_{WAKEUP\_VALID\_H}$
VSF2_ENABLE_STATUS	RO	8	1	0x0	RESET_2	VSF2 enable state:

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						0 = OFF 1 = ON
VSF1_ENABLE_STATUS	RO	7	1	0x0	RESET_2	VSF1 enable state: 0 = OFF 1 = ON
VCC_BCK_ON	RO	6	1	0x0	RESET_2	VCC buck state: 0 = OFF 1 = ON
SAT_BCK_ON	RO	5	1	0x0	RESET_2	Satbuck state: 0 = OFF 1 = ON
SYS_BST_ON	RO	4	1	0x0	RESET_2	SysBoost state: 0 = OFF 1 = ON
ER_SW_ON	RO	3	1	0x0	RESET_2	ER_SWITCH state: 0 = OFF 1 = ON
ER_DSCHRG_SW_ON	RO	2	1	0x0	RESET_2	ER_DISCHARGE_SWITCH state: 0 = OFF 1 = ON
ER_CHRG_SW_ON	RO	1	1	0x0	RESET_2	ER_CHARGE_SWITCH state: 0 = OFF 1 = ON
ER_BST_ON	RO	0	1	0x0	RESET_2	ERBST ON state: 0 = OFF 1 = ON

Table 32. WD_CFG_0 - 0x014

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	15	1	0x0	x	Not used
WD_MODE	RW	14	1	0x0	RESET_3	WD mode: 0 = Fast max 2 ms with resolution 8 µs 1 = Slow max 16.3 ms resolution 64 µs
WDTMIN	RW	7	7	0x32	RESET_3	WD window minimum value - resolution according to WD_MODE bit
WDTDELTA	RW	0	7	0x19	RESET_3	WD window delta value - WDTMAX = WDTMIN + WDTDELTA - resolution according to WD_MODE bit

Table 33. WD_CTRL_0 - 0x015

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	13	3	0x0	x	Not used

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
WD_TIMER	RO	5	8	0x0	RESET_3	WD window timer value (resolution according to WD_MODE bit)
UNUSED	RO	2	3	0x0	x	Not used
WDCTL	RW	0	2	0x0	RESET_4	WD control command: 00 = NOP 01 = Code 10 = Code B 11 = NOP

Table 34. WD_CFG_1 - 0x016

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	3	13	0x0	x	Not used
WD_RETRY_TH	RW	0	3	0x7	RESET_3	WD retry counter threshold (number of WD errors permitted before latching WD1_LOCKOUT = 1)

Table 35. WD_STATUS - 0x017

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	10	6	0x0	x	Not used
WD_LO	RO	9	1	0x1	RESET_3	WD lockout - reflects WD1 lockout state: 0 = Inactive 1 = Active
WD_TM	RO	8	1	0x0	RESET_3	Test mode pin echo - reflects TM pin signal state: 0 = Do not echo test mode pin 1 = Echo test mode pin
WD_WDR	RO	7	1	0x0	RESET_3	WD reset latch: 0 = WD_WDR signal = 0 1 = WD1_WDR signal = 1
WD_ERR_CNT	RO	3	4	0x0	RESET_3	WD error counter
WD_STATE	RO	0	3	0x0	RESET_3	WD state: 000 = Init 001 = Run 010 = Test 011 = reset 100 = Override 111 = WSM_Reset others = unused

Table 36. WD_CTRL_1 - 0x018

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	7	0x0	x	Not used

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
WD_TIMEOUT_DISABLE	RW	8	1	0x0	RESET_3	Disable of the initial 500 ms timeout function of WD1 state machine: 0 = Do not disable the 500 ms timeout 1 = Disable the 500 ms timeout
WD_TEST	WO	0	8	0x0	RESET_3	Non-latched WD test commands = 0x3C

Table 37. PWR_ADC_A - 0x019

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
NEWDATA_A	RLR	15	1	0x0	RESET_4	1 = New data available from conversion
ADCRES_A	RO	5	10	0x0	RESET_4	10-bit ADC result value corresponding to ADCREQ request
ADCREQ_A	RW	0	5	0x0	RESET_4	ADC request select command

Table 38. PWR_ADC_B - 0x01A

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
NEWDATA_B	RLR	15	1	0x0	RESET_4	1 = New data available from conversion
ADCRES_B	RO	5	10	0x0	RESET_4	10-bit ADC result value corresponding to ADCREQ request
ADCREQ_B	RW	0	5	0x0	RESET_4	ADC request select command

Table 39. PWR_ADC_C - 0x01B

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
NEWDATA_C	RLR	15	1	0x0	RESET_4	1 = New data available from conversion
ADCRES_C	RO	5	10	0x0	RESET_4	10-bit ADC result value corresponding to ADCREQ request
ADCREQ_C	RW	0	5	0x0	RESET_4	ADC request select command

Table 40. PWR_ADC_D - 0x01C

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
NEWDATA_D	RLR	15	1	0x0	RESET_4	1 = New data available from conversion
ADCRES_D	RO	5	10	0x0	RESET_4	10-bit ADC result value corresponding to ADCREQ request
ADCREQ_D	RW	0	5	0x0	RESET_4	ADC request select command

Table 41. ER_CAP_DIAG_ESR_STATUS - 0x01D

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
NEWDATA	RLR	15	1	0x0	RESET_4	1 = New data available from conversion
ERCAP_DIAG_ERR_RESULT	RO	14	1	0x0	RESET_4	Error result in ER ADC diagnostic: 0 = No error

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						1 = Error
ERCAP_DIAG_RUNNING	RO	13	1	0x0	RESET_4	ER_CAP DIAG STATUS: 0 = ERCAP DIAG is not on-going 1 = ERCAP DIAG is running
ESR	RO	0	13	0x0	RESET_4	ESR ADC RESULT

Table 42. ER_CAP_DIAG_CAP_STATUS - 0x01E

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
NEWDATA	RLR	15	1	0x0	RESET_4	1 = New data available from conversion
ERCAP_DIAG_END_FOR_TIMEOUT	RO	14	1	0x0	RESET_4	ERCAP DIAG END FOR TIMEOUT 0 = No timeout 1 = Timeout
ER_CAP	RO	0	14	0x0	RESET_4	ERCAP ADC RESULT

Table 43. ER_CAP_DIAG_STATUS_0 - 0x01F

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
VSTART_T1	RO	8	8	0x0	RESET_4	VSTART_T1 value
VSTART	RO	0	8	0x0	RESET_4	VSTART value

Table 44. ER_CAP_DIAG_STATUS_1 - 0x020

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
VSTOP_T2	RO	8	8	0x0	RESET_4	VSTOP_T2 value
VSTOP	RO	0	8	0x0	RESET_4	VSTOP value

Table 45. ER_CAP_DIAG_STATUS_2 - 0x021

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DELTA_T2	RO	8	8	0x0	RESET_4	DELTA_T2 value
DELTA_T1	RO	0	8	0x0	RESET_4	DELTA_T1 value

Table 46. ER_CAP_DIAG_STATUS_3 - 0x022

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
INTEGRAL	RO	0	16	0x0	RESET_4	INTEGRAL value

Table 47. ER_CAP_DIAG_CTRL - 0x023

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	4	12	0x0	x	Not used

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
ER_DIS_MEAS_DELAY	RW	3	1	0x0	RESET_4	0 = DELAY 1 = NO DELAY
ER_DIAG_TIMEOUT	RW	1	2	0x0	RESET_4	ER_DIAG_TIMEOUT: 00 = 5 ms 01 = 10 ms 10 = 20 ms 11 = 65 ms
ER_DIAG_START	RW	0	1	0x0	RESET_4	ER ADC CONTROL: 0 = Stop ER diag 1 = Start ER diag

Table 48. SSM_CTRL - 0x024

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SS_STATE_CODE	WO	0	16	0x0	RESET_4	Non-latched IC operating state transition command: 0x3CC3 = Diag state (only for Slave) 0xACAC = Safing state 0x3535 = Scrap state

Table 49. SAFING_SCRAP_CTRL - 0x025

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAFING_SCRAP_FBCK	RO	12	4	0x0	RESET_4	SAFING_SCRAP_FR_CNT in IDLE state (frozen when SAFING_SCRAP_CODE_A is received): SEED_A (0x1) in SCRAP_CMD_A_OK state SEED_B (0x2) in SCRAP_CMD_B_OK state SEED_C (0x4) in SCRAP_CMD_C_OK state
SAFING_SCRAP_CODE	WO	0	12	0x0	RESET_4	Non-latched IC command to pass from SAFING to ACL state. A, B, C commands have to be issued in sequence to set SCRAP_CMD_SEQ_VALID: SAFING_SCRAP_CODE_A = 0xA1B SAFING_SCRAP_CODE_B = SAFING_SCRAP_FR_CNT << 8 | not (SAFING_SCRAP_FR_CNT) SAFING_SCRAP_CODE_C = SAFING_SCRAP_CODE_B xor 0xAAA

Table 50. SCRAP_CTRL - 0x026

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SEED	RO	8	8	0x0	RESET_4	Random scrap seed value - generated from a free-running 8-bit counter
KEY	WO	0	8	0x0	RESET_4	KEY value submitted to the SCRAP state machine

Table 51. **ACL_PSINH_STATUS - 0x027**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
PSINH_DCS_EXP_TIMER	RO	15	1	0x0	RESET_4	State of PSINH DCS expiration timer: 0 = If PSINH DCS timeout is not expired 1 = If PSINH DCS timeout is expired
PSINHEXT	RO	14	1	0x0	RESET_4	External PSINH signal status: 0 = PSINHEXT inactive 1 = PSINHEXT is active
PSINHMCU2	RO	13	1	0x0	RESET_4	MCU2 PSINH signal status: 0 = PSINHEXT inactive 1 = PSINHEXT is active
PSINHINTLIN	RO	12	1	0x0	RESET_4	LIN PSINH signal status: 0 = PSINH LIN inactive 1 = PSINH LIN is active
PSINHINTDCS1	RO	11	1	0x0	RESET_4	DCS CH1 PSINH signal status: 0 = PSINH DCS1 inactive 1 = PSINH DCS1 is active
PSINHINTDCS0	RO	10	1	0x0	RESET_4	DCS CH0 PSINH signal status: 0 = PSINH DCS0 inactive 1 = PSINH DCS0 is active
ACL_PIN_STATE	RO	9	1	0x0	RESET_4	Echo of ACL pin: 0 = LOW 1 = HIGH
ACL_VALID	RO	8	1	0x0	RESET_4	Valid ACL detection: 0 = ACL Invalid 1 = ACL Valid
UNUSED	RO	0	8	0x0	x	Not used

Table 52. **ARM_PSINH_INT_STATUS - 0x028**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
PSINHINT	RO	15	1	0x0	RESET_4	Internal PSINH signal status: 0 = Not Inhibited 1 = Inhibited
ARM_DISABLE	RO	14	1	0x0	RESET_4	ARM_DISABLE - reflects ARM_DISABLE state that is set when not(WD_LOCKOUT) and WD_RUN state is equal to 0 or WD is not in WD_OVERRIDE state , reported here in order to be snooped by the slave: 0 = arming is not inhibited 1 = arming is inhibited
UNUSED	RO	8	6	0x0	x	Not used
ARMINT_x	RO	0	8	0x0	RESET_4	Internal ARM x (x from 0 to 7) signal status: 0 = ARMINTx inactive 1 = ARMINTx is active

Table 53. **ARM_PSINH_EXT_STATUS - 0x029**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
PSINHEXT	RO	15	1	0x0	RESET_4	External PSINH signal status: 0 = PSINHEXT inactive 1 = PSINHEXT is active
ARM_DISABLE_EXT	RO	14	1	0x0	RESET_4	External ARM_DISABLE - reflects ARM_DISABLE state in the SLAVE device: 0 = Arming is not inhibited, 1 = Arming is inhibited
UNUSED	RO	8	6	0x0	x	Not used
ARMEXT_x	RO	0	8	0x0	RESET_4	External ARM x (x from 0 to 7) signal status: 0 = ARMEXTx inactive 1 = ARMEXTx is active

Table 54. **ARM_E2E_STATUS - 0x02A**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	8	8	0x0	x	Not used
ARME2E_x	RO	0	8	0x0	RESET_4	E2E ARM x (x from 0 to 7) signal status: 0 = ARME2Ex inactive 1 = ARME2Ex is active

Table 55. **ARM_PSINH_MCU2_STATUS - 0x02B**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
PSINHMCU2	RO	15	1	0x0	RESET_4	MCU2 PSINH signal status: 0 = PSINHEXT inactive 1 = PSINHEXT is active
UNUSED	RO	8	7	0x0	x	Not used
ARMMCU2_x	RO	0	8	0x0	RESET_4	MCU2 ARM x (x from 0 to 7) signal status: 0 = ARMMCUx inactive 1 = ARMMCUx is active

Table 56. **MCU2_RESERVED_ADDRESS - 0x02C**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	7	0x0	x	Not used
ARM_MCU2_ADDR	RO	0	9	0x0	RESET_4	MCU2 address to be snooped

Table 57. **ARM_PSINH_MCU2_CTRL - 0x02D**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
PSINHMCU2_EN	RW	15	1	0x0	RESET_4	MCU2 PSINH enable: 0 = PSINHMCU2 is disabled 1 = PSINHMCU2 is enabled

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	8	7	0x0	x	Not used
ARMMCU2_x_EN	RW	0	8	0x0	RESET_4	MCU2 ARM x (x from 0 to 7) enable: 0 = ARMMCUx is disabled 1 = ARMMCUx is enabled

Table 58. SW_RESET_CTRL - 0x02E

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SOFT_RESET_CMD	WO	0	16	0x0	RESET_4	SW reset command 0x3C95 that generates RST_4

Table 59. E2E_PROTOCOL_CTRL - 0x02F

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
E2E_PROTOCOL_CMD	WO	0	16	0x0	RESET_4	Command 0x0E2E to pass from standard G_SPI protocol to E2E protocol

Table 60. SNOOPING_TEST_INT - 0x030

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SNOOP_TEST_INT	RW	0	16	0x0	RESET_4	Register to test snooping logic. Data written by MCU writes this register that will be snooped by other device when Read request is issued

Table 61. SNOOPING_TEST_EXT - 0x031

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SNOOP_TEST_EXT	RO	0	16	0x0	RESET_4	Register updated by SNOOP_TEST_INT content to verify the snooping integrity

Table 62. E2E_CRC_CTRL - 0x032

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
CRC_ERR_E2E	RLR	15	1	0x0	RESET_4	CRC error flag: 0 = CRC error is not present 1 = CRC error is present
UNUSED	RO	13	2	0x0	x	Not used
CRC_EXP_E2E	RO	1	12	0x0	RESET_4	CRC to be matched (computed internally by the device after RECALC command is set)
RECALC_E2E	WO	0	1	0x0	RESET_4	CRC calculation restart: 1= Request the recalculation of the CRC 0 = No action

Table 63. **DEVICE_ID - 0x033**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	13	3	0x0	x	Not used
WAFER	RO	8	5	0x0	RESET_1	DIE_ID WAFER
ID_VERSION	RO	0	8	0x0	RESET_1	Identification of the silicon version: 0010_0001 = AA VERSION 0100_0001 = BA VERSION 0110_0001 = CA VERSION

Table 64. **NOP_GID_000 - 0x03F**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	0	16	0x0	x	No operation response

5.1.2.2 *DCS, GPO, LIN and PSINH registers (GID = 001)*

Table 65. DCS_ENG0_CTRL - 0x040

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	2	0x0	x	Not used
DCS_PDCURR_ENG0	RW	13	1	0x0	RESET_4	Disable of all pull-down current for DC sensor: 0 = Do not disable PDCURR 1 = Disable PDCURR
STRONG_PD_EN_ENG0	WO	7	6	0x0	RESET_4	Strong pull-down enable for ENG0: 000001 = Enable strong PD channel 0 000010 = Enable strong PD channel 1 000100 = Enable strong PD channel 2 001000 = Enable strong PD channel 3 010000 = Enable strong PD channel 10 100000 = Enable strong PD channel 11 others are invalid (no strong PD enabled)
DCS_VOUT_SEL_ENG0	RW	4	3	0x0	RESET_4	Selector and enable for ENG0 voltage: 0xx = Disable 100 = Vlow 101 = Vhigh 110 or 111 = Vsys
ILIM_ENG0	RW	3	1	0x0	RESET_4	Selector for ENG0 current limit: 0 = Low current limit 1 = High current limit
DCS_CH_SEL_ENG0	RW	0	3	0x0	RESET_4	Channel ID - selects DC sensor channel for output activation of ENG0: 001 = DCS0 010 = DCS1 011 = DCS2 100 = DCS3 101 = DCS10 110 = DCS11 other are invalid, that means channel disable

Table 66. DCS_ENG1_CTRL1 - 0x041

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	2	0x0	x	Not used
DCS_PDCURR_ENG1	RW	13	1	0x0	RESET_4	Disable of all pull-down current for DC sensor: 0 = Do not disable PDCURR 1 = Disable PDCURR
STRONG_PD_EN_ENG1	WO	7	6	0x0	RESET_4	Strong pull-down enable for ENG1: 000001 = Enable strong PD channel 4 000010 = Enable strong PD channel 5

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						000100 = Enable strong PD channel 6 001000 = Enable strong PD channel 7 010000 = Enable strong PD channel 8 100000 = Enable strong PD channel 9 others are invalid (no strong PD enabled)
DCS_VOUT_SEL_ENG1	RW	4	3	0x0	RESET_4	Selector and enable for ENG0 voltage: 0xx = Disable 100 = Vlow 101 = Vhigh 110 or 111 = Vsys
ILIM_ENG1	RW	3	1	0x0	RESET_4	Selector for ENG0 current limit: 0 = Low current limit 1 = High current limit
DCS_CH_SEL_ENG1	RW	0	3	0x0	RESET_4	Channel ID - selects DC sensor channel for output activation of ENG1: 001 = DCS4 010 = DCS5 011 = DCS6 100 = DCS7 101 = DCS8 110 = DCS9 other are invalid, that means channel disable

Table 67. DCS_DIAG_CFG - 0x042

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	13	3	0x0	x	Not used
DCS_MEAS	RW	11	2	0x2	RESET_4	Sample number in DCs measurement conversions: 00 = 25 µs (4 samples) 01 = 41 µs (8 samples) 10 = 73 µs (16 samples) 11 = 137 µs (32 samples)
DCS_AUTO_SWITCH_OFF	RW	10	1	0x0	RESET_4	Disable automatically DCS when the ADC measurement is completed: 0 = DCS auto-switchoff disable 1 = DCS auto switch-off enable
XCONN_THRESH	RW	0	10	0x0	RESET_4	Threshold to check cross connection between DC sensors: -1.5 V to 20.5 V, with LSB = 22 mV

Table 68. DCS_ADC_A - 0x043

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DCS_NEWDATA_A	RLR	15	1	0x0	RESET_4	1 = New data available from conversion

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DCS_ADCRES_A	RO	5	10	0x0	RESET_4	10-bit ADC result value corresponding to ADCREQ_x request
DCS_ADCREQ_A	RW	0	5	0x0	RESET_4	ADC request select command

Table 69. DCS_ADC_B - 0x044

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DCS_NEWDATA_B	RLR	15	1	0x0	RESET_4	1 = New data available from conversion
DCS_ADCRES_B	RO	5	10	0x0	RESET_4	10-bit ADC result value corresponding to ADCREQ_x request
DCS_ADCREQ_B	RW	0	5	0x0	RESET_4	ADC request select command

Table 70. DCS_ADC_C - 0x045

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DCS_NEWDATA_C	RLR	15	1	0x0	RESET_4	1 = New data available from conversion
DCS_ADCRES_C	RO	5	10	0x0	RESET_4	10-bit ADC result value corresponding to ADCREQ_x request
DCS_ADCREQ_C	RW	0	5	0x0	RESET_4	ADC request select command

Table 71. DCS_ADC_D - 0x046

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DCS_NEWDATA_D	RLR	15	1	0x0	RESET_4	1 = New data available from conversion
DCS_ADCRES_D	RO	5	10	0x0	RESET_4	10-bit ADC result value corresponding to ADCREQ_x request
DCS_ADCREQ_D	RW	0	5	0x0	RESET_4	ADC request select command

Table 72. GPO0_CTRL - 0x047

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
GPO_DIAG_OFF_STATUS	RO	15	1	0x0	RESET_4	GPO diag off status: 1 = Enabled 0 = Disabled automatically due VIN < VINGOOD or VIN > VIN_OV
GPO_LIM	RO	14	1	0x0	RESET_4	GPO current limit flag: 0 = Current limit is not present 1 = Current limit is present
GPO_TEMP	RLR	13	1	0x0	RESET_4	GPO over temp detect: 0 = Over temp is not present 1 = Over temp is present
GPO_OFFHI	RO	12	1	0x0	RESET_4	GPO OFF high voltage threshold detect (2/3Vin): 0 = Below threshold 1 = Above threshold

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
GPO_OFFLO	RO	11	1	0x0	RESET_4	GPO OFF low voltage threshold detect (1/3Vin): 0 = Above threshold 1 = Below threshold
GPO_ONHI	RO	10	1	0x0	RESET_4	GPO ON high voltage threshold detect (2/3Vin): 0 = Below threshold 1 = Above threshold
GPO_ONLO	RO	9	1	0x0	RESET_4	GPO ON low voltage threshold detect (1/3Vin): 0 = Above threshold 1 = Below threshold
GPO_ON_CURRENT	RO	8	1	0x0	RESET_4	GPO ON current threshold detect: 0 = No current detected 1 = Current detected
GPO_PWM	RW	0	8	0x0	RESET_4	PWM% with scaling of 0.4% per count

Table 73. GPO1_CTRL - 0x048

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
GPO_DIAG_OFF_STATUS	RO	15	1	0x0	RESET_4	GPO diag off status: 1 = Enabled 0 = Disabled automatically due VIN < VINGOOD or VIN > VIN_OV
GPO_LIM	RO	14	1	0x0	RESET_4	GPO current limit flag: 0 = Current limit is not present 1 = Current limit is present
GPO_TEMP	RLR	13	1	0x0	RESET_4	GPO over temp detect: 0 = Over temp is not present 1 = Over temp is present
GPO_OFFHI	RO	12	1	0x0	RESET_4	GPO OFF high voltage threshold detect (2/3Vin): 0 = Below threshold 1 = Above threshold
GPO_OFFLO	RO	11	1	0x0	RESET_4	GPO OFF low voltage threshold detect (1/3Vin): 0 = Above threshold 1 = Below threshold
GPO_ONHI	RO	10	1	0x0	RESET_4	GPO ON high voltage threshold detect (2/3Vin): 0 = Below threshold 1 = Above threshold
GPO_ONLO	RO	9	1	0x0	RESET_4	GPO ON low voltage threshold detect (1/3Vin): 0 = Above threshold

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						1 = Below threshold
GPO_ON_CURRENT	RO	8	1	0x0	RESET_4	GPO ON current threshold detect: 0 = No current detected 1 = Current detected
GPO_PWM	RW	0	8	0x0	RESET_4	PWM% with scaling of 0.4% per count

Table 74. GPO2_CTRL - 0x049

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
GPO_DIAG_OFF_STATUS	RO	15	1	0x0	RESET_4	GPO diag off status: 1 = Enabled 0 = Disabled automatically due VIN < VINGOOD or VIN > VIN_OV
GPO_LIM	RO	14	1	0x0	RESET_4	GPO current limit flag: 0 = Current limit is not present 1 = Current limit is present
GPO_TEMP	RLR	13	1	0x0	RESET_4	GPO over temp detect: 0 = Over temp is not present 1 = Over temp is present
GPO_OFFHI	RO	12	1	0x0	RESET_4	GPO OFF high voltage threshold detect (2/3Vin): 0 = Below threshold 1 = Above threshold
GPO_OFFLO	RO	11	1	0x0	RESET_4	GPO OFF low voltage threshold detect (1/3Vin): 0 = Above threshold 1 = Below threshold
GPO_ONHI	RO	10	1	0x0	RESET_4	GPO ON high voltage threshold detect (2/3Vin): 0 = Below threshold 1 = Above threshold
GPO_ONLO	RO	9	1	0x0	RESET_4	GPO ON low voltage threshold detect (1/3Vin) 0 = Above threshold 1 = Below threshold
GPO_ON_CURRENT	RO	8	1	0x0	RESET_4	GPO ON current threshold detect 0 = No current detected 1 = Current detected
GPO_PWM	RW	0	8	0x0	RESET_4	PWM% with scaling of 0.4% per count

Table 75. GPO0_CFG - 0x04A

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	2	0x0	x	Not used

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
GPO_PU_EN	RW	13	1	0x0	RESET_4	GPO pull-up enable: 0 = Pull-up disabled 1 = Pull-up enabled
GPO_SEL_SR	RW	12	1	0x0	RESET_4	Slew rate selection: 0 = 0.25 V/µs 1 = 0.75 V/µs
SEL_FREQ_PWM	RW	8	4	0x0	RESET_4	4 bit frequency selection (100 Hz - 400 Hz, 25 Hz of resolution): 0000 = 100 Hz 0001 = 125 Hz 0010 = 150 Hz 0011 = 175 Hz 0100 = 200 Hz 0101 = 225 Hz 0110 = 250 Hz 0111 = 275 Hz 1000 = 300 Hz 1001 = 325 Hz 1010 = 350 Hz 1011 = 375 Hz 1100 = 400 Hz others = Invalid
BLANKING_DIAG	RW	6	2	0x0	RESET_4	Blanking delay time (4 settings): 00 = 72 µs 01 = 120 µs 10 = 168 µs 11 = 224 µs
HIGH_THRESHOLD_CONF	RW	4	2	0x0	RESET_4	High threshold adjust (2/3): 00 = 60% VIN 01 = 66% VIN 10 = 75% VIN 11 = 80% VIN
LOW_THRESHOLD_CONF	RW	2	2	0x0	RESET_4	Low threshold adjust (1/3): 00 = 20% VIN 01 = 25% VIN 10 = 33% VIN 11 = 40% VIN
THRESHOLD_ON_CURRENT	RW	0	2	0x0	RESET_4	Current reference for ON threshold: 00 = 2 mA 01 = 4 mA 10 = 6 mA 11 = 8 mA

Table 76. **GPO1_CFG - 0x04B**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	2	0x0	x	Not used
GPO_PU_EN	RW	13	1	0x0	RESET_4	GPO pull-up enable: 0 = Pull-up disabled 1 = Pull-up enabled
GPO_SEL_SR	RW	12	1	0x0	RESET_4	Slew rate selection: 0 = 0.25 V/µs 1 = 0.75 V/µs
SEL_FREQ_PWM	RW	8	4	0x0	RESET_4	4 bit frequency selection (100 Hz - 400Hz, 25 Hz of resolution): 0000 = 100 Hz 0001 = 125 Hz 0010 = 150 Hz 0011 = 175 Hz 0100 = 200 Hz 0101 = 225 Hz 0110 = 250 Hz 0111 = 275 Hz 1000 = 300 Hz 1001 = 325 Hz 1010 = 350 Hz 1011 = 375 Hz 1100 = 400 Hz others = Invalid
BLANKING_DIAG	RW	6	2	0x0	RESET_4	Blanking delay time (4 settings): 00 = 72 µs 01 = 120 µs 10 = 168 µs 11 = 224 µs
HIGH_THRESHOLD_CONF	RW	4	2	0x0	RESET_4	High threshold adjust (2/3): 00 = 60% VIN 01 = 66% VIN 10 = 75% VIN 11 = 80% VIN
LOW_THRESHOLD_CONF	RW	2	2	0x0	RESET_4	Low threshold adjust (1/3): 00 = 20% VIN 01 = 25% VIN 10 = 33% VIN 11 = 40% VIN
THRESHOLD_ON_CURRENT	RW	0	2	0x0	RESET_4	Current reference for ON threshold: 00 = 2 mA 01 = 4 mA 10 = 6 mA

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						11 = 8 mA

Table 77. **GPO2_CFG - 0x04C**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	2	0x0	x	Not used
GPO_PU_EN	RW	13	1	0x0	RESET_4	GPO pull-up enable: 0 = Pull-up disabled 1 = Pull-up enabled
GPO_SEL_SR	RW	12	1	0x0	RESET_4	Slew rate selection: 0 = 0.25 V/µs 1 = 0.75 V/µs
SEL_FREQ_PWM	RW	8	4	0x0	RESET_4	4 bit frequency selection (100 Hz - 400 Hz, 25 Hz of resolution) 0000 = 100 Hz 0001 = 125 Hz 0010 = 150 Hz 0011 = 175 Hz 0100 = 200 Hz 0101 = 225 Hz 0110 = 250 Hz 0111 = 275 Hz 1000 = 300 Hz 1001 = 325 Hz 1010 = 350 Hz 1011 = 375 Hz 1100 = 400 Hz others = Invalid
BLANKING_DIAG	RW	6	2	0x0	RESET_4	Blanking delay time (4 settings) 00 = 72 µs 01 = 120 µs 10 = 168 µs 11 = 224 µs
HIGH_THRESHOLD_CONF	RW	4	2	0x0	RESET_4	High threshold adjust (2/3): 00 = 60% VIN 01 = 66% VIN 10 = 75% VIN 11 = 80% VIN
LOW_THRESHOLD_CONF	RW	2	2	0x0	RESET_4	Low threshold adjust (1/3): 00 = 20% VIN 01 = 25% VIN 10 = 33% VIN 11 = 40% VIN

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
THRESHOLD_ON_CURRENT	RW	0	2	0x0	RESET_4	Current reference for ON threshold: 00 = 2 mA 01 = 4 mA 10 = 6 mA 11 = 8 mA

Table 78. LIN_OCS_MASK_PT0 - 0x04D

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
OCS_MASK_15_0	RW	0	16	0x0	RESET_4	LIN_OCS_Mask value to indicate the bit locations of critical OCS data 16-bit data that is bit-wise AND'd with the captured Rx data stream

Table 79. LIN_OCS_MASK_PT1 - 0x04E

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
OCS_MASK_31_16	RW	0	16	0x0	RESET_4	LIN_OCS_Mask value to indicate the bit locations of critical OCS data 16-bit data that is bit-wise AND'd with the captured Rx data stream

Table 80. LIN_OCS_MASK_PT2 - 0x04F

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
OCS_MASK_47_32	RW	0	16	0x0	RESET_4	LIN_OCS_Mask value to indicate the bit locations of critical OCS data 16-bit data that is bit-wise AND'd with the captured Rx data stream

Table 81. LIN_OCS_MASK_PT3 - 0x050

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
OCS_MASK_63_48	RW	0	16	0x0	RESET_4	LIN_OCS_Mask value to indicate the bit locations of critical OCS data 16-bit data that is bit-wise AND'd with the captured Rx data stream

Table 82. LIN_OCS_TGT1_PT0 - 0x051

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
OCS_TARGET1_15_0	RW	0	16	0x0	RESET_4	LIN_OCS_Target value required to indicate specific OCS status 1 16-bit target value that is compared to the bit-wise result of the Rx data stream and mask

Table 83. **LIN_OCS_TGT1_PT1 - 0x052**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
OCS_TARGET1_31_16	RW	0	16	0x0	RESET_4	LIN_OCS_Target value required to indicate specific OCS status 1

Table 84. **LIN_OCS_TGT1_PT2 - 0x053**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
OCS_TARGET1_47_32	RW	0	16	0x0	RESET_4	LIN_OCS_Target value required to indicate specific OCS status 1

Table 85. **LIN_OCS_TGT1_PT3 - 0x054**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
OCS_TARGET1_63_48	RW	0	16	0x0	RESET_4	LIN_OCS_Target value required to indicate specific OCS status 1

Table 86. **LIN_OCS_TGT2_PT0 - 0x055**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
OCS_TARGET1_15_0	RW	0	16	0x0	RESET_4	LIN_OCS_Target value required to indicate specific OCS status 2 16-bit target value that is compared to the bit-wise result of the Rx data stream and mask

Table 87. **LIN_OCS_TGT2_PT1 - 0x056**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
OCS_TARGET1_31_16	RW	0	16	0x0	RESET_4	LIN_OCS_Target value required to indicate specific OCS status 2

Table 88. **LIN_OCS_TGT2_PT2 - 0x057**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
OCS_TARGET1_47_32	RW	0	16	0x0	RESET_4	LIN_OCS_Target value required to indicate specific OCS status 2

Table 89. **LIN_OCS_TGT2_PT3 - 0x058**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
OCS_TARGET1_63_48	RW	0	16	0x0	RESET_4	LIN_OCS_Target value required to indicate specific OCS status 2

Table 90. **LIN_STATUS - 0x059**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	11	5	0x0	x	Not used

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
LIN_SLEEP_MODE	RO	10	1	0x0	RESET_4	0 = ACTIVE (decoder is able to decode a new message) 1 = SLEEP
LIN_PROTOCOL_TO_ERR	RLR	9	1	0x0	RESET_4	LIN protocol timeout error fault: 0 = NO FAULT 1 = FAULT
LIN_TX_DOM_TO	RLR	8	1	0x0	RESET_4	LIN TXD dominant timeout fault: 0 = NO FAULT 1 = FAULT
LIN_PERM_REC_TO	RLR	7	1	0x0	RESET_4	LIN permanent recessive fault: 0 = NO FAULT 1 = FAULT
PERM_DOM_TO	RLR	6	1	0x0	RESET_4	LIN permanent dominant fault: 0 = NO FAULT 1 = FAULT
MSG_TO_ERR	RLR	5	1	0x0	RESET_4	LIN timeout error fault: 0 = NO FAULT 1 = FAULT
CKSUM_CHECK	RLR	4	1	0x0	RESET_4	LIN checksum error: 0 = NO FAULT 1 = FAULT
PID_P1_CHECK	RLR	3	1	0x0	RESET_4	LIN PID parity fault P1: 0 = NO FAULT 1 = FAULT
PID_P0_CHECK	RLR	2	1	0x0	RESET_4	LIN PID parity fault P0: 0 = NO FAULT 1 = FAULT
OT_LIN	RLR	1	1	0x0	RESET_4	LIN thermal fault: 0 = NO FAULT 1 = FAULT
UNUSED	RO	0	1	0x0	RESET_4	Not used

Table 91. LIN_CFG - 0x05A

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
LIN_MON_EN	RW	15	1	0x0	RESET_4	Enable for the error handling features TX dominant, permanent recessive and permanent dominant: 0 = NO 1 = YES
LIN_TX_DOM_TO_CFG	RW	14	1	0x0	RESET_4	Error state for transmitter in the event of TX_Dominant timeout: 0 = Re-enabled after status register is cleared

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						1 = Re-enabled after TX returns to recessive (high-level) state
MSG_TO_ERR_PSINH_SEL	RW	13	1	0x0	RESET_4	Enable of the effect of a message timeout error: 0 = PSINH_LIN set to 1 to inhibit 1 = PSINH_LIN unchanged
MSG_TO	RW	11	2	0x0	RESET_4	Message valid timeout configuration: 00 = 0.5 s 01 = 1 s 10 = 2 s 11 = 4 s
LENGTH_MATCH	RW	9	2	0x0	RESET_4	Message length configuration: 00 = 1 byte 01 = 2 bytes 10 = 4 bytes 11 = 8 bytes
PSINH_LIN_EN	RW	8	1	0x0	RESET_4	LIN passenger inhibit usage: 0 = Disabled 1 = Enabled
PID_MATCH	RW	2	6	0x0	RESET_4	Protected identifier field to be matched
TX_RX_EN	RW	1	1	0x0	RESET_4	Enable the interface transmitter and receiver: 0 = NO 1 = YES
DEC_EN	RW	0	1	0x0	RESET_4	Enable internal message decoder: 0 = NO 1 = YES

Table 92. LIN_CRC_CTRL - 0x05B

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
CRC_ERR_LIN	RLR	15	1	0x0	RESET_4	CRC error flag: 0 = CRC error is not present 1 = CRC error is present
UNUSED	RO	13	2	0x0	RESET_4	Not used
CRC_EXP_LIN	RO	1	12	0x0	RESET_4	CRC to be matched (computed internally by the device after RECALC command is set)
RECALC_LIN	WO	0	1	0x0	RESET_4	CRC calculation restart: 1= request the recalculation of the CRC 0 = no action

Table 93. **PSINH_DCS_CFG - 0x05C**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DCS_TIMEOUT_PSINH_1	RW	14	2	0x0	RESET_4	DCS PSINH channel 1 measure timeout configuration: 00 = 0.5 s 01 = 1 s 10 = 2 s 11 = 4 s
DCS_TIMEOUT_PSINH_0	RW	12	2	0x0	RESET_4	DCS PSINH channel 0 measure timeout configuration: 00 = 0.5 s 01 = 1 s 10 = 2 s 11 = 4 s
V_PSINH_1_SEL	RW	10	2	0x0	RESET_4	DCS1 measurement voltage setting: 00 = Vlow 01 = Vhigh 10 = 11 = unused
I_PSINH_1_SEL	RW	9	1	0x0	RESET_4	DCS1 measurement current setting: 0 = Ilim_low 1 = Ilim_hi
V_PSINH_0_SEL	RW	7	2	0x0	RESET_4	DCS0 measurement voltage setting: 00 = Vlow 01 = Vhigh 10 = 11 = unused
I_PSINH_0_SEL	RW	6	1	0x0	RESET_4	DCS0 measurement current setting: 0 = Ilim_low 1 = Ilim_hi
PAD_V_1	RW	5	1	0x0	RESET_4	DCS1 measurement to compare: 0 = Current 1 = Voltage
PAD_V_0	RW	4	1	0x0	RESET_4	DCS0 measurement to compare: 0 = Current 1 = Voltage
PSINH_EN1	RW	3	1	0x0	RESET_4	DCS1 passenger inhibit usage: 0 = Disabled 1 = Enabled
PSINH_EN0	RW	2	1	0x0	RESET_4	DCS0 passenger inhibit usage: 0 = Disabled 1 = Enabled
PSINH_POL_1	RW	1	1	0x0	RESET_4	DCS1 passenger inhibit polarity: 0 = Inhibit outside window [th_lo,th_hi] 1 = Inhibit inside window [th_lo,th_hi]
PSINH_POL_0	RW	0	1	0x0	RESET_4	DCS0 passenger inhibit polarity:

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						0 = Inhibit outside window [th_lo,th_hi] 1 = Inhibit inside window [th_lo,th_hi]

Table 94. PSINH_DCS0_TH_HI_SAMPLES_CFG - 0x05D

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
PSINH_SAMPLES_MEAS_0	RW	10	6	0x4	RESET_4	Passenger inhibit samples number for up_down counter to change state. From 0 to 63 samples: 000001 = (1 sample) --- 111111 = (63 samples)
PASTHRESH_HI_0	RW	0	10	0x0	RESET_4	Passenger inhibit upper threshold DCS0

Table 95. PSINH_DCS0_TH_LO_CFG - 0x05E

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	10	6	0x0	x	Not used
PASTHRESH_LO_0	RW	0	10	0x0	RESET_4	Passenger inhibit lower threshold DCS0

Table 96. PSINH_DCS1_TH_HI_SAMPLES_CFG - 0x05F

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
PSINH_SAMPLES_MEAS_1	RW	10	6	0x4	RESET_4	Passenger inhibit samples number for up_down counter to change state. From 0 to 63 samples: 000001 = (1 sample) --- 111111 = (63 samples)
PASTHRESH_HI_1	RW	0	10	0x0	RESET_4	Passenger inhibit upper threshold DCS1

Table 97. PSINH_DCS1_TH_LO_CFG - 0x060

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	10	6	0x0	x	Not used
PASTHRESH_LO_1	RW	0	10	0x0	RESET_4	Passenger inhibit lower threshold DCS1

Table 98. SAF_EN_CTRL_PT1 - 0x061

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
EN_SAFx	RW	0	16	0x0	RESET_4	Safing record x (x from 0 to 15) enable

Table 99. **SAF_EN_CTRL_PT2 - 0x062**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	6	10	0x0	x	Not used
EN_SAFx	RW	0	6	0x0	RESET_4	Safing record x (x from 16 to 21) enable

Table 100. **SAF_NODATA_STATUS_PT1 - 0x063**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
NO_VALID_DATA_x	RLR	0	16	0x0	RESET_4	No data valid in safing record x (x from 0 to 15) inside sampling window

Table 101. **SAF_NODATA_STATUS_PT2 - 0x064**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	7	9	0x0	x	Not used
SAF_RAM_CRC_ERR	RLR	6	1	0x0	RESET_4	CRC error in RAM used to store sample for moving average: 0 = No CRC error 1 = CRC error
NO_VALID_DATA_x	RLR	0	6	0x0	RESET_4	No data valid in safing record x (x from 16 to 21) inside sampling window

Table 102. **SAF_REC_ARM_STATUS_PT1 - 0x065**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REC_ARM_STATUS_x	RLR	0	16	0x0	RESET_4	Safing record x (x from 0 to 15) is activating the related ARMINT signals (according to SAF_CONTROL register setting)

Table 103. **SAF_REC_ARM_STATUS_PT2 - 0x066**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	6	10	0x0	x	Not used
SAF_REC_ARM_STATUS_x	RLR	0	6	0x0	RESET_4	Safing record x (x from 16 to 21) is activating the related ARMINT signals (according to SAF_CONTROL register setting)

Table 104. **SAF_EVC_CFG - 0x067**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	10	6	0x0	x	Not used
ARM_TH	RW	6	4	0x3	RESET_4	Event counter threshold to assert arming
SUB_VAL	RW	3	3	0x3	RESET_4	Decremental step size of the event counter
ADD_VAL	RW	0	3	0x3	RESET_4	Incremental step size of the event counter

Table 105. **SAF_CS0_CFG - 0x068**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
CS0_CRC_INIT	RW	8	8	0x0	RESET_4	CRC initialization value of configurable CS x
CS0_CRC_POLY	RW	0	8	0x0	RESET_4	CRC polynomial of configurable CS x

Table 106. **SAF_CS1_CFG - 0x069**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
CS1_CRC_INIT	RW	8	8	0x0	RESET_4	CRC initialization value of configurable CS x
CS1_CRC_POLY	RW	0	8	0x0	RESET_4	CRC polynomial of configurable CS x

Table 107. **SAF_CS2_CFG - 0x06A**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
CS2_CRC_INIT	RW	8	8	0x0	RESET_4	CRC initialization value of configurable CS x
CS2_CRC_POLY	RW	0	8	0x0	RESET_4	CRC polynomial of configurable CS x

Table 108. **SAF_CS3_CFG - 0x06B**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
CS3_CRC_INIT	RW	8	8	0x0	RESET_4	CRC initialization value of configurable CS x
CS3_CRC_POLY	RW	0	8	0x0	RESET_4	CRC polynomial of configurable CS x

Table 109. **SAF_CS4_CFG - 0x06C**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
CS4_CRC_INIT	RW	8	8	0x0	RESET_4	CRC initialization value of configurable CS x
CS4_CRC_POLY	RW	0	8	0x0	RESET_4	CRC polynomial of configurable CS x

Table 110. **SAF_CSX_CFG - 0x06D**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	15	1	0x0	x	Not used
CS4_FORWARD_CRC	RW	14	1	0x0	RESET_4	Forward CRC on configurable CS4: 0 = Polynomial divider (NOT forward) 1 = No polynomial divider (forward)
CS4_IN_FRAME	RW	13	1	0x0	RESET_4	In-frame or out-of-frame configuration for configurable CS4: 0 = OUT of frame 1 = IN frame
CS4_CPHA	RW	12	1	0x0	RESET_4	Clock phase selection for configurable CS4: 0 = CPHA 0 1 = CPHA 1
CS3_FORWARD_CRC	RW	11	1	0x0	RESET_4	Forward CRC on configurable CS3: 0 = Polynomial divider (NOT forward)

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						1 = No polynomial divider (forward)
CS3_IN_FRAME	RW	10	1	0x0	RESET_4	In-frame or out-of-frame configuration for configurable CS3: 0 = OUT of frame 1 = IN frame
CS3_CPHA	RW	9	1	0x0	RESET_4	Clock phase selection for configurable CS3: 0 = CPHA 0 1 = CPHA 1
CS2_FORWARD_CRC	RW	8	1	0x0	RESET_4	Forward CRC on configurable CS2: 0 = Polynomial divider (NOT forward) 1 = No polynomial divider (forward)
CS2_IN_FRAME	RW	7	1	0x0	RESET_4	In-frame or out-of-frame configuration for configurable CS2: 0 = OUT of frame 1 = IN frame
CS2_CPHA	RW	6	1	0x0	RESET_4	Clock phase selection for configurable CS2: 0 = CPHA 0 1 = CPHA 1
CS1_FORWARD_CRC	RW	5	1	0x0	RESET_4	Forward CRC on configurable CS1: 0 = Polynomial divider (NOT forward) 1 = No polynomial divider (forward)
CS1_IN_FRAME	RW	4	1	0x0	RESET_4	In-frame or out-of-frame configuration for configurable CS1: 0 = OUT of frame 1 = IN frame
CS1_CPHA	RW	3	1	0x0	RESET_4	Clock phase selection for configurable CS1: 0 = CPHA 0 1 = CPHA 1
CS0_FORWARD_CRC	RW	2	1	0x0	RESET_4	Forward CRC on configurable CS0: 0 = Polynomial divider (NOT forward) 1 = No polynomial divider (forward)
CS0_IN_FRAME	RW	1	1	0x0	RESET_4	In-frame or out-of-frame configuration for configurable CS0: 0 = OUT of frame 1 = IN frame
CS0_CPHA	RW	0	1	0x0	RESET_4	Clock phase selection for configurable CS0: 0 = CPHA 0 1 = CPHA 1

Table 111. NOP_GID_001 - 0x07F

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	0	16	0x0	x	No operation response

5.1.2.3 *Deploy config and diag registers (GID = 010)*

Table 112. DEP_AUTOPROF_CFG - 0x080

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_AUTOPROF_x	RW	0	16	0x0	RESET_4	Automatic profile deployment mode selection on channel x (x from 0 to 15): 0 = OFF 1 = ON

Table 113. DEP_DIAG_ADC_A - 0x081

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
NEWDATA_A	RLR	15	1	0x0	RESET_4	1 = New data available from conversion
DEP_DIAG_ADC_RES_A	RO	5	10	0x0	RESET_4	10-bit ADC result value corresponding to DEP_DIAG_ADC_REQ_A request
DEP_DIAG_ADC_REQ_A	RW	0	5	0x0	RESET_4	ADC request select command

Table 114. DEP_DIAG_ADC_B - 0x082

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
NEWDATA_B	RLR	15	1	0x0	RESET_4	1 = New data available from conversion
DEP_DIAG_ADC_RES_B	RO	5	10	0x0	RESET_4	10-bit ADC result value corresponding to DEP_DIAG_ADC_REQ_A request
DEP_DIAG_ADC_REQ_B	RW	0	5	0x0	RESET_4	ADC request select command

Table 115. DEP_DIAG_CTRL_A - 0x083

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	13	3	0x0	x	Not used
DEP_ISINK_PIN_SEL_CH_5	RW	12	1	0x0	RESET_4	Selection of ISINK current redirection for channel 5: 0 = ISINK on SR5 1 = ISINK on SF5
DEP_ISINK_PIN_SEL_CH_3	RW	11	1	0x0	RESET_4	Selection of ISINK current redirection for channel 3: 0 = ISINK on SR3 1 = ISINK on SF3
DEP_MUX_LRM_SEL	RW	9	2	0x0	RESET_4	Enable connection of differential amplifier for load resistance measurement: 00 = Not connected 01 = Connected on pins SRx/SFx on channel selected by DEP_CH_SEL_DIAG_CTRL_A 10 = Connected on pins SFx/SFy on channel selected by DEP_CH_SEL_DIAG_CTRL_A (selection valid only for CSR channels)

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						11 = Not used
DEP_ISINK_A_EN	RW	8	1	0x0	RESET_4	Enable ISINK current on channel selected by DEP_CH_SEL_DIAG_CTRL_A: 0 = OFF 1 = ON
DEP_ISRC_PIN_SEL	RW	7	1	0x0	RESET_4	Selection of ISRC current redirection for channel selected by DEP_CH_SEL_DIAG_CTRL_A: 0 = ISRC on SFx 1 = ISRC on SRx
DEP_ISRC_SLEW_RATE_SEL	RW	6	1	0x0	RESET_4	Selection of ISRC current slew rate: 0 = 200 µA/µs 1 = Slew rate not controlled
DEP_ISRC_EN	RW	5	1	0x0	RESET_4	Enable ISRC current on channel selected by DEP_CH_SEL_DIAG_CTRL_A: 0 = OFF 1 = ON
DEP_ISRC_VAL_SEL	RW	4	1	0x0	RESET_4	Selection of ISRC current value: 0 = 40 mA 1 = 8 mA
DEP_CH_SEL_DIAG_CTRL_A	RW	0	4	0x0	RESET_4	Measurement channel selection: 0000 = Channel 0 0001 = Channel 1 0010 = Channel 2 0011 = Channel 3 0100 = Channel 4 0101 = Channel 5 0110 = Channel 6 0111 = Channel 7 1000 = Channel 8 1001 = Channel 9 1010 = Channel 10 1011 = Channel 11 1100 = Channel 12 1101 = Channel 13 1110 = Channel 14 1111 = Channel 15

Table 116. DEP_DIAG_CTRL_B - 0x084

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEL_LEA_FLT_SEL	RW	14	2	0x0	RESET_4	Filter time selection for LEA diagnostic filter time: 00 =1 µs 01 =2 µs

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						10 =4 µs 11 =8 µs
DEP_LEA_POL_SEL	RW	13	1	0x0	RESET_4	Selection of polarity for LEA diag test: 0 = LEA reverse test 1 = LEA forward test
DEP_LEA_CH_SEL	RW	11	2	0x0	RESET_4	Channel selection for LEA diag test: 00 = No channel 01 = Channel 6 10 = Channel 7 11 = Not used
DEP_LEA_TH_SEL	RW	10	1	0x0	RESET_4	Threshold selection for LEA diag test: 0 = 1 V 1 = 0.5 V
DEP_LEA_DIAG_TEST_EN	RW	9	1	0x0	RESET_4	Enable and run LEA diag test (ISRC on the selected channel is switched on too): 0 = OFF 1 = ON
DEP_CUR_ADC_RANGE_SEL	RW	8	1	0x0	RESET_4	Selection of current ADC range: 0 = 500 µA-6.5 mA 1 = 100 µA-0.9 mA
DEP_VRCM_OUT_SEL	RW	7	1	0x0	RESET_4	Selection of VRCM regulated output: 0 = 2.5 V 1 = 1.5 V
DEP_MUX_VRCM_SEL	RW	5	2	0x0	RESET_4	Enable connection of VRCM: 00 = Not connected 01 = VRCM output connected on pin SRx on channel selected by DEP_CH_SEL_DIAG_CTRL_B 10 = VRCM output connected on pin SFx on channel selected by DEP_CH_SEL_DIAG_CTRL_B 11 = Not used
DEP_ISINK_B_EN	RW	4	1	0x0	RESET_4	Enable ISINK current on channel selected by DEP_CH_SEL_DIAG_CTRL_B 0 = OFF 1 = ON
DEP_CH_SEL_DIAG_CTRL_B	RW	0	4	0x0	RESET_4	Measurement channel selection: 0000 = Channel 0 0001 = Channel 1 0010 = Channel 2 0011 = Channel 3 0100 = Channel 4 0101 = Channel 5 0110 = Channel 6 0111 = Channel 7

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						1000 = Channel 8 1001 = Channel 9 1010 Channel 10 1011 = Channel 11 1100 = Channel 12 1101 = Channel 13 1110 = Channel 14 1111 = Channel 15

Table 117. DEP_DIAG_STATUS_0 - 0x085

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_MUX_VRCM_SEL	RO	14	2	0x0	RESET_4	Feedback of connection of VRCM MUX
DEP_CH_SEL_DIAG_CTRL_B	RO	10	4	0x0	RESET_4	Feedback of selected channel
DEP_MUX_LRM_SEL	RO	8	2	0x0	RESET_4	Feedback of connection of LRM amplifier
DEP_CH_SEL_DIAG_CTRL_A	RO	4	4	0x0	RESET_4	Feedback of selected channel
DEP_DIAG_VRCM_STG	RO	3	1	0x0	RESET_4	Short to ground test status: 0 = STG not detected 1 = STG detected
DEP_DIAG_VRCM_STB	RO	2	1	0x0	RESET_4	Short to battery test status: 0 = STB not detected 1 = STB detected
DEP_DIAG_H_RES	RO	1	1	0x0	RESET_4	High resistance test feedback: 0 = R < Rhigh 1 = R > Rhigh
DEP_DIAG_L_RES	RO	0	1	0x0	RESET_4	Low resistance test feedback: 0 = R > Rlow 1 = R < Rlow

Table 118. DEP_DIAG_STATUS_1 - 0x086

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	7	0x0	x	Not used
DEP_LEA_POL_SEL	RO	8	1	0x0	RESET_4	Feedback of polarity for LEA diag test
DEP_LEA_CH_SEL	RO	6	2	0x0	RESET_4	Feedback of selected channel for LEA test
DEP_LEA_TH_SEL	RO	5	1	0x0	RESET_4	Feedback of selected threshold for LEA test
UNUSED	RO	4	1	0x0	x	Not used
DEP_DIAG_FET_ON	RO	3	1	0x0	RESET_4	FET activation during diagnostic: 0 = FET is off during diagnostic 1 = FET is on during diagnostic

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_DIAG_LEA_TIP	RO	2	1	0x0	RESET_4	LEA diag test in progress: 0 = Test finished or not started 1 = Test in progress
DEP_DIAG_LEA_REV	RO	1	1	0x0	RESET_4	0 = LEA inductance not present OR (LEA inductance present AND (LEA diode short circuit OR LEA diode connection reversed) 1 = LEA inductance present AND (LEA diode blocking OR LEA diode open circuit)
DEP_DIAG_LEA_FWD	RO	0	1	0x0	RESET_4	0 = LEA inductance not present OR (LEA inductance present AND (LEA diode shorted OR LEA diode forward active clamping) 1 = LEA inductance present AND (LEA diode open circuit OR LEA diode connection reversed)

Table 119. SS_PD_CTRL - 0x087

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SS_PD_EN_x	RW	0	16	0x0	RESET_4	Squib supply pull-down enable on channel x (x from 0 to 15): 0 = OFF 1 = ON

Table 120. SR_SF_PD_CTRL - 0x088

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SR_SF_PD_DIS_x	RW	0	16	0x0	RESET_4	Pull-down current control on SRx and SFx (x from 0 to 15): 0 = ON 1 = OFF

Table 121. VSF0_CTRL - 0x089

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	2	14	0x0	x	Not used
PSINH_VSF0	RW	1	1	0x0	RESET_4	VSF0 regulator sensitivity to PSINH latched state: 0 = OFF 1 = ON
UNUSED	RO	0	1	0x0	x	Not used

Table 122. VSF1_CTRL - 0x08A

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	2	14	0x0	x	Not used
PSINH_VSF1	RW	1	1	0x0	RESET_4	VSF1 regulator sensitivity to PSINH latched state:

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						0 = OFF 1 = ON
UNUSED	RO	0	1	0x0	x	Not used

Table 123. DEP_CMT_H_CTRL - 0x08B

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
START_CMT_H_x	WO	0	16	0x0	RESET_4	High current monitor test for channel x (x from 0 to 15): 1 = Start the high current monitor counter 0 = No effect

Table 124. DEP_CMT_L_CTRL - 0x08C

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
START_CMT_L_x	WO	0	16	0x0	RESET_4	Low current monitor test for channel x (x from 0 to 15): 1 = Start the low current monitor counter 0 = No effect

Table 125. DEP_DWELL_CTRL - 0x08D

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
START_DWELL_x	WO	0	16	0x0	RESET_4	Dwell test for channel x (x from 0 to 15): 1 = start the Dwell counter 0 = No effect

Table 126. DEP_CMT_0 - 0x08E

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_CMT_H_0	RO	8	8	0x0	RESET_4	Deployment high current monitor timer value: LSB = 16 µs
DEP_CMT_L_0	RO	0	8	0x0	RESET_4	Deployment low current monitor timer value: LSB = 16 µs

Table 127. DEP_CMT_1 - 0x08F

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_CMT_H_1	RO	8	8	0x0	RESET_4	Deployment high current monitor timer value: LSB = 16 µs
DEP_CMT_L_1	RO	0	8	0x0	RESET_4	Deployment low current monitor timer value: LSB = 16 µs

Table 128. **DEP_CMT_2 - 0x090**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_CMT_H_2	RO	8	8	0x0	RESET_4	Deployment high current monitor timer value: LSB = 16 µs
DEP_CMT_L_2	RO	0	8	0x0	RESET_4	Deployment low current monitor timer value: LSB = 16 µs

Table 129. **DEP_CMT_3 - 0x091**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_CMT_H_3	RO	8	8	0x0	RESET_4	Deployment high current monitor timer value: LSB = 16 µs
DEP_CMT_L_3	RO	0	8	0x0	RESET_4	Deployment low current monitor timer value: LSB = 16 µs

Table 130. **DEP_CMT_4 - 0x092**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_CMT_H_4	RO	8	8	0x0	RESET_4	Deployment high current monitor timer value: LSB = 16 µs
DEP_CMT_L_4	RO	0	8	0x0	RESET_4	Deployment low current monitor timer value: LSB = 16 µs

Table 131. **DEP_CMT_5 - 0x093**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_CMT_H_5	RO	8	8	0x0	RESET_4	Deployment high current monitor timer value: LSB = 16 µs
DEP_CMT_L_5	RO	0	8	0x0	RESET_4	Deployment low current monitor timer value: LSB = 16 µs

Table 132. **DEP_CMT_6 - 0x094**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_CMT_H_6	RO	8	8	0x0	RESET_4	Deployment high current monitor timer value: LSB = 16 µs
DEP_CMT_L_6	RO	0	8	0x0	RESET_4	Deployment low current monitor timer value: LSB = 16 µs

Table 133. **DEP_CMT_7 - 0x095**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_CMT_H_7	RO	8	8	0x0	RESET_4	Deployment high current monitor timer value: LSB = 16 µs
DEP_CMT_L_7	RO	0	8	0x0	RESET_4	Deployment low current monitor timer value: LSB = 16 µs

Table 134. **DEP_CMT_8 - 0x096**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_CMT_H_8	RO	8	8	0x0	RESET_4	Deployment high current monitor timer value: LSB = 16 µs
DEP_CMT_L_8	RO	0	8	0x0	RESET_4	Deployment low current monitor timer value: LSB = 16 µs

Table 135. **DEP_CMT_9 - 0x097**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_CMT_H_9	RO	8	8	0x0	RESET_4	Deployment high current monitor timer value: LSB = 16 µs
DEP_CMT_L_9	RO	0	8	0x0	RESET_4	Deployment low current monitor timer value: LSB = 16 µs

Table 136. **DEP_CMT_10 - 0x098**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_CMT_H_10	RO	8	8	0x0	RESET_4	Deployment high current monitor timer value: LSB = 16 µs
DEP_CMT_L_10	RO	0	8	0x0	RESET_4	Deployment low current monitor timer value: LSB = 16 µs

Table 137. **DEP_CMT_11 - 0x099**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_CMT_H_11	RO	8	8	0x0	RESET_4	Deployment high current monitor timer value: LSB = 16 µs
DEP_CMT_L_11	RO	0	8	0x0	RESET_4	Deployment low current monitor timer value: LSB = 16 µs

Table 138. **DEP_CMT_12 - 0x09A**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_CMT_H_12	RO	8	8	0x0	RESET_4	Deployment high current monitor timer value: LSB = 16 µs
DEP_CMT_L_12	RO	0	8	0x0	RESET_4	Deployment low current monitor timer value: LSB = 16 µs

Table 139. **DEP_CMT_13 - 0x09B**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_CMT_H_13	RO	8	8	0x0	RESET_4	Deployment high current monitor timer value: LSB = 16 µs
DEP_CMT_L_13	RO	0	8	0x0	RESET_4	Deployment low current monitor timer value: LSB = 16 µs

Table 140. **DEP_CMT_14 - 0x09C**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_CMT_H_14	RO	8	8	0x0	RESET_4	Deployment high current monitor timer value: LSB = 16 µs
DEP_CMT_L_14	RO	0	8	0x0	RESET_4	Deployment low current monitor timer value: LSB = 16 µs

Table 141. **DEP_CMT_15 - 0x09D**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_CMT_H_15	RO	8	8	0x0	RESET_4	Deployment high current monitor timer value: LSB = 16 µs
DEP_CMT_L_15	RO	0	8	0x0	RESET_4	Deployment low current monitor timer value: LSB = 16 µs

Table 142. **DEP_CFG_A - 0x09E**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	13	3	0x0	x	Not used
DEP_CFG_ERR_A	RO	12	1	0x0	RESET_4	Deployment configuration error: 0 = NO FAULT 1 = FAULT
DEP_EXPIRE_TIME_A	RW	10	2	0x0	RESET_4	Deployment command expiration timer: 00 = 500 ms 01 = 250 ms 10 = 125 ms 11 = 0 ms
DEP_DWELL_TIME_A	RW	2	8	0x0	RESET_4	Deployment dwell time: 000000 = INVALID OTHERS = DEPLOYMENT DWELL TIME (LSB = 16 µs)
DEP_CURRENT_A	RW	0	2	0x0	RESET_4	Deployment current value: 00 = INVALID 01 = LOW CURRENT 10 = HIGH CURRENT 11 = INVALID

Table 143. **DEP_CFG_B - 0x09F**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	13	3	0x0	x	Not used
DEP_CFG_ERR_B	RO	12	1	0x0	RESET_4	Deployment configuration error: 0 = NO FAULT 1 = FAULT

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_EXPIRE_TIME_B	RW	10	2	0x0	RESET_4	Deployment command expiration timer: 00 = 500 ms 01 = 250 ms 10 = 125 ms 11 = 0 ms
DEP_DWELL_TIME_B	RW	2	8	0x0	RESET_4	Deployment dwell time: 000000 = INVALID OTHERS = DEPLOYMENT DWELL TIME (LSB = 16 µs)
DEP_CURRENT_B	RW	0	2	0x0	RESET_4	Deployment current value: 00 = INVALID 01 = LOW CURRENT 10 = HIGH CURRENT 11 = INVALID

Table 144. DEP_CFG_C - 0x0A0

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	13	3	0x0	x	Not used
DEP_CFG_ERR_C	RO	12	1	0x0	RESET_4	Deployment configuration error: 0 = NO FAULT 1 = FAULT
DEP_EXPIRE_TIME_C	RW	10	2	0x0	RESET_4	Deployment command expiration timer: 00 = 500 ms 01 = 250 ms 10 = 125 ms 11 = 0 ms
DEP_DWELL_TIME_C	RW	2	8	0x0	RESET_4	Deployment dwell time: 000000 = INVALID OTHERS = DEPLOYMENT DWELL TIME (LSB = 16 µs)
DEP_CURRENT_C	RW	0	2	0x0	RESET_4	Deployment current value: 00 = INVALID 01 = LOW CURRENT 10 = HIGH CURRENT 11 = INVALID

Table 145. DEP_CFG_D - 0x0A1

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	13	3	0x0	x	Not used
DEP_CFG_ERR_D	RO	12	1	0x0	RESET_4	Deployment configuration error: 0 = NO FAULT

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						1 = FAULT
DEP_EXPIRE_TIME_D	RW	10	2	0x0	RESET_4	Deployment command expiration timer: 00 = 500 ms 01 = 250 ms 10 = 125 ms 11 = 0 ms
DEP_DWELL_TIME_D	RW	2	8	0x0	RESET_4	Deployment dwell time: 000000 = INVALID OTHERS = DEPLOYMENT DWELL TIME (LSB = 16 µs)
DEP_CURRENT_D	RW	0	2	0x0	RESET_4	Deployment current value: 00 = INVALID 01 = LOW CURRENT 10 = HIGH CURRENT 11 = INVALID

Table 146. DEP_PROF1_MATRIX_L0_7 - 0x0A2

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_PROF1_Lx	RW	0	16	0x0	RESET_4	Deployment current profile 1 assignment to channel x (x from 0 to 7): 00 = CFG A 01 = CFG B 10 = CFG C 11 = CFG D

Table 147. DEP_PROF1_MATRIX_L8_15 - 0x0A3

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_PROF1_Lx	RW	0	16	0x0	RESET_4	Deployment current profile 1 assignment to channel x (x from 8 to 15): 00 = CFG A 01 = CFG B 10 = CFG C 11 = CFG D

Table 148. DEP_CTRL - 0x0A4

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	13	3	0x0	x	Not used
DEP_CMT_MODE	RW	12	1	0x0	RESET_4	Deployment current monitor mode selection: 0 = CUMULATIVE 1 = MAX UNINTERRUPTED

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_CFG_SEL_CH45	RW	11	1	0x0	RESET_4	Topology selection for channels 4-5: 0 = Standard connection (SRx separated) 1 = Common SRx connection
DEP_CFG_SEL_CH23	RW	10	1	0x0	RESET_4	Topology selection for channels 2-3: 0 = Standard connection (SRx separated) 1 = Common SRx connection
DEP_LOAD_SEL_CH7	RW	9	1	0x0	RESET_4	Load selection for channel 7: 0 = LEA 1 = SQUIB
DEP_LOAD_SEL_CH6	RW	8	1	0x0	RESET_4	Load selection for channel 6: 0 = LEA 1 = SQUIB
DEP_ADC_MEAS_SAMPLE	RW	6	2	0x2	RESET_4	Sample number in deployment voltage measurement conversions: 00 = 4 samples 01 = 16 samples 10 = 8 samples 11 = 1 sample
ER_BYP_EN	RW	5	1	0x0	RESET_4	ER bypass switch enable: 0 = OFF 1 = ON
VSF_D_PD_EN	RW	4	1	0x0	RESET_4	VSF_D pull-down enable: 0 = OFF 1 = ON
TEST_CODE	RW	0	4	0x0	RESET_4	0001 = VSF0 TEST 0010 = VSF1 TEST 0011 = VSF0 VSF1 TEST 0100 = HS FET TEST 0101 = LS FET TEST 0110 = DEP_CMD SET 1001 = DEP_CMD_N SET OTHERS = NO TEST

Table 149. DEP_CMD - 0x0A5

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_CMD_x	WO	0	16	0x0	RESET_4	Selects channel x (x from 0 to 15) for deployment: 0 = NO 1 = YES (WO exception: DEP_CMD_0 echo state)

Table 150. **DEP_CMD_N - 0x0A6**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_CMD_N_x	WO	0	16	0x0	RESET_4	Selects channel x (x from 0 to 15) for deployment: 0 = NO 1 = YES (WO exception: DEP_CMD_0 echo state)

Table 151. **DEP_EN_CTRL - 0x0A7**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_EN_CMD	WO	0	16	0x0	RESET_4	MOSI: 0F0F = LOCK F0F0 = UNLOCK (WO exception: DEP_ENABLED state updated according to deployment enable state machine)

Table 152. **DEP_DIS - 0x0A8**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_DIS_x	RW	0	16	0x0	RESET_4	Selects channel x (x from 0 to 15) for deployment disable: 0 = NO 1 = YES

Table 153. **LOOP_MATRIX_ARM0 - 0x0A9**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
ARM0_Lx	RW	0	16	0x0	RESET_4	Assignment of ARM_RSLT_0 to channel x (x from 0 to 15): 0 = NO 1 = YES

Table 154. **LOOP_MATRIX_ARM1 - 0x0AA**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
ARM1_Lx	RW	0	16	0x0	RESET_4	Assignment of ARM_RSLT_1 to channel x (x from 0 to 15): 0 = NO 1 = YES

Table 155. **LOOP_MATRIX_ARM2 - 0x0AB**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
ARM2_Lx	RW	0	16	0x0	RESET_4	Assignment of ARM_RSLT_2 to channel x (x from 0 to 15): 0 = NO 1 = YES

Table 156. **LOOP_MATRIX_ARM3 - 0x0AC**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
ARM3_Lx	RW	0	16	0x0	RESET_4	Assignment of ARM_RSLT_3 to channel x (x from 0 to 15): 0 = NO 1 = YES

Table 157. **LOOP_MATRIX_ARM4 - 0x0AD**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
ARM4_Lx	RW	0	16	0x0	RESET_4	Assignment of ARM_RSLT_4 to channel x (x from 0 to 15): 0 = NO 1 = YES

Table 158. **LOOP_MATRIX_ARM5 - 0x0AE**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
ARM5_Lx	RW	0	16	0x0	RESET_4	Assignment of ARM_RSLT_5 to channel x (x from 0 to 15): 0 = NO 1 = YES

Table 159. **LOOP_MATRIX_ARM6 - 0x0AF**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
ARM6_Lx	RW	0	16	0x0	RESET_4	Assignment of ARM_RSLT_6 to channel x (x from 0 to 15): 0 = NO 1 = YES

Table 160. **LOOP_MATRIX_ARM7 - 0x0B0**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
ARM7_Lx	RW	0	16	0x0	RESET_4	Assignment of ARM_RSLT_7 to channel x (x from 0 to 15):

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						0 = NO 1 = YES

Table 161. **LOOP_MATRIX_PSINH - 0x0B1**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
PSINH_Lx	RW	0	16	0x0	RESET_4	Assignment of PSINH_RSLT_LATCHED to channel x (x from 0 to 15): 0 = NO 1 = YES

Table 162. **DEP_STATUS_0_7 - 0x0B2**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_FINISHED_7	RO	15	1	0x0	RESET_4	Deployment event finished on channel 7: 0 = NO 1 = YES
DEP_RUNNING_7	RO	14	1	0x0	RESET_4	Deployment event running on channel 7: 0 = NO 1 = YES
DEP_FINISHED_6	RO	13	1	0x0	RESET_4	Deployment event finished on channel 6: 0 = NO 1 = YES
DEP_RUNNING_6	RO	12	1	0x0	RESET_4	Deployment event running on channel 6: 0 = NO 1 = YES
DEP_FINISHED_5	RO	11	1	0x0	RESET_4	Deployment event finished on channel 5: 0 = NO 1 = YES
DEP_RUNNING_5	RO	10	1	0x0	RESET_4	Deployment event running on channel 5: 0 = NO 1 = YES
DEP_FINISHED_4	RO	9	1	0x0	RESET_4	Deployment event finished on channel 4: 0 = NO 1 = YES
DEP_RUNNING_4	RO	8	1	0x0	RESET_4	Deployment event running on channel 4: 0 = NO 1 = YES
DEP_FINISHED_3	RO	7	1	0x0	RESET_4	Deployment event finished on channel 3: 0 = NO 1 = YES
DEP_RUNNING_3	RO	6	1	0x0	RESET_4	Deployment event running on channel 3: 0 = NO

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						1 = YES
DEP_FINISHED_2	RO	5	1	0x0	RESET_4	Deployment event finished on channel 2: 0 = NO 1 = YES
DEP_RUNNING_2	RO	4	1	0x0	RESET_4	Deployment event running on channel 2: 0 = NO 1 = YES
DEP_FINISHED_1	RO	3	1	0x0	RESET_4	Deployment event finished on channel 1: 0 = NO 1 = YES
DEP_RUNNING_1	RO	2	1	0x0	RESET_4	Deployment event running on channel 1: 0 = NO 1 = YES
DEP_FINISHED_0	RO	1	1	0x0	RESET_4	Deployment event finished on channel 0: 0 = NO 1 = YES
DEP_RUNNING_0	RO	0	1	0x0	RESET_4	Deployment event running on channel 0: 0 = NO 1 = YES

Table 163. DEP_STATUS_8_15 - 0x0B3

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_FINISHED_15	RO	15	1	0x0	RESET_4	Deployment event finished on channel 15: 0 = NO 1 = YES
DEP_RUNNING_15	RO	14	1	0x0	RESET_4	Deployment event running on channel 15: 0 = NO 1 = YES
DEP_FINISHED_14	RO	13	1	0x0	RESET_4	Deployment event finished on channel 14: 0 = NO 1 = YES
DEP_RUNNING_14	RO	12	1	0x0	RESET_4	Deployment event running on channel 14: 0 = NO 1 = YES
DEP_FINISHED_13	RO	11	1	0x0	RESET_4	Deployment event finished on channel 13: 0 = NO 1 = YES
DEP_RUNNING_13	RO	10	1	0x0	RESET_4	Deployment event running on channel 13: 0 = NO 1 = YES
DEP_FINISHED_12	RO	9	1	0x0	RESET_4	Deployment event finished on channel 12: 0 = NO 1 = YES

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_RUNNING_12	RO	8	1	0x0	RESET_4	Deployment event running on channel 12: 0 = NO 1 = YES
DEP_FINISHED_11	RO	7	1	0x0	RESET_4	Deployment event finished on channel 11: 0 = NO 1 = YES
DEP_RUNNING_11	RO	6	1	0x0	RESET_4	Deployment event running on channel 11: 0 = NO 1 = YES
DEP_FINISHED_10	RO	5	1	0x0	RESET_4	Deployment event finished on channel 10: 0 = NO 1 = YES
DEP_RUNNING_10	RO	4	1	0x0	RESET_4	Deployment event running on channel 10: 0 = NO 1 = YES
DEP_FINISHED_9	RO	3	1	0x0	RESET_4	Deployment event finished on channel 9: 0 = NO 1 = YES
DEP_RUNNING_9	RO	2	1	0x0	RESET_4	Deployment event running on channel 9: 0 = NO 1 = YES
DEP_FINISHED_8	RO	1	1	0x0	RESET_4	Deployment event finished on channel 8: 0 = NO 1 = YES
DEP_RUNNING_8	RO	0	1	0x0	RESET_4	Deployment event running on channel 8: 0 = NO 1 = YES

Table 164. DEP_DIAG_SG_LOSS - 0x0B4

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_DIAG_SG_LOSS_x	RLR	0	16	0x0	RESET_4	Squib ground loss flag on channel x (x from 0 to 15): 0 = NO FAULT 1 = FAULT

Table 165. DEP_DIAG_OC - 0x0B5

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_DIAG_OC_x	RLR	0	16	0x0	RESET_4	LS overcurrent flag on channel x (x from 0 to 15): 0 = NO FAULT 1 = FAULT

Table 166. **DEP_AUTO_SAFE_CTRL - 0x0B6**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEP_AUTO_SAFE_x	WO	0	1'6	0x0	RESET_4	Safe autoprof test for channel x (x from 0 to 15): 1 = Start the autoprof safe counter 0 = No effect

Table 167. **DEP_DIAG_SS_OV - 0x0B7**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	7	0x0	x	Unused
DEP_DIAG_SS_OV_x_y	RLR	2	7	0x0	RESET_4	Squib supply overvoltage flag on channel x_y (x_y = 2_3, 4_5, 6_7, 8_9, 10_11, 12_13, 14_15): 0 = NO FAULT 1 = FAULT
DEP_DIAG_SS_OV_x	RLR	0	2	0x0	RESET_4	Squib supply overvoltage flag on channel x (x from 0 to 1): 0 = NO FAULT 1 = FAULT

Table 168. **DEP_DIAG_CHECK - 0x0B8**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	12	4	0x0	x	Not used
DEP_CMP_CHECK	RW	11	1	0x0	RESET_4	Deployment comparator check: 0 = Deployment comparator threshold SS_OV and GG_LOSSx normal behavior 1 = Deplomentcomparator threshold SS_OV and SG_LOSSx are inverted
DEP_ABIST_COMPLETED	RO	10	1	0x0	RESET_4	Deployment analog bist status: 0 = Running 1 = Completed
DEP_ABIST_ERR	RO	9	1	0x0	RESET_4	Deployment analog bist error: 0 = NO 1 = YES
DEP_ABIST_CMD	WO	8	1	0x0	RESET_4	Deployment analog bist command: 0 = NO 1 = YES
DEP_VRCM_SELFTEST_SEL	RW	7	1	0x0	RESET_4	Selection of VRCM STB and STG thresholds for selftest: 0 = Leakage diag 1 = FET test
DEP_VRCM_STG_SELFTEST_EN	RW	6	1	0x0	RESET_4	Enable VRCM STG selftest: 0 = OFF

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						1 = ON
DEP_VRCM_STB_SELFTEST_EN	RW	5	1	0x0	RESET_4	Enable VRCM STB selftest: 0 = OFF 1 = ON
DEP_ISRC_CHECK_EN	RW	4	1	0x0	RESET_4	Enable ISRC check on channel selected by DEP_ISRC_CHECK_CH_SEL: 0 = OFF 1 = ON
DEP_ISRC_CHECK_CH_SEL	RW	0	4	0x0	RESET_4	Measurement channel selection: 0000 = Channel 0 0001 = Channel 1 0010 = Channel 2 0011 = Channel 3 0100 = Channel 4 0101 = Channel 5 0110 = Channel 6 0111 = Channel 7 1000 = Channel 8 1001 = Channel 9 1010 = Channel 10 1011 = Channel 11 1100 = Channel 12 1101 = Channel 13 1110 = Channel 14 1111 = Channel 15

Table 169. DEP_CRC_CTRL - 0x0B9

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
CRC_ERR_DEP	RLR	15	1	0x0	RESET_4	CRC error flag: 0 = CRC error is not present 1 = CRC error is present
UNUSED	RO	13	2	0x0	x	Not used
CRC_EXP_DEP	RO	1	12	0x0	RESET_4	CRC to be matched (computed internally by the device after RECALC command is set)
RECALC_DEP	WO	0	1	0x0	RESET_4	CRC calculation restart: 1 = Request the recalculation of the CRC 0 = No action

Table 170. DEP_DIAG_SS_OV_DIS - 0x0BA

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	10	6	0x0	x	Not used

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SS_OV_DEP_INH_CTRL	RW	9	1	0x0	RESET_4	0 = SS_OV filter output used as the signal to inhibit deployment 1 = SS_OV latched output used as the signal to inhibit deployment (same behavior as BA silicon)
DEP_DIAG_SS_OV_DIS_x_y	RW	2	7	0x0	RESET_4	Disable squib supply overvoltage effect during deployment: 0 = ENABLE 1 = DISABLE
DEP_DIAG_SS_OV_DIS_x	RW	0	2	0x0	RESET_4	Disable squib supply overvoltage effect during deployment: 0 = ENABLE 1 = DISABLE

Table 171. NOP_GID_010 - 0x0BF

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	0	16	0x0	x	No operation response

5.1.2.4 *Safing 1 registers (GID = 011)*

Table 172. SAF_REC0_CTRL_PT1 - 0x0C0

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	15	1	0x0	x	Not used
ARM_METHOD	RW	14	1	0x0	RESET_4	ARMING method based on valid sensor data: 0 = EVC 1 = Moving average
ARM_STRETCHER	RW	11	3	0x0	RESET_4	Safing stretcher dwell extension time select: 000 = 32 ms 001 = 128 ms 010 = 256 ms 011 = 512 ms 100 = 2048 ms 101 = 4096 ms others = 256 ms
ARMx	RW	3	8	0x0	RESET_4	ARMINT_x (x from 0 to 7) select for safing record 0
SAF_CS_SELECTION	RW	0	3	0x0	RESET_4	SPI CS select: 001 = SAF_CS0 010 = SAF_CS1 011 = SAF_CS2 100 = SAF_CS3 101 = SAF_CS4 110 = RS_CS_SPI

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						000 or 111 = None assigned CS

Table 173. **SAF_REC0_CTRL_PT2 - 0x0C1**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	2	0x0	x	Not used
RANGE_CHECK_EN	RW	13	1	0x0	RESET_4	Data range limit enable: 0 = Data range limit disabled 1 = Data range limit enabled
SENSOR_TYPE	RW	12	1	0x0	RESET_4	Sensor data type: 0 = Signed 1 = Unsigned
PED_PRO	RW	11	1	0x0	RESET_4	Pedestrian protection sensor validation range: 0 = Standard 1 = Limited
DOWNSAMPLE	RW	9	2	0x0	RESET_4	Downsampling factor n: 00 = No down 01 = 2 10 = 4 11 = 8
NO_DATA_EVCNT	RW	8	1	0x0	RESET_4	No data event counter: 0 = Reset 1 = Subtract
NO_DATA_MA	RW	7	1	0x0	RESET_4	No data moving average: 0 = Use 0 1 = Use last known value
HPF_SHIFT_FACTOR	RW	4	3	0x0	RESET_4	Value N of high pass filter: from 000 = 12 to 101 = 17
HPF_BYPASS	RW	3	1	0x0	RESET_4	Sensor offset processing: 0 = High pass filter is used 1 = High pass filter is bypassed
PSEUDO_4K_SENSOR	RW	2	1	0x0	RESET_4	PSI5 sensor sampling pseudo 4 kHz: 0 = Standard PSI5 sensor 1 = Sensor sampling pseudo 4K
AMA_SAMPLES	RW	0	2	0x0	RESET_4	Moving average sample size: 00 = 2 01 = 4 10 = 8 11 = 16

Table 174. **SAF_REC1_CTRL_PT1 - 0x0C2**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	15	1	0x0	x	Not used
ARM_METHOD	RW	14	1	0x0	RESET_4	ARMING method based on valid sensor data: 0 = EVC 1 = Moving average
ARM_STRETCHER	RW	11	3	0x0	RESET_4	Safing stretcher dwell extension time select: 000 = 32 ms 001 = 128 ms 010 = 256 ms 011 = 512 ms 100 = 2048 ms 101 = 4096 ms others = 256 ms
ARMx	RW	3	8	0x0	RESET_4	ARMINT_x (x from 0 to 7) select for safing record 1
SAF_CS_SELECTION	RW	0	3	0x0	RESET_4	SPI CS select: 001 = SAF_CS0 010 = SAF_CS1 011 = SAF_CS2 100 = SAF_CS3 101 = SAF_CS4 110 = RS_CS_SPI 000 or 111 = None assigned CS

Table 175. **SAF_REC1_CTRL_PT2 - 0x0C3**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	2	0x0	x	Not used
RANGE_CHECK_EN	RW	13	1	0x0	RESET_4	Data range limit enable: 0 = Data range limit disabled 1 = Data range limit enabled
SENSOR_TYPE	RW	12	1	0x0	RESET_4	Sensor data type: 0 = Signed 1 = Unsigned
PED_PRO	RW	11	1	0x0	RESET_4	Pedestrian protection sensor validation range: 0 = Standard 1 = Limited
DOWNSAMPLE	RW	9	2	0x0	RESET_4	Downsampling factor n: 00 = No down 01 = 2 10 = 4 11 = 8
NO_DATA_EVCNT	RW	8	1	0x0	RESET_4	No data event counter:

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						0 = Reset 1 = Subtract
NO_DATA_MA	RW	7	1	0x0	RESET_4	No data moving average: 0 = Use 0 1 = Use last known value
HPF_SHIFT_FACTOR	RW	4	3	0x0	RESET_4	Value N of high pass filter: from 000 = 12 to 101 = 17
HPF_BYPASS	RW	3	1	0x0	RESET_4	Sensor offset processing: 0 = High pass filter is used 1 = High pass filter is bypassed
PSEUDO_4K_SENSOR	RW	2	1	0x0	RESET_4	PSI5 sensor sampling pseudo 4 kHz: 0 = Standard PSI5 sensor 1 = Sensor sampling pseudo 4K
AMA_SAMPLES	RW	0	2	0x0	RESET_4	Moving average sample size: 00 = 2 01 = 4 10 = 8 11 = 16

Table 176. SAF_REC2_CTRL_PT1 - 0x0C4

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	15	1	0x0	x	Not used
ARM_METHOD	RW	14	1	0x0	RESET_4	ARMING method based on valid sensor data: 0 = EVC 1 = Moving average
ARM_STRETCHER	RW	11	3	0x0	RESET_4	Safing stretcher dwell extension time select: 000 = 32 ms 001 = 128 ms 010 = 256 ms 011 = 512 ms 100 = 2048 ms 101 = 4096 ms others = 256 ms
ARMx	RW	3	8	0x0	RESET_4	ARMINT_x (x from 0 to 7) select for safing record 2
SAF_CS_SELECTION	RW	0	3	0x0	RESET_4	SPI CS select: 001 = SAF_CS0 010 = SAF_CS1 011 = SAF_CS2 100 = SAF_CS3 101 = SAF_CS4 110 = RS_CS_SPI

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						000 or 111 = None assigned CS

Table 177. **SAF_REC2_CTRL_PT2 - 0x0C5**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	2	0x0	x	Not used
RANGE_CHECK_EN	RW	13	1	0x0	RESET_4	Data range limit enable: 0 = Data range limit disabled 1 = Data range limit enabled
SENSOR_TYPE	RW	12	1	0x0	RESET_4	Sensor data type: 0 = Signed 1 = Unsigned
PED_PRO	RW	11	1	0x0	RESET_4	Pedestrian protection sensor validation range: 0 = Standard 1 = Limited
DOWNSAMPLE	RW	9	2	0x0	RESET_4	Downsampling factor n: 00 = No down 01 = 2 10 = 4 11 = 8
NO_DATA_EVCNT	RW	8	1	0x0	RESET_4	No data event counter: 0 = Reset 1 = Subtract
NO_DATA_MA	RW	7	1	0x0	RESET_4	No data moving average: 0 = Use 0 1 = Use last known value
HPF_SHIFT_FACTOR	RW	4	3	0x0	RESET_4	Value N of high pass filter: from 000 = 12 to 101 = 17
HPF_BYPASS	RW	3	1	0x0	RESET_4	Sensor offset processing: 0 = High pass filter is used 1 = High pass filter is bypassed
PSEUDO_4K_SENSOR	RW	2	1	0x0	RESET_4	PSI5 sensor sampling pseudo 4 kHz: 0 = Standard PSI5 sensor 1 = Sensor sampling pseudo 4K
AMA_SAMPLES	RW	0	2	0x0	RESET_4	Moving average sample size 00 = 2 01 = 4 10 = 8 11 = 16

Table 178. **SAF_REC3_CTRL_PT1 - 0x0C6**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	15	1	0x0	x	Not used
ARM_METHOD	RW	14	1	0x0	RESET_4	ARMING method based on valid sensor data: 0 = EVC 1 = Moving average
ARM_STRETCHER	RW	11	3	0x0	RESET_4	Safing stretcher dwell extension time select: 000 = 32 ms 001 = 128 ms 010 = 256 ms 011 = 512 ms 100 = 2048 ms 101 = 4096 ms others = 256 ms
ARMx	RW	3	8	0x0	RESET_4	ARMINT_x (x from 0 to 7) select for safing record 3
SAF_CS_SELECTION	RW	0	3	0x0	RESET_4	SPI CS select: 001 = SAF_CS0 010 = SAF_CS1 011 = SAF_CS2 100 = SAF_CS3 101 = SAF_CS4 110 = RS_CS_SPI 000 or 111 = None assigned CS

Table 179. **SAF_REC3_CTRL_PT2 - 0x0C7**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	2	0x0	x	Not used
RANGE_CHECK_EN	RW	13	1	0x0	RESET_4	Data range limit enable: 0 = Data range limit disabled 1 = Data range limit enabled
SENSOR_TYPE	RW	12	1	0x0	RESET_4	Sensor data type: 0 = Signed 1 = Unsigned
PED_PRO	RW	11	1	0x0	RESET_4	Pedestrian protection sensor validation range: 0 = Standard 1 = Limited
DOWNSAMPLE	RW	9	2	0x0	RESET_4	Downsampling factor n: 00 = No down 01 = 2 10 = 4 11 = 8
NO_DATA_EVCNT	RW	8	1	0x0	RESET_4	No data event counter:

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						0 = Reset 1 = Subtract
NO_DATA_MA	RW	7	1	0x0	RESET_4	No data moving average: 0 = Use 0 1 = Use last known value
HPF_SHIFT_FACTOR	RW	4	3	0x0	RESET_4	Value N of high pass filter: from 000 = 12 to 101 = 17
HPF_BYPASS	RW	3	1	0x0	RESET_4	Sensor offset processing: 0 = High pass filter is used 1 = High pass filter is bypassed
PSEUDO_4K_SENSOR	RW	2	1	0x0	RESET_4	PSI5 sensor sampling pseudo 4 kHz: 0 = Standard PSI5 sensor 1 = Sensor sampling pseudo 4K
AMA_SAMPLES	RW	0	2	0x0	RESET_4	Moving average sample size: 00 = 2 01 = 4 10 = 8 11 = 16

Table 180. SAF_REC4_CTRL_PT1 - 0x0C8

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	15	1	0x0	x	Not used
ARM_METHOD	RW	14	1	0x0	RESET_4	ARMING method based on valid sensor data: 0 = EVC 1 = Moving average
ARM_STRETCHER	RW	11	3	0x0	RESET_4	Safing stretcher dwell extension time select: 000 = 32 ms 001 = 128 ms 010 = 256 ms 011 = 512 ms 100 = 2048 ms 101 = 4096 ms others = 256 ms
ARMx	RW	3	8	0x0	RESET_4	ARMINT_x (x from 0 to 7) select for safing record 4
SAF_CS_SELECTION	RW	0	3	0x0	RESET_4	SPI CS select: 001 = SAF_CS0 010 = SAF_CS1 011 = SAF_CS2 100 = SAF_CS3 101 = SAF_CS4 110 = RS_CS_SPI

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						000 or 111 = None assigned CS

Table 181. **SAF_REC4_CTRL_PT2 - 0x0C9**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	2	0x0	x	Not used
RANGE_CHECK_EN	RW	13	1	0x0	RESET_4	Data range limit enable: 0 = Data range limit disabled 1 = Data range limit enabled
SENSOR_TYPE	RW	12	1	0x0	RESET_4	Sensor data type: 0 = Signed 1 = Unsigned
PED_PRO	RW	11	1	0x0	RESET_4	Pedestrian protection sensor validation range: 0 = Standard 1 = Limited
DOWNSAMPLE	RW	9	2	0x0	RESET_4	Downsampling factor n: 00 = No down 01 = 2 10 = 4 11 = 8
NO_DATA_EVCNT	RW	8	1	0x0	RESET_4	No data event counter: 0 = Reset 1 = Subtract
NO_DATA_MA	RW	7	1	0x0	RESET_4	No data moving average: 0 = Use 0 1 = Use last known value
HPF_SHIFT_FACTOR	RW	4	3	0x0	RESET_4	Value N of high pass filter: from 000 = 12 to 101 = 17
HPF_BYPASS	RW	3	1	0x0	RESET_4	Sensor offset processing: 0 = High pass filter is used 1 = High pass filter is bypassed
PSEUDO_4K_SENSOR	RW	2	1	0x0	RESET_4	PSI5 sensor sampling pseudo 4 kHz: 0 = Standard PSI5 sensor 1 = Sensor sampling pseudo 4K
AMA_SAMPLES	RW	0	2	0x0	RESET_4	Moving average sample size: 00 = 2 01 = 4 10 = 8 11 = 16

Table 182. **SAF_REC5_CTRL_PT1 - 0x0CA**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	15	1	0x0	x	Not used
ARM_METHOD	RW	14	1	0x0	RESET_4	ARMING method based on valid sensor data: 0 = EVC 1 = Moving average
ARM_STRETCHER	RW	11	3	0x0	RESET_4	Safing stretcher dwell extension time select: 000 = 32 ms 001 = 128 ms 010 = 256 ms 011 = 512 ms 100 = 2048 ms 101 = 4096 ms others = 256 ms
ARMx	RW	3	8	0x0	RESET_4	ARMINT_x (x from 0 to 7) select for safing record 5
SAF_CS_SELECTION	RW	0	3	0x0	RESET_4	SPI CS select: 001 = SAF_CS0 010 = SAF_CS1 011 = SAF_CS2 100 = SAF_CS3 101 = SAF_CS4 110 = RS_CS_SPI 000 or 111 = None assigned CS

Table 183. **SAF_REC5_CTRL_PT2 - 0x0CB**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	2	0x0	x	Not used
RANGE_CHECK_EN	RW	13	1	0x0	RESET_4	Data range limit enable: 0 = Data range limit disabled 1 = Data range limit enabled
SENSOR_TYPE	RW	12	1	0x0	RESET_4	Sensor data type: 0 = Signed 1 = Unsigned
PED_PRO	RW	11	1	0x0	RESET_4	Pedestrian protection sensor validation range: 0 = Standard 1 = Limited
DOWNSAMPLE	RW	9	2	0x0	RESET_4	Downsampling factor n: 00 = No down 01 = 2 10 = 4 11 = 8
NO_DATA_EVCNT	RW	8	1	0x0	RESET_4	No data event counter:

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						0 = Reset 1 = Subtract
NO_DATA_MA	RW	7	1	0x0	RESET_4	No data moving average: 0 = Use 0 1 = Use last known value
HPF_SHIFT_FACTOR	RW	4	3	0x0	RESET_4	Value N of high pass filter: from 000 = 12 to 101 = 17
HPF_BYPASS	RW	3	1	0x0	RESET_4	Sensor offset processing: 0 = High pass filter is used 1 = High pass filter is bypassed
PSEUDO_4K_SENSOR	RW	2	1	0x0	RESET_4	PSI5 sensor sampling pseudo 4 kHz: 0 = Standard PSI5 sensor 1 = Sensor sampling pseudo 4K
AMA_SAMPLES	RW	0	2	0x0	RESET_4	Moving average sample size: 00 = 2 01 = 4 10 = 8 11 = 16

Table 184. SAF_REC6_CTRL_PT1 - 0x0CC

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	15	1	0x0	x	Not used
ARM_METHOD	RW	14	1	0x0	RESET_4	ARMING method based on valid sensor data: 0 = EVC 1 = Moving average
ARM_STRETCHER	RW	11	3	0x0	RESET_4	Safing stretcher dwell extension time select: 000 = 32 ms 001 = 128 ms 010 = 256 ms 011 = 512 ms 100 = 2048 ms 101 = 4096 ms others = 256 ms
ARMx	RW	3	8	0x0	RESET_4	ARMINT_x (x from 0 to 7) select for safing record 6
SAF_CS_SELECTION	RW	0	3	0x0	RESET_4	SPI CS select: 001 = SAF_CS0 010 = SAF_CS1 011 = SAF_CS2 100 = SAF_CS3 101 = SAF_CS4 110 = RS_CS_SPI

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						000 or 111 = None assigned CS

Table 185. **SAF_REC6_CTRL_PT2 - 0x0CD**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	2	0x0	x	Not used
RANGE_CHECK_EN	RW	13	1	0x0	RESET_4	Data range limit enable: 0 = Data range limit disabled 1 = Data range limit enabled
SENSOR_TYPE	RW	12	1	0x0	RESET_4	Sensor data type: 0 = Signed 1 = Unsigned
PED_PRO	RW	11	1	0x0	RESET_4	Pedestrian protection sensor validation range: 0 = Standard 1 = Limited
DOWNSAMPLE	RW	9	2	0x0	RESET_4	Downsampling factor n: 00 = No down 01 = 2 10 = 4 11 = 8
NO_DATA_EVCNT	RW	8	1	0x0	RESET_4	No data event counter: 0 = Reset 1 = Subtract
NO_DATA_MA	RW	7	1	0x0	RESET_4	No data moving average: 0 = Use 0 1 = Use last known value
HPF_SHIFT_FACTOR	RW	4	3	0x0	RESET_4	Value N of high pass filter: from 000 = 12 to 101 = 17
HPF_BYPASS	RW	3	1	0x0	RESET_4	Sensor offset processing: 0 = High pass filter is used 1 = High pass filter is bypassed
PSEUDO_4K_SENSOR	RW	2	1	0x0	RESET_4	PSI5 sensor sampling pseudo 4 kHz: 0 = Standard PSI5 sensor 1 = Sensor sampling pseudo 4K
AMA_SAMPLES	RW	0	2	0x0	RESET_4	Moving average sample size: 00 = 2 01 = 4 10 = 8 11 = 16

Table 186. **SAF_REC7_CTRL_PT1 - 0x0CE**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	15	1	0x0	x	Not used
ARM_METHOD	RW	14	1	0x0	RESET_4	ARMING method based on valid sensor data: 0 = EVC 1 = Moving average
ARM_STRETCHER	RW	11	3	0x0	RESET_4	Safing stretcher dwell extension time select: 000 = 32 ms 001 = 128 ms 010 = 256 ms 011 = 512 ms 100 = 2048 ms 101 = 4096 ms others = 256 ms
ARMx	RW	3	8	0x0	RESET_4	ARMINT_x (x from 0 to 7) select for safing record 7
SAF_CS_SELECTION	RW	0	3	0x0	RESET_4	SPI CS select: 001 = SAF_CS0 010 = SAF_CS1 011 = SAF_CS2 100 = SAF_CS3 101 = SAF_CS4 110 = RS_CS_SPI 000 or 111 = None assigned CS

Table 187. **SAF_REC7_CTRL_PT2 - 0x0CF**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	2	0x0	x	Not used
RANGE_CHECK_EN	RW	13	1	0x0	RESET_4	Data range limit enable: 0 = Data range limit disabled 1 = Data range limit enabled
SENSOR_TYPE	RW	12	1	0x0	RESET_4	Sensor data type: 0 = Signed 1 = Unsigned
PED_PRO	RW	11	1	0x0	RESET_4	Pedestrian protection sensor validation range: 0 = Standard 1 = Limited
DOWNSAMPLE	RW	9	2	0x0	RESET_4	Downsampling factor n: 00 = No down 01 = 2 10 = 4 11 = 8
NO_DATA_EVCNT	RW	8	1	0x0	RESET_4	No data event counter:

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						0 = Reset 1 = Subtract
NO_DATA_MA	RW	7	1	0x0	RESET_4	No data moving average: 0 = Use 0 1 = Use last known value
HPF_SHIFT_FACTOR	RW	4	3	0x0	RESET_4	Value N of high pass filter: from 000 = 12 to 101 = 17
HPF_BYPASS	RW	3	1	0x0	RESET_4	Sensor offset processing: 0 = High pass filter is used 1 = High pass filter is bypassed
PSEUDO_4K_SENSOR	RW	2	1	0x0	RESET_4	PSI5 sensor sampling pseudo 4 kHz: 0 = Standard PSI5 sensor 1 = Sensor sampling pseudo 4K
AMA_SAMPLES	RW	0	2	0x0	RESET_4	Moving average sample size: 00 = 2 01 = 4 10 = 8 11 = 16

Table 188. SAF_REC8_CTRL_PT1 - 0x0D0

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	15	1	0x0	x	Not used
ARM_METHOD	RW	14	1	0x0	RESET_4	ARMING method based on valid sensor data: 0 = EVC 1 = Moving average
ARM_STRETCHER	RW	11	3	0x0	RESET_4	Safing stretcher dwell extension time select: 000 = 32 ms 001 = 128 ms 010 = 256 ms 011 = 512 ms 100 = 2048 ms 101 = 4096 ms others = 256 ms
ARMx	RW	3	8	0x0	RESET_4	ARMINT_x (x from 0 to 7) select for safing record 8
SAF_CS_SELECTION	RW	0	3	0x0	RESET_4	SPI CS select: 001 = SAF_CS0 010 = SAF_CS1 011 = SAF_CS2 100 = SAF_CS3 101 = SAF_CS4 110 = RS_CS_SPI

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						000 or 111 = None assigned CS

Table 189. **SAF_REC8_CTRL_PT2 - 0x0D1**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	2	0x0	x	Not used
RANGE_CHECK_EN	RW	13	1	0x0	RESET_4	Data range limit enable: 0 = Data range limit disabled 1 = Data range limit enabled
SENSOR_TYPE	RW	12	1	0x0	RESET_4	Sensor data type: 0 = Signed 1 = Unsigned
PED_PRO	RW	11	1	0x0	RESET_4	Pedestrian protection sensor validation range: 0 = Standard 1 = Limited
DOWNSAMPLE	RW	9	2	0x0	RESET_4	Downsampling factor n: 00 = No down 01 = 2 10 = 4 11 = 8
NO_DATA_EVCNT	RW	8	1	0x0	RESET_4	No data event counter: 0 = Reset 1 = Subtract
NO_DATA_MA	RW	7	1	0x0	RESET_4	No data moving average: 0 = Use 0 1 = Use last known value
HPF_SHIFT_FACTOR	RW	4	3	0x0	RESET_4	Value N of high pass filter: from 000 = 12 to 101 = 17
HPF_BYPASS	RW	3	1	0x0	RESET_4	Sensor offset processing: 0 = High pass filter is used 1 = High pass filter is bypassed
PSEUDO_4K_SENSOR	RW	2	1	0x0	RESET_4	PSI5 sensor sampling pseudo 4 kHz: 0 = Standard PSI5 sensor 1 = Sensor sampling pseudo 4K
AMA_SAMPLES	RW	0	2	0x0	RESET_4	Moving average sample size: 00 = 2 01 = 4 10 = 8 11 = 16

Table 190. **SAF_REC9_CTRL_PT1 - 0x0D2**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	15	1	0x0	x	Not used
ARM_METHOD	RW	14	1	0x0	RESET_4	ARMING method based on valid sensor data: 0 = EVC 1 = Moving average
ARM_STRETCHER	RW	11	3	0x0	RESET_4	Safing stretcher dwell extension time select: 000 = 32 ms 001 = 128 ms 010 = 256 ms 011 = 512 ms 100 = 2048 ms 101 = 4096 ms others = 256 ms
ARMx	RW	3	8	0x0	RESET_4	ARMINT_x (x from 0 to 7) select for safing record 9
SAF_CS_SELECTION	RW	0	3	0x0	RESET_4	SPI CS select: 001 = SAF_CS0 010 = SAF_CS1 011 = SAF_CS2 100 = SAF_CS3 101 = SAF_CS4 110 = RS_CS_SPI 000 or 111 = None assigned CS

Table 191. **SAF_REC9_CTRL_PT2 - 0x0D3**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	2	0x0	x	Not used
RANGE_CHECK_EN	RW	13	1	0x0	RESET_4	Data range limit enable: 0 = Data range limit disabled 1 = Data range limit enabled
SENSOR_TYPE	RW	12	1	0x0	RESET_4	Sensor data type: 0 = Signed 1 = Unsigned
PED_PRO	RW	11	1	0x0	RESET_4	Pedestrian protection sensor validation range: 0 = Standard 1 = Limited
DOWNSAMPLE	RW	9	2	0x0	RESET_4	Downsampling factor n: 00 = No down 01 = 2 10 = 4 11 = 8
NO_DATA_EVCNT	RW	8	1	0x0	RESET_4	No data event counter:

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						0 = Reset 1 = Subtract
NO_DATA_MA	RW	7	1	0x0	RESET_4	No data moving average: 0 = Use 0 1 = Use last known value
HPF_SHIFT_FACTOR	RW	4	3	0x0	RESET_4	Value N of high pass filter: from 000 = 12 to 101 = 17
HPF_BYPASS	RW	3	1	0x0	RESET_4	Sensor offset processing: 0 = High pass filter is used 1 = High pass filter is bypassed
PSEUDO_4K_SENSOR	RW	2	1	0x0	RESET_4	PSI5 sensor sampling pseudo 4 kHz: 0 = Standard PSI5 sensor 1 = Sensor sampling pseudo 4K
AMA_SAMPLES	RW	0	2	0x0	RESET_4	Moving average sample size: 00 = 2 01 = 4 10 = 8 11 = 16

Table 192. SAF_REC10_CTRL_PT1 - 0x0D4

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	15	2	0x0	x	Not used
ARM_METHOD	RW	14	1	0x0	RESET_4	ARMING method based on valid sensor data: 0 = EVC 1 = Moving average
ARM_STRETCHER	RW	11	3	0x0	RESET_4	Safing stretcher dwell extension time select: 000 = 32 ms 001 = 128 ms 010 = 256 ms 011 = 512 ms 100 = 2048 ms 101 = 4096 ms others = 256 ms
ARMx	RW	3	8	0x0	RESET_4	ARMINT_x (x from 0 to 7) select for safing record 10
SAF_CS_SELECTION	RW	0	3	0x0	RESET_4	SPI CS select: 001 = SAF_CS0 010 = SAF_CS1 011 = SAF_CS2 100 = SAF_CS3 101 = SAF_CS4 110 = RS_CS_SPI

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						000 or 111 = None assigned CS

Table 193. **SAF_REC10_CTRL_PT2 - 0x0D5**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	2	0x0	x	Not used
RANGE_CHECK_EN	RW	13	1	0x0	RESET_4	Data range limit enable: 0 = Data range limit disabled 1 = Data range limit enabled
SENSOR_TYPE	RW	12	1	0x0	RESET_4	Sensor data type: 0 = Signed 1 = Unsigned
PED_PRO	RW	11	1	0x0	RESET_4	Pedestrian protection sensor validation range: 0 = Standard 1 = Limited
DOWNSAMPLE	RW	9	2	0x0	RESET_4	Downsampling factor n: 00 = No down 01 = 2 10 = 4 11 = 8
NO_DATA_EVCNT	RW	8	1	0x0	RESET_4	No data event counter: 0 = Reset 1 = Subtract
NO_DATA_MA	RW	7	1	0x0	RESET_4	No data moving average: 0 = Use 0 1 = Use last known value
HPF_SHIFT_FACTOR	RW	4	3	0x0	RESET_4	Value N of high pass filter: from 000 = 12 to 101 = 17
HPF_BYPASS	RW	3	1	0x0	RESET_4	Sensor offset processing: 0 = High pass filter is used 1 = High pass filter is bypassed
PSEUDO_4K_SENSOR	RW	2	1	0x0	RESET_4	PSI5 sensor sampling pseudo 4 kHz: 0 = Standard PSI5 sensor 1 = Sensor sampling pseudo 4K
AMA_SAMPLES	RW	0	2	0x0	RESET_4	Moving average sample size: 00 = 2 01 = 4 10 = 8 11 = 16

Table 194. **SAF_REC11_CTRL_PT1 - 0x0D6**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	15	1	0x0	x	Not used
ARM_METHOD	RW	14	1	0x0	RESET_4	ARMING method based on valid sensor data: 0 = EVC 1 = Moving average
ARM_STRETCHER	RW	11	3	0x0	RESET_4	Safing stretcher dwell extension time select: 000 = 32 ms 001 = 128 ms 010 = 256 ms 011 = 512 ms 100 = 2048 ms 101 = 4096 ms others = 256 ms
ARMx	RW	3	8	0x0	RESET_4	ARMINT_x (x from 0 to 7) select for safing record 11
SAF_CS_SELECTION	RW	0	3	0x0	RESET_4	SPI CS select: 001 = SAF_CS0 010 = SAF_CS1 011 = SAF_CS2 100 = SAF_CS3 101 = SAF_CS4 110 = RS_CS_SPI 000 or 111 = None assigned CS

Table 195. **SAF_REC11_CTRL_PT2 - 0x0D7**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	1	0x0	x	Not used
RANGE_CHECK_EN	RW	13	1	0x0	RESET_4	Data range limit enable: 0 = Data range limit disabled 1 = Data range limit enabled
SENSOR_TYPE	RW	12	1	0x0	RESET_4	Sensor data type: 0 = Signed 1 = Unsigned
PED_PRO	RW	11	1	0x0	RESET_4	Pedestrian protection sensor validation range: 0 = Standard 1 = Limited
DOWNSAMPLE	RW	9	2	0x0	RESET_4	Downsampling factor n: 00 = No down 01 = 2 10 = 4 11 = 8
NO_DATA_EVCNT	RW	8	1	0x0	RESET_4	No data event counter:

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						0 = Reset 1 = Subtract
NO_DATA_MA	RW	7	1	0x0	RESET_4	No data moving average: 0 = Use 0 1 = Use last known value
HPF_SHIFT_FACTOR	RW	4	3	0x0	RESET_4	Value N of high pass filter: from 000 = 12 to 101 = 17
HPF_BYPASS	RW	3	1	0x0	RESET_4	Sensor offset processing: 0 = High pass filter is used 1 = High pass filter is bypassed
PSEUDO_4K_SENSOR	RW	2	1	0x0	RESET_4	PSI5 sensor sampling pseudo 4 kHz: 0 = Standard PSI5 sensor 1 = Sensor sampling pseudo 4K
AMA_SAMPLES	RW	0	2	0x0	RESET_4	Moving average sample size: 00 = 2 01 = 4 10 = 8 11 = 16

Table 196. SAF_REC12_CTRL_PT1 - 0x0D8

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	15	1	0x0	x	Not used
ARM_METHOD	RW	14	1	0x0	RESET_4	ARMING method based on valid sensor data: 0 = EVC 1 = Moving average
ARM_STRETCHER	RW	11	3	0x0	RESET_4	Safing stretcher dwell extension time select: 000 = 32 ms 001 = 128 ms 010 = 256 ms 011 = 512 ms 100 = 2048 ms 101 = 4096 ms others = 256 ms
ARMx	RW	3	8	0x0	RESET_4	ARMINT_x (x from 0 to 7) select for safing record 12
SAF_CS_SELECTION	RW	0	3	0x0	RESET_4	SPI CS select: 001 = SAF_CS0 010 = SAF_CS1 011 = SAF_CS2 100 = SAF_CS3 101 = SAF_CS4 110 = RS_CS_SPI

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						000 or 111 = None assigned CS

Table 197. **SAF_REC12_CTRL_PT2 - 0x0D9**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	1	0x0	x	Not used
RANGE_CHECK_EN	RW	13	1	0x0	RESET_4	Data range limit enable: 0 = Data range limit disabled 1 = Data range limit enabled
SENSOR_TYPE	RW	12	1	0x0	RESET_4	Sensor data type: 0 = Signed 1 = Unsigned
PED_PRO	RW	11	1	0x0	RESET_4	Pedestrian protection sensor validation range: 0 = Standard 1 = Limited
DOWNSAMPLE	RW	9	2	0x0	RESET_4	Downsampling factor n: 00 = No down 01 = 2 10 = 4 11 = 8
NO_DATA_EVCNT	RW	8	1	0x0	RESET_4	No data event counter: 0 = Reset 1 = Subtract
NO_DATA_MA	RW	7	1	0x0	RESET_4	No data moving average: 0 = Use 0 1 = Use last known value
HPF_SHIFT_FACTOR	RW	4	3	0x0	RESET_4	Value N of high pass filter: from 000 = 12 to 101 = 17
HPF_BYPASS	RW	3	1	0x0	RESET_4	Sensor offset processing: 0 = High pass filter is used 1 = High pass filter is bypassed
PSEUDO_4K_SENSOR	RW	2	1	0x0	RESET_4	PSI5 sensor sampling pseudo 4 kHz: 0 = Standard PSI5 sensor 1 = Sensor sampling pseudo 4K
AMA_SAMPLES	RW	0	2	0x0	RESET_4	Moving average sample size: 00 = 2 01 = 4 10 = 8 11 = 16

Table 198. **SAF_REC13_CTRL_PT1 - 0x0DA**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	15	1	0x0	x	Not used
ARM_METHOD	RW	14	1	0x0	RESET_4	ARMING method based on valid sensor data: 0 = EVC 1 = Moving average
ARM_STRETCHER	RW	11	3	0x0	RESET_4	Safing stretcher dwell extension time select: 000 = 32 ms 001 = 128 ms 010 = 256 ms 011 = 512 ms 100 = 2048 ms 101 = 4096 ms others = 256 ms
ARMx	RW	3	8	0x0	RESET_4	ARMINT_x (x from 0 to 7) select for safing record 13
SAF_CS_SELECTION	RW	0	3	0x0	RESET_4	SPI CS select: 001 = SAF_CS0 010 = SAF_CS1 011 = SAF_CS2 100 = SAF_CS3 101 = SAF_CS4 110 = RS_CS_SPI 000 or 111 = None assigned CS

Table 199. **SAF_REC13_CTRL_PT2 - 0x0DB**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	2	0x0	x	Not used
RANGE_CHECK_EN	RW	13	1	0x0	RESET_4	Data range limit enable: 0 = Data range limit disabled 1 = Data range limit enabled
SENSOR_TYPE	RW	12	1	0x0	RESET_4	Sensor data type: 0 = Signed 1 = Unsigned
PED_PRO	RW	11	1	0x0	RESET_4	Pedestrian protection sensor validation range: 0 = Standard 1 = Limited
DOWNSAMPLE	RW	9	2	0x0	RESET_4	Downsampling factor n: 00 = No down 01 = 2 10 = 4 11 = 8
NO_DATA_EVCNT	RW	8	1	0x0	RESET_4	No data event counter:

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						0 = Reset 1 = Subtract
NO_DATA_MA	RW	7	1	0x0	RESET_4	No data moving average: 0 = Use 0 1 = Use last known value
HPF_SHIFT_FACTOR	RW	4	3	0x0	RESET_4	Value N of high pass filter: from 000 = 12 to 101 = 17
HPF_BYPASS	RW	3	1	0x0	RESET_4	Sensor offset processing: 0 = High pass filter is used 1 = High pass filter is bypassed
PSEUDO_4K_SENSOR	RW	2	1	0x0	RESET_4	PSI5 sensor sampling pseudo 4 kHz: 0 = Standard PSI5 sensor 1 = Sensor sampling pseudo 4K
AMA_SAMPLES	RW	0	2	0x0	RESET_4	Moving average sample size: 00 = 2 01 = 4 10 = 8 11 = 16

Table 200. SAF_REC14_CTRL_PT1 - 0x0DC

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	15	1	0x0	x	Not used
ARM_METHOD	RW	14	1	0x0	RESET_4	ARMING method based on valid sensor data: 0 = EVC 1 = Moving average
ARM_STRETCHER	RW	11	3	0x0	RESET_4	Safing stretcher dwell extension time select: 000 = 32 ms 001 = 128 ms 010 = 256 ms 011 = 512 ms 100 = 2048 ms 101 = 4096 ms others = 256 ms
ARMx	RW	3	8	0x0	RESET_4	ARMINT_x (x from 0 to 7) select for safing record 14
SAF_CS_SELECTION	RW	0	3	0x0	RESET_4	SPI CS select: 001 = SAF_CS0 010 = SAF_CS1 011 = SAF_CS2 100 = SAF_CS3 101 = SAF_CS4 110 = RS_CS_SPI

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						000 or 111 = None assigned CS

Table 201. SAF_REC14_CTRL_PT2 - 0x0DD

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	1	0x0	x	Not used
RANGE_CHECK_EN	RW	13	1	0x0	RESET_4	Data range limit enable: 0 = Data range limit disabled 1 = Data range limit enabled
SENSOR_TYPE	RW	12	1	0x0	RESET_4	Sensor data type: 0 = Signed 1 = Unsigned
PED_PRO	RW	11	1	0x0	RESET_4	Pedestrian protection sensor validation range: 0 = Standard 1 = Limited
DOWNSAMPLE	RW	9	2	0x0	RESET_4	Downsampling factor n: 00 = No down 01 = 2 10 = 4 11 = 8
NO_DATA_EVCNT	RW	8	1	0x0	RESET_4	No data event counter: 0 = Reset 1 = Subtract
NO_DATA_MA	RW	7	1	0x0	RESET_4	No data moving average: 0 = Use 0 1 = Use last known value
HPF_SHIFT_FACTOR	RW	4	3	0x0	RESET_4	Value N of high pass filter: from 000 = 12 to 101 = 17
HPF_BYPASS	RW	3	1	0x0	RESET_4	Sensor offset processing: 0 = High pass filter is used 1 = High pass filter is bypassed
PSEUDO_4K_SENSOR	RW	2	1	0x0	RESET_4	PSI5 sensor sampling pseudo 4 kHz: 0 = Standard PSI5 sensor 1 = Sensor sampling pseudo 4K
AMA_SAMPLES	RW	0	2	0x0	RESET_4	Moving average sample size: 00 = 2 01 = 4 10 = 8 11 = 16

Table 202. **SAF_REC15_CTRL_PT1 - 0x0DE**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	15	1	0x0	x	Not used
ARM_METHOD	RW	14	1	0x0	RESET_4	ARMING method based on valid sensor data: 0 = EVC 1 = Moving average
ARM_STRETCHER	RW	11	3	0x0	RESET_4	Safing stretcher dwell extension time select: 000 = 32 ms 001 = 128 ms 010 = 256 ms 011 = 512 ms 100 = 2048 ms 101 = 4096 ms others = 256 ms
ARMx	RW	3	8	0x0	RESET_4	ARMINT_x (x from 0 to 7) select for safing record 15
SAF_CS_SELECTION	RW	0	3	0x0	RESET_4	SPI CS select: 001 = SAF_CS0 010 = SAF_CS1 011 = SAF_CS2 100 = SAF_CS3 101 = SAF_CS4 110 = RS_CS_SPI 000 or 111 = None assigned CS

Table 203. **SAF_REC15_CTRL_PT2 - 0x0DF**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	2	0x0	x	Not used
RANGE_CHECK_EN	RW	13	1	0x0	RESET_4	Data range limit enable: 0 = Data range limit disabled 1 = Data range limit enabled
SENSOR_TYPE	RW	12	1	0x0	RESET_4	Sensor data type: 0 = Signed 1 = Unsigned
PED_PRO	RW	11	1	0x0	RESET_4	Pedestrian protection sensor validation range: 0 = Standard 1 = Limited
DOWNSAMPLE	RW	9	2	0x0	RESET_4	Downsampling factor n: 00 = No down 01 = 2 10 = 4 11 = 8
NO_DATA_EVCNT	RW	8	1	0x0	RESET_4	No data event counter:

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						0 = Reset 1 = Subtract
NO_DATA_MA	RW	7	1	0x0	RESET_4	No data moving average: 0 = Use 0 1 = Use last known value
HPF_SHIFT_FACTOR	RW	4	3	0x0	RESET_4	Value N of high pass filter: from 000 = 12 to 101 = 17
HPF_BYPASS	RW	3	1	0x0	RESET_4	Sensor offset processing: 0 = High pass filter is used 1 = High pass filter is bypassed
PSEUDO_4K_SENSOR	RW	2	1	0x0	RESET_4	PSI5 sensor sampling pseudo 4 kHz: 0 = Standard PSI5 sensor 1 = Sensor sampling pseudo 4K
AMA_SAMPLES	RW	0	2	0x0	RESET_4	Moving average sample size: 00 = 2 01 = 4 10 = 8 11 = 16

Table 204. SAF_REC16_CTRL_PT1 - 0x0E0

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	15	1	0x0	x	Not used
ARM_METHOD	RW	14	1	0x0	RESET_4	ARMING method based on valid sensor data: 0 = EVC 1 = Moving average
ARM_STRETCHER	RW	11	3	0x0	RESET_4	Safing stretcher dwell extension time select: 000 = 32 ms 001 = 128 ms 010 = 256 ms 011 = 512 ms 100 = 2048 ms 101 = 4096 ms others = 256 ms
ARMx	RW	3	8	0x0	RESET_4	ARMINT_x (x from 0 to 7) select for safing record 16
SAF_CS_SELECTION	RW	0	3	0x0	RESET_4	SPI CS select: 001 = SAF_CS0 010 = SAF_CS1 011 = SAF_CS2 100 = SAF_CS3 101 = SAF_CS4 110 = RS_CS_SPI

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						000 or 111 = None assigned CS

Table 205. **SAF_REC16_CTRL_PT2 - 0x0E1**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	1	0x0	x	Not used
RANGE_CHECK_EN	RW	13	1	0x0	RESET_4	Data range limit enable: 0 = Data range limit disabled 1 = Data range limit enabled
SENSOR_TYPE	RW	12	1	0x0	RESET_4	Sensor data type: 0 = Signed 1 = Unsigned
PED_PRO	RW	11	1	0x0	RESET_4	Pedestrian protection sensor validation range: 0 = Standard 1 = Limited
DOWNSAMPLE	RW	9	2	0x0	RESET_4	Downsampling factor n: 00 = No down 01 = 2 10 = 4 11 = 8
NO_DATA_EVCNT	RW	8	1	0x0	RESET_4	No data event counter: 0 = Reset 1 = Subtract
NO_DATA_MA	RW	7	1	0x0	RESET_4	No data moving average: 0 = Use 0 1 = Use last known value
HPF_SHIFT_FACTOR	RW	4	3	0x0	RESET_4	Value N of high pass filter: from 000 = 12 to 101 = 17
HPF_BYPASS	RW	3	1	0x0	RESET_4	Sensor offset processing: 0 = High pass filter is used 1 = High pass filter is bypassed
PSEUDO_4K_SENSOR	RW	2	1	0x0	RESET_4	PSI5 sensor sampling pseudo 4 kHz: 0 = Standard PSI5 sensor 1 = Sensor sampling pseudo 4K
AMA_SAMPLES	RW	0	2	0x0	RESET_4	Moving average sample size: 00 = 2 01 = 4 10 = 8 11 = 16

Table 206. **SAF_REC17_CTRL_PT1 - 0x0E2**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	15	1	0x0	x	Not used
ARM_METHOD	RW	14	1	0x0	RESET_4	ARMING method based on valid sensor data: 0 = EVC 1 = Moving average
ARM_STRETCHER	RW	11	3	0x0	RESET_4	Safing stretcher dwell extension time select: 000 = 32 ms 001 = 128 ms 010 = 256 ms 011 = 512 ms 100 = 2048 ms 101 = 4096 ms others = 256 ms
ARMx	RW	3	8	0x0	RESET_4	ARMINT_x (x from 0 to 7) select for safing record 17
SAF_CS_SELECTION	RW	0	3	0x0	RESET_4	SPI CS select: 001 = SAF_CS0 010 = SAF_CS1 011 = SAF_CS2 100 = SAF_CS3 101 = SAF_CS4 110 = RS_CS_SPI 000 or 111 = None assigned CS

Table 207. **SAF_REC17_CTRL_PT2 - 0x0E3**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	1	0x0	x	Not used
RANGE_CHECK_EN	RW	13	1	0x0	RESET_4	Data range limit enable: 0 = Data range limit disabled 1 = Data range limit enabled
SENSOR_TYPE	RW	12	1	0x0	RESET_4	Sensor data type: 0 = Signed 1 = Unsigned
PED_PRO	RW	11	1	0x0	RESET_4	Pedestrian protection sensor validation range: 0 = Standard 1 = Limited
DOWNSAMPLE	RW	9	2	0x0	RESET_4	Downsampling factor n: 00 = No down 01 = 2 10 = 4 11 = 8
NO_DATA_EVCNT	RW	8	1	0x0	RESET_4	No data event counter:

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						0 = Reset 1 = Subtract
NO_DATA_MA	RW	7	1	0x0	RESET_4	No data moving average: 0 = Use 0 1 = Use last known value
HPF_SHIFT_FACTOR	RW	4	3	0x0	RESET_4	Value N of high pass filter: from 000 = 12 to 101 = 17
HPF_BYPASS	RW	3	1	0x0	RESET_4	Sensor offset processing: 0 = High pass filter is used 1 = High pass filter is bypassed
PSEUDO_4K_SENSOR	RW	2	1	0x0	RESET_4	PSI5 sensor sampling pseudo 4 kHz: 0 = Standard PSI5 sensor 1 = Sensor sampling pseudo 4K
AMA_SAMPLES	RW	0	2	0x0	RESET_4	Moving average sample size: 00 = 2 01 = 4 10 = 8 11 = 16

Table 208. SAF_REC18_CTRL_PT1 - 0x0E4

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	15	1	0x0	x	Not used
ARM_METHOD	RW	14	1	0x0	RESET_4	ARMING method based on valid sensor data: 0 = EVC 1 = Moving average
ARM_STRETCHER	RW	11	3	0x0	RESET_4	Safing stretcher dwell extension time select: 000 = 32 ms 001 = 128 ms 010 = 256 ms 011 = 512 ms 100 = 2048 ms 101 = 4096 ms others = 256 ms
ARMx	RW	3	8	0x0	RESET_4	ARMINT_x (x from 0 to 7) select for safing record 18
SAF_CS_SELECTION	RW	0	3	0x0	RESET_4	SPI CS select: 001 = SAF_CS0 010 = SAF_CS1 011 = SAF_CS2 100 = SAF_CS3 101 = SAF_CS4 110 = RS_CS_SPI

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						000 or 111 = None assigned CS

Table 209. **SAF_REC18_CTRL_PT2 - 0x0E5**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	2	0x0	x	Not used
RANGE_CHECK_EN	RW	13	1	0x0	RESET_4	Data range limit enable: 0 = Data range limit disabled 1 = Data range limit enabled
SENSOR_TYPE	RW	12	1	0x0	RESET_4	Sensor data type: 0 = Signed 1 = Unsigned
PED_PRO	RW	11	1	0x0	RESET_4	Pedestrian protection sensor validation range: 0 = Standard 1 = Limited
DOWNSAMPLE	RW	9	2	0x0	RESET_4	Downsampling factor n: 00 = No down 01 = 2 10 = 4 11 = 8
NO_DATA_EVCNT	RW	8	1	0x0	RESET_4	No data event counter: 0 = Reset 1 = Subtract
NO_DATA_MA	RW	7	1	0x0	RESET_4	No data moving average: 0 = Use 0 1 = Use last known value
HPF_SHIFT_FACTOR	RW	4	3	0x0	RESET_4	Value N of high pass filter: from 000 = 12 to 101 = 17
HPF_BYPASS	RW	3	1	0x0	RESET_4	Sensor offset processing: 0 = High pass filter is used 1 = High pass filter is bypassed
PSEUDO_4K_SENSOR	RW	2	1	0x0	RESET_4	PSI5 sensor sampling pseudo 4 kHz: 0 = Standard PSI5 sensor 1 = Sensor sampling pseudo 4K
AMA_SAMPLES	RW	0	2	0x0	RESET_4	Moving average sample size: 00 = 2 01 = 4 10 = 8 11 = 16

Table 210. **SAF_REC19_CTRL_PT1 - 0x0E6**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	15	1	0x0	x	Not used
ARM_METHOD	RW	14	1	0x0	RESET_4	ARMING method based on valid sensor data: 0 = EVC 1 = Moving average
ARM_STRETCHER	RW	11	3	0x0	RESET_4	Safing stretcher dwell extension time select: 000 = 32 ms 001 = 128 ms 010 = 256 ms 011 = 512 ms 100 = 2048 ms 101 = 4096 ms others = 256 ms
ARMx	RW	3	8	0x0	RESET_4	ARMINT_x (x from 0 to 7) select for safing record 19
SAF_CS_SELECTION	RW	0	3	0x0	RESET_4	SPI CS select: 001 = SAF_CS0 010 = SAF_CS1 011 = SAF_CS2 100 = SAF_CS3 101 = SAF_CS4 110 = RS_CS_SPI 000 or 111 = None assigned CS

Table 211. **SAF_REC19_CTRL_PT2 - 0x0E7**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	2	0x0	x	Not used
RANGE_CHECK_EN	RW	13	1	0x0	RESET_4	Data range limit enable: 0 = Data range limit disabled 1 = Data range limit enabled
SENSOR_TYPE	RW	12	1	0x0	RESET_4	Sensor data type: 0 = Signed 1 = Unsigned
PED_PRO	RW	11	1	0x0	RESET_4	Pedestrian protection sensor validation range: 0 = Standard 1 = Limited
DOWNSAMPLE	RW	9	2	0x0	RESET_4	Downsampling factor n: 00 = No down 01 = 2 10 = 4 11 = 8
NO_DATA_EVCNT	RW	8	1	0x0	RESET_4	No data event counter:

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						0 = Reset 1 = Subtract
NO_DATA_MA	RW	7	1	0x0	RESET_4	No data moving average: 0 = Use 0 1 = Use last known value
HPF_SHIFT_FACTOR	RW	4	3	0x0	RESET_4	Value N of high pass filter: from 000 = 12 to 101 = 17
HPF_BYPASS	RW	3	1	0x0	RESET_4	Sensor offset processing: 0 = High pass filter is used 1 = High pass filter is bypassed
PSEUDO_4K_SENSOR	RW	2	1	0x0	RESET_4	PSI5 sensor sampling pseudo 4 kHz: 0 = Standard PSI5 sensor 1 = Sensor sampling pseudo 4K
AMA_SAMPLES	RW	0	2	0x0	RESET_4	Moving average sample size: 00 = 2 01 = 4 10 = 8 11 = 16

Table 212. SAF_REC20_CTRL_PT1 - 0x0E8

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	15	1	0x0	x	Not used
ARM_METHOD	RW	14	1	0x0	RESET_4	ARMING method based on valid sensor data: 0 = EVC 1 = Moving average
ARM_STRETCHER	RW	11	3	0x0	RESET_4	Safing stretcher dwell extension time select: 000 = 32 ms 001 = 128 ms 010 = 256 ms 011 = 512 ms 100 = 2048 ms 101 = 4096 ms others = 256 ms
ARMx	RW	3	8	0x0	RESET_4	ARMINT_x (x from 0 to 7) select for safing record 20
SAF_CS_SELECTION	RW	0	3	0x0	RESET_4	SPI CS select: 001 = SAF_CS0 010 = SAF_CS1 011 = SAF_CS2 100 = SAF_CS3 101 = SAF_CS4 110 = RS_CS_SPI

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						000 or 111 = None assigned CS

Table 213. **SAF_REC20_CTRL_PT2 - 0x0E9**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	2	0x0	x	Not used
RANGE_CHECK_EN	RW	13	1	0x0	RESET_4	Data range limit enable: 0 = Data range limit disabled 1 = Data range limit enabled
SENSOR_TYPE	RW	12	1	0x0	RESET_4	Sensor data type: 0 = Signed 1 = Unsigned
PED_PRO	RW	11	1	0x0	RESET_4	Pedestrian protection sensor validation range: 0 = Standard 1 = Limited
DOWNSAMPLE	RW	9	2	0x0	RESET_4	Downsampling factor n: 00 = No down 01 = 2 10 = 4 11 = 8
NO_DATA_EVCNT	RW	8	1	0x0	RESET_4	No data event counter: 0 = Reset 1 = Subtract
NO_DATA_MA	RW	7	1	0x0	RESET_4	No data moving average: 0 = Use 0 1 = Use last known value
HPF_SHIFT_FACTOR	RW	4	3	0x0	RESET_4	Value N of high pass filter: from 000 = 12 to 101 = 17
HPF_BYPASS	RW	3	1	0x0	RESET_4	Sensor offset processing: 0 = High pass filter is used 1 = High pass filter is bypassed
PSEUDO_4K_SENSOR	RW	2	1	0x0	RESET_4	PSI5 sensor sampling pseudo 4 kHz: 0 = Standard PSI5 sensor 1 = Sensor sampling pseudo 4K
AMA_SAMPLES	RW	0	2	0x0	RESET_4	Moving average sample size: 00 = 2 01 = 4 10 = 8 11 = 16

Table 214. **SAF_REC21_CTRL_PT1 - 0x0EA**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	15	1	0x0	x	Not used
ARM_METHOD	RW	14	1	0x0	RESET_4	ARMING method based on valid sensor data: 0 = EVC 1 = Moving average
ARM_STRETCHER	RW	11	3	0x0	RESET_4	Safing stretcher dwell extension time select: 000 = 32 ms 001 = 128 ms 010 = 256 ms 011 = 512 ms 100 = 2048 ms 101 = 4096 ms others = 256 ms
ARMx	RW	3	8	0x0	RESET_4	ARMINT_x (x from 0 to 7) select for safing record 21
SAF_CS_SELECTION	RW	0	3	0x0	RESET_4	SPI CS select: 001 = SAF_CS0 010 = SAF_CS1 011 = SAF_CS2 100 = SAF_CS3 101 = SAF_CS4 110 = RS_CS_SPI 000 or 111 = None assigned CS

Table 215. **SAF_REC21_CTRL_PT2 - 0x0EB**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	2	0x0	x	Not used
RANGE_CHECK_EN	RW	13	1	0x0	RESET_4	Data range limit enable: 0 = Data range limit disabled 1 = Data range limit enabled
SENSOR_TYPE	RW	12	1	0x0	RESET_4	Sensor data type: 0 = Signed 1 = Unsigned
PED_PRO	RW	11	1	0x0	RESET_4	Pedestrian protection sensor validation range: 0 = Standard 1 = Limited
DOWNSAMPLE	RW	9	2	0x0	RESET_4	Downsampling factor n: 00 = No down 01 = 2 10 = 4 11 = 8
NO_DATA_EVCNT	RW	8	1	0x0	RESET_4	No data event counter:

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						0 = Reset 1 = Subtract
NO_DATA_MA	RW	7	1	0x0	RESET_4	No data moving average: 0 = Use 0 1 = Use last known value
HPF_SHIFT_FACTOR	RW	4	3	0x0	RESET_4	Value N of high pass filter: from 000 = 12 to 101 = 17
HPF_BYPASS	RW	3	1	0x0	RESET_4	Sensor offset processing: 0 = High pass filter is used 1 = High pass filter is bypassed
PSEUDO_4K_SENSOR	RW	2	1	0x0	RESET_4	PSI5 sensor sampling pseudo 4 kHz: 0 = Standard PSI5 sensor 1 = Sensor sampling pseudo 4K
AMA_SAMPLES	RW	0	2	0x0	RESET_4	Moving average sample size: 00 = 2 01 = 4 10 = 8 11 = 16

Table 216. SAF_THRESHOLD_P_0 - 0x0EC

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_P	RW	0	16	0x0	RESET_4	Positive safing threshold for safing record 0

Table 217. SAF_THRESHOLD_P_1 - 0x0ED

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_P	RW	0	16	0x0	RESET_4	Positive safing threshold for safing record 1

Table 218. SAF_THRESHOLD_P_2 - 0x0EE

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_P	RW	0	16	0x0	RESET_4	Positive safing threshold for safing record 2

Table 219. SAF_THRESHOLD_P_3 - 0x0EF

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_P	RW	0	16	0x0	RESET_4	Positive safing threshold for safing record 3

Table 220. **SAF_THRESHOLD_P_4 - 0x0F0**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_P	RW	0	16	0x0	RESET_4	Positive safing threshold for safing record 4

Table 221. **SAF_THRESHOLD_P_5 - 0x0F1**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_P	RW	0	16	0x0	RESET_4	Positive safing threshold for safing record 5

Table 222. **SAF_THRESHOLD_P_6 - 0x0F2**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_P	RW	0	16	0x0	RESET_4	Positive safing threshold for safing record 6

Table 223. **SAF_THRESHOLD_P_7 - 0x0F3**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_P	RW	0	16	0x0	RESET_4	Positive safing threshold for safing record 7

Table 224. **SAF_THRESHOLD_P_8 - 0x0F4**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_P	RW	0	16	0x0	RESET_4	Positive safing threshold for safing record 8

Table 225. **SAF_THRESHOLD_P_9 - 0x0F5**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_P	RW	0	16	0x0	RESET_4	Positive safing threshold for safing record 9

Table 226. **SAF_THRESHOLD_P_10 - 0x0F6**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_P	RW	0	16	0x0	RESET_4	Positive safing threshold for safing record 10

Table 227. **SAF_THRESHOLD_P_11 - 0x0F7**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_P	RW	0	16	0x0	RESET_4	Positive safing threshold for safing record 11

Table 228. **SAF_THRESHOLD_P_12 - 0x0F8**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_P	RW	0	16	0x0	RESET_4	Positive safing threshold for safing record 12

Table 229. **SAF_THRESHOLD_P_13 - 0x0F9**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_P	RW	0	16	0x0	RESET_4	Positive safing threshold for safing record 13

Table 230. **SAF_THRESHOLD_P_14 - 0x0FA**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_P	RW	0	16	0x0	RESET_4	Positive safing threshold for safing record 14

Table 231. **SAF_THRESHOLD_P_15 - 0x0FB**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_P	RW	0	16	0x0	RESET_4	Positive safing threshold for safing record 15

Table 232. **SAF_THRESHOLD_P_16 - 0x0FC**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_P	RW	0	16	0x0	RESET_4	Positive safing threshold for safing record 16

Table 233. **SAF_THRESHOLD_P_17 - 0x0FD**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_P	RW	0	16	0x0	RESET_4	Positive safing threshold for safing record 17

Table 234. **SAF_THRESHOLD_P_18 - 0x0FE**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_P	RW	0	16	0x0	RESET_4	Positive safing threshold for safing record 18

Table 235. **NOP_GID_011 - 0x0FF**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	0	16	0x0	x	No operation response

5.1.2.5 *Safing 2 registers (GID = 100)*

Table 236. SAF_THRESHOLD_P_19 - 0x100

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_P	RW	0	16	0x0	RESET_4	Positive safing threshold for safing record 19

Table 237. SAF_THRESHOLD_P_20 - 0x101

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_P	RW	0	16	0x0	RESET_4	Positive safing threshold for safing record 20

Table 238. SAF_THRESHOLD_P_21 - 0x102

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_P	RW	0	16	0x0	RESET_4	Positive safing threshold for safing record 21

Table 239. SAF_THRESHOLD_N_0 - 0x103

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_N	RW	0	16	0x0	RESET_4	Negative safing threshold for safing record 0

Table 240. SAF_THRESHOLD_N_1 - 0x104

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_N	RW	0	16	0x0	RESET_4	Negative safing threshold for safing record 1

Table 241. SAF_THRESHOLD_N_2 - 0x105

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_N	RW	0	16	0x0	RESET_4	Negative safing threshold for safing record 2

Table 242. SAF_THRESHOLD_N_3 - 0x106

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_N	RW	0	16	0x0	RESET_4	Negative safing threshold for safing record 3

Table 243. SAF_THRESHOLD_N_4 - 0x107

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_N	RW	0	16	0x0	RESET_4	Negative safing threshold for safing record 4

Table 244. **SAF_THRESHOLD_N_5 - 0x108**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_N	RW	0	16	0x0	RESET_4	Negative safing threshold for safing record 5

Table 245. **SAF_THRESHOLD_N_6 - 0x109**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_N	RW	0	16	0x0	RESET_4	Negative safing threshold for safing record 6

Table 246. **SAF_THRESHOLD_N_7 - 0x10A**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_N	RW	0	16	0x0	RESET_4	Negative safing threshold for safing record 7

Table 247. **SAF_THRESHOLD_N_8 - 0x10B**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_N	RW	0	16	0x0	RESET_4	Negative safing threshold for safing record 8

Table 248. **SAF_THRESHOLD_N_9 - 0x10C**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_N	RW	0	16	0x0	RESET_4	Negative safing threshold for safing record 9

Table 249. **SAF_THRESHOLD_N_10 - 0x10D**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_N	RW	0	16	0x0	RESET_4	Negative safing threshold for safing record 10

Table 250. **SAF_THRESHOLD_N_11 - 0x10E**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_N	RW	0	16	0x0	RESET_4	Negative safing threshold for safing record 11

Table 251. **SAF_THRESHOLD_N_12 - 0x10F**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_N	RW	0	16	0x0	RESET_4	Negative safing threshold for safing record 12

Table 252. **SAF_THRESHOLD_N_13 - 0x110**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_N	RW	0	16	0x0	RESET_4	Negative safing threshold for safing record 13

Table 253. **SAF_THRESHOLD_N_14 - 0x111**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_N	RW	0	16	0x0	RESET_4	Negative safing threshold for safing record 14

Table 254. **SAF_THRESHOLD_N_15 - 0x112**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_N	RW	0	16	0x0	RESET_4	Negative safing threshold for safing record 15

Table 255. **SAF_THRESHOLD_N_16 - 0x113**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_N	RW	0	16	0x0	RESET_4	Negative safing threshold for safing record 16

Table 256. **SAF_THRESHOLD_N_17 - 0x114**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_N	RW	0	16	0x0	RESET_4	Negative safing threshold for safing record 17

Table 257. **SAF_THRESHOLD_N_18 - 0x115**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_N	RW	0	16	0x0	RESET_4	Negative safing threshold for safing record 18

Table 258. **SAF_THRESHOLD_N_19 - 0x116**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_N	RW	0	16	0x0	RESET_4	Negative safing threshold for safing record 19

Table 259. **SAF_THRESHOLD_N_20 - 0x117**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_N	RW	0	16	0x0	RESET_4	Negative safing threshold for safing record 20

Table 260. **SAF_THRESHOLD_N_21 - 0x118**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_THRESHOLD_N	RW	0	16	0x0	RESET_4	Negative safing threshold for safing record 21

Table 261. **SAF_FOC_SEEDVAL_0 - 0x119**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_FOC_SEEDVAL	RW	0	16	0x0	RESET_4	Fast offset cancellation value for safing record 0

Table 262. **SAF_FOC_SEEDVAL_1 - 0x11A**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_FOC_SEEDVAL	RW	0	16	0x0	RESET_4	Fast offset cancellation value for safing record 1

Table 263. **SAF_FOC_SEEDVAL_2 - 0x11B**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_FOC_SEEDVAL	RW	0	16	0x0	RESET_4	Fast offset cancellation value for safing record 2

Table 264. **SAF_FOC_SEEDVAL_3 - 0x11C**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_FOC_SEEDVAL	RW	0	16	0x0	RESET_4	Fast offset cancellation value for safing record 3

Table 265. **SAF_FOC_SEEDVAL_4 - 0x11D**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_FOC_SEEDVAL	RW	0	16	0x0	RESET_4	Fast offset cancellation value for safing record 4

Table 266. **SAF_FOC_SEEDVAL_5 - 0x11E**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_FOC_SEEDVAL	RW	0	16	0x0	RESET_4	Fast offset cancellation value for safing record 5

Table 267. **SAF_FOC_SEEDVAL_6 - 0x11F**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_FOC_SEEDVAL	RW	0	16	0x0	RESET_4	Fast offset cancellation value for safing record 6

Table 268. **SAF_FOC_SEEDVAL_7 - 0x120**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_FOC_SEEDVAL	RW	0	16	0x0	RESET_4	Fast offset cancellation value for safing record 7

Table 269. **SAF_FOC_SEEDVAL_8 - 0x121**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_FOC_SEEDVAL	RW	0	16	0x0	RESET_4	Fast offset cancellation value for safing record 8

Table 270. **SAF_FOC_SEEDVAL_9 - 0x122**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_FOC_SEEDVAL	RW	0	16	0x0	RESET_4	Fast offset cancellation value for safing record 9

Table 271. **SAF_FOC_SEEDVAL_10 - 0x123**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_FOC_SEEDVAL	RW	0	16	0x0	RESET_4	Fast offset cancellation value for safing record 10

Table 272. **SAF_FOC_SEEDVAL_11 - 0x124**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_FOC_SEEDVAL	RW	0	16	0x0	RESET_4	Fast offset cancellation value for safing record 11

Table 273. **SAF_FOC_SEEDVAL_12 - 0x125**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_FOC_SEEDVAL	RW	0	16	0x0	RESET_4	Fast offset cancellation value for safing record 12

Table 274. **SAF_FOC_SEEDVAL_13 - 0x126**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_FOC_SEEDVAL	RW	0	16	0x0	RESET_4	Fast offset cancellation value for safing record 13

Table 275. **SAF_FOC_SEEDVAL_14 - 0x127**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_FOC_SEEDVAL	RW	0	16	0x0	RESET_4	Fast offset cancellation value for safing record 14

Table 276. **SAF_FOC_SEEDVAL_15 - 0x128**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_FOC_SEEDVAL	RW	0	16	0x0	RESET_4	Fast offset cancellation value for safing record 15

Table 277. **SAF_FOC_SEEDVAL_16 - 0x129**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_FOC_SEEDVAL	RW	0	16	0x0	RESET_4	Fast offset cancellation value for safing record 16

Table 278. **SAF_FOC_SEEDVAL_17 - 0x12A**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_FOC_SEEDVAL	RW	0	16	0x0	RESET_4	Fast offset cancellation value for safing record 17

Table 279. **SAF_FOC_SEEDVAL_18 - 0x12B**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_FOC_SEEDVAL	RW	0	16	0x0	RESET_4	Fast offset cancellation value for safing record 18

Table 280. **SAF_FOC_SEEDVAL_19 - 0x12C**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_FOC_SEEDVAL	RW	0	16	0x0	RESET_4	Fast offset cancellation value for safing record 19

Table 281. **SAF_FOC_SEEDVAL_20 - 0x12D**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_FOC_SEEDVAL	RW	0	16	0x0	RESET_4	Fast offset cancellation value for safing record 20

Table 282. **SAF_FOC_SEEDVAL_21 - 0x12E**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_FOC_SEEDVAL	RW	0	16	0x0	RESET_4	Fast offset cancellation value for safing record 21

Table 283. **SAF_REQ_TARGET_0_PT1 - 0x12F**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable request target for safing record 0 (bits 15:0)

Table 284. **SAF_REQ_TARGET_0_PT2 - 0x130**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable request target for safing record 0 (bits 31:16)

Table 285. **SAF_REQ_TARGET_1_PT1 - 0x131**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable request target for safing record 1 (bits 15:0)

Table 286. **SAF_REQ_TARGET_1_PT2 - 0x132**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable request target for safing record 1 (bits 31:16)

Table 287. **SAF_REQ_TARGET_2_PT1 - 0x133**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable request target for safing record 2 (bits 15:0)

Table 288. **SAF_REQ_TARGET_2_PT2 - 0x134**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable request target for safing record 2 (bits 31:16)

Table 289. **SAF_REQ_TARGET_3_PT1 - 0x135**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable request target for safing record 3 (bits 15:0)

Table 290. **SAF_REQ_TARGET_3_PT2 - 0x136**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable request target for safing record 3 (bits 31:16)

Table 291. **SAF_REQ_TARGET_4_PT1 - 0x137**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable request target for safing record 4 (bits 15:0)

Table 292. **SAF_REQ_TARGET_4_PT2 - 0x138**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable request target for safing record 4 (bits 31:16)

Table 293. **SAF_REQ_TARGET_5_PT1 - 0x139**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable request target for safing record 5 (bits 15:0)

Table 294. **SAF_REQ_TARGET_5_PT2 - 0x13A**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable request target for safing record 5 (bits 31:16)

Table 295. **SAF_REQ_TARGET_6_PT1 - 0x13B**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable request target for safing record 6 (bits 15:0)

Table 296. **SAF_REQ_TARGET_6_PT2 - 0x13C**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable request target for safing record 6 (bits 31:16)

Table 297. **SAF_REQ_TARGET_7_PT1 - 0x13D**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable request target for safing record 7 (bits 15:0)

Table 298. **SAF_REQ_TARGET_7_PT2 - 0x13E**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable request target for safing record 7 (bits 31:16)

Table 299. **NOP_GID_100 - 0x13F**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	0	16	0x0	x	No operation response

5.1.2.6 *Safing 3 registers (GID = 101)*

Table 300. SAF_REQ_TARGET_8_PT1 - 0x140

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable request target for safing record 8 (bits 15:0)

Table 301. SAF_REQ_TARGET_8_PT2 - 0x141

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable request target for safing record 8 (bits 31:16)

Table 302. SAF_REQ_TARGET_9_PT1 - 0x142

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable request target for safing record 9 (bits 15:0)

Table 303. SAF_REQ_TARGET_9_PT2 - 0x143

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable request target for safing record 9 (bits 31:16)

Table 304. SAF_REQ_TARGET_10_PT1 - 0x144

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable request target for safing record 10 (bits 15:0)

Table 305. SAF_REQ_TARGET_10_PT2 - 0x145

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable request target for safing record 10 (bits 31:16)

Table 306. SAF_REQ_TARGET_11_PT1 - 0x146

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable request target for safing record 11 (bits 15:0)

Table 307. **SAF_REQ_TARGET_11_PT2 - 0x147**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable request target for safing record 11 (bits 31:16)

Table 308. **SAF_REQ_TARGET_12_PT1 - 0x148**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable request target for safing record 12 (bits 15:0)

Table 309. **SAF_REQ_TARGET_12_PT2 - 0x149**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable request target for safing record 12 (bits 31:16)

Table 310. **SAF_REQ_TARGET_13_PT1 - 0x14A**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable request target for safing record 13 (bits 15:0)

Table 311. **SAF_REQ_TARGET_13_PT2 - 0x14B**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable request target for safing record 13 (bits 31:16)

Table 312. **SAF_REQ_TARGET_14_PT1 - 0x14C**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable request target for safing record 14 (bits 15:0)

Table 313. **SAF_REQ_TARGET_14_PT2 - 0x14D**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable request target for safing record 14 (bits 31:16)

Table 314. **SAF_REQ_TARGET_15_PT1 - 0x14E**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable request target for safing record 15 (bits 15:0)

Table 315. SAF_REQ_TARGET_15_PT2 - 0x14F

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable request target for safing record 15 (bits 31:16)

Table 316. SAF_REQ_TARGET_16_PT1 - 0x150

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable request target for safing record 16 (bits 15:0)

Table 317. SAF_REQ_TARGET_16_PT2 - 0x151

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable request target for safing record 16 (bits 31:16)

Table 318. SAF_REQ_TARGET_17_PT1 - 0x152

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable request target for safing record 17 (bits 15:0)

Table 319. SAF_REQ_TARGET_17_PT2 - 0x153

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable request target for safing record 17 (bits 31:16)

Table 320. SAF_REQ_TARGET_18_PT1 - 0x154

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable request target for safing record 18 (bits 15:0)

Table 321. SAF_REQ_TARGET_18_PT2 - 0x155

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable request target for safing record 18 (bits 31:16)

Table 322. SAF_REQ_TARGET_19_PT1 - 0x156

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable request target for safing record 19 (bits 15:0)

Table 323. **SAF_REQ_TARGET_19_PT2 - 0x157**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable request target for safing record 19 (bits 31:16)

Table 324. **SAF_REQ_TARGET_20_PT1 - 0x158**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable request target for safing record 20 (bits 15:0)

Table 325. **SAF_REQ_TARGET_20_PT2 - 0x159**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable request target for safing record 20 (bits 31:16)

Table 326. **SAF_REQ_TARGET_21_PT1 - 0x15A**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable request target for safing record 21 (bits 15:0)

Table 327. **SAF_REQ_TARGET_21_PT2 - 0x15B**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable request target for safing record 21 (bits 31:16)

Table 328. **SAF_DATA_MASK_CS0_PT1 - 0x15C**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_DATA_MASK_15_0	RW	0	16	0x0	RESET_4	Programmable data mask for CS0 (bits 15:0)

Table 329. **SAF_DATA_MASK_CS0_PT2 - 0x15D**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_DATA_MASK_31_16	RW	0	16	0x0	RESET_4	Programmable data mask for CS0 (bits 31:16)

Table 330. **SAF_DATA_MASK_CS1_PT1 - 0x15E**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_DATA_MASK_15_0	RW	0	16	0x0	RESET_4	Programmable data mask for CS1 (bits 15:0)

Table 331. **SAF_DATA_MASK_CS1_PT2 - 0x15F**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_DATA_MASK_31_16	RW	0	16	0x0	RESET_4	Programmable data mask for CS1 (bits 31:16)

Table 332. **SAF_DATA_MASK_CS2_PT1 - 0x160**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_DATA_MASK_15_0	RW	0	16	0x0	RESET_4	Programmable data mask for CS2 (bits 15:0)

Table 333. **SAF_DATA_MASK_CS2_PT2 - 0x161**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_DATA_MASK_31_16	RW	0	16	0x0	RESET_4	Programmable data mask for CS2 (bits 31:16)

Table 334. **SAF_DATA_MASK_CS3_PT1 - 0x162**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_DATA_MASK_15_0	RW	0	16	0x0	RESET_4	Programmable data mask for CS3 (bits 15:0)

Table 335. **SAF_DATA_MASK_CS3_PT2 - 0x163**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_DATA_MASK_31_16	RW	0	16	0x0	RESET_4	Programmable data mask for CS3 (bits 31:16)

Table 336. **SAF_DATA_MASK_CS4_PT1 - 0x164**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_DATA_MASK_15_0	RW	0	16	0x0	RESET_4	Programmable data mask for CS4 (bits 15:0)

Table 337. **SAF_DATA_MASK_CS4_PT2 - 0x165**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_DATA_MASK_31_16	RW	0	16	0x0	RESET_4	Programmable data mask for CS4 (bits 31:16)

Table 338. **SAF_REQ_MASK_CS0_PT1 - 0x166**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_MASK_15_0	RW	0	16	0x0	RESET_4	Programmable request mask for CS0 (bits 15:0)

Table 339. **SAF_REQ_MASK_CS0_PT2 - 0x167**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_MASK_31_16	RW	0	16	0x0	RESET_4	Programmable request mask for CS0 (bits 31:16)

Table 340. **SAF_REQ_MASK_CS1_PT1 - 0x168**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_MASK_15_0	RW	0	16	0x0	RESET_4	Programmable request mask for CS1 (bits 15:0)

Table 341. **SAF_REQ_MASK_CS1_PT2 - 0x169**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_MASK_31_16	RW	0	16	0x0	RESET_4	Programmable request mask for CS1 (bits 31:16)

Table 342. **SAF_REQ_MASK_CS2_PT1 - 0x16A**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_MASK_15_0	RW	0	16	0x0	RESET_4	Programmable request mask for CS2 (bits 15:0)

Table 343. **SAF_REQ_MASK_CS2_PT2 - 0x16B**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_MASK_31_16	RW	0	16	0x0	RESET_4	Programmable request mask for CS2 (bits 31:16)

Table 344. **SAF_REQ_MASK_CS3_PT1 - 0x16C**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_MASK_15_0	RW	0	16	0x0	RESET_4	Programmable request mask for CS3 (bits 15:0)

Table 345. **SAF_REQ_MASK_CS3_PT2 - 0x16D**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_MASK_31_16	RW	0	16	0x0	RESET_4	Programmable request mask for CS3 (bits 31:16)

Table 346. **SAF_REQ_MASK_CS4_PT1 - 0x16E**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_MASK_15_0	RW	0	16	0x0	RESET_4	Programmable request mask for CS4 (bits 15:0)

Table 347. **SAF_REQ_MASK_CS4_PT2 - 0x16F**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_REQ_MASK_31_16	RW	0	16	0x0	RESET_4	Programmable request mask for CS4 (bits 31:16)

Table 348. **SAF_RESP_MASK_CS0_PT1 - 0x170**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_MASK_15_0	RW	0	16	0x0	RESET_4	Programmable response mask for CS0 (bits 15:0)

Table 349. **SAF_RESP_MASK_CS0_PT2 - 0x171**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_MASK_31_16	RW	0	16	0x0	RESET_4	Programmable response mask for CS0 (bits 31:16)

Table 350. **SAF_RESP_MASK_CS1_PT1 - 0x172**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_MASK_15_0	RW	0	16	0x0	RESET_4	Programmable response mask for CS1 (bits 15:0)

Table 351. **SAF_RESP_MASK_CS1_PT2 - 0x173**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_MASK_31_16	RW	0	16	0x0	RESET_4	Programmable response mask for CS1 (bits 31:16)

Table 352. **SAF_RESP_MASK_CS2_PT1 - 0x174**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_MASK_15_0	RW	0	16	0x0	RESET_4	Programmable response mask for CS2 (bits 15:0)

Table 353. **SAF_RESP_MASK_CS2_PT2 - 0x175**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_MASK_31_16	RW	0	16	0x0	RESET_4	Programmable response mask for CS2 (bits 31:16)

Table 354. **SAF_RESP_MASK_CS3_PT1 - 0x176**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_MASK_15_0	RW	0	16	0x0	RESET_4	Programmable response mask for CS3 (bits 15:0)

Table 355. **SAF_RESP_MASK_CS3_PT2 - 0x177**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_MASK_31_16	RW	0	16	0x0	RESET_4	Programmable response mask for CS3 (bits 31:16)

Table 356. **SAF_RESP_MASK_CS4_PT1 - 0x178**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_MASK_15_0	RW	0	16	0x0	RESET_4	Programmable response mask for CS4 (bits 15:0)

Table 357. **SAF_RESP_MASK_CS4_PT2 - 0x179**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_MASK_31_16	RW	0	16	0x0	RESET_4	Programmable response mask for CS4 (bits 31:16)

Table 358. **NOP_GID_101 - 0x17F**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	0	16	0x0	x	No operation response

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Table 359. SAF_RESP_TARGET_0_PT1 - 0x180

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 0 (bits 15:0)

Table 360. SAF_RESP_TARGET_0_PT2 - 0x181

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 0 (bits 31:16)

Table 361. SAF_RESP_TARGET_1_PT1 - 0x182

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 1 (bits 15:0)

Table 362. SAF_RESP_TARGET_1_PT2 - 0x183

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 1 (bits 31:16)

Table 363. SAF_RESP_TARGET_2_PT1 - 0x184

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 2 (bits 15:0)

Table 364. SAF_RESP_TARGET_2_PT2 - 0x185

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 2 (bits 31:16)

Table 365. SAF_RESP_TARGET_3_PT1 - 0x186

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 3 (bits 15:0)

Table 366. **SAF_RESP_TARGET_3_PT2 - 0x187**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 3 (bits 31:16)

Table 367. **SAF_RESP_TARGET_4_PT1 - 0x188**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 4 (bits 15:0)

Table 368. **SAF_RESP_TARGET_4_PT2 - 0x189**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 4 (bits 31:16)

Table 369. **SAF_RESP_TARGET_5_PT1 - 0x18A**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 5 (bits 15:0)

Table 370. **SAF_RESP_TARGET_5_PT2 - 0x18B**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 5 (bits 31:16)

Table 371. **SAF_RESP_TARGET_6_PT1 - 0x18C**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 6 (bits 15:0)

Table 372. **SAF_RESP_TARGET_6_PT2 - 0x18D**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 6 (bits 31:16)

Table 373. SAF_RESP_TARGET_7_PT1 - 0x18E

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 7 (bits 15:0)

Table 374. SAF_RESP_TARGET_7_PT2 - 0x18F

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 7 (bits 31:16)

Table 375. SAF_RESP_TARGET_8_PT1 - 0x190

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 8 (bits 15:0)

Table 376. SAF_RESP_TARGET_8_PT2 - 0x191

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 8 (bits 31:16)

Table 377. SAF_RESP_TARGET_9_PT1 - 0x192

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 9 (bits 15:0)

Table 378. SAF_RESP_TARGET_9_PT2 - 0x193

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 9 (bits 31:16)

Table 379. SAF_RESP_TARGET_10_PT1 - 0x194

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 10 (bits 15:0)

Table 380. **SAF_RESP_TARGET_10_PT2 - 0x195**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 10 (bits 31:16)

Table 381. **SAF_RESP_TARGET_11_PT1 - 0x196**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 11 (bits 15:0)

Table 382. **SAF_RESP_TARGET_11_PT2 - 0x197**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 11 (bits 31:16)

Table 383. **SAF_RESP_TARGET_12_PT1 - 0x198**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 12 (bits 15:0)

Table 384. **SAF_RESP_TARGET_12_PT2 - 0x199**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 12 (bits 31:16)

Table 385. **SAF_RESP_TARGET_13_PT1 - 0x19A**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 13 (bits 15:0)

Table 386. **SAF_RESP_TARGET_13_PT2 - 0x19B**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 13 (bits 31:16)

Table 387. **SAF_RESP_TARGET_14_PT1 - 0x19C**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 14 (bits 15:0)

Table 388. **SAF_RESP_TARGET_14_PT2 - 0x19D**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 14 (bits 31:16)

Table 389. **SAF_RESP_TARGET_15_PT1 - 0x19E**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 15 (bits 15:0)

Table 390. **SAF_RESP_TARGET_15_PT2 - 0x19F**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 15 (bits 31:16)

Table 391. **SAF_RESP_TARGET_16_PT1 - 0x1A0**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 16 (bits 15:0)

Table 392. **SAF_RESP_TARGET_16_PT2 - 0x1A1**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 16 (bits 31:16)

Table 393. **SAF_RESP_TARGET_17_PT1 - 0x1A2**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 17 (bits 15:0)

Table 394. **SAF_RESP_TARGET_17_PT2 - 0x1A3**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 17 (bits 31:16)

Table 395. **SAF_RESP_TARGET_18_PT1 - 0x1A4**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 18 (bits 15:0)

Table 396. **SAF_RESP_TARGET_18_PT2 - 0x1A5**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 18 (bits 31:16)

Table 397. **SAF_RESP_TARGET_19_PT1 - 0x1A6**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 19 (bits 15:0)

Table 398. **SAF_RESP_TARGET_19_PT2 - 0x1A7**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 19 (bits 31:16)

Table 399. **SAF_RESP_TARGET_20_PT1 - 0x1A8**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 20 (bits 15:0)

Table 400. **SAF_RESP_TARGET_20_PT2 - 0x1A9**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 20 (bits 31:16)

Table 401. SAF_RESP_TARGET_21_PT1 - 0x1AA

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_15_0	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 21 (bits 15:0)

Table 402. SAF_RESP_TARGET_21_PT2 - 0x1AB

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
SAF_RESP_TARGET_31_16	RW	0	16	0x0	RESET_4	Programmable response mask for safing record 21 (bits 31:16)

Table 403. SAF_CRC_CTRL - 0x1AD

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
CRC_ERR	RLR	15	1	0x0	RESET_4	CRC error flag: 0 = CRC error is not present 1 = CRC error is present
UNUSED	RO	13	2	0x0	x	Not used
CRC_EXP	RO	1	12	0x0	RESET_4	CRC to be matched (computed internally by the device after RECALC command is set)
RECALC	WO	0	1	0x0	RESET_4	CRC calculation restart: 1 = Request the recalculation of the CRC 0 = No action

Table 404. NOP_GID_110 - 0x1BF

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	0	16	0x0	x	No operation response

5.1.3 Global E2E SPI format

This format is specific to end to end communications and is used for writing and reading the E2E configuration registers, the writing of the ARM_E2E_STATUS register and the reading of ARM_RSLT[7:0] bit field. To use this specific SPI format, the E2E protocol must be active (as shown in Figure 26) and the GID must be set to “111”. The first MISO response after E2E activation will be 0x00000E2E. The 3-bit OPCODE determines the operation and the definition of the following bits in the SPI command frame. The E2E response is always out-of-frame.

Table 405. Global E2E SPI format, 32-bit out-of-frame protocol

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI_RS	111			0	OPCODE			E2E ADD						0	0	P	E2E CMD															
MISO_RS	SPI FLT		0	0	0	E2E FEEDBACK		Add Err	E2E DATA																							

While the E2E protocol is active, any global SPI commands with GID ≠ 111 will be ignored and the E2E data field in the response will be set to a fault response (address error).

In case of E2E active, if GID = 111 and the address is unused or OPCODE is unused, MISO response is all 0’s and the parity bit (odd parity).

SPI frame length and parity are checked also in case of E2E protocol is active.

Finally, E2E FEEDBACK bit field is included in the following frame to provide a response that the message has been received and is being processed according to the requested OPCODE.

5.1.4 Global E2E SPI register map

Note:

- *RO: READ ONLY*
- *RLR: READ LATCH UNTIL READ (clear on read)*
- *RW: READ/WRITE*
- *WO: WRITE ONLY (data read from WO registers/bits cannot necessarily be trusted except for ones indicated in register map description as "WO exception")*
- *RWL: CLEAR ON WRITE (the register is cleared writing '1' in the relative field)*

Table 406. E2E_NOP - 0x000

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	7	0x0	RESET_4	UNUSED
E2E_RX_CRC_ERR	RO	8	1	0x0	RESET_4	S8 = CRC received is wrong
E2E_RX_STATUS_REPEATED	RO	7	1	0x0	RESET_4	S7 = No N consecutive new data (N depends on profile)
E2E_RX_STATUS_WRONG_SEQUENCE	RO	6	1	0x0	RESET_4	S6 = Number of data lost is greater than allowed limit
E2E_RX_STATUS_OK_SOME_LOST	RO	5	1	0x0	RESET_4	S5 = Current received counter is ok but some data has been lost in previous communication
E2E_RX_STATUS_OK	RO	4	1	0x0	RESET_4	S4 = Counter received is ok and no data lost
E2E_RX_STATUS_SYNC	RO	3	1	0x0	RESET_4	S3 = Synchronization error
E2E_RX_STATUS_INIT	RO	2	1	0x0	RESET_4	S2 = Initialization phase is completed
E2E_RX_WAIT_FOR_FIRST_DATA	RO	1	1	0x0	RESET_4	S1 = First data is received
E2E_RX_NEW_DATA_AVAILABLE	RO	0	1	0x0	RESET_4	S0 = New update command is received

Table 407. E2E_ARM_GLOBAL_CFG - 0x001

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	4	12	0x0	RESET_4	NOTE: IF E2E_ACTIVATION IS INACTIVE THEN REMAINING BITS ARE DON'T CARE
E2E_RX_ARM_ACTIVATION	RW	3	1	0x0	RESET_4	0 = E2E_RX_ARM IS INACTIVE 1 = E2E_RX_ARM IS ACTIVE
E2E_TX2_ARM_ACTIVATION	RW	2	1	0x0	RESET_4	0 = E2E_TX2_ARM IS INACTIVE 1 = E2E_TX2_ARM IS ACTIVE
E2E_TX1_ARM_ACTIVATION	RW	1	1	0x0	RESET_4	0 = E2E_TX1_ARM IS INACTIVE 1 = E2E_TX1_ARM IS ACTIVE
E2E_ACTIVATION	RW	0	1	0x0	RESET_4	0 = E2E is INACTIVE 1 = E2E IS ACTIVE

Table 408. **E2E_ARM_DATA_ID_00_CFG - 0x002**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	12	2	0x0	RESET_4	Not used
DATA_ID_VALUE	RW	0	12	0x0	RESET_4	8 BIT OR 12 BIT DATA ID VALUE

Table 409. **E2E_ARM_DATA_ID_01_CFG - 0x003**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	12	2	0x0	RESET_4	Not used
DATA_ID_VALUE	RW	0	12	0x0	RESET_4	8 BIT OR 12 BIT DATA ID VALUE

Table 410. **E2E_ARM_DATA_ID_02_CFG - 0x004**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	12	2	0x0	RESET_4	Not used
DATA_ID_VALUE	RW	0	12	0x0	RESET_4	8 BIT OR 12 BIT DATA ID VALUE

Table 411. **E2E_ARM_DATA_ID_LIST_00_CFG - 0x005**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	12	2	0x0	RESET_4	Not used
DATA_ID_VALUE	RW	0	12	0x0	RESET_4	8 BIT OR 12 BIT DATA ID VALUE

Table 412. **E2E_ARM_DATA_ID_LIST_01_CFG - 0x006**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	12	2	0x0	RESET_4	Not used
DATA_ID_VALUE	RW	0	12	0x0	RESET_4	8 BIT OR 12 BIT DATA ID VALUE

Table 413. **E2E_ARM_DATA_ID_LIST_02_CFG - 0x007**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	12	2	0x0	RESET_4	Not used
DATA_ID_VALUE	RW	0	12	0x0	RESET_4	8 BIT OR 12 BIT DATA ID VALUE

Table 414. **E2E_ARM_DATA_ID_LIST_03_CFG - 0x008**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	12	2	0x0	RESET_4	Not used
DATA_ID_VALUE	RW	0	12	0x0	RESET_4	8 BIT OR 12 BIT DATA ID VALUE

Table 415. **E2E_ARM_DATA_ID_LIST_04_CFG - 0x009**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	12	2	0x0	RESET_4	Not used
DATA_ID_VALUE	RW	0	12	0x0	RESET_4	8 BIT OR 12 BIT DATA ID VALUE

Table 416. **E2E_ARM_DATA_ID_LIST_05_CFG - 0x00A**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	12	2	0x0	RESET_4	Not used
DATA_ID_VALUE	RW	0	12	0x0	RESET_4	8 BIT OR 12 BIT DATA ID VALUE

Table 417. **E2E_ARM_DATA_ID_LIST_06_CFG - 0x00B**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	12	2	0x0	RESET_4	Not used
DATA_ID_VALUE	RW	0	12	0x0	RESET_4	8 BIT OR 12 BIT DATA ID VALUE

Table 418. **E2E_ARM_DATA_ID_LIST_07_CFG - 0x00C**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	12	2	0x0	RESET_4	Not used
DATA_ID_VALUE	RW	0	12	0x0	RESET_4	8 BIT OR 12 BIT DATA ID VALUE

Table 419. **E2E_ARM_DATA_ID_LIST_08_CFG - 0x00D**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	12	2	0x0	RESET_4	Not used
DATA_ID_VALUE	RW	0	12	0x0	RESET_4	8 BIT OR 12 BIT DATA ID VALUE

Table 420. **E2E_ARM_DATA_ID_LIST_09_CFG - 0x00E**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	12	2	0x0	RESET_4	Not used
DATA_ID_VALUE	RW	0	12	0x0	RESET_4	8 BIT OR 12 BIT DATA ID VALUE

Table 421. **E2E_ARM_DATA_ID_LIST_0A_CFG - 0x00F**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	12	2	0x0	RESET_4	Not used
DATA_ID_VALUE	RW	0	12	0x0	RESET_4	8 BIT OR 12 BIT DATA ID VALUE

Table 422. **E2E_ARM_DATA_ID_LIST_0B_CFG - 0x010**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	12	2	0x0	RESET_4	Not used
DATA_ID_VALUE	RW	0	12	0x0	RESET_4	8 BIT OR 12 BIT DATA ID VALUE

Table 423. **E2E_ARM_DATA_ID_LIST_0C_CFG - 0x011**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	12	2	0x0	RESET_4	Not used
DATA_ID_VALUE	RW	0	12	0x0	RESET_4	8 BIT OR 12 BIT DATA ID VALUE

Table 424. **E2E_ARM_DATA_ID_LIST_0D_CFG - 0x012**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	12	2	0x0	RESET_4	Not used
DATA_ID_VALUE	RW	0	12	0x0	RESET_4	8 BIT OR 12 BIT DATA ID VALUE

Table 425. **E2E_ARM_DATA_ID_LIST_03_CFG - 0x013**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	12	2	0x0	RESET_4	Not used
DATA_ID_VALUE	RW	0	12	0x0	RESET_4	8 BIT OR 12 BIT DATA ID VALUE

Table 426. **E2E_ARM_DATA_ID_LIST_0F_CFG - 0x014**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	12	2	0x0	RESET_4	Not used
DATA_ID_VALUE	RW	0	12	0x0	RESET_4	8 BIT OR 12 BIT DATA ID VALUE

Table 427. **E2E_TX1_ARM_CFG - 0x015**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	2	0x0	RESET_4	UNUSED
E2E_TX1_PROFILE2_MODE	RW	13	1	0x0	RESET_4	0 = USE SHORT MODE 1 = USE LONG MODE
E2E_TX1_FORWARD_CRC	RW	12	1	0x0	RESET_4	Forward CRC on TX1 Function: 0 = Polynomial divider (NOT forward) 1 = No Polynomial divider (Forward)
E2E_TX1_ARM_DATA_ID_SELECTION	RW	9	3	0x0	RESET_4	000 = DATA_ID_00 001 = DATA_ID_01 010 = DATA_ID_02 011 = DATA_ID_LIST (IF PROFILE 2 IS USED)
E2E_TX1_ARM_PROFILE_SELECTION	RW	8	1	0x0	RESET_4	0 = USE PROFILE 1A 1 = USE PROFILE 2
E2E_TX1_ARM_BITx_ACTIVE	RW	0	8	0x0	RESET_4	ARMx (x from 0 to 7) BIT: 0 = IS NOT PART OF THE DATA PAYLOAD 1 = IS PART OF THE DATA PAYLOAD

Table 428. **E2E_TX1_ARM01_MAPPING_CFG - 0x016**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
E2E_ARMx_BIT1	RW	8	8	0x0	RESET_4	E2E_ARMx (x from 0 to 7) SIGNAL: 0 = IS NOT MAPPED TO E2E_TX1_ARM_BIT1

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						1 = IS MAPPED TO E2E_TX1_ARM_BIT1
E2E_ARMx_BIT0	RW	0	8	0x0	RESET_4	E2E_ARMx (x from 0 to 7) SIGNAL: 0 = IS NOT MAPPED TO E2E_TX1_ARM_BIT0 1 = IS MAPPED TO E2E_TX1_ARM_BIT0

Table 429. **E2E_TX1_ARM23_MAPPING_CFG - 0x017**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
E2E_ARMx_BIT3	RW	8	8	0x0	RESET_4	E2E_ARMx (x from 0 to 7) SIGNAL: 0 = IS NOT MAPPED TO E2E_TX1_ARM_BIT3 1 = IS MAPPED TO E2E_TX1_ARM_BIT3
E2E_ARMx_BIT2	RW	0	1	0x0	RESET_4	E2E_ARMx (x from 0 to 7) SIGNAL: 0 = IS NOT MAPPED TO E2E_TX1_ARM_BIT2 1 = IS MAPPED TO E2E_TX1_ARM_BIT2

Table 430. **E2E_TX1_ARM45_MAPPING_CFG - 0x018**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
E2E_ARMx_BIT5	RW	8	8	0x0	RESET_4	E2E_ARMx (x from 0 to 7) SIGNAL: 0 = IS NOT MAPPED TO E2E_TX1_ARM_BIT5 1 = IS MAPPED TO E2E_TX1_ARM_BIT5
E2E_ARMx_BIT4	RW	0	8	0x0	RESET_4	E2E_ARMx (x from 0 to 7) SIGNAL: 0 = IS NOT MAPPED TO E2E_TX1_ARM_BIT4 1 = IS MAPPED TO E2E_TX1_ARM_BIT4

Table 431. **E2E_TX1_ARM67_MAPPING_CFG - 0x019**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
E2E_ARMx_BIT7	RW	8	8	0x0	RESET_4	E2E_ARMx (x from 0 to 7) SIGNAL: 0 = IS NOT MAPPED TO E2E_TX1_ARM_BIT7 1 = IS MAPPED TO E2E_TX1_ARM_BIT7
E2E_ARMx_BIT6	RW	0	8	0x0	RESET_4	E2E_ARMx (x from 0 to 7) SIGNAL: 0 = IS NOT MAPPED TO E2E_TX1_ARM_BIT6 1 = IS MAPPED TO E2E_TX1_ARM_BIT6

Table 432. **E2E_TX2_ARM_CFG - 0x01A**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	2	0x0	RESET_4	UNUSED
E2E_TX2_PROFILE2_MODE	RW	13	1	0x0	RESET_4	0 = USE SHORT MODE 1 = USE LONG MODE

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
E2E_TX2_FORWARD_CRC	RW	12	1	0x0	RESET_4	Forward CRC on TX2 function: 0 = Polynomial divider (NOT forward) 1 = No polynomial divider (forward)
E2E_TX2_ARM_DATA_ID_SELECTION	RW	9	3	0x0	RESET_4	000 = DATA_ID_00 001 = DATA_ID_01 010 = DATA_ID_02 011 = DATA_ID_LIST (IF PROFILE 2 IS USED)
E2E_TX2_ARM_PROFILE_SELECTION	RW	8	1	0x0	RESET_4	0 = USE PROFILE 1A 1 = USE PROFILE 2
E2E_TX2_ARM_BITx_ACTIVE	RW	0	8	0x0	RESET_4	ARMx (x from 0 to 7) BIT: 0 = IS NOT PART OF THE DATA PAYLOAD 1 = IS PART OF THE DATA PAYLOAD

Table 433. E2E_TX2_ARM01_MAPPING_CFG - 0x01B

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
E2E_ARMx_BIT1	RW	8	8	0x0	RESET_4	E2E_ARMx (x from 0 to 7) SIGNAL: 0 = IS NOT MAPPED TO E2E_TX2_ARM_BIT1 1 = IS MAPPED TO E2E_TX2_ARM_BIT1
E2E_ARMx_BIT0	RW	0	8	0x0	RESET_4	E2E_ARMx (x from 0 to 7) SIGNAL: 0 = IS NOT MAPPED TO E2E_TX2_ARM_BIT0 1 = IS MAPPED TO E2E_TX2_ARM_BIT0

Table 434. E2E_TX2_ARM23_MAPPING_CFG - 0x01C

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
E2E_ARMx_BIT3	RW	8	8	0x0	RESET_4	E2E_ARMx (x from 0 to 7) SIGNAL: 0 = IS NOT MAPPED TO E2E_TX2_ARM_BIT3 1 = IS MAPPED TO E2E_TX2_ARM_BIT3
E2E_ARMx_BIT2	RW	0	8	0x0	RESET_4	E2E_ARMx (x from 0 to 7) SIGNAL: 0 = IS NOT MAPPED TO E2E_TX2_ARM_BIT2 1 = IS MAPPED TO E2E_TX2_ARM_BIT2

Table 435. E2E_TX2_ARM45_MAPPING_CFG - 0x01D

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
E2E_ARMx_BIT5	RW	8	8	0x0	RESET_4	E2E_ARMx (x from 0 to 7) SIGNAL: 0 = IS NOT MAPPED TO E2E_TX2_ARM_BIT5 1 = IS MAPPED TO E2E_TX2_ARM_BIT5

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
E2E_ARMx_BIT4	RW	0	8	0x0	RESET_4	E2E_ARMx (x from 0 to 7) SIGNAL: 0 = IS NOT MAPPED TO E2E_TX2_ARM_BIT4 1 = IS MAPPED TO E2E_TX2_ARM_BIT4

Table 436. E2E_TX2_ARM67_MAPPING_CFG - 0x01E

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
E2E_ARMx_BIT7	RW	8	8	0x0	RESET_4	E2E_ARMx (x from 0 to 7) SIGNAL: 0 = IS NOT MAPPED TO E2E_TX2_ARM_BIT7 1 = IS MAPPED TO E2E_TX2_ARM_BIT7
E2E_ARMx_BIT6	RW	0	8	0x0	RESET_4	E2E_ARMx (x from 0 to 7) SIGNAL: 0 = IS NOT MAPPED TO E2E_TX2_ARM_BIT6 1 = IS MAPPED TO E2E_TX2_ARM_BIT6

Table 437. E2E_RX_ARM_CFG - 0x01F

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	14	2	0x0	RESET_4	UNUSED
E2E_RX_PROFILE2_MODE	RW	13	1	0x0	RESET_4	0 = USE SHORT MODE 1 = USE LONG MODE
E2E_RX_FORWARD_CRC	RW	12	1	0x0	RESET_4	Forward CRC on RX function: 0 = Polynomial divider (NOT forward) 1 = No polynomial divider (forward)
E2E_RX_ARM_DATA_ID_SELECTION	RW	9	3	0x0	RESET_4	000 = DATA_ID_00 001 = DATA_ID_01 010 = DATA_ID_02 011 = DATA_ID_LIST (IF PROFILE 2 IS USED)
E2E_RX_ARM_PROFILE_SELECTION	RW	8	1	0x0	RESET_4	0 = USE PROFILE 1A 1 = USE PROFILE 2
E2E_RX_ARM_BITx_ACTIVE	RW	0	8	0x0	RESET_4	ARMx (x from 0 to 7) BIT: 0 = IS NOT PART OF THE DATA PAYLOAD 1 = IS PART OF THE DATA PAYLOAD

Table 438. E2E_RX_ARM_CFG3 - 0x020

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
E2E_RX_ARM_MAX_DELTA_COUNTER_INIT	RW	12	4	0x0	RESET_4	INITIAL MAX DELTA VALUE

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
E2E_RX_ARM_SYNC_COUNTER_INIT	RW	8	4	0x0	RESET_4	INITIAL SYNC COUNTER VALUE
E2E_RX_ARM_MAX_NO_NEW_OR_REPEATED_DATA	RW	4	4	0x0	RESET_4	MAXIMUM ALLOWED NO MESSAGES OR REPEATED MESSAGES
E2E_RX_ARM_DATA_ID_SELECT	RW	1	3	0x0	RESET_4	000 = DATA_ID_00 001 = DATA_ID_01 010 = DATA_ID_02 011 = DATA_ID_LIST (IF PROFILE 2 IS USED)
E2E_RX_ARM_PROFILE	RW	0	1	0x0	RESET_4	0 = USE PROFILE 1A 1 = USE PROFILE 2

Table 439. E2E_RX_ARM01_MAPPING_CFG - 0x021

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
E2E_ARMx_BIT1	RW	8	8	0x0	RESET_4	E2E_ARMx (x from 0 to 7) SIGNAL: 0 = IS NOT MAPPED TO E2E_RX_ARM_BIT1 1 = IS MAPPED TO E2E_RX_ARM_BIT1
E2E_ARMx_BIT0	RW	0	8	0x0	RESET_4	E2E_ARMx (x from 0 to 7) SIGNAL: 0 = IS NOT MAPPED TO E2E_RX_ARM_BIT0 1 = IS MAPPED TO E2E_RX_ARM_BIT0

Table 440. E2E_RX_ARM23_MAPPING_CFG - 0x022

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
E2E_ARMx_BIT3	RW	8	8	0x0	RESET_4	E2E_ARMx (x from 0 to 7) SIGNAL: 0 = IS NOT MAPPED TO E2E_RX_ARM_BIT3 1 = IS MAPPED TO E2E_RX_ARM_BIT3
E2E_ARMx_BIT2	RW	0	8	0x0	RESET_4	E2E_ARMx (x from 0 to 7) SIGNAL: 0 = IS NOT MAPPED TO E2E_RX_ARM_BIT2 1 = IS MAPPED TO E2E_RX_ARM_BIT2

Table 441. E2E_RX_ARM45_MAPPING_CFG - 0x023

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
E2E_ARMx_BIT5	RW	8	8	0x0	RESET_4	E2E_ARMx (x from 0 to 7) SIGNAL: 0 = IS NOT MAPPED TO E2E_RX_ARM_BIT5 1 = IS MAPPED TO E2E_RX_ARM_BIT5
E2E_ARMx_BIT4	RW	0	8	0x0	RESET_4	E2E_ARMx (x from 0 to 7) SIGNAL:

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						0 = IS NOT MAPPED TO E2E_RX_ARM_BIT4 1 = IS MAPPED TO E2E_RX_ARM_BIT4

Table 442. E2E_RX_ARM67_MAPPING_CFG - 0x024

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
E2E_ARMx_BIT7	RW	8	8	0x0	RESET_4	E2E_ARMx (x from 0 to 7) SIGNAL: 0 = IS NOT MAPPED TO E2E_RX_ARM_BIT7 1 = IS MAPPED TO E2E_RX_ARM_BIT7
E2E_ARMx_BIT6	RW	0	8	0x0	RESET_4	E2E_ARMx (x from 0 to 7) SIGNAL: 0 = IS NOT MAPPED TO E2E_RX_ARM_BIT6 1 = IS MAPPED TO E2E_RX_ARM_BIT6

Table 443. E2E_RX_ARM_DWELL_CFG - 0x025

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
E2E_ARMx_DWELL	RW	0	16	0x0	RESET_4	Two bits for each ARMx (x from 0 to 7): 00 = 2048 ms 01 = 256 ms 10 = 32 ms 11 = 0 ms

Table 444. GSPI_PROTOCOL_CTRL - 0x026

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
GSPI_PROTOCOL_CMD	WO	0	16	0x0	RESET_4	Command 0xF0F0 to pass from E2E to standard G_SPI

5.2 Remote sensor SPI protocol

Remote sensor SPI interface is a 32-bit bus compatible with SAFE SPI v1.0 standard (out-of-frame). The first MISO response is all 0's except the CRC field.

The remote sensor SPI is used by MCU to:

- Configure and communicate with the PSI5 sensor connected to the RSUx pins.
- Communicate with other digital sensors: MCU uses SPI_SAF_CSx to communicate with external digital sensors, providing additional sensor data to be used in the safing engine. When a specific SPI_SAF_CSx becomes active, both MOSI and MISO pins become inputs for the device that starts monitoring the communication between MCU and external devices, decoding the command and the response transferred on MOSI/MISO lines.

  A dedicated configurable SPI decoder is implemented for each specific SPI_SAF_CSx, supporting the protocol configured by the registers on the global SPI. If two or more SPI_SAF_CSx or SPI_CS_RS are asserted at the same time, the device cannot snoop the communication and MISO_RS is in HiZ.

The remote sensors SPI frame is composed has shown in Table 445.

Table 445. Remote sensor SPI frames

		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Command frame	MOSI_RS	TA										R/W	DATA																		CRC		
NON-Sensor data frame	MISO_RS	D=0	SA										DATA																		CRC		
Sensor data frame	MISO_RS	D=1	SA=00		SA[7:3]=LCID[4:0]					0	0	FC	S1	DATA																S0	CRC		

In MOSI frame, R/W bit distinguishes a read access (R/W = 0) or a write access (R/W = 1). The Target address (TA) is used to determine which is the register requested from the MCU. DATA field is used only in case of write access (in case of read access it is “don’t care”).

In MISO frame, the MSB distinguishes sensor data frame (D = 1) from non-sensor data frame (D = 0). In sensor data frame, the two status bits (S1 and S0), are used to indicate if the data field reports a valid sensor data or an error state with the detected faults. For the RSU interface, the cases S1:S0 = 0b10/0b11 are not used. In case of non-sensor data frame, the source address (SA) reports the address feedback of the previous access. Otherwise, in case of sensor data frame, the SA reports the LCID[4:0] = CH[2:0] + TimeSlot[1:0] used to uniquely identify the sensor and a frame counter (FC) that toggles for each valid sensor data received from remote sensor interface for that LCID.

For MISO responses from sensors that are selected by any of the SPI_SAF_CSx, the addressing field definitions are configured for the safing logic. Any data and status bit fields usage are also configured based upon the definitions for the sensor.

In case of a PSI5 sensor data request, the CRC is computed after Manchester decoding on the whole SPI response frame, to cover all the path from sensor to MISO_RS pin. The SPI response is then placed into the associated RSDRx buffer. In case of non-sensor data, the CRC is computed inside SPI decoder when the access is request. In both cases, the CRC polynomial is equal to x^3+x+1 with seed = 0b100 with “forward” method (this is equivalent to “nonforward” with seed = b101 as per SafeSPI spec).

Also for remote sensor SPI the device checks the validity of the access evaluating the frame length, the CRC and the address (address not existing) in each access. In case of SPI error (CRC, frame length or address error), a NOP response is generated, as shown in Table 446 and Table 447. The NOP register can also be requested with a normal read access (TA = 0x3FF).

Table 446. RS_SPI - NOP register format

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISO_RS	D=0	1	1	1	1	1	1	1	1	1	1	STATUS FLAGS																		CRC		

Table 447. RS_SPI - NOP status flags

Bit	20	19	18	17	16	15	14	13	12
Flag	Unused	SPI FAULTS CRC	SPI FAULT ADDRESS	SPI FAULT CLK PULSES	Unused	Unused	Unused	CLK IN ERR	VSYNC ERR
Bit	11	10	9	8	7	6	5	4	3
Flag	SATBCK ERR	RSU FLT CH7	RSU FLT CH6	RSU FLT CH5	RSU FLT CH4	RSU FLT CH3	RSU FLT CH2	RSU FLT CH1	RSU FLT CH0

The Table 446 and Table 447 show the scenario in case of SPI communication error and the status flags:

- SPI_FAULT_CRC: set in case of CRC error
- SPI_FAULT_ADDRESS: set in case of target address (TA) request does not exist
- SPI_FAULT_CLK_PULSES: set in case of frame short or frame long

- CLK_IN_ERR: set in case of clock monitor fault (echo of FREQ_ERR_FLAG)
- VSYNC_ERR: set in case of VSYNC_UV
- SATBCK_ERR: set in case of SATBCK fault (OT, UV, GND_LOSS)
- RSU_FLT_CHx: bitwise OR E1- E8 sensor error flags

Figure 27. SPI_RS communication error

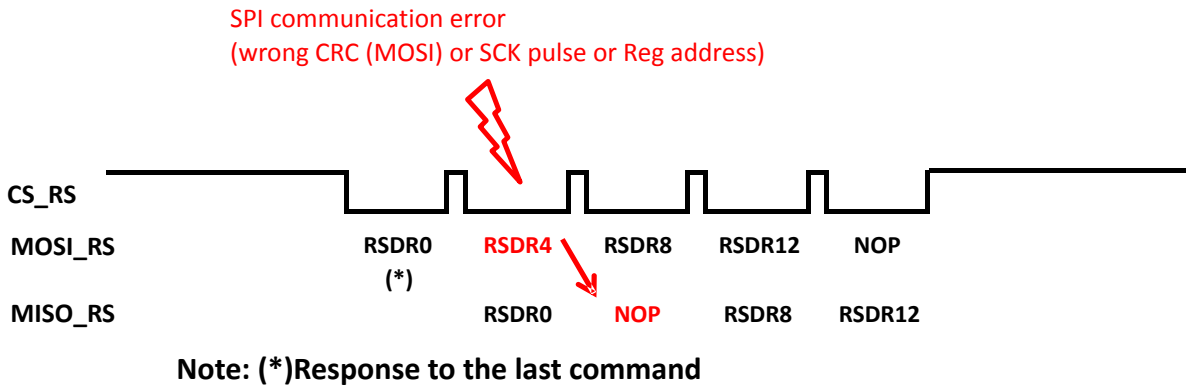
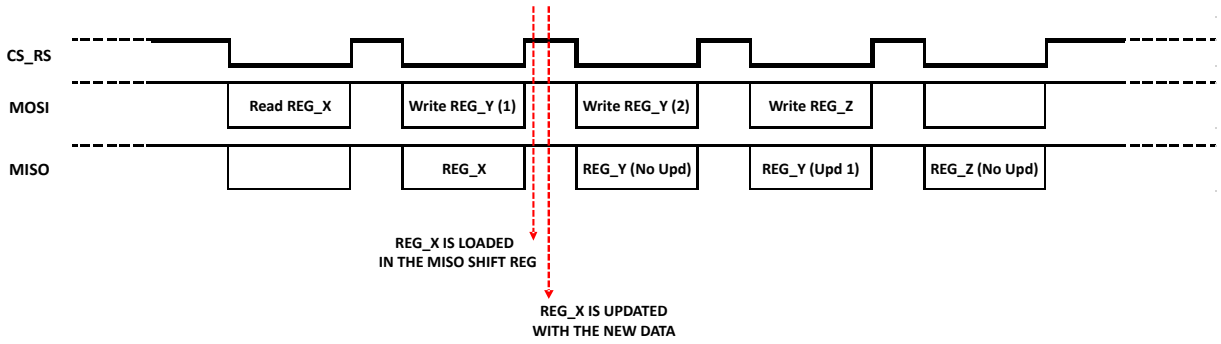


Figure 28. Write access SPI register updating



5.2.1 Global E2E SPI register map

Note:

- *RO: READ ONLY*
- *RLR: READ LATCH UNTIL READ (clear on read)*
- *RW: READ/WRITE*
- *WO: WRITE ONLY (data read from WO registers/bits cannot necessarily be trusted except for ones indicated in register map description as "WO exception")*
- *RWL: CLEAR ON WRITE (the register is cleared writing '1' in the relative field)*

Table 448. SPI_RS_MAP_intro

Register name	Address (HEX)	Init	Diag	Safing	Scrap	Arming safing	Arming scraping
RSDR0	0x000						
RSDR1	0x008						
RSDR2	0x010						
RSDR3	0x018						
RSDR4	0x020						
RSDR5	0x028						
RSDR6	0x030						
RSDR7	0x038						
RSDR8	0x040						
RSDR9	0x048						
RSDR10	0x050						
RSDR11	0x058						
RSDR12	0x060						
RSDR13	0x068						
RSDR14	0x070						
RSDR15	0x078						
RSDR16	0x080						
RSDR17	0x088						
RSDR18	0x090						
RSDR19	0x098						
RSDR20	0x0A0						
RSDR21	0x0A8						
RSDR22	0x0B0						
RSDR23	0x0B8						
RSDR24	0x0C0						
RSDR25	0x0C8						
RSDR26	0x0D0						
RSDR27	0x0D8						
RSDR28	0x0E0						
RSDR29	0x0E8						
RSDR30	0x0F0						
RSDR31	0x0F8						

Register name	Address (HEX)	Init	Diag	Safing	Scrap	Arming safing	Arming scraping
RSCR0	0x100		x				
Config_ST0_CH0	0x101		x				
Config_ST1_CH0	0x102		x				
Config_ST2_CH0	0x103		x				
Config_ST3_CH0	0x104		x				
Config_ET_CH0	0x105		x				
RSTH_CH0	0x106						
RSCR1	0x120		x				
Config_ST0_CH1	0x121		x				
Config_ST1_CH1	0x122		x				
Config_ST2_CH1	0x123		x				
Config_ST3_CH1	0x124		x				
Config_ET_CH1	0x125		x				
RSTH_CH1	0x126						
RSCR2	0x140		x				
Config_ST0_CH2	0x141		x				
Config_ST1_CH2	0x142		x				
Config_ST2_CH2	0x143		x				
Config_ST3_CH2	0x144		x				
Config_ET_CH2	0x145		x				
RSTH_CH2	0x146						
RSCR3	0x160		x				
Config_ST0_CH3	0x161		x				
Config_ST1_CH3	0x162		x				
Config_ST2_CH3	0x163		x				
Config_ST3_CH3	0x164		x				
Config_ET_CH3	0x165		x				
RSTH_CH3	0x166						
RSCR4	0x180		x				
Config_ST0_CH4	0x181		x				
Config_ST1_CH4	0x182		x				
Config_ST2_CH4	0x183		x				
Config_ST3_CH4	0x184		x				
Config_ET_CH4	0x185		x				
RSTH_CH4	0x186						
RSCR5	0x1A0		x				
Config_ST0_CH5	0x1A1		x				
Config_ST1_CH5	0x1A2		x				
Config_ST2_CH5	0x1A3		x				
Config_ST3_CH5	0x1A4		x				
Config_ET_CH5	0x1A5		x				

Register name	Address (HEX)	Init	Diag	Safing	Scrap	Arming safing	Arming scraping
RSTH_CH5	0x1A6						
RSCR6	0x1C0		x				
Config_ST0_CH6	0x1C1		x				
Config_ST1_CH6	0x1C2		x				
Config_ST2_CH6	0x1C3		x				
Config_ST3_CH6	0x1C4		x				
Config_ET_CH6	0x1C5		x				
RSTH_CH6	0x1C6						
RSCR7	0x1E0		x				
Config_ST0_CH7	0x1E1		x				
Config_ST1_CH7	0x1E2		x				
Config_ST2_CH7	0x1E3		x				
Config_ST3_CH7	0x1E4		x				
Config_ET_CH7	0x1E5		x				
RSTH_CH7	0x1E6						
RSCTRL	0x200		x	x	x	x	x
SYNC_PULSE	0x201		x	x	x	x	x
SAF_CC_PT1	0x202		x	x	x	x	x
SAF_CC_PT2	0x203		x	x	x	x	x
ARM_RSLT_STATE	0x204						
SNOOPING_TEST_INT_RS	0x205	x	x				
TM_ENTER	0x300	x	x	x	x	x	x
TM_FSM	0x301						
NOP	0x3FF						

Table 449. RSDR0 - 0x000

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 450. RSDR1 - 0x008

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 451. **RSDR2 - 0x010**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 452. **RSDR3 - 0x018**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 453. **RSDR4 - 0x020**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 454. **RSDR5 - 0x028**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 455. **RSDR6 - 0x030**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 456. **RSDR7 - 0x038**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 457. **RSDR8 - 0x040**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 458. **RSDR9 - 0x048**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 459. **RSDR10 - 0x050**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 460. **RSDR11 - 0x058**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 461. **RSDR12 - 0x060**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 462. **RSDR183 - 0x068**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 463. **RSDR14 - 0x070**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 464. **RSDR15 - 0x078**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 465. **RSDR16 - 0x080**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 466. **RSDR17 - 0x088**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 467. **RSDR18 - 0x090**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 468. **RSDR19 - 0x098**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 469. **RSDR20 - 0x0A0**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 470. **RSDR21 - 0x0A8**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 471. **RSDR22 - 0x0B0**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 472. **RSDR23 - 0x0B8**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 473. **RSDR24 - 0x0C0**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 474. **RSDR25 - 0x0C8**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 475. **RSDR26 - 0x0D0**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 476. **RSDR27 - 0x0D8**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 477. **RSDR28 - 0x0E0**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 478. **RSDR29 - 0x0E8**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 479. **RSDR30 - 0x0F0**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 480. **RSDR31 - 0x0F8**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
S1	RO	17	1	0x0	RESET_4	Status bit
DATA	RO	1	16	0x0	RESET_4	Sensor data if S1/S0 = 00 Error state if S1/S0 = 01 S1/S0 = 10 and S1/S0 = 11 Not used
S0	RO	0	1	0x0	RESET_4	Status bit

Table 481. **RSCR0 - 0x100**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
P_CRC_CHECKER_STATUS	RO	17	1	0x0	RESET_4	Parity/CRC CHECKER PSI5 interface status flag: 0 = CHECKER test not passed 1 = CHECKER test passed
P_CRC_CHECKER_START	RW	15	2	0x0	RESET_4	Parity/CRC CHECKER PSI5 interface start command: 00/11 = No action 01 = CHECKER start (correct data, expected status = 1) 10 = CHECKER start (wrong data, expected status = 0)
BLOCK_CURR_IN_MSG	RW	14	1	0x0	RESET_4	Tracking enable of base and delta current during message transmission: 0 = Ibase tracking is enabled during blanking and after start bits recognition 1 = Ibase tracking is enabled during blanking and disabled after start bits recognition
PERIOD_MEAS_DISABLE	RW	13	1	0x0	RESET_4	Disabling of start bits period measure to decode following bits: 0 = Period is measured 1 = Period is not measured
TS_DIS	RW	12	1	0x0	RESET_4	Time slot control disable: 0 = Control enable 1 = Control disable
SYNC_AMPL	RW	11	1	0x0	RESET_4	Sync pulse amplitude (only for trapezoidal wave): 0 = Normal 1 = Low
SYNC_WAVE	RW	10	1	0x0	RESET_4	Sync pulse waveform: 0 = Trapezoidal 1 = Sinusoidal
BLKT_SEL	RW	9	1	0x0	RESET_4	Blanking time selection: 0 = 5 ms 1 = 10 ms
FILT	RW	5	4	0x0	RESET_4	Filter time selection: for 125k filter time = (24+x)*Tosc for 189k filter time = (16+x)*Tosc
IMOD	RW	4	1	0x0	RESET_4	Modulation current: 0 = Normal 1 = Low power
STS	RW	0	4	0x0	RESET_4	Sensor type selection (PSI5 protocol)

Table 482. **Config_ST0_CH0 - 0x101**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 483. **Config_ST1_CH0 - 0x102**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 484. **Config_ST2_CH0 - 0x103**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 485. **Config_ST3_CH0 - 0x104**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 486. **Config_ET_CH0 - 0x101**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	End time (from 0 µs to 1023 µs with resolution of 1 µs) of last time slot. Internally clamped at max 516 µs

Table 487. **RSTH_CH0 - 0x106**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
AVERAGE_DELTA_CURRENT	RO	9	9	0x0	RESET_4	Average delta current (LSB = 187.5 µA ±9%)
BASE_CURRENT	RO	0	9	0x0	RESET_4	Base current (LSB = 187.5 µA ±9%)

Table 488. **RSCR1 - 0x120**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
P_CRC_CHECKER_STATUS	RO	17	1	0x0	RESET_4	Parity/CRC CHECKER PSI5 interface status flag: 0 = CHECKER test not passed 1 = CHECKER test passed
P_CRC_CHECKER_START	RW	15	2	0x0	RESET_4	Parity/CRC CHECKER PSI5 interface start command: 00/11 = No action 01 = CHECKER start (correct data, expected status = 1) 10 = CHECKER start (wrong data, expected status = 0)
BLOCK_CURR_IN_MSG	RW	14	1	0x0	RESET_4	Tracking enable of base and delta current during message transmission: 0 = Ibase tracking is enabled during blanking and after start bits recognition 1 = Ibase tracking is enabled during blanking and disabled after start bits recognition
PERIOD_MEAS_DISABLE	RW	13	1	0x0	RESET_4	Disabling of start bits period measure to decode following bits: 0 = Period is measured 1 = Period is not measured
TS_DIS	RW	12	1	0x0	RESET_4	Time slot control disable: 0 = Control enable 1 = Control disable
SYNC_AMPL	RW	11	1	0x0	RESET_4	Sync pulse amplitude (only for trapezoidal wave): 0 = Normal 1 = Low
SYNC_WAVE	RW	10	1	0x0	RESET_4	Sync pulse waveform: 0 = Trapezoidal 1 = Sinusoidal
BLKT_SEL	RW	9	1	0x0	RESET_4	Blanking time selection: 0=5 ms, 1=10 ms
FILT	RW	5	4	0x0	RESET_4	Filter time selection: for 125k filter time = (24+x)*Tosc for 189k filter time = (16+x)*Tosc
IMOD	RW	4	1	0x0	RESET_4	Modulation current: 0 = Normal 1 = Low power
STS	RW	0	4	0x0	RESET_4	Sensor type selection (PSI5 protocol)

Table 489. **Config_ST0_CH1 - 0x121**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 490. Config_ST1_CH1 - 0x122

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 491. Config_ST2_CH1 - 0x123

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 492. Config_ST3_CH1 - 0x124

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 493. Config_ET_CH1 - 0x125

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	End time (from 0 µs to 1023 µs with resolution of 1 µs) of last time slot. Internally clamped at max 516 µs

Table 494. RSTH_CH1 - 0x126

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
AVERAGE_DELTA_CURRENT	RO	9	9	0x0	RESET_4	Average delta current (LSB = 187.5 µA ±9%)
BASE_CURRENT	RO	0	9	0x0	RESET_4	Base current (LSB = 187.5 µA ±9%)

Table 495. RSCR2 - 0x140

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
P_CRC_CHECKER_STATUS	RO	17	1	0x0	RESET_4	Parity/CRC CHECKER PSI5 interface status flag: 0 = CHECKER test not passed

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						1 = CHECKER test passed
P_CRC_CHECKER_START	RW	15	2	0x0	RESET_4	Parity/CRC CHECKER PSI5 interface start command: 00/11 = No action 01 = CHECKER start (correct data, expected status = 1) 10 = CHECKER start (wrong data, expected status = 0)
BLOCK_CURR_IN_MSG	RW	14	1	0x0	RESET_4	Tracking enable of base and delta current during message transmission: 0 = Ibase tracking is enabled during blanking and after start bits recognition 1 = Ibase tracking is enabled during blanking and disabled after start bits recognition
PERIOD_MEAS_DISABLE	RW	13	1	0x0	RESET_4	Disabling of start bits period measure to decode following bits: 0 = Period is measured 1 = Period is not measured
TS_DIS	RW	12	1	0x0	RESET_4	Time slot control disable: 0 = Control enable 1 = Control disable
SYNC_AMPL	RW	11	1	0x0	RESET_4	Sync pulse amplitude (only for trapezoidal wave): 0 = Normal 1 = Low
SYNC_WAVE	RW	10	1	0x0	RESET_4	Sync pulse waveform: 0 = Trapezoidal 1 = Sinusoidal
BLKT_SEL	RW	9	1	0x0	RESET_4	Blanking time selection:. 0 = 5 ms 1 = 10 ms
FILT	RW	5	4	0x0	RESET_4	Filter time selection: for 125k filter time = (24+x)*Tosc for 189k filter time = (16+x)*Tosc
IMOD	RW	4	1	0x0	RESET_4	Modulation current: 0 = Normal 1 = Low power
STS	RW	0	4	0x0	RESET_4	Sensor type selection (PSI5 protocol)

Table 496. Config_ST0_CH2 - 0x141

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 497. **Config_ST1_CH2 - 0x142**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 498. **Config_ST2_CH2 - 0x143**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 499. **Config_ST3_CH2 - 0x144**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 500. **Config_ET_CH2 - 0x145**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	End time (from 0 µs to 1023 µs with resolution of 1 µs) of last time slot. Internally clamped at max 516 µs

Table 501. **RSTH_CH2 - 0x146**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
AVERAGE_DELTA_CURRENT	RO	9	9	0x0	RESET_4	Average delta current (LSB = 187.5 µA ±9%)
BASE_CURRENT	RO	0	9	0x0	RESET_4	Base current (LSB = 187.5 µA ±9%)

Table 502. **RSCR3 - 0x160**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
P_CRC_CHECKER_STATUS	RO	17	1	0x0	RESET_4	Parity/CRC CHECKER PSI5 interface status flag: 0 = CHECKER test not passed 1 = CHECKER test passed
P_CRC_CHECKER_START	RW	15	2	0x0	RESET_4	Parity/CRC CHECKER PSI5 interface start command: 00/11 = No action

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						01 = CHECKER start (correct data, expected status = 1) 10 = CHECKER start (wrong data, expected status = 0)
BLOCK_CURR_IN_MSG	RW	14	1	0x0	RESET_4	Tracking enable of base and delta current during message transmission: 0 = Ibase tracking is enabled during blanking and after start bits recognition 1 = Ibase tracking is enabled during blanking and disabled after start bits recognition
PERIOD_MEAS_DISABLE	RW	13	1	0x0	RESET_4	Disabling of start bits period measure to decode following bits: 0 = Period is measured 1 = Period is not measured
TS_DIS	RW	12	1	0x0	RESET_4	Time slot control disable: 0 = Control enable 1 = Control disable
SYNC_AMPL	RW	11	1	0x0	RESET_4	Sync pulse amplitude (only for trapezoidal wave): 0 = Normal 1 = Low
SYNC_WAVE	RW	10	1	0x0	RESET_4	Sync pulse waveform: 0 = Trapezoidal 1 = Sinusoidal
BLKT_SEL	RW	9	1	0x0	RESET_4	Blanking time selection: 0 = 5 ms 1 = 10 ms
FILT	RW	5	4	0x0	RESET_4	Filter time selection: for 125k filter time = (24+x)*Tosc for 189k filter time = (16+x)*Tosc
IMOD	RW	4	1	0x0	RESET_4	Modulation current: 0 = Normal 1 = Low power
STS	RW	0	4	0x0	RESET_4	Sensor type selection (PSI5 protocol)

Table 503. Config_ST0_CH3 - 0x161

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 504. **Config_ST1_CH3 - 0x162**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 505. **Config_ST2_CH3 - 0x163**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 506. **Config_ST3_CH3 - 0x164**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 507. **Config_ET_CH3 - 0x165**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	End time (from 0 µs to 1023 µs with resolution of 1 µs) of last time slot. Internally clamped at max 516 µs

Table 508. **RSTH_CH3 - 0x166**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
AVERAGE_DELTA_CURRENT	RO	9	9	0x0	RESET_4	Average delta current (LSB = 187.5 µA ±9%)
BASE_CURRENT	RO	0	9	0x0	RESET_4	Base current (LSB = 187.5 µA ±9%)

Table 509. **RSCR4 - 0x180**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
P_CRC_CHECKER_STATUS	RO	17	1	0x0	RESET_4	Parity/CRC CHECKER PSI5 interface status flag: 0 = CHECKER test not passed 1 = CHECKER test passed
P_CRC_CHECKER_START	RW	15	2	0x0	RESET_4	Parity/CRC CHECKER PSI5 interface start command: 00/11 = No action

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						01 = CHECKER start (correct data, expected status = 1) 10 = CHECKER start (wrong data, expected status = 0)
BLOCK_CURR_IN_MSG	RW	14	1	0x0	RESET_4	Tracking enable of base and delta current during message transmission: 0 = Ibase tracking is enabled during blanking and after start bits recognition 1 = Ibase tracking is enabled during blanking and disabled after start bits recognition
PERIOD_MEAS_DISABLE	RW	13	1	0x0	RESET_4	Disabling of start bits period measure to decode following bits: 0 = Period is measured 1 = Period is not measured
TS_DIS	RW	12	1	0x0	RESET_4	Time slot control disable: 0 = Control enable 1 = Control disable
SYNC_AMPL	RW	11	1	0x0	RESET_4	Sync pulse amplitude (only for trapezoidal wave): 0 = Normal 1 = Low
SYNC_WAVE	RW	10	1	0x0	RESET_4	Sync pulse waveform: 0 = Trapezoidal 1 = Sinusoidal
BLKT_SEL	RW	9	1	0x0	RESET_4	Blanking time selection: 0 = 5 ms 1 = 10 ms
FILT	RW	5	4	0x0	RESET_4	Filter time selection: for 125k filter time = (24+x)*Tosc for 189k filter time = (16+x)*Tosc
IMOD	RW	4	1	0x0	RESET_4	Modulation current: 0 = Normal 1 = Low power
STS	RW	0	4	0x0	RESET_4	Sensor type selection (PSI5 protocol)

Table 510. Config_ST0_CH4 - 0x181

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 511. **Config_ST1_CH4 - 0x182**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 512. **Config_ST2_CH4 - 0x183**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 513. **Config_ST4_CH4 - 0x184**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 514. **Config_ET_CH4 - 0x185**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	End time (from 0 µs to 1023 µs with resolution of 1 µs) of last time slot. Internally clamped at max 516 µs

Table 515. **RSTH_CH4 - 0x186**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
AVERAGE_DELTA_CURRENT	RO	9	9	0x0	RESET_4	Average delta current (LSB = 187.5 µA ±9%)
BASE_CURRENT	RO	0	9	0x0	RESET_4	Base current (LSB = 187.5 µA ±9%)

Table 516. **RSCR5 - 0x1A0**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
P_CRC_CHECKER_STATUS	RO	17	1	0x0	RESET_4	Parity/CRC CHECKER PSI5 interface status flag: 0 = CHECKER test not passed 1 = CHECKER test passed
P_CRC_CHECKER_START	RW	15	2	0x0	RESET_4	Parity/CRC CHECKER PSI5 interface start command: 00/11 = No action

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						01 = CHECKER start (correct data, expected status = 1) 10 = CHECKER start (wrong data, expected status = 0)
BLOCK_CURR_IN_MSG	RW	14	1	0x0	RESET_4	Tracking enable of base and delta current during message transmission: 0 = Ibase tracking is enabled during blanking and after start bits recognition 1 = Ibase tracking is enabled during blanking and disabled after start bits recognition
PERIOD_MEAS_DISABLE	RW	13	1	0x0	RESET_4	Disabling of start bits period measure to decode following bits: 0 = Period is measured 1 = Period is not measured
TS_DIS	RW	12	1	0x0	RESET_4	Time slot control disable: 0 = Control enable 1 = Control disable
SYNC_AMPL	RW	11	1	0x0	RESET_4	Sync pulse amplitude (only for trapezoidal wave): 0 = Normal 1 = Low
SYNC_WAVE	RW	10	1	0x0	RESET_4	Sync pulse waveform: 0 = Trapezoidal 1 = Sinusoidal
BLKT_SEL	RW	9	1	0x0	RESET_4	Blanking time selection: 0 = 5 ms 1 = 10 ms
FILT	RW	5	4	0x0	RESET_4	Filter time selection: for 125k filter time = (24+x)*Tosc for 189k filter time = (16+x)*Tosc
IMOD	RW	4	1	0x0	RESET_4	Modulation current: 0 = Normal 1 = Low power
STS	RW	0	4	0x0	RESET_4	Sensor type selection (PSI5 protocol)

Table 517. Config_ST0_CH5 - 0x1A1

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 518. **Config_ST1_CH5 - 0x1A2**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 519. **Config_ST2_CH5 - 0x1A3**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 520. **Config_ST3_CH5 - 0x1A4**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 521. **Config_ET_CH5 - 0x1A5**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	End time (from 0 µs to 1023 µs with resolution of 1 µs) of last time slot. Internally clamped at max 516 µs

Table 522. **RSTH_CH5 - 0x1A6**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
AVERAGE_DELTA_CURRENT	RO	9	9	0x0	RESET_4	Average delta current (LSB = 187.5 µA ±9%)
BASE_CURRENT	RO	0	9	0x0	RESET_4	Base current (LSB = 187.5 µA ±9%)

Table 523. **RSCR6 - 0x1C0**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
P_CRC_CHECKER_STATUS	RO	17	1	0x0	RESET_4	Parity/CRC CHECKER PSI5 interface status flag: 0 = CHECKER test not passed 1 = CHECKER test passed
P_CRC_CHECKER_START	RW	15	2	0x0	RESET_4	Parity/CRC CHECKER PSI5 interface start command: 00/11 = No action

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						01 = CHECKER start (correct data, expected status = 1) 10 = CHECKER start (wrong data, expected status = 0)
BLOCK_CURR_IN_MSG	RW	14	1	0x0	RESET_4	Tracking enable of base and delta current during message transmission: 0 = Ibase tracking is enabled during blanking and after start bits recognition 1 = Ibase tracking is enabled during blanking and disabled after start bits recognition
PERIOD_MEAS_DISABLE	RW	13	1	0x0	RESET_4	Disabling of start bits period measure to decode following bits: 0 = Period is measured 1 = Period is not measured
TS_DIS	RW	12	1	0x0	RESET_4	Time slot control disable: 0 = Control enable 1 = Control disable
SYNC_AMPL	RW	11	1	0x0	RESET_4	Sync pulse amplitude (only for trapezoidal wave): 0 = Normal 1 = Low
SYNC_WAVE	RW	10	1	0x0	RESET_4	Sync pulse waveform: 0 = Trapezoidal 1 = Sinusoidal
BLKT_SEL	RW	9	1	0x0	RESET_4	Blanking time selection: 0 = 5 ms 1 = 10 ms
FILT	RW	5	4	0x0	RESET_4	Filter time selection: for 125k filter time = (24+x)*Tosc for 189k filter time = (16+x)*Tosc
IMOD	RW	4	1	0x0	RESET_4	Modulation current: 0 = Normal 1 = Low power
STS	RW	0	4	0x0	RESET_4	Sensor type selection (PSI5 protocol)

Table 524. Config_ST0_CH6 - 0x1C1

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 525. **Config_ST1_CH6 - 0x1C2**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 526. **Config_ST2_CH6 - 0x1C3**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 527. **Config_ST3_CH6 - 0x1C4**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 528. **Config_ET_CH6 - 0x1C5**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	End time (from 0 µs to 1023 µs with resolution of 1 µs) of last time slot. Internally clamped at max 516 µs

Table 529. **RSTH_CH6 - 0x1C6**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
AVERAGE_DELTA_CURRENT	RO	9	9	0x0	RESET_4	Average delta current (LSB = 187.5 µA ±9%)
BASE_CURRENT	RO	0	9	0x0	RESET_4	Base current (LSB = 187.5 µA ±9%)

Table 530. **RSCR7 - 0x1E0**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
P_CRC_CHECKER_STATUS	RO	17	1	0x0	RESET_4	Parity/CRC CHECKER PSI5 interface status flag: 0 = CHECKER test not passed 1 = CHECKER test passed
P_CRC_CHECKER_START	RW	15	2	0x0	RESET_4	Parity/CRC CHECKER PSI5 interface start command: 00/11 = No action

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
						01 = CHECKER start (correct data, expected status = 1) 10 = CHECKER start (wrong data, expected status = 0)
BLOCK_CURR_IN_MSG	RW	14	1	0x0	RESET_4	Tracking enable of base and delta current during message transmission: 0 = Ibase tracking is enabled during blanking and after start bits recognition 1 = Ibase tracking is enabled during blanking and disabled after start bits recognition
PERIOD_MEAS_DISABLE	RW	13	1	0x0	RESET_4	Disabling of start bits period measure to decode following bits: 0 = Period is measured 1 = Period is not measured
TS_DIS	RW	12	1	0x0	RESET_4	Time slot control disable: 0 = Control enable 1 = Control disable
SYNC_AMPL	RW	11	1	0x0	RESET_4	Sync pulse amplitude (only for trapezoidal wave): 0 = Normal 1 = Low
SYNC_WAVE	RW	10	1	0x0	RESET_4	Sync pulse waveform: 0 = Trapezoidal 1 = Sinusoidal
BLKT_SEL	RW	9	1	0x0	RESET_4	Blanking time selection: 0 = 5 ms 1 = 10 ms
FILT	RW	5	4	0x0	RESET_4	Filter time selection: for 125k filter time = (24+x)*Tosc for 189k filter time = (16+x)*Tosc
IMOD	RW	4	1	0x0	RESET_4	Modulation current: 0 = Normal 1 = Low power
STS	RW	0	4	0x0	RESET_4	Sensor type selection (PSI5 protocol)

Table 531. Config_ST0_CH7 - 0x1E1

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 532. **Config_ST1_CH7 - 0x1E2**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 533. **Config_ST2_CH7 - 0x1E3**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 534. **Config_ST3_CH7 - 0x1E4**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	Start time (from 0 µs to 511 µs with resolution of 1 µs)

Table 535. **Config_ET_CH7 - 0x1E5**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	9	9	0x0	x	Not used
START_TIME	RW	0	9	0x0	RESET_4	End time (from 0 µs to 1023 µs with resolution of 1 µs) of last time slot. Internally clamped at max 516 µs

Table 536. **RSTH_CH7 - 0x1E6**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
AVERAGE_DELTA_CURRENT	RO	9	9	0x0	RESET_4	Average delta current (LSB = 187.5 µA ±9%)
BASE_CURRENT	RO	0	9	0x0	RESET_4	Base current (LSB = 187.5 µA ±9%)

Table 537. **RSCTRL - 0x200**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	8	10	0x0	x	Not used
CHxEN	RW	0	8	0x0	RESET_2	Remote sensor interface channel x (x from 0 to 7) enable

Table 538. **SYNC_PULSE - 0X201**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	17	1	0x0	x	Not used
SAF_CC_CLEAR_ALL	WO	16	1	0x0	RESET_4	Command to clear all SAF_CC bits: 0 = No effect 1 = Clear all SAF_CC flags
UNUSED	RO	8	8	0x0	x	Not used
CHxSYNC	WO	0	8	0x0	RESET_4	Sync pulse generation on channel x (x from 0 to 7)

Table 539. **SAF_CC_PT1 - 0X202**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	16	2	0x0	x	Not used
SAF_CCx	RLW	0	16	0x0	RESET_2	Compare complete status and end of sample cycle of safing record x (x from 0 to 15)

Table 540. **SAF_CC_PT2 - 0X203**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	6	12	0x0	x	Not used
SAF_CCx	RLW	0	16	0x0	RESET_2	Compare complete status and end of sample cycle of safing record x (x from 16 to 21)

Table 541. **ARM_RSLT_STATE - 0x204**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	16	2	0x0	x	Not used
PSINHRSLT	RO	15	1	0x0	RESET_4	Resulting PSINH signal status latched PSINH status when DEP_ENABLED is true (unlocked). Otherwise, it becomes the combinatorial status of PSINH.
UNUSED	RO	8	7	0x0	x	Not used
ARMRSLT_x	RO	0	8	0x0	RESET_4	Resulting ARM x (x from 0 to 7) signal status

Table 542. **SNOOPING_TEST_INT_RS - 0x205**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	16	2	0x0	x	Not used
SNOOP_TEST_INT_RS	RW	0	16	0x0	RESET_4	Register to test snooping logic. Data written by MCU writes this register which is snooped by other device when Read request is issued.

Table 543. **TM_ENTER - 0x300**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	16	2	0x0	x	Not used
TM_ENTER_CMD	RW	0	16	0x0	RESET_1	ST_RESEVED

Table 544. **TM_FSM - 0x301**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	5	13	0x0	x	Not used
TM_PIN_FDBK	RO	4	1	0x0	RESET_1	TM pin status monitor
UNUSED	RO	3	1	0x0	RESET_1	Not used
TM_FSM_STATUS	RO	0	3	0x0	RESET_1	Status of TM FSM: 000 = Func 001 = HW TM pin 010 = Partial TM 011 = Full_TM 100 = Err others = Not used

Table 545. **NOP - 0x3FF**

Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
UNUSED	RO	17	1	0x0	x	Not used
SPI_FAULT_CRC	RO	16	1	0x0	RESET_4	SPI communication fault: CRC error
SPI_FAULT_ADDRESS	RO	15	1	0x0	RESET_4	SPI communication fault: target address (TA) error
SPI_FAULT_CLK_PULSES	RO	14	1	0x0	RESET_4	SPI communication fault: wrong frame lenght
UNUSED	RO	11	3	0x0	x	Not used
CLK_ERR	RLR	10	1	0x0	RESET_2	Clock monitor error: echo of CLK_FREQ_ERR_FLAG[1] (that is CLK_MAIN or CLK_AUX error) or FLL is not enabled
VSYNC_ERR	RLR	9	1	0x0	RESET_2	VSYNC fault (UV)
VSAT_ERR	RLR	8	1	0x0	RESET_2	SATBUCK fault (OT,UV,GND_LOSS), echo of SPI_G flag
RSU_FLT_CHx	RO	0	8	0x0	RESET_4	Bit-wise OR of all RSU error flags (except NO_DATA) on CHx (x from 0 to 7)

6 Power supply and energy reserve management

6.1 SYS boost regulator

SYS boost regulator is a DC-DC boost converter with integrated LS driver and switching frequency in the range of 2 MHz whose function is to provide sufficient system power under low battery voltage condition (that is low voltage at VIN pin), guaranteeing a nominal 10 V supply voltage to the device (V_{O_SYSBST}). Regulator circuit involves 3 pins:

- SYSBST: boost regulation output.
- SYSBSTSW: boost switching node, connecting to the integrated LS driver stage.
- BSTGND: LS driver power ground (shared with ER boost).

Regulator circuit is enabled at power-up, as soon as device enters ACTIVE mode, STARTUP state; if VIN voltage is above $V_{VIN\_SYSBST\_DIS}$ threshold (with hysteresis $V_{VIN\_SYSBST\_DIS\_HYST}$), regulator is forced in disable state and SYSBST pin is supplied directly from the battery line through the external components placed on the ECU (that is diodes, inductors, etc.). As VIN voltage drops below $V_{VIN\_SYSBST\_DIS}$, switching regulator circuit is enabled; actual switching operation starts as soon as SYSBST node voltage is charged up to V_{VIN}-$V_{SYSBST\_CHG\_DIS}$, ensuring that the external diode connected between VIN and SYSBST pins, thus the SYSBST pin is not open. Additionally, as device enters PASSIVE mode, regulator is disabled, as SYSBST pin is externally supplied from the ER capacitor.

Every time SYS boost regulator is enabled, soft start is performed by applying a ramp on LS overcurrent threshold $I_{OC\_SYSBSTSW}$, that is within t_{SOFTST_SYSBST} time, $I_{OC\_SYSBSTSW}$ value is increased from 20% to 100% with 16 steps. As soft start transition is completed, V_{O_SYSBST} regulation voltage output is guaranteed if both VIN voltage is the $V_{VIN\_SYSBST\_LINEAR}$ range and regulator output current is in I_{O_SYSBST} range, that is regulator linear operation; in this condition, control circuit ensures that both subharmonic generation and burst mode are avoided. Switching frequency can be tuned using PWR_CTRL_1 global SPI register, SWREG_F_SEL bit; 2 options are available:

- SWREG_F_SEL = 0 (default): $f_{SW\_SYSBST\_1}$ = 2 MHz typical value
- SWREG_F_SEL = 1: $f_{SW\_SYSBST\_2}$ = 2.13 MHz typical value

If VIN voltage increases and goes outside $V_{VIN\_SYSBST\_LINEAR}$ range, switching duty-cycle is reduced to the minimum value and SYSBST voltage goes outside the nominal operation range, that is V_{SYSBST}>V_{O_SYSBST}; no action is taken until SYSBST voltage goes above V_{OV_SYSBST} overvoltage threshold (with hysteresis $V_{OV\_SYSBST\_HYST}$) for a time longer than $t_{OV\_SYSBST\_FLT}$: this happens when output current goes below I_{O_SYSBST} range; if this happens, SYS boost regulator is disabled and SYSBST_OV bit (PWR_STATUS_0 global SPI register) is set. SYS boost operation is then recovered in either of the 2 following cases:

- SYSBST voltage goes again below V_{OV_SYSBST} for a time longer than $t_{OV\_SYSBST\_BLK}$
- SYSBST voltage goes below V_{UV_SYSBST} undervoltage threshold value for a time longer than $t_{UV\_SYSBST\_FLT}$

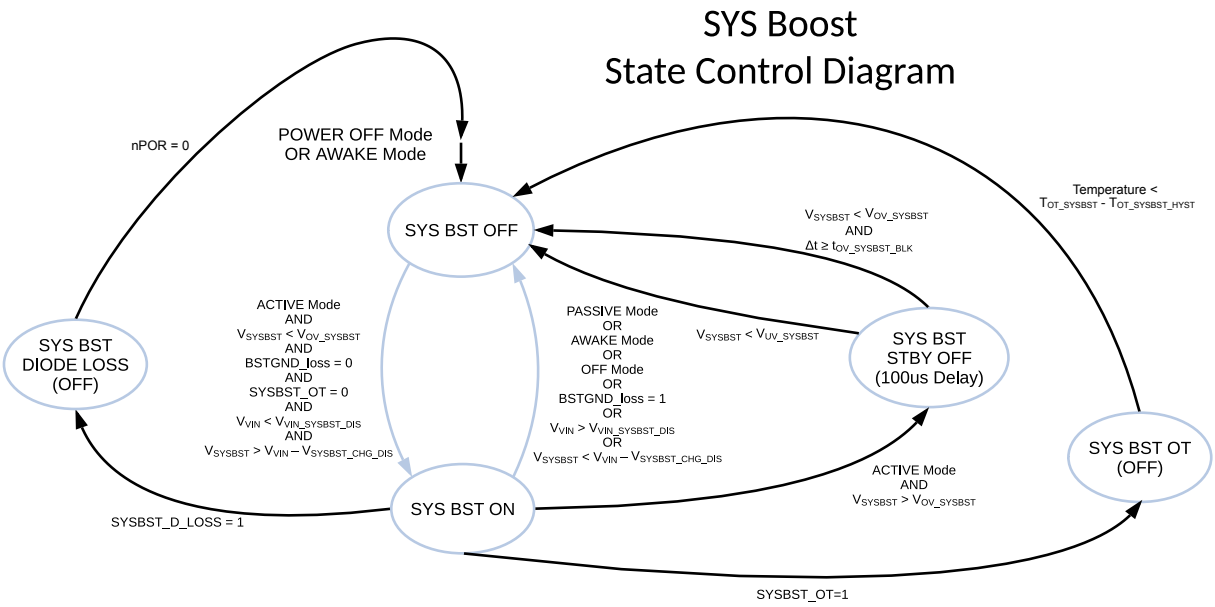
In both cases, SYSBST_OV bit is cleared upon SPI reading, after overvoltage has disappeared.

The following diagnostic and protection features are provided as well:

- Undervoltage detection: as SYSBST pin voltage goes below V_{UV_SYSBST} threshold value for a time longer than $t_{UV\_SYSBST\_FLT}$, undervoltage is detected and SYSBST_UV bit (PWR_STATUS_0 global SPI register) is set; bit is cleared upon SPI reading after fault has disappeared.
- BSTGND ground loss detection: as V_{BSTGND}-$V_{SUBGNDx}$ exceeds $V_{BSTGND\_LOSS\_TH}$ for a time longer than $t_{BSTGND\_LOSS\_FLT}$, regulator is disabled and automatically reenabled once ground connection is restored. Ground loss detection is available even when regulator is off, as a pullup current generator I_{PU_BSTGND} is always connected to BSTGND; detection in disabled state does not allow SYS boost enabling. As detection occurs, BSTGND_LOSS bit (PWR_STATUS_0 global SPI register) is set; bit is cleared upon SPI reading as fault has disappeared.

- Overtemperature detection: as LS driver temperature exceeds T_{OT_SYSBST} (with hysteresis $T_{OT\_SYSBST\_HYST}$) for a time longer than $t_{OT\_SYSBST\_FLT}$, regulator is disabled; SYSBST_OT bit (PWR_STATUS_0 global SPI register) is set. Regulator is automatically reenabled once fault has disappeared, that is when the temperature decreases under the low temperature threshold.
- Diode loss detection and SYSBSTSW pin voltage clamping: external diode loss failure is detected as $V_{SYSBSTSW}$ - V_{SYSBST} voltage difference exceeds $V_{D\_LOSS\_TH\_SYSBST}$ threshold; this event activates the voltage clamping circuit on SYSBSTSW pin, limiting voltage value to $V_{CLAMP\_SYSBSTSW}$. As 5 successive clamping events are counted, SYS boost regulator is disabled permanently and SYSBST_D_LOSS bit (GSW global SPI register) is set; power recycle is needed to restart again, that is transition to POWER OFF mode, OFF state and then restart.

Figure 29. SYS boost state control diagram



6.2 ER boost regulator

ER boost regulator is a DC-DC boost converter with integrated LS driver and switching frequency in the range of 2 MHz whose main function is to provide power to charge the energy reserve tank capacitor (that is ER capacitor), up to a 24 V/33 V selectable nominal voltage value ($V_{O\_ERBST\_L}$/$V_{O\_ERBST\_H}$); [end] [DOS_UR7S_0302001]voltage selection is done using PWR_CTRL_0 global SPI register, ERBST_V_SEL bit (default configuration is 33 V). Additionally, ER boost output is used to supply the safing FET regulator circuit.

Regulator circuit involves 3 pins:

- ERBST: boost regulation output
- ERBSTSW: boost switching node, connecting to the integrated LS driver stage
- BSTGND: LS driver power ground (shared with SYS boost)

There is no internal connection path between ERBST pin and the ER capacitor pin (VER) inside the device, that is actual connection is obtained by enabling ER charge switch circuit as well.

ER boost circuit is enabled using PWR_CTRL_0 global SPI register, ERBST_EN bit; enable request is accepted only when device is in either ACTIVE mode or PASSIVE mode-ER state, that is regulator cannot be enabled in PASSIVE mode-SHUTDOWN state. Additionally, as ER boost is cascaded to SYS boost in standard application scenario, an undervoltage lockout function is provided, disabling regulator operation if SYSBST voltage is lower than V_{UV_SYSBST} threshold. As regulator is enabled, actual switching operation starts as soon as ERBST node voltage is charged up to V_{SYSBST} - $V_{ERBST\_CHG\_DIS}$, ensuring that the external diode connected between SYSBST and ERBST, thus the ERBST pin is not open.

Every time ER boost regulator is enabled, soft start is performed by applying a ramp on LS over current threshold $I_{OC\_ERBSTSW}$, that is within t_{SOFTST_ERBST} time, $I_{OC\_ERBSTSW}$ value is increased from 40% to 100% with 16 steps.

As ER capacitor charging phase is started and VER/ERBST pin voltage has still not reached $V_{O\_ERBST\_L}$/$V_{O\_ERBST\_H}$ value, boost control strategy acts on switching duty cycle in order to limit the peak inductor current; this limitation is performed through the ERBSTSW LS overcurrent detection circuit ($I_{OC\_ERBSTSW}$) and allows to keep ER capacitor charge current within the desired range. As nominal voltage regulation value is reached, charge phase is completed and control acts to ensure nominal voltage regulation.

In order to achieve a good trade-off between EME and efficiency, ERBSTSW transition times can be configured between “slow” and “fast” in these conditions:

- Slow mode if device is in ACTIVE mode and $V_{VIN} > V_{VIN\_FASTSLOPE\_H}$
- Fast mode if device is either in PASSIVE mode or device is in ACTIVE mode and $V_{VIN} < V_{VIN\_FASTSLOPE\_L}$

$V_{O\_ERBST\_L}$/$V_{O\_ERBST\_H}$ regulation voltage output is guaranteed if both SYSBST voltage is the $V_{SYSBST\_ERBST\_LINEAR}$ range and regulator output current is in I_{O_ERBST} range, that is regulator linear operation; in this condition, control circuit ensures that both subharmonic generation and burst mode are avoided. Switching frequency can be tuned using PWR_CTRL_1 global SPI register, SWREG_F_SEL bit; 2 options are available:

- SWREG_F_SEL = 0 (default): $f_{SW\_ERSBST\_1}$ = 2 MHz typical value
- SWREG_F_SEL = 1: $f_{SW\_ERBST\_2}$ = 2.13 MHz typical value

If SYSBST voltage increases and goes outside $V_{SYSBST\_ERBST\_LINEAR}$ range and output current goes below I_{O_ERBST} range, switching duty-cycle is reduced to the minimum value and the control circuit raises pulse_skip signal, that is switching operation is stopped to keep ERBST voltage within its nominal operation range. After pulse_skip = 1 for a time longer than $t_{PLS\_SKIP\_ERBST\_FLT}$ ER boost enters in ER BST PULSE SKIP state and the operation is then recovered in either of the 2 following cases:

- After $t_{SKP\_ERBST\_BLKx}$ time and with pulse_skip = 0, in case of NVM_ERBOOST_PLS_SKIP_DIS = ’0’. The blanking time $t_{SKP\_ERBST\_BLKx}$ can be 100us or 50 us according to NVM_ERBOOST_PLS_SKIP_BLK_SEL configured by NVM; while blanking time can be totally disable setting NVM_ERBOOST_PLS_SKIP_DIS = ’1’ by NVM. In this case, the pulse skip is handled only inside the regulator, so the ER_BST_PLS_SKIP bit is not set.
- ERBST voltage goes below $V_{UV\_ERBST\_L}$/$V_{UV\_ERBST\_H}$ undervoltage threshold value for a time longer than $t_{UV\_ERBST\_FLT}$.

If ERBST voltage goes above $V_{OV\_ERBST\_L}$/$V_{OV\_ERBST\_H}$ overvoltage threshold for a time longer than $t_{OV\_ERBST\_FLT}$, ER boost regulator is disabled and ERBST_OV bit (PWR_STATUS_0 global SPI register) is set. ER boost operation is then recovered in either of the 2 following cases:

- Pulse_skip goes back to 0 logic level and ER voltage goes again below $V_{OV\_ERBST\_L}$/$V_{OV\_ERBST\_H}$ for a time longer than $t_{OV\_ERBST\_BLK}$
- ERBST voltage goes below $V_{UV\_ERBST\_L}$/$V_{UV\_ERBST\_H}$ undervoltage threshold value for a time longer than $t_{UV\_ERBST\_FLT}$

In both cases, in case overvoltage had happened, ERBST_OV bit is cleared upon SPI reading, after overvoltage has disappeared.

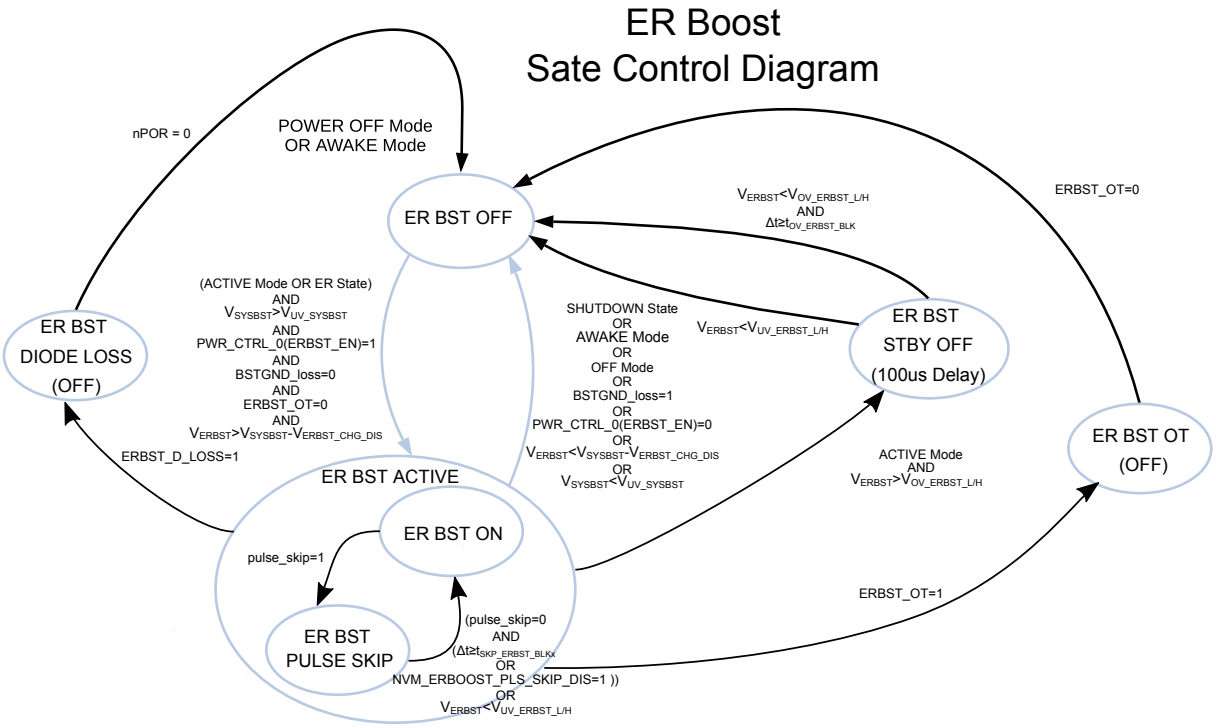
The following diagnostic and protection features are provided as well:

- Undervoltage detection: as ERBST pin voltage goes below $V_{UV\_ERBST\_H}$/$V_{UV\_ERBST\_L}$ threshold value for a time longer than $t_{UV\_ERBST\_FLT}$, undervoltage is detected and ERBST_UV bit (PWR_STATUS_0 global SPI register) is set; bit is cleared upon SPI reading after fault has disappeared.
- BSTGND ground loss detection: shared with SYS boost, see Section 6.1 SYS boost regulator.
- Overtemperature detection: as LS driver temperature exceeds T_{OT_ERBST} (with hysteresis $T_{OT\_ERBST\_HYST}$) for a time longer than $t_{OT\_ERBST\_FLT}$, regulator is disabled; ERBST_OT bit (PWR_STATUS_0 global SPI register) is set. Regulator is reenabled once fault has disappeared and SPI bit is read and cleared.
- Diode loss detection and ERBSTSW pin voltage clamping: external diode loss failure is detected as $V_{ERBSTSW}$-V_{ERBST} voltage difference exceeds $V_{D\_LOSS\_TH\_ERBST}$ threshold; this event activates the voltage clamping circuit on ERBSTSW pin, limiting voltage value to $V_{CLAMP\_ERBSTSW}$. As 5 successive clamping events are counted, ER boost regulator is disabled permanently and ERBST_D_LOSS bit (GSW global SPI register) is set; power recycle is needed to restart again, that is transition to POWER OFF mode, OFF state and then restart.

The slope compensation of ER boost regulator can be configured through SPI field ERBOOST_SLOPE_SEL in CLK_CTRL based on the selected value of the mounted inductor. The suggested values are:

- 00 → 22 µH
- 01 → 33 µH
- 10 → 47-68 µH
- 11 → 100 µH

Figure 30. ER boost state control diagram



6.3 ER charge and discharge circuits

ER capacitor charge circuit consists of a SPI-controllable current-limited switch whose main purpose is to create a low-ohmic path between ER boost output and the ER capacitor during the charge phase. The integrated switch is connected between ERBST and ERCHSW pins. In standard application scenario, ERCHSW is then externally connected to the ER capacitor (that is VER device pin) either with a direct (short-circuit) connection or with an external resistor (R_{ERCHSW}). This resistor is mainly used as a sense component for capacitor diagnostic purposes: normally, resistor value has to be chosen in order not to limit the charge current. Additionally, switch limitation current value I_{LIM_ERCHSW} is set in order to be always higher than $I_{OC\_ERBSTSW}$, that is ER charge switch should not limit the current during ER capacitor charge phase. Note that current is limited only in the direction from ERBST to ERCHSW.

ER capacitor discharge circuit consists of a SPI-controllable overcurrent-protected switch whose main purpose is to create a low-ohmic path between the ER capacitor and ground during the discharge phase; the overcurrent protection function is performed through a voltage comparator, monitoring the switch V_{DS} voltage. The integrated switch is connected between ERDCHSW and AGND pins. In standard application scenario, ERDCHSW is then externally connected to the ER capacitor (that is VER device pin) with an external resistor ($R_{ERDCHSW}$), mainly used to define and limit the current during discharge phase. As a consequence, resistor value has to be chosen to determine the discharge current value and kept high enough in order not to trigger the overcurrent protection V_{DS} comparator.

ER charge and discharge circuits are controlled with ER_SW_CHG_DCHG_EN 2-bit field, located in PWR_CTRL_0 global SPI register. Field coding avoids concurrent activation of both charge and discharge paths:

- ER_SW_CHG_DCHG_EN=00: all switches off
- ER_SW_CHG_DCHG_EN=10: ER charge enable request
- ER_SW_CHG_DCHG_EN=11: ER discharge enable request

By the way, in order to avoid anomalous operation, enable request is accepted only in the following conditions:

- ER charge: device is in ACTIVE mode and ER cap diagnostic is not running; once ER cap diagnostic is finished, if ER_SW_CHG_DCHG_EN = 10, ER charge is reenabled automatically
- ER discharge: device is either in ACTIVE mode or in PASSIVE mode

Normally, ER_SW_CHG_DCHG_EN bits are set by the microcontroller, but they are automatically cleared (thus, both charge and discharge circuits are forced to disable state) at the following transitions:

- Upon entry into ER state
- Upon entry into DEP_ENABLED state, that is prior to deployment events (ER charge should be disabled to keep ERBST voltage separate from VER voltage, that is ERBST voltage can remain at its nominal value, while ER cap is being discharged)
- From ER state to WAKEUP LATCHED

After those transitions, ER_SW_CHG_DCHG_EN bits can be controlled by SPI. Additionally, if ER_SW_CHG_DCHG_EN = 11, as device enters in PASSIVE mode - SHUTDOWN state, ER discharge switch is kept enabled as long as possible, even after RESET_N has gone to '0', in order to discharge the ER capacitor as much as possible (that is, until discharge switch can be kept on, roughly down to nPOR = 0). It is mandatory to wait that SYSBST voltage is lower than V_{OV_SYSBST} before activating the ER discharge path, thus ensuring that ER cap voltage has decreased enough in order not have resistor overheating.

The following diagnostic and protection features are provided as well:

- ER charge switch overtemperature detection: as switch temperature exceeds T_{OT_ERCHSW} (with hysteresis $T_{OT\_ERCHSW\_HYST}$) for a time longer than $t_{OT\_ERCHSW\_FLT}$, switch is disabled; ERCHSW_OT bit (PWR_STATUS_0 global SPI register) is set. Switch is reenabled once fault has disappeared and SPI bit is read and cleared.
- ER discharge switch overvoltage: if ERDCHSW voltage exceeds $V_{LIM\_ERDCHSW}$ for a time longer then $t_{ERDCHSW\_FLT}$, switch is disabled; ERDCHSW_OC bit (PWR_STATUS_0 global SPI register) is set. Switch is reenabled once fault has disappeared and SPI bit is read and cleared.

Figure 31. ER charge state control diagram

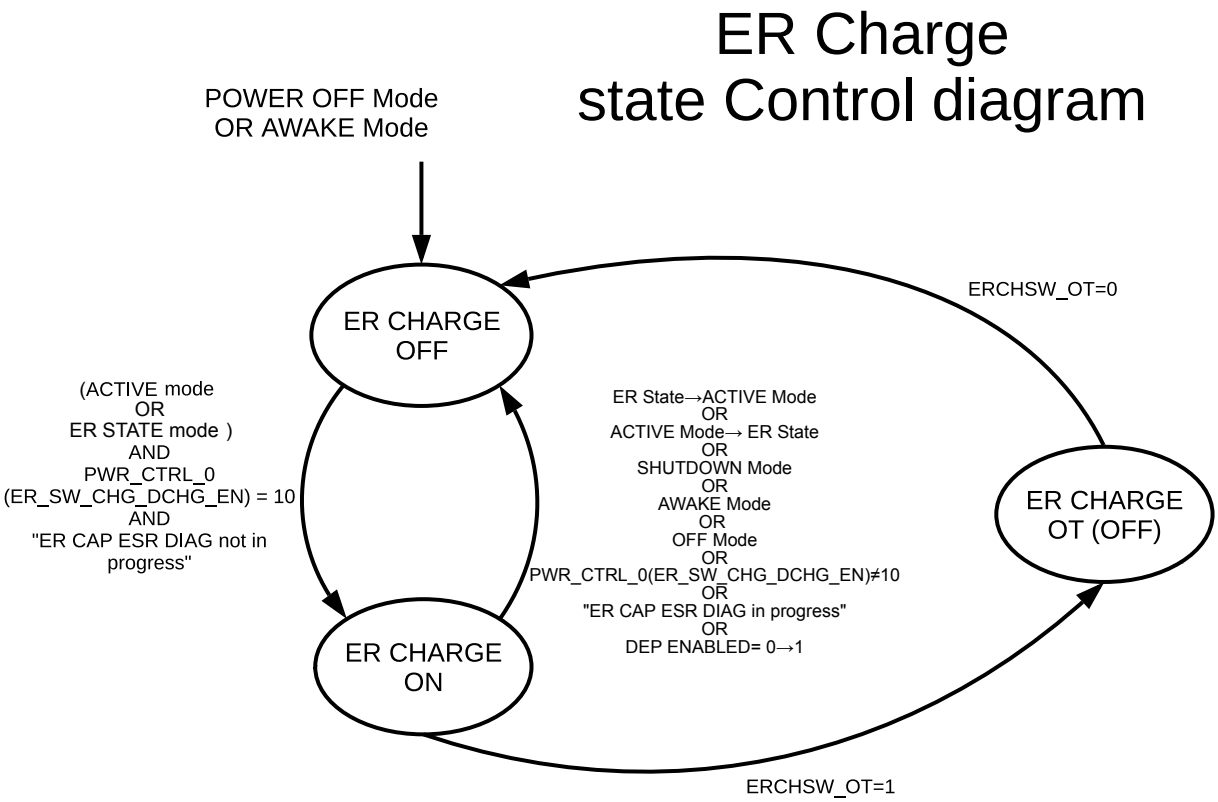
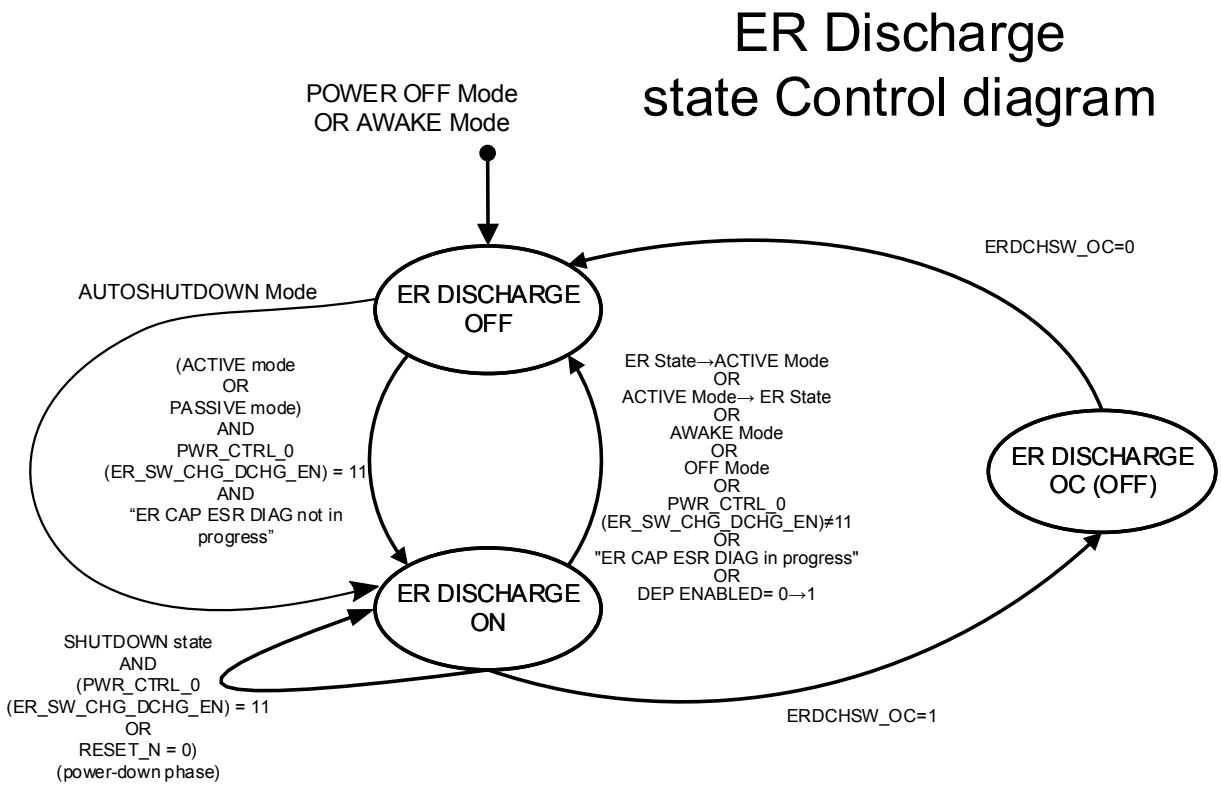


Figure 32. **ER discharge state control diagram**



6.4 ER switch and COVRACT digital input/output

ER switch circuit consists of a bidirectional switch whose main purpose is to create a low-ohmic path between the ER capacitor and the device main supply input (that is SYSBST pin), in order to provide power in case of loss of battery supply (autarchy/energy-reserve mode). The integrated switch is connected between VER and ERSW pins. In standard application scenario, ERSW is then externally connected to SYSBST pin with an external diode/ resistor network (R_{ERSW_FWD}, D_{ERSW_FWD}, R_{ERSW_REV}, D_{ERSW_REV}) in order to manage the opposite directions for the current:

- Forward path: current is flowing from VER to ERSW (autarchy/energy-reserve mode) and it is limited by the switch at the value I_{LIM_ERSW}.
- Reverse path: current is flowing from ERSW to VER for an eventual precharge of the ER capacitor and it is not limited internally by the switch; thus, current limitation for this direction, if necessary, relies on external resistor R_{ERSW_REV}.

When switch is disabled, back-to-back diode isolation between VER and ERSW is provided in order to avoid unwanted supply back feeding from the ER capacitor to SYSBST pin.

As a complementary function, COVRACT digital input/output pin allows to communicate ER switch activation status. As device is configured as master, COVRACT is automatically configured as output and its function is to indicate ER switch activation to the slave device and/or to an external module; in slave mode, COVRACT is automatically configured as input and it is used to activate the slave device ER switch as a high logic level is detected.

ER switch and COVRACT handling is managed either automatically by the device or via global SPI or by COVRACT pin. Here is a description of the different possible scenarios with respect to Master/Slave configuration and power supply control state machine modes:

- Master + PASSIVE mode: if device enters this mode, ER switch is automatically enabled; COVRACT output is set to high logic level.

- Master + ACTIVE mode: while in this mode, ER switch is normally disabled; however, it can be enabled via global SPI by ER_SW_CHG_DCHG_EN = 01 (PWR_CTRL_0 register), that is a direct request of ER switch enabling, normally used for fast precharge of ER capacitor voltage up to SYSBST during power-up phase (reverse path); COVRACT is kept to low logic level. Bit field coding avoids concurrent activation of ER switch and charge/discharge paths.
- Slave + ACTIVE mode: two scenarios are possible:
  - As COVRACT input is set to high logic level, device enters PASSIVE mode and ER switch is enabled if ER_SW_SLAVE_EN = 1 (default value) inside PWR_CTRL_0 register; if ER_SW_SLAVE_EN = 0, device remains in PASSIVE mode, but ER switch is kept disabled.
  - While COVRACT input is set to low logic level, slave ER switch is enabled via global SPI by ER_SW_CHG_DCHG_EN = 01 (PWR_CTRL_0 register) for fast precharge of a second optional ER capacitor.
- Slave + PASSIVE mode: as COVRACT input is set to low logic level, ER switch is disabled and device enters ACTIVE mode (otherwise it remains enabled).
- All other cases: ER switch is kept disabled and COVRACT output (master only) is kept disabled as well (COVRACT configured as input for the slave remains active).

ER switch is immediately disabled in case the voltage difference between VIN and VER voltages exceeds $V_{VIN\_VER\_DIFF\_TH}$ threshold in PASSIVE mode. This feature avoids that ER capacitor is kept charged by VIN through SYSBST pin and the ER switch, for example, ER capacitor voltage is discharged down to SYSBST voltage in PASSIVE mode. Therefore, this feature is not working, that is ER switch is not disabled, if it is enabled via global SPI by ER_SW_CHG_DCHG_EN = 01, because in this case it is normal to precharge the capacitor through SYSBST pin and the ER switch.

Additionally, ER switch is protected against overtemperature, that is as switch temperature exceeds T_{OT_ERSW} (with hysteresis $T_{OT\_ERSW\_HYST}$) for a time longer than $t_{OT\_ERSW\_FLT}$, overtemperature event is detected and ERSW_OT bit (PWR_STATUS_0 global SPI register) is set; bit is cleared upon SPI reading as fault has disappeared. If a deployment event is in progress, no further action is taken; otherwise, switch is immediately disabled. As soon as temperature recovers, switch is kept in off state for an additional $t_{OT\_ERSW\_BLK}$ blanking time, then automatic enable retry is performed. However, if a new deployment event is started during blanking time interval, ER switch is immediately reenabled without waiting blanking time counter expiration. Additionally, if temperature exceeds T_{OT_ERSW} again during blanking time interval, $t_{OT\_ERSW\_BLK}$ blanking time is reset.

Figure 33. **ER switch state control diagram - master device**

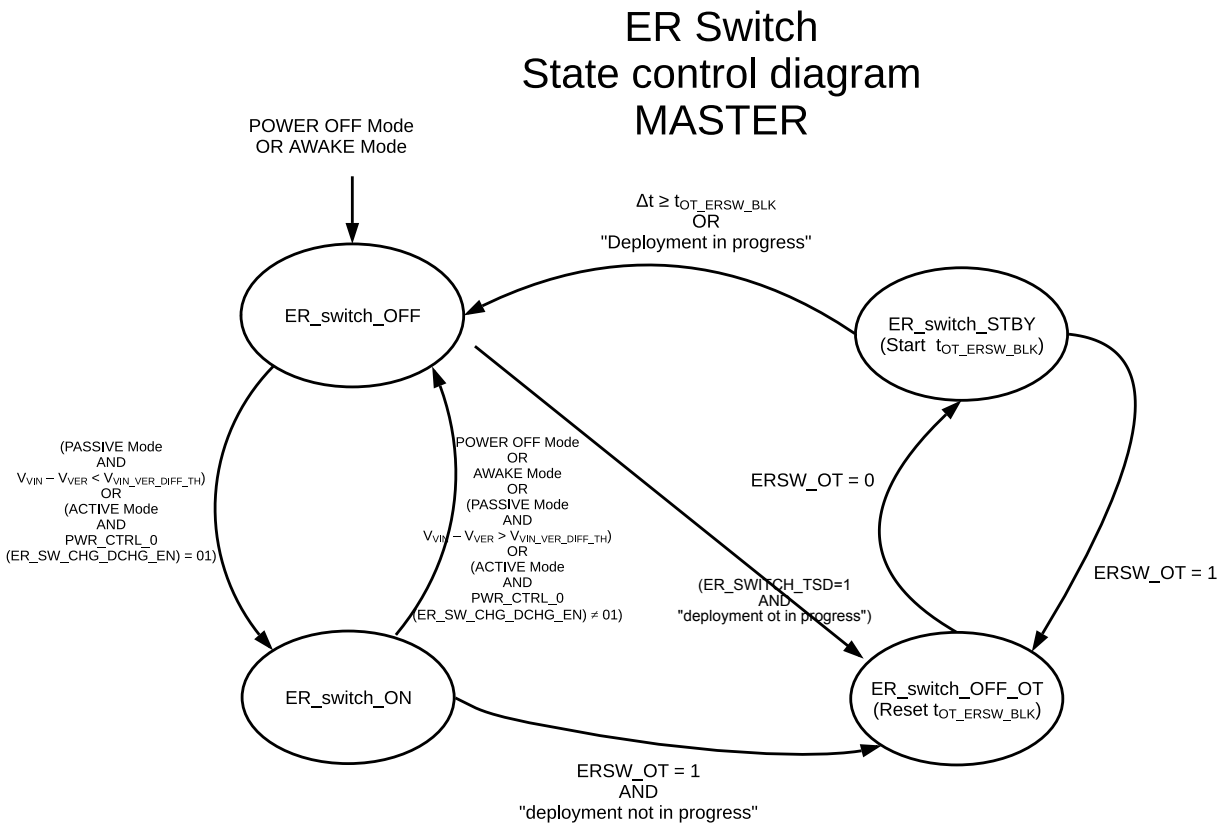
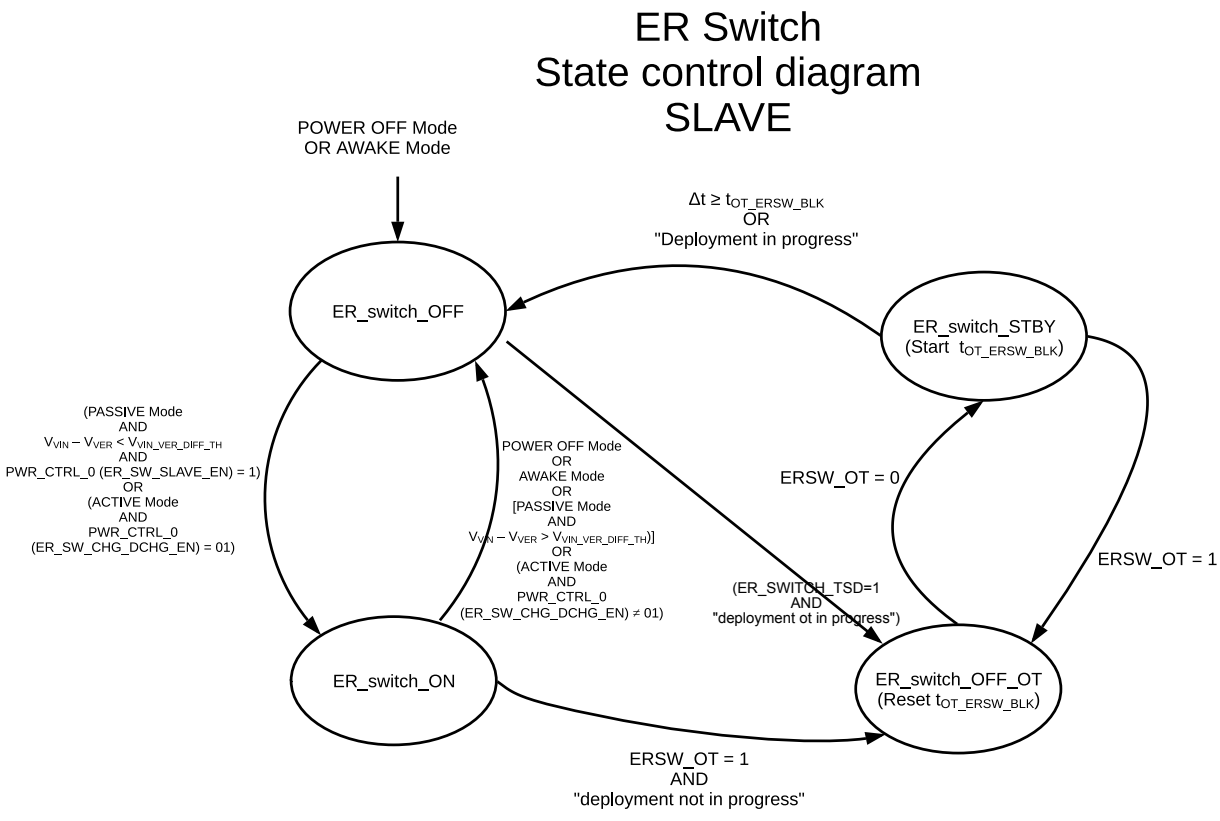


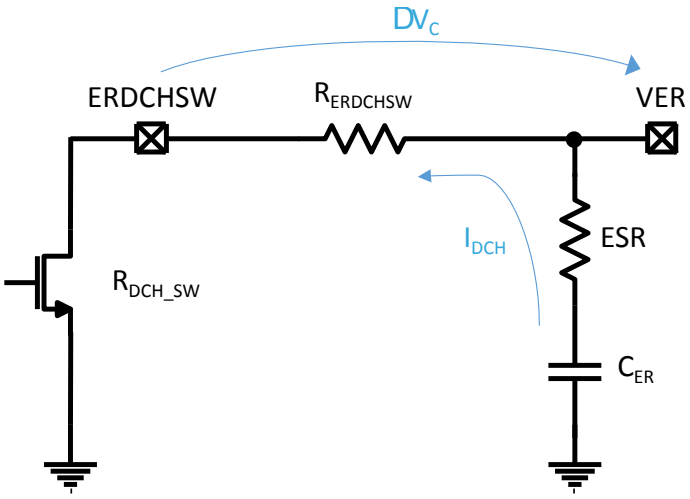
Figure 34. **ER switch state control diagram - slave device**



6.5 Energy reserve capacitor (ER cap) diagnostics

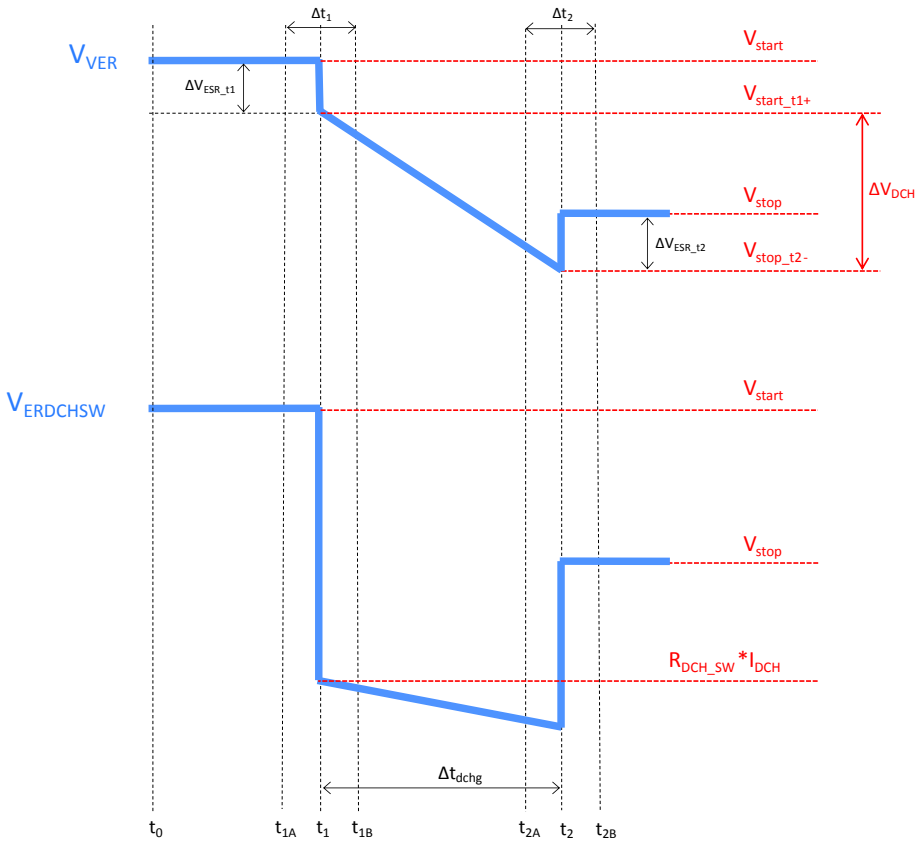
The energy reserve capacitor (ER cap) health is monitored by measuring its capacitance and ESR values. These two measurements can be done at the same time by activating the ER discharge switch and measuring the voltage drop on VER pin and current flowing in $R_{ERDCHSW}$.

Figure 35. ER cap discharge path



Referring to simplified schematic of Figure 35, typical V_{VER} and $V_{ERDCHSW}$ discharge profiles are shown in Figure 36.

Figure 36. ER cap discharge pins voltage profiles



In order to run the diagnostic, the microcontroller has to perform the following operations:

1. Request the diagnostic, by writing Reg ER_CAP_DIAG_CTRL[0] = 1 (ER_DIAG_START).
2. Depending on ER capacitor size, diagnostic time is different. A timeout for diagnostic duration can be set through register ER_DIAG_TIMEOUT:
   a. If the diagnostic exceeds the timeout, the process is halted and flag ERCAP_DIAG_END_FOR_TIMEOUT is set in register ER_CAP_DIAG_ESR_STATUS.
   b. If the diagnostic ends within the timeout, the device asserts bits NEWDATA for both measurements (ER_CAP_DIAG_ESR_STATUS[15] and ER_CAP_DIAG_CAP_STATUS[15]).
3. Write ER_DIS_MEAS_DELAY = 0 if V_{start_t1+} and V_{start} need to be delayed of 64us to reach the steady state after the ERDCHSW commutation. Write ER_DIS_MEAS_DELAY = 1 if no slew-rate limiting components are mounted.
4. Read results of C and ESR conversion in ER_CAP_DIAG_CAP_STATUS_0[13:0] and ER_CAP_DIAG_ESR_STATUS[12:0] bit fields.
5. Calculate C and ESR, knowing $R_{ERDCHSW}$ value, as follows:

$$C = ER\_CAP\_DIAG\_CAP\_STATUS\_0\left[13:0\right] \times LSB_C \times \frac{1}{R_{ERDCHSW}} \quad (1)$$

$$ESR = ER\_CAP\_DIAG\_ESR\_STATUS\_0\left[12:0\right] \times LSB_{ESR} \times R_{ERDCHSW} \quad (2)$$

Once diagnostic process is started, it can be forced to a halt by the microcontroller by writing Reg ER_CAP_DIAG_CTRL[0] = 0.

Once a request is over, to proceed with a new one the ER_CAP_DIAG_CTRL[0] (ER_DIAG_START) bit has to be written first to 0 and then to 1.

6.6 SAT buck regulator

Satellite buck regulator is a DC-DC synchronous rectifier buck converter with integrated HS and LS drivers and switching frequency in the range of 2 MHz whose main function is to provide power to the remote sensor satellite unit (that is RSU), compatible with PSI-5 standard. Regulation voltage can be configured as either 6.5 V or 8 V ($V_{O\_SATBCK\_L}$/$V_{O\_SATBCK\_H}$) via NVM programming, default configuration is 8 V. Additionally, SAT buck output is used as supply line input for both VCC buck and the internal low voltage regulators, providing supply to all the analog and digital circuitry.

Regulator circuit involves 3 pins:

- SATBCK: buck regulation output
- SATBCKSW: buck switching node, connecting to the integrated LS/HS driver stage
- SATBCKGND: LS driver power ground (dedicated)

SAT buck is powered from the to SYS boost output by internal metal connection; however, there is no internal connection path between SATBCK pin and the RSU circuits inside the device, that is external connection between SATBCK and RSU_SUP_FLT pins must be provided on the ECU.

Regulator circuit is enabled at power-up, as soon as SYSBST pin voltage goes above V_{UV_SYSBST} value; soft start, that is transition from 10% to 90% of regulation value within t_{SOFTST_SATBCK} time is performed every time that regulator moves from disabled to enabled state. In order to prevent anomalous supply operation, regulator is immediately disabled as overvoltage event is detected on VCCBCK pin, when VCC regulator is not configurated as FDM.

In order to achieve a good trade-off between EME and efficiency, SATBCKSW transition times can be configured between “slow” and “fast” in these conditions:

- Slow mode if device is in ACTIVE mode and $V_{VIN} > V_{VIN\_FASTSLOPE\_H}$ and $V_{SYSBST} < V_{SYSBST\_FASTSLOPE\_L}$
- Fast mode if device is either in PASSIVE mode or device is in ACTIVE mode and $V_{VIN} < V_{VIN\_FASTSLOPE\_L}$ or $V_{SYSBST} > V_{SYSBST\_FASTSLOPE\_H}$

The fast mode can be forced in all condition with the SATBCK_FORCE_F_SLOPE bit.

The SATBCK is not turned OFF with V_{UV_SYSBST} and it can work at 100% duty cycle to have the minimum drop possible on SATBCK pin when the ER cap is discharged in PASSIVE mode.

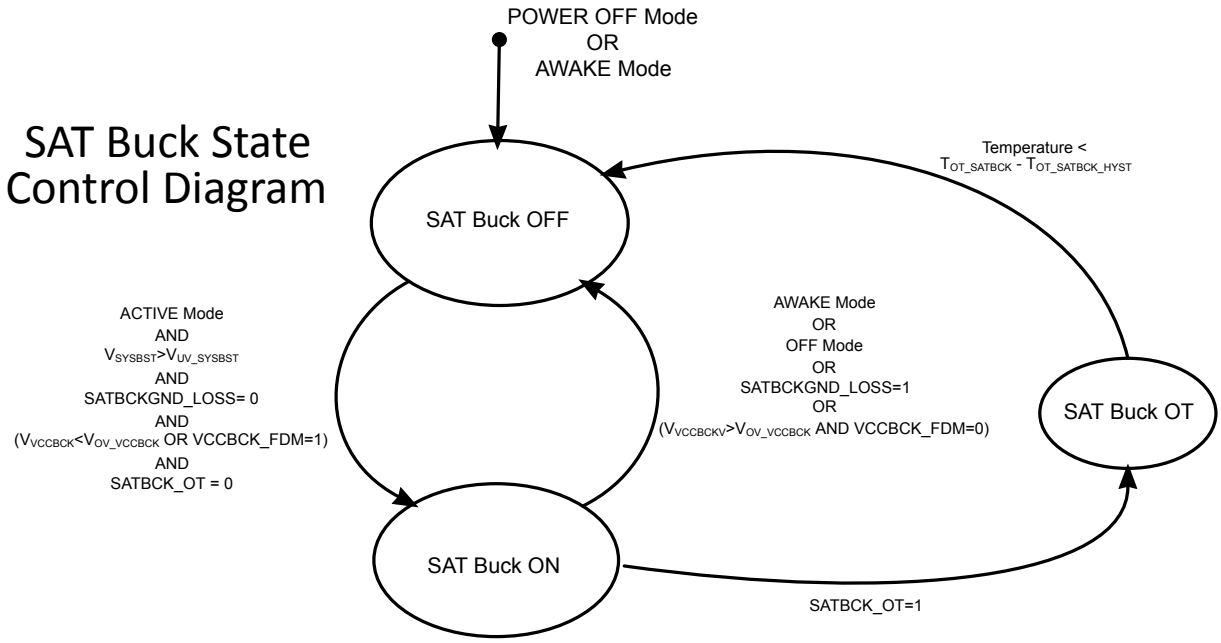
Control circuitry ensures absence of subharmonic generation; switching frequency can be tuned using PWR_CTRL_1 global SPI register, SWREG_F_SEL bit; 2 options are available:

- SWREG_F_SEL = 0 (default): $f_{SW\_SATBCK\_1}$ = 2 MHz typical value
- SWREG_F_SEL = 1: $f_{SW\_SATBCK\_2}$ = 2.13 MHz typical value

The following diagnostic and protection features are provided as well:

- Undervoltage detection: as SATBCK pin voltage goes below $V_{UV\_SATBCK\_L}$/$V_{UV\_SATBCK\_H}$ threshold value for a time longer than $t_{UV\_SATBCK\_FLT}$, undervoltage is detected and SATBCK_UV bit (PWR_STATUS_1 global SPI register) is set; bit is cleared upon SPI reading after fault has disappeared.
- SATBCKGND ground loss detection: as $V_{SATBCKGND}$ - $V_{SUBGNDx}$ exceeds $V_{SATBCKGND\_LOSS\_TH}$ for a time longer than $t_{SATBCKGND\_LOSS\_FLT}$, regulator is disabled and automatically reenabled once ground connection is restored. Ground loss detection is available even when drivers are off, as a pullup current generator $I_{PU\_SATBCKGND}$ is always connected to SATBCKGND; detection in disabled state does not allow SAT buck enabling. As detection occurs, SATBCKGND_LOSS bit (PWR_STATUS_1 global SPI register) is set; bit is cleared upon SPI reading as fault has disappeared.
- Over temperature detection: as HS/LS driver temperature exceeds TOT_SATBCK (with hysteresis TOT_SATBCK_HYST) for a time longer than tOT_SATBCK_FLT, regulator is disabled; SATBCK_OT bit (PWR_STATUS_1 global SPI register) is set. Once fault has disappeared, regulator is automatically reenabled, while status bit is cleared after SPI reading.
- Over-current on HS power MOS during the high PWM phase, if the output current from SATBCKSW exceeds the IOC_HS_SATBCKSW, the HS is turned off until the next switching period and the LS power MOS is turned on.
- Over-current on LS power MOS during the low PWM phase, if the output current from SATBCKSW exceeds the $I_{OC\_LS\_SRC\_SATBCKSW}$, the next switching period HS power MOS is kept disabled to reduce the current flowing through the inductor.
- During the low PWM phase also the current flowing into SATBCKSW pin is monitored, if the current is higher than $I_{OC\_LS\_SNK\_SATBCKSW}$, the LS power MOS is turned off until the next PWM falling edge.

Figure 37. SAT buck state control diagram



6.7 VCC buck regulator

VCC buck regulator is a DC-DC synchronous rectifier buck converter with integrated HS and LS drivers and switching frequency in the range of 2 MHz whose main function is to provide power to the ECU microcontroller core and I/Os. Regulation voltage nominal value is set to 3.3 V (V_{O_VCCBCK}). Additionally, VCC buck output is internally used as supply line for the device digital I/Os and provides low voltage supply to the device digital circuitry after power-up sequence is completed.

Regulator circuit involves 3 pins:

- VCCBCK: buck regulation output
- VCCBCKSW: buck switching node, connecting to the integrated LS/HS driver stage
- VCCBCKGND: LS driver power ground (dedicated)

As VCC buck is powered from the SAT buck output by internal metal connection, regulator is enabled and starts ramp-up phase as soon as SATBCK pin voltage goes above $V_{UV\_SATBCK\_H/L}$ value; a ramp-up phase duration timer is started as well, with t_{RU_VCCBCK} expiration time. Regulator soft start, that is transition from 10% to 90% of regulation value within t_{SOFTST_VCCBCK} time, is performed every time that regulator moves from disabled to enabled state.

As soft start is beginning, an open feedback diagnostic procedure is performed in order to prevent load damage due to anomalous feedback connection failures; at first, $I_{PU\_OF\_VCCBCK}$ pullup current generator is connected to VCCBCK pin and overvoltage monitoring circuit becomes active, in this state the digital IOs pull-ups and pull-downs are disabled. Until ramp-up phase duration timer expires, as VCCBCK voltage goes above V_{OV_VCCBCK} overvoltage threshold for a time longer than $t_{OV\_VCCBCK\_RU\_FLT}$, open feedback is detected, regulator is immediately disabled and is kept in this state for $t_{DIS\_VCCBCK\_BLK}$ blanking time, then an automatic start retry is performed.

During ramp-up phase, VCCBCK undervoltage monitoring becomes active as well in order to determine if regulator is starting-up correctly; two undervoltage thresholds, that is $V_{UV\_H\_VCCBCK}$ high threshold and $V_{UV\_L\_VCCBCK}$ low threshold, are provided, with the same filter time duration $t_{UV\_VCCBCK\_FLT}$. If both undervoltage monitors do not show any detection as ramp-up phase timer expires, ramp-up phase ends and regulator enter normal operation phase; otherwise, regulator is immediately disabled and kept in this state for $t_{DIS\_VCCBCK\_BLK}$ blanking time, then an automatic start retry is performed.

In order to achieve a good trade-off between EME and efficiency, VCCBCKSW transition times can be configured between “slow” and “fast” in these conditions:

- Slow mode if device is in ACTIVE mode and $V_{VIN} > V_{VIN\_FASTSLOPE\_H}$
- Fast mode if device is either in PASSIVE mode or device is in ACTIVE mode and $V_{VIN} < V_{VIN\_FASTSLOPE\_L}$

The fast mode can be forced in all condition with the VCCBCK_FORCE_F_SLOPE bit.

In normal operation phase, control circuitry ensures absence of subharmonic generation; switching frequency can be tuned using PWR_CTRL_1 global SPI register, SWREG_F_SEL bit; 2 options are available:

- SWREG_F_SEL =0 (default): $f_{SW\_SATBCK\_1}$ = 2 MHz typical value
- SWREG_F_SEL = 1: $f_{SW\_SATBCK\_2}$ = 2.13 MHz typical value

The following diagnostic and protection features are provided as well:

- Undervoltage detection in normal operation phase, low threshold: as VCCBCK pin voltage goes below $V_{UV\_L\_VCCBCK}$ threshold value for a time longer than $t_{UV\_VCCBCK\_FLT}$, low undervoltage status is detected and VCCBCK_UVL bit (PWR_STATUS_1 global SPI register) is set; bit is cleared upon SPI reading as fault has disappeared. Regulator is immediately disabled and kept in this state for $t_{DIS\_VCCBCK\_BLK}$ blanking time, then an automatic start retry is performed.
- Undervoltage detection in normal operation phase, high threshold: as VCCBCK pin voltage goes below $V_{UV\_H\_VCCBCK}$ threshold value for a time longer than $t_{UV\_VCCBCK\_FLT}$, high undervoltage status is detected and VCCBCK_UVH bit (PWR_STATUS_1 global SPI register) is set; bit is cleared upon SPI reading as fault has disappeared. No action is taken on regulator operation.
- Overvoltage detection in normal operation phase: as VCCBCK pin voltage goes above V_{OV_VCCBCK} threshold value for a time longer than $t_{OV\_VCCBCK\_FLT}$, overvoltage is detected and VCCBCK_OV bit (PWR_STATUS_1 global SPI register) is set; bit is cleared upon SPI reading as fault has disappeared. Regulator is immediately disabled and kept in this state for $t_{DIS\_VCCBCK\_BLK}$ blanking time, then an automatic start retry is performed (in case of overvoltage on VCCBCK, SAT buck regulator is disabled too).

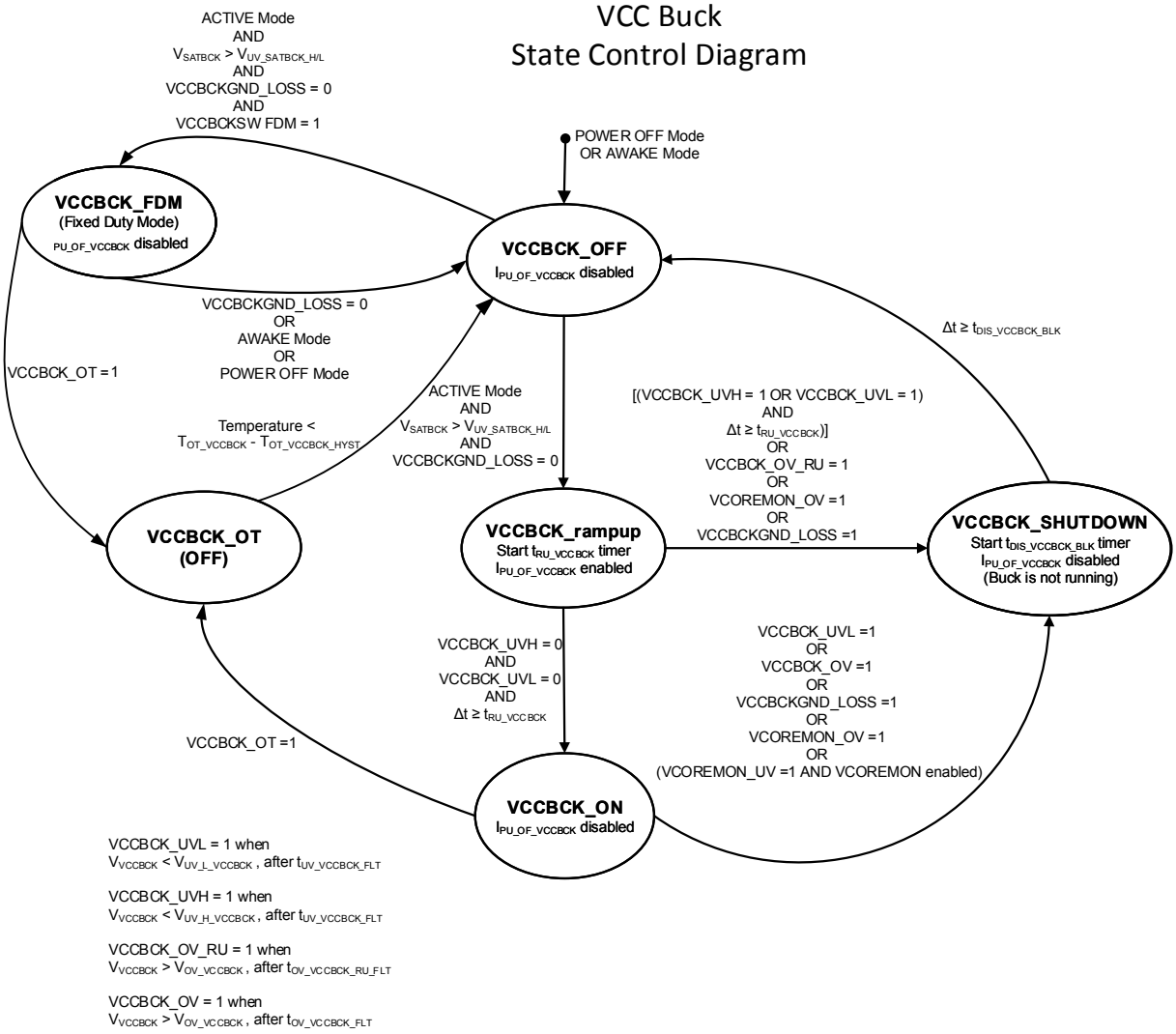
- VCCBCKGND ground loss detection: as $V_{VCCBCKGND}$-$V_{SUBGNDx}$ exceeds $V_{VCCBCKGND\_LOSS\_TH}$ for a time longer than $t_{VCCBCKGND\_LOSS\_FLT}$, ground loss failure is detected. Ground loss detection is available even when drivers are off, as a pullup current generator $I_{PU\_VCCBCKGND}$ is always connected to VCCBCKGND; a detection in disable state does not allow regulator to start ramp-up phase. If detection occurs during either ramp-up or in normal operation phase, regulator is immediately disabled and kept in this state for $t_{DIS\_VCCBCK\_BLK}$ blanking time, then restart is automatically performed once the fault has disappeared. As detection occurs, VCCBCKGND_LOSS bit (PWR_STATUS_1 global SPI register) is set; bit is cleared upon SPI reading as fault has disappeared.
- Overtemperature detection: as HS/LS driver temperature exceeds T_{OT_VCCBCK} (with hysteresis $T_{OT\_VCCBCK\_HYST}$) for a time longer than $t_{OT\_VCCBCK\_FLT}$, regulator is disabled; VCCBCK_OT bit (PWR_STATUS_1 global SPI register) is set. Once fault has disappeared, regulator is automatically reenabled, while status bit is cleared after SPI reading.
- Over-current on HS power MOS during the high PWM phase, if the output current from VCCBCKSW exceeds the $I_{OC\_HS\_VCCBCKSW}$, the HS is turned off until the next switching period and the LS power MOS is turned on.
- Over-current on LS power MOS during the low PWM phase, if the output current from SATBCKSW exceeds the $I_{OC\_LS\_SRC\_VCCBCKSW}$, the next switching period HS power MOS is kept disabled to reduce the current flowing through the inductor.
- During the low PWM phase also the current flowing into VCCCKSW pin is monitored, if the current is higher than $I_{OC\_LS\_SNK\_VCCBCKSW}$, the LS power MOS is turned off until the next PWM falling edge.

VCCBCKSW switching output provides an alternative usage mode, that is fixed duty mode (FDM), that allows to use VCCBCKSW pin as a LS/HS driver operating at a fixed 50% DC ($DC_{FDM\_VCCBCKSW}$); this mode is useful in application scenarios in which VCC buck is not used, thus driver circuit can be reused to drive an external custom circuit, for example a simple SATBCK voltage doubler for VSYNC input supply. Consequently, VCCBCK pin has to be supplied externally to guarantee correct functionality of device I/Os and internal regulators.

VCCBCKSW FDM is configured via NVM programming; default configuration is normal buck operation mode (FDM disabled). As happens in buck operation mode, driver is enabled as soon as SATBCK pin voltage goes above V_{UV_SATBCK}.

VCCBCK overvoltage and undervoltage monitorings do not influence FDM operation; however, as VCCBCKGND loss failure is detected, VCCBCKSW drivers are immediately disabled and automatically reenabled once ground connection is restored. Ground loss detection is available even when drivers are off, not allowing driver operation to start. As detection occurs, VCCBCKGND_LOSS bit (PWR_STATUS_1 global SPI register) is set; bit is cleared upon SPI reading as fault has disappeared.

Figure 38. **VCC buck state control diagram**



6.8 Microcontroller core voltage monitor (VCOREMON)

In specific application scenarios, an additional external regulator is cascaded to VCC buck in order to provide power to the microcontroller core circuit, providing a 1.2 V nominal output voltage. The current value of the core voltage regulator can be monitored using the VCOREMON functionality whose main purpose is to detect if either undervoltage or overvoltage events are occurring and react by disabling VCC buck regulator. VCOREMON functionality is enabled/disabled via NVM programming, default configuration is VCOREMON disabled.

VCOREMON circuit consists of the following elements:

- VCOREMON input pin, to be externally connected to the core regulator output; pin is provided with and internal pulldown resistor $R_{PD\_VCOREMON}$, that allow to detect open connection failures
- Overvoltage comparator, with $V_{OV\_VCOREMON}$ voltage threshold and a deglitch filter equal to $t_{OV\_VCOREMON\_FLT}$
- Undervoltage comparator, with $V_{UV\_VCOREMON}$ voltage threshold and a deglitch filter equal to $t_{UV\_VCOREMON\_FLT}$

VCOREMON overvoltage monitoring is activated as VCC buck regulator enters ramp-up phase; if overvoltage event is detected, VCC buck regulator is immediately disabled. VCOREMON_OV bit (PWR_STATUS_1 global SPI register) is set accordingly; bit is cleared upon SPI reading as fault has disappeared. VCC buck is kept disabled for $t_{DIS\_VCCBCK\_BLK}$ blanking time, then restart is retried.

As VCC buck enters normal operation mode (VCCBCK_ON state, see Figure 38), both VCOREMON overvoltage and undervoltage monitorings become active; if failure is detected, VCC buck is immediately disabled. VCOREMON_OV and VCOREMON_UV bits (PWR_STATUS_1 global SPI register) are set accordingly; bits are cleared upon SPI reading as fault has disappeared. VCC buck is kept disabled for $t_{DIS\_VCCBCK\_BLK}$ blanking time, then restart is tried.

In case both VCCBCKSW FDM and VCOREMON functionality are enabled, both VCOREMON overvoltage and undervoltage monitorings do not influence FDM operation.

6.9 V5 linear regulator

V5 regulator is a linear voltage regulator circuit whose main function is to provide power to external ECU modules (for example CAN interface), providing an output voltage nominal value equal to 5V ($V_{O\_V5\_SENSE}$); regulation circuit relies on an external PNP discrete transistor as power element. V5 regulator is not mandatory in some application scenarios, so PNP component could be not mounted on the ECU: to deal with this, the regulator can be kept disabled through SPI programming, by setting bit V5_REG_EN = 0 (default value) inside PWR_CTRL_0 register.

Regulator circuit involves 2 pins:

- V5_DRV: PNP base driving output
- V5_SENSE: regulation node, PNP collector sense feedback input

V5 regulator analog circuit is internally supplied by SATBCK regulator; in a standard application scenario, the PNP emitter is connected to SATBCK line as well, that is SAT buck is the supply line input for V5 regulator.

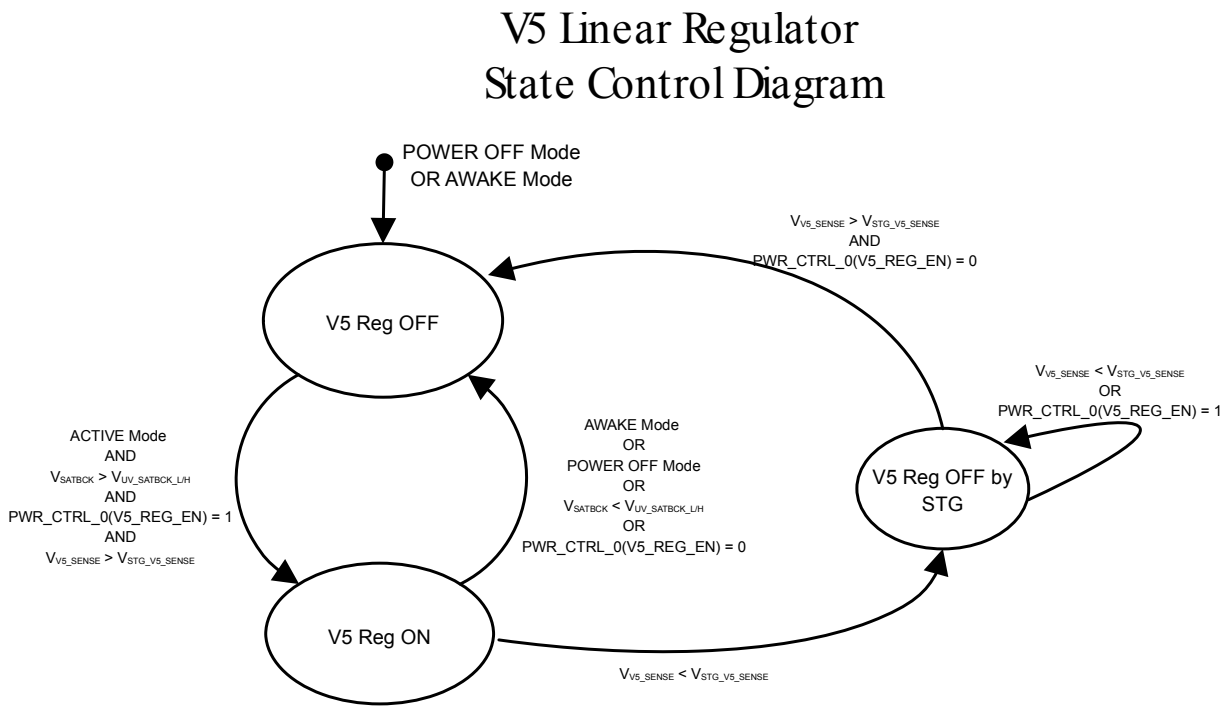
To limit current in case of PNP base shorted to PNP collector, an external resistor can be placed in series to PNP emitter. Maximum value to avoid PNP saturation must be 11 Ω when SATBCK voltage is set to 8 V, 3.7 Ω when SATBK voltage is set to 6.5 V.

If V5_REG_EN = 1, regulator is enabled and starts ramp-up phase as soon as SATBCK pin voltage goes above $V_{UV\_SATBCK\_L}$/$V_{UV\_SATBCK\_H}$ value; every time that regulator is enabled, soft start is applied that is transition from 10% to 90% of regulation value within $t_{SOFTST\_V5\_SENSE}$.

The following diagnostic and protection features are provided as well:

- Sinking current limit on V5_DRV pin ($I_{LIM\_V5\_DRV}$)
- Pullup resistance between V5_DRV and SATBCK pins ($R_{PU\_V5\_DRV}$), acting as both passive turn-off for PNP emitter-base voltage and sourcing current limitation on V5_DRV pin.
- Short to ground detection on V5_SENSE pin: as V5_SENSE pin voltage goes below $V_{STG\_V5\_SENSE}$ threshold value for a time longer than $t_{STG\_V5\_SENSE\_FLT}$, short to ground status is detected, V5_SENSE_STG bit (global SPI register) is set and regulator is disabled; SPI V5_REG_EN read returns 0, but in order to reenable the regulator, SPI V5_REG_EN bit must be written to 0 and then to 1.
- Overvoltage detection on V5_SENSE pin: as V5_SENSE pin voltage goes above $V_{OV\_V5\_SENSE}$ threshold value (with hysteresis $V_{OV\_V5\_SENSE\_HYST}$) for a time longer than $t_{OV\_V5\_SENSE\_FLT}$, overvoltage is detected and V5_SENSE_OV bit (PWR_STATUS_1 global SPI register) is set; bit is cleared upon SPI reading as fault has disappeared. No action is taken on regulator operation.
- Undervoltage detection on V5_SENSE pin: as V5_SENSE pin voltage goes below $V_{UV\_V5\_SENSE}$ threshold value (with hysteresis $V_{UV\_V5\_SENSE\_HYST}$) for a time longer than $t_{UV\_V5\_SENSE\_FLT}$, undervoltage is detected and V5_SENSE_UV bit (PWR_STATUS_1 global SPI register) is set; bit is cleared upon SPI reading as fault has disappeared. No action is taken on regulator operation.
- Pullup current generator on V5_SENSE pin up to SATBCK ($I_{PU\_OF\_V5\_SENSE}$), used to trigger an overvoltage detection in case of V5_SENSE open feedback failure.

Figure 39. **V5 linear reg state control diagram**



7 Safing FET regulator and diagnostics

7.1 Regulator and control logic

The HS safing FET regulator circuit (VSFx regulator) provides capability to regulate LEA/squib deployment loop supply voltage through an external nch MOS safing FET. Regulation accuracy is guaranteed by direct sensing of safing FET source voltage with a dedicated pin. Transient performance allows to guarantee regulation stability with up to a maximum of 16 parallel deployment events with high or low current profile as well as under diagnostic load conditions. In order to guarantee stability of the VSFx regulator a minimum load current I_{LOAD_MIN} connected on the source of the external safing FET is required; a minimum capacitive load of a single C_{SSx}/C_{SSxy} capacitor is needed too (see Figure 40 for reference), especially in the scenario in which the regulator is used to supply a single deployment loop. For each device, two VSFx regulators are provided (VSF0 and VSF1), with fully isolated regulator loops and enabling circuits. A simplified overview of a fully populated dual VSFx regulator circuit is shown in Figure 25.

Safing FET source voltage is sensed with VSFx_S pin as feedback input, used also as regulator circuit floating supply line; VSFx_G pin provides the required FET V_{GS} driving capability, thus allowing the regulator loop to regulate $V_{REG\_VSF\_S}$ voltage on VSFx_S pin.

Connection between safing FET source and deployment loop supply pins (SSx/SSxy) must be provided externally to the device, that is no device internal supply path is present; depending on the application scenario, this connection can be realized either by directly (short) or through a channel decoupling diode (D_{SSxy}). Usage of R_{VSF_S} series resistance is suggested in order to avoid high current back-feeding to deployment supply pins in case of internal short on VSFx_S pin to high voltage (for example ERBST).

Safing FET drain supply line (that is the diode-OR between battery and energy reserve cap lines) is connected to the device as well through VSF_D pin for diagnostic purposes. Even if both VSFx regulators are used, only one VSF_D pin is available.

VSFx regulator is internally supplied by ERBST, that is energy reserve boost regulator; in order to guarantee the expected regulation voltage and accuracy:

- ERBST regulator must be enabled with PWR_CTRL_0 global SPI register, ERBST_EN bit set to 1. By the way, as device enters ER state, the IC is supplied directly from the ER capacitor; as the ER capacitor discharges, SYSBST pin voltage could eventually reach its UV threshold, triggering a forced turn-off of the ER boost regulator.
- A minimum dropout voltage $V_{DO\_VSF\_G}$ is needed between ERBST and VSFx_G pins. As described before, as device enters ER state, a forced turn-off of the ER boost regulator could be triggered, as the ER capacitor discharges through the SYSBST pin current: thus, ERBST pin voltage starts to discharge too and reach values that will not allow to guarantee the minimum required dropout voltage.

VSFx_G regulator driving output is provided with a sourcing current limitation ($I_{LIM\_VSF\_G}$) and a voltage clamping circuit (with $V_{VSF\_G\_CLAMP}$ clamping voltage) that limits VSFx_G maximum voltage in case of open-loop conditions; this may occur in case of:

- Regulator enabling while VSFx_G pin is still not connected to safing FET gate: this happens because a redundant external FET enable circuitry is normally present, enabling/disabling VSFx_G to safing FET gate connection.
- Open feedback fault (for example, VSFx_S not properly connected).

The external FET operates in voltage follower mode when an open feedback fault occurs while redundant external FET enable circuitry is enabled. Additionally, as already described above, when device enters ER state, ER capacitor discharges through the SYSBST pin current; as shown in Figure 25, ER capacitor supplies the safing FET drain voltage too. Consequently, as safing FET drain voltage is reduced to a value around $V_{REG\_VSF\_S}$, regulator starts to operate in follower mode and VGS of the external FET will be clamped to $V_{VGS\_SF\_CLAMP}$.

As VSFx regulator is disabled, a pulldown current on VSFx_G pin ($I_{PD\_VSF\_G}$) is automatically activated. An external resistor (R_{PU}) and a diode ($D_{VSF\_S\_BIAS}$) are used to set VSFx_S voltage at a biasing value of approximately V_{SATBCK}, chosen to be lower than $V_{REG\_VSF\_S}$ voltage and higher than 5 V, so that regulator enabling circuit malfunctions can be detected, bias current drawn from battery can be minimized and LS/HS FET test can be performed properly.

A high-level description of VSFx regulator enabling control logic is shown in Figure 41. In order to enable VSFx regulator (that is VSFx_EN set to 1), all the following conditions must be met:

- Device must be in SAFING STATE or in ARM_SAFE
- No watchdog error is present
- PSINH_RSLT_LATCHED = 0 or PSINH_VSFx = 0
- At least one of ARM_RSLTx signals should be set to 1 (arming condition)

By the way, VSFx regulator can be configured as “passenger” or “nonpassenger” via PSINH_VSFx bit, located in VSFx_CTRL global SPI register; if set to 1, this bit makes VSFx regulator enabling signal sensitive to passenger inhibit latched state (PSINH_RSLT_LATCHED), that is if PSINH_RSLT is 1, VSFx regulator will not be enabled even if all the above conditions are met. PSINH_RSLT_LATCHED signal is updated with the current passenger inhibit status and stored as deployment enable state machine enters DEP_ENABLED state; this allow to keep regulator enable signals stable during deployment (see Section 8 Deployment drivers and diagnostics).

Moreover, if the device is in ARM_SCRAP state, VSFx regulator is automatically enabled without any other condition needed.

Figure 40. **Example of dual safing FET regulator circuit and diagnostic**

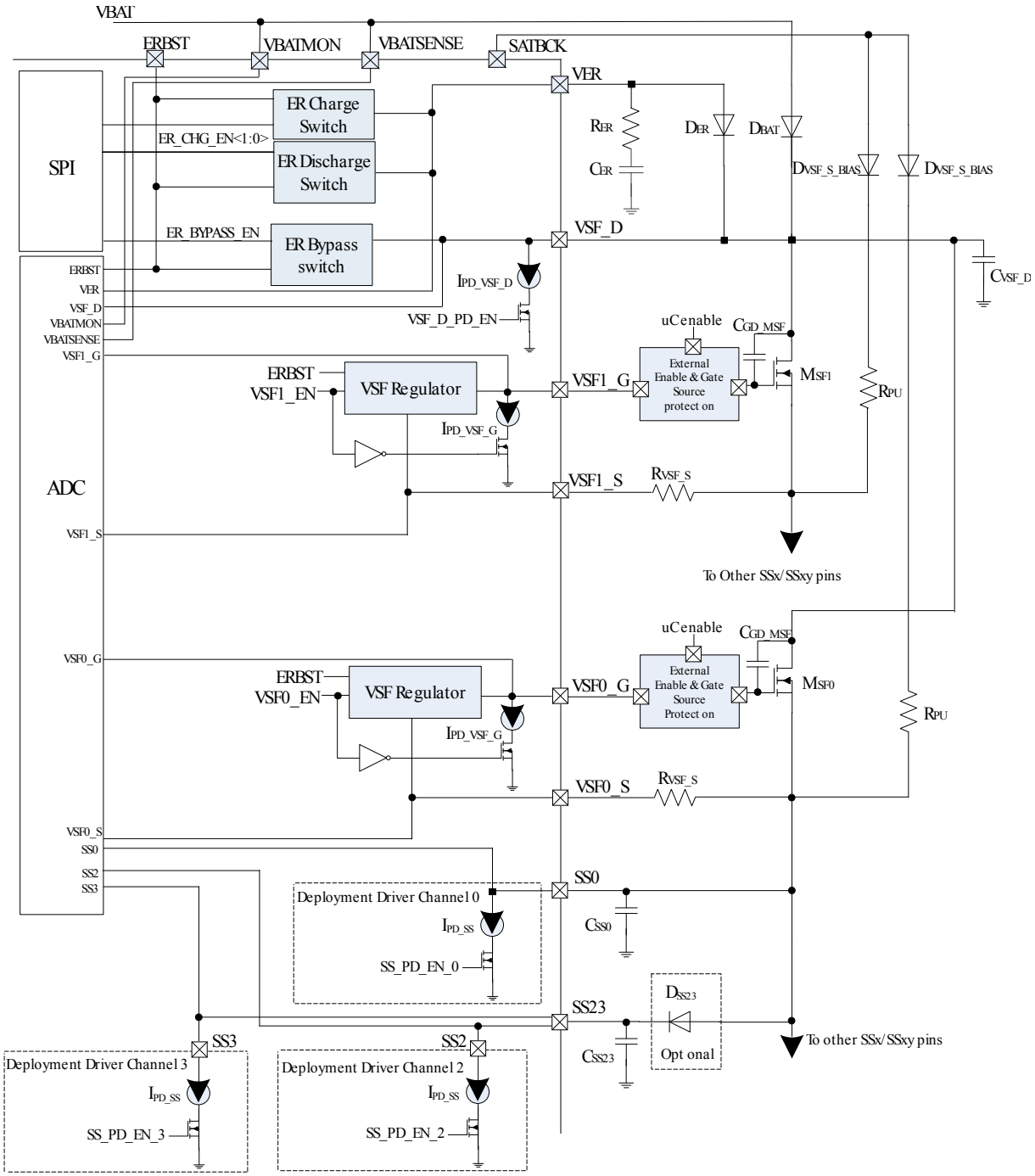
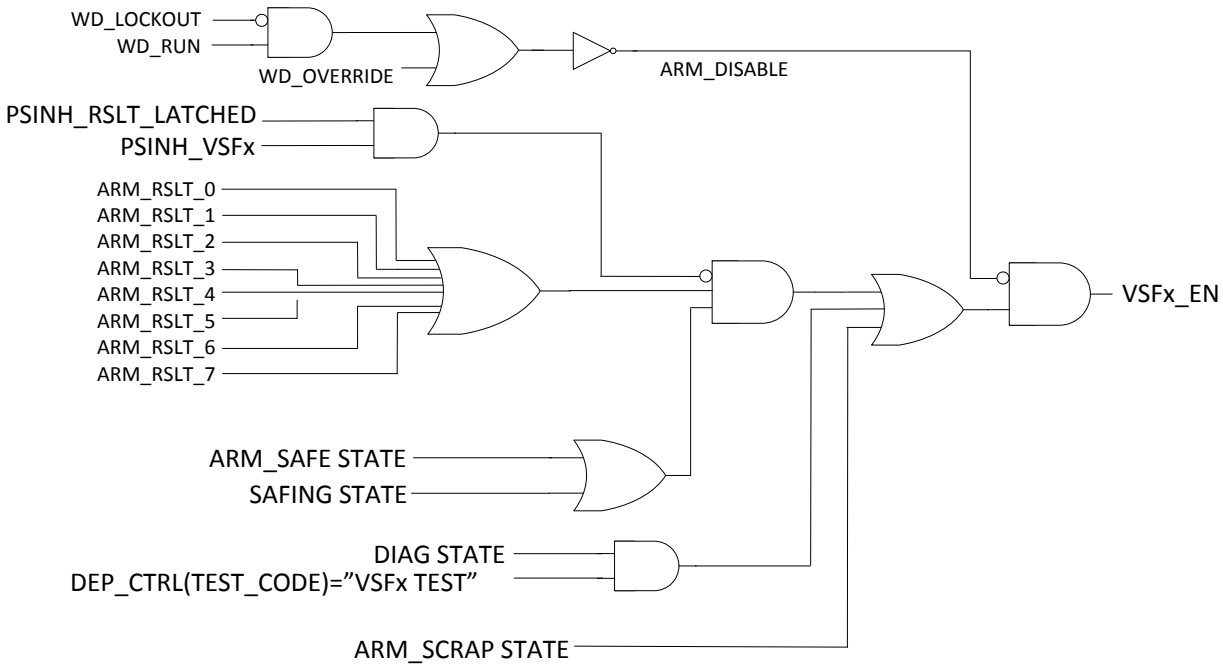


Figure 41. **VSFx regulator control logic**



7.2 Safety switch-off path

In case the V3V3_DIG or the V3V3PRE are in overvoltage condition, or a fault on the internal oscillators is detected (RESET_2_N is asserted), a safety switch-off path is triggered. The meaning of this safety path is to ensure a safe state for the system even in case the over voltage condition ($V_{OV\_SOFF\_V3V3\_DIG}$, $V_{OV\_SOFF\_V3V3PRE}$) caused by overshoot, particles, latent fault, etc., leads to absolute violation for the internal CMOS circuitry. In this latest event, functionality of the device cannot be guaranteed so a high voltage protected circuitry is needed to ensure switch-off of the VSFx regulators.

If an unsafe condition is detected, the high voltage switches directly connected to VSFx_G and to the bias current of the VSFx regulators are activated in order the switch-off the safing FET regulators. In case the logic is not damaged by an overvoltage condition, the safety echo status is available on SAFETY_ECHO_N bit in the DEVICE_STATUS global SPI register with a filter time $t_{FLT\_SAFETY\_ECHO\_N}$.

To ensure the right functionality in case the safe operating area of internal CMOS circuitry is exceeded, the reference and the supply of the safety switch off architecture is kept independent from the nets under monitor, moreover, according to the state of the art solutions, the safety circuitry is placed in an isolated layout area where no routing from other circuit functions is allowed and a safe distance from other circuits is kept to avoid crosstalk.

In order to detect a latent fault, at every startup, a selftest is implemented in the V3V3_DIG and V3V3PRE monitor circuitry. If a failure of these circuits is detected the bist fails with an error indication on SELFTEST_SAFETY_ECHO_ERR bit in the DEVICE_CTRL global SPI register. The completion of the BIST can be checked through SELFTEST_SAFETY_ECHO_COMPLETED in DEVICE_CTRL global SPI register.

7.3 Diagnostics

To support diagnostic check of VSFx regulator circuit and external connection integrity, the following additional features are provided:

- Capability to enable regulators even without a valid arming condition present
- SPI-controllable pulldown currents on VSF_D and SSx/SSxy pins
- Voltage measurements related to VSFx regulator circuit, provided by an internal A/D converter (requested and read via global SPI)

7.3.1 Safing FET and connection diagnostics

This diagnostic is performed while the device is in DIAG STATE and using DEP_CTRL global SPI register to enable the VSFx test (TEST_CODE bit field set to “VSFx TEST” modality, see Figure 41); VSFx regulator is enabled without any other condition needed.

Additionally, SSx/SSxy pull down currents (I_{PD_SS}) can be enabled in order to provide low current loading to the regulator and test connection integrity; even if SSxy deployment supply pins are internally connected to 2 channels, there is one pulldown current per each pad (see Figure 25). Each current generator can be enabled with SS_PD_EN_x bit, located in SS_PD_CTRL global SPI register.

A pulldown current on VSF_D pin is available as well ($I_{PD\_VSF\_D}$) and can be enabled through VSF_D_PD_EN bit, located in DEP_CTRL global SPI register; this current is used for both diagnostic purposes and to give the capability to discharge safing FET drain line capacitance.

After setting time (see Section 8 Deployment drivers and diagnostics, voltage A/D conversions of SSx/SSxy, VSFx_G, VSFx_S and VSF_D pins can be requested and read through DEP_DIAG_ADC_A and DEP_DIAG_ADC_B global SPI registers; if safing FET circuitry is properly working and connected, all measured voltages will be in the expected range.

The voltage conversions are not used by the device to take any action, such as regulator disabling. In order to avoid saturation of high voltage signal, an internal voltage divider of 15:1 is used. The bit fields, used to address the different measurements, are listed in Table 546.

Table 546. A/D conversion list for safing FET regulator circuits

ADC request [Hex] (DEP_DIAG_ADC_REQ_x)	ADC Results (DEP_DIAG_ADC_RES_A)	ADC Results (DEP_DIAG_ADC_RES_B)
1A	VSF_D	V_{OUT_LRM}(1)
1B	VSF0_G	VSF1_G
1C	VSF0_S	VSF1_S

1. *LRM voltage conversion; not related to safing FET and connection diagnostics.*

7.3.2 ER bypass switch

ER bypass switch is a current-limited back-to-back protected switch, controllable with ER_BYP_EN bit, located in DEP_CTRL global SPI register. When enabled, it provides an optional connection path from ERBST boost output to VSF_D pin. The main purpose of this switch is to allow charging of VSF_D pin up to ERBST voltage in order to perform safing FET diagnostic (described in previous section) directly through ERBST output, thus not needing to wait for ER cap to be charged.

7.3.3 Battery/ER cap diode connection diagnostic

As shown in Figure 25, deployment safing FET drain is normally connected to both battery and ER cap lines through a diode-OR connection.

The goal of battery/ER cap diode diagnostic is to detect if D_{ER} and D_{BAT} diodes are properly connected and operating without faults (short, open); this can be performed using both ER charge and discharge switches, controlled with ER_SW_CHG_DCHG_EN 2 bit field, located in PWR_CTRL_0 global SPI register.

As battery voltage (VBAT) is correctly supplied to the device, ER discharge switch can be enabled (ER_SW_CHG_DCHG_EN = 11) for enough time to discharge VER pin down to (VBAT - $V_{D\_BAT\_FWD}$), where $V_{D\_BAT\_FWD}$ is D_{BAT} diode forward voltage; then, by comparing VSF_D voltage A/D conversion and checking it vs. battery voltage one (given either by VBATMON or VBATSENSE voltage A/D conversion), it is possible to check if D_{BAT} diode is forward-biased and D_{ER} diode is in reverse-biased as expected.

On the other hand, ER charge switch can be enabled (ER_SW_CHG_DCHG_EN = 10) for enough time to charge VER pin to a voltage higher than VBAT; by comparing again VSF_D voltage A/D conversion vs. VBATMON/VBATSENSE one, it is possible to check if D_{BAT} diode is reverse-biased and D_{ER} diode in forward-biased as expected.

8 Deployment drivers and diagnostics

8.1 Deployment drivers

A deployment driver channel consists of a fully independent high-side and low-side driver, providing deployment and diagnostic capability for both squib and low energy actuator (LEA) loads; a model overview of both type of loads is shown in 0.

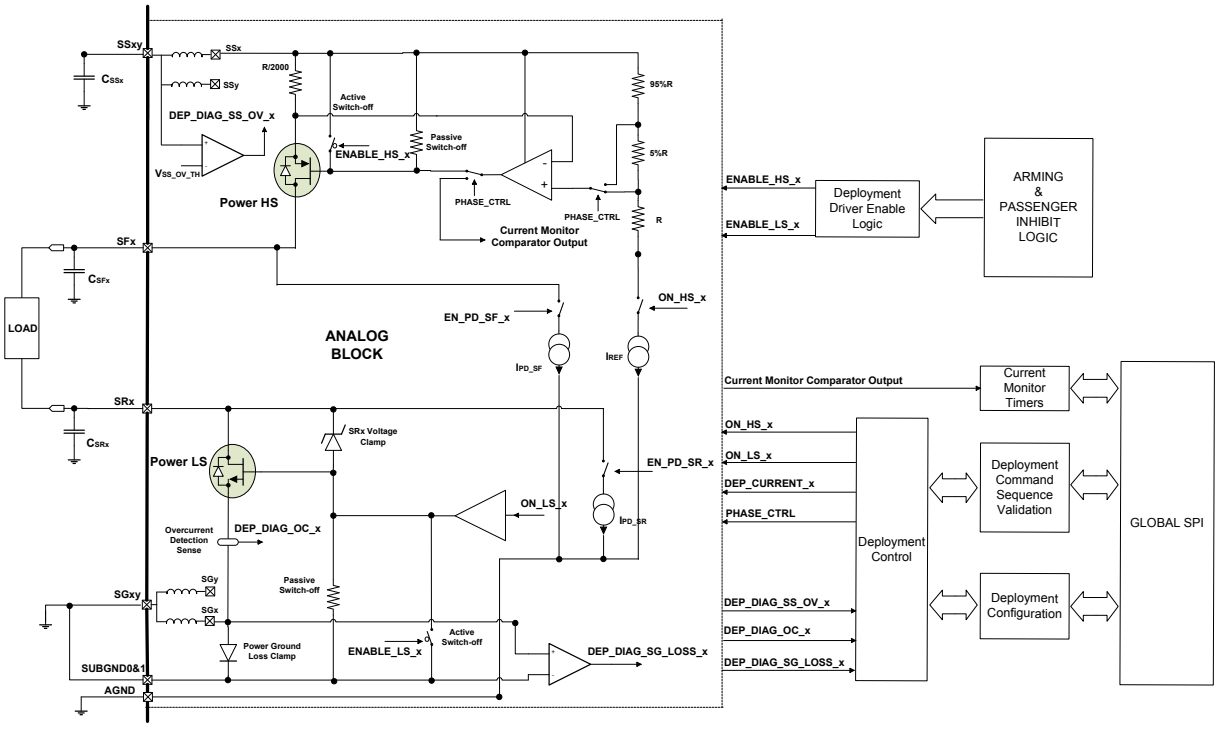
All deployment channels fully support squib load deployment and diagnostics; LEA load is fully supported for both deployment and diagnostics on channels 6 and 7 only.

Information that an LEA load is connected on channels 6 and/or 7 is given to the IC via DEP_CTRL Global SPI register through the dedicated bits DEP_LOAD_SEL_CH6 and DEP_LOAD_SEL_CH7.

8.2 Channel overview

A general overview of a deployment channel is shown in Figure 42.

Figure 42. Deployment channel general overview



Each deployment channel is provided with a deployment loop feed pin (SFx) and deployment loop return pin (SRx); load terminals are connected to these two pins. Both SFx and SRx pins can be loaded with additional external capacitors C_{SFx} and C_{SRx}, if needed for protection against ESD events.

SFx pin is connected to the deployment HS driver circuit, whose function is to regulate a constant current on the load for a programmed dwell time; both high and low current profiles are available to support the majority of load types. HS driver is supplied by a deployment supply pin, which could be either channel-dedicated (SSx) or grouped in channel pairs (SSxy); pin grouping scheme depends on the IC pinout. Current regulation accuracy is granted by dynamic offset compensation and high accuracy of an internal bias reference current (I_{REF}).

HS driver is controlled by logic with a dedicated enable signal (ENABLE_HS_x) and driver regulation activation signal (ON_HS_x). When ENABLE_HS_x signal is 0, driver gate is actively switched off; when device is unpowered, driver gate is kept in off state with a passive switch off circuit.

SRx pin is connected to the deployment LS driver circuit, whose function is to provide a low ohmic return path to ground for the load current; driver is supplied by an internal low voltage regulator. Driver power ground is provided by a deployment ground pin (SGxy), grouped in channel pairs.

LS driver is controlled by logic with a dedicated enable signal (ENABLE_LS_x) and driver activation signal (ON_LS_x). When ENABLE_LS_x signal is 0, driver gate is actively switched off; when device is unpowered, driver gate is kept in off state with a passive switch off circuit.

SRx and SFx pins have a dedicated pulldown current generator (I_{PD_SR}, I_{PD_SF} respectively) used for pin voltage conditioning and diagnostic purposes; these generators are automatically disabled during deployment on the channels being deployed while they remain active on channels not deployed.

Each deployment channel can withstand a minimum number of 300 deployments along lifetime, with energy E_{DEP} and with a deployment repetition time higher than 10 s; a maximum of 16 channels can be deployed simultaneously or in any other serial pattern. Additionally, many detection and protection features are provided as well (see Section 8.4 Driver protection and detection features) in order to protect each channel against overstress.

In case of short to ground/battery of SFx/SRx when the device is unpowered the energy transferred to the load must be less than E_{UNPOW}.

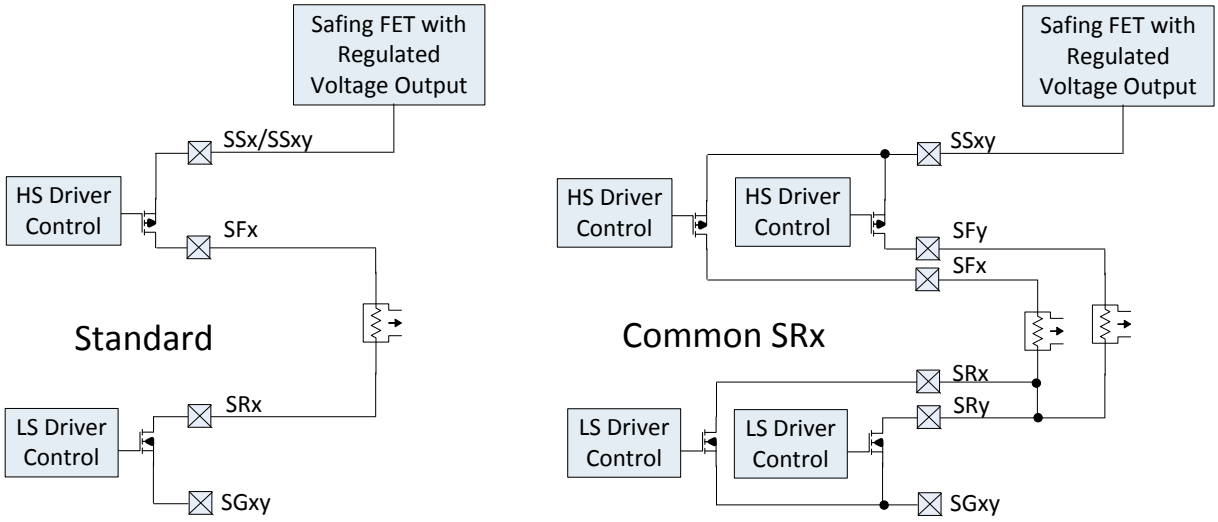
8.3 Application topologies

Supported application topologies are shown in Figure 43. There are two main loop topologies:

- Standard: each channel is connected to a single load.
- Common SRx: SRx pins of two channels are shorted outside the IC, in order to save one connection line on the application.

Common SRx topology is fully supported for both deployment and diagnostics on channel pairs (2, 3) and (4, 5) only. Information that common SRx configuration is done on channel pairs (2, 3) and/or (4, 5) is given to the IC via DEP_CTRL global SPI register through the dedicated bits DEP_CFG_SEL_CH23 and DEP_CFG_SEL_CH45.

Figure 43. Loop application topologies



To optimize power/energy dissipation on the HS driver power MOS during deployment, supply voltage for SSx/SSxy pins is provided by an integrated voltage regulator, using an external safing FET transistor as power element.

8.4 Driver protection and detection features

Deployment drivers provide several additional protection/detection features. A short description of each of them is provided below.

8.4.1 LS driver deactivation delay

A delay in LS driver deactivation with respect to HS driver ($t_{DEL\_OFF\_LS}$) is implemented in order to protect device pins against voltage spikes at the end of a deployment event. No equivalent delay is applied at deployment event start. In case an LEA load is used on channels 6 and/or 7 (selected through the dedicated bits DEP_LOAD_SEL_CH6 and DEP_LOAD_SEL_CH7), in order to discharge the stored energy in the LEA the delay in LS driver deactivation becomes $t_{DEL\_OFF\_LS\_LEA}$.

8.4.2 Power ground loss clamp, detection and protection

SGxy pin low ohmic connection to ground can be lost due to open/high resistance pin/bond wire faults; if deployment is executed in this situation, parasitic path activation can occur, creating a potential violation of the device safe operating area. For this reason, deployment drivers provide the following features:

- A power ground voltage clamp, in order to limit ground voltage; each channel has a dedicated clamp, even if power ground pins are grouped in pairs.
- A power ground loss comparator with threshold $V_{SG\_LOSS\_TH}$; even if ground pins are grouped in pairs, there is one comparator per each channel. Comparator detects a ground loss event and provides this information to the logic, that validates it with a filter time $t_{FLT\_SG\_LOSS}$. If ground loss event is confirmed, both LS and HS driver are immediately deactivated at the same time.

Occurrence of a confirmed power ground loss event is visible by accessing DEP_DIAG_SG_LOSS global SPI register; each channel has a dedicated bit (DEP_DIAG_SG_LOSS_x), indicating detection of a ground loss event since last SPI reading and cleared upon reading. DEP_DIAG_SG_LOSS_x bit reading and clearing is mandatory to allow a new deployment event for the faulted channels.

Outside a deployment event, power ground loss can be detected during load resistance measurement diagnostic execution, as the activation of I_{SRC} and I_{SINK} diagnostic currents allows to lift the open ground voltage up to comparator threshold.

8.4.3 LS driver current limitation, overcurrent detection and protection

In case SRx pin is shorted to battery with low resistance during deployment, LS driver current is limited at I_{LIM_LS} to avoid overstress. A dedicated overcurrent comparator with threshold $I_{OC\_LS\_TH}$ detects an overcurrent event and provides this information to the logic, that validates it with a filter time $t_{FLT\_OC\_LS}$. An up-down counter is implemented which counts up if the LS current is above the overcurrent threshold and counts down if below threshold. If overcurrent event is confirmed, LS driver is immediately deactivated for the rest of the dwell time, while HS driver is kept active. LS activation capability is restored at the next deployment event.

Occurrence of a confirmed overcurrent event is visible by accessing DEP_DIAG_OC global SPI register; each channel has a dedicated bit (DEP_DIAG_OC_x), indicating detection of an overcurrent event since last SPI reading and cleared upon reading. DEP_DIAG_OC_x bit reading and clearing is mandatory to allow a new deployment event for the faulted channels.

The user should be aware that if the LS driver is deactivated for a confirmed overcurrent event, DEP_DIAG_OC_x is read and cleared and new deployment commands (DEP_CMD_x and DEP_CMD_N_x) are issued, while the device is still in DEP_ENABLED state, the LS driver is enabled again leading the LS to energy overstress during deployment.

8.4.4 LS driver drain voltage clamp

When LS driver is turned off, high voltage transients at SRx pin can occur due to load inductive behavior, potentially causing voltage overstress on LS driver. A LS drain to gate flyback clamp circuit is implemented to trigger reactivation of LS driver, thus allowing residual inductance current recirculation. As an effect, SRx voltage will be limited to a value V_{CLAMP_SR}.

8.4.5 Short to ground

Deployment driver is capable of granting a successful deployment in case of short to ground on SFx or SRx pin, as HS driver is intrinsically current limited and the HS FET is sized to handle the related energy.

A short to ground event during deployment may also occurs after an open circuit; in this case, HS current regulator normally reacts by increasing HS power MOS VGS, generating a high amplitude current overshoot. For this reason, HS driver provides a dedicated fast comparator detecting this condition, generating a quick VGS discharge and reducing current overshoot time duration and amplitude.

8.4.6 SSx/SSxy overvoltage protection and detection

An overvoltage condition on SSx/SSxy pins, that is, pin voltage higher than the normal regulation voltage, can lead HS driver to energy overstress during deployment; for this reason, SSx/SSxy pins are monitored with a dedicated comparator with threshold $V_{SS\_OV\_TH}$. In case comparator detects an overvoltage event, it provides this information to the logic, that validates it with a deglitch asymmetrical filter. An asymmetrical filter time is implemented with rising filter time $t_{FLT\_SS\_OV\_RISE}$ when the SSx/SSxy voltage goes above the threshold and with falling filter time $t_{FLT\_SS\_OV\_FALL}$ when the SSx/SSxy voltage goes below the threshold. If overvoltage event is confirmed, deployment is terminated using the same procedure as described in Section 8.4.1 LS driver deactivation delay. Using SS_OV_DEP_INH_CTRL bit located in DEP_DIAG_SS_OV_DIS global SPI register, it is possible to use latched output (SS_OV_DEP_INH_CTRL = '1') or filtered output to inhibit the deployment (SS_OV_DEP_INH_CTRL = '0').

Occurrence of a confirmed overvoltage event is visible by accessing DEP_DIAG_SS_OV global SPI register; each pin has a dedicated bit (DEP_DIAG_SS_OV_x/DEP_DIAG_SS_OV_x_y), indicating detection of an overvoltage event since last SPI reading and cleared upon reading. DEP_DIAG_SS_OV_x bit reading and clearing is mandatory to allow a new deployment event for the faulted channels, in case of SS_OV_DEP_INH_CTRL = '1'. DEP_DIAG_SS_OV_x bit reading and clearing is not mandatory to allow a new deployment event for the faulted channels, in case of SS_OV_DEP_INH_CTRL = '0'.

Overvoltage detection and protection are active only during deployment dwell time, that is, if an overvoltage condition is present before deployment start, it does not prevent deployment to occur. Additionally, the overvoltage protection is active also in DIAG STATE as described in section 9.8, and so when the device exits from DIAG STATE the DEP_DIAG_SS_OV SPI register must be read and cleared. Overvoltage protection can be disabled using DEP_DIAG_SS_OV_DIS_x/DEP_DIAG_SS_OV_DIS_x_y bit located in DEP_DIAG_SS_OV_DIS global SPI register (0 default value at power-on). Only the effect on the deployment is masked, that means in case an SSx/SSxy overvoltage event occurs the deployment will not be interrupted while the overvoltage event will be reported on the DEP_DIAG_SS_OV global SPI register. The user should be aware that disabling the SSx/SSxy overvoltage protection can lead to a violation of the maximum allowed V_{DEP} and so it can lead HS driver to energy overstress during deployment.

8.5 Deployment logic

A simplified block diagram of deployment logic and its interaction with analog part is given in Figure 42.

In order to occur, deployment requires two main concurrent conditions:

- A valid arming condition generated by arming logic; this allows to enable the deployment driver circuits.
- A specific sequence of deploy commands, received on global SPI, confirming the will to deploy one or more specific channels.

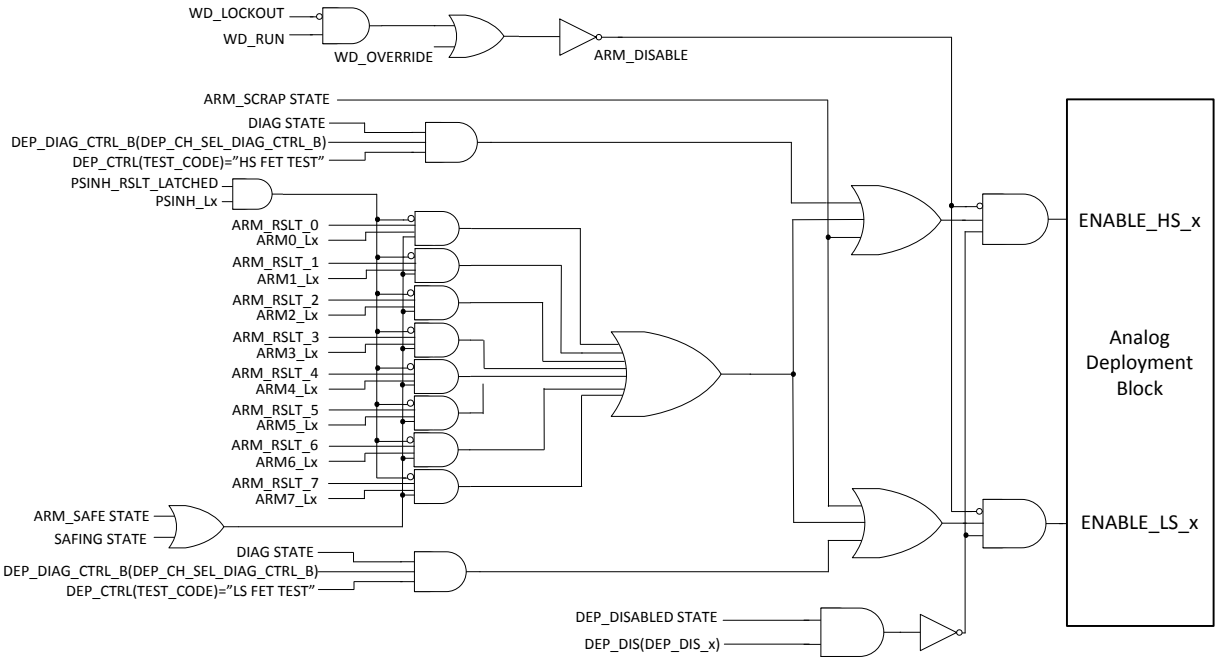
There is no hard constraint on the order with which arming condition and deployment command sequence should be received; thus, two realistic scenarios are possible:

- Deploy command sequence is received while a valid arming condition is already present (within Arm pulse stretch timer duration t_{PULSE_STRECH}): in this case, deployment is started immediately.
- Deploy command sequence is received without a valid arming condition already present: in this case, deployment request is accepted and remains valid until deployment expiration timer reaches the programmed value t_{DEP_EXPIRE}.

8.5.1 Driver enabling

Necessary condition to perform deployment is that both LS and HS driver circuits are enabled; the simplified logic that controls ENABLE_LS_x and ENABLE_HS_x signals is shown in Figure 44.

Figure 44. **Deployment driver enable logic**



Logic requires the following conditions in order to set both HS and LS driver enable signals to 1:

- Logic is out of power-on reset (POR = 1).
- No watchdog error is present.
- Device is in SAFING STATE or in ARM_SAFE STATE.
- A valid arming condition from arming logic is present, that is one or more of the 8 ARM_RSLT_y signals are set to 1.
- Channel is correctly mapped to one or more ARM_RSLT_y signals via arming loop matrix; this is done by programming the 8 LOOP_MATRIX_ARMy registers on global SPI (one register per each ARM_RSLT_y). Each of these registers contains 16 ARMy_Lx bits; if ARMy_Lx bit is set to 1, ARM_RSLT_y signal is mapped to channel x.

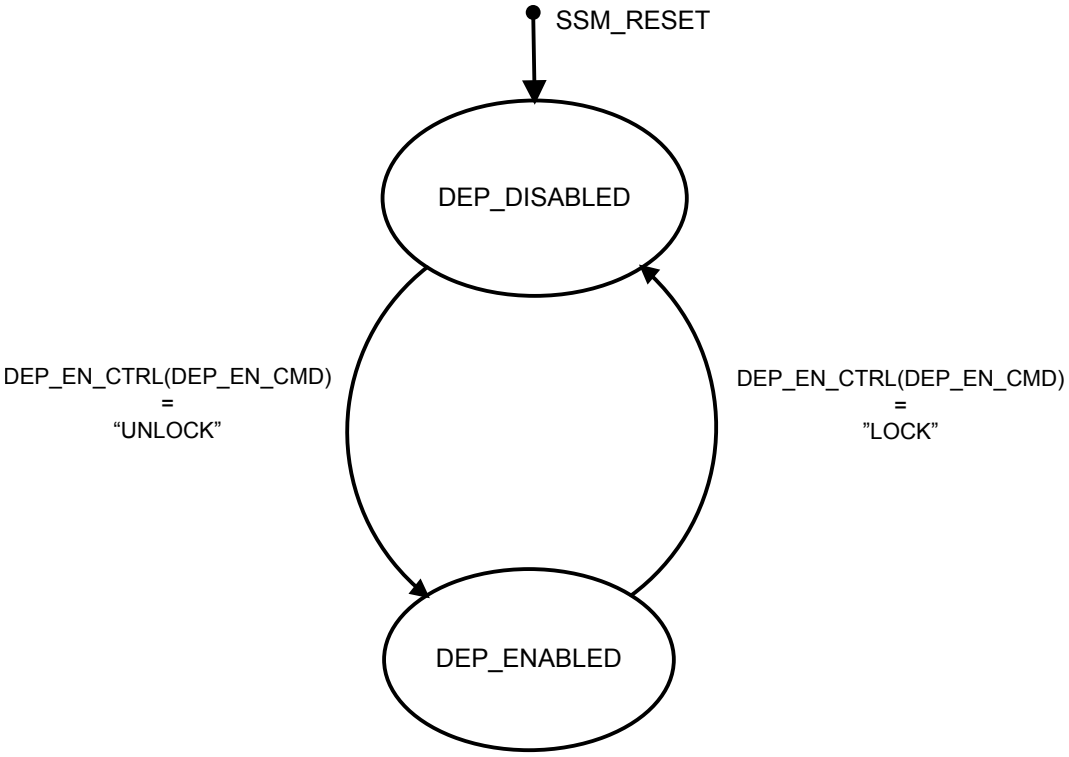
Additionally, each deployment channel can be configured as “passenger” or “nonpassenger”; this is done by programming LOOP_MATRIX_PSINH register on global SPI. This register contains 16 PSINH_Lx bits; if PSINH_Lx bit is set to 1, channel x is defined as a “passenger” channel and makes its enabling signals sensitive to passenger inhibit latched state that is if PSINH_RSLT_LATCHED is 1, both LS and HS driver enable signals will not be set to 1 even if all conditions described before are met.

If the device is in ARM_SCRAP STATE, all deployment drivers are automatically enabled without any other condition needed. Additionally, as the device in DIAG STATE, it is possible to enable drivers as well to perform LS/HS FET test diagnostics.

8.5.2 Deployment command sequence

Deployment start request procedure is performed through global SPI communication and correct handling of deployment enable state machine (shown in Figure 45).

Figure 45. Deployment enable state machine



In order to provide to the IC a valid deployment request on the required channels, these conditions must be met:

- Deployment enable state machine is put in DEP_ENABLED state, using DEP_EN_CTRL global SPI register and writing the UNLOCK code (F0F0) in DEP_EN_CMD 16 bit data field. DEP_ENABLED state is global for the whole device, that is valid for all channels.
- A deployment command global SPI frame (DEP_CMD) is received, with the required channel-dependent DEP_CMD_x bit set to 1.
- An additional deployment command global SPI frame (DEP_CMD_N) is received, with the required channel-dependent DEP_CMD_N_x bit set to 0, as confirmation of DEP_CMD frame.

DEP_DISABLED is the default state after power-on. After entering DEP_ENABLED state, the following functionalities are no more available, that is will not be enabled even if requested via SPI:

- Modification of deployment command expiration time (DEP_EXPIRE_TIME_x, see Section 8.6.1 Standard deployment profile)
- All diagnostic voltage and current sources that can be connected to deployment pins (SFx and SRx)

Additionally, as device enters DEP_ENABLED state, PSINH_RSLT_LATCHED signal is updated with the current passenger inhibit status and stored; this allows to keep deployment analog block enable signals stable during deployment (see Figure 44).

Moreover, as device enters DEP_ENABLED state, the ground loss detection of the following pins SATBCKGND, VCCBCKGND, BSTGND, AGND, PGND can be inhibited during a deployment event using GND_LOSS_DEP_INH_EN bit located in CLK_CTRL global SPI register.

If state machine is not in DEP_ENABLED state, DEP_CMD and DEP_CMD_N requests are discarded; on the other hand, there is no hard constraint on DEP_CMD and DEP_CMD_N frame receiving order. When state machine is in DEP_ENABLED state the two commands DEP_CMD and DEP_CMD_N are automatically cleared as soon as they are issued. If only one of the two commands is sent while in DEP_ENABLED state and the state machine is put back in DEP_DISABLED state, DEP_CMD and DEP_CMD_N registers are cleared.

Once deployment is initiated on a channel and state machine is in DEP_ENABLED state, an SSM_RESET (safety state machine reset, RESET_4_N) can prematurely terminate it.

Should it be necessary to redeploy a channel, previous deployment must be completed before initiating the new one, that is deployment dwell timer expiration; then, upon completing first deployment, it is mandatory to follow these steps:

- Put deployment enable state machine back to DEP_DISABLED state, using DEP_EN_CTRL global SPI register and writing the LOCK code (0F0F) in DEP_EN_CMD 16 bit data field. As DEP_ENABLED state, DEP_DISABLED state is global for the whole device, that is valid for all channels.
- Issue the reading of the deployment protection registers DEP_DIAG_SG_LOSS, DEP_DIAG_OC, DEP_DIAG_SS_OV to provide mandatory clearing of the faults before a new deployment event.
- Reenter DEP_ENABLED state back again, as already described at the beginning of this section.
- Send the required DEP_CMD and DEP_CMD_N global SPI commands, as already described.

Deploy expiration timer is not reset when the device come back in DEP_DISABLED state. So, if a first deployment has been completed and the deploy expiration time is not expired when the device goes again in DEP_ENABLED state, a new deployment is started again without sending DEP_CMD and DEP_CMD_N global SPI commands. In order to avoid this behavior is mandatory to configure the deploy expiration time with the dedicated 2 bit field “11” = 0 ms (see Section 8.6.1 Standard deployment profile).

In order to be able to stop a malfunctioning deployment behavior caused by hardware failure (for example, deployment dwell timer not expiring), both LS, and HS drivers of a channel can be immediately disabled with the DEP_DIS global SPI frame, using one or more of the 16 DEP_DIS_x bits (one per each channel); however, as shown in Figure 44, this disable request is accepted only in DEP_DISABLED state, as the intent of this feature is not to give the possibility to prematurely stop a correctly behaving deployment event. The DEP_DIS command has only effect in DEP_DISABLED state and so it is mandatory to write to ‘0’ the DEP_DIS global SPI register before entering DEP_ENABLED state in order to be sure that bits are of the DEP_DIS_x mistakenly set.

8.6 Deployment profile settings and current monitoring

Deployment profile settings are programmed using global SPI interface. Main deployment parameters are listed here:

- Deployment current value (high/low)
- Deployment dwell time
- Deployment command expiration time

Each deployment HS driver provides a current monitoring feature, which allows to understand if actual regulated deployment current is above 90% of the programmed value; monitoring circuit includes deployment current monitor digital counters, whose values can be accessed via global SPI. Deployment running/successful status global SPI bits are available as well.

In addition to a standard deployment profile (that is constant current regulation for the programmed dwell time, without any possibility of runtime current value change), all deployment channels support the automatic dynamic profile change feature, that is automatic runtime change of deployment current and dwell time value due to not achieving initially programmed current value for entire programmed dwell time.

8.6.1 Standard deployment profile

Standard deployment profile is the default deployment mode for all channels after power-on; when deployment is started, HS driver tries to regulate the programmed current value, that is I_{DEP_H} in case of high value, I_{DEP_L} in case of low value.

At the same time, deployment dwell timer is started as well; as this timer reaches the programmed value t_{DEP_DWELL}, LS, and HS drivers are turned-off with the sequence described in Section 8.4.1 LS driver deactivation delay. The deployment dwell timers are count-up counters; as a deployment event starts, timers are initialized to 0 and will count up. All counters are initialized to 0 upon system power-on and reset; moreover, counters are reset upon entering in SAFING STATE.

In order to define standard deployment profile parameters for each channel, the following steps are needed:

- In DIAG STATE programming of the 4 deployment profile configuration registers on global SPI, that is DEP_CFG_A, DEP_CFG_B, DEP_CFG_C and DEP_CFG_D

- In DIAG STATE or SAFING STATE or SCRAP STATE or ARM_SAFE STATE or ARM_SCRAP STATE programming of the 2 deployment profile loop association registers on global SPI, that is DEP_PROF1_MATRIX_L0_7 and DEP_PROF1_MATRIX_L8_15

Each of the 4 DEP_CFG_x registers allows to configure a predefined profile type, composed by:

- DEP_CURRENT_x: defines deployment current value with a 2 bit field, “01” selects low current while “10” selects high current; “00”and “11” are considered as invalid values. Default value at power-on is “00”, thus this bit field must be programmed at least once.
- DEP_DWELL_TIME_x: defines deployment dwell time with an 8 bit field and time LSB equal to $t_{RES\_DEP\_DWELL}$; “00000000” is considered as invalid value. Default value at power-on is “00000000”, thus this bit field must be programmed at least once.
- DEP_EXPIRE_TIME_x: it defines deployment command expiration time, that is valid deployment command sequence expiration time, with a 2 bit field; 4 fixed and valid selection values are available, with “00”=500ms default value at power-on.

The 4 DEP_CFG_x registers can be written only in DIAG STATE.

If DEP_CURRENT_x and/or DEP_DWELL_TIME_x bits are programmed with invalid values, deployment will not start even if a potentially valid deployment request is received by logic.

If uC tries to change DEP_CURRENT_x and/or DEP_DWELL_TIME_x values while deployment is running (that is dwell timer started and counting up), new programming values are rejected and configuration error detection bit (that is DEP_CFG_ERR_x bit in DEP_CFG_x register) is set to 1.

Additionally, DEP_CFG_ERR_x bit is set to 1 even if µC tries to change DEP_EXPIRE_TIME_x value while device is in DEP_ENABLED state, rejecting the new programmed value.

Then, using DEP_PROF1_MATRIX_L0_7 register bits (DEP_PROF1_Lx, 2 bit field, with x from 0 to 7) and/or DEP_PROF1_MATRIX_L8_15 bits (DEP_PROF1_Lx, 2 bit field, with x from 8 to 15), association between channel and deployment profile A/B/C/D is done.

This profile configuration strategy is implemented in order to allow fast switching from one profile to another, for example if, for some reason, µC wants to change configuration of channel 10 from profile A to profile C, only reprogramming of DEP_PROF1_MATRIX_L8_15 register is needed (but before the deployment starts).

8.6.2 Current monitoring

Even if deployment current regulator is kept on for all the dwell timer duration, actual current provided to the load could be lower than the programmed value for a significative part of the dwell time; this behavior is mainly due to transitory variation of the load impedance. For this reason, actual HS output current is monitored by a dedicated current comparator, whose threshold is $I_{DEP\_MON\_TH}$; threshold value is proportional to the programmed deployment current value. The effective deployment time t_{DEP_EFF}, that is, the time interval in which deployment current value is above 90% of the programmed target value I_{DEP_L}/I_{DEP_H}, can be calculated as follows:

$$t_{DEP\_EFF} = DEP\_DWELL\_TIME\_x \times t_{RES\_DEP\_DWELL} - t_{DEP\_DEL} \quad (3)$$

Where t_{DEP_DEL} is the delay time between the actual receiving of the deployment start command (global SPI CS rising edge) and the rising deployment current value reaching 90% of the programmed target value and DEP_DWELL_TIME_x x $t_{RES\_DEP\_DWELL}$ is the programmed dwell timer counter value equivalent time.

In addition to the comparator, digital current counters are present as well, counting for how much time output current stays above $I_{DEP\_MON\_TH}$. Each channel has 2 independent 8 bit current counters:

- Low current counter: active only when I_{DEP_L} current value is configured; counting depending on current monitor comparator output.
- High current counter: active only when I_{DEP_H} current value is configured; counting depending on current monitor comparator output.

All counters are initialized to 0 upon system power-on and reset; moreover, counters are reset upon entering DEP_DISABLED state and a new valid deployment command sequence is received.

Additionally, counter monitor timer circuit can be configured in 2 different modes:

- Cumulative
- Max uninterrupted

Timer mode configuration is done via DEP_CTRL global SPI register, DEP_CMT_MODE bit; 0 selects cumulative mode, 1 selects max uninterrupted mode. If not programmed elsewhere after power-on, cumulative timer mode is the default.

Selection of one of the two modes determines the content meaning of DEP_CMT_x global SPI read-only registers. There is one register per each channel; each register provides 2 separate 8 bit data fields:

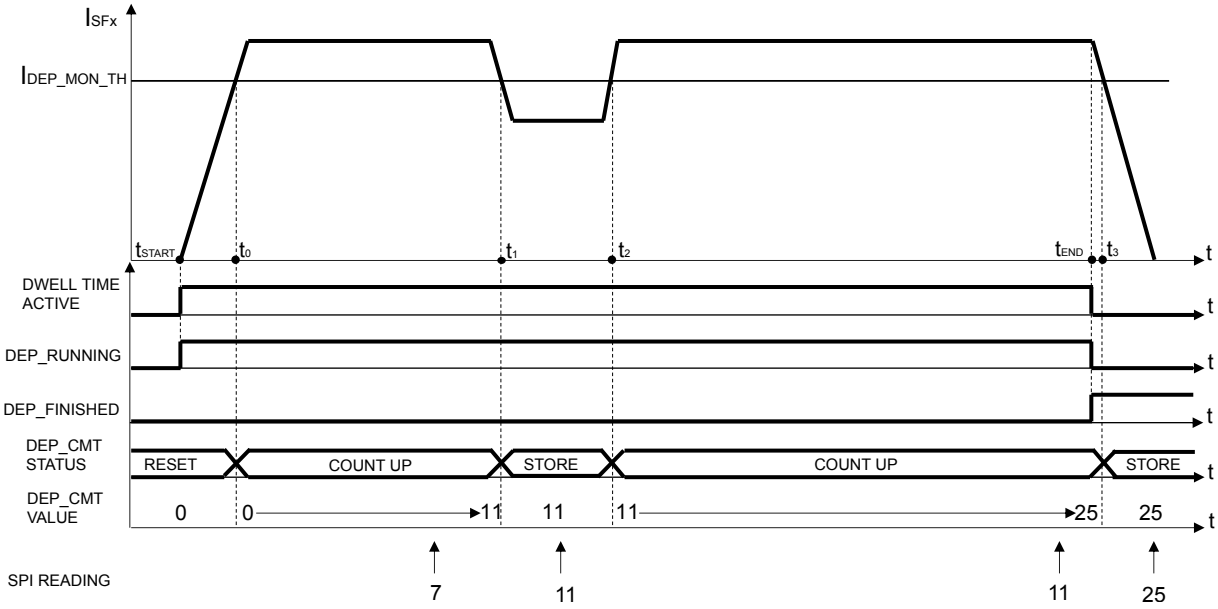
- Low current field (DEP_CMT_L_x)
- High current field (DEP_CMT_H_x)

8.6.2.1 *Cumulative mode*

See Figure 46 for a quick example of cumulative mode operation. If deployment current falls below current comparator threshold momentarily and recovers, the relative current counter pauses during the drop-out and continues once current exceeds the threshold again; counter is neither reset or decreased by the presence or absence of current output.

Cumulative counter value can be read in either DEP_CMT_L_x or DEP_CMT_H_x data fields; read value indicates counter value as it is at the moment of SPI reading event.

Figure 46. Cumulative mode operation

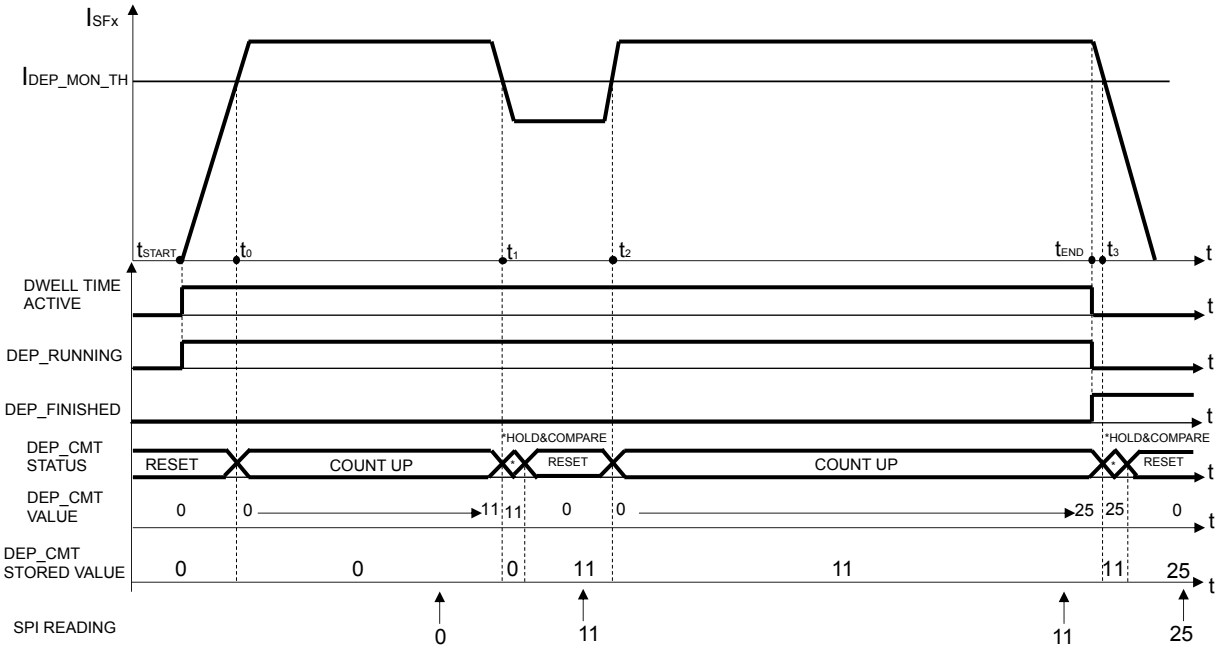


8.6.2.2 *Max uninterrupted mode*

See Figure 47 for a quick example of max uninterrupted mode operation; current monitor current counter will be used to measure the longest time for which deployment current has exceeded $I_{DEP\_MON\_TH}$ without interruption. As current falls below threshold, counter will hold its count value and then compare it to the previous stored value (0 at deployment start), updating the stored value if a new maximum is found; then, counter is reset, waiting for current to go above threshold again. All digital operations (comparison, storage of new value, counter reset) occur within one counter clock sample $t_{RES\_DEP\_CMT}$.

Max uninterrupted counter value can be read in either DEP_CMT_L_x or DEP_CMT_H_x data fields; read value indicates counter value as it is at the moment of SPI reading event.

Figure 47. Max uninterrupted mode



8.6.3 Automatic dynamic profile mode

Automatic dynamic profile mode allows to do a deployment current value change within deployment dwell time, normally not allowed in standard profile mode. This feature is mainly used to face the following two main applicative scenarios:

- High deployment current value is programmed and started; however, high current level cannot be reached or sustained due to insufficient current capability of either ER cap or VBAT line.
- High deployment current value is programmed and started; however, high current level cannot be reached or sustained due to transient increase of squib resistance value.

Thus, main usage model is the following:

- A “primary” deployment profile is configured (PROF1, high current value).
- Deployment starts with PROF1 but, in case HS output current cannot be sustained, switch to PROF2 is performed.

The “secondary” deployment profile is automatically fixed (PROF2, low current value and such dwell time as to reach a total composite dwell time of $t_{DEP\_AUTO\_SAFE}$). A safe timer starts along with the PROF1 dwell time and last always $t_{DEP\_AUTO\_SAFE}$. The safe timers are count-up counters; as a deployment event starts, timers are initialized to 0 and will count up. All counters are initialized to 0 upon system power-on and reset; moreover, counters are reset upon entering in SAFING STATE.

In order to detect the need to switch from PROF1 to PROF2 within dwell time, automatic dynamic deployment relies on the already available current monitor circuitry, with the addition of a deglitch filter ($t_{DEP\_AUTO\_FLT}$) in order to avoid spurious detections; as logic detects and validates an insufficient current level condition, automatic profile switching is started.

If the switch from PROF1 to PROF2 is validated the PROF1 dwell time is interrupted and the deployment continues until the safe timer $t_{DEP\_AUTO\_SAFE}$ is expired. Otherwise, if the high deployment current value is sustained for all the PROF1 dwell time the deployment is interrupted at the end of the PROF1 dwell time.

Additionally, it is possible that PROF1 is never reached at all in the initial current rise phase; to cover this particular scenario, a deployment start counter is provided (with duration $t_{DEP\_AUTO\_START}$), that is if PROF1 current level is not reached before this counter expires, switching to PROF2 is started.

In order to be correctly selected and executed, automatic dynamic deployment mode requires to follow these global SPI programming steps:

- Selection of automatic dynamic profile mode, using DEP_AUTOPROF_CFG; mode is selectable on all channels independently with DEP_AUTOPROF_x bits (default value at power-on is “0”). DEP_AUTOPROF_CFG register can be written in DIAG STATE or SAFING STATE or SCRAP STATE or ARM_SAFE STATE or ARM_SCRAP STATE.
- Programming of the 4 deployment profile configuration registers on global SPI, that is DEP_CFG_A, DEP_CFG_B, DEP_CFG_C and DEP_CFG_C, equivalent to what described in Section 8.6.1 Standard deployment profile.
- Programming of the 2 deployment primary profile loop association registers on global SPI, that is DEP_PROF1_MATRIX_L0_7 and DEP_PROF1_MATRIX_L8_15, equivalent to what described in Section 8.6.1 Standard deployment profile; this configuration defines the primary deployment profile PROF1.

As to current monitoring feature, there is no difference with respect to what described in Section 8.6.2 Current monitoring; if within dwell time both current levels are deployed due to profile switching, DEP_CMT_L_x or DEP_CMT_H_x will give separate indication of the actual deployment times at high/low current. Both cumulative and max uninterrupted timer modes are available.

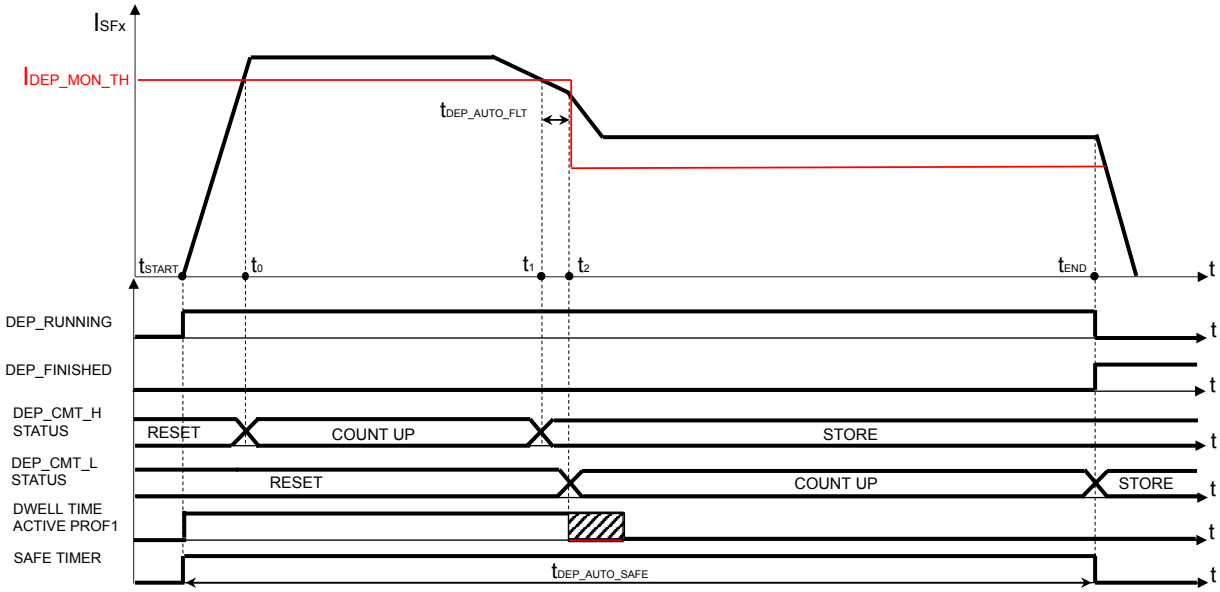
8.6.3.1 *Example 1*

See Figure 48. Channel is configured as indicated:

- Automatic dynamic deployment enabled
- PROF1: high current, $t_{DEP\_DWELL\_TIME\_P1}$ dwell time

Deployment process begins normally: primary dwell timer starts to count from t_{START} and high current level is achieved in the required time, that is $I_{DEP\_MON\_TH}$ value is reached at t_0, with (t_0 - t_{START}) < $t_{DEP\_AUTO\_START}$; while regulated current is above $I_{DEP\_MON\_TH}$, deployment high current monitor counter increments. Due to external insufficient current capability, at time t_1 current drops below $I_{DEP\_MON\_TH}$ for a time longer than $t_{DEP\_AUTO\_FLT}$, thus at time t_2 HS driver automatically starts to switch to the PROF2 low current profile; deployment high current monitor timer value at t_1 is stored in DEP_CMT_H_x. The current successfully reaches the PROF2 current value; deployment low current monitor timer starts counting from t_2 as well. As safe timer expires, at time t_{END} deployment is terminated; deployment low current monitor timer value at t_{END} is stored in DEP_CMT_L_x. Total composite dwell time is t_{END} - t_{START}, that is (t_2 - t_{START}) + $t_{DEP\_DWELL\_TIME\_P2}$, where (t_2 - t_{START}) ≤ $t_{DEP\_DWELL\_TIME\_P1}$.

Figure 48. Automatic dynamic deployment example 1



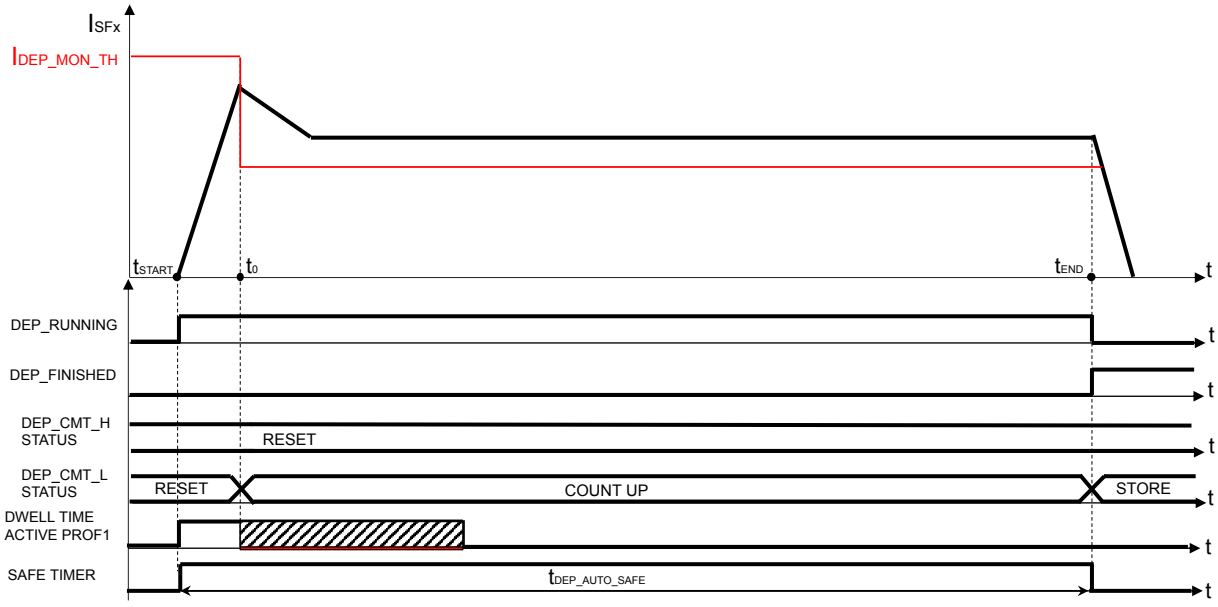
8.6.3.2 *Example 2*

See Figure 49. Channel is configured as indicated:

- Automatic dynamic deployment enabled
- PROF1: high current, $t_{DEP\_DWELL\_TIME\_P1}$ dwell time

Deployment process begins normally: primary dwell timer starts to count from t_{START} but, because of external insufficient current capability, high current level cannot be achieved in the required time, that is $I_{DEP\_MON\_TH}$ value is not reached in a time lower than $t_{DEP\_AUTO\_START}$; so at time $t_0 = t_{START} + t_{DEP\_AUTO\_START}$, HS driver automatically starts to switch to the PROF2 low current profile, so deployment high current monitor counter never starts counting. Safe timer continues to count and current successfully reaches the low current value; deployment low current monitor timer starts counting from t_0 as well. As safe timer expires, at time t_{END} deployment is terminated; deployment low current monitor timer value at t_{END} is stored in DEP_CMT_L_x. Total composite dwell time is t_{END} - t_{START}, that is $t_{DEP\_AUTO\_START}$ + $t_{DEP\_DWELL\_TIME\_P2}$.

Figure 49. Automatic dynamic deployment example 2



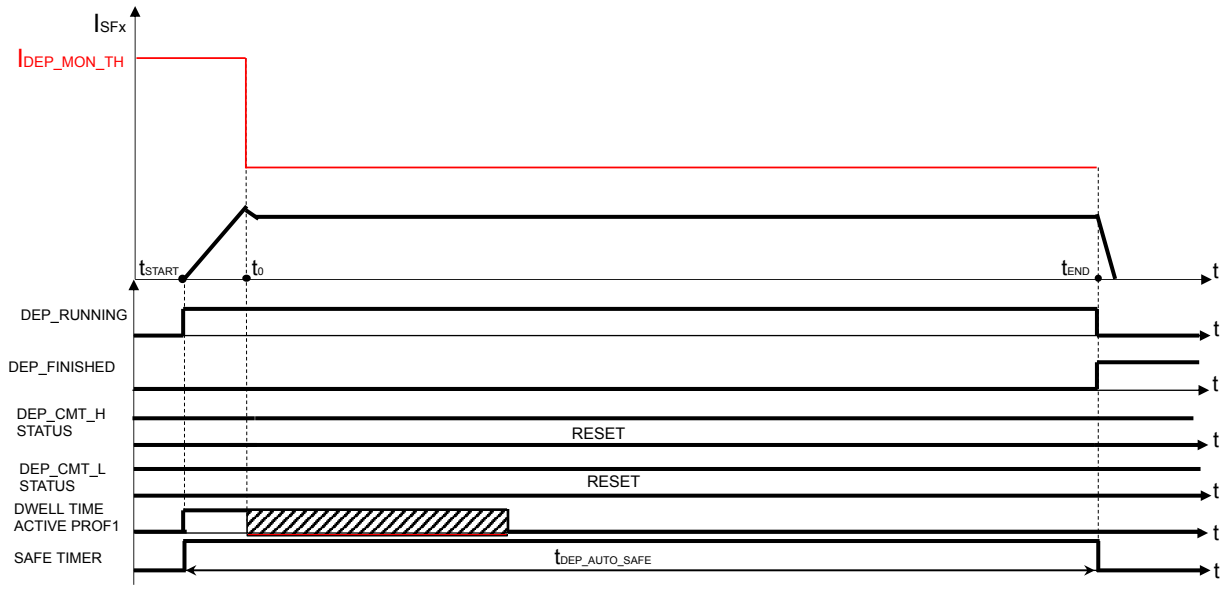
8.6.3.3 *Example 3*

See Figure 50. Channel is configured as indicated:

- Automatic dynamic deployment enabled
- PROF1: high current, $t_{DEP\_DWELL\_TIME\_P1}$ dwell time

Deployment process begins normally: primary dwell timer starts to count from t_{START} but, because of external insufficient current capability, high current level cannot be achieved in the required time, that is $I_{DEP\_MON\_TH}$ value is not reached in a time lower than $t_{DEP\_AUTO\_START}$; so at time $t_0 = t_{START} + t_{DEP\_AUTO\_START}$, HS driver automatically starts to switch to the secondary low current profile, so deployment high current monitor counter never starts counting. Safe timer continues to count but current cannot reach the low current value too; deployment low current monitor timer never starts counting as well. As safe timer expires, at time t_{END} deployment is terminated; total composite dwell time is $t_{END} - t_{START}$, that is $t_{DEP\_AUTO\_START} + t_{DEP\_DWELL\_TIME\_P2}$.

Figure 50. Automatic dynamic deployment example 3



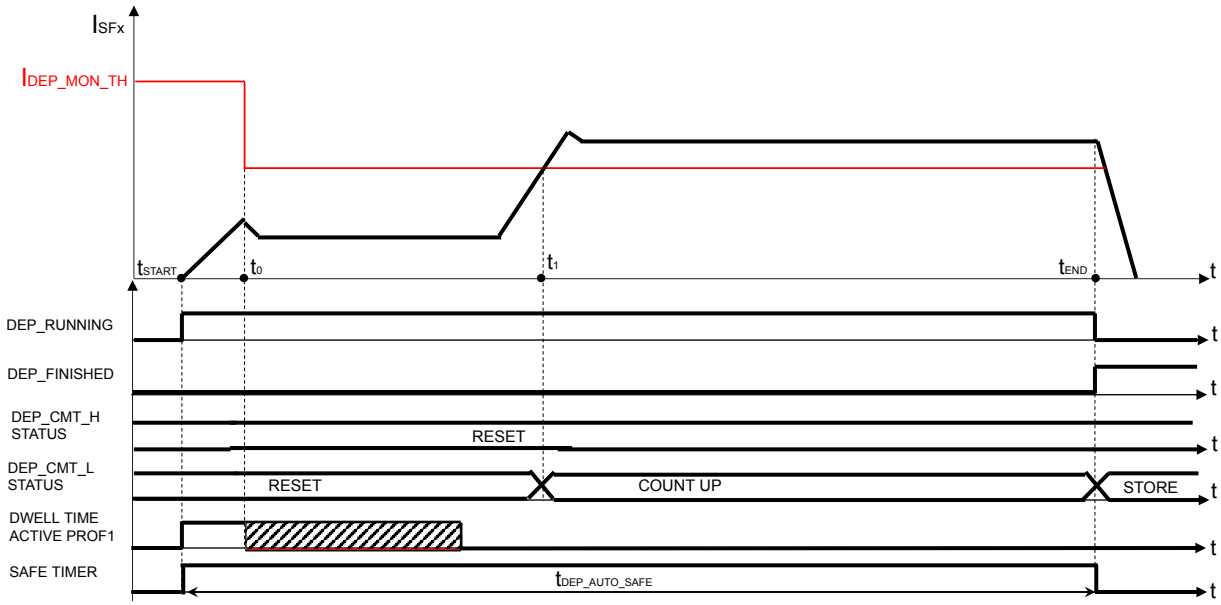
8.6.3.4 *Example 4*

See Figure 51. Channel is configured as indicated:

- Automatic dynamic deployment enabled
- PROF1: high current, $t_{DEP\_DWELL\_TIME\_P1}$ dwell time

Deployment process begins normally: primary dwell timer starts to count from t_{START} but, because of external insufficient current capability, high current level cannot be achieved in the required time, that is $I_{DEP\_MON\_TH}$ value is not reached in a time lower than $t_{DEP\_AUTO\_START}$; so at time $t_0 = t_{START} + t_{DEP\_AUTO\_START}$, HS driver automatically starts to switch to the secondary low current profile, so deployment high current monitor counter never starts counting. Safe timer continues to count but current cannot reach the low current value, so deployment low current monitor timer does not start counting; however, at time t_1, current capability recovers and reaches $I_{DEP\_MON\_TH}$ value and low current monitor counter starts to increment. As safe timer expires, at time t_{END} deployment is terminated; deployment low current monitor timer value at t_{END} is stored in DEP_CMT_L_x. Total composite dwell time is t_{END}-t_{START}, that is $t_{DEP\_AUTO\_START} + t_{DEP\_DWELL\_TIME\_P2}$.

Figure 51. Automatic dynamic deployment example 4



8.6.4 Deployment status flags

Two flags are provided via DEP_STATUS_0_7 and DEP_STATUS_8_15 global SPI frames in order to monitor deployment status:

- Deployment running flag (DEP_RUNNING_x bit): if set to 1, it indicates that a deployment event is running on a channel; SPI bit indicates the actual status at reading time.
- Deployment finished flag (DEP_FINISHED_x bit): if set to 1, it indicates that a deployment event has been performed on a channel and dwell timer is expired since last SPI reading. SPI bit is read-only and it is reset to 0 when a new deployment event is started.

There is one register per each deployment channel. In order to clarify status flag functionalities, DEP_RUNNING and DEP_FINISHED internal signal behavior is indicated in Figure 46, Figure 47, Figure 48, Figure 49, Figure 50 and Figure 51.

8.7 Diagnostics

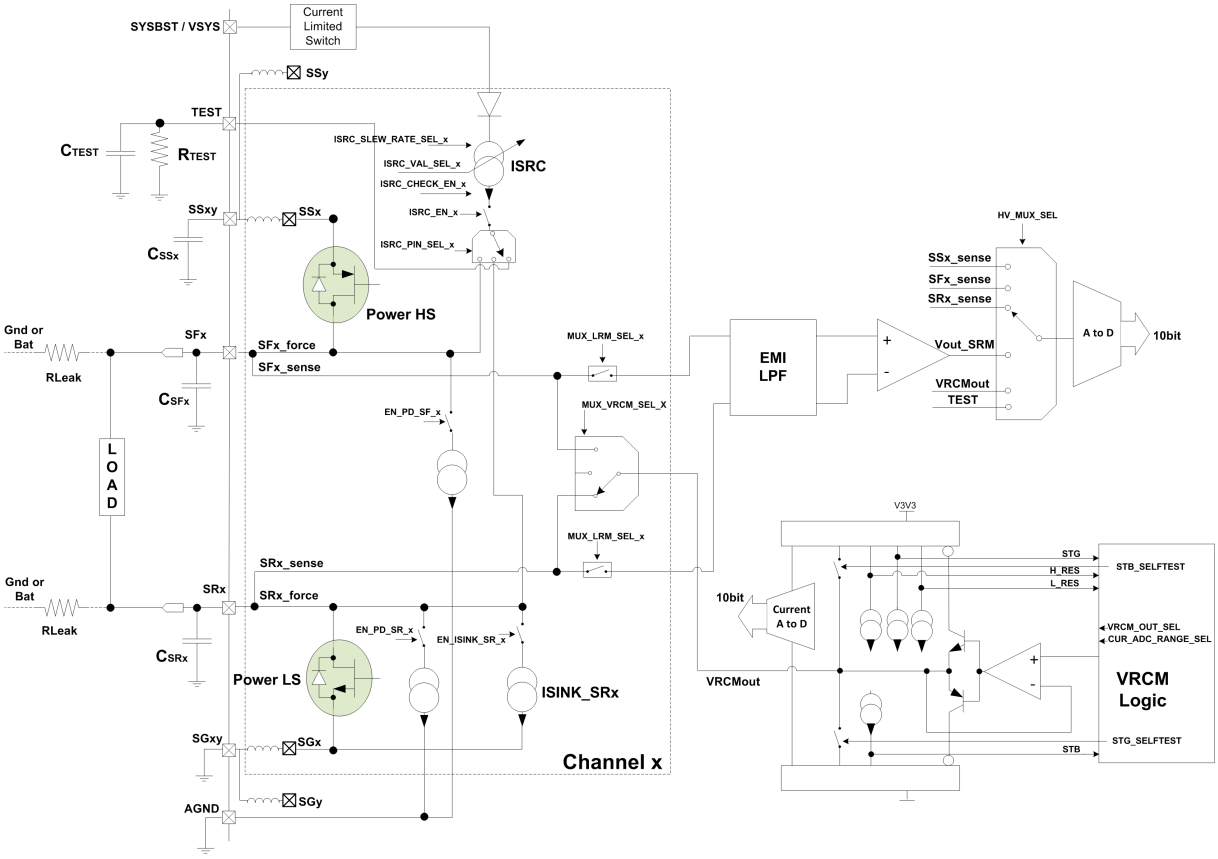
Deployment channels provide capability to perform the following set of diagnostics:

- Leakage to battery/ground diagnostic on SFx/SRx pins (LD)
- Short between loops diagnostic, supporting both standard and CSRx topologies (SBLD)
- High load resistance diagnostic (HLRD)
- Load resistance measurement through A/D conversion (LRM)
- LS/HS FET test
- LEA presence diagnostic (channels 6 and 7 only)
- Deployment voltage A/D conversions

Each channel shares a similar diagnostic circuit architecture; however, channels from 2 to 5, that is supporting CSRx topology, and from 6 to 7, that is supporting both squib and LEA load, provide additional dedicated hardware.

A general overview of deployment diagnostic circuitry available on the channels from 0 to 1 and from 8 to 15, that is squib load support only and CSRx topology not available, is shown in Figure 52.

Figure 52. Deployment diagnostic circuitry general overview - squib only, no CSRx topology



Part of the diagnostic circuits is replicated on each channel instance, while some other blocks are centralized and shared among all channels; as it will be described later, analog circuit architecture and SPI handling strategy allows a partial parallelization of diagnostic execution on a maximum of two channels, that will be referred to as A and B channel-under-test.

Here is a detailed description of the channel-replicated circuitry:

- Source current generator (I_{SRCx}), mainly used to provide an accurate diagnostic current to either SFx or SRx pin in order to perform LRM. Current generator circuit is supplied from SYSBST/VSYS pin through a current limited switch, shared among all channels; voltage back feeding to SYSBST pin due SFx/SRx pin short to battery events is avoided through a dedicated protection circuit. In order to limit power dissipation, only a single I_{SRCx} generator can be enabled at the same time in the whole device; the channel on which I_{SRCx} generator can be enabled is A channel-under-test only. Generator circuit can be controlled/configured in the following way:
  - Channel selection: used to define on which channel that the generator has to be enabled; this is done using DEP_CH_SEL_DIAG_CTRL_A 4 bit field, located in DEP_DIAG_CTRL_A global SPI register (default is channel 0).
  - SFx/SRx connection selection: used to define if generator output has to be connected to either SFx or SRx pin; this is done using DEP_ISRC_PIN_SEL bit, located in DEP_DIAG_CTRL_A global SPI register (default is SFx). Actually, generator output is connected to SFx/SRx force pad, connected to LS/HS deployment driver output as well.
  - Output current value selection: two values are available, that is I_{SRCx_H} high value, I_{SRCx_L} low value; it is configured using DEP_ISRC_VAL_SEL bit, located in DEP_DIAG_CTRL_A global SPI register (default is I_{SRCx_H}).
  - Selection of slew-rate: two configurations are available, that is controlled slew rate (SR_{ISRCx_FAST} or SR_{ISRCx_SLOW}) and not controlled slew rate; SR_{ISRCx_SLOW} and not controlled slew-rate are configured using DEP_ISRC_SLEW_RATE_SEL bit, located in DEP_DIAG_CTRL_A global SPI register (default is SR_{ISRCx_SLOW}). Additionally, SR_{ISRCx_FAST} selection is done via NVM programming (default is SR_{ISRCx_SLOW}).
  - Enable command: used to actually enable the generator circuit; this is done using DEP_ISRC_EN bit, located in DEP_DIAG_CTRL_A global SPI register.
- SRx sink current generator (I_{SINK_SRx}), mainly used to provide a robust current-limited pulldown path to SRx pin, mainly used during LRM; circuit is connected between SRx pin force pad and SGxy pin. It is allowed to have two sink generators enabled at the same time on two different channels, that is A and B channel-under-test, controlled and configured in the following way:
  - A channel selection: this is done using the same bits used for I_{SRCx} channel selection, that is DEP_CH_SEL_DIAG_CTRL_A 4 bit field, located in DEP_DIAG_CTRL_A global SPI register (default is channel 0).
  - B channel selection: this is done using DEP_CH_SEL_DIAG_CTRL_B 4 bit field, located in DEP_DIAG_CTRL_B global SPI register (default is channel 0).
  - Output current value selection: two values are available, that is $I_{SINK\_SRx\_H}$ high value, $I_{SINK\_SRx\_L}$ low value; this is configured using the same bits used for I_{SRCx} value selection, that is DEP_ISRC_VAL_SEL bit, located in DEP_DIAG_CTRL_A global SPI register (default is $I_{SINK\_SRx\_H}$). Value selection applies to both A and B channel-under-test.
  - Generator enable command on channel A: used to actually enable the generator circuit on A channel-under-test; this is done using DEP_ISINK_A_EN bit, located in DEP_DIAG_CTRL_A global SPI register.
  - Generator enable command on channel B: used to actually enable the generator circuit on B channel-under-test; this is done using DEP_ISINK_B_EN bit, located in DEP_DIAG_CTRL_B global SPI register.
- SRx and SFx pulldown current generators (I_{PD_SRx}, I_{PD_SFx}), mainly used to provide a minimum current-limited pulldown path to SRx and SFx pin respectively; circuit is connected between SRx or SFx pin force pad and AGND pin. Normally, as a diagnostic resource is enabled on a channel (channel under test), its pulldown generators are automatically disabled; by the way, it is possible to force the disable state of the pulldown generators on one or more channels, using SR_SF_PD_DIS_x bits, located in SR_SF_PD_CTRL global SPI register.

- Load resistance measurement amplifier connection switches, that allows to connect SFx and SRx pin sense pads to the input stage of the voltage amplifier used to perform load resistance measurement (shared among all channels); these switches allow to handle the extended CSRx LRM diagnostic, that is SFx-to-SFy measurement. Switches can be enabled on A channel-under-test only, using the following SPI commands:
  - A channel selection: this is done using the same bits used for I_{SRCx} channel selection, that is DEP_CH_SEL_DIAG_CTRL_A 4 bit field, located in DEP_DIAG_CTRL_A global SPI register (default is channel 0).
  - Enable command: used to actually enable the switches; this is done by writing DEP_MUX_LRM_SEL 2 bit field, located in DEP_DIAG_CTRL_A global SPI register, with the following coding:
    - “00” (default): all switches disabled
    - “01”: switch enabled in standard LRM mode, that is SFx connected to LRM amplifier positive input and SRx connected to LRM amplifier negative input
    - “10”: switch enabled in CSRx LRM mode, that is SFx connected to LRM amplifier positive input and SFy connected to LRM amplifier negative input; this configuration is accepted only when (x, y) are either (2, 3) or (4, 5)
    - “11”: not used.
- VRCM multiplexer, that allows to connect either SFx and SRx pin sense pads to the output stage of the voltage regulator/current monitor circuit (VRCM, shared among all channels), mainly used to perform leakage diagnostics; multiplexer activation can be done on B channel-under-test only, using the following SPI commands:
  - B channel selection: this is done using DEP_CH_SEL_DIAG_CTRL_B 4 bit field, located in DEP_DIAG_CTRL_B global SPI register (default is channel 0).
  - Enable command: used to actually connect the multiplexer; this is done by writing DEP_MUX_VRCM_SEL 2 bit field, located in DEP_DIAG_CTRL_B global SPI register, with the following coding:
    - “00” (default): no connection
    - “01”: mux connected to SRx
    - “10”: mux connected to SFx
    - “11”: not used

    In order to mitigate emissions, when the enable command is received the VRCM output is closed on both SFx and SRx of the selected channel for a certain time duration ($t_{ON\_VRCM\_MUX\_PARALLEL}$). This operation allows to charge the external capacitors (C_{SFx} and C_{SRx}) at the same time and to avoid emission noise due to the long wire connections on the deployment pins. After this time, the VRCM output stays connected only on the selected pin.

Here is a list of the channel-shared diagnostic circuits:

- SYSBST current limited switch, whose output is used to provide voltage supply to all the I_{SRCx} generator circuits present in the device; as its output current is lower than $I_{LIM\_DEP\_DIAG\_SW}$ limitation value, output provides a low resistance connection path to SYSBST/VSYS pin, otherwise circuit operates in current limitation mode. This circuit purpose is to avoid high current feeding to the squib/LEA load in case of malfunction/failure of the I_{SRC} generator.
- LRM differential voltage amplifier, providing a differential voltage input and a single-ended voltage output, connecting to one of the multiplexer inputs of deployment A/D converter; input is filtered against EMI with a low-pass filter with f_{LP_LRM} bandwidth.[end] Amplifier voltage characteristics is given by the following equation:

$$V_{OUT\_LRM} = V_{B\_OUT\_LRM} + G_{LRM} \times (V_+ - V_-) \quad (4)$$

  where G_{LRM} is the amplifier gain and $V_{B\_OUT\_LRM}$ is the amplifier base voltage output, measure as differential input voltage is equal to zero.

- Voltage regulator/current monitor circuit (VRCM), used in the execution of leakage diagnostics, LS/HS FET test and high load resistance diagnostic. As a regulator, VRCM circuit provides a current-limited regulation output, with the following features:
  - SPI-selectable regulation voltage, with 2 available values: $V_{O\_VRCM\_L}$ low value and $V_{O\_VRCM\_H}$ high value; it is configured using DEP_VRCM_OUT_SEL bit, located in DEP_DIAG_CTRL_B global SPI register (default is $V_{O\_VRCM\_H}$).
  - Sinking current limitation ($I_{LIM\_SINK\_VRCM}$).
  - Sourcing current limitation ($I_{LIM\_SRC\_VRCM}$).

  As a monitor, VRCM circuit provides multiple current comparators, giving an indication of VRCM output current value; here is a list of the available thresholds:
  - $I_{STB\_VRCM\_TH}$: short-to-battery threshold, used in leakage diagnostic
  - $I_{STG\_VRCM\_TH}$: short-to-ground threshold, used in leakage diagnostic
  - $I_{R\_LOW\_VRCM\_TH}$: low resistance threshold, used in high load resistance diagnostic
  - $I_{R\_HIGH\_VRCM\_TH}$: high resistance threshold, used in high load resistance diagnostic
  - $I_{STB\_LS\_FET\_TEST\_TH}$: short-to-battery modified threshold, used during LS FET test
  - $I_{STG\_HS\_FET\_TEST\_TH}$: short-to-ground modified threshold, used during HS FET test

  As an extension of the standard monitoring function, VRCM output current can be converted through a dedicated 10 bit A/D converter; relation between conversion code (10 bit signed, two's complement representation) and VRCM output current is given by the following equation:

$$CONV_{ADC\_VRCM} = -\frac{I_{O_{VRCM}}}{G_{ADC_{VRCM}}} \times \frac{512}{I_{ADC_{VRCM_{FS}}}} + CONV_{OFFSET}$$

  where I_{O_VRCM} is VRCM output current (convention for positive value: current flowing into SFx/SRx pins) and $I_{ADC\_VRCM\_FS}$ is A/D full scale conversion range; G_{ADC_VRCM} is a configurable current scaling factor, defining the overall current conversion range, that is $G_{ADC\_VRCM\_HR}$ for the high current range and $G_{ADC\_VRCM\_LR}$ for the low current range: selection is done using DEP_ADC_VRCM_RANGE_SEL bit, located in DEP_DIAG_CTRL_B global SPI register (default is $G_{ADC\_VRCM\_HR}$). Conversion is performed within $t_{CONV\_ADC\_VRCM}$ total time.
- Deployment A/D converter, used to provide a 10 bit digital conversion of voltages related to device deployment section; A/D input is connected to the required node through a dedicated multiplexer. In order to avoid saturation of high voltage internal signal, an internal voltage divider is used. 10 bit A/D voltage conversion is requested and read through DEP_DIAG_ADC_A and DEP_DIAG_ADC_B global SPI registers;[end] relation between conversion code and input voltage is given by the following equation:

$$CONV_{ADC\_DEP} = 1024 \times \frac{V_{IN\_ADC}}{V_{DEP\_ADC\_REF}} \quad (5)$$

  where V_{IN_ADC} is the A/D input voltage and $V_{DEP\_ADC\_REF}$ is A/D reference voltage. Single conversion is performed within $t_{DEP\_ADC\_CONV}$ total time.

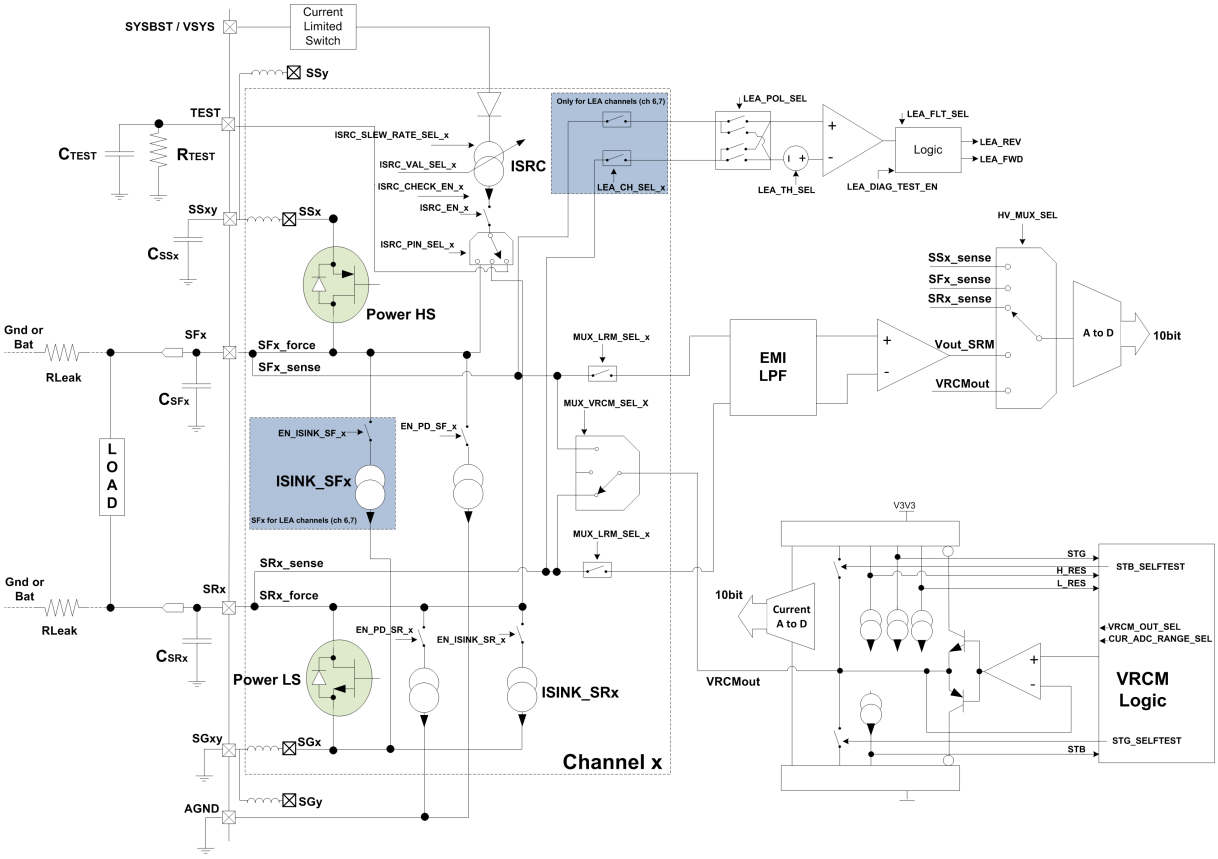
A general overview of deployment diagnostic circuitry available on the channels 6 and 7, that is squib and LEA load support, is shown in Figure 53.

Channel 6 and 7, supporting LEA load, provide the following additional diagnostic circuits:

- I_{SINK_SF} generator is connected between SFx pin force pad and SGxy pin.
- LEA presence diagnostic comparator connection switches, that allows to connect both SFx and SRx pin sense pads to the input stage of the voltage comparator (shared among all channels) used to perform LEA presence diagnostic; both switches are activated through DEP_LEA_CH_SEL bits located in DEP_DIAG_CTRL_B global SPI register.

LEA presence differential comparator is shared among the channels 6 and 7 and is used to perform LEA presence diagnostic. Comparator has V_{SFx} - V_{SRx} as differential voltage input and provides the capability to invert the polarity of its input connection through DEP_LEA_POL_SEL bit located in DEP_DIAG_CTRL_B global SPI register. Additionally, the comparator differential threshold ($V_{LEA\_TH\_L}$, $V_{LEA\_TH\_H}$) is selectable through global SPI as well using DEP_LEA_TH_SEL bit in DEP_DIAG_CTRL_B register (default is $V_{LEA\_TH\_H}$).

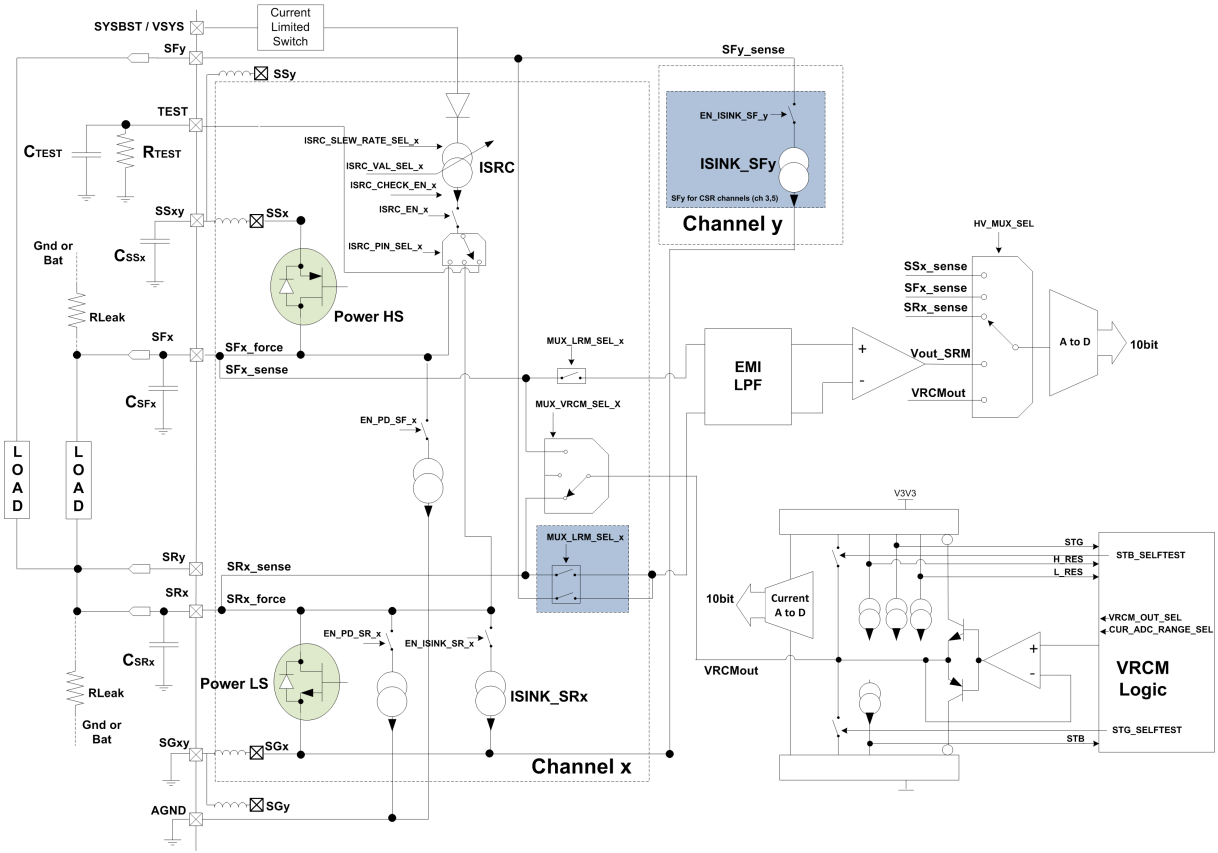
Figure 53. Deployment diagnostic circuitry general overview - squib and LEA support



I_{SINK_SF} SFx sink current generator is also present on channels 3 and 5 in order to fully support short between loops diagnostic in case common SRx topology is used, as shown in Figure 54. SFx sink current generator (I_{SINK_SF}) can be activated through DEP_ISINK_PIN_SEL_CH_5 and DEP_ISINK_PIN_SEL_CH_3 bits located in DEP_DIAG_CTRL_A global SPI register.

Information that common SRx configuration is done on channel pairs (2, 3) and/or (4, 5) is given through the dedicated bits DEP_CFG_SEL_CH23 and DEP_CFG_SEL_CH45 located in DEP_CTRL global SPI. The purpose of this bit is to control the pull-down current on each channel to be consistent with or without the common SRx topology.

Figure 54. **Deployment diagnostic circuitry general overview - squib and CSRx topology**



8.7.1 Leakage to battery/ground diagnostic on SFx/SRx pins

Before starting the test, the VRCM has to be tested and validated as described in Section 8.8 Resources check. The IC provides two different methods to make a leakage to battery/ground diagnostic on SFx/SRx pins.

Method 1

In order to perform the leakage to battery/ground diagnostic the VRCM output must be connected to the desired pin (SFx or SRx) using DEP_DIAG_CTRL_B global SPI register. By doing this, also the pulldown current on the selected pin is automatically deactivated. During the test, if no leakage is present the voltage on the selected SFx or SRx pin will be forced by the VRCM to the V_{O_VRCM} level and no current is sunk or sourced by the VRCM. If there is leakage to ground or battery, the VRCM will sink or source current trying to maintain V_{O_VRCM}. Two current comparators detect the abnormal current flow: the current exceeds the threshold ($I_{STG\_VRCM\_TH}$ or $I_{STB\_VRCM\_TH}$) for the deglitch filter time ($t_{FLT\_STG\_VRCM}$, $t_{FLT\_STB\_VRCM}$) and the related flags, DEP_DIAG_VRCM_STG and DEP_DIAG_VRCM_STB, will be given in the DEP_DIAG_STATUS_0 global SPI register. These flags are not latched and report the real time status of the comparators.

Method 2

The leakage resistance on the selected SFx or SRx pin can be calculated making two measurements:

First measurement. It is performed forcing the VRCM output voltage $V_{O\_VRCM\_H}$ on the desired pin while the VRCM output current I_{O_VRCM} is converted through the dedicated 10 bit A/D converter. The VRCM output voltage is also available through the 10 bit voltage A/D converter. The relationship from this first measurement can be given by the following equation (where V_{SHORT} is the external short voltage):

$$V_{SHORT} - \left|I_{O\_VRCM}\left(V_{O\_VRCM\_H}\right)\right| \times R_{LEAK} = V_{O\_VRCM\_H} \quad (6)$$

Second measurement. It is performed forcing the VRCM output voltage $V_{O\_VRCM\_L}$ on the desired pin while the VRCM output current I_{O_VRCM} is converted through the dedicated 10 bit A/D converter. The VRCM output voltage is also available through the 10 bit voltage A/D converter. The relationship from this second measurement can be given by the following equation:

$$V_{SHORT} - \left|I_{O\_VRCM}\left(V_{O\_VRCM\_L}\right)\right| \times R_{LEAK} = V_{O\_VRCM\_L} \quad (7)$$

From these results the microcontroller can calculate the value of the external leakage resistance R_{LEAK}, without the impact of the external short voltage:

$$R_{LEAK} = \frac{V_{O\_VRCM\_H} - V_{O\_VRCM\_L}}{I_{O\_VRCM}\left(V_{O\_VRCM\_L}\right) - I_{O\_VRCM}\left(V_{O\_VRCM\_H}\right)} \quad (8)$$

8.7.2 Short between loops diagnostic

In case a leakage to battery/ground fault is reported, the short between loops diagnostic should be run.

In order to perform the test, VRCM output must be connected to the desired pin (SFx or SRx) using DEP_DIAG_CTRL_B global SPI register; pulldown current generator on the channel-under-test is automatically disabled. Then, all the other SRx/SFx pulldown current generators, that is, the ones connected to all the channels except the one under test, can be turned off using SR_SF_PD_CTRL global SPI register. If the previously detected leakage to battery/ground fault disappears after the pulldown currents are disabled, then the channel under test has a short to another channel.

Table 547. Short between loops diagnostic decoding

Fault condition on squib channel	Leakage to battery/ground diagnostic (with I_{PD_SR}/I_{PD_SF} off on the channel under test)	Leakage to battery/ground diagnostic (with I_{PD_SR}/I_{PD_SF} off on all the channels)
No shorts	No fault	No fault
Short to battery	STB fault	STB fault
Short to ground	STG fault	STG fault
Short between loops	STG fault	No fault

8.7.3 High load resistance diagnostic

With this test the device is able to understand if the load resistance value is below 200 Ω, between 500 Ω and 2 kΩ or beyond 5 kΩ. In order to perform this test, the VRCM output must be connected on the SFx of the selected channel and the SRx sink current generator (I_{SINK_SRx}) must be enabled on the same channel using DEP_DIAG_CTRL_B global SPI register. The VRCM sources current trying to maintain V_{O_VRCM}; the current flowing from SFx will be compared to the low ($I_{R\_LOW\_VRCM\_TH}$) and high ($I_{R\_HIGH\_VRCM\_TH}$) thresholds for the related filter time ($t_{FLT\_R\_LOW\_VRCM}$ or $t_{FLT\_R\_HIGH\_VRCM}$) in order to identify if the load resistance is above or below low resistance or high resistance levels. The related flags, DEP_DIAG_H_RES and DEP_DIAG_L_RES, are read through the DEP_DIAG_STATUS_0 global SPI register. When the VRCM output is not connected, the default values are DEP_DIAG_H_RES = 1 and DEP_DIAG_L_RES = 0.

8.7.4 Load resistance measurement

The load resistance measurement is a two-step process. The following procedure is valid for the deployment channels supporting both squib and LEA load and is not valid for CSRx topology.

At first step, source current generator (I_{SRCx}) must be enabled and connected to the SFx pin of the selected channel and SRx sink current generator (I_{SINK_SRx}) must be enabled on the same channel using DEP_DIAG_CTRL_A global SPI register. The source current can be configured to either I_{SRCx_H} high value or I_{SRCx_L} low value in order to provide two different measurement range options. The LRM differential voltage amplifier must be connected in standard mode (SFx connected to LRM amplifier positive input and SRx connected to LRM amplifier negative input) using DEP_MUX_LRM_SEL located in DEP_DIAG_CTRL_A global SPI register. By doing this, also the pulldown currents on the selected SRx/SFx pin are automatically deactivated. A differential voltage is created between the SFx and SRx pin based on the source current and load resistance between the pins. The single-ended voltage output of the amplifier, $V_{OUT\_LRM\_1}$, is connected to one of the multiplexer inputs of deployment A/D converter.

The second measurement step can be performed redirecting the source current to the selected SRx pin, while keeping SRx sink current on (bypass measurement). In this way, the LRM differential amplifier and the following deployment A/D converter output the offset measurement, $V_{OUT\_LRM\_2}$.

The values of each measurement step can be requested and read through DEP_DIAG_ADC_A and DEP_DIAG_ADC_B global SPI registers. From these results the microcontroller can calculate the mathematical difference between first and second measurement to obtain the load resistance value:

$$R_{LOAD} = \frac{V_{OUT\_LRM\_1} - V_{OUT\_LRM\_2}}{G_{LRM} \times I_{SCRx}} \left(ASSUMING \;\; R_{LEAK\_SFx} >> R_{LOAD}\right) \quad (9)$$

Where R_{LEAK_SFx} is the leakage resistance on SFx pin. This calculation eliminates the offset contribution, it is tolerant to leakages and to high frequency noise on SFx/SRx lines.

The second measurement step can also be performed using a second value for the current source (I_{SRCx}) which must be enabled and connected to the SFx pin of the selected channel and SRx sink current generator (I_{SINK_SRx}) must be enabled on the same channel using DEP_DIAG_CTRL_A global SPI register.). The values of each measurement step can be requested and read through DEP_DIAG_ADC_A and DEP_DIAG_ADC_B global SPI registers and from these results the microcontroller can calculate the mathematical difference between first and second measurement to obtain the load resistance value:

$$R_{LOAD} = \frac{V_{OUT\_LRM\_1} - V_{OUT\_LRM\_2}}{G_{LRM} \times (I_{SCRx\_H} - I_{SCRx\_L})} \left(ASSUMING \;\; R_{LEAK\_SFx} >> R_{LOAD}\right) \quad (10)$$

For the deployment channels supporting the common SRx topology is valid the same procedure described above except that for the first measurement step the source current generator (I_{SRCx}) must be enabled and connected to the SFx pin of the selected channel (x = 2, 4) and SFy sink current generator (I_{SINK_SFy}) must be enabled on the coupled channel (y = 3, 5). The LRM differential voltage amplifier must be connected in the appropriate mode (SFx connected to LRM amplifier positive input and SFy connected to LRM amplifier negative input). In this case the measured load resistance will be the total combined load resistance of both loads sharing the common SRx. If a short between SFx pin and SFy pin is present the load resistance measurement result will be close to 0.

8.7.5 LS/HS FET test

This diagnostic can be performed only while the device is in DIAG STATE using DEP_CTRL global SPI register to enable the LS FET test or the HS FET test and setting the appropriate code in the TEST_CODE bit field.

Before initiating the FET diagnostics the VRCM output must be connected to the desired pin (SFx or SRx) using DEP_DIAG_CTRL_B global SPI register; VRCM high regulation selection ($V_{O\_VRCM\_H}$) must be used. When the FET diagnostic command is issued with the SPI command, DEP_DIAG_VRCM_STB and DEP_DIAG_VRCM_STG flags are cleared, the deglitch filter time is switched from the leakage to battery/ground diagnostic filter time ($t_{FLT\_STB\_VRCM}$, $t_{FLT\_STG\_VRCM}$) to the FET test deglitch filter time ($t_{FLT\_FET\_TEST}$).[end]

The VRCM will sink or source current trying to maintain V_{O_VRCM}; if the FET is working properly, this current exceeds the threshold ($I_{STG\_VRCM\_TH}$ or $I_{STB\_VRCM\_TH}$) for the filter time $t_{FLT\_FET\_TEST}$ and the driver under test is turned off immediately.

Because of the large difference between the filtering of leakage diagnostic and FET tests in order to prevent leakage detections during FET tests separate thresholds are provided. If there is a leakage fault to battery during the LS FET test and the current exceeds the threshold $I_{STB\_LS\_FET\_TEST\_TH}$ for the filter time $t_{FLT\_FET\_TEST}$ then the LS driver is turned off immediately. If there is a leakage fault to ground during the HS FET test and the current exceeds the threshold $I_{STB\_LS\_FET\_TEST\_TH}$ for the filter time $t_{FLT\_FET\_TEST}$ then the HS driver is turned off immediately.

The DEP_DIAG_VRCM_STB and DEP_DIAG_VRCM_STG flags are available on the DEP_DIAG_STATUS_0 global SPI register. The status of these flags after the FET tests is latched and can be cleared upon DEP_CTRL, DEP_DIAG_CTRL_B SPI commands.

If the current does not exceed the current threshold, the test is terminated and the driver is anyway turned off within the FET test timeout $t_{TO\_FET\_TEST}$. During the timeout period, the DEP_DIAG_FET_ON bit stating that the FET is enabled will be set and will be cleared as soon as the FET is switched back off.

For all conditions, the current on SFx/SRx pins will not exceed the VRCM current limitation value $I_{LIM\_SRC\_VRCM}$ or $I_{LIM\_SINK\_VRCM}$. During FET tests, energy available to the load is limited to less than E_{FET_TEST}. Finally, after FET test is completed, the VRCM deglitch filter time is switched from the FET test deglitch filter time to the leakage to battery/ground diagnostic filter time. In addition, before requesting a new execution of the LS/HS FET test through DEP_CTRL global SPI register, it is mandatory to reset TEST_CODE to 0000 in order to do a correct preconditioning of the digital part.

The possible results that can be found with the LS/HS FET tests are summarized in Table 548.

Table 548. Different result scenarios for LS/HS FET test

	DEP_DIAG_VRCM_STG	DEP_DIAG_VRCM_STB	Result
HS FET TEST	0	0	FET test fail
	0	1	FET test pass OR leakage to battery
	1	0	FET test disabled due to leakage to ground
	1	1	FET test pass OR leakage to battery then followed by leakage to ground
LS FET TEST	0	0	FET test fail
	0	1	FET test disabled due to leakage to battery
	1	0	FET test pass OR leakage to ground
	1	1	FET test pass OR leakage to ground then followed by leakage to battery

In the table, the state 1, 1 (DEP_DIAG_VRCM_STG = 1 and DEP_DIAG_VRCM_STB = 1) represents a special case which can occurs when a dynamic STG/STB happens after the execution of a successful HS/LS FET test and before to reset TEST_CODE.

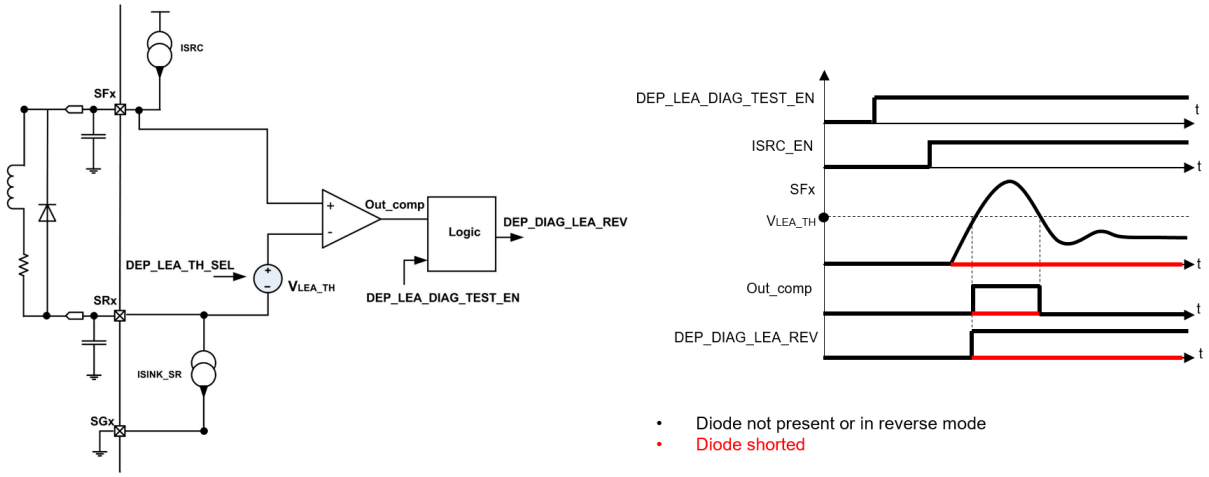
8.7.6 LEA presence diagnostic

Diagnostics functions specific to this load configuration are diode and inductance presence. Only channels 6 and 7 have these added diagnostic features.

In order to perform the test the channel under test, the intended bias direction and the comparator threshold V_{LEA_TH} must be selected through DEP_LEA_CH_SEL, DEP_LEA_POL_SEL, DEP_LEA_TH_SEL bits located in DEP_DIAG_CTRL_B global SPI register. Additionally, the not controlled slew-rate for I_{SRCx} generator must be selected using DEP_ISRC_SLEW_RATE_SEL bit located in DEP_DIAG_CTRL_A global SPI register. To initiate the test the DEP_LEA_DIAG_TEST_EN bit in DEP_DIAG_CTRL_B register must be set. By doing this, also the pulldown currents on the SRx/SFx pin are automatically deactivated.

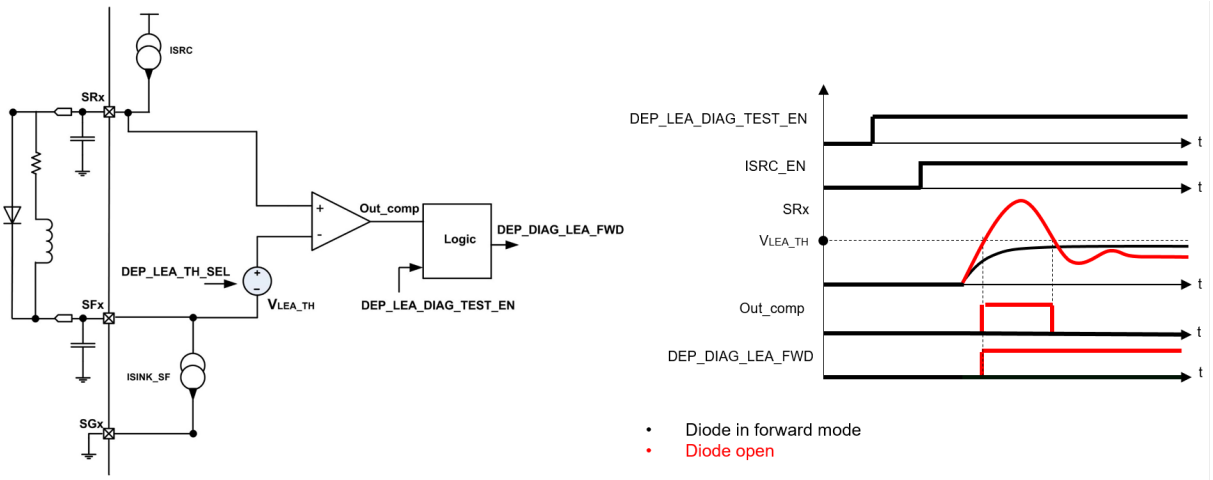
When configured for **reverse diode bias**, the I_{SRCx} current is applied to SFx pin and the I_{SINK_SRx} current will pull down the SRx pin; the I_{SRCx} and I_{SINK_SRx} currents are automatically enabled when DEP_LEA_DIAG_TEST_EN bit is set. In this case, as shown in Figure 55, the voltage across the load increases above the threshold voltage for a certain duration. This duration is influenced by the external capacitance placed at SFx/SRx pins with the response becoming more dampened with increasing capacitance. The logic validates the information with a deglitch filter ($t_{FLT\_LEA\_DIAG}$) in order to avoid spurious detections. The filter time can be programmed through DEP_LEA_FLT_SEL bits in DEP_DIAG_CTRL_B global SPI register. If the captured voltage is greater than the selected threshold, the load is diagnosed as good and the result can be read through DEP_DIAG_LEA_REV bit in DEP_DIAG_STATUS_1 global SPI register.

Figure 55. LEA presence diagnostic - reverse test



When configured for **forward diode bias**, the I_{SRCx} current is applied to SRx pin and the I_{SINK_SFx} current will pull down the SFx pin; the I_{SRCx} and I_{SINK_SFx} currents are automatically enabled when DEP_LEA_DIAG_TEST_EN bit is set. In this case, as shown in Figure 56, the voltage across the load is clamped by the diode and the slope of the curve is influenced by the external capacitance placed at SFx/SRx pins. The logic validates the information with a deglitch filter ($t_{FLT\_LEA\_DIAG}$) in order to avoid spurious detections. The filter time can be programmed through DEP_LEA_FLT_SEL bits in DEP_DIAG_CTRL_B global SPI register. If the captured voltage is less than the selected threshold, the load is diagnosed as good and the result can be read through DEP_DIAG_LEA_FWD bit in DEP_DIAG_STATUS_1 global SPI register. The status of the flags after the LEA presence test is latched and can be cleared upon DEP_CTRL, DEP_DIAG_CTRL_A, DEP_DIAG_CTRL_B SPI commands.

Figure 56. **LEA presence diagnostic - forward test**



The test is terminated after the LEA diagnostic test timeout $t_{TO\_LEA\_DIAG}$. During the timeout period, DEP_DIAG_LEA_TIP bit stating that LEA diagnostic test is in progress will be set and will be cleared as soon as the test is terminated.

8.8 Resources check

The IC provides capability to validate the following internal resources.

8.8.1 Source current generators (ISRCx)

A scaled version (I_{SRCx_TEST}) of the internal source current can be checked activating DEP_ISRC_CHECK_EN bit located in DEP_DIAG_CHECK global SPI register. The channel selection is done using DEP_ISRC_CHECK_CH_SEL bit field in the same register. In this way, a scaled version of the selected source current will be output to the TEST pin that requires an external pulldown resistor (R_{TEST}). If a short to battery with a voltage higher than SYS boost regulator output is present on SFx/SRx pins and the ISRC check is performed, the test can fail because of additional current flowing in the external resistor through ISRC mux; thus, it is mandatory to execute a leakage to battery diagnostic on both SFx and SRx pins before ISRC check test execution, ensuring that no leakage to battery is present.

8.8.2 Voltage regulator/current monitor circuit (VRCM)

The validation of VRCM goes into verifying short to battery flag and short to ground flag without connections to the SFx or SRx pins. The selection of the VRCM thresholds to be checked can be done using DEP_VRCM_SELFTEST_SEL bit in DEP_DIAG_CHECK global SPI register (0 selects $I_{STG\_VRCM\_TH}$ and $I_{STB\_VRCM\_TH}$; 1 selects $I_{STG\_HS\_FET\_TEST\_TH}$ $I_{STB\_LS\_FET\_TEST\_TH}$). The self-tests can be enabled through DEP_VRCM_STG_SELFTEST_EN and DEP_VRCM_STB_SELFTEST_EN bits in the same register and the related flags, DEP_DIAG_VRCM_STG and DEP_DIAG_VRCM_STB, will be given in the DEP_DIAG_STATUS_0 global SPI register. The VRCM can be checked verifying also the VRCM multiplexer connections to the SFx or SRx pins: the I_{SRCx} generator must be first connected to SFx pin, then the VRCM must be connected to the selected SFx pin and if the VRCM works properly the DEP_DIAG_VRCM_STB flag will be asserted. Then the I_{SINK} generator must be connected to SRx pin, the VRCM must be connected to the selected SRx pin and if the VRCM works properly the DEP_DIAG_VRCM_STG flag will be asserted.

8.8.3 Deployment comparators for auto shutdown features

An analog BIST checks all the comparators for SSx/SSxy overvoltage protection and SGxy loss protection. The comparators inputs are continuously switched so that comparators output continuously switch. In case the comparators fail, with a stuck-at failure mode, the comparators outputs stop switching and hence the failure can be detected. The BIST is automatically performed after each power-up or can be requested through DEP_ABIST_CMD in DEP_DIAG_CHECK global SPI register. The completion of the BIST can be checked through DEP_ABIST_COMPLETED in DEP_DIAG_CHECK global SPI register. If a failure of these circuits is detected the bist fails with an error indication on DEP_ABIST_ERR in the same register. The BIST on SSx/SSxy comparators works regardless of enable/disable of SSx/SSxy overvoltage protection.

The complete signal path between the deployment comparators and the functional result registers (for example DEP_DIAG_SS_OV, DEP_DIAG_SG_LOSS) can be checked through DEP_CMP_CHECK in DEP_DIAG_CHECK global SPI register. When DEP_CMP_CHECK is set to 1, all the comparators outputs change state and after the filter time ($t_{FLT\_SS\_OV}$, $t_{FLT\_SG\_LOSS}$) the related flags will be set to 1 if the all path is working properly. The test can only be performed when the analog BIST is not running.

8.8.4 Deployment dwell time and current monitor counters

The correct functionality and the duration of these counters can be checked programming the desired duration through DEP_DWELL_TIME_A in DEP_CFG_A global SPI register. The values for all the counters (DEP_DWELL_TIME_x, DEP_CMT_L_x, DEP_CMT_H_x, AUTO_SAFE_x) obtained will be the value that is configured in the DEP_CFG_A register through DEP_DWELL_TIME_A field.

The check can be executed through:

- START_CMT_H_x in DEP_CMT_H_CTRL global SPI register for high current counters.
- START_CMT_L_x in DEP_CMT_L_CTRL global SPI register for low current counters.
- START_DWELL_x in DEP_DWELL_CTRL global SPI register for dwell time counters.
- START_AUTO_SAFE_x in DEP_AUTO_SAFE_CTRL global SPI register for automatic dynamic safe time counters.

As the test procedure starts, counters are initialized to 0 and will count up; current counters value can be read in either DEP_CMT_L_x or DEP_CMT_H_x data fields for the related current counters. The counters value of the dwell time counters can be read also in DEP_CMT_L_x data field. The counters value of the safe time counters can be read in DEP_CMT_H_x data field.

The check can be run only while the device is in DIAG STATE. DEP_CMT_x registers are cleared upon START_CMT_H_x, START_CMT_L_x, START_DWELL_x, START_AUTO_SAFE_x or when the device enters in SAFING STATE.

8.8.5 Deployment disable command

The DEP_DIS_x command can disable deployment only in DEP_DISABLED state and must be checked for proper operation with the following steps:

- DEP_DIS_x = 1: this step verifies that LS/HS FET test fails. If DEP_DIAG_VRCM_STB flag does not occur for HS FET test and DEP_DIAG_VRCM_STG flag does not occur for LS FET test then DEP_DIS_x command is operating properly.
- DEP_DIS_x = 0: this step verifies that LS/HS FET test passes. If DEP_DIAG_VRCM_STB flag occurs for HS FET test and DEP_DIAG_VRCM_STG flag occurs for LS FET test then DEP_DIS_x command is operating properly.

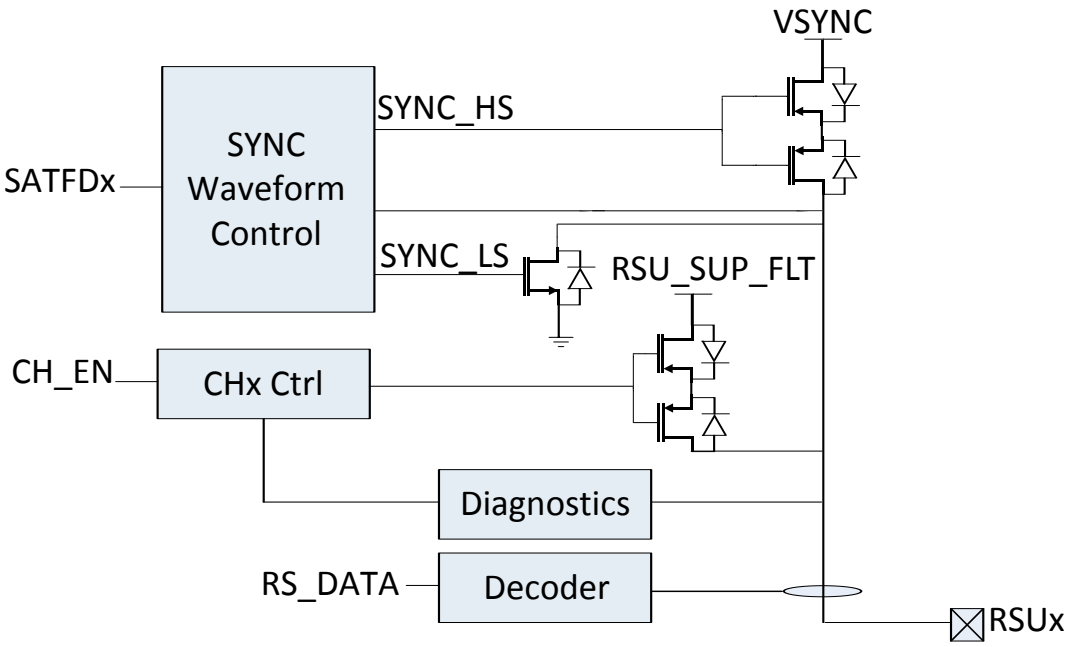
8.8.6 DEP_CMD and DEP_CMD_N registers

In DIAG STATE it is possible to check the state of DEP_CMD and DEP_CMD_N registers setting the appropriate code in the TEST_CODE bit field located in DEP_CTRL global SPI register. The result is visible on the DEP_CMD and DEP_CMD_N registers that in DIAG STATE are cleared upon reading. Additionally, the DEP_CMD and DEP_CMD_N registers are automatically reset when the device exits from DIAG STATE.

9 Remote sensor interface

The remote sensor interface is capable of supporting PSI5 protocol (synchronous mode, extended current range). A simplified block diagram of the interface is shown in Figure 57. The circuitry consists of a power interface that mirrors current flowing in the external sensor and transmits this current information to the decoder, which produces a digital value for each remote sensor channel. The main supply of the interface is RSU_SUP_FLT pin. The voltage at the RSUx pins is limited by the power interface when a RSU_SUP_FLT overvoltage occurs.

Figure 57. Remote sensor interface control block



Remote sensor configuration and control are addressed via dedicated registers (respectively, RSCRx registers and RSCTRL register) for each channel including enable, disable and sync pulse control. Configuration, control, data and fault information for each channel (RSDRx) are accessed through the RS SPI Bus. The device accommodates a total of 32 data registers (RSDRx).

9.1 PSI5 mode

Each channel is configurable to support the following PSI5 synchronous parallel protocols as described in the PSI5 airbag substandard (rev 2.3):

- P10P-250/1L (STS = 0x0)
- P10P-500/2L (STS = 0x1)
- P10P-250/2H (STS = 0x2)
- P10P-500/3L (STS = 0x3)
- P10P-500/4H (STS = 0x4)
- P16CRC-250/1L (STS = 0x5)
- P16CRC-250/1H (STS = 0x6)
- P16CRC-500/2L (STS = 0x7)
- P16CRC-500/2H (STS = 0x8)
- P20CRC-500/2L (2 low precision 10 bits data) (STS = 0xB)
- P20CRC-500/2H (2 low precision 10 bits data) (STS = 0xC)

PSI5 custom protocols:

- P20CRC-250/1H (2 low precision 10 data bits) (STS = 0xA)

- P16CRC-500/3H (STS = 0x9)

PSI5 daisy chain protocols, with communication handled by MCU trough tooth gap method

- D10P-500/3L (STS = 0xD)
- D10P-500/4H (STS = 0xE)

Each channel is configurable to support:

- PSI5 standard mode and low power mode (with reduced modulation current and reduced sync pulse amplitude) as described in the PSI5 base specification (v2.3)
- PSI5 sync pulse as described in the PSI5 base specification v2.3 with pulse shaping and a semisinus waveform to improve the EMI performance

9.1.1 Functional description

The remote sensor Interface block provides a hardware connection between the microcontroller and remote satellite sensors. Each channel is independent and is not influenced by fault conditions occurring on other device channels, such as short to ground or battery. The device supports the measurement of RSUx pins voltage through sensor ADC queue: enabling one channel at time, this feature could be used for detecting external shorts between channels. Each channel is supplied by a current limited DC voltage derived from RSU_SUP_FLT and VSYNC, monitoring the current to extract encoded data. The remote sensor modulates load current to transmit Manchester-encoded data to the receiver. The current level detection threshold for all channels is internally computed by the IC in order to adapt the detection threshold to the sensors quiescent current.

All channels can be enabled or disabled independently via SPI commands through RSCTRL register. The operational status (sensor and fault status) of all channels can be read via SPI read command of the desired channel's RSDRx register.

Received message data are stored in independent data registers that are read by the microcontroller via the remote sensor SPI interface. Four data registers per channel are used to store remote sensor messages received during timeslots 1, 2, 3 and 4 respectively. Each register is updated after a specified delay ($t_{WRITE\_EN\_DELAY}$) from the end of a valid sensor message, or with a fault response instead of sensor data if no valid data is present. The fault response is written whenever a qualified fault is present or a corrupted data is received. After data for a given RSDRx register is read via the remote sensor SPI, subsequent requests for data from this RSDRx register will result in an error response, with NO DATA bit (RSDRx register) set to "1", until new data is received.

9.1.2 Sync pulse generation and configurability

To allow for sampling synchronization of remote sensor data with software in the microcontroller, the remote sensor interface block includes sync-pulse circuitry to signal initiation of sampling in the remote sensor. The sync-pulse is output to the remote sensors in the form of a voltage pulse on the RSUx pins which defines when remote sensor sampling is to be conducted.

The higher voltage level required for the sync-pulse is sourced from the VSYNC regulator:

- For trapezoidal sync pulse shape (see Figure 58) it can be selected between two values, V_{t2_CM} and V_{t2_LPM}, by setting bit 11 (SYNC_AMPL) in RSCRx registers.
- For sinusoidal sync pulse (see Figure 59) it is fixed at V_{t2_CM}. Pulse shaping is used to limit the slew rate of the pulses to reduce EMI, allowing selection between trapezoidal and sinusoidal shape, through bit 10 (SYNC_WAVE) in RSCRx registers.

Figure 58. **Trapezoidal sync pulse**

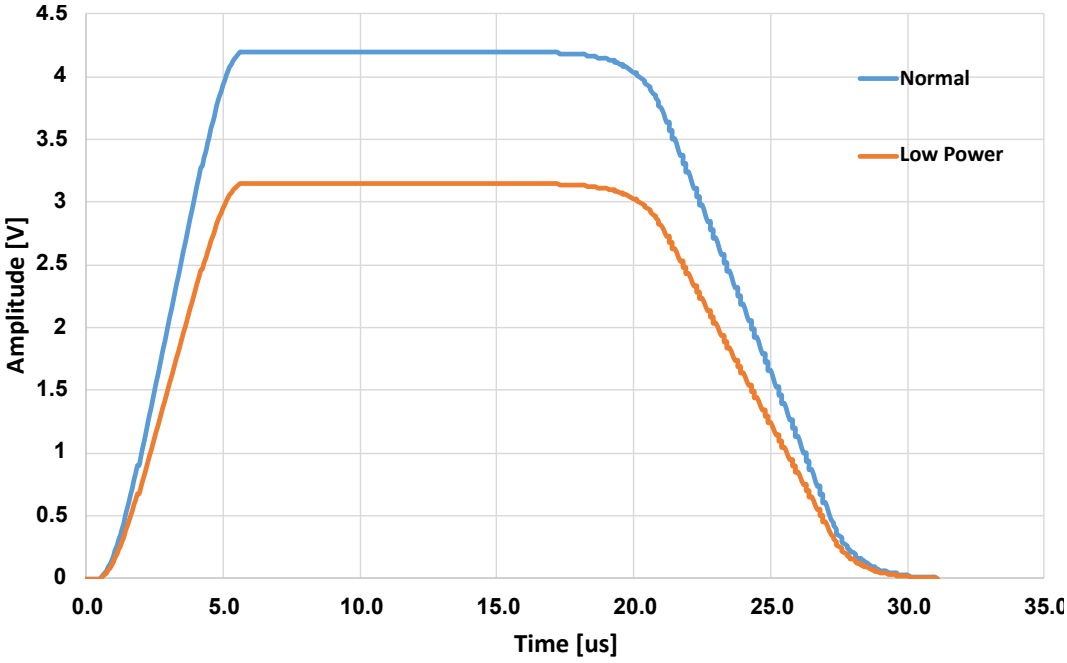
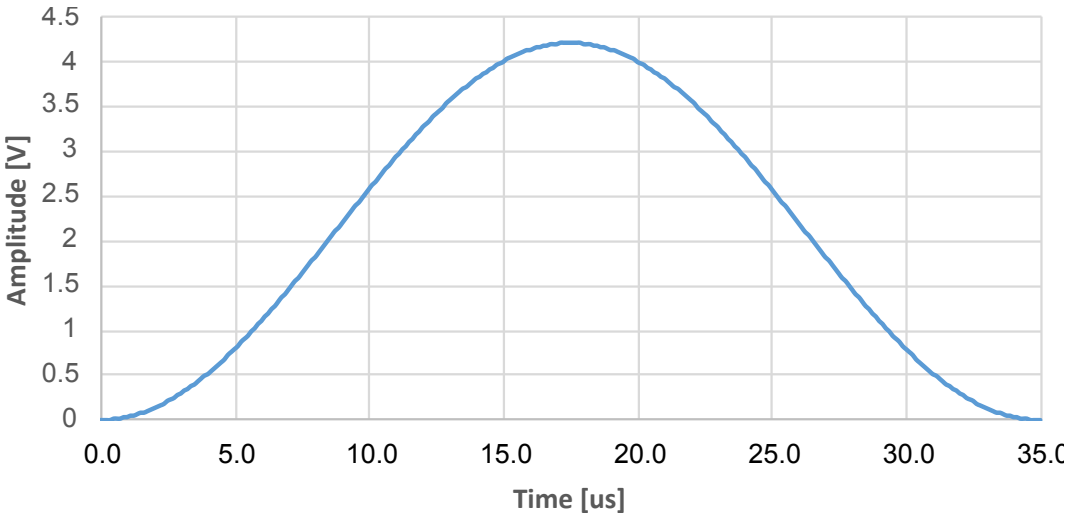


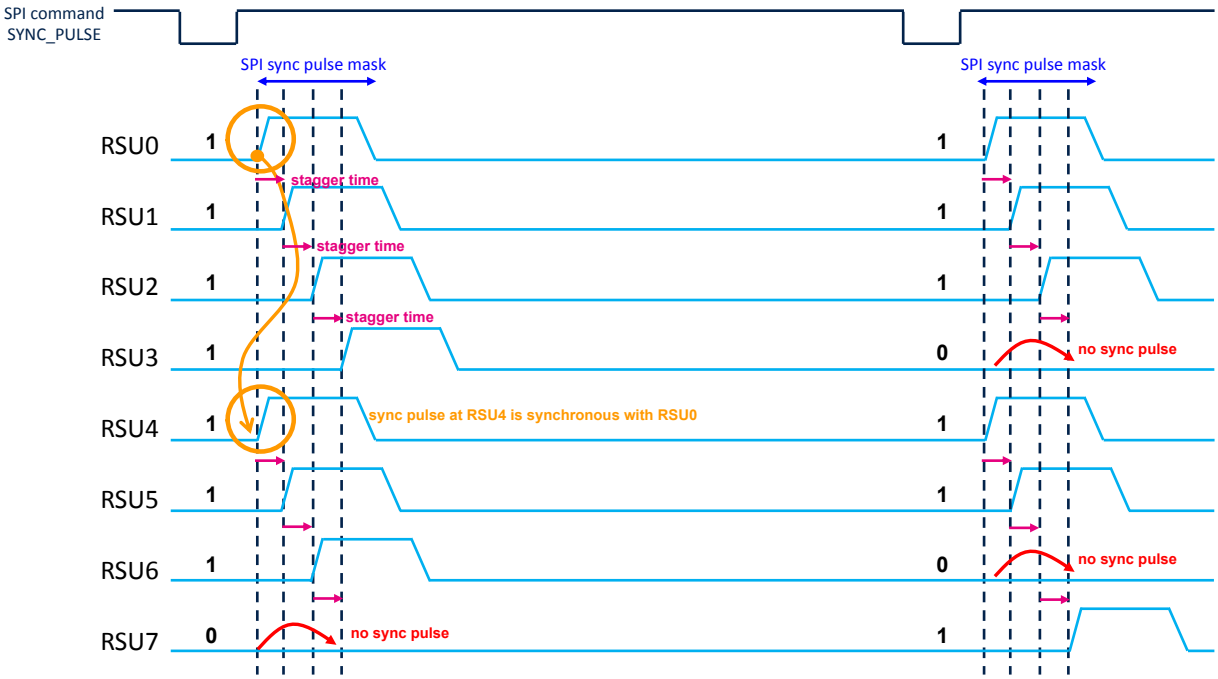
Figure 59. **Sinusoidal sync pulse**



All channels support an individual sync-pulse enable control to allow communication to the remote sensor via sync-pulse voltage modulation as described in the PSI5 v2.3 specification. The supported PSI5 protocols allow sync pulse periods of 500 µs and 250 µs; although the time slot monitoring supports only the protocols previously reported, a sync pulse with a period of 1 ms is also allowed.

If VSYNC voltage is lower than V_{VSYNC_UV}, the sync pulse generation cannot be guaranteed, but the IC will not inhibit the sync pulse generation and only the flag VSYNC_ERR on NOP frame will be asserted. The sync pulse generation is inhibited in case of SYNC_INH fault active. The microcontroller schedules the activation of the sync pulses to all channels by providing a periodic SPI command (SYNC PULSE). When the CHxSYNC bit is set to “1” in the SYNC_PULSE register, the remote sensor interface block staggers sync pulses on channels RSUx in sequence with 2 synchronous channels to reduce the average current inrush from VSYNC. As shown in Figure 60, the sync pulses are generated in sequence on the channels after a scheduled delay with respect to the previous channel (except for channels 0 and 4), and the CHxSYNC bit is automatically cleared. The staggering delay is configurable via global SPI through the STAG_SYNC_PULSE_DLY bit in the DEVICE_CTRL register, choosing between $t_{SYNC\_DLY\_SHORT}$ or $t_{SYNC\_DLY\_LONG}$. The configuration set, short or long, will be the same for all channels. The generation of a new sync-pulse is inhibited until the sync-pulse is completed on that channel and the RSUx line returns to its nominal output voltage. The remote sensor interface power control block can source and sink current to control rising and falling output voltage slew rate and is used to discharge bus capacitance at the end of the sync pulse. The pull-down device is current limited.

Figure 60. Remote sensor synchronization pulses

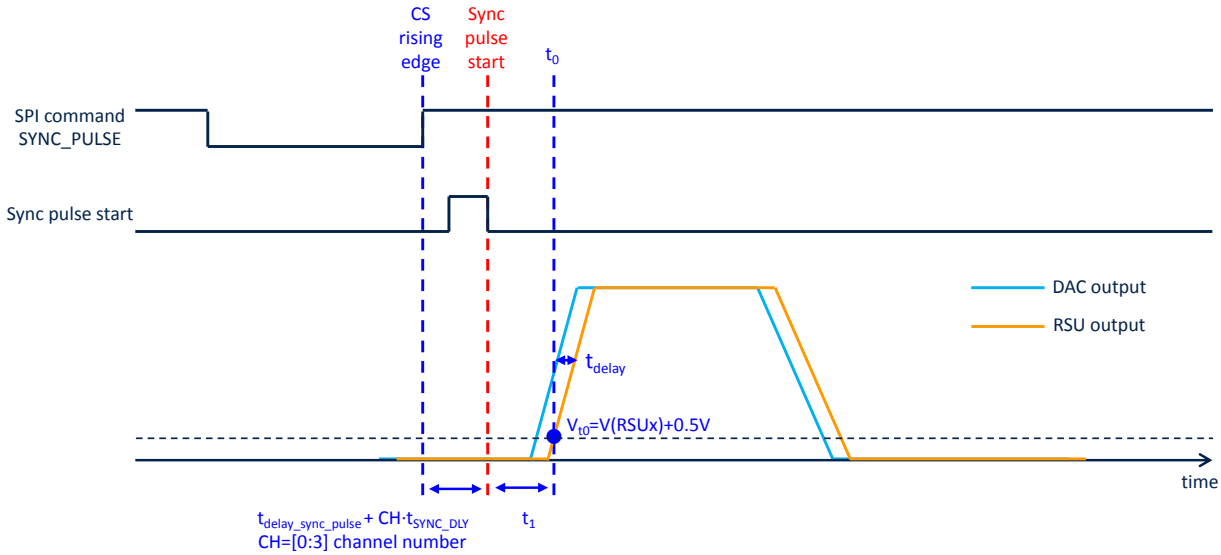


The delay represented in Figure 61, from the SPI command (that is the CS RS rising edge) for the sync pulse generation to the PSI5 standard reference time t_0, can be computed as follows:

$$t_{sync\_cmd\_dly} = t_{delay\_sync\_pulse} + CH \times t_{SYNC\_DLY} + t_1 \quad (11)$$

Where CH is the channel number [0:3] for the staggering and t_{SYNC_DLY} can be short or long according to the configuration of STAG_SYNC_PULSE_DLY bit. The delay t_1, from the sync pulse start to t_0, cumulates digital and analog contributions to reach 0.5 V on top of V(RSUx) as defined by t_0. The sync pulse start is the reference time from which the remote sensor interface starts modulating the sync pulse.

Figure 61. **Sync pulse generation**



9.1.3 Time slot control

Remote sensor interface supports up to four time slots in 500 µs sync period or two time slots in 250 µs sync period, using associated data registers. The messages received within one sync period are routed to the corresponding RSDRx register associated to each channel/time slot combination. The time slot control, that can be disabled, allows to verify if the incoming sensors messages fall within the assigned time slots. The implemented strategy is sketched in Figure 62, assuming a PSI5 protocol with four slots (for the other protocols, the last N slots can be neglected), and the distribution of the sensor data to the related RSDR registers is reported in Table 549.

Figure 62. **Time slot control**

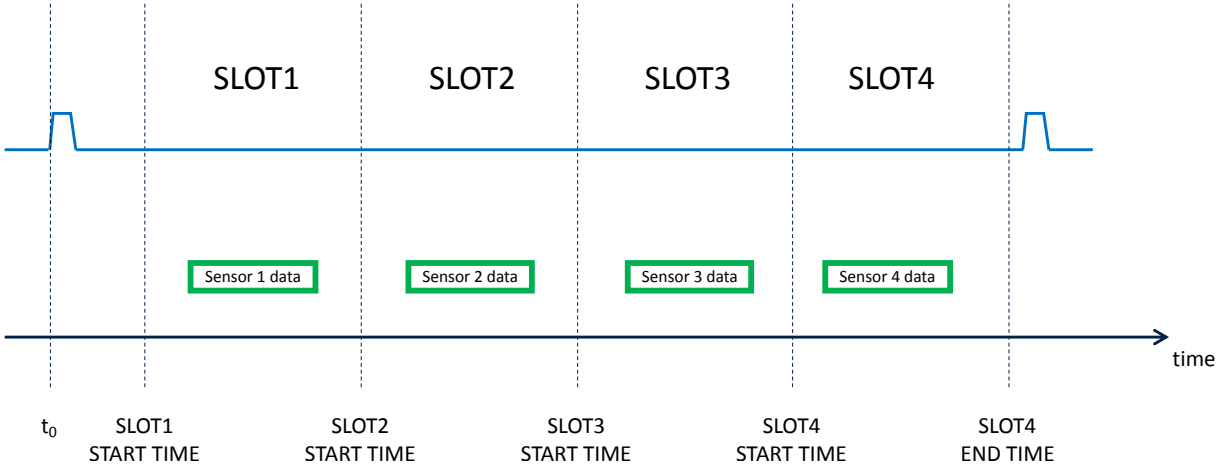


Table 549. **RSDR registers management (regular case)**

Sensor	RSDR S1 S0	RSDR data field
#1	00	Data sensor
#2	00	Data sensor
#3	00	Data sensor
#4	00	Data sensor

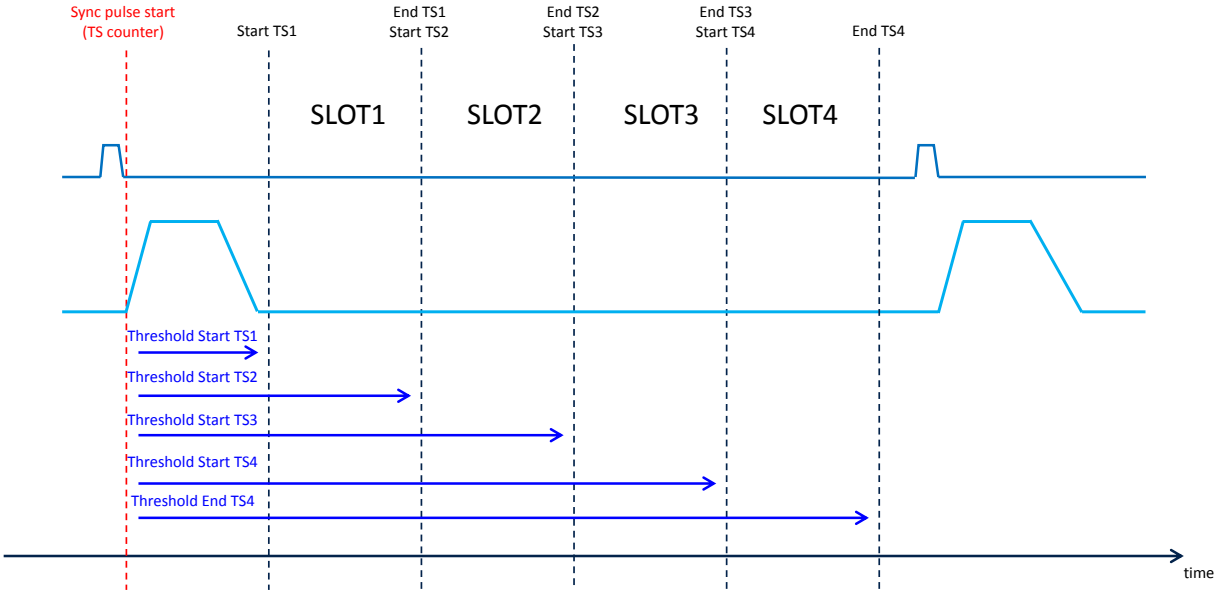
The time slot controller assumes as valid the whole time slot, which is defined from its start time to the one of the next time slots. Instead, according to the configured PSI5 protocol, the end of last time slot will be defined separately. In order to handle the different protocols in a flexible way, the start time of all slots and the end time of last one will be configurable via SPI in steps of 1 µs, with no limitations, as described in Table 550.

Table 550. Time slots management

Slot	Start Time			Stop Time		
	Threshold	Min [µs]	Max [µs]	Threshold	Min [µs]	Max [µs]
PSI5 protocols 500 µs period - 4 slots						
#00	Programmable	0	511	Start time #01		
#01	Programmable	0	511	Start time #10		
#10	Programmable	0	511	Start time #11		
#11	Programmable	0	511	Programmable	0	516
PSI5 protocols 250 µs period - 2 slots						
#00	Programmable	0	511	Start time #01		
#01	Programmable	0	511	Programmable	0	516

These values are referred to the sync pulse start (that is time slot counter reset at 0), as represented Figure 61 and Figure 63, and their configuration is affected by t_1, $t_{FLT\_DIG\_LPF}$, $t_{FLT\_PSI5\_LF/HF}$, SOM and EOM. Each programmed threshold is characterized by an uncertainly on f_{OSC} (main clock frequency with FLL enable). Since no control will be implemented on them, the consistency of the programmed values is demanded to the MCU. According to the PSI5 mode is configured (sync period and number of sensors) in the RSCRx register, the MCU has to properly program the start time of all time slots effectively used by the protocol and the end time of last slot through the 32 registers Config_STx_CHy and the 8 Config_ET_CHy on RS_SPI (5 registers per channel, 9 bits for Config_STx_Chy and 10 bits for Config_ET_CHy). Regardless the configured PSI5 protocol, the threshold programmed in the Config_ET_CHy register is always used to close the last time slot. For example, if the protocol uses only three slots, it is considered as closing time for the third time slot instead of the start time of forth slot. In case of sync pulse period is greater than 511 µs, the last time slot is closed always at 511 µs (by design, even if user sets the parameter at 516 µs, in this specific case last time slot shall anyway close at 511 µs).

Figure 63. Time slot counter control example for PSI5 protocols 500 µs period - 4 slots



9.2 Sensor data integrity

The IC ensures the sensor data integrity through different strategy and, from the PSI5 interface to the main logic, at different levels.

Each RSDRx register contains:

- a 5-bit field logical channel ID (LCID) included in the address field, used to recognize the sensor and to link the data field to the corresponding register.
- a 1-bit frame counter, which toggles at each valid sensor data.
- a 3-bit CRC computed on the whole frame, as described in SPI section.

Logical channel ID, frame counter, and CRC fields propagate through the same data path as a single item to the SPI output.

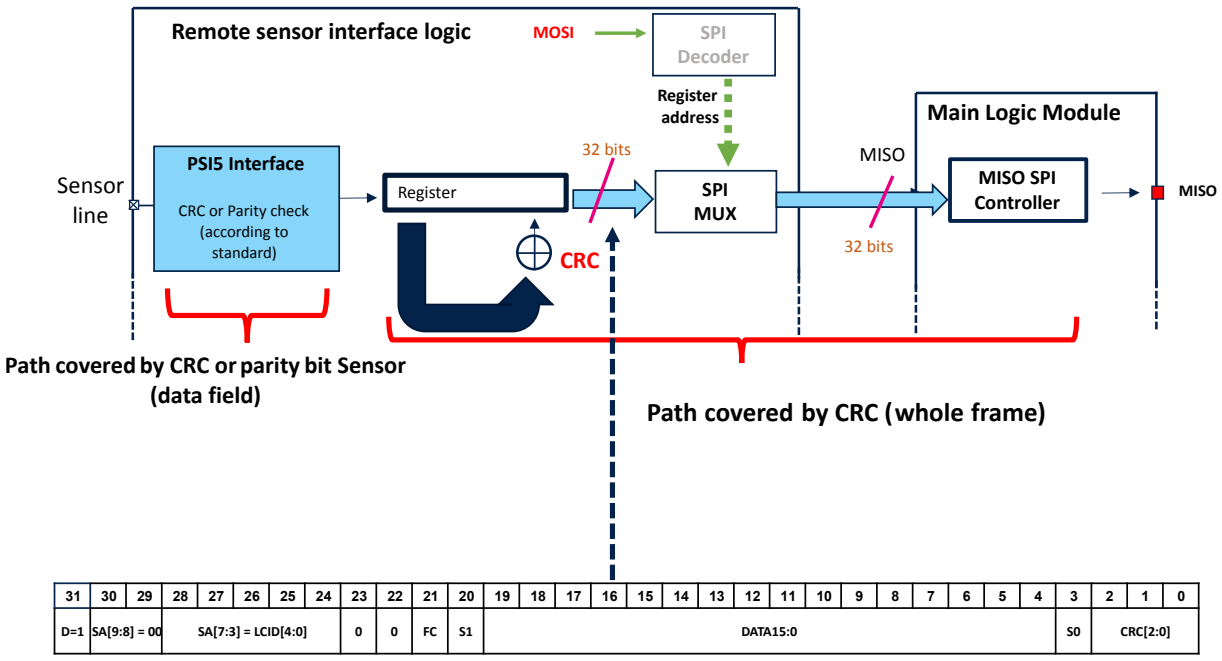
The path from sensor line to PSI5 interface is covered by checking the CRC or odd parity bit received from the sensor. The generator polynomial of the CRC is $g(x) = 1 + x + x^3$ with initialization value equal to '111', as described in the PSI5 v2.3 specification.

Once the data is decoded and Parity/CRC checked by Manchester decoder, it is stored in a register and the SPI CRC is computed on the whole frame; no further changes occur to this register through the SPI path. When the MCU read the data, the payload (DATA + CRC) is transferred to MISO_RS line and MCU can check if the CRC is correct.

A diagnostic detection method ensures that CRC and parity circuit inside PSI5 interface are properly working by sending a hard-coded 10-bit constant value in the circuits and evaluating the CRC and parity results with known hard-coded CRC and parity values. In diag state, for each channel enabled, the MCU can activate this diagnostic through the P_CRC_CHECKER_START command and check the result in the P_CRC_CHECKER_STATUS bit, both in the RSCRx register. When the MCU sends the command P_CRC_CHECKER_START = '01' or '10' it activates the diagnostic:

- With the command '01' the data is uploaded in parallel into the parity and CRC block of Manchester decoder, then parity and CRC results are checked with the expected ones and, if the interface works properly, P_CRC_CHECKER_STATUS should be 1 (pass) and it can be read in the following frame.
- With the command '10' the fault-injected data is uploaded in parallel into the parity and CRC block of Manchester decoder, then parity and CRC results are checked with the expected ones and, in this case, the P_CRC_CHECKER_STATUS should be 0 (fail) it can be read in the following frame.

Figure 64. Sensor data integrity on RSDRx register



9.2.1 Decoder detailed description

9.2.1.1 Manchester decoding

The Manchester decoder will support remote sensor communication as per PSI5 specification rev 2.3. The Manchester decoder checks start bit duty-cycle and period to determine validity, depending on the configuration programmed by the user. The Manchester decoder is kept enable during sync pulse generation in order to manage the overlapping between sync pulse generation (from sync pulse start to t4) and last slot of previous period. The expected time windows for the mid bit transitions of each subsequent bit within the received frame are determined by means of the main clock.

A Manchester decoder error occurs if one or more of the following are true:

- Two valid start bits are detected and at least one of the expected midbit transitions are not detected.
- Two valid start bits are detected and more midbit transitions than selected protocol are detected.
- When the number of bits decoded is incorrect (either too many or too few), a bit error is indicated.
- When the measured bit period is beyond ±25% to the expected one.
- When any bit error is detected (bit time, too many bits, too few bits), the decoder will revert to the minimum bit time of the selected range and the message is discarded.

When a valid message is correctly decoded, data bits are stored into the appropriate sensor data register together with the related logical channel Identifier (LCID) with status bits set to 0b00. All these errors coming from Manchester decoder and PSI5 CRC/P detected errors result in an invalid PSI5 message, readable through the remote sensor SPI as INVALID error flag in the RSDRx registers with status bits set to 0b01. Status bit combinations equal to 0b10 or 0b11 are not used for PSI5 remote sensor data packets.

Regarding the time slot control and the correct programming of thresholds, it is necessary to consider the following features of Manchester decoder:

- It is not reset by time slot monitoring, in order to recognize correct sensor data transmission or slot error fault.
- Assuming a valid sensor data transmission, the decoding starts after the recognition of start bits, therefore the start of message (SOM) is $1.5t_{Bit}$ after beginning of a PSI5 data frame.
- Assuming a valid sensor data transmission, the received communication is validated at the end of message (EOM), that is $1t_{Bit}$ after end of a PSI5 data frame.

9.2.1.2 Current sensor with auto-adjust trip current

The sensed current in the RSU power stage is internally downscaled and converted to the digital domain using a 10-bit A/D converter and digitally processed to extract both the sensor quiescent current I_B and the average delta current (that is $\Delta I_S/2$). Each remote sensor channel has an independent current sensing circuit. The current sense is disabled during SYNC pulse generation to avoid compromising current trip point.

The interface is compatible with two types of sensors: common mode and low power mode. Registers RSCRx allow the selection of sensor type through the IMOD bit. For common mode sensors (IMOD = 0) the default current threshold is I_{TH_CM}, for low power mode sensors (IMOD = 1) is I_{TH_LPM}. The threshold is used to discriminate high/low sensor sink current, and its starting value is defined in the middle point of delta current range defined by the PSI5 standard.

The delta current trip point for signal detection is auto-adjusted to the actual calculated sensor delta current, with a different starting point, according to the selected sensor type. The current trip point is dynamically determined by adding the delta current threshold to the quiescent current. The RSU current is compared against the current trip point to determine the current demodulator digital output: a logic ‘1’ represents the sensor current above the current trip point. The current demodulator output feeds the Manchester decoder. With this decoding strategy, the receiver is able to automatically adapt to different quiescent currents and to be tolerant to sensor current drifts over lifetime.

Both base and average delta current computed by the algorithm will be readable in the RSTH_CHx register. The algorithm is configurable with 2 bits in NVM:

1. BASE_LPF_FREQ_CTRL that changes the RSU base LPF sampling frequency control signal.
2. THRESH_HIST_EN that adds a hysteresis on the trip point for the delta current.

The RSU current is filtered by a digital LPF and the delay introduced on the internal current conversion is indicated by $t_{FLT\_DIG\_LPF}$. Additionally, the digital comparator output is delayed by internal deglitch filter, configurable in RSCRx register through FILT field. The total delay between the current modulation at the input of RSUx pin and the Manchester decoder is $t_{FLT\_DIG\_LPF} + t_{FLT\_PSI5\_x}$. The delay has to be taken in account configuring the time slot.

9.2.1.3 *Transfer to SPI register*

There are 4 SPI data registers RSDRx per channel related respectively to time slot1, 2, 3, 4 (from P10P-500/4H). The distribution of RSUx channels and time slots in RSDRx registers is shown in Table 551:

Table 551. Channels and time slots distribution in registers RSDRx

Register Name	RSU Channel	LCID	Time Slot Number	Time Slot Number PSI5 P20CRC
RSDR0	RSU0	0	#1 DATA	#1 DATA A
RSDR1	RSU0	1	#2 DATA	#1 DATA B
RSDR2	RSU0	2	#3 DATA	#2 DATA A
RSDR3	RSU0	3	#4 DATA	#2 DATA B
RSDR4	RSU1	4	#1 DATA	#1 DATA A
RSDR5	RSU1	5	#2 DATA	#1 DATA B
RSDR6	RSU1	6	#3 DATA	#2 DATA A
RSDR7	RSU1	7	#4 DATA	#2 DATA B
RSDR8	RSU2	8	#1 DATA	#1 DATA A
RSDR9	RSU2	9	#2 DATA	#1 DATA B
RSDR10	RSU2	10	#3 DATA	#2 DATA A
RSDR11	RSU2	11	#4 DATA	#2 DATA B
RSDR12	RSU3	12	#1 DATA	#1 DATA A
RSDR13	RSU3	13	#2 DATA	#1 DATA B
RSDR14	RSU3	14	#3 DATA	#2 DATA A
RSDR15	RSU3	15	#4 DATA	#2 DATA B
RSDR16	RSU4	16	#1 DATA	#1 DATA A
RSDR17	RSU4	17	#2 DATA	#1 DATA B
RSDR18	RSU4	18	#3 DATA	#2 DATA A
RSDR19	RSU4	19	#4 DATA	#2 DATA B
RSDR20	RSU5	20	#1 DATA	#1 DATA A
RSDR21	RSU5	21	#2 DATA	#1 DATA B
RSDR22	RSU5	22	#3 DATA	#2 DATA A
RSDR23	RSU5	23	#4 DATA	#2 DATA B
RSDR24	RSU6	24	#1 DATA	#1 DATA A
RSDR25	RSU6	25	#2 DATA	#1 DATA B
RSDR26	RSU6	26	#3 DATA	#2 DATA A
RSDR27	RSU6	27	#4 DATA	#2 DATA B
RSDR28	RSU7	28	#1 DATA	#1 DATA A
RSDR29	RSU7	29	#2 DATA	#1 DATA B
RSDR30	RSU7	30	#3 DATA	#2 DATA A

Register Name	RSU Channel	LCID	Time Slot Number	Time Slot Number PSI5 P20CRC
RSDR31	RSU7	31	#4 DATA	#2 DATA B

For example:

- With the protocol P10P-500/4H, all the registers are used.
- With the protocol P10P-500/3L, the register related to the time slot 4 will not be used.
- In P20CRC 10 + 10 bits low precision data, 2 SPI registers are associated to one PSI5 time slot.
- 10 bit sensor data from all PSI5 messages are left-aligned in the data field of SPI register.

9.3 Remote sensors interface faults

Table 552. Remote sensor interface error bits definition

Flag	Description	Setting condition	Clearing condition	Fault priority	Channel behavior
CH_OFF (E9)	Channel OFF	STG = 1 | RSTEMP = 1 | CHxEN = 0	Fault reported until SPI command to enable switch channel ON	1	Channel is turned OFF. Continuously updated.
RSTEMP (E8)	Over temperature	Over temperature condition detected	Fault reported until SPI command to disable switch channel OFF	1	Channel is turned OFF when fault is qualified
STG (E7)	Short to GND	Total current measured at ADC output higher than I_{STG} threshold	Fault reported until SPI command to disable switch channel OFF	1	Channel is turned OFF when fault is qualified
SYNC_INH (E6)	Sync pulse inhibited	Total current measured at ADC output higher than I_{STG} threshold	Fault reported until SPI command to switch disable channel OFF or upon SPI read if fault is not present or new valid data received	1	Sync pulse generation inhibited while fault is present
STB (E5)	Short to battery	Channel voltage above detection threshold	Fault reported until SPI command to disable switch channel OFF or upon SPI read if fault is not present or new valid data received	1	Channel output disconnected while fault is present
CURRENT_HI (E4)	Leakage to ground	Average quiescent current, calculated from adaptive algorithm, higher than ILKGG threshold	Fault reported until SPI command to switch disable channel OFF or upon SPI read if fault is not present or new valid data received	1	None
INVALID (E2)	Manchester or parity/CRC error	In case a message is received with valid start bit and wrong number of bit, or parity / CRC error	Fault reported until SPI command to disable switch channel OFF or upon SPI read if fault is not present or new valid data received	2	None
SLOT (E1)	Slot error	In case a message is received out of a valid time slot window	Fault reported until SPI command to disable switch channel OFF or upon SPI read if fault is not present or new valid data received	2	None
NODATA (E0)	No data	SPI readout and no other error present	Valid data received.	3	None

Table 553. RSDRx error flags

S1	DATA[15:0]										S0
0	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0	1
	CH_OFF	RSTEMP	STG	SYNC_INH	STB	CURRENT_HI	X	INVALID	SLOT	NODATA	

9.3.1 Thermal shutdown

Each output is protected by an independent over-temperature detection circuit that is detected only in case of short ground condition. Should the thermal protection fault be triggered, the output stage is disabled and the RSTEMP fault code is set in DATA field of the corresponding RSDRx register. The error flag is cleared when the sensor channel is disabled by sending a SPI command (even though the channel was already disabled due to the temperature fault) to the corresponding bit in RSCTRL register, then the channel can be re-enabled by the user.

9.3.2 Short to ground and current limit

Each output is short circuit protected by an independent current limit I_{LIM_RSU}. When the output current level reach or exceed the I_{STG} value out of the sync pulse generation for a time period greater than the configurable $t_{FLT\_OCTH\_RSU\_SHORT}$ or $t_{FLT\_OCTH\_RSU\_LONG}$, the remote sensor output stage is disabled. When the output is turned off due to current limit, the STG fault code is set in DATA field of the corresponding RSDRx sensor data register. The error flag is cleared when the sensor channel is disabled by sending a SPI command (even though the channel was already disabled due to the STG fault) to the corresponding bit in RSCTRL register, then the channel can be re-enabled by the user.

In order to fulfill the blanking time requirement at channel activation per PSI5 specification, a dedicated masking time $t_{BLK\_OCTH\_RSUx}$ is applied to the current limitation fault detection each time a channel is activated, in order to avoid false current limit detection for in-rush current that occur at sensor power-up. This masking time is selectable between two values, $t_{BLK\_OCTH\_RSU0}$ (5 ms) and $t_{BLK\_OCTH\_RSU1}$ (10 ms), through bit BLKT_SEL in corresponding RSCRx register. During the blanking time, the STG filter is kept under reset and the total time to disable the channel is $t_{BLK\_OCTH\_RSUx}$ plus $t_{FLT\_OCTH\_RSU\_SHORT/LONG}$.

9.3.3 Sync pulse inhibition

The sync pulse generation will be inhibited if the output current level exceeds the I_{STG} value before the sync pulse generation for a time period greater than $t_{FLT\_SYNC\_INH\_RSU}$. The SYNC_INH fault code is set in DATA field of the corresponding RSDRx sensor data register, and is cleared upon reading the register, receiving a new data or disabling the channel through the corresponding bit in RSCTRL register.

9.3.4 Short to battery

All outputs are independently protected against a short to battery condition. Short to battery protection disconnects the channel from its supply rail to guarantee that no adverse condition occurs within the IC. The short-to-battery detection circuit has input offset voltage to prevent disconnecting the output under an open circuit condition. A short to battery is detected when the output RSUx pin voltage increases above RSU_SUP_FLT + $V_{RSU\_STB\_OS}$ supply pin voltage for a time longer than t_{STBTH}. During the sync-pulse, the comparator output is masked, but in case of RSUx pin higher than V_{VSYNC} + $V_{RSU\_STB\_OS}$, the reverse current path is disconnected. The channel in short to battery is not shut-down by this condition. The STB fault code is set in DATA field of the corresponding RSDRx sensor data register and is reset upon reading the register, receiving a new data or disabling the channel through the corresponding bit in RSCTRL register.

9.3.5 Leakage to ground

A leakage to ground is detected when the RSUx output base current exceeds I_{LKGG} (typ 42 mA) for a time longer than $t_{FLT\_LKG\_RSU}$. The CURRENT_HI fault code is set in DATA field of the corresponding RSDRx sensor data register and is cleared upon reading the register, receiving a new data or disabling the channel through the corresponding bit in RSCTRL register. The faulted channel is not shut-down due to this fault.

9.3.6 Invalid PSI5 message

When the number of bits decoded is incorrect (too many or too few), INVALID fault code is set in DATA field of the corresponding RSDRx sensor data register. When any bit error is detected, the decoder will revert to the minimum bit time of the selected range and the message is discarded.

The INVALID code is set in case any combination of the following errors occurs:

- Data length error.
- Parity or CRC Error of received remote sensor message.
- Bit time error (a data bit edge is not received inside the expected time window).

9.3.7 Invalid time slot

The time slot monitoring verifies that the transmission of a sensor data starts and ends within the assigned time slot, otherwise a slot fault code is set in DATA field of the corresponding RSDRx sensor data register.

Some possible cases, and the related system behavior, are presented in Figure 65 and Table 554 below. For each channel, the time slot monitoring can be disabled by setting TS_DIS = 1 in the RSCRx register.

Figure 65. Time slot and faults priority management

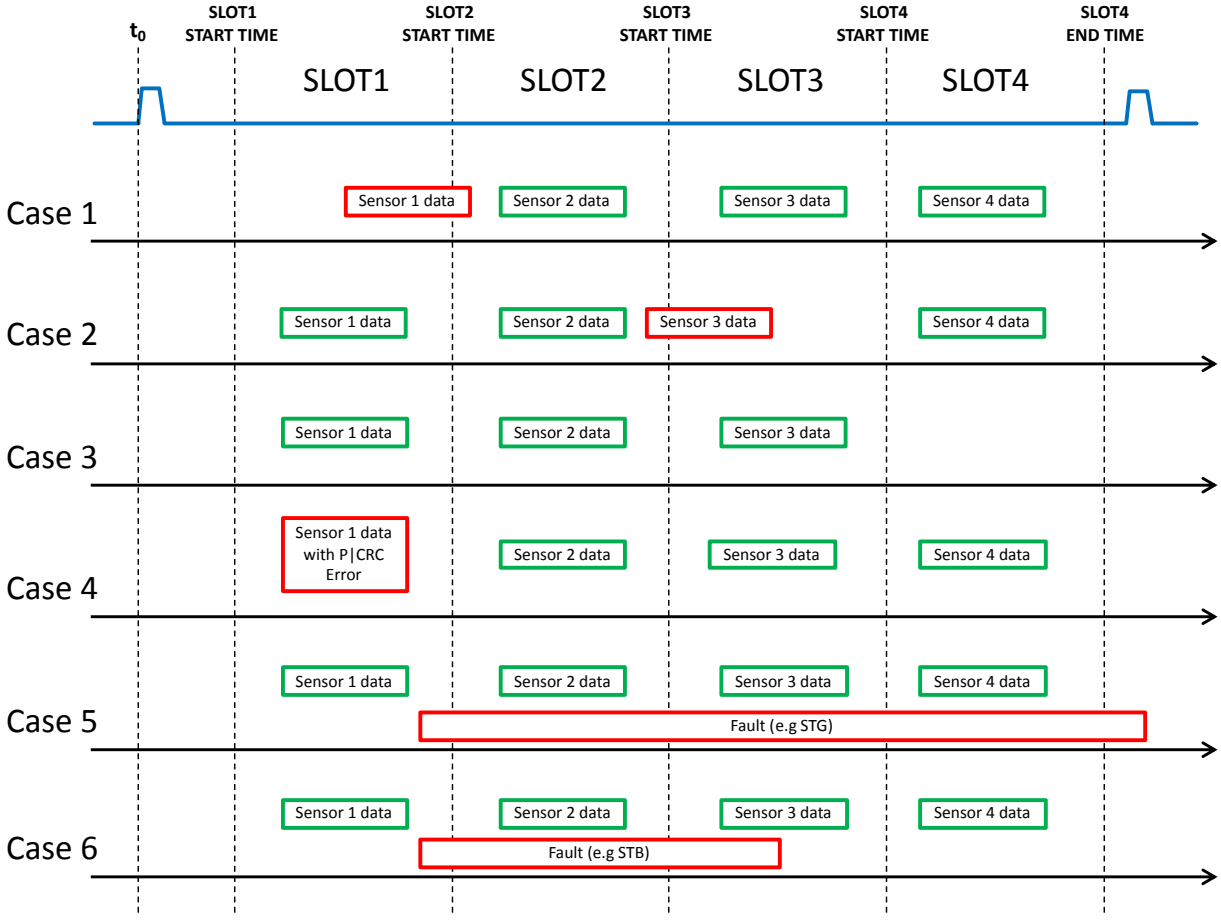


Table 554. **Scenarios handling**

Case	Sensor	RSDR s1 s0	RSDR Data field
#1	#1	01	SLOT
	#2	00	Data sensor
	#3	00	Data sensor
	#4	00	Data sensor
#2	#1	00	Data sensor
	#2	00	Data sensor
	#3	01	SLOT
	#4	00	Data sensor
#3	#1	00	Data sensor
	#2	00	Data sensor
	#3	00	Data sensor
	#4	01	NODATA
#4	#1	01	INVALID
	#2	00	Data sensor
	#3	00	Data sensor
	#4	00	Data sensor
#5	#1	00	Data sensor
	#2	01	STG
	#3	01	STG
	#4	01	STG
#6	#1	00	Data sensor
	#2	01	STB
	#3	01	STB
	#4	00	Data sensor

9.3.8 Channel OFF

This flag CH_OFF is continuously updated based upon the ON/OFF state of the channel.

9.3.9 Fault priority management

The diagnostic faults, indicated with **priority 1** in Table 552, mask the sensor data decoding, even when a valid modulation is applied to the interface current. The faults with **priority 2** are detected from the data decoding and are overwritten in case of a valid sensor data received in the assigned time slot. The NO_DATA fault is the default state for RSDRx register and it is overwritten in case of RSDRx error flags or a **higher priority** fault is detected.

10 DC sensor interface

DC sensor interface supports with a variety of positioning sensors such as hall-effect, resistive or simple switches with the following parameters:

- Resistive sensor: 50 Ω to 5 KΩ
- Hall-effect sensor: 1.5 mA to 40 mA

10.1 Channel overview

The primary voltage supply of DC sensor interface is SYSBST pin. The channel is configurable through DCS_ENGx_CTRL registers. The output voltage is selectable between three options: $V_{OUT\_DCS\_SYSBST}$, $V_{OUT\_DCS\_HIGH}$ or $V_{OUT\_DCS\_LOW}$ through DCS_VOUT_SEL_ENGx field. $V_{OUT\_DCS\_LOW}$ and $V_{OUT\_DCS\_HIGH}$ configurations are regulated with current limit selectable between $I_{LIM\_DCS\_LOW}$ and $I_{LIM\_DCS\_HIGH}$ through ILIM_ENGx bit. When selecting $V_{OUT\_DCS\_SYS}$ as the output voltage, the channel works as switch connected to SYSBST protected with a series diode and the current limit is fixed to $I_{LIM\_DCS\_SYSBST}$. The $V_{OUT\_DCS\_SYSBST}$ voltage is typically used to ensure connection integrity between the sensor and ECU. Measurements of DCSx pin voltage and current are provided to allow sensor resistance measurement.

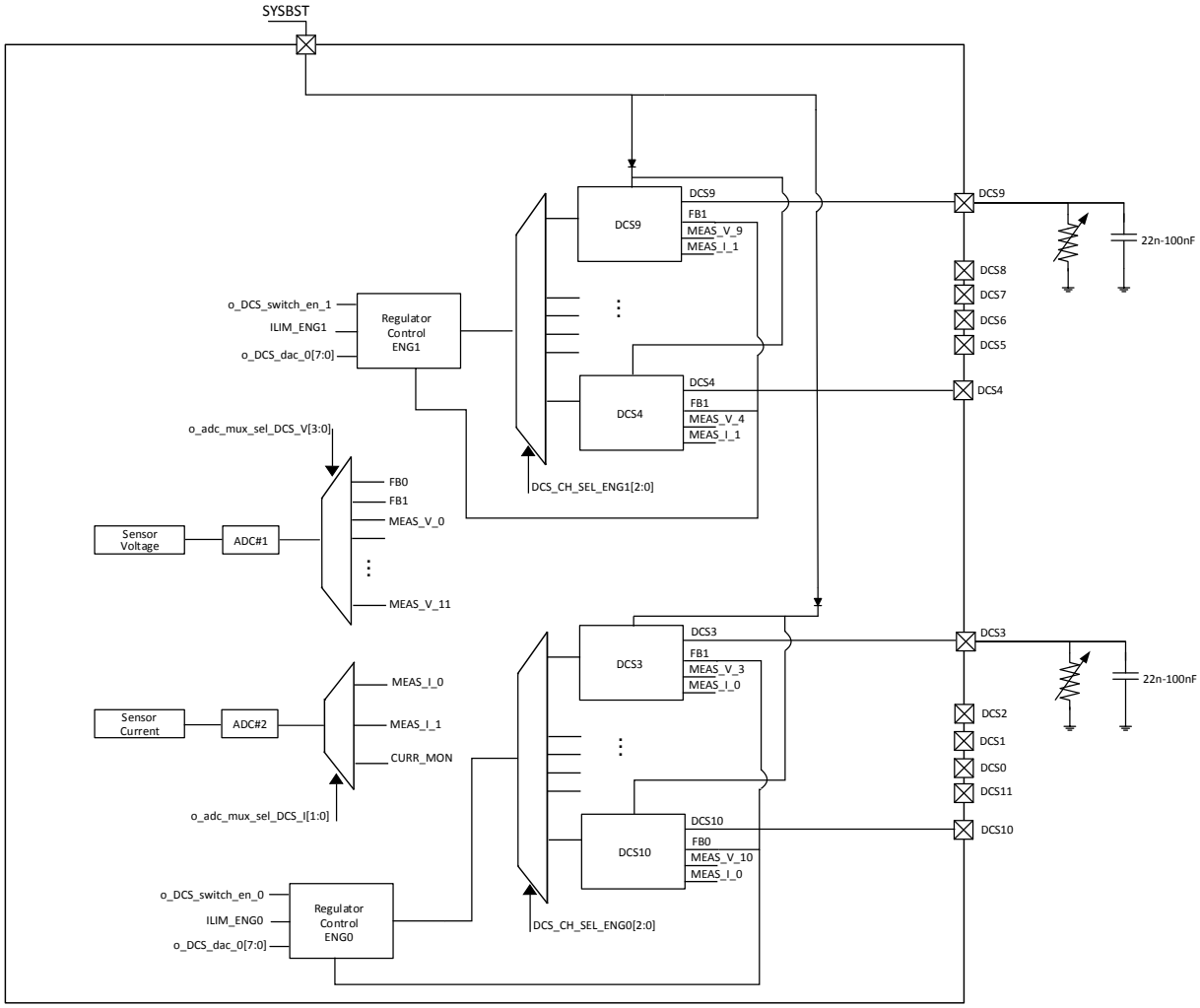
In case of hall-effect sensors, a single current measurement is processed. The current load needed for regulating the pin is internally reflected to a reference resistance, whose voltage drop is then measured through the internal ADC converter.

When resistive or switch sensors are used, a more complex measurement is performed. In a first step, the current information as above described is provided. Then, also the information on the voltage level achieved on the output pin is provided via ADC. By processing these two values, the MCU can understand the resistive value. The DCSx voltage is internally rescaled by 2 voltage dividers into the ADC converter voltage range. Additionally, a positive voltage offset is internally applied to the scaled voltage in order to allow voltage measurement capability for DCSx down to -1 V.

In order to get accurate resistive information even in case of an external ground voltage shift on the sensor of up to ±1 V, the voltage measurement step actually needs two DCSx voltage measurements: a first voltage measurement has to be done with selection of $V_{OUT\_DCS\_HIGH}$ voltage at the output channel, and a second one with $V_{OUT\_DCS\_LOW}$ voltage. The difference between the two measurements cancel out the ground offset.

The interface section is split into two independent engines: Engine0 selectable through DCS_CH_SEL_ENG0 and Engine1 selectable through DCS_CH_SEL_ENG1. To limit the system power dissipation, only two channels, one per engine, can be enabled simultaneously. A high-level diagram is shown in Figure 66.

Figure 66. **DC sensor interface block diagram**



Upon receiving a configuration change on DCS_ENGx_CTRL, the output is turned off before restarting the channel with the new configuration, and it enables a slew rate limited strong pull-down current, $I_{PD\_STR\_DCS}$, to properly discharge the external circuit for the time $t_{PD\_STR\_DCS}$.

The strong pull-down can be also activated through SPI for a time $t_{PD\_STR\_DCS}$ on channels off by selecting the desired channel on the STRONG_PD_EN_ENGx field (DCS_ENGx_CTRL register). This command is masked if the channel is active or another strong pull-down requested through command on the same engine is active.

An additional weaker pull-down, I_{PD_DCS}, is used to actively keep all DC sensor channels discharged while the device is enabled. This weak pull-down is active by default and will be disabled when one of the following cases is met:

- Voltage source active on channel
- Voltage extended conversion in progress on engine
- SPI configuration DCS_PDCURR_ENGx = ’1’

In addition, the sensor interface has an integrated passive resistive pull-down on each channel, R_{PD_DCS}, to keep all channels discharged while the device is off.

The channel is enabled or disabled directly by the user unless the automatic switch off function is enabled through DCS_AUTO_SWITCH_OFF in DCS_DIAG_CFG register which will automatically disable the channel upon completing the measurement (valid only for the requests on a channel selected). This can be useful in reducing or preventing thermal conditions when performing current or resistance measurements.

Measurements are performed with multiple SPI communications. One communication is needed to activate the channel and turn off the previous channel. Channel output pin voltage is slew rate controlled during activation and deactivation. When the output is stable, another communication initiates simultaneous sampling of voltage and current on the activated channel on 2 dedicated ADCs.

The DC interface is protected against short to battery by protection diode on supply, the condition can be monitored with the voltage ADC.

10.2 Cross-connection check

The device also provides capability to cross check outputs for detecting shorts between channels. This is achieved by setting a threshold and send the request on DCS_ADC_A. An internal state-machine sequentially sampling each channel and comparing them to the threshold set in XCONN_THRESH field in DCS_DIAG_CFG register in global SPI. The threshold set is based on the V_{EXT} conversion range (-1.5 V to 20.5 V). If higher, '1' is set in output bit position. If lower, '0' is set in output bit position. The total time required to complete the automated diagnostic loop is $t_{CROS\_CONN\_x}$ and depends on the configuration of DCS_MEAS field. If the DCS_AUTO_SWITCH_OFF = 1, the enabled channel is turned off when all conversions are done.

The output of cross-connection check is located in DCS_ADC_A and DCS_ADC_B and with the structure shown in Table 555.

Table 555. Cross-connection output

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DCS_ADC_A																
MOSI	x	x	x	x	x	x	x	x	x	x	x	0x03				
MISO	NEWDATA_A	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0	0x03				
DCS_ADC_B																
MOSI	x	x	x	x	x	x	x	x	x	x	x	0x03				
MISO	NEWDATA_B									CH11	CH10	0x03				

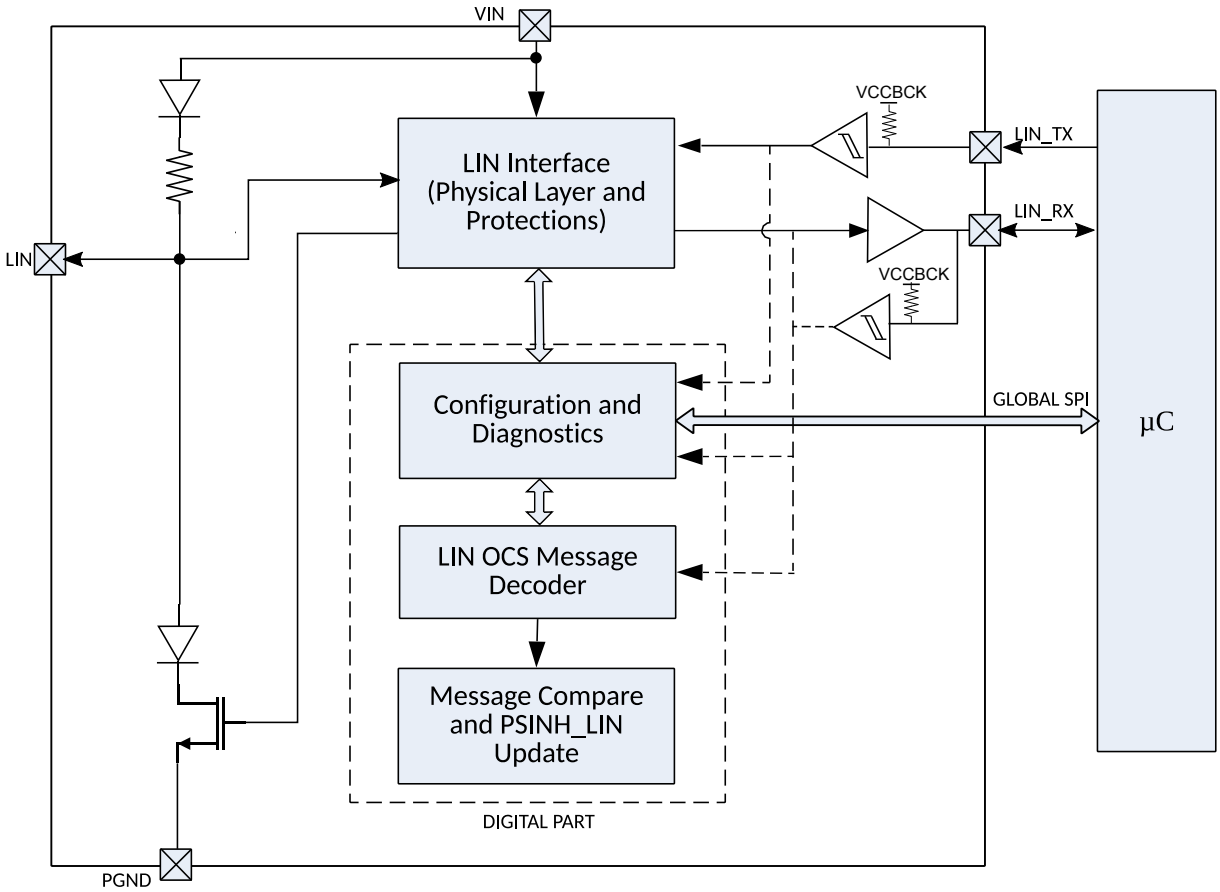
11 LIN interface and decoder

11.1 General overview

LIN interface is compliant to LIN specification rev 2.2A and it is compatible with K-LINE specification (ISO9141), with a baud rate between 400 bit/s (not monitored) to 20 Kbit/s. The full module provides both the physical layer (transmitter/receiver) and a specific communication digital decoder, mainly focused on handling occupant classification system (OCS) communication contributing to passenger deployment loop inhibit status generation. OCS is guaranteed within baud rate higher than 1 Kbit/s.

A simplified block diagram is shown in Figure 67.

Figure 67. LIN interface block diagram



Interface circuit involves three device pins:

- LIN: analog connection of transmitter/receiver circuit to the LIN bus line.
- LIN_TX: digital input used to drive the transmitter circuit. LIN_TX = 0 puts bus in dominant state, LIN_TX = 1 puts interface in recessive state. Pin is provided with an internal 100 kΩ resistive pull-up and it is internally monitored for potential driving anomalies.
- LIN_RX: digital input/output used to provide received data to internal/external decoder for processing. LIN_RX = 0 is received dominant state, LIN_RX = 1 is received recessive stat. pin is internally monitored for potential behavior anomalies.

Interface operation mode can be configured with the 2 following bits located in LIN_CFG register on global SPI:

- TX_RX_EN: if set to 1, it enables the interface transmitter and receiver.
- DEC_EN: if set to 1, it enables the internal message decoder; in this case if the TX_RX_EN is set to 0, the LIN_RX pin is set as input and the decoder can work with an external transceiver, otherwise the internal transceiver is used.

After power-up, default state for both bits is 0, that is both transmitter and receiver are disabled.

The analog transmitter/receiver circuit is supplied from both VIN pin and by the internal low voltage linear regulators; transmitter power ground is connected to PGND pin. In case of loss of analog circuit supply (VIN disconnected or in unpowered condition) or PGND ground loss, the interface is configured as receiver-only and LIN driver should not disturb communication of other active nodes on the bus. Once supply/ground are restored, interface returns to normal operation without any kind of intervention from outside.

In addition, the following protection, detection and monitoring features are provided:

- Protection against LIN pin short to battery, even above VIN voltage value.
- Driver current limitation (I_{LIM_LIN}) in case of LIN pin short to battery while in dominant state.
- Overtemperature detection and protection. As temperature exceeds $T_{OT\_LIN\_H}$ for a time longer than $t_{OT\_LIN\_FLT}$, transmitter is disabled. Normal operation is automatically recovered as temperature goes below $T_{OT\_LIN\_L}$ for a time longer than $t_{OT\_LIN\_FLT}$. Overtemperature actual status can be read by accessing LIN_STATUS global SPI register, OT_LIN bit.
- LIN pin voltage A/D conversion through global SPI request.
- LIN_TX dominant timeout monitoring. If LIN_TX voltage remains low (dominant state) for a time longer then $t_{LIN\_TX\_DOM\_TO}$, transmitter is disabled and LIN_TX_DOM_TO bit (LIN_STATUS global SPI register) is set and latched. LIN_TX_DOM_TO bit is cleared upon reading. Normal operation restore strategy can be selected with LIN_CFG global SPI register, LIN_TX_DOM_TO_CFG bit, as follows:
  - If set to 0 (default), operation is restored after LIN_TX_DOM_TO bit reading.
  - If set to 1, operation is restored as LIN_TX pin returns to high value (recessive state).
- Permanent recessive fault monitoring. If LIN_TX voltage goes low (dominant state) but LIN_RX voltage does not follow this transition within $t_{LIN\_PERM\_REC\_TO}$ time, transmitter is disabled and LIN_PERM_REC_TO bit (LIN_STATUS global SPI register) is set and latched. LIN_PERM_REC_TO bit is cleared upon reading. Normal operation is restored after LIN_PERM_REC_TO bit reading and clearing.
- Permanent dominant fault monitoring. If LIN_RX voltage remains low (dominant state) for a time longer then $t_{LIN\_PERM\_DOM\_TO}$, PERM_DOM_TO bit (LIN_STATUS global SPI register) is set and latched. PERM_DOM_TO bit is cleared upon reading. Transmitter circuit is not disabled.

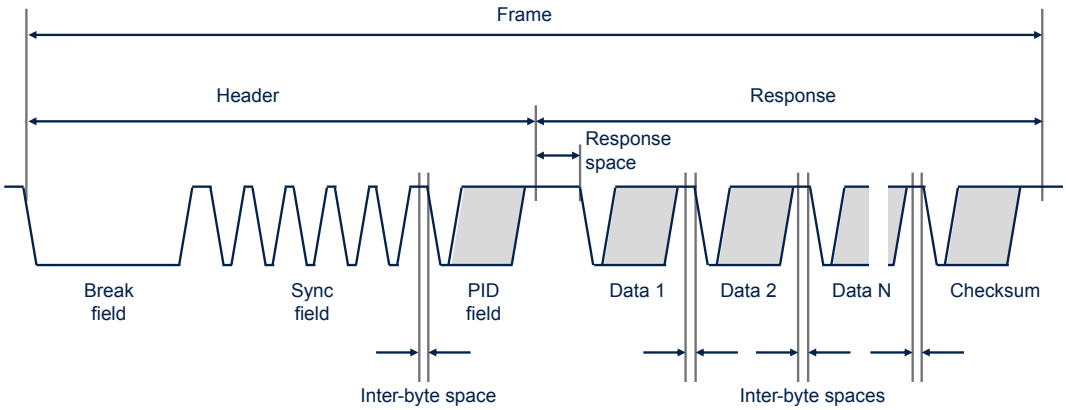
LIN_TX dominant timeout, permanent recessive, and permanent dominant monitoring features are globally enabled/disabled through LIN_MON_EN bit in LIN_CFG global SPI register. Default state is 0.

11.2 Communication validation and decoding

11.2.1 Message structure

Structure of a standard LIN_RX communication message frame is shown in Figure 68.

Figure 68. LIN_RX frame structure



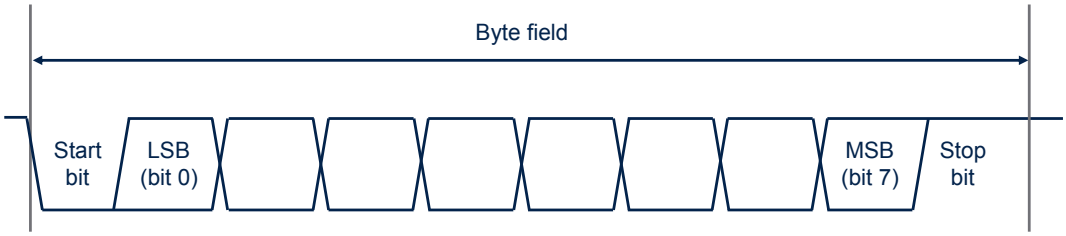
The frame is constructed as follows:

- Header section: composed by break field, sync field and the protected identifier byte field (PID).
- Response section: composed by 1 to 8 data byte fields and the checksum byte field.

Header starts at the falling edge of the break field and ends after the end of the stop bit of the PID field, while response starts at the end of the stop bit of the PID field and ends after the stop bit of the checksum field. The interbyte space is the time between the end of the stop bit of the preceding field and the start bit of the following byte, while the response space is the interbyte space between the PID field and the first data field; both of them must be non negative.

Each byte field is transmitted as shown in Figure 69, that is LSB first, MSB last. Start bit is encoded as value zero (dominant), while stop bit is encoded as value one (recessive).

Figure 69. Byte field structure



Break field structure is shown in Figure 70. It is used to signal the beginning of a new frame; it is the only field that does not comply with the byte field structure shown in Figure 69. A break field is always present and it composed by at least 13 nominal bit times of dominant value, followed by a break delimiter, lasting for at least one nominal bit time of recessive value. Message receiver uses a break detection threshold of 11 dominant bit times.

Figure 70. Break field structure

Sync field is a byte field with the data value equal to 0x55. Message receiver detects a break/sync field sequence, even if it expects a byte field (assuming the byte fields are separated from each other). Whenever a break/sync field sequence happens, the message transfer in progress is aborted, all received data is cleared and processing of the new frame begins. There are no fault indicators for this kind of event.

Protected Identifier field (PID) is a byte field consisting of 6 frame identifier bits (IDx) and P0/P1 parity bits. Its structure is shown in Figure 71. Parity calculations are shown below:

P0 = ID0 ⊕ ID1 ⊕ ID2 ⊕ ID4

P1 = NOT (ID1 ⊕ ID3 ⊕ ID4 ⊕ ID5)

Figure 71. PID field structure

A frame carries a data entity composed by several data byte fields (from 1 to 8); for data entities longer than one byte, the entity LSB is contained in the byte sent first, while the entity MSB is in the byte sent last (little-endian).

Checksum field is the last byte field of the frame, the validation of uses the enhanced method: over all data bytes and the protected identifier byte.

11.2.2 Validation and decoding

A flow chart diagram of LIN OCS message validation and decoding procedure is shown in Figure 72.

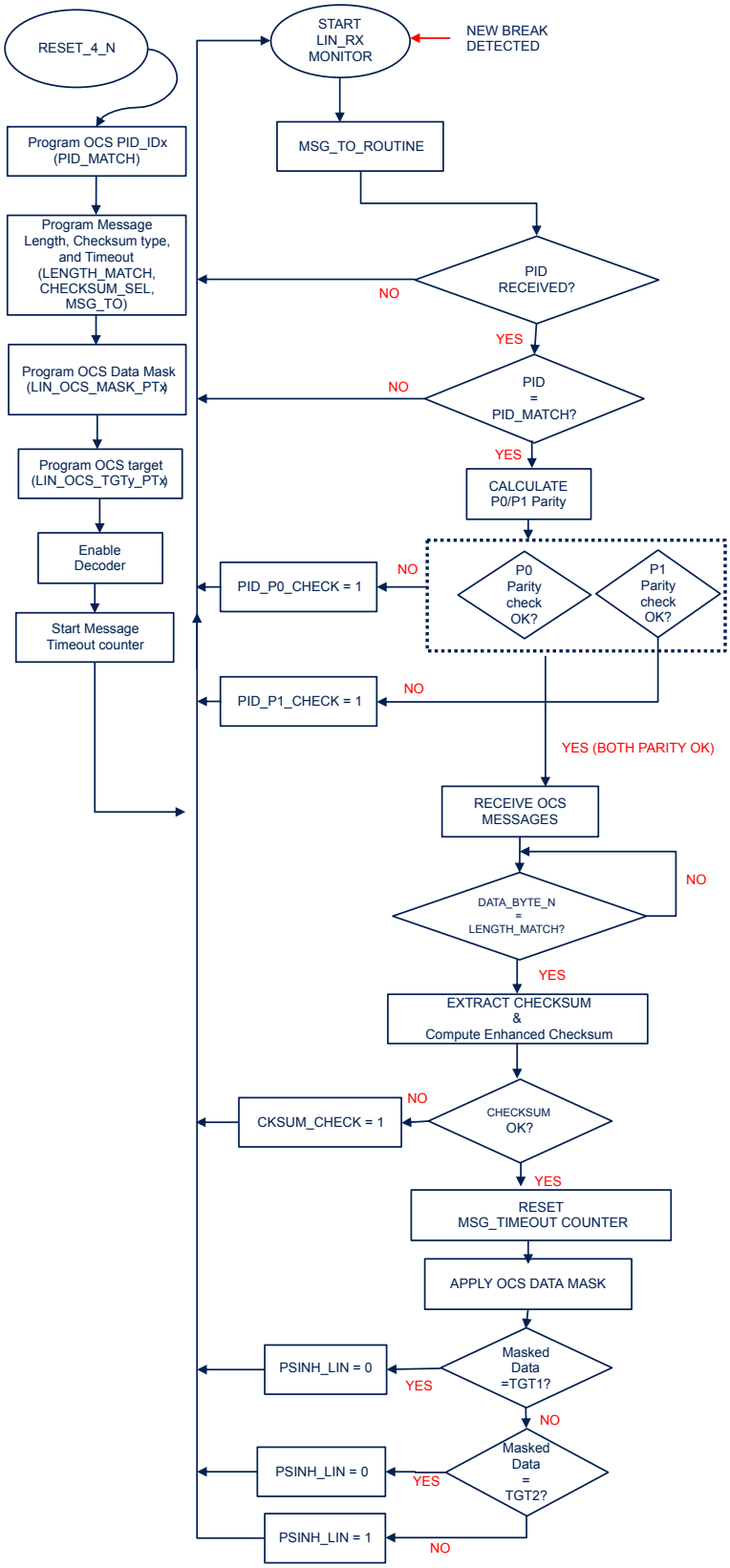
As the internal LIN message digital decoder is enabled, it starts monitoring all communication on the LIN bus checking for messages with the following characteristics:

- A specific matching PID: expected IDx bit values are programmed using PID_MATCH 6 bit field, located in LIN_CFG global SPI register. Parity bits P0 and P1 are checked as well to verify PID integrity; result of this check can be read on LIN_STATUS global SPI register, PID_P0_CHECK and PID_P1_CHECK bits (0 = OK, 1 = parity error).
- A specific number of data bytes: expected byte number is programmed using LENGTH_MATCH 2 bit field, located in LIN_CFG global SPI register. Available values are 00 = 1 byte, 01 = 2 bytes, 10 = 4 bytes and 11 = 8 bytes.
- A valid checksum: check result can be read on LIN_STATUS global SPI register, CKSUM_CHECK bit (0 = OK, 1 = checksum error).

A message is considered as “valid” when it passes the following checks in this order:

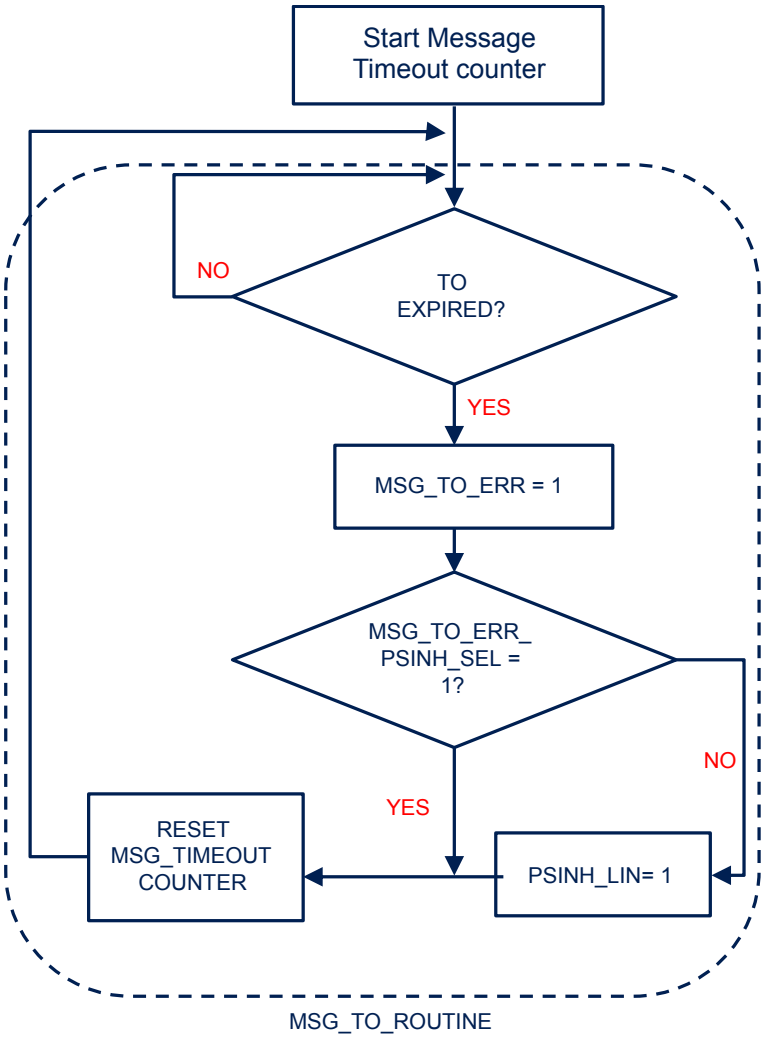
1. PID value matches the expected value.
2. PID parity bit checks are OK.
3. Correct checksum calculation.

Figure 72. LIN OCS message validation and decoding flow chart



Additionally, decoder expects to receive a “valid” message within a specific time with respect to the previous one. This timeout value is programmed using MSG_TO 2-bit field, located in LIN_CFG global SPI register: available values are 00 = 0.5 s, 01 = 1 s, 10 = 2 s and 11 = 4 s. Message timeout timer is started as decoder is enabled and its routine (see Figure 73) works in parallel during the LIN OCS message validation, while it is reset as soon as a new message is received and validated or the timeout itself expired. When the timer expires the MSG_TO_ERR bit in LIN_STATUS global SPI register is set to 1.

Figure 73. LIN message timeout routine



In addition, in case of no activity on the LIN bus, after $t_{LIN\_PROT\_TO}$ the protocol timeout is set and the flag LIN_PROTOCOL_TO_ERR (flag clear on read) is asserted. To recover the LIN communication, it is required a wakeup pattern (150 µs typ in case of 20kbaud) or a break field along with a sync field. A LIN protocol timeout puts the LIN into a sleep state (read only bit LIN_SLEEP_MODE in LIN_STATUS register is set) and the recovery procedure does not include a LIN response decode if a new LIN command is given. After the recovery procedure, LIN_SLEEP_MODE is set automatically to ‘0’ and the next message is decoded correctly.

After passing validation process, each message data entity content is ready to be analyzed in order to determine if LIN-related passenger inhibit status signal (PSINH_LIN) has to be updated or not. Here is the procedure with the correct order execution:

1. The significant part of each data byte is extracted using a SPI-programmed mask. There are 4 global SPI registers dedicated to mask definition:
   a. LIN_OCS_MASK_PT0: data byte 1 and 2 mask
   b. LIN_OCS_MASK_PT1: data byte 3 and 4 mask
   c. LIN_OCS_MASK_PT2: data byte 5 and 6 mask
   d. LIN_OCS_MASK_PT3: data byte 7 and 8 mask

   Within each data byte, a bit is considered as significative when the corresponding mask bit inside LIN_OCS_MASK_PTx register is set to 1.
2. Masked data is compared to the first OCS target value and, if matching is found, PSINH_LIN is set to 0. There are 4 global SPI registers dedicated to first OCS target definition:
   a. LIN_OCS_TGT1_PT0: data byte 1 and 2 target 1
   b. LIN_OCS_TGT1_PT1: data byte 3 and 4 target 1
   c. LIN_OCS_TGT1_PT2: data byte 5 and 6 target 1
   d. LIN_OCS_TGT1_PT3: data byte 7 and 8 target 1
3. Only in case target 1 is not matched, masked data is compared to the second OCS target value and, if matching is found, PSINH_LIN is set to 0. There are 4 global SPI registers dedicated to second OCS target definition:
   a. LIN_OCS_TGT2_PT0: data byte 1 and 2 target 2
   b. LIN_OCS_TGT2_PT1: data byte 3 and 4 target 2
   c. LIN_OCS_TGT2_PT2: data byte 5 and 6 target 2
   d. LIN_OCS_TGT2_PT3: data byte 7 and 8 target 2
4. If target 2 is not matched as well, PSINH_LIN is finally set to 1.

It is possible to configure the effect of a message timeout error (MSG_TO_ERR = 1) of the PSINH_LIN signal status by programming MSG_TO_ERR_PSINH_SEL bit in LIN_CFG global SPI register:

- If set to 0: PSINH_LIN is set to 1 after timeout.
- If set to 1: no effect.

In ACL_PSINH_STATUS global SPI register, PSINHINTLIN read-only bit provides PSINH_LIN signal current status (after power-up, PSINH_LIN signal is 1).

12 Arming logic

There are eight ARM signals that can be generated by three arming methods:

- **Internal arming** by internal safing logic

  Safing logic supports total 22 independent programmable safing records. In the safing state, the MCU periodically requests for sensor data and, using either fixed or programmable mask, safing logic decodes 32-bit of remote bus SPI transmission. Each safing record can be configured to process data either through the single sample comparator or through the moving average comparator. Once the sensor SPI transmission and correctness of the SPI frames are validated, data or event counts are compared against the threshold to determine if arming and VSF regulator enable output should be asserted.

- **External arming** by external sources:
  - E2E (End-to-End) module.

    Only the master SBC receives E2E request by MCU. The slave SBC updates ARM_E2E register by monitoring ARM_E2E status request by main MCU from master SBC over global SPI bus.
  - Snooping ARM result from another L9691.

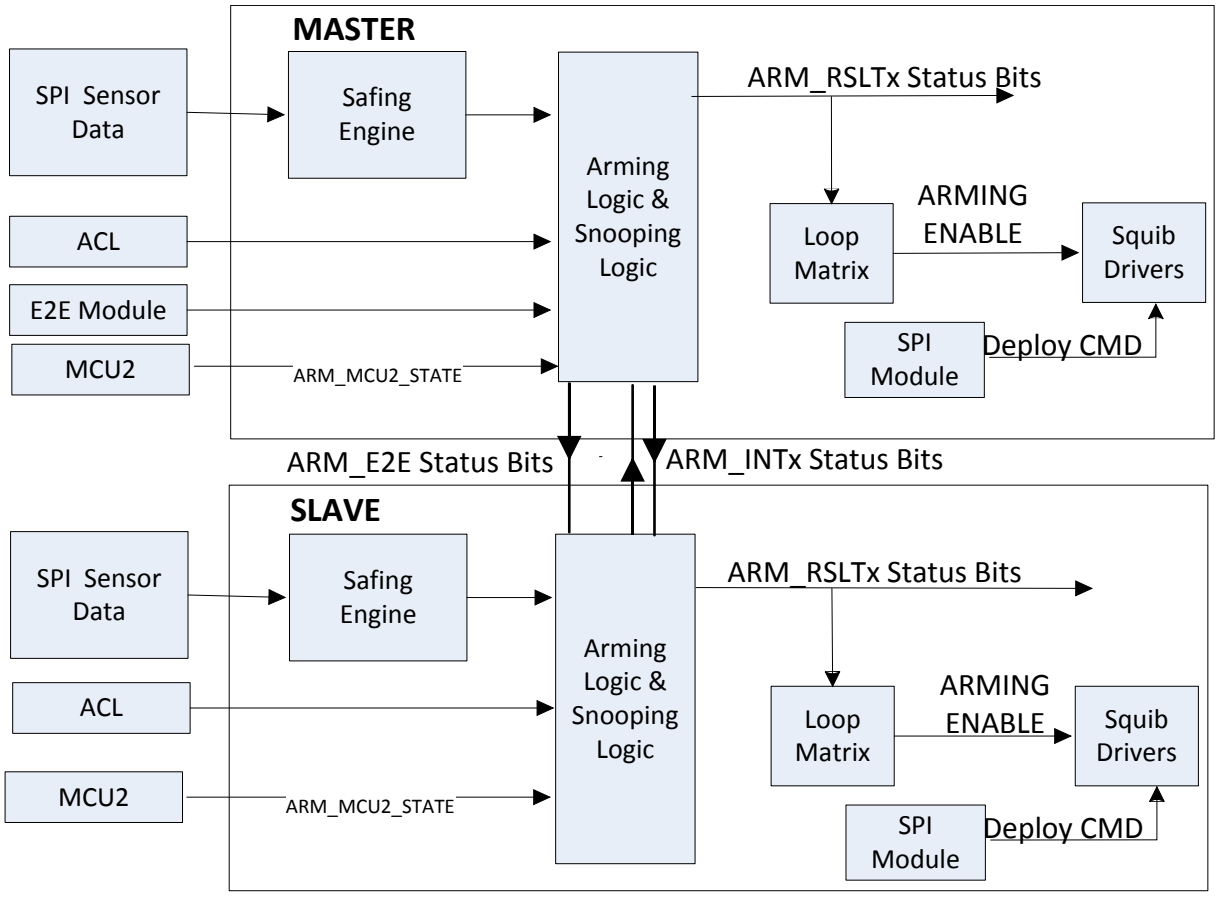
    The device can update its arm result by snooping the information from another device (master or slave).
  - Snooping ARM result from MCU2.

    The device can update its arm result by snooping the information from a secondary MCU2.

- **Scrap vehicle arming** by ACL input: safely activating arming and safing switch control at the end of vehicle life.

A general arming overview diagram is shown in Figure 74.

Figure 74. General arming overview



12.1 Internal arming: safing logic

Safing safety concept uses independent silicon other than MCU to monitor and process on-board and remote sensors data to determine whether necessary conditions are met to activate arming outputs used to control the deployment logic. Deployment is inhibited when safing is not met.

Safing logic can be divided into the following sub-blocks:

- Configuration - configuration of safing registers
- Physical layer decoder - CRC and frame check
- Protocol layer decoder - extraction of relevant information from SPI message
- Safing engine data updater - extraction is matched to safing records that means check if data received has to be used by the safing engine based on specific configuration of the safing record
- Safing engine:
  - Data processing: offset cancellation, moving average computation
  - Data compare: data comparison to configured threshold
  - ARM control: ARM and ARM stretcher

To support sensor with different sampling rate, the sampling window to acquire new data from sensor is managed by MCU.

The sampling window is closed when (SAF_CC_x registers cleared in order to acquire new data):

- SAF_CC_PTx clear on write access: MCU request a write access (writing 1) to SAF_CC_x register to clear only the SAF_CC[i] bit of interest. This method allows handling of various sensor sampling rate (every sampling period for every safing record could be independent).
- SAF_CC_CLEAR_ALL is set: MCU set the SAF_CC_CLEAR_ALL and clear all the SAF_CC register bits (all 22 registers) at once, so all the sampling windows are closed in the same time.

If “no valid match” is found when sampling window is closed for records that have SAF_EN bit set, this is considered as NO DATA for that record in the sampling period (SAF_NODATA_STATUS_PTx register will be updated).

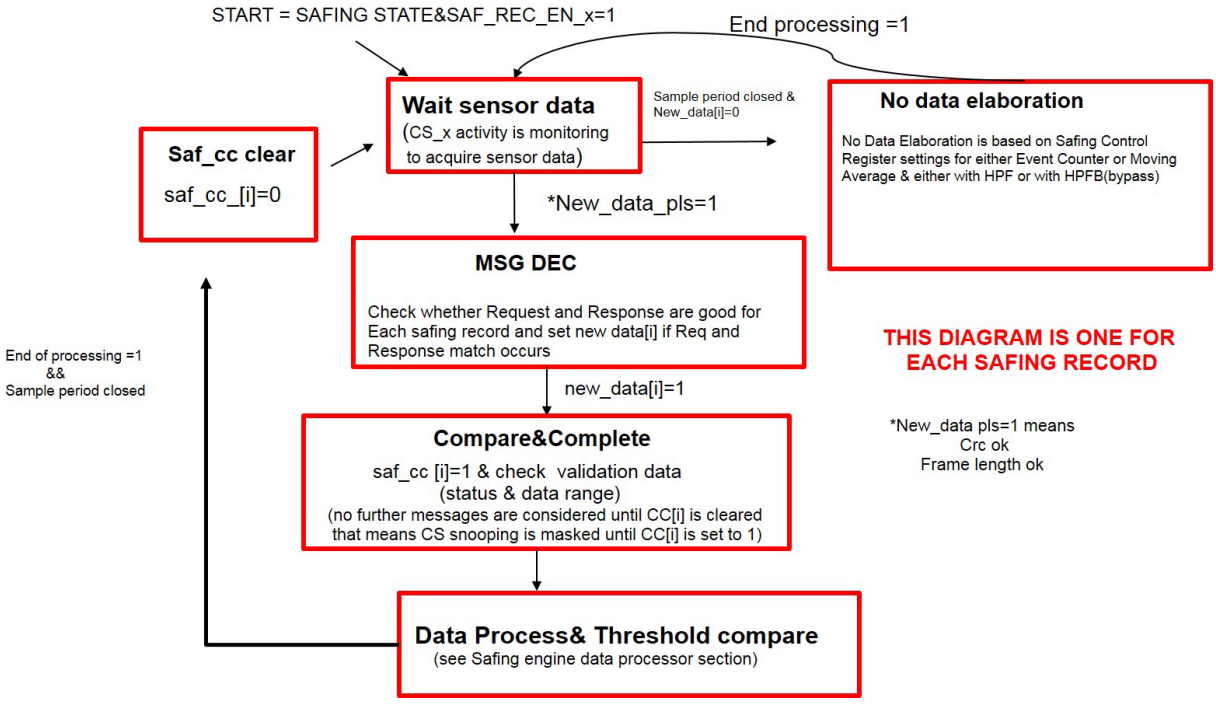
No valid match can be caused by the following events:

- CRC or frame length error.
- Safing engine acquires data but there are no matching between REQ_TARGET and received data (RS_MOSI) or RESP_TARGET and received data (RS_MISO).
- Request and response match occurs but sensor data is “out of range”: data range check fails, SAF_CC_x will be set to 1 but the data are substituted with value based on NO data configuration (NO_DATA_EVCNT and NO_DATA_MA bits), setting a status fault bit in SAF_NODATA_STATUS_PTx_NO_VALID_DATA_y.
- MCU did not request sensor data before that sampling window is closed.

In all these cases where a “no valid match” is detected when the sampling window is closed, enabled safing records that were not updated will substitute data with bias data and re-calculate/update.

The top level safing engine flow diagram is shown in Figure 75.

Figure 75. **Safing control logic data control**



12.1.1 Safing configuration

There are total 22 safing records supported by device. Each safing record is independently configured and enabled. Each safing record allows configurations of:

- Request mask: 10 x register addresses (5 SPI protocols * 2(16 bits register)) that contain mask for sensor address (SAF_REQ_MASK_CSx_PT1 and SAF_REQ_MASK_CSx_PT2)
- Request Target: 44 x register addresses (22 safing records * 2(16 bits register)) that contain expected sensor address (SAF_REQ_TARGET_x_PT1 and SAF_REQ_TARGET_x_PT2)
- Response mask: 10 x register addresses (5 SPI protocols * 2(16 bits register)) that contain mask for sensor address, sensor status and data identifier bits (SAF_RESP_MASK_CSx_PT1 and SAF_RESP_MASK_CSx_PT2)
- Response Target: 44 x register addresses (22 safing records * 2(16 bits register)) that contain expected sensor address and sensor status (SAF_RESP_TARGET_x_PT1 and SAF_RESP_TARGET_x_PT2)
- Data mask: 10 x register addresses (5 SPI protocols * 2(16 bits register)) that contain mask for sensor data bits (SAF_DATA_MASK_CSx_PT1 and SAF_DATA_MASK_CSx_PT2)
- Safing threshold positive: 22 x 16-bits in length registers for positive data threshold (SAF_THRESHOLD_P_x)
- Safing threshold negative: 22 x 16-bits in length registers for negative data threshold (SAF_THRESHOLD_N_x)
- Safing control registers: independent registers for all 22 safing records (SAF_RECx_CTRL_PT1 and SAF_RECx_CTRL_PT2)
- Safing event algorithm register for event counter and threshold configuration (SAF_EVC_CFG)
- Safing enable registers: safing engine enable bit for each safing record (SAF_EN_CTRL_PT1 and SAF_EN_CTRL_PT2)
- Safing CS registers: safing engine registers to configure the protocol associated for every SAF_CSx (SAF_CSx_CGF and SAF_CSX_CFG)

Safing control registers (SAF_RECx_CTRL_PT1 and SAF_RECx_CTRL_PT2) allows configurability of the following parameters:

- ARM pulse stretcher duration selection 32 ms, 128 ms, 256 ms, 512 ms, 2048 ms and 4096 ms (ARM_STRETCHER bits)
- Mapping to any combinations of the 8 ARMINT_x signals (ARMx bits)
- Mapping of safing record to SAF_CSx/RS_CS (SAF_CS_SELECTION bits)
- Selection of either event method or moving average method (ARM_METHOD bit)
- Selection of either slow offset cancelled data processing or no slow offset cancelled data processing (HPF_BYPASS bit)
- HPF time constant selection configurable choosing the right N, that is numerator/denominator shift (HPF_SHIFT_FACTOR bits)
- Selection of number of samples used in moving average: 2, 4, 8, 16 (AMA_SAMPLES)
- Downsampling factor for AMA: 00 = take every sample, 01 = take every other sample, 10 = take every 4^{th} sample, 11 = take every 8^{th} sample (DOWNSAMPLE bits)
- Pseudo 4K or non-pseudo 4K sampling selection (PSEUDO_4K_SENSOR bit)
- Selection to either reset or decrement event counter strategy if “no data” received in the sample period (NO_DATA_EVCNT bit)
- Selection to input either 0 value or last known value for moving average method (included down-sampling path) when “no data” received in the sample period (NO_DATA_MA bit)
- Sensor data type: signed or unsigned (SENSOR_TYPE bit)
- Data range type: PED_PRO = 0 (standard PSI5 range: -480 ≤ validation range ≤ 480), PED_PRO = 1 (pedestrian protection: 307 ≤ validation range ≤ 2048)
- Data range limit enable (RANGE_CHECK_EN bit)

Safing enable (SAF_EN_CTRL_PTx) is allowed in DIAG and in SAFING states. All other safing registers described above are allowed to be configured in DIAG state only and register content goes to default value when RESET4 occurs.

12.1.2 Sensor data acquisition - SPI block diagram

There are two similar data acquisition flows for data coming from the communication between MCU and satellite logic (SPI_RS_CS) and between MCU and on-board sensors (SPI_SAF_CSx):

- The acquisition by SPI_SAF_CSx is based on the configurable SPI decoder described before and manages data from on-board sensors to safing records (Figure 77).
- The acquisition by SPI_RS_CS manages data from satellite sensors to the safing records (Figure 78).

Both ones are enabled in SAFING state.

If more than one SAF_CSx or RS_CS is asserted at the same time, the sensor data is not acquired in any safing record because it is not possible to recognize which is the data source. In this case, the MISO_RS will be in high impedance.

Figure 76. **Sensor data monitoring data path**

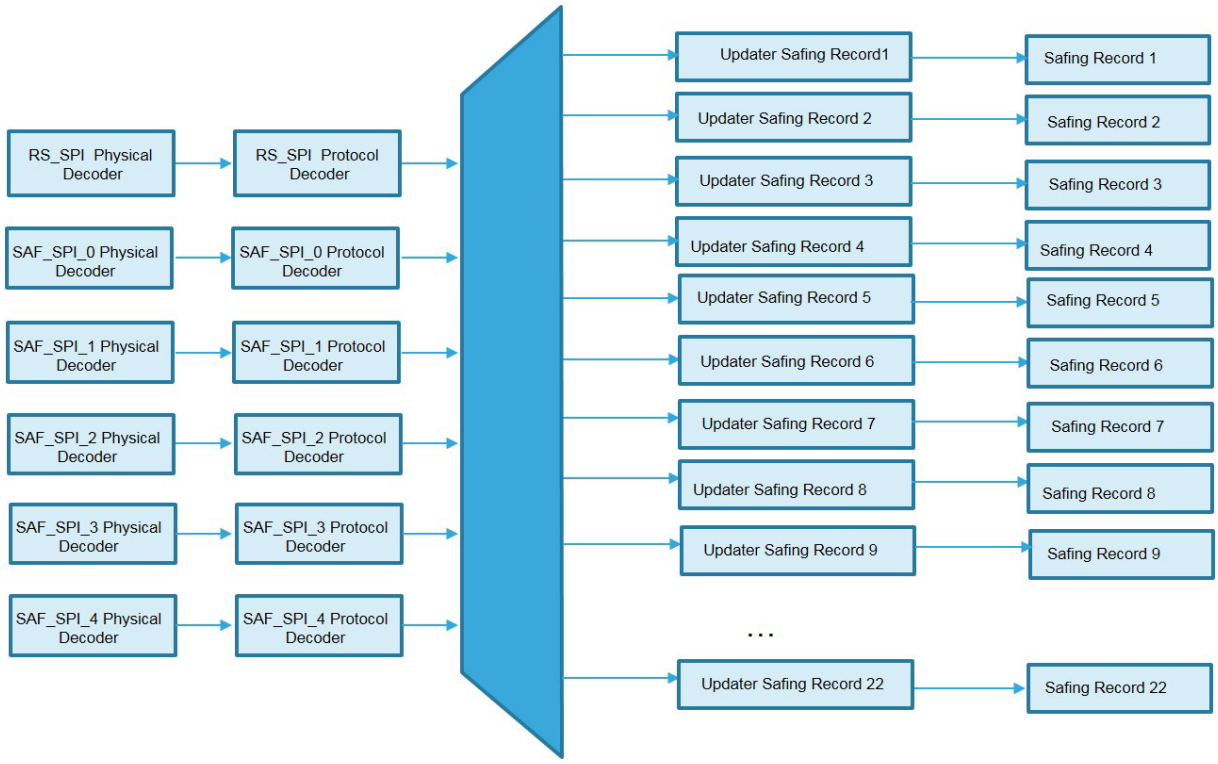


Figure 77. **Snooping control SPI_SAF_CSx sensor data**

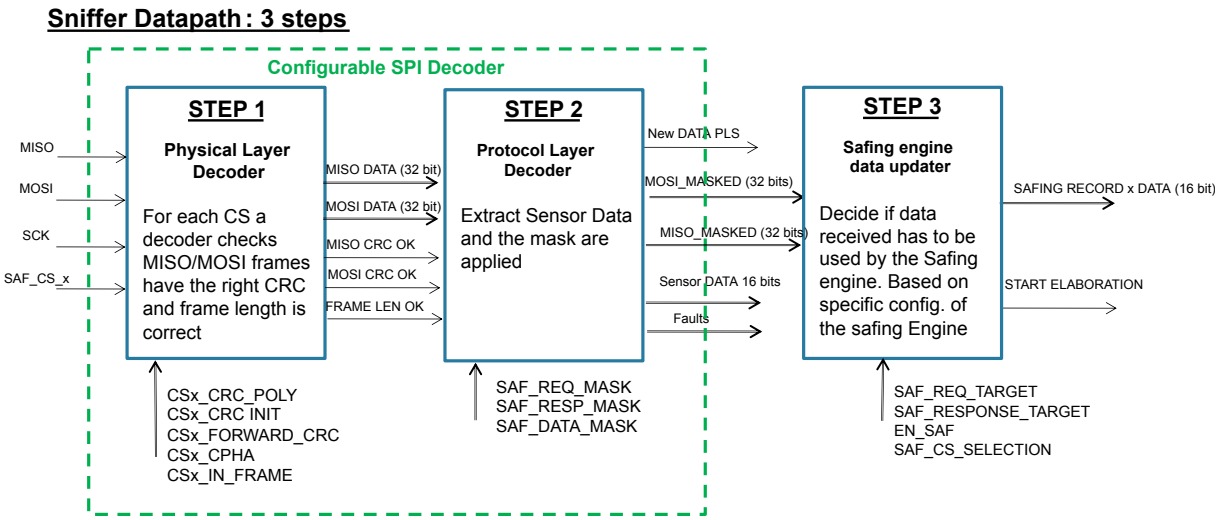
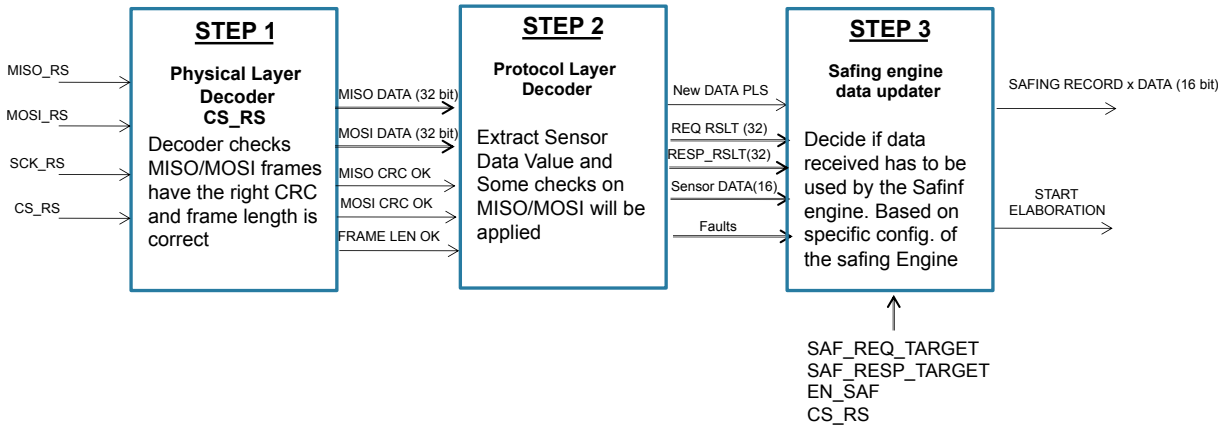


Figure 78. **Snooping control SPI_RS sensor data**



12.1.3 SPI monitor physical layer decoder - STEP 1

Task of physical layer decode is to validate integrity of SPI frame regardless of the format.

For on-board sensors the protocol frame format is set through SAF_CSX_CFG register, while for satellite sensors the safe SPI format is used.

The CRC polynomial used by on-board sensors can be configured in SAF_CS0_CFG, SAF_CS1_CFG, SAF_CS2_CFG, SAF_CS3_CFG, SAF_CS4_CFG registers choosing both the polynomial (max 8 bits) and the init value for every protocol.

For the programmable protocols there are the following constraints:

- CRC computed on whole frame: the receiver calculates CRC over the complete 32-bit frame and final result shall be zero
- CRC max poly order is 8
- CRC bits have to be placed in LSB bits
- CRC of MOSI and MISO have the same configuration (same poly, same init value…)

In addition, the register SAF_CSX_CFG register has to be programmed in order to define:

- CRC implementation: Forward or not forward
- In-Frame or Out-Of-Frame selection
- CPHA selection (0 or 1)

The “forward” architecture is not a pure polynomial divider. The CRC value of the “input sequence” can be read on the register bits just after the last “input sequence”’s bit has entered the architecture.

The “not forward” architecture is a pure polynomial divider. The CRC value of the “input sequence” can be read on the register bits after the input sequence followed by 5 zeros (as many zeros as the polynomial order that in this example is 5) has entered the architecture.

In case the initial value in CRC(5:1) register is not all 0’s (00000) the 2 architectures give 2 different CRCs for the same input sequence.

For all data sensor snooped, two main checks are performed:

- Frame length: expected frame has 32 SCLK edges. In case of failure, error is communicated to other safing sub-blocks.
- CRC: using known CRC polynomial and init value, target is computed by physical layer decoder and compared to the message CRC. In case of failure, error is communicated to other safing sub-blocks. CRC check can be skipped through DEVICE_CTRL configuration register (CRC_MASK_SAF_CSx or CRC_MASK_RS_CS).

12.1.4 SPI monitor protocol layer decoder - STEP 2

Sensor data is periodically communicated with the main MCU over RS_SPI bus. The L9691 monitors SPI traffic on MOSI_RS and MISO_RS bus to extract the necessary information from the bus. It uses protocol frame format information to mask the bits of interest.

The SPI protocol layer Decoder supports 5 SPI programmable frame formats for data from on-board sensors (SPI_SAF_CS_x) while hardwired mask is used for data from satellite sensors (SPI_RS_CS).

For all the protocols, data size is no larger than16 bits in length.

The satellite sensor data can be 10 or 16 bits:

- the 10-bit remote sensor data left-justify the data (padded with six 0's on the right) when the SPI response is generated, before further processing steps which assume data is signed should be using two's complement representation.
- The 16-bit data field should already aligned properly for 16-bit safing records.

This stage generates a new data pulse when all the following conditions are satisfied:

- MISO CRC and MOSI CRC are correct.
- Frame length is correct (32 bits).

When new data pulse is generated, sensor data, request result and response result are forwarded to next step.

The hardwired mask used for data received by satellite logic are in Table 556, Table 557 and Table 558.

Table 556. Hardwired request mask (MOSI line)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 557. Hardwired response mask (MISO line)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISO	1	1	1	1	1	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Table 558. Hardwired data mask (MISO line)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISO	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0

12.1.5 Safing engine data updater - STEP 3

Once the information from protocol layer Decoder is available, safing engine processes it to determine if the request and response match the Target value. If match occurs, "New_Data" flag and SAF_CC get set. "New_Data" flag is used to determine if data is allowed to be further processed.

Figure 80. Safing engine message decoder for pseudo 4K sampling is for safing engine message decoding pseudo 4K sampling which allows the use of single safing record per sensor channel when data is received in two different PSI5 registers of a given RSU channel. Figure 79 concept is applicable to all others. If input packet matches multiple safing records, the safing engine processes all records and process them independently. A safing record can only be evaluated on the first matching input packet. Any additional message packets for that given safing record are ignored (that is once compared complete is set indicating the arming logic has completed evaluation of recent data, further processing cannot be done until the compare complete flag is cleared). At the end of sensor data acquisition period, MCU can read SAF_CC register to determine if CC bits were set for the expected safing records. Safing engine can process same SPI frame from two or more sources according to SAF_CS_SELECTION configuration.

Figure 79. **Safing engine message decoder**

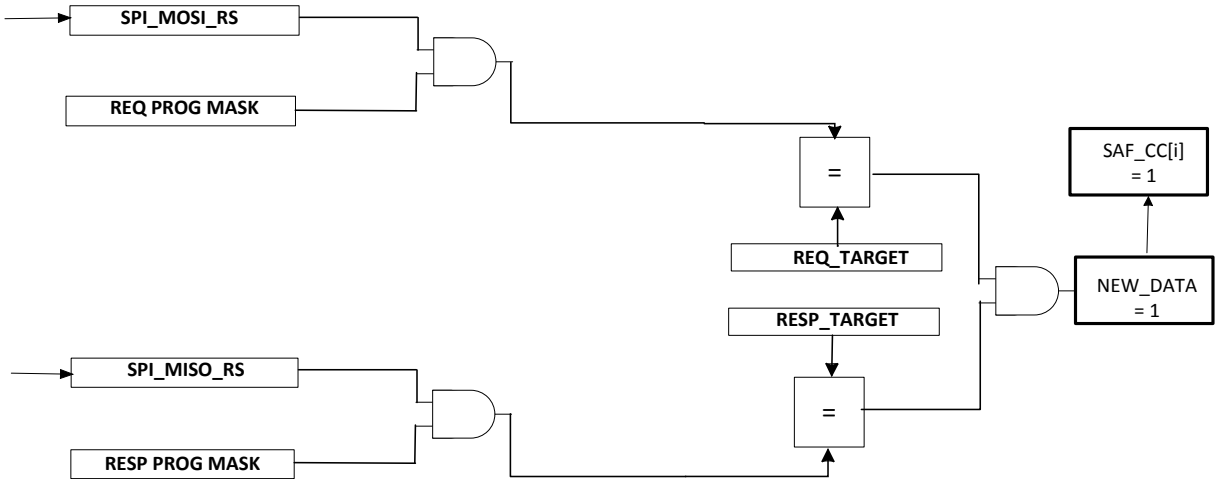
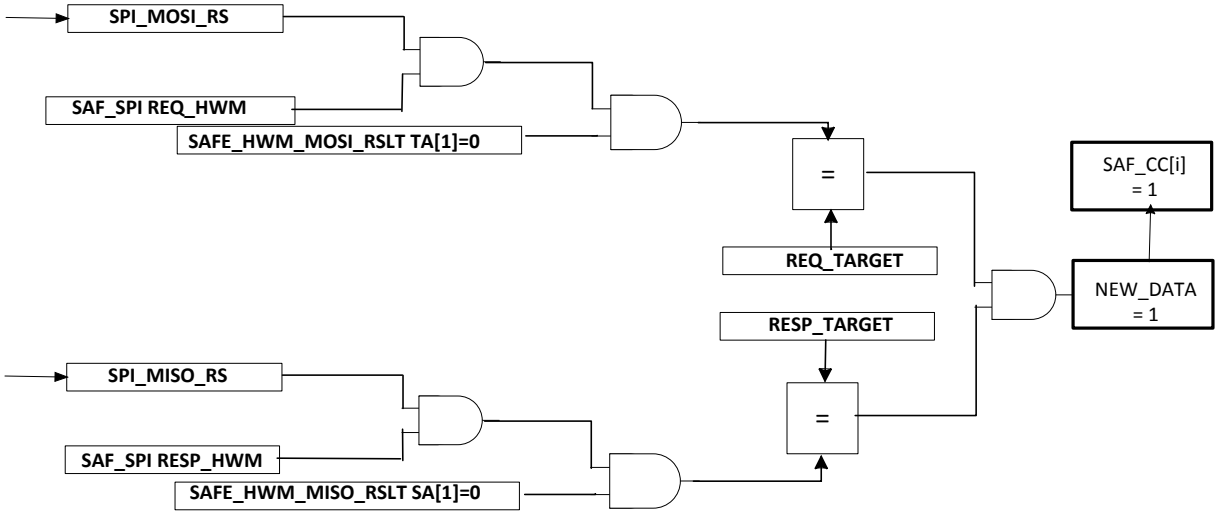


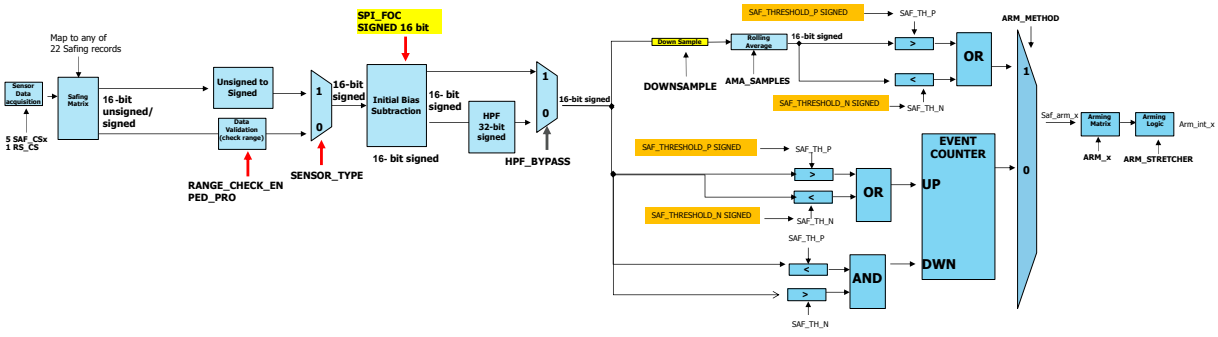
Figure 80. **Safing engine message decoder for pseudo 4K sampling**



12.1.6 Safing engine data processor

After that the sensor data is acquired by the mapped safing record according to the safing matrix, the data is elaborated in the safing engine. The safing engine could be programmable according to the relative safing control register (SAF_RECx_CTRL_PTy and SAF_EVC_CFG).

Figure 81. **Safing engine data processing**



When the device is into SAFING state and safing record is enabled, the data acquisition is started. A data will be acquired by safing engine every sampling window.

A “no valid match” found by SAF_CC clear (sampling window closed) will lead to the cases illustrated in Table 559 and in Table 560, and shown in Figure 82 and Figure 83.

Table 559. AMA arming method configuration

AMA arming method		
HPF_BYPASS = 0 (HPF path)	NO_DATA_MA = 0	**HPF update**: 0 value into HPF digital filter **Rolling average update**: 0 value into rolling average (before down-sampling block)
	NO_DATA_MA = 1	**HPF update**: Last valid input used as current input into HPF **Rolling average update**: HPF output into rolling average (before down-sampling block)
HPF_BYPASS = 1 (no HPF path)	NO_DATA_MA = 0	**Rolling average update**: 0 value into rolling average (before down-sampling block)
	NO_DATA_MA = 1	**Rolling average update**: Last valid input into rolling average (before down-sampling block)

Figure 82. No data case with AMA arming method

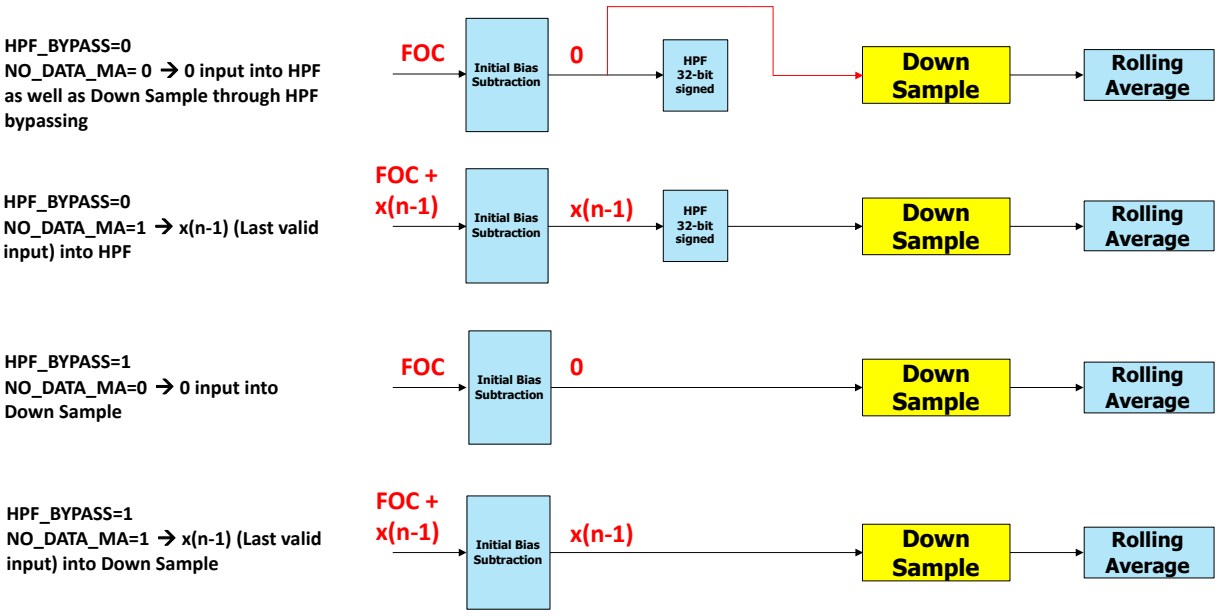
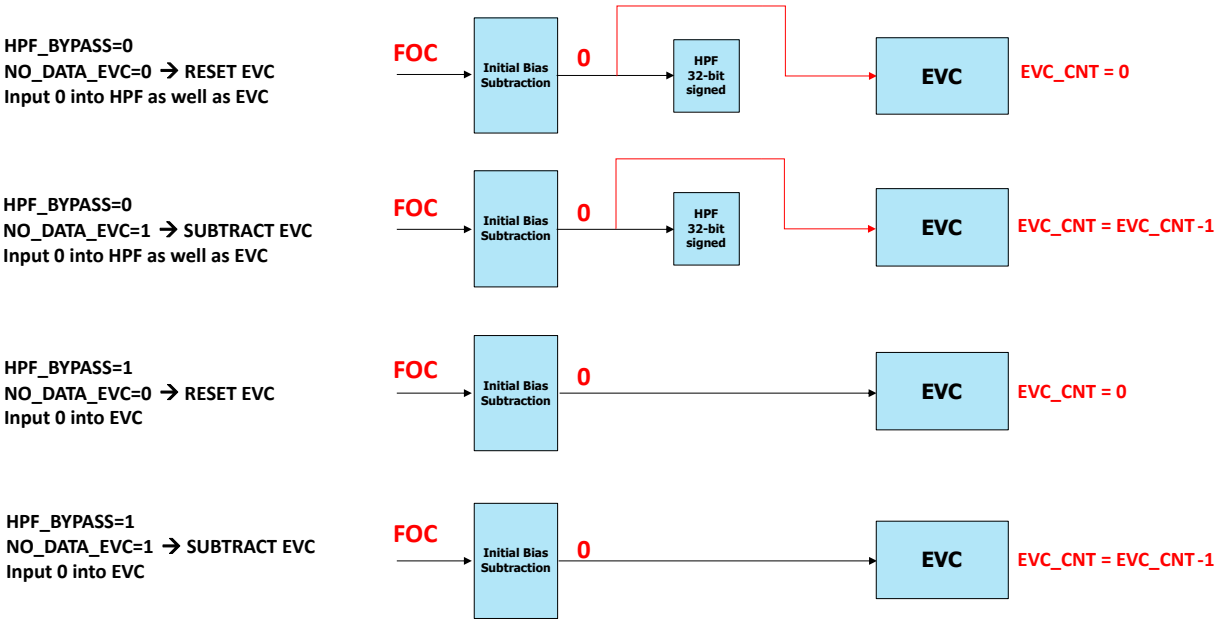


Table 560. Event counter arming method configuration

Event counter arming method		
HPF_BYPASS = 0 (HPF path)	NO_DATA_EVC = 0	**HPF update**: 0 value into HPF digital filter **Event counter update**: EVC output is reset to 0
	NO_DATA_EVC = 1	**HPF update**: 0 value into HPF digital filter **Event counter update**: EVC output is decremented by 1
HPF_BYPASS = 1 (no HPF path)	NO_DATA_EVC = 0	**Event counter update**: EVC output is reset to 0
	NO_DATA_EVC = 1	**Event counter update**: EVC output is decremented by 1

Figure 83. **No data case with event counter arming method**



A RAM block is used to memorize the sensor data samples for all safing engines configured for using rolling average. Each safing engine has a dedicated section in the RAM.

A memory BIST is implemented to check the RAM functionality. It is activated at power-up and on demand by MCU in INIT or DIAG states.

The sensor data integrity can be covered by using an internal CRC circuit: the CRC is computed before memorizing the data and stored with it, then when the data is read, the CRC will be checked. In case of CRC error, the corrupted data cannot be used for the computation. A flag is set to latch this event and reported in SAF_RAM_CRC_ERR register, and the elaboration is brought in a safety condition by disabling the safing record (EN_SAFx = '0') affected by the corrupted data. In this way, the MCU can check the safing record affected by the fault and re-enable it. When the safing record is disabled, the datapath is initialized (HPF, AMA and RAM dedicated section, event counter), and the related SAF_ARM_x is reset. However, if the dwell timer (that is arm pulse stretch) has started, it continues, as it is not stopped by the safing record enable.

The Safing record enable bit for any record is programmable as ON or OFF at any time and will enable/disable the record itself upon the following sampling window will be closed (that is clear SAF_CC).

Every time that a safing record is disabled, all the datapath is reset and the related SAF_ARM_x is reset, while the ARM_STRETCHER counter is not stopped.

The safing record output active SAF_ARM_x (unlatched status) is reported in SAF_REC_ARM_STATUS_PTx.

12.1.6.1 *Data validation*

The first step of safing engine data processor is data validation: the range of incoming data is checked.

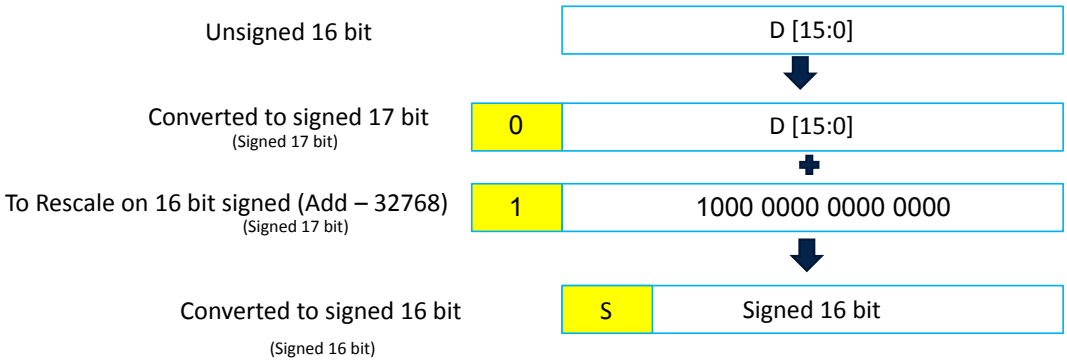
If the data is > |30720| (-480 ≤ validation range ≤ 480 standard range), it is not recognized as valid data (received data is always left justified inside 16 bit data field). If RANGE_CHECK_EN = 0, this step is skipped. In case of PED_PRO = 1, a different limitation range is used to support pressure sensor in pedestrian protection application where the data is 16 bits in 14 + 2 format: the data is valid if -307 ≤ validation range ≤ 2048.

In case of unsigned data (SENSOR_TYPE = 1), set RANGE_CHECK_EN = 0 (disabled).

12.1.6.2 *Unsigned conversion block*

In case of unsigned sensor data (SENSOR_TYPE = 1 in SAF_RECx_CTRL_PT2), the sensor data is converted to signed value according to Figure 84: all the computations in safing engine are performed with signed data. In case of signed sensor data (SENSOR_TYPE = 0), this block is skipped.

Figure 84. **Unsigned to signed data conversion**



12.1.6.3 *Offset cancellation*

The second step of safing engine data processor is offset cancellation.

Sensor can transmit data with or without offset. Sensor offset comprises of two elements, fast offset and slow offset, and the offset cancellation block within safing engine must remove both.

Fast offset is normally realized upon sensor power-on and slow offset is realized over time and temperature change. Sensor fast offset will be computed by the MCU in the DIAG state and written to SAF_FOC_SEEDVALx register before entering into SAFING state. Safing logic supports 22 fast offset seed registers (default value is 0), one for each safing record.

Once the sensor request and response are validated, data is stripped from the response and fast offset is removed. The resulting value is fed into single pole digital HPF for slow offset removal. The device supports several configurable HPF (single pole) time constants programming HPF_SHIFT_FACTOR N according to the sensor sampling rates (that is for 2 kHz sensor sampling 4 s with N = 13 or 32 s with N = 16).

The transfer function of the single pole HPF is the following:

$$H(z) = \frac{Y(z)}{X(z)} = \frac{z-1}{z-\left(1-\frac{1}{2^N}\right)} \quad (12)$$

From the sampling period and the shift factor it is possible to calculate the time constant (Table 561):

$$T_C = \frac{-T}{ln\left(1-\frac{1}{2^N}\right)}$$

Table 561. **High pass filter (HPF) time constant**

Sampling period T [s]	Shift factor N [integer]	Time constant T_C [s]
1/1000	12 or 15	4.1 or 32.8
1/2000	13 or 16	4.1 or 32.8
1/4000	14 or 17	4.1 or 32.8

The HPF implementation uses one shift value. The shift factor N is configurable among the following values: 12, 13, 14, 15, 16, 17. The sample period T depends on sampling window period. The input, InPort, is a signed 32-bit number, created by shifting the bias adjust result by 16 (Bias_adjust << 16). Filter computation is done in 32 bit memory space to allow proper math operation (overflow protected) with shift factor to achieve the desired time constant.

The HPF output is a 16-bit signed number, computed with the following formula:

$$y(n) = y(n-1) - \frac{y(n-1)}{2^N} + x(n) - x\left(n-1\right) \quad (13)$$

When HPF_BYPASS = 1, HPF block is skipped and sensor data is directly compared to safing threshold or processed through moving average calculator before comparison.

12.1.6.4 Data threshold comparison

Safing control register is individually configurable to allow ARM through an event counter reaching the target value or through moving average meeting the safing threshold, using ARM_METHOD bit (SAF_RECxx_CTRL_PT1). SAF_THRESHOLD_P_x and SAF_THRESHOLD_N_x are defined as signed using two's complement representation. SAF_THRESHOLD_P_x must be configured with a positive value and SAF_THRESHOLD_N_x with a negative value.

In **moving average method** *(ARM_METHOD = 1)*, number of samples N used in the calculation is also configurable through the safing control AMA_SAMPLES bit (SAF_RECxx_CTRL_PT2). Moving average buffer initializes with initial value of 0.

$$MA(k) = \frac{\sum_{n=0}^{Samples} a(k-n)}{n+1} \quad (14)$$

To increase the time for moving average sampling, downsampling approach is used in order to have M samples using the same storage location, where M = downsampling_factor * N. Downsampling factor is programmable by DOWNSAMPLE bit in SAF_RECx_CTRL_PT2:

- 00 = take every sample
- 01 = take every other sample (the first sample is skipped, the second one is taken)
- 10 = take every 4th sample
- 11 = take every 8th sample

Once the moving average value exceeds the safing threshold (greater than the positive one or less than the negative one), appropriate ARMINT_x is set. The ARMINT_x is masked for the first AMA_SAMPLE to avoid unwanted arming. For example, setting AMA_SAMPLE = 0x2 (8 samples used in moving average), the ARMINT_x signal is set (if the case) after the 8th sample is received.

Setting the positive threshold to the maximum positive 16-bit signed number will not allow the ARMINT_x to be set due to a positive threshold check because the safing result cannot be greater this number. Setting the negative threshold to the most negative 16-bit signed number will not allow the ARMINT_x to be set due to a negative threshold check because the safing result cannot be less than this number.

In **event counter mode** *(ARM_METHOD = 0)*, sensor data received through the sensor SPI interface and validated by the safing record is passed to the safing algorithm. The simple threshold comparison algorithm compares the received data to two thresholds, SAF_THRESHOLD_P_x (positive threshold) and SAF_THRESHOLD_N_x (negative threshold). If the sensor data is greater than SAF_THRESHOLD_P_x or lower than SAF_THRESHOLD_N_x, event is flagged and the single event counter is incremented based on the programmed value of ADD_VAL. Otherwise, the single event counter is decremented by SUB_VAL. SUB_VAL is programmed by the user and can be same or different than ADD_VAL. This feature allows for an asymmetrical counter function making the system either more or less sensitive to sensor data.

Once the counter value reaches ARM_TH, ARMINT_x bit (ARM_PSINH_INT_STATUS register) is set. When the counter value reaches ARM_TH and a new data exceed the threshold, the counter is clamped at that threshold limit.

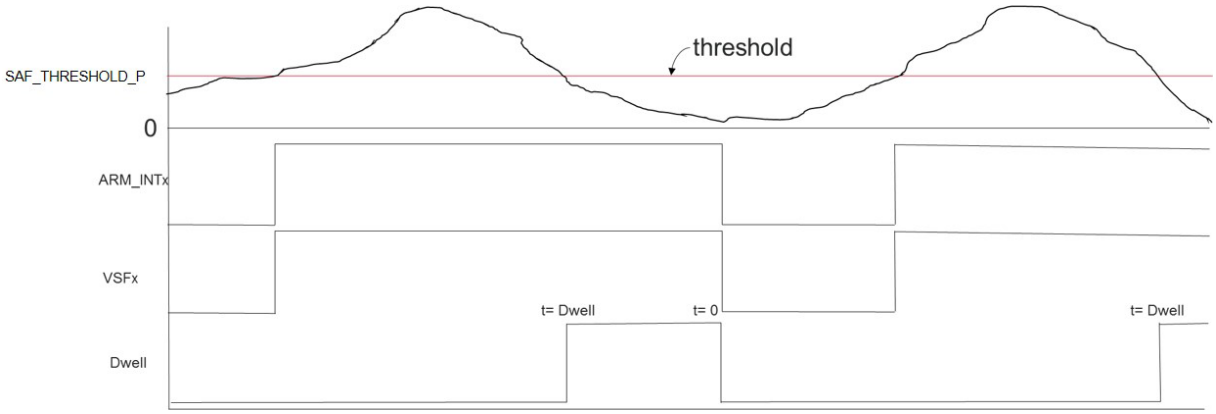
12.1.6.5 Arming matrix (ARMINT_x)

SPI messages are monitored and mapped to specific safing records. Each safing record is configured with its own threshold, dwell time and the appropriate ARMINT_x signal to activate when safing criteria are met. Any enabled safing record can be programmed to an arming signal. All safing records arming status is logically “OR’d” to its programmed arming signal. For example, if safing records 1, 2 and 4 are programmed to ARMINT1 and the records are enabled, any of the records can set the ARMINT1 signal.

12.1.6.6 Arming pulse stretch

ARMINT_x and VSF are kept active for the dwell period based on safing record configuration (ARM_STRETCHER register). The device has eight ARMINT_x and for each ARMINT_x, there is one corresponding timer counter register. In the event mode or moving average mode upon arming, dwell value gets loaded in the appropriate counter register and when safing record output (SAF_ARM_x) is no longer active, counter counts down to 0. As long as counter value remains above 0, arming condition and VSF remain active. Once dwell time has started, it continues, regardless of the en (record enable) bit. Dwell will be truncated in case of SSM reset. If different dwell values are assigned to the same ARMINT_x, the longer value is used. Dwell times can only be extended, not reduced. If the remaining dwell time is less than the new dwell extension setting, the new setting is loaded into the dwell counter. The behavior of the pulse stretch timer is shown below.

Figure 85. **Pulse stretch timer example**



12.2 External arming

There are two sources for external arming:

- E2E communication
- Arming snooping logic

12.2.1 E2E communication

The end-to-end (E2E) communication interface is available to safely receive an ARMing request from outside of the internal safing engine, and to similarly transmit the ARMing status.

This communication is done via the global SPI bus, using a unique GID (111) and SPI frame protocol. Construction of the E2E message is handled within the device, independent of the MCU, to validate and assign (or provide) the proper ARMing.

Only the MASTER device of a dual system will be able to receive and operate on E2E messages. The SLAVE device updates its own E2E ARM status via the SPI monitoring function on the SPI global bus, similar to the mechanism used to ARM_INT.

There are four elements that need to be exchanged for successful E2E communication:

- ARM_STATUS - 8 bits
- DATA_ID - 8 or 12 bits
- ROLL_CTR - 4 bits
- E2E_CRC - 8 bits

The DATA_ID is not sent in the E2E message and is instead configured during INIT or DIAG state and stored. DATA_ID, rolling counter and ARM_STATUS are used in the calculation of the CRC. The E2E module shall manage the counter and CRC fields of each protected E2E message.

The device supports two E2E protection profiles, profile 1A and profile 2, based on autosar 4.2.

The profile determines:

- CRC configuration:
  - *Profile 1*: polynomial = $x^8 + x^4 + x^3 + x^2 + 1$ (0x1D), seed = 0x00. Result xored with 0x00.
  - *Profile 2*: polynomial = $x^8 + x^5 + x^3 + x^2 + x + 1$ (0x2F), seed = 0xFF. Result xored with 0xFF.
- Counter handling:
  - *Profile 1*: 4 bit representing numbers from 0 to 14 incremented on every send request. The CRC is computed before to increment the counter.
  - *Profile 2*: 4 bit representing numbers representing numbers from 0 to 15 incremented by 1 on every send request. The counter is incremented and then the CRC is computed based on incremented counter.
- Data ID:
  - Profile 1: DATA_ID is 2 bytes: 12 bits with 0 appended to the unused bits
  - Profile 2: DATA_ID is 1 byte

12.2.1.1 *E2E SPI frame format*

The E2E exchange is initiated with a message on the global SPI bus with a unique GID (111) and OPCODE to indicate type of E2E operation to follow. The E2E messages use Out-of-Frame format. To indicate the MOSI frame has been correctly received and processed, MISO frame contains feedback in OPCODE bits position. Bit 24 instead is an ADDRESS error flag. The device allows write access to the E2E configuration registers only in INIT and DIAG states. Table 562 to Table 569 show the possible E2E SPI commands.

Table 562. E2E - Read status bits (NOP)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI FLT	0	0	0	0	0	0	Addr Err	0	0	0	0	0	0	0	P	0	0	0	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	S0

Table 563. E2E - Read E2E configuration register (RD E2E CFG)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	1	1	1	0	0	1	0	ADD						0	0	P	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI FLT	0	0	0	0	0	0	Addr Err	0	0	0	0	0	0	0	P	DATA															

Table 564. E2E - Write E2E configuration register (WR E2E CFG)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	1	1	1	0	1	0	0	ADD						0	0	P	DATA															
MISO	SPI FLT	0	0	0	0	0	0	Addr Err	0	0	0	0	0	0	0	P	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 565. E2E - Request to generate E2E TX1 message (REQ E2E_TX1_ARM)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI FLT	0	0	0	1	1	0	Addr Err	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 566. E2E - Read TX1 ARM message requested before (RD E2E_TX1_ARM)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	1	1	1	0	0	1	1	0	0	0	0	0	0	0	0	P	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI FLT	0	0	0	0	1	1	Addr Err	CRC								x	x	x	x	CTR			ARM_STATUS								

Table 567. E2E - Request to generate E2E TX2 message (REQ E2E_TX2_ARM)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	P	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI FLT	0	0	0	0	0	1	Addr Err	0	0	0	0	0	0	0	P	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 568. E2E - Read TX2 ARM message requested before (RD E2E_TX2_ARM)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	1	1	1	0	1	0	1	0	0	0	0	0	0	0	0	P	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI FLT	0	0	0	1	0	1	Addr Err	CRC								x	x	x	x	CTR				ARM_STATUS							

Table 569. E2E - Command to update ARM status, RX function (UPDATE_E2E_ARM_ST)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	1	1	1	0	1	1	1	CRC								P	x	x	x	x	CTR				ARM_STATUS							
MISO	SPI FLT	0	0	0	1	1	1	Addr Err	0	0	0	0	0	0	0	P	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

12.2.1.2 *E2E configuration*

The device includes configuration registers to:

- Enable/disable E2E function
- Enable/disable E2E_TX_1
- Enable/disable E2E_TX_2
- Enable/disable E2E_RX
- Set DATA_ID value(s) and length(es) for TX1/TX2/RX
- Set DATA_Field and Autosar profile to use for TX1/TX2/RX
- Set ARM bit mapping to E2E signal for TX1/TX2/RX
- Set E2E RX counter behavior
- Set E2E RX ARM Dwell time
- Set E2E TX1, TX2, RX CRC forward/not forward architecture

The device provides a LBIST for E2E to guarantee the integrity of E2E logic. E2E LBIST starts automatically at power-up and can be retriggered on demand in INIT or in DIAG state.

12.2.1.3 *E2E transmission*

The E2E module shall manage two E2E protected transmitted arming message types, ARM_TX_1 and ARM_TX_2, whose data field (ARM_STATUS) is 8 bits long.

A configurable ARMing matrix shall manage the data field of each protected E2E message.

The source of the data field is generated from the status of the ARMRSLT_x bits inside the device. Each bit from ARMRSLT_x is mapped by configuration to create 8 bit data field.

For the transmitted arming message, the E2E module shall implement a 4 bit counter, incremented on every send request:

- Profile 1: the counter initializes at 0, increments to 14, and then restarts from 0.
- Profile 2: the counter initializes at 0, increments 0 to 15, and then restarts from 0.

The counter is used in the CRC calculation and is transmitted as part of the E2E protected message.

For each ARMing message sent or received, the E2E module shall calculate an 8 bit CRC according to the selected profile (inactive bits are not part of the payload), as in Table 570.

Table 570. Payload for CRC computation

profile 1 (32 bit)	0x0	DATA_ID (12 bit)	0xF	CTR (4 bit)	ARM_STATUS (8 bit)
profile 2 - short payload (24 bit)	0x0	CTR (4 bit)	ARM_STATUS (8 bit)		DATA_ID (8 bit)
profile 2 - long payload (64 bit)	0x0	CTR (4 bit)	0x0000000000	ARM_STATUS (8 bit)	DATA_ID (8 bit)

The Data_ID is used for calculating the CRC but is not transmitted with the message. It is extracted according to the E2E configuration registers.

The **sequence for E2E TX function** is the following:

1. MCU writes and reads E2E TX configuration registers.
2. MCU enables TX function and sends the REQ_E2E_TX_ARM command.
3. MCU sends the RD_E2E_TX_ARM command to read the generated TX message.

The **E2E TX flow to generate TX1/TX2 message** is the following:

- **E2E_TX_ARM_STATUS**: TX ARM status is generated according to the E2E configuration register (active bits and mapping bits) and ARM_RSLT register.
- **E2E_TX_ARM_VALIDATION**: the payload is composed to compute the CRC.

Counter is incremented every transmission request. Data ID depends on the E2E_ARM_DATA_ID_SELECTION register: it can be an element of a predefined set of data IDs (value of the counter as index to select the particular data ID used for the protection) or it is the one written in DATA_ID_VALUE register. Once that the payload is ready (counter, arm_status, data_id), the CRC is computed using the configured profile (1 or 2).

12.2.1.4 *E2E reception*

The E2E module shall manage eight E2E protected received arming message 8 bits long. For each ARM_RX_x message, a configurable arming matrix shall manage an 8-bit mask to select which bits of the arming message shall be used as inputs (by default, all bits are masked).

The arming matrix shall process external arming sources only while the device is in the SAFING state.

The E2E module shall evaluate the counter of each received arming message against the previously received message and detect the counter change from the previous message to generate status for the received frame.

Status registers are available to indicate E2E_RX message faults.

For each arming message sent or received, the E2E module shall calculate an 8 bit CRC according to the selected profile. (inactive bits are not part of the payload).

The data ID is used for calculating the CRC but is not transmitted with the message and it is extracted exactly in the same way of TX function. The **sequence for E2E RX function** is the following:

1. MCU writes and reads E2E RX configuration registers.
2. MCU enables RX function and sends the UPDATE_E2E_ARM_ST.
3. MCU sends NOP operation to check RX status bits.

The **E2E RX flow to generate ARM E2E message** is the following:

1. **E2E_RX_ARM_VALIDATION**: the received CRC is checked according to the selected profile. If the CRC_ERR_E2E = 0, in the first access the status bits and last counter is assigned to RX_counter in order to synchronize for the following messages.

   After that the initialization phase is completed, every update access, the counter of received data is compared against the counter of previously received data in order to compute the delta value:

   DELTA COUNTER = RX COUNTER - LAST RX COUNTER

   (the delta should always be ≥ 0)

   From this difference, the following status can be recognized:

   – Delta counter = 0: no new data has arrived or no new data has arrived since receiver start or the data is repeated. E2E_RX_STATUS_REPEATED (S7 bit) is setE2E_RX_STATUS_REPEATED (S7 bit) is set. E2E_RX_STATUS_REPEATED is set.

   – Delta counter = 1: counter is incremented by one (that is normal operation, no data lost). If E2E_RX_SYNC_COUNTER = 0, E2E_RX_STATUS_OK (S4 bit) is set to 1, otherwise E2E_RX_STATUS_SYNC (S3 bit) is set.

   – 1 ≤ delta counter ≤ E2E_RX_ARM_MAX_NO_NEW_OR_REPEAT_DATA: counter is incremented more than by one, but still within allowed limits (that is some data lost/skipped). E2E_RX_STATUS_OK_SOME_LOST (S6 bit) is set.

   – Delta counter > E2E_RX_ARM_MAX_NO_NEW_OR_REPEAT_DATA: counter is incremented more than threshold (that is too many data lost). E2E_RX_STATUS_WRONG_SEQUENCE (S5 bit) is set to 1.

   – For profile 1A, the device requires that the MCU/TX module must ensure that RX packets are not created with a RX counter = 15. In case of RX counter = 15, the reaction is delayed by one cycle because the next RX counter = 0 is considered as repeated (delta counter = 0).

   According to these checks, some status bits are reported (see Table 571).

Table 571. E2E RX status bits

REGISTER	STATUS BITS	DESCRIPTION
S0	E2E_RX_NEW_DATA_AVAILABLE	New update command is received
S1	E2E_RX_WAIT_FOR_FIRST_DATA	First data is received
S2	E2E_RX_STATUS_INIT	Initialization phase is completed
S3	E2E_RX_STATUS_SYNC	Synchronization error
S4	E2E_RX_STATUS_OK	Counter received is ok and no data lost
S5	E2E_RX_STATUS_OK_SOME_LOST	Current received counter is ok but some data has been lost in previous communication
S6	E2E_RX_STATUS_WRONG_SEQUENCE	Number of data lost is greater than allowed limit
S7	E2E_RX_STATUS_REPEATED	No N consecutive new data (N depends on profile)
S8	E2E_RX_CRC_ERR	CRC received is wrong

2. **E2E_RX_ARM_STATUS**: if in the previous stages there are no faults (no CRC error and RX status OK is set), the E2E ARM RX status is evaluated in order to set ARM_E2E bit that has been mapped in configuration register.

   The E2E_RX_ARM_CFG register is configured to mask bits 7:0 of the E2E_ARM_RX status to zero out unused bits received. ARM_E2E bit 7:0 will be held valid until E2E ARM DWELL timer is expired, similar to the dwell timer used for the sensor based safing logic. Once a given input bit x for the ARM_E2E_STATUS transitions from a logic 1 to a logic 0, the dwell timer for that bit x will be loaded with its configured dwell timing and begin counting down and hold the ARM_E2E_STATUS bit x to a logic 1 until the dwell timer expires (reaches 0), then transitions the bit x to a logic 0. If the ARM_E2E_STATUS input transitions back to a logic 1 while the dwell timer is active, the dwell timer counter stops counting and reset to its configured dwell timing.

The E2E_RX_ARMxy_MAPPING_CFG registers are used to remap the 8 bits result after the dwell timer has been applied to the configuration to create an 8-bit value that will be used to load the ARM_E2E_STATUS(7:0) register on the master device.

The remapped ARME2E_x bit field will be used by the master device as an input for the ARM_RSLT_STATE(7:0). The slave device updates its ARM_E2E_STATUS through snooping a read of the ARM_E2E_STATUS from the master.

12.2.2 Arming snooping logic

Both master and slave can update their ARM_RSLT_STATE by snooping the ARM information from another device (MASTER or SLAVE) or from another MCU (MCU2). The snooping logic is active in every operating state and is activated when ARM_CS_G is asserted. There will be two addresses that the device recognize when ARM_CS_G is active:

- The ARM_PSINH_INT_STATUS (0x028) of the other L9691: data from a matching address will be stored in ARM_PSINH_EXT_STATUS (0x029). In case of slave device, the additional bit ARM_DISABLE will be snooped from the master device to inhibit the arming. The ARM_DISABLE bit is set when the master device is in WD_LOCKOUT state.
- The MCU2_RESERVED_ADDRESS of the MCU2 (Table 43): data from a matching address and matching MCU2 CODE ID (1010) will be stored in ARM_PSINH_MCU2_STATUS (0x02B). When MCU request a read access to MCU2, ARM_CS_G of both master and slave devices are asserted, while their SPI_CS_G have not to be asserted otherwise the information cannot be snooped.

  In case of MCU request a read access to this register, the device will response all 0's data, in order to prevent conflict with the monitoring by the other device. The ARMMCU2_x bit can be gated by ARM_PSINH_MCU2_CTRL register: a dedicated enable, ARMMCU2_x_EN, for every ARMMCU2_x bit.

Table 572. MCU2 response to MCU read access

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI MCU1	ARM_MCU2_ADDRESS (0x02C)									WID						WPAR	WRITE DATA															
MISO MCU2	GSW															RPAR	ARM_PSINH_MCU2	X	MCU2 CODE ID				X	X	ARM_MCU2							

There is actually a third address to recognize that is only allowed by the slave device:

- The ARM_E2E_STATUS of the master device: data from a matching address will be stored in ARM_E2E_STATUS of the slave.

In addition, before to match the snooped address, the parity is checked in order to guarantee the message integrity. In case of parity check fail (WPAR or RPAR) the message is discarded.

In case of missing refresh from the monitored communication on the global SPI, the device clears all ARM_EXT bits after 2ms. Three dedicated timeouts are implemented to clear:

- ARM_PSINH_EXT_STATUS register: ARMEXT_x bits.
- ARM_E2E_STATUS register: ARME2E_x bits (only for slave device because only the slave snoops the E2E ARM bits while master includes the E2E logic).
- ARM_PSINH_MCU2_STATUS: ARMMCU2_x bits.

The timeout starts every time that the relative address is decoded by the relative snooping logic. This function can be disabled by SNOOPING_TIMEOUT_DISABLE bit in DEVICE_CTRL register.

MCU can check the snooping logic using SNOOPING_TEST_INT register. In DIAG state, MCU can write that register via global SPI and the content will be snooped by slave when master issues a read request. MCU can read SNOOPING_TEST_EXT to verify that the content will be updated with the pattern written in the SNOOPING_TEST_INT register. The same procedure can be applied for the slave device (in that case master device snoops the information by the slave). Additionally, the remote SPI has a SNOOPING_TEST_INT_RS register that may be written and then read to verify that expansion devices will be updated with the test value written to this register.

In case of SPI clock length/frame length errors or parity errors detected in the snooping logic (in MOSI command or in MISO response) by both master and slave devices, the snoop register is not updated.

12.3 Scrap vehicle arming and VSF activation

The handshake sequence for activating the arming outputs is illustrated in Figure 86:

1. The strategy involves generation of a seed value from within the device using a free-running 8-bit counter running at f_{SCRAP_SEED} rate, where it can be read by the microcontroller.
2. The microcontroller uses it to generate an 8-bit key value.
3. When the seed value is read (SCRAP_CTRL register - SEED command), device also freezes the seed value and computes its own key, which is used for comparison to the key subsequently submitted by the microcontroller.
4. The key value is submitted by the microcontroller using the SCRAP_CTRL register - KEY command (RID must be different from 0x26, otherwise a new seed value is generated), and successful reception of this command with a key value matching the internally calculated key allows the successful completion of the first handshake.
5. After that, in case a second handshake (seed-key) completes successfully and if a valid ACL is detected (as described below) the device transitions from scrap state to arming state.

To remain in arming scrap state, the microcontroller must periodically refresh device with the SCRAP_CTRL.KEY command containing the correct key value in the data field of the command, and device must also receive the correct ACL signal. [DOS_UR7S_0901308]This must occur before the scrap timeout timer expires ($T_{SCRAP\_TIMEOUT}$). The scrap key is derived from the seed value using a simple logical inversion on the even-numbered bits (0, 2, 4, 6), that is equivalent to a bit-wise XOR of the seed value with 0x55.

While the SSM is in arming scrap state, the arming outputs are asserted and VSF is enabled. If the periodic scrap key is incorrect, or not received before the timeout expires, or the ACL is not correctly received, the SSM reverts back to the scrap state, and the arming outputs are deactivated.

The ACL pin is the additional communication line input that provides a means of safely activating arming and safing switch control for disposal of restraints devices at the end of vehicle life.

The ACL pin can toggle at any time, but it will be ignored if the device is not in the SCRAP or the SCRAP_ARM states. This permits to check the ACL pin (in DIAG state) thanks to ACL_VALID flag (ACL_PSINH_STATUS). The echo of ACL pin (ACL_PIN_STATE flag) is updated with a delay of 2 ms (max).

A specific waveform needs to be present on ACL input in order to instruct device to arm all deployment loops. Device is designed to support the additional communication line (ACL) aspect of the ISO-26021 standard, which requires an independent hardwired signal (ACL) to implement the scrapping feature. The disposal signal may come from either the vehicle's service connector or the systems main microcontroller, depending on the end customer's requirements.

The arming function monitors the disposal PWM input (ACL pin) for a command to arm all loops for vehicle end-of-life airbag disposal. The disposal signal characteristic is shown in Figure 88. To remain in arming scrap state, at least three cycles of the ACL signal must be qualified (in addition to the periodic KEY value being received from the microcontroller).

For the device to qualify the periodic ACL signal, the period and duty cycle are checked. Two consecutive cycles of invalid disposal signal are to be received to disqualify the ACL signal. If the logic detects the signal is incorrect or missing while in SCRAP state, the device stays in SCRAP state; should it happen in ARMING SCRAP state, the device transitions immediately to SCRAP state. To guarantee a correct ACL timing detection, “Cycle time” must be between t_{ACL_LO} (max) and t_{ACL_HI} (min) and “on time” must be between $t_{ON\_ACL\_LO}$ (max) and $t_{ON\_ACL\_HI}$ (min).

Figure 86. **Scrap SEED-KEY state diagram**

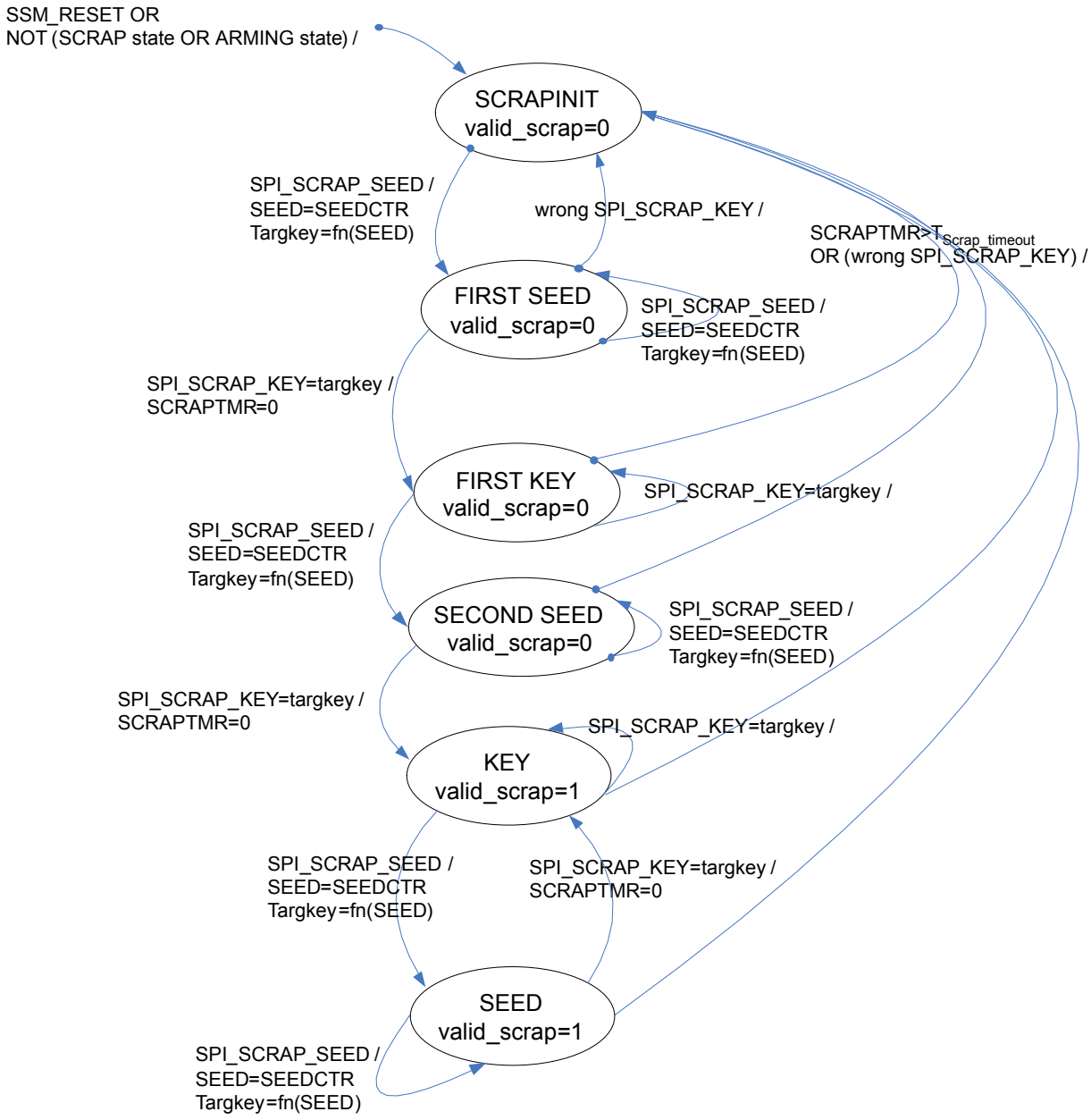


Figure 87. **Scrap ACL state diagram**

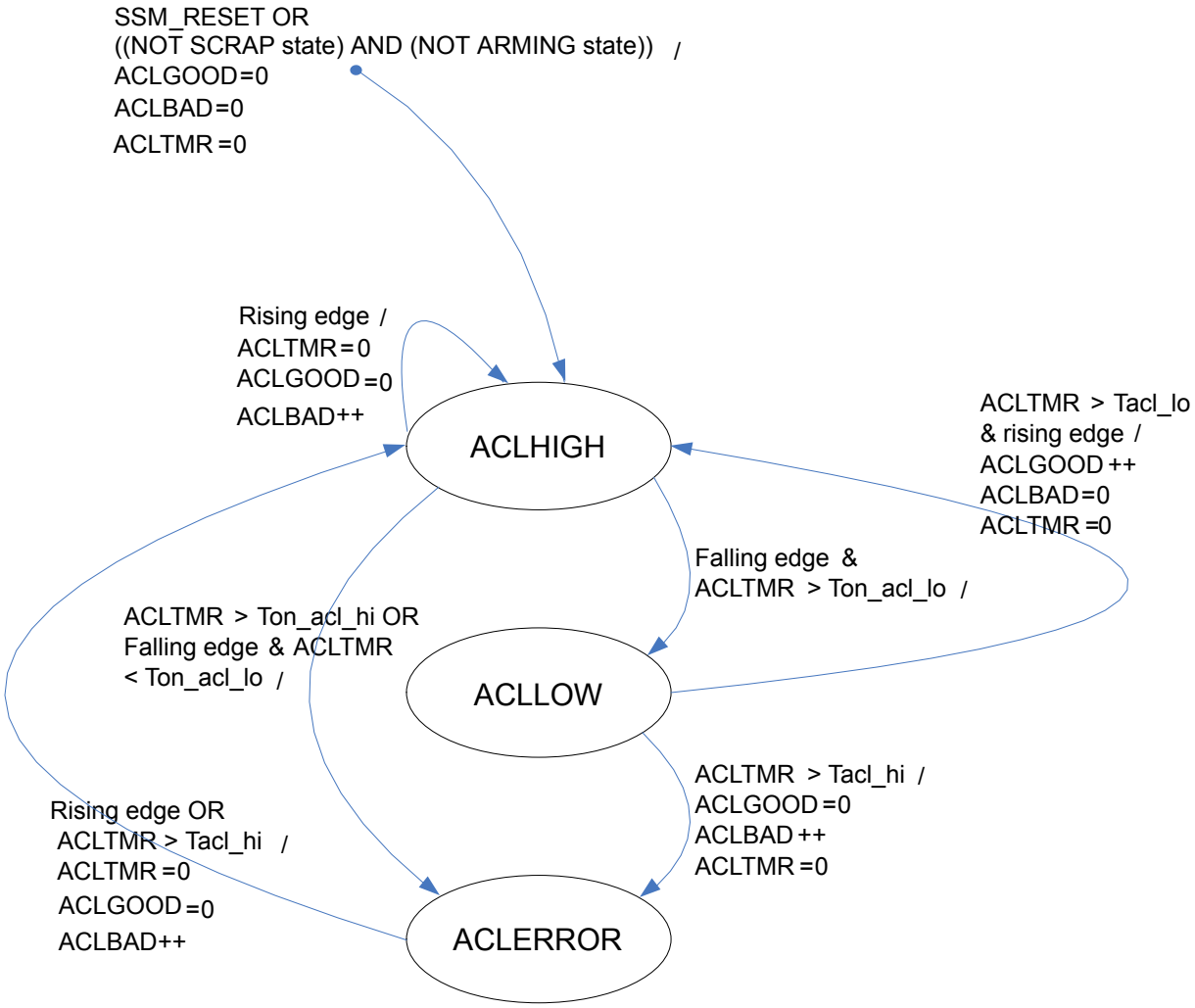
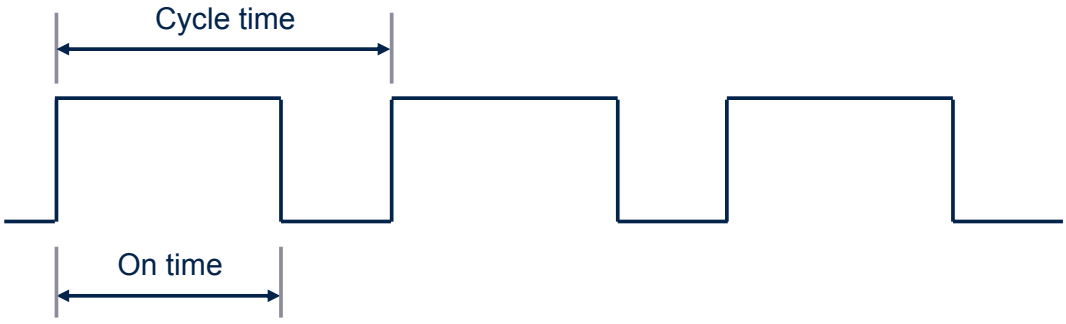


Figure 88. **Disposal PWM signal**



13 Passenger inhibit logic

13.1 Internal PSINH

13.1.1 PSINH based on DC sensor

The L9691 provides a feature to deactivate passenger restraint devices based on a preprogrammed mask. It generates a signal (DCS_PSINHINT) based on microcontroller-initiated measurements performed on the first two channels of engine 0 (DCS0 and DCS1). This concept is valid only for system basis chips. Either channel can be selected for PSINH generation by its PSINH_ENx bit in PSINH_DCS_CFG register. All DCS PSINH configurations can be performed in all the states except INIT.

The control (PAD_V_x in the PSINH_DCS_CFG) is pre-programmed to select either a voltage measurement or a current measurement on DCS0 and DCS1 for this purpose. To adapt the threshold comparison according to the supply voltage and the current limitation used for the involved DCS channel, V_PSINH_x_SEL and I_PSINH_x_SEL bits can be configured. Both bits must be configured and consistent with the involved DCS channel, regardless of whether a voltage or current measurement is programmed by PAD_V_x.

An upper and lower 10 bit threshold are preprogrammed via SPI during the DIAG state using PADTHRESH_HI_x and PADTHRESH_LO_x registers on global SPI. These thresholds define a measurement window [PADTHRESH_LO_x, PADTHRESH_HI_x]: according to the PSINH_POL_x bit setting in the PSINH_DCS_CFG register. The inhibition is asserted when a configurable number of measurements is received within the window (polarity PSINH_POL_x = 1) or out of the window (polarity PSINH_POL_x = 0). When a new DCS measurement is received, an up/down counter is updated. The counter is incremented when the sample is in the range defined by PSINH_POL. The counter is decremented when the sample is outside the range defined by the PSINH_POL. The update rate is based upon the rate that the MCU performs DCS measurements for the enabled DCSx. The number of samples required to change state (for example from inhibit to no inhibit) is configurable through PSINH_DCS0_TH_HI_SAMPLES_CFG registers. The max configurable value is 63 samples.

If no valid measurement is received before a timeout occurs, the inhibition is set (default value). This timeout is configurable through PSINH_DCS_CFG (DCS_TIMEOUT_PSINH_x) register between 0.5 s, 1 s, 2 s or 4 s.

In case of timeout expired, PSINH_DCS_EXP_TIMER is set in the ACL_PSINH_STATUS register, PSINH is asserted and the sample up/down counter is reset to the configured sample count.

In the Figure 89 is shown an example in which 4 samples are set as threshold and an in-window polarity to allow safing FET activation is chosen (PSINH = 0).

When the configured threshold is reached, PSINHINTDCSx bit field in the ACL_PSINH_STATUS register is set.

The logic permits the PSINH_DCS to potentially disable either of VSF safing regulators when PSINH_VSFx bit is set in the corresponding VSFx_CTRL register(s). The resultant PSINH must be first latched with the change to the “Deploy Enabled” state. The latched state of the PSINH signal is then used to gate the activation of the VSFx (Safing FET enable output).

Another control (PAD_V_x in the PSINH_DCS_CFG) is preprogrammed to select either a voltage measurement or a current measurement on DCS0 and DCS1 for this purpose. To adapt the threshold comparison according to the supply voltage and the current limitation used for the involved DCS channel bit V_PSINH_x_SEL and I_PSINH_x_SEL can be configured.

Figure 89. Example of PSINH control logic

Sample	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
STATE 0 (out of window)												•	•			•							
PASTHRESH_HI																							
STATE 1 (within window)	•	•	•					•	•	•	•			•	•		•				•		
PASTHRESH_LO																							
STATE 0 (out of window)				•	•	•	•											•	•	•		•	•
Counter	4	4	4	3	2	1	0	1	2	3	4	3	2	3	4	3	4	3	2	1	2	1	0
PSINH_DC	1	1	1	1	1	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0

13.1.2 PSINH based on LIN communication

The device can receive the PSINHINT LIN information through LIN bus, snooping the LIN_RX communication (see Section 11 LIN interface and decoder).

In case of OCS received by LIN, PSINHLIN bit is set.

13.2 External PSINH

Two external sources can also update the passenger inhibit result PSINHRSLT (see Figure 90) of device:

- Snooping the PSINHINT signal in the ARM_INT_STATE register of another L9691.
- Snooping the PSINH from a secondary MCU.

13.2.1 PSINH snooping logic

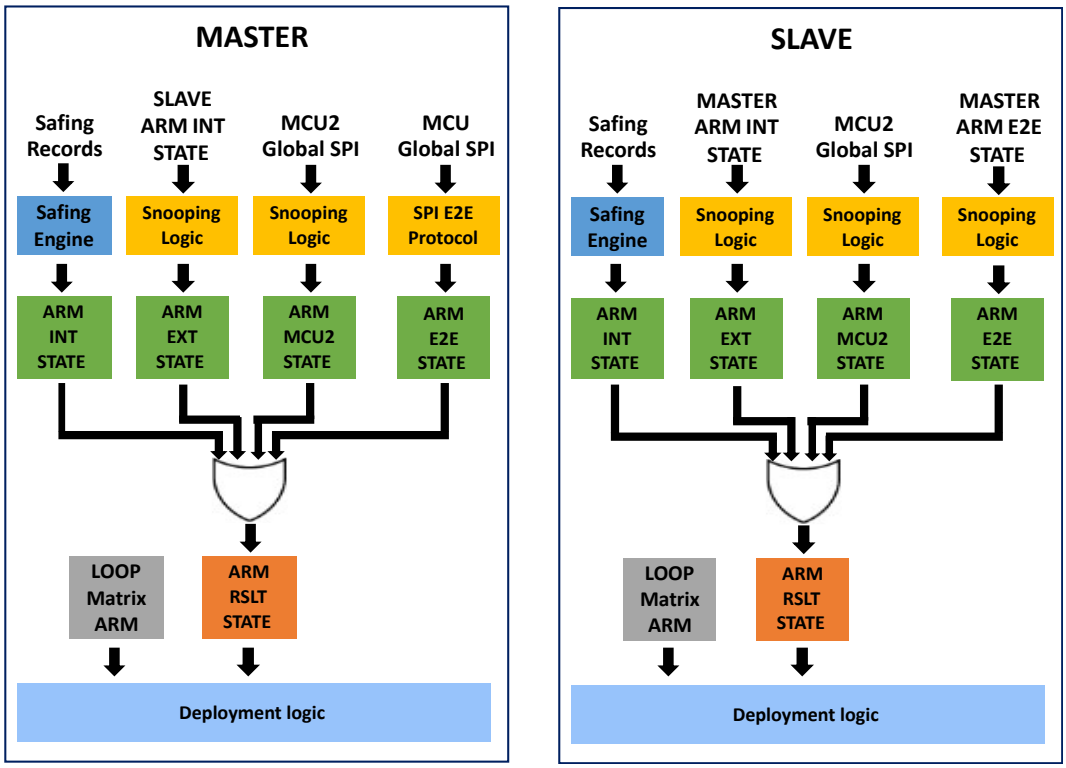
Both master and slave can update the PSINHRSLT by snooping the PSINH information from another device (master or slave) or from another MCU (MCU2). The snooping logic is activated when ARM_CS_G is asserted. The concept is exactly the same described in the arming snooping logic section, except for E2E communication, as it does not receive or transmit PSINH information.[end]

14 Arming status and passenger inhibit management

14.1 Arming status management

In a dual system, two L9691 devices in master-slave configuration can share information regarding arming conditions, and the strategy adopted is shown in Figure 90:

Figure 90. L9691 master-slave arming modes



Both master and slave have four arming sources:

- **Internal arming**, which is the result of the local safing engines according to its safing records value. The ARMINT_x state is set in the ARM_PSINH_INT_STATUS register on global SPI bus.
- **External arming**, set through SPI monitoring on the global SPI bus of the ARM_PSINH_INT_STATUS register of the other device. The resulting ARMEXT_x state is available in the ARM_PSINH_EXT_STATUS register on global SPI bus.
- **MCU2 arming**, set through SPI monitoring on the global SPI bus of arming status coming from a secondary microcontroller. The result ARMMCU2 is stored in the ARM_PSINH_MCU2_STATUS register on global SPI. Dwell timers for the ARMMCU2_x inputs are supported/maintained within the MCU2 and not on the L9691.
- **E2E arming**: only the master device can receive and decode E2E messages, thus setting its ARME2E_x state in the ARM_E2E_STATUS register according to the E2E communication. The slave device can only update its E2E ARM status via the SPI monitoring function on the global SPI of master ARM_E2E_STATUS register. Dwell timers for the E2E ARM inputs are supported within the E2E logic.

The ARM results (ARMRSLT_x) will be a bitwise OR of internal, external, MCU2 and E2E ARM states, and they are available in the ARM_RSLT_STATE register on remote sensor SPI bus through snooping operation. The ARM results (ARMRSLT_x) are forced to 0's while the ARM_DISABLE is asserted. This occurs in both the master and the slave devices.

When the ARM_RSLT_STATE register is read on the remote sensor SPI bus, the expansion device snoops the ARM_RSLT_STATE. This is used as the safing inputs for the expansion component(s). The snooping logic is active in every operating state.

When the SSM state = “ARM_SCRAP”, the ARM_RSLT_STATE will be forced to activate all ARMx within the register. The PSINH is forced to “0”. The ARM_RSLT_STATE must be read by the MCU to allow all expansion devices to snoop the ARM_RSLT_STATE for scrap vehicle deployment. This must be completed before commanding an expansion chip to deploy its squibs. While the slave device cannot snoop the master ARM_SCRAP (and vice versa), so every system basis chip must be put into ARM_SCRAP state by MCU.

Each resulting ARMRSLT_x signal is then bitwise AND-ed with the corresponding LOOP_MATRIX_ARMx register, allowing to independently select the squib loops to be armed.

ARM_RSLT_STATE.PSINHRSLT will be the latched result when DEP_ENABLED = 1 (deployment unlocked) and the unlatched PSINH result when DEP_DISABLED = 1 (deployment locked).

The ARM_x signals are also “OR’ed” together and are gated (by configuration) with the PSINH (latched value) to generate the VSFx.

14.2 Passenger inhibit management

L9691 provides a feature to deactivate passenger restraint devices and, in a master-slave system, there could be overall three passengers inhibit signal sources, as shown in Figure 91:

- **Internal PSINH signal**: a preprogrammed window comparator that generates a signal based on microcontroller-initiated measurements performed on DCS0 and DCS1, or OCS messages captured via LIN. These three sources set the internal passenger inhibit state, which will be available as PSINHINT state bit in the ARM_PSINH_INT_STATUS register on global SPI.
- **External PSINH signal**, set through SPI monitoring on the global SPI bus of the ARM_PSINH_INT_STATUS of the other device. The resulting PSINHEXT state bit is available in the ARM_PSINH_EXT_STATUS register on global SPI bus.
- **MCU2 PSINH signal**: both master and slave can capture a PSINH status from a secondary MCU by monitoring the global SPI. The resulting PSINHMCU2 state is available in the ARM_PSINH_MCU2_STATUS register.
- The E2E interface does not support a PSHINH status.

According to the logic shown in Figure 91, the resulting PSINH signal will be an OR of internal, external, and MCU2 states (if enabled); the PSINHRSLT state will be available in the ARM_RSLT_STATE register on remote sensor SPI bus.

The PSINHEXT is already gated inside the logic that has generated it.

This signal is then AND-ed with the loop matrix mask register (LOOP_MATRIX_PSINH), allowing selective deactivation of squib loops.

Figure 91. **L9691 master-slave passenger inhibit modes**

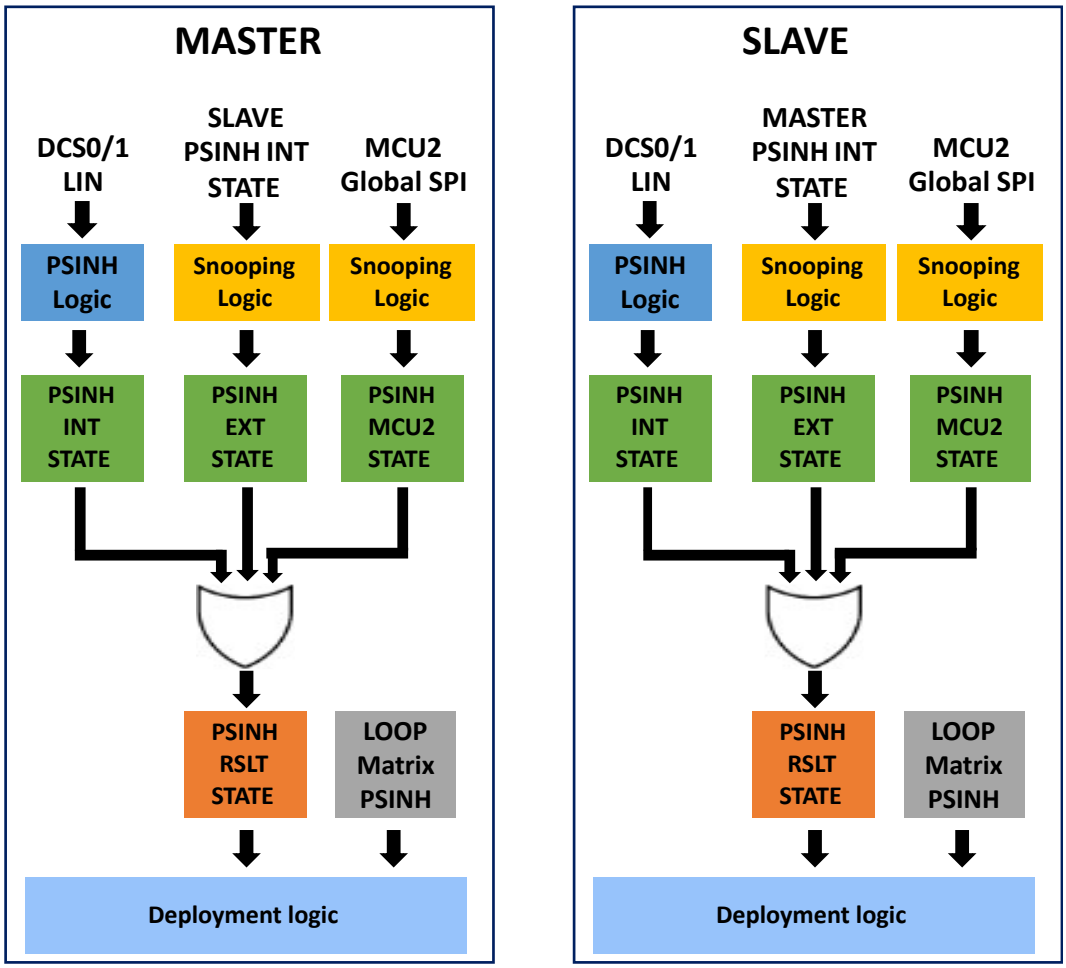
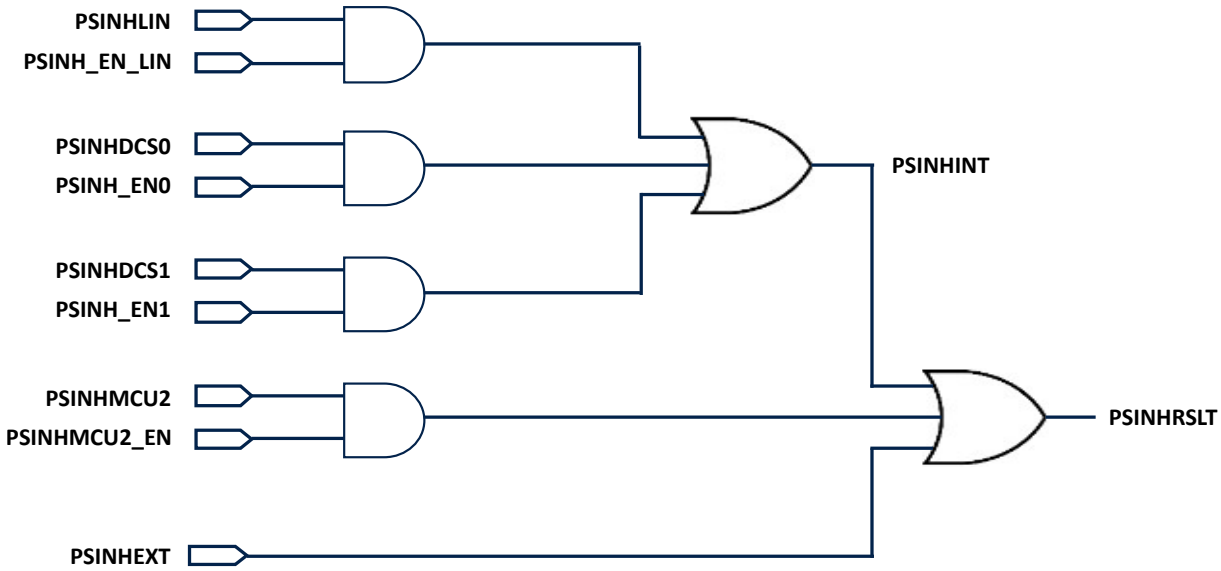


Figure 92. **PSINH logic**



15 General purpose low-side outputs

General purpose low side drivers can be independently controlled in ON (100%), OFF (0%) or PWM mode by setting the desired duty cycle through the global SPI.

The default state of all drivers is OFF and are independently activated through GPOx_CTRL SPI register. The PWM frequency is user selectable from f_{PWM_LOW} to f_{PWM_HIGH} in 25 Hz increments and the duty cycle is user selectable from 0% to 100% with increments of 0.4% through GPO_PWM field in GPOx_CTRL: when GPO_PWM value is set to 0, the output is OFF, when it is set from 250 to 255 the output will be fully ON. The frequency is programmed using the SEL_FREQ_PWM field in GPOx_CFG. The output driver is slew rate controlled. The slew rate value can be selected between two values, dV_{SRL_GPOx} and dV_{SRH_GPOx} through GPO_SEL_SR field in SPI register GPOx_CFG. There are independent GPOx_CTRL and GPOx_CFG registers for each channel.

When two GPO channels are used in PWM mode at the same frequency, they are synchronized to provide parallel configuration capability. This feature is automatically activated as soon as a write access on GPOx_CFG is performed. Every time that a write access to one of the GPOx_CFG register used in parallel configuration is performed, the PWM will be reset and resynchronized. In case one of the GPO is switched off (for example due to a fault), a write access on GPOx_CFG is needed to reactivate the parallel capability. Driver output structure is designed to withstand -1 V on GPODx.

Open load and short to ground diagnosis in OFF condition are provided using two comparators that sense output voltage. As well, undercurrent and overcurrent diagnosis in ON state are provided. The diagnostic and control block diagram are shown in Figure 93. The output is always weakly biased to ½ VIN: open load or short to ground can be diagnosed when the driver is disabled. To improve output transitioning back to a high state, the user may select a high current pull-up to VIN/2 ($I_{GPO\_DYNAMIC\_PULLUP}$), automatically activated at driver transition from ON to OFF. This pull-up is enabled through the GPO_PU_EN bit for maximum 50 µs and is automatically disabled upon the output reaches $V_{DYNAMIC\_PULLUP}$.

Output diagnostics use 2 comparators:

- One referenced to $V_{GPO\_TH\_HIGH\_X}$ for detecting when the output is higher than high level threshold
- One referenced to $V_{GPO\_TH\_LOW\_X}$ for detecting when the output is lower than low level threshold. [DOS_UR7S_0801015]

Both thresholds are configurable trough GPOx_CFG register, and there are 4 selectable values for HIGH_THRESHOLD_CONF and LOW_THRESHOLD_CONF. There are 4 fault mask times ($T_{GPO\_FLT\_MASKX}$) selectable by the user to support different battery voltages trough BLANKING_DIAG field. All diagnostic thresholds are independently selectable for each channel. The control commands and all fault status information is available in the GPOx_CTRL register.

The output voltage on all channels can be read using the power supply ADC.

All status bits (GPO_ONHI, GPO_ONLO, GPO_ON_CURRENT, GPO_OFFHI and GPO_OFFLO) are read-only over global SPI and not cleared after reading. The ON diagnostic is continuously updated only when the output is active, and kept latched during the OFF phase and during the configured blanking time. The OFF diagnostic is continuously updated only when the output is disabled, and kept latched during the ON phase and during the configured blanking time.

Blanking time is defined to allow transition of voltage due to slew rate limit. The Figure 94 shows the blanking time during the PWM activation.

Figure 93. **GPO (low side driver) block diagram**

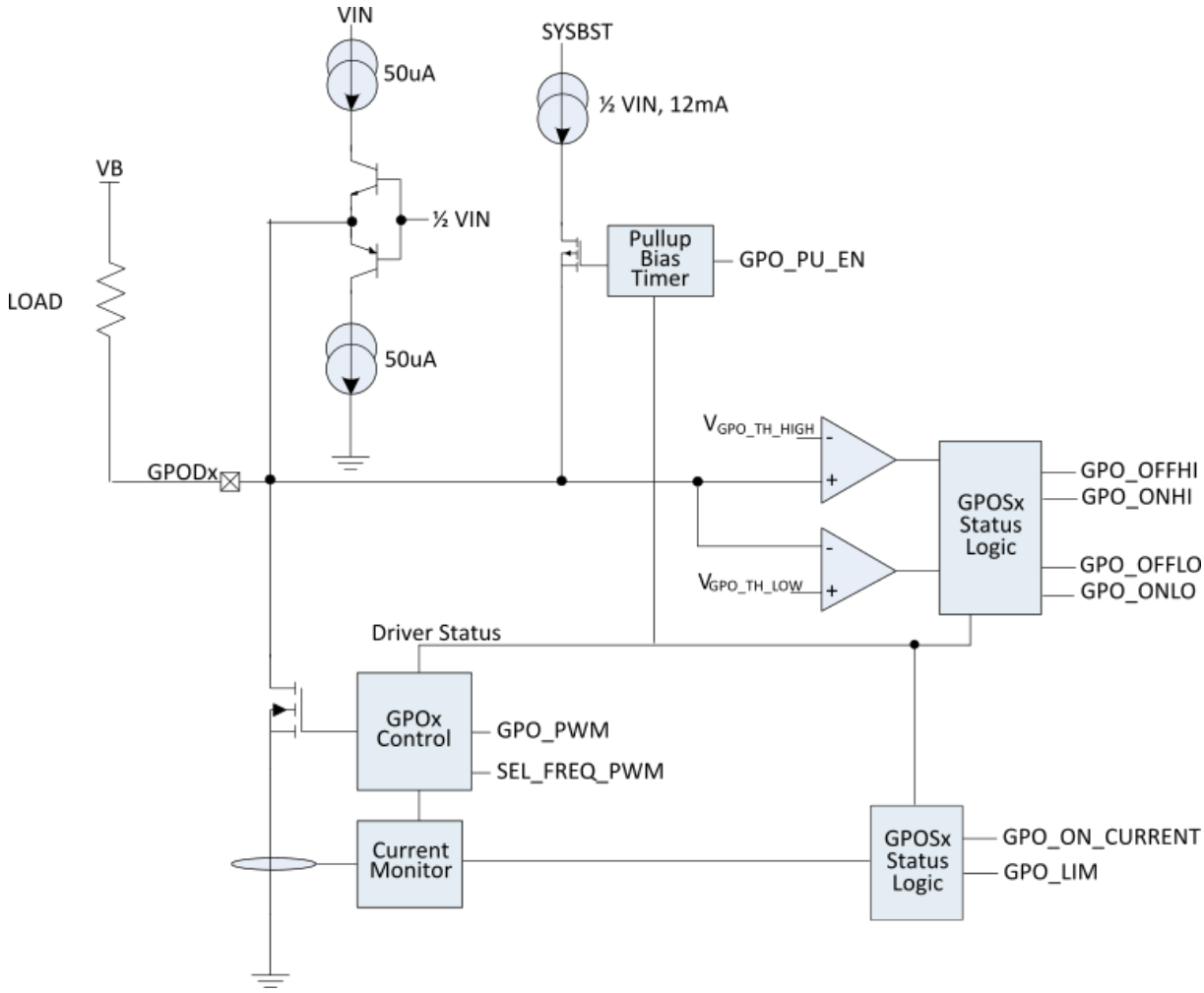
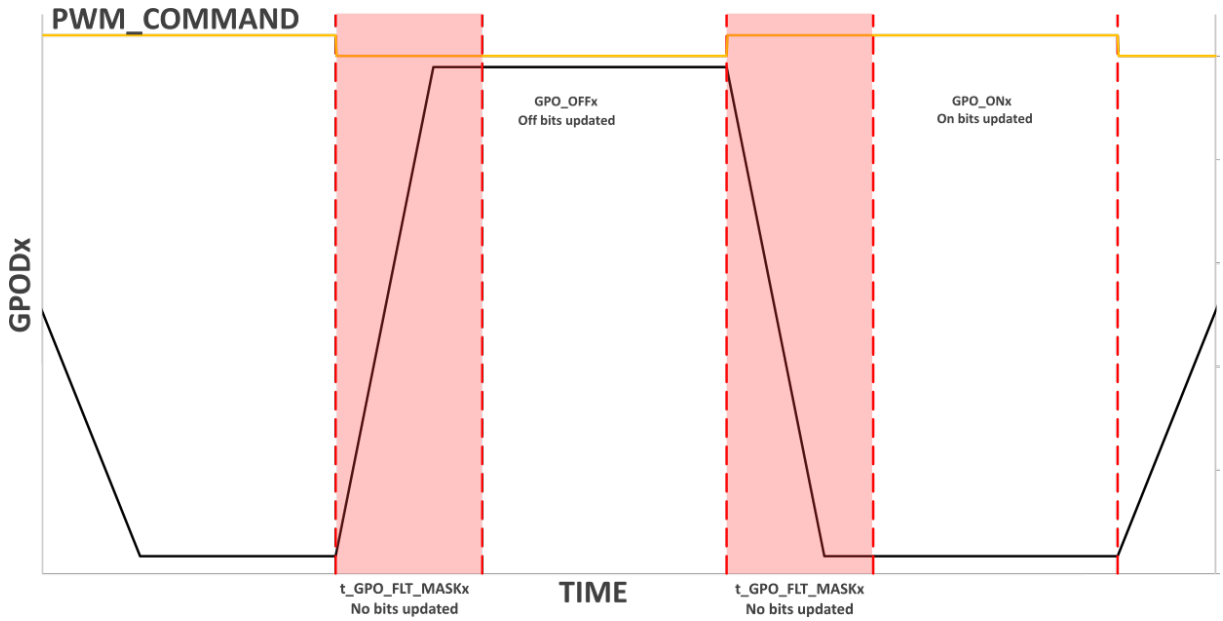


Figure 94. **Blanking time**



The GPO_ON_CURRENT flag is set when the output current is above the $I_{GPO\_ON\_TH\_X}$ selected threshold (normal operative condition). The threshold is configurable between 4 values through THRESHOLD_ON_CURR field in the GPOx_CFG register.

For current limit faults, the output driver operates in saturation region with current I_{LIM_GPO} and the GPO_LIM bit is set to 1, until a thermal fault condition is detected.

The thermal overload GPO_TEMP bit is latched after filter time $t_{GPO\_FLT\_TSD}$ until read on global SPI. Thermal overload faults will remain active after reading should the temperature remain above the thermal fault condition. Once a thermal fault is set, the driver is switched-off and an OFF-ON transition is needed to be re-enabled.

When the VIN voltage is lower than $V_{IN,GOOD}$ or higher than V_{VIN_OV}, the diagnostics is disabled and GPO_DIAG_OFF_STATUS in GPOx_CTRL register is set to 0, but the GPO output driver will continue to work: GPODx pins can be driven without VIN voltage, with loss of 50 µA pullup current and the strong pullup current.

GPO block is designed in order to avoid back-feeding of the rest of the product through the GPOx pin if a voltage is applied to it.

16 Analog to digital converters (ADCs)

16.1 Power supply ADC queue

The power supply ADC is used to provide a 10-bit digital conversion of voltages related to device supplies, regulators, and other relevant voltages for diagnostics. The several voltages are addressed with an internal multiplexer.

The power supply ADC queue is structured to take four conversions at a time through the queue mechanism: when a new request is received, it is queued if other conversions are ongoing. The conversions are executed in the same order as their request arrived in the corresponding PWR_ADC_x register. The queue is 4 measures long, so it is possible to send all 4 requests without waiting for the results. An echo of the requested voltage conversion selection code, ADCREQ_x, along with the new data flag, NEWDATA_x, are reported when conversion is completed. The NEWDATA_x is cleared when the result is read. If a new conversion request is received before the end of previous conversion, it is ignored. Actual data is cleared only when a new result is available.

The total conversion time includes the number of samples taken for any measurement and the various settling times. For maximum 4 conversion (N_{CONV}) it is:

$$t_{CONV\_TOT} = t_{PRE\_SETTL} + N_{CONV}\left(t_{CONV} \times N_S\right) + \left(N_{CONV} - 1\right)t_{INT\_SETTL} + t_{POST\_SETTL} \quad (15)$$

The number of samples, N_S, that are filtered vary depending on the chosen conversion. The number of used samples defaults to 4. The sample number can be configured using POWER_SUPPLY_ADC_MEAS_SAMPLE bits field in PWR_CTRL global SPI register.

The input voltage of ADC can be calculated with the following formula:

$$V_{IN} = \frac{ADCRES\_x}{1024} \times V_{REF\_ADC\_PWR} \times RATIO_{DIV\_x} \quad (16)$$

Table 573. Power supply ADC conversions

ADC Request (ADCREQ_x)						Voltage Measurement Selection	ADC Results (ADCRES_x)
Bit[4:0]					Hex		Bit[9:0]
0	0	0	0	0	0x00	Not available	-
0	0	0	0	1	0x01	Bandgap main, voltage	$RATIO_{DIV\_1}$
0	0	0	1	0	0x02	Bandgap diag, voltage	$RATIO_{DIV\_1}$
0	0	0	1	1	0x03	Central temperature sensor, voltage	See Section 16.1.1 Temperature sensor
0	0	1	0	0	0x04	VCOREMON pin, voltage	$RATIO_{DIV\_1}$
0	0	1	0	1	0x05	Not available	-
0	0	1	1	0	0x06	V3V3_ANA, voltage	$RATIO_{DIV\_4}$
0	0	1	1	1	0x07	V3V3_DIG, voltage	$RATIO_{DIV\_4}$
0	1	0	0	0	0x08	VCCBCK pin, voltage	$RATIO_{DIV\_4}$
0	1	0	0	1	0x09	V5_SENSE pin, voltage	$RATIO_{DIV\_4}$
0	1	0	1	0	0x0A	VIN pin, voltage low range	$RATIO_{DIV\_4}$
0	1	0	1	1	0x0B	SATBCK pin, voltage	$RATIO_{DIV\_7}$
0	1	1	0	0	0x0C	RSU_SUP_FLT pin, voltage	$RATIO_{DIV\_7}$
0	1	1	0	1	0x0D	Not available	-
0	1	1	1	0	0x0E	LIN pin, voltage	$RATIO_{DIV\_10}$

ADC Request (ADCREQ_x)						Voltage Measurement Selection	ADC Results (ADCRES_x)
Bit[4:0]					Hex		Bit[9:0]
0	1	1	1	1	0x0F	VSYNC pin, voltage	$RATIO_{DIV\_10}$
1	0	0	0	0	0x10	GPOD0 pin, voltage	$RATIO_{DIV\_10}$
1	0	0	0	1	0x11	GPOD1 pin, voltage	$RATIO_{DIV\_10}$
1	0	0	1	0	0x12	GPOD2 pin, voltage	$RATIO_{DIV\_10}$
1	0	0	1	1	0x13	WAKEUP pin, voltage	$RATIO_{DIV\_10}$
1	0	1	0	0	0x14	VIN pin, voltage	$RATIO_{DIV\_10}$
1	0	1	0	1	0x15	VBATMON pin, voltage	$RATIO_{DIV\_10}$
1	0	1	1	0	0x16	VBATSENSE pin, voltage	$RATIO_{DIV\_10}$
1	0	1	1	1	0x17	SYSBST pin, voltage	$RATIO_{DIV\_10}$
1	1	0	0	0	0x18	VER_S pad, voltage	$RATIO_{DIV\_15}$
1	1	0	0	1	0x19	ERBST pin, voltage	$RATIO_{DIV\_15}$
1	1	0	1	0	0x1A	ERSW pin, voltage	$RATIO_{DIV\_15}$
1	1	0	1	1	0x1B	ERCHSW pin, voltage	$RATIO_{DIV\_15}$
1	1	1	0	0	0x1C	ERDCHSW pin, voltage	$RATIO_{DIV\_15}$
1	1	1	0	1	0x1D	Not available	-
1	1	1	1	0	0x1E	Not available	-
1	1	1	1	1	0x1F	Not available	-

16.1.1 Temperature sensor

The L9691 provides an internal analog temperature sensor to provide the device's average junction temperature. The sensor is placed far away from power dissipating stages and squib deployment drivers. The formula to calculate temperature from ADC reading is:

$$T(^{o}C) = -332.8\frac{ADCRES\_x}{1024} + 243.5 \quad (17)$$

16.2 Sensor ADC queue

DC sensor Interface has 2 ADCs dedicated to DC sensors queue: a voltage ADC and a current ADC. The inputs are selected with an internal multiplexer, and resistor dividers to scale down the external voltage to the ADCs references.

The DC sensors voltage conversion is structured to take 4 conversions at a time through the queue mechanism: when a new request is received, it is queued if other conversions are ongoing. The conversions are executed in the same order as their request arrived in the corresponding DCS_ADC_x register. The queue is 4 measures long, so it is possible to send all 4 requests without waiting for the results. The new data flag, NEWDATA_x, is asserted when conversion is completed and cleared when the result is read. If a new conversion request is received before the end of conversion, it is ignored. Actual data is cleared only when a new result is available.

Table 574. DCS_ADC_X command

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	x	x	x	x	x	x	x	x	x	x	x	ADCREQ_x[4:0]				
MISO	NEWDATA_x	ADCRES_x[9:0]										ADCREQ_x[4:0]				

The measures requested with ADCREQ_x = 0x00-02 are specific for enabled channels. Requests on an inactive channel are dispatched, but the ADCRES_X data is not valid. DCS_ADC_A and DCS_ADC_B are dedicated to channels on Engine0, instead DCS_ADC_C and DCS_ADC_D are dedicated to channels on Engine1.

The resistance measure can be requested trough the DCS_ADC_A and DCS_ADC_C registers. The device is able to provide voltage-current measure pairs of the same channel sampled simultaneously over the same time period. The measure request stores the current data on DCS_ADC_A/C registers of the corresponding channel, and the voltage data on DCS_ADC_B/D registers. The ADCREQ_B/D field on the results echoes the ID of the active channel, displaying the voltage conversion code (0x1_CH_ID). In case of a request on an engine with all channel disabled, the code reported is 0x11111.

Table 575. Example of resistance measure on engine0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DCS_ADC_A																
MOSI	x	x	x	x	x	x	x	x	x	x	x	0x02				
MISO	NEWDATA_A	ADCRES_A[9:0]										0x02				
DCS_ADC_C																
MOSI	x	x	x	x	x	x	x	x	x	x	x	X				
MISO	NEWDATA_B	ADCRES_B[9:0]										CH_ID				

The voltage measure range is adjusted from extended V_{DCS_RANGE2} (-1.5 V to 20.5 V) to reduced V_{DCS_RANGE1} (0 V to 8 V) to improve the accuracy on resistance measure on the active channel. Also the measure range of current is changed based on the current limitation selected to improve the accuracy at low currents: with $I_{LIM\_DCS\_LOW}$ selected, the measure range is I_{DCS_RANGE1} (0 mA ~ 24 mA), with $I_{LIM\_DCS\_HIGH}$ selected, the range is extended up to I_{DCS_RANGE2} (0 mA ~ 48 mA). When the output is configured to $V_{OUT\_DCS\_SYSBST}$, the measure range is I_{DCS_RANGE1} (0 mA ~ 24 mA).

Voltage conversion formulas are the following:

$$V_{ACT} = \frac{ADCRES\_x}{1024} \times V_{REF\_ADC} \times RATIO_{ACT} \quad (18)$$

$$V_{EXT} = \frac{ADCRES\_x}{1024} \times V_{REF_{ADC}} \times RATIO_{EXT} - 1.5V \quad (19)$$

$$V_{RSU} = \frac{ADCRES\_x}{1024} \times V_{REF\_ADC} \times RATIO_{RSU} \quad (20)$$

$$V_{VER} = \frac{ADCRES\_x}{1024} \times V_{REF\_ADC} \times RATIO_{VER} \quad (21)$$

Current conversion formulas are the following:

$$I_{\mathrm{CURR\_LOW}} = \frac{ADCRES\_x}{1024} \times I_{REF\_ADC} \times RATIO_{\mathrm{CURR\_LOW}}$$

$$I_{\mathrm{CURR\_HIGH}} = \frac{ADCRES\_x}{1024} \times I_{REF\_ADC} \times RATIO_{\mathrm{CURR\_HIGH}}$$

The output measures are obtained averaging multiple ADC conversions. The integration period is user selectable through DCS_MEAS field (default 0b10) in DCS_DIAG_CFG register. Before the request of a new conversion, the default sampling time is $t_{S\_DCS\_2}$ (73 µs). The resistor divider used to measure the extended range voltage V_{EXT} is connected to the selected channel only for the sampling time.

The conversion of an internal current, I_{CURR_MON}, independent from the ADC's current reference, can be requested through ADCREQ 0x1C, and the results can be compared to the expected value to validate the integrity of ADC conversion.

Table 576. DCS measures list

ADC Request (ADCREQ_x)						Voltage Measurement Selection	ADC Results (ADCRES_x)
Bit[4:0]					Hex		Bit[9:0]
0	0	0	0	0	0x00	DC sensor ch. selected, voltage	V_{ACT}

ADC Request (ADCREQ_x)						Voltage Measurement Selection	ADC Results (ADCRES_x)
Bit[4:0]					Hex		Bit[9:0]
0	0	0	0	1	0x01	DC sensor ch. selected, current	I_{CURR_LOW} or I_{CURR_HIGH}
0	0	0	1	0	0x02	DC sensor ch. selected, resistance	(I_{CURR_LOW} or I_{CURR_HIGH}) and V_{ACT}
0	0	0	1	1	0x03	DC sensor cross-connect check(1)	See Table 555
0	0	1	0	0	0x04	RSU0, voltage	V_{RSU}
0	0	1	0	1	0x05	RSU1, voltage	V_{RSU}
0	0	1	1	0	0x06	RSU2, voltage	V_{RSU}
0	0	1	1	1	0x07	RSU3, voltage	V_{RSU}
0	1	0	0	0	0x08	RSU4, voltage	V_{RSU}
0	1	0	0	1	0x09	RSU5, voltage	V_{RSU}
0	1	0	1	0	0x0A	RSU6, voltage	V_{RSU}
0	1	0	1	1	0x0B	RSU7, voltage	V_{RSU}
0	1	1	0	0	0x0C	Not available	-
0	1	1	0	1	0x0D	Not available	-
0	1	1	1	0	0x0E	Not available	-
0	1	1	1	1	0x0F	VER voltage (measure on force pad)	V_{VER}
1	0	0	0	0	0x10	DC sensor ch. 0, voltage	V_{EXT}
1	0	0	0	1	0x11	DC sensor ch. 1, voltage	V_{EXT}
1	0	0	1	0	0x12	DC sensor ch. 2, voltage	V_{EXT}
1	0	0	1	1	0x13	DC sensor ch. 3, voltage	V_{EXT}
1	0	1	0	0	0x14	DC sensor ch. 4, voltage	V_{EXT}
1	0	1	0	1	0x15	DC sensor ch. 5, voltage	V_{EXT}
1	0	1	1	0	0x16	DC sensor ch. 6, voltage	V_{EXT}
1	0	1	1	1	0x17	DC sensor ch. 7, voltage	V_{EXT}
1	1	0	0	0	0x18	DC sensor ch. 8, voltage	V_{EXT}
1	1	0	0	1	0x19	DC sensor ch. 9, voltage	V_{EXT}
1	1	0	1	0	0x1A	DC sensor ch. 10, voltage	V_{EXT}
1	1	0	1	1	0x1B	DC sensor ch. 11, voltage	V_{EXT}
1	1	1	0	0	0x1C	Current monitor	I_{CURR_MON}
1	1	1	0	1	0x1D	Not available	-
1	1	1	1	0	0x1E	Not available	-
1	1	1	1	1	0x1F	Not available	-

1. *Writing the request for cross connect check will start the automated diagnostics for DC sensors.*

16.3 Deployment ADC queue

The deployment A/D converter is used to provide a 10-bit digital conversion of voltages related to device deployment section. The several voltages are addressed with an internal analog multiplexer.

10-bit A/D voltage conversion is requested and read through DEP_DIAG_ADC_A and DEP_DIAG_ADC_B global SPI registers. The bit fields, used to address the different measurements, are listed in Table 577.
All diagnostics results are available on the DEP_DIAG_ADC_RES_x bits when addressed by the related DEP_DIAG_ADC_REQ_x bits.

Each NEWDATA_x flag located in DEP_DIAG_ADC_x register is asserted when conversion is finished, and cleared when result is read out. The result DEP_DIAG_ADC_RES_x is cleared only when new result for that register is available. When a new request is received, it is rejected if other conversions are ongoing.

The relation between conversion code and input voltage is given by the following equation:

$$CONV_{ADC\_DEP} = 1024 \times \frac{V_{IN\_ADC}}{V_{DEP\_ADC\_REF}} \quad (22)$$

Where V_{IN_ADC} is the A/D input voltage and $V_{DEP\_ADC\_REF}$ is A/D reference voltage.

A single conversion is performed within $t_{DEP\_ADC\_CONV}$ total time. The total conversion time includes the number of samples taken for any one measurement and the various settling times:

The number of samples, N_S, that are filtered vary depending on the chosen conversion. The number of samples for all other measurements defaults to 8. The sample number can be configured using DEP_ADC_MEAS_SAMPLE bits in DEP_CTRL global SPI register.

Table 577. Deployment A/D conversions

ADC Request [Hex] (DEP_DIAG_ADC_REQ_x)	ADC Results (DEP_DIAG_ADC_RES_A)	ADC Results (DEP_DIAG_ADC_RES_B)
00	Reserved	Reserved
01	SR0 voltage	SR8 voltage
02	SF0 voltage	SF8 voltage
03	SS0 voltage	SS8 voltage
04	SR1 voltage	SR9 voltage
05	SF1 voltage	SF9 voltage
06	SS1 voltage	SS9 voltage
07	SR2 voltage	SR10 voltage
08	SF2 voltage	SF10 voltage
09	SS2 voltage	SS10 voltage
0A	SR3 voltage	SR11 voltage
0B	SF3 voltage	SF11 voltage
0C	SS3 voltage	SS11 voltage
0D	SR4 voltage	SR12 voltage
0E	SF4 voltage	SF12 voltage
0F	SS4 voltage	SS12 voltage
10	SR5 voltage	SR13 voltage
11	SF5 voltage	SF13 voltage
12	SS5 voltage	SS13 voltage
13	SR6 voltage	SR14 voltage
14	SF6 voltage	SF14 voltage
15	SS6 voltage	SS14 voltage
16	SR7 voltage	SR15 voltage
17	SF7 voltage	SF15 voltage
18	SS7 voltage	SS15 voltage

ADC Request [Hex] (DEP_DIAG_ADC_REQ_x)	ADC Results (DEP_DIAG_ADC_RES_A)	ADC Results (DEP_DIAG_ADC_RES_B)
19	V_{O_VRCM}	I_{O_VRCM}
1A	VSF_D voltage	V_{OUT_LRM}
1B	VSF0_G voltage	VSF1_G voltage
1C	VSF0_S voltage	VSF1_S voltage
1D	TEST voltage	Reserved

The only exception is given by V_{O_VRCM} and I_{O_VRCM} conversions: in this case, the measurements of voltage and current will be available simultaneously on the related bit field result DEP_DIAG_ADC_RES_A and DEP_DIAG_ADC_RES_B with one single request addressed through DEP_DIAG_ADC_REQ_A bits.

Proper scaling is necessary for various measurements. The divider ratios vary by measurement and are summarized by function in Table 578.

Table 578. Deployment voltage divider ratios

Measurements	Divider Ratio		
	15:1	4:1	1:1
SRx	✓	-	-
SFx	✓	-	-
SSx	✓	-	-
V_{O_VRCM}	-	✓	-
V_{OUT_LRM}	-	-	✓
TEST	-	✓	-

17 Electrical characteristics

17.1 Main features

17.1.1 Power supply and power mode control

-40 °C < T_J < 175 °C, unless otherwise noted.

Table 579. Power supply and power mode control electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
I_{VIN_OFF}	VIN pin current in OFF state	-	-5	-	5	µA	VIN
I_{SYSBST_OFF}	SYSBST pin current in OFF state	$V_{WAKEUP} < V_{WU\_MON\_H}$ $V_{VBATMON} < V_{WU\_MON\_H}$	-10	-	10	µA	SYSBST
V_{SYSBST_ALIVE}	SYSBST pin voltage minimum value for wakeup monitor correct operation	-	-	-	4.2	V	SYSBST
$V_{WAKEUP\_MON\_H}$	WAKEUP pin voltage threshold to initiate OFF → WAKEUP MONITOR transition	$V_{SYSBST} > V_{SYSBST\_ALIVE}$	1.3	-	2.42	V	WAKEUP
$V_{WAKEUP\_MON\_L}$	WAKEUP pin voltage threshold to initiate WAKEUP MONITOR → OFF transition	$V_{SYSBST} > V_{SYSBST\_ALIVE}$	0.5	-	1.2	V	WAKEUP
$V_{VBATMON\_MON\_H}$	VBATMON pin voltage threshold to initiate OFF → WAKEUP MONITOR transition	$V_{SYSBST} > V_{SYSBST\_ALIVE}$	1.3	-	2.42	V	VBATMON
$V_{VBATMON\_MON\_L}$	VBATMON pin voltage threshold to initiate WAKEUP MONITOR → OFF transition	$V_{SYSBST} > V_{SYSBST\_ALIVE}$	0.5	-	1.2	V	VBATMON
$I_{VIN\_WU\_MON}$	VIN pin current in WAKEUP MONITOR state	$V_{SYSBST} > V_{SYSBST\_ALIVE}$	-	230	300	µA	VIN
$I_{SYSBST\_WU\_MON}$	SYSBST pin current in WAKEUP MONITOR state	$V_{SYSBST} > V_{SYSBST\_ALIVE}$	-	2	3	mA	SYSBST
$V_{WAKEUP\_VALID\_H}$	WAKEUP pin voltage threshold to initiate WAKEUP MONITOR → WAKEUP VALID transition	$V_{SYSBST} > V_{SYSBST\_ALIVE}$	2.8	3	3.15	V	WAKEUP
$V_{WAKEUP\_VALID\_L}$	WAKEUP pin voltage threshold to initiate WAKEUP VALID → WAKEUP MONITOR transition	$V_{SYSBST} > V_{SYSBST\_ALIVE}$	2.34	2.5	2.65	V	WAKEUP
$V_{VBATMON\_VALID\_H}$	VBATMON pin voltage threshold to initiate WAKEUP MONITOR → WAKEUP VALID transition	$V_{SYSBST} > V_{SYSBST\_ALIVE}$	2.8	3	3.15	V	VBATMON
$V_{VBATMON\_VALID\_L}$	VBATMON pin voltage threshold to initiate WAKEUP VALID → WAKEUP MONITOR transition	$V_{SYSBST} > V_{SYSBST\_ALIVE}$	2.34	2.5	2.65	V	VBATMON
V_{VIN_ALIVE}	VIN pin voltage minimum value for internal regulators correct operation	-	-	-	4.8	V	VIN

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
$I_{VIN\_WU\_VALID}$	VIN pin current in WAKEUP VALID state	$V_{SYSBST} > V_{SYSBST\_ALIVE}$ $V_{VIN} > V_{VIN\_ALIVE}$	32	-	70	mA	VIN
$I_{SYSBST\_WU\_VALID}$	SYSBST pin current in WAKEUP VALID state	$V_{SYSBST} > V_{SYSBST\_ALIVE}$ $V_{VIN} > V_{VIN\_ALIVE}$	2	-	5	mA	SYSBST
$I_{ERBST\_VSF\_OFF}$	ERBST pin current with both VSF regulators disabled	ERBST = 33 V ERBST_EN = 1	-	0.65	-	mA	ERBST
$I_{ERBST\_VSF\_ON}$	ERBST pin current with both VSF regulators enabled	ERBST = 33 V ERBST_EN = 1	-	4	-	mA	ERBST
I_{SYSBST_INT}	SYSBST pin current without SATBCK consumption	SATBCK disabled, design info	-	7	10	mA	SYSBST
$I_{VIN\_WU\_LATCHED}$	VIN pin current in WAKEUP LATCHED state	$V_{SATBCK} > V_{SATBCK\_UV}$	0.5	-	1.2	mA	VIN
V_{VIN_GOOD}	VIN value to initiate WAKEUP VALID → STARTUP transition	-	5	-	5.4	V	VIN
V_{VIN_BAD}	VIN value to initiate STARTUP → WAKEUP VALID transition	-	4.0	-	4.5	V	VIN
V_{VIN_OV}	VIN overvoltage threshold	-	19.5	-	21.5	V	VIN
$I_{LKG\_VIN\_25C}$	VIN pin current in OFF state at 25°C	OFF state, T_J = 25 °C VIN = 13 V	-0.2	-	0.2	µA	VIN
$I_{LKG\_VIN\_85C}$	VIN pin current in OFF state at 85°C	OFF state, T_J = 85 °C VIN = 13 V	-0.5	-	0.5	µA	VIN
$I_{LKG\_VBATSENSE}$	VBATSENSE pin current in OFF state	OFF state VBATSENSE = 13 V	-5	-	5	µA	VBATSENSE
$I_{LKG\_VBATSENSE\_25C}$	VBATSENSE pin current in OFF state at 25°C	OFF state T_J = 25 °C VBATSENSE = 13 V	-0.1	-	0.1	µA	VBATSENSE
$I_{LKG\_VBATSENSE\_85C}$	VBATSENSE pin current in OFF state at 85°C	OFF state T_J = 85 °C VBATSENSE = 13 V	-0.5	-	0.5	µA	VBATSENSE
$I_{LKG\_SYSBST\_25C}$	SYSBST pin current in OFF state at 25°C	OFF state T_J = 25 °C SYSBST = 13V	-0.4	-	0.4	µA	SYSBST
$I_{LKG\_SYSBST\_85C}$	SYSBST pin current in OFF state at 85°C	OFF state T_J = 85 °C SYSBST = 13V	-2	-	2	µA	SYSBST
$I_{LKG\_SYSBSTSW}$	SYSBSTSW pin current in OFF state	OFF state SYSBSTSW = 13 V	-20	-	20	µA	SYSBSTSW
$I_{LKG\_SYSBSTSW\_25C}$	SYSBSTSW pin current in OFF state at 25°C	OFF state T_J = 25 °C SYSBSTSW = 13 V	-0.4	-	0.4	µA	SYSBSTSW
$I_{LKG\_SYSBSTSW\_85C}$	SYSBSTSW pin current in OFF state at 85°C	OFF state T_J = 85 °C SYSBSTSW = 13 V	-2	-	2	µA	SYSBSTSW

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
I_{LKG_ERBST}	ERBST pin current in OFF state	OFF state ERBST = 13 V	-5	-	5	µA	ERBST
$I_{LKG\_ERBST\_25C}$	ERBST pin current in OFF state at 25°C	OFF state T_J = 25 °C ERBST = 13 V	-0.1	-	0.1	µA	ERBST
$I_{LKG\_ERBST\_85C}$	ERBST pin current in OFF state at 85°C	OFF state T_J = 85 °C ERBST = 13 V	-0.5	-	0.5	µA	ERBST
$I_{LKG\_ERBSTSW}$	ERBSTSW pin current in OFF state	OFF state ERBSTSW = 13 V	-5	-	5	µA	ERBSTSW
$I_{LKG\_ERBSTSW\_25C}$	ERBSTSW pin current in OFF state at 25°C	OFF state T_J = 25 °C ERBSTSW = 13 V	-0.1	-	0.1	µA	ERBSTSW
$I_{LKG\_ERBSTSW\_85C}$	ERBSTSW pin current in OFF state at 85°C	OFF state T_J = 85 °C ERBSTSW = 13 V	-0.5	-	0.5	µA	ERBSTSW
I_{LKG_ERSW}	ERSW pin current in OFF state	OFF state ERSW = 13 V	-10	-	10	µA	ERSW
$I_{LKG\_ERSW\_25C}$	ERSW pin current in OFF state at 25°C	OFF state T_J = 25 °C ERSW = 13 V	-0.2	-	0.2	µA	ERSW
$I_{LKG\_ERSW\_85C}$	ERSW pin current in OFF state at 85°C	OFF state T_J = 85 °C ERSW = 13 V	-1	-	1	µA	ERSW
$I_{LKG\_VSF\_D}$	VSF_D pin current in OFF state	OFF state VSF_D = 13 V	-1	-	1	µA	VSF_D
$I_{LKG\_VSF\_D\_25C}$	VSF_D pin current in OFF state at 25°C	OFF state T_J = 25 °C VSF_D = 13 V	-0.1	-	0.1	µA	VSF_D
$I_{LKG\_VSF\_D\_85C}$	VSF_D pin current in OFF state at 85°C	OFF state T_J = 85 °C VSF_D = 13 V	-0.1	-	0.1	µA	VSF_D
R_{IN_WAKEUP}	WAKEUP pin input resistance to ground	OFF state	150	-	270	kΩ	WAKEUP
$R_{IN\_VBATMON}$	VBATMON pin input resistance to ground	OFF state	150	-	270	kΩ	VBATMON
$t_{WU\_VALID\_FLT}$	WAKEUP or VBATMON pin voltage valid threshold filter time	-	0.9	1	1.2	ms	WAKEUP, VBATMON
$t_{WU\_VALID\_LTCH}$	STARTUP → WAKEUP LATCHED transition time	-	2.4	3	3.4	ms	WAKEUP, VBATMON
$t_{VIN\_GOOD\_FLT}$	VIN voltage recovery time to initiate ER → WAKEUP LATCHED transition (V_{VIN} > V_{VIN_GOOD})	-	8.5	10	11.5	ms	VIN

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
$t_{RESET\_N\_FLT}$	RESET_N filter time, initiates WAKEUP LATCHED → SHUTDOWN transition	-	0.8	1	1.2	s	RESET_N
$t_{SHUTDOWN\_TO}$	Permanence in SHUTDOWN state timeout, initiates SHUTDOWN → OFF transition	-	50	60	70	s	-
$t_{RISE\_VIN\_GOOD}$	VIN good thresholds deglitch filter time rising edge	-	2.3	3	3.5	µs	VIN
$t_{FALL\_VIN\_GOOD}$	VIN good thresholds deglitch filter time falling edge	-	1.7	2	2.5	µs	VIN
$t_{RISE\_VIN\_BAD}$	VIN Bad thresholds deglitch filter time rising edge	-	2.2	3	3.4	µs	VIN
$t_{FALL\_VIN\_BAD}$	VIN Bad thresholds deglitch filter time falling edge	-	21	26	31	µs	VIN
$V_{AGND\_LOSS\_TH}$	AGND ground loss detection threshold	$V_{SUBGNDx}$ = 0 V	100	200	300	mV	AGND
t_{LBIST}	Logic BIST duration	-	18	19	20	ms	-
t_{MBIST}	Memory BIST duration	-	3.8	4	4.3	ms	-
$t_{SAFING\_SCRAP\_TO}$	Safing scrap timeout	-	4.4	5	5.3	s	-

17.1.2 Internal regulators and nPOR generation

-40 °C < T_J < 175 °C, unless otherwise noted.

Table 580. Internal regulators and nPOR generation electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
V_{BG_MAIN}	Bandgap reference	Accuracy after trimming	1.188	1.2	1.212	V	-
V_{BG_MON}	Bandgap monitor	Accuracy after trimming	1.188	1.2	1.212	V	-
V_{V3V3_ANA}	Voltage of internal analog supply	-	3.1	3.3	3.5	V	-
V_{V3V0_DIG}	Voltage of internal digital supply provided by V3V0 DIG reg	V_{VCCBCK} = 0 V	2.8	3.0	3.2	V	-
V_{V3V3_DIG}	Voltage of internal digital supply provided by VCC buck	V_{VCCBCK} = 3.3 V	3.1	3.25	3.3	V	-

17.1.3 Oscillators, FLL function and CLKSW usage

-40 °C < T_J < 175 °C, unless otherwise noted.

Table 581. Oscillators, FLL function and CLKSW usage electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
f_{OSC}	Main oscillator average frequency - no FLL	Accuracy after trimming	15.2	16	16.8	MHz	-
f_{OSC}	Main oscillator average frequency, with FLL	Accuracy with FLL enabled, considering ±1% of ext clock and ±0.3% of loop error	15.8	16	16.2	MHz	-
f_{MOD_OSC}	Main oscillator modulation frequency	-	-	$\frac{f_{OSC}}{128}$	-	MHz	-

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
I_{MOD_OSC}	Main oscillator modulation index	-	2.5	3	5	%	-
f_{AUX}	Auxiliary (monitor) oscillator average frequency	Accuracy after trimming	9.5	10	10.5	MHz	-
$f_{OSC\_LOW\_TH}$	Main oscillator low frequency detection threshold	-	-	-15%	-	MHz	-
$f_{OSC\_HIGH\_TH}$	Main oscillator high frequency detection threshold	-	-	+15%	-	MHz	-
T_{FLL_LOCK}	FLL timing lock	SPI_FLL_EN = 1	-	2	-	ms	-
$T_{DLY\_CLKSW\_SYSBSTSW}$	Delay between CLKSW rising edge and SYSBSTSW falling edge	SYBST_PH_SEL = 0 Design info	-	260	-	ns	CLKSW SYSBSTSW
$T_{DLY\_CLKSW\_ERBSTSW}$	Delay between CLKSW rising edge and ERBSTSW falling edge	ERBST_PH_SEL = 0 Design info	-	260	-	ns	CLKSW ERBSTSW
$T_{DLY\_CLKSW\_SATBCK}$	Delay between CLKSW rising edge and SATBCKSW rising edge	SATBCK_PH_SEL = 0 Design info	-	320	-	ns	CLKSW SATBCK
$T_{DLY\_CLKSW\_VCCBCK}$	Delay between CLKSW rising edge and VCCBCKSW rising edge	VCCBCK_PH_SEL = 0 Design info	-	320	-	ns	CLKSW VCCBCK

17.1.4 Watchdog

-40 °C < T_J < 175 °C, ACTIVE or PASSIVE mode, unless otherwise noted.

Table 582. Watchdog electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
$t_{WDT\_TIMEOUT1}$	Temporal watchdog timeout 1	-	-	-	2.00	ms	-
$t_{WDT\_TIMEOUT2}$	Temporal watchdog timeout 2	-	-	-	16.3	ms	-
t_{WDT_RST}	Temporal watchdog reset time	-	0.9	1.0	1.1	ms	-

17.1.5 Reset control

-40 °C < T_J < 175 °C, unless otherwise noted.

Table 583. Reset control electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
$V_{OH\_RESET\_N}$	RESET_N high level output voltage	Valid for master device only I_{LOAD} = -2.0 mA	V_{VCCBCK} - 0.4	-	V_{VCCBCK}	V	VCCBCK, RESET_N
$V_{OL\_RESET\_N}$	RESET_N low level output voltage	I_{LOAD} = 2.0 mA	0	-	0.4	V	RESET_N
$R_{PD\_RESET\_N}$	RESET_N pull-down resistance	-	65	100	135	kΩ	RESET_N
$V_{IH\_RESET\_N}$	RESET_N high level input voltage	Valid for slave device only	2	-	-	V	RESET_N

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
$V_{IL\_RESET\_N}$	RESET_N low level input voltage	Valid for slave device only	-	-	0.8	V	RESET_N
t_{HOLD_RESET}	RESET_N hold time	-	0.9	1	1.1	ms	RESET_N
$t_{RISE\_RESET\_N}$	RESET_N rise time	50 pF load 20% - 80%, valid for master only	-	-	1.00	µs	RESET_N
$t_{FALL\_RESET\_N}$	RESET_N fall time	50 pF load, 20% - 80%	-	-	1.00	µs	RESET_N

17.1.6 Digital I/O

-40 °C < T_J < 175 °C, unless otherwise noted.

Table 584. Digital I/O electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
$V_{IH\_DIG\_IO}$	High level input voltage	-	2	-	-	V	-
[$V_{IL\_DIG\_IO}$	Low level input voltage	-	-	-	0.8	V	-
$R_{PU\_DIG\_IO}$	Pull-up resistor	At 2 V on pin	60	100	140	kΩ	-
$R_{PD\_DIG\_IO}$	Pull-down resistor	At 1 V on pin	60	100	140	kΩ	-
$V_{OH\_DIG\_IO}$	High level output voltage	I_{LOAD} = -2 mA	V_{VCCBCK} -0.4	-	V_{VCCBCK}	V	-
$V_{OL\_DIG\_IO}$	Low level output voltage	I_{LOAD} = 2.0 mA	-	-	0.4	V	-
$t_{R\_SPI\_FAST}$	Rise time	DIG_IO_SPEED = 1 20% to 80% of VCCBCK 100 pF load	-	-	11.5	ns	SPI_MISO_G SPI_MISO_RS
$t_{F\_SPI\_FAST}$	Fall time	DIG_IO_SPEED = 1 20% to 80% of VCCBCK 100 pF load	-	-	11.5	ns	SPI_MISO_G SPI_MISO_RS
$t_{R\_SPI\_SLOW}$	Rise time	DIG_IO_SPEED = 1 20% to 80% of VCCBCK 100 pF load	-	-	22	ns	SPI_MISO_G SPI_MISO_RS
$t_{F\_SPI\_SLOW}$	Fall time	DIG_IO_SPEED = 1 20% to 80% of VCCBCK 100 pF load	-	-	22	ns	SPI_MISO_G SPI_MISO_RS
t_{R_DIGOUT}	Rise time	20% to 80% of VCCBCK 50 pF load	-	-	30	ns	COVRACT CLKSW LIN_RX
t_{F_DIGOUT}	Fall time	80% to 20% of VCCBCK 50 pF load	-	-	30	ns	COVRACT CLKSW LIN_RX

17.2 Serial peripheral interface (SPI)

-40 °C < T_J < 175 °C, ACTIVE or PASSIVE mode, unless otherwise noted.

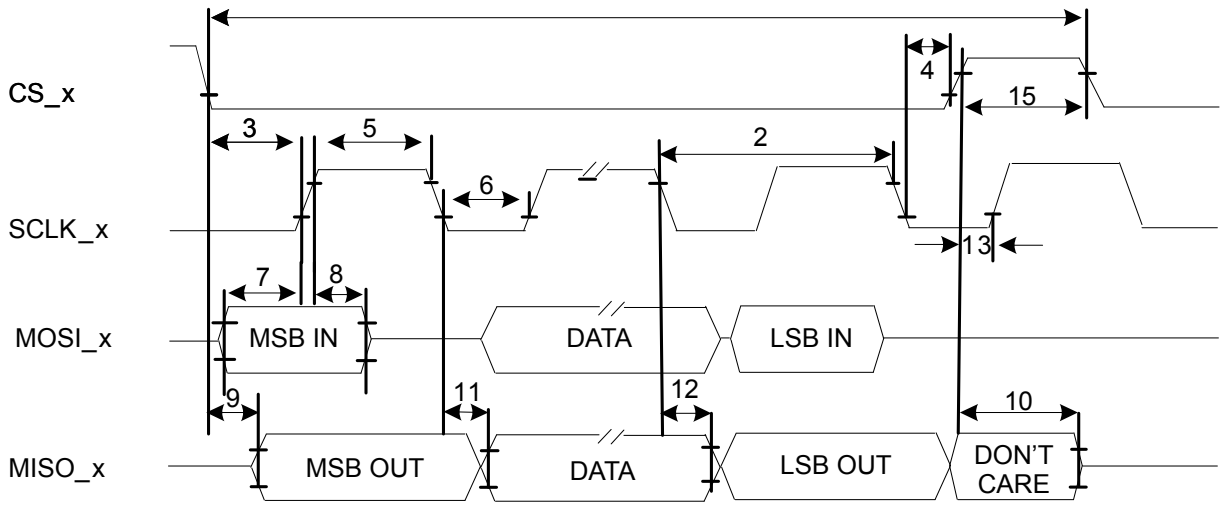
Table 585. SPI electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
f_{SCLK}	SPI transfer frequency	-	-	-	13.5	MHz	-
t_{SCLK}	SCLK_x period (2[1])	-	74	-	-	ns	-
t_{LEAD}	Enable lead time (3[1])	-	150	-	-	ns	-
t_{LAG}	Enable lag time (4[1])	-	50	-	-	ns	-
t_{HIGH_SCLK}	SCLK_x high time (5[1])	-	22	-	-	ns	-
t_{LOW_SCLK}	SCLK_x low time (6[1])	-	25	-	-	ns	-
t_{SETUP_MOSI}	MOSI_x input setup time (7[1])	-	12.5	-	-	ns	-
t_{HOLD_MOSI}	MOSI_x input hold time (8[1])	-	12.5	-	-	ns	-
t_{ACC_MISO}	MISO_x access time (9[1])	100pF load	-	-	50	ns	-
t_{DIS_MISO}	MISO_x disable time (10[1])	100pF load	-	-	50	ns	-
$t_{VALID\_MISO\_FAST}$	MISO_x output valid time (11[1])	DIG_IO_SPEED=1, 20% to 80% of VCCBCK 100pF load	-	-	25	ns	-
$t_{VALID\_MISO\_SLOW}$	MISO_x output valid time (11[1])	DIG_IO_SPEED=0, 20% to 80% of VCCBCK 100pF load	-	-	30	ns	-
t_{HOLD_MISO}	MISO_x output hold time (12[1])	100pF load design info	0	-	-	ns	-
t_{HOLD_SCLK}	SCLK_x hold time (13[1])	-	20	-	-	ns	-
t_{NODATA}	SPI interframe time (15[1])	-	600	-	-	ns	-
t_{SETUP_MISO}	MISO_RS input setup time (7[1])	-	12.5	-	-	ns	-
t_{HOLD_MISO}	MISO_RS input hold time (8[1])	-	12.5	-	-	ns	-

1. *Refer to Figure 95*

Note: All timing is shown with respect to 10% and 90% of the actual delivered VCC voltage except for $t_{VALID\_MISO\_*}$ as reported in dedicated test condition.

Figure 95. SPI timing diagram



17.3 Power supply and energy reserve management

17.3.1 SYS boost regulator

-40 °C < T_J < 175 °C, ACTIVE mode, V_{VIN}<$V_{VIN\_SYSBST\_DIS}$, unless otherwise noted.

Table 586. SYS boost regulator electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
V_{O_SYSBST}	SYS boost output voltage, linear operation	VIN inside $V_{VIN\_SYSBST\_LINEAR}$ range, output current inside I_{O_SYSBST} range	9.2	10	10.8	V	SYSBST
$V_{VIN\_SYSBST\_LINEAR}$	VIN value range for SYS boost linear operation	-	5.1	6.5	8.3	V	VIN
I_{O_SYSBST}	SYS boost output current, linear operation	5.1 V < V_{VIN} < 8.3 V	470	500	870	mA	SYSBST
$I_{O\_SYSBST\_VIN\_BAD}$	SYS boost output current, linear operation, VIN extended down to V_{VIN_BAD}	4.0 V < V_{VIN} < 5.1 V	470	-	600	mA	SYSBST
$V_{VIN\_SYSBST\_DIS}$	VIN threshold for SYS boost disabling	-	10.6	11	11.4	V	VIN
$V_{VIN\_SYSBST\_DIS\_HYST}$	VIN threshold hysteresis, disabling SYS boost	-	440	480	520	mV	VIN
$V_{SYSBST\_CHG\_DIS}$	SYS boost disable threshold during SYSBST initial charge phase (V_{VIN} - V_{SYSBST})	-	1.6	2.2	2.5	V	VIN, SYSBST
dV_{SR_SYSBST}	Supply line transient response	VIN step 5.1 V → 8.3 V → 5.1 V in 20 µs, measured at SYSBST pin	-8	-	8	%	SYSBST
dV_{LR_SYSBST}	Load transient response	Current step 47 0 mA → 870 mA → 470 mA in 40 µs measured at SYSBST pin	-8	-	8	%	SYSBST
$I_{OC\_SYSBSTSW}$	SYS boost LS overcurrent threshold	-	2.6	3.2	4.3	A	SYSBSTSW
V_{OV_SYSBST}	SYSBST overvoltage threshold	-	17.45	18	18.55	V	SYSBST
$V_{OV\_SYSBST\_HYST}$	SYSBST overvoltage threshold hysteresis	-	0.8	0.95	1.1	V	SYSBST
V_{UV_SYSBST}	SYSBST undervoltage threshold	-	8.4	-	9.1	V	SYSBST
R_{DSON_SYSBST}	Power switch resistance (SYSBSTSW to BSTGND)	-	-	-	0.35	Ω	SYSBSTSW, BSTGND
$V_{BSTGND\_LOSS\_TH}$	BSTGND ground loss detection threshold	$V_{SUBGNDx}$ = 0 V	100	200	300	mV	BSTGND
I_{PU_BSTGND}	BSTGND pullup current	-	130	-	270	µA	BSTGND
$V_{D\_LOSS\_TH\_SYSBST}$	SYS boost diode loss detection threshold ($V_{SYSBSTSW}$ - V_{SYSBST})	-	2.6	3.3	3.7	V	SYSBSTSW, SYSBST

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
$V_{CLAMP\_SYSBSTSW}$	SYSBSTSW pin clamping voltage	-	31	32.5	34	V	SYSBSTSW
T_{OT_SYSBST}	Overtemperature shut down threshold	-	185	-	215	deg	SYSBST
$T_{OT\_SYSBST\_HYST}$	Overtemperature shut down threshold hysteresis	-	15	-	25	deg	SYSBST
$f_{SW\_SYSBST\_1}$	Switching frequency 1	Oscillator accuracy after trimming(1) design info	1.9	2	2.1	MHz	SYSBSTSW
$f_{SW\_SYSBST\_2}$	Switching frequency 2	Oscillator accuracy after trimming(1) Design info	2.0235	2.130	2.2365	MHz	SYSBSTSW
$DC_{SYSBST\_MIN\_1}$	Minimum duty cycle 1	Min T_{ON} at $f_{SW\_SYSBST\_1}$ Design info	-	14	-	%	SYSBSTSW
$DC_{SYSBST\_MIN\_2}$	Minimum duty cycle 2	Min T_{ON} at $f_{SW\_SYSBST\_2}$ Design info	-	15	-	%	SYSBSTSW
$t_{SYSBSTSW\_RISE}$	SYSBSTSW rise time 10% - 90%	ILOAD = 600 mA	5	10	15	ns	SYSBSTSW
$t_{SYSBSTSW\_FALL}$	SYSBSTSW fall time 90% - 10%	ILOAD = 600 mA	5	10	15	ns	SYSBSTSW
t_{SOFTST_SYSBST}	SYS boost soft start time	(1)	850	960	1010	µs	SYSBST
$t_{OV\_SYSBST\_FLT}$	SYSBST overvoltage filter time	(1)	8	10	12	µs	SYSBST
$t_{OV\_SYSBST\_BLK}$	SYSBST overvoltage blanking time	(1)	80	100	130	µs	SYSBST
$t_{UV\_SYSBST\_FLT}$	SYSBST undervoltage filter time	(1)	8	10	12	µs	SYSBST
$t_{BSTGND\_LOSS\_FLT}$	BSTGND ground loss detection filter time	(1)	1.9	2.3	2.7	µs	BSTGND
$t_{OT\_SYSBST\_FLT}$	Overtemperature shut down filter time	(1)	7	8.5	10	µs	SYSBST
$t_{VIN\_OV\_FLT}$	VIN overvoltage filter time	(1)	13	19	25	µs	VIN
$t_{VIN\_FAST\_SLOPE\_FLT}$	Deglitch filter applied on $V_{VIN\_FASTSLOPE}$	(1)	3	5	7	µs	VIN
$t_{VIN\_SYSBST\_DIS\_FLT}$	Deglitch filter applied on $V_{VIN\_SYSBST\_DIS}$	(1)	8	10	12	µs	VIN, SYSBST
$t_{VIN\_VER\_FLT}$	Deglitch filter applied on $V_{VIN\_VER\_DIFF\_TH}$	(1)	26	30	33	µs	VIN, VER
$t_{READY\_SYSBST\_FLT}$	-	(1)	10	20	25	µs	SYSBST

1. *Guaranteed only in case CLKIN is provided with 1% accuracy and FLL is enabled.*

17.3.2 ER boost regulator

-40 °C < T_J < 175 °C, ACTIVE mode or PASSIVE mode + ER state, V_{UV_SYSBST} < V_{SYSBST} < 35 V, unless otherwise noted.

Table 587. ER boost regulator electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
$V_{O\_ERBST\_H}$	ER boost output voltage, high voltage configuration, linear operation	SYSBST inside $V_{SYSBST\_ERBST\_LINEAR}$ range, output current inside I_{O_ERBST} range	31	33	35	V	ERBST
$V_{O\_ERBST\_L}$	ER boost output voltage, low voltage configuration, linear operation	SYSBST inside $V_{SYSBST\_ERBST\_LINEAR}$ range, output current inside I_{O_ERBST} range	22.5	23.8	25	V	ERBST
$V_{SYSBST\_ERBST\_LINEAR}$	SYSBST value range for ER boost linear operation	-	10	13	16	V	SYSBST
I_{O_ERBST}	ER boost output current, linear operation	-	16	-	20	mA	ERBST
$V_{ERBST\_CHG\_DIS}$	ER boost disable threshold during ERBST initial charge phase (V_{SYSBST} - V_{ERBST})	-	1.6	2.2	2.5	V	SYSBST, ERBST
dV_{SR_ERBST}	Supply line transient response	SYSBST step 10 V → 15 V → 10 V in 20 µs, measured at ERBST pin	-8	-	8	%	ERBST
dV_{LR_ERBST}	Load transient response	Current step 10 mA → 20 mA → 10 mA in 20 µs, measured at ERBST pin	-8	-	8	%	ERBST
$I_{OC\_ERBSTSW}$	ER boost LS overcurrent threshold	V_{SYSBST} = V_{ERBST}	150	210	270	mA	ERBSTSW
$V_{OV\_ERBST\_H}$	ERBST overvoltage threshold, high voltage configuration	-	35	-	39	V	ERBST
$V_{OV\_ERBST\_L}$	ERBST overvoltage threshold, low voltage configuration	-	25.5	-	29.5	V	ERBST
$V_{UV\_ERBST\_H}$	ERBST undervoltage threshold, high voltage configuration	-	26	28	30	V	ERBST
$V_{UV\_ERBST\_L}$	ERBST undervoltage threshold, low voltage configuration	-	18	20	22	V	ERBST

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
R_{DSON_ERBST}	Power switch resistance (ERBSTSW to BSTGND)	-	-	-	1	Ω	ERBSTSW, BSTGND
$V_{D\_LOSS\_TH\_ERBST}$	ER boost diode loss detection threshold ($V_{ERBSTSW}$ - V_{ERBST})	-	2.7	3.3	3.7	V	ERBSTSW, ERBST
$V_{CLAMP\_ERBSTSW}$	ERBSTSW pin clamping voltage	-	35	-	40	V	ERBSTSW
T_{OT_ERBST}	Overtemperature shutdown threshold	-	185	-	215	deg	ERBST
$T_{OT\_ERBST\_HYST}$	Overtemperature shutdown threshold hysteresis	-	15	-	25	deg	ERBST
$f_{SW\_ERBST\_1}$	Switching frequency 1	Oscillator accuracy after trimming(1) Design info	1.9	2	2.1	MHz	ERBSTSW
$f_{SW\_ERBST\_2}$	Switching frequency 2	Oscillator accuracy after trimming(1) Design info	2.0235	2.130	2.2365	MHz	ERBSTSW
$DC_{ERBST\_MIN\_1}$	Minimum Duty cycle 1	Min T_{ON} at $f_{SW\_ERBST\_1}$ Design info	-	14	-	%	ERBSTSW
$DC_{ERBST\_MIN\_2}$	Minimum Duty cycle 2	Min T_{ON} at $f_{SW\_ERBST\_2}$ Design info	-	15	-	%	ERBSTSW
$V_{VIN\_FASTSLOPE\_H}$	V_{VIN} threshold used to change ERBSTSW rise/ fall times (fast to slow)	-	9.3	9.8	10.3	V	VIN
$V_{VIN\_FASTSLOPE\_L}$	V_{VIN} threshold used to change ERBSTSW rise/ fall times (slow to fast)	-	9	9.5	10	V	VIN
$V_{VIN\_FASTSLOPE\_HYS}$	V_{VIN} threshold used to change ERBSTSW rise/ fall times, hysteresis	-	0.2	0.3	0.4	V	VIN
$t_{ERBSTSW\_RISE\_SLOW}$	ERBSTSW rise time 10% - 90%, slow mode	-	15	25	35	ns	ERBSTSW
$t_{ERBSTSW\_FALL\_SLOW}$	ERBSTSW fall time 90% - 10%, slow mode	-	15	25	35	ns	ERBSTSW
$t_{ERBSTSW\_RISE\_FAST}$	ERBSTSW rise time 10% - 90%, fast mode	-	5	10	15	ns	ERBSTSW
$t_{ERBSTSW\_FALL\_FAST}$	ERBSTSW fall time 90% - 10%, fast mode	-	5	10	15	ns	ERBSTSW

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
t_{SOFTST_ERBST}	ER boost soft start time	(1)	850	960	1010	µs	ERBST
$t_{OV\_ERBST\_FLT}$	ERBST overvoltage filter time	(1)	8	10	12	µs	ERBST
$t_{OV\_ERBST\_BLK}$	ERBST overvoltage blanking time	(1)	80	100	130	µs	ERBST
$t_{UV\_ERBST\_FLT}$	ERBST undervoltage filter time	(1)	8	10	12	µs	ERBST
$t_{OT\_ERBST\_FLT}$	Overtemperature shutdown filter time	(1)	7	8.5	10	µs	ERBST
$t_{READY\_ERBST\_FLT}$	-	(1)	10	20	25	µs	ERBST
$t_{PLS\_SKIP\_ERBST\_FLT}$	ERBST pulse skip filter time	(1)	0.8	1	1.2	µs	ERBST
$t_{SKP\_ERBST\_BLK1}$	ERBST pulse skip blanking time	NVM_ERBOOST_PLS_SKIP_BLK_SEL = 0	80	100	130	µs	ERBST
$t_{SKP\_ERBST\_BLK2}$	ERBST pulse skip blanking time	NVM_ERBOOST_PLS_SKIP_BLK_SEL = 1	40	50	65	µs	ERBST

1. *Guaranteed only in case CLKIN is provided with 1% accuracy and FLL is enabled.*

17.3.3 ER charge and discharge circuits

-40 °C < T_J < 175 °C, for ER charge: ACTIVE mode or PASSIVE mode + ER state; for ER discharge: ACTIVE or PASSIVE mode; V_{VER} < 35 V, unless otherwise noted.

Table 588. ER charge and discharge electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
R_{DSON_ERCHSW}	ER charge switch ON resistance	I_{ERCHSW} = -200 mA	-	2	3	Ω	ERBST, ERCHSW
$R_{DSON\_ERDCHSW}$	ER discharge switch ON resistance	$I_{ERDCHSW}$ = 1 A	-	1	2	Ω	ERDCHSW, AGND
I_{LIM_ERCHSW}	ER charge switch limitation current	-	250	330	420	mA	ERCHSW
$V_{LIM\_ERDCHSW}$	ER discharge switch V_{DS} monitor threshold	-	3.4	-	3.8	V	ERDCHSW
T_{OT_ERCHSW}	ER charge switch overtemperature shutdown threshold	-	185	-	215	deg	ERCHSW
$T_{OT\_ERCHSW\_HYST}$	ER charge switch overtemperature shutdown threshold hysteresis	-	15	-	25	deg	ERCHSW
$t_{OT\_ERCHSW\_FLT}$	ER charge switch overtemperature shutdown filter time	(1)	7	8.5	10	µs	ERCHSW
$t_{ERDCHSW\_FLT}$	ER discharge switch filter time	(1)	8	10	12	µs	ERDCHSW

1. *Guaranteed only in case CLKIN is provided with 1% accuracy and FLL is enabled.*

17.3.4 ER switch

-40 °C < T_J < 175 °C, ACTIVE or PASSIVE mode, V_{VER} < 35 V, unless otherwise noted.

Table 589. ER switch electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
R_{DSON_ERSW}	ER switch ON resistance	I_{ERSW} = -500 mA	-	-	1.5	Ω	VER, ERSW
I_{LIM_ERSW}	ER switch limitation current	-	870	1200	1500	mA	ERSW
$V_{VIN\_VER\_DIFF\_TH}$	V_{VIN} - V_{VER} difference detection threshold, disabling ER switch	-	10	-	200	mV	VIN, VER
T_{OT_ERSW}	Overtemperature shutdown threshold	-	185	-	215	deg	ERSW
$T_{OT\_ERSW\_HYST}$	Overtemperature shutdown threshold hysteresis	-	15	-	25	deg	ERSW
t_{ON_ERSW}	ER switch ON time	From off state to 800 mA	-	-	5	µs	ERSW
$t_{OT\_ERSW\_FLT}$	Overtemperature shutdown filter time	(1)	7	8.5	10	µs	ERSW
$t_{OT\_ERSW\_BLK}$	Overtemperature shutdown blanking time	(1)	0.7	1	1.2	ms	ERSW

1. *Guaranteed only in case CLKIN is provided with 1% accuracy and FLL is enabled.*

17.3.5 Energy Reserve Capacitor (ER Cap) diagnostics

-40 °C < T_J < 175 °C, ACTIVE mode, 20 V < V_{VER} < 35 V, unless otherwise noted.

Table 590. ER Cap diagnostics electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
$V_{DISCHARGE}$	V_{VER} - $V_{ERDCHSW}$ input differential measurement range	-	20	-	35	V	VER ERDCHSW
$V_{DISCHARGE\_RES}$	V_{VER} - $V_{ERDCHSW}$ input differential measurement LSB	-	-	140.62	-	mV	VER ERDCHSW
$V_{DISCHARGE\_ACC}$	V_{VER} - $V_{ERDCHSW}$ Voltage Measurement Accuracy	20 V < V_{VER} – $V_{ERDCHSW}$ < 35 V	-5		5	%	VER ERDCHSW
$V_{DISCHARGE\_INTG\_RES}$	Integral of V_{VER} - $V_{ERDCHSW}$ internal number of bits	Design info	-	18	-	bit	VER ERDCHSW
ΔV_{VER}	V_{VER} input discharge voltage range (during ER cap measurement)	Design info	0	-	1.2	V	VER
ΔV_{VER_RES}	V_{VER} input discharge voltage LSB (during ER cap measurement)	-	-	5.545	-	mV	VER
ΔV_{VER_ACC}	V_{VER} input discharge voltage measurement accuracy	Use dedicated A/D to convert directly differential voltage	-70		+70	mV	VER
ΔV_{VER_CAP}	V_{VER} input discharge voltage due to cap discharge		0.4		0.7	V	VER
ΔV_{VER_ESR}	V_{VER} input discharge voltage due to ESR	Design info	0.1		0.6	V	VER
I_{LEAK_VER}	Leakage on VER without diagnostic running	-	-	-	1.4	mA	VER
$I_{LEAK\_VER\_DIAG}$	Additional current from VER pin for ER CAP diagnostic	-	-	-	1.2	mA	VER

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
$t_{ER\_CAP\_DIAG1}$	ER_CAP_DIAG total running time	Design info(1) With 2.2 mF V_{VER} =33 V $R_{ERDCHSW}$ = 33 Ω	-	1.7	-	ms	-
$t_{ER\_CAP\_DIAG2}$	ER_CAP_DIAG total running time	Design info(1) With 52 mF V_{VER} =33 V $R_{ERDCHSW}$ = 33 Ω	-	27	-	ms	-
LSB_{ESR}	$ESR/R_{ERDCHSW}$	Design info	-	38.5	-	µ	-
LSB_C	$R_{ERDCHSW}$*C_{ER}	Design info(1)	-	405	-	µF*Ω	-
$t_{S\_ER\_CAP}$	Sample time of each conversion on voltage ADCs	Design info(1)	-	64	-	µs	-
t_{LOCK_VER}	Time needed for t_{START} conversion	Design info(1)	-	464	-	µs	-

1. *Guaranteed only in case CLKIN is provided with 1% accuracy and FLL is enabled.*

17.3.6 SAT buck regulator

-40 °C < T_J < 175 °C, ACTIVE or PASSIVE mode, V_{UV_SYSBST} < V_{SYSBST} < 35 V, unless otherwise noted.

Table 591. SAT buck regulator electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
$V_{O\_SATBCK\_H}$	SAT buck output voltage, high voltage configuration	-	7.68	8	8.32	V	SATBCK
$V_{O\_SATBCK\_L}$	SAT buck output voltage, low voltage configuration	-	6.24	6.5	6.76	V	SATBCK
I_{O_SATBCK}	SAT buck output current	-	-	500	700	mA	SATBCK
dV_{SR_SATBCK}	Supply line transient response	SYSBST step 10 V → 33 V → 10 V in 60 µs, measured at SATBCK pin	-4	-	4	%	SATBCK
dV_{LR_SATBCK}	Load transient response	Current step 100 mA → 500 mA → 100 mA in 20 µs, measured at SATBCK pin	-4	-	4	%	SATBCK
$I_{OC\_HS\_SATBCKSW}$	SATBCKSW HS overcurrent threshold	-	-1.95	-1.55	-1.15	A	SATBCKSW
$I_{OC\_LS\_SRC\_SATBCKSW}$	SATBCKSW LS sourcing overcurrent threshold	-	-2.3	-1.85	-1.35	A	SATBCKSW
$I_{OC\_LS\_SNK\_SATBCKSW}$	SATBCKSW LS sinking overcurrent threshold	-	100	200	350	mA	SATBCKSW
$R_{DSON\_SATBCK\_HS}$	HS power switch resistance (SYSBST to SATBCKSW)	-	-	-	0.55	Ω	SYSBST, SATBCKSW
$R_{DSON\_SATBCK\_LS}$	LS power switch resistance (SATBCKSW to SATBCKGND)	-	-	-	0.45	Ω	SATBCKSW, SATBCKGND

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
$V_{UV\_SATBCK\_H}$	SATBCK undervoltage threshold, high voltage configuration	-	6.5	7	7.5	V	SATBCK
$V_{UV\_SATBCK\_L}$	SATBCK undervoltage threshold, low voltage configuration	-	5.45	5.8	6.15	V	SATBCK
$V_{SATBCKGND\_LOSS\_TH}$	SATBCKGND ground loss detection threshold	$V_{SUBGNDx}$ = 0 V	100	200	300	mV	SATBCKGND
$I_{PU\_SATBCKGND}$	SATBCKGND pullup current	-	130	-	270	µA	SATBCKGND
$f_{SW\_SATBCK\_1}$	Switching frequency 1	Oscillator accuracy after trimming Design info	1.9	2	2.1	MHz	SATBCKSW
$f_{SW\_SATBCK\_2}$	Switching frequency 2	Oscillator accuracy after trimming Design info	2.0235	2.130	2.2365	MHz	SATBCKSW
$DC_{SATBCK\_MIN\_1}$	Minimum duty cycle 1	Min T_{ON} at $f_{SW\_SATBCK\_1}$ Design info	-	14	-	%	SATBCKSW
$DC_{SATBCK\_MIN\_2}$	Minimum duty cycle 2	Min T_{ON} at $f_{SW\_SATBCK\_2}$ Design info	-	15	-	%	SATBCKSW
$V_{SYSBST\_FASTSLOPE\_H}$	V_{SYSBST} threshold used to change SATBCKSW rise/fall times (slow to fast)	-	17.45	18	18.55	V	SYSBST
$V_{SYSBST\_FASTSLOPE\_L}$	V_{SYSBST} threshold used to change SATBCKSW rise/fall times (fast to slow)	-	16.45	17	17.55	V	SYSBST
$V_{SYSBST\_FASTSLOPE\_HYS}$	V_{SYSBST} threshold used to change SATBCKSW rise/fall times, hysteresis	-	0.8	0.95	1.1	V	SYSBST
$t_{SATBCKSW\_RISE\_SLOW}$	SATBCKSW rise time 10% - 90%, slow mode	Design info	5	13	20	ns	SATBCKSW
$t_{SATBCKSW\_FALL\_SLOW}$	SATBCKSW fall time 90% - 10%, slow mode	Design info	5	13	20	ns	SATBCKSW
$t_{SATBCKSW\_RISE\_FAST}$	SATBCKSW rise time 10% - 90%, fast mode	Design info	3	7	15	ns	SATBCKSW
$t_{SATBCKSW\_FALL\_FAST}$	SATBCKSW fall time 90% - 10%, fast mode	Design info	3	7	15	ns	SATBCKSW
t_{SOFTST_SATBCK}	SAT buck soft start time	(1)	-	180	-	µs	SATBCK
$t_{UV\_SATBCK\_FLT}$	SATBCK undervoltage filter time	(1)	8	10	12	µs	SATBCK
$t_{SATBCKGND\_LOSS\_FLT}$	SATBCKGND ground loss detection filter time	(1)	1.9	2.3	2.7	µs	SATBCKGND
T_{OT_SATBCK}	Overtemperature shut down threshold	-	185	-	215	deg	SATBCK
$T_{OT\_SATBCK\_HYST}$	Overtemperature shut down threshold hysteresis	-	15	-	25	deg	SATBCK
$t_{OT\_SATBCK\_FLT}$	Overtemperature shut down filter time	(1)	-	-	10	µs	SATBCK

1. *Guaranteed only in case CLKIN is provided with 1% accuracy and FLL is enabled.*

17.3.7 VCC buck regulator

-40 °C < T_J < 175 °C, ACTIVE or PASSIVE mode, V_{SATBCK} > $V_{UV\_SATBCK\_L}$/$V_{UV\_SATBCK\_H}$, unless otherwise noted.

Table 592. VCC buck regulator electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
V_{O_VCCBCK}	VCC buck output voltage	-	3.2	3.3	3.4	V	VCCBCK
I_{O_VCCBCK}	VCC buck output current	-	-	300	450	mA	VCCBCK
dV_{SR_VCCBCK}	Supply line transient response	SATBCK step 6.5 V → 8.5 V → 6.5 V in 10 µs, measured at VCCBCK pin	-4	-	4	%	VCCBCK
dV_{LR_VCCBCK}	Load transient response	Current step 10 mA → 300 mA → 10 mA in 20 µs, measured at VCCBCK pin	-4	-	4	%	VCCBCK
$I_{OC\_HS\_VCCBCKSW}$	VCCBCKSW HS overcurrent threshold	-	-1.1	-0.8	-0.7	A	VCCBCKSW
$I_{OC\_LS\_SRC\_VCCBCKSW}$	VCCBCKSW LS sourcing overcurrent threshold	-	-1.25	-1	-0.75	A	VCCBCKSW
$I_{OC\_LS\_SNK\_VCCBCKSW}$	VCCBCKSW LS sinking overcurrent threshold	-	100	200	350	mA	VCCBCKSW
$I_{PU\_OF\_VCCBCK}$	VCCBCK open feedback diagnostic pullup current	-	-200	-150	-100	µA	VCCBCK
$R_{DSON\_VCCBCK\_HS}$	HS power switch resistance (SATBCK to VCCBCKSW)	-	-	-	0.7	Ω	SATBCK, VCCBCKSW
$R_{DSON\_VCCBCK\_LS}$	LS power switch resistance (VCCBCKSW to VCCBCKGND)	-	-	-	0.58	Ω	VCCBCKSW, VCCBCKGND
$V_{UV\_H\_VCCBCK}$	VCCBCK undervoltage high threshold	-	3.0	-	3.18	V	VCCBCK
$V_{UV\_L\_VCCBCK}$	VCCBCK undervoltage low threshold	-	1.8	2	2.2	V	VCCBCK
V_{OV_VCCBCK}	VCCBCK overvoltage threshold	-	3.43	-	3.6	V	VCCBCK
$V_{VCCBCKGND\_LOSS\_TH}$	VCCBCKGND ground loss detection threshold	$V_{SUBGNDx}$ = 0 V	100	200	300	mV	VCCBCKGND
$I_{PU\_VCCBCKGND}$	VCCBCKGND pullup current	-	130	-	270	µA	VCCBCKGND
$f_{SW\_VCCBCK\_1}$	Switching frequency 1	Oscillator accuracy after trimming(1) Design info	1.9	2	2.1	MHz	VCCBCKSW
$f_{SW\_VCCBCK\_2}$	Switching frequency 2	Oscillator accuracy after trimming(1) Design info	2.0235	2.130	2.2365	MHz	VCCBCKSW
$DC_{SATBCK\_MIN\_1}$	Minimum Duty cycle 1	Min T_{ON} at $f_{SW\_VCCBCK\_1}$ Design info	-	14	-	%	VCCBCKSW

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
$DC_{SATBCK\_MIN\_2}$	Minimum Duty cycle 2	Min T_{ON} at $f_{SW\_VCCBCK\_2}$ Design info	-	15	-	%	VCCBCKSW
$t_{VCCBCKSW\_RISE\_SLOW}$	VCCBCKSW rise time 10% - 90%, slow mode	I_{O_VCCBCK} > 200 mA	10	20	30	ns	VCCBCKSW
$t_{VCCBCKSW\_FALL\_SLOW}$	VCCBCKSW fall time 90% - 10%, slow mode	-	4	10	20	ns	VCCBCKSW
$t_{VCCBCKSW\_RISE\_FAST}$	VCCBCKSW rise time 10% - 90%, fast mode	I_{O_VCCBCK} > 200 mA	2	8	15	ns	VCCBCKSW
$t_{VCCBCKSW\_FALL\_FAST}$	VCCBCKSW fall time 90% - 10%, fast mode	-	4	10	15	ns	VCCBCKSW
t_{SOFTST_VCCBCK}	VCC buck soft start time	(1)	-	180	-	µs	VCCBCK
t_{RU_VCCBCK}	VCC buck ramp-up phase duration	(1)	380	450	480	µs	VCCBCK
$t_{DIS\_VCCBCK\_BLK}$	VCC buck failure disable blanking time	(1)	4.3	5	5.5	ms	VCCBCK
$t_{UV\_VCCBCK\_FLT}$	VCCBCK undervoltage filter time	(1)	27	30	33	µs	VCCBCK
$t_{OV\_VCCBCK\_RU\_FLT}$	VCCBCK overvoltage filter time, used during ramp-up phase	(1)	1.5	2	2.5	µs	VCCBCK
$t_{OV\_VCCBCK\_FLT}$	VCCBCK overvoltage filter time, used during normal operation	(1)	27	30	33	µs	VCCBCK
$t_{VCCBCKGND\_LOSS\_FLT}$	VCCBCKGND ground loss detection filter time	(1)	1.9	2.3	2.7	µs	VCCBCKGND
$DC_{FDM\_VCCBCKSW}$	FDM VCCBCKSW duty-cycle	-	40	50	60	%	VCCBCKSW
T_{OT_VCCBCK}	Overtemperature shutdown threshold	-	185	-	215	deg	VCCBCK
$T_{OT\_VCCBCK\_HYST}$	Overtemperature shutdown threshold hysteresis	-	15	-	25	deg	VCCBCK
$t_{OT\_VCCBCK\_FLT}$	Overtemperature shutdown filter time	(1)	7	8.5	10	µs	VCCBCK

1. *Guaranteed only in case CLKIN is provided with 1% accuracy and FLL is enabled.*

17.3.8 Microcontroller core voltage monitor (VCOREMON)

-40 °C < T_J < 175 °C, ACTIVE or PASSIVE mode, V_{SATBCK} > $V_{UV\_SATBCK\_L}$/$V_{UV\_SATBCK\_H}$, unless otherwise noted.

Table 593. VCOREMON electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
$R_{PD\_VCOREMON}$	VCOREMON pin pulldown resistance	-	65	100	135	kΩ	VCOREMON
$V_{OV\_VCOREMON}$	VCOREMON overvoltage threshold	-	1.26	1.29	1.32	V	VCOREMON
$V_{UV\_VCOREMON}$	VCOREMON undervoltage threshold	-	1.08	1.11	1.14	V	VCOREMON
$t_{OV\_VCOREMON\_FLT}$	VCOREMON overvoltage filter time	(1)	27	30	33	µs	VCOREMON
$t_{UV\_VCOREMON\_FLT}$	VCOREMON undervoltage filter time	(1)	27	30	33	µs	VCOREMON

1. *Guaranteed only in case CLKIN is provided with 1% accuracy and FLL is enabled.*

17.3.9 V5 linear regulator

-40 °C < T_J < 175 °C, ACTIVE or PASSIVE mode, V_{SATBCK} > V_{UV_SATBCK}, unless otherwise noted.

Table 594. V5 linear regulator electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
$V_{O\_V5\_SENSE}$	V5_SENSE regulation output voltage	Q_{V5} I_C = 1 mA - 200 mA	4.85	5	5.15	V	V5_SENSE
$I_{LIM\_V5\_DRV}$	V5_DRV sinking limitation current	-	4	-	10	mA	V5_DRV
$dV_{SR\_V5\_SENSE}$	Supply line transient response	Emitter voltage step 6.5 V → 8.5 V → 6.5 V in 10 µs, measured at V5_SENSE	-8	-	8	%	V5_SENSE
$dV_{LR\_V5\_SENSE}$	Load transient response	Q_{V5} I_C current step 1 mA → 135 mA → 1 mA in 10 µs, measured at V5_SENSE	-8	-	8	%	V5_SENSE
$I_{PU\_OF\_V5\_SENSE}$	V5_SENSE open feedback diagnostic pullup current	V_{V5_SENSE} = 0 V	60	-	200	µA	V5_SENSE
$R_{PU\_V5\_DRV}$	V5_DRV internal pullup resistance (to SATBCK)	-	10	15	20	kΩ	V5_DRV SATBCK
$V_{UV\_V5\_SENSE\_H}$	V5_SENSE undervoltage high threshold	-	4.55	-	4.8	V	V5_SENSE
$V_{UV\_V5\_SENSE\_L}$	V5_SENSE undervoltage low threshold	-	4.45	-	4.7	V	V5_SENSE
$V_{UV\_V5\_SENSE\_HYST}$	V5_SENSE undervoltage threshold hysteresis	-	80	100	120	mV	V5_SENSE
$V_{OV\_V5\_SENSE\_H}$	V5_SENSE overvoltage high threshold	-	5.28	-	5.58	V	V5_SENSE
$V_{OV\_V5\_SENSE\_L}$	V5_SENSE overvoltage low threshold	-	5.2	-	5.48	V	V5_SENSE
$V_{OV\_V5\_SENSE\_HYST}$	V5_SENSE overvoltage threshold hysteresis	-	90	110	130	mV	V5_SENSE
$V_{STG\_V5\_SENSE}$	V5_SENSE short to ground threshold	-	1	-	1.4	V	V5_SENSE
$t_{SOFTST\_V5\_SENSE}$	V5_SENSE voltage soft start time	(1)	85	100	115	µs	V5_SENSE
$t_{UV\_V5\_SENSE\_FLT}$	V5_SENSE undervoltage filter time	(1)	27	30	33	µs	V5_SENSE
$t_{OV\_V5\_SENSE\_FLT}$	V5_SENSE overvoltage filter time	(1)	90	100	110	µs	V5_SENSE
$t_{STG\_V5\_SENSE\_FLT}$	V5_SENSE short to ground filter time	(1)	9	10	11	µs	V5_SENSE
$t_{BLK\_STG\_V5\_SENSE}$	Blanking time on STG fault during powerup	(1)	60	70	80	µs	V5_SENSE

1. *Guaranteed only in case CLKIN is provided with 1% accuracy and FLL is enabled.*

17.4 Safing FET regulator and diagnostics

40 °C < T_J < 175 °C, ACTIVE or PASSIVE mode, ERBST > VSF_G + $V_{DO\_VSF\_G}$, unless otherwise noted.

Table 595. Safing FET and ER management electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
$V_{REG\_VSF\_S}$	Regulated output voltage on VSFx_S, transient	Regulator on, 16 synchronous high current deployment events, I_{LOAD_MIN} = 2.7 mA	17.7	18.63	19.56	V	VSFx_S
I_{VSF_G}	VSFx_G load current	-	-1.5	-	0	mA	VSFx_G
$I_{LIM\_VSF\_G}$	Gate driver sourcing output current limit on VSFx_G	Regulator on	-4	-	-2	mA	VSFx_G
I_{VSF_S}	VSFx_S current	Regulator on	-1.12	-0.5	-	mA	VSFx_S
$V_{DO\_VSF\_G}$	V(ERBST-VSFx_G) drop-out voltage	-	1.6	-	-	V	ERBST, VSFx_G
$V_{VSF\_G\_CLAMP}$	VSFx_G clamping voltage	-	25	27.8	30.6	V	VSFx_G
$V_{VGS\_SF\_CLAMP}$	V(VSFx_G-VSFx_S) clamping voltage	-	9.3	10	10.7	V	VSFx_G, VSFx_S
$I_{LKG\_VSF\_G\_OFF}$	VSFx_G input leakage	Device off	-5	-	5	µA	VSFx_G
$I_{LKG\_VSF\_S\_OFF}$	VSFx_S input leakage	Device off	-5	-	5	µA	VSFx_S
$I_{PD\_VSF\_G}$	VSFx_G pulldown current	Regulator off	1.5	2	2.5	mA	VSFx_G
$I_{PD\_VSF\_D}$	VSF_D pulldown current	VSF_D_PD_EN = 1	31	41.5	52	mA	VSF_D
I_{PD_SS}	SSx/SSxy pulldown current	SS_PD_EN_x = 1	2.7	3	3.4	mA	SSx, SSxy
$t_{ON\_REG\_VSF\_S}$	Regulator turn on time	-	-	-	100	µs	VSFx_S
R_{ER_BYP}	ER bypass switch resistance	-	-	-	45	Ω	ERBST, VSF_D
$I_{LIM\_ER\_BYP}$	ER bypass switch current limit, source from VSF_D	VSF_D_PD_EN = 0	-90	-	-50	mA	VSF_D
$V_{OV\_SOFF\_V3V3\_DIG}$	Safety overvoltage threshold for V3V3_DIG supply	-	3.6	-	4.6	V	VSFx_G
$V_{OV\_SOFF\_V3V3PRE}$	Safety overvoltage threshold for V3V3PRE supply	-	3.6	-	4.6	V	VSFx_G
$t_{FLT\_SAFETY\_ECHO\_N}$	Safety echo filter time	(1)	-	10	-	µs	-
$R_{VSF\_S\_INT}$	VSFx_S resistance, IC internal	Device on, regulator off (VSF_S < 30 V)	460 k	780 k	1.1 M	Ω	VSFx_S

1. *Guaranteed only in case CLKIN is provided with 1% accuracy and FLL is enabled.*

17.5 Deployment drivers and diagnostics

17.5.1 Deployment drivers

-40 °C < T_J < 175 °C, ACTIVE or PASSIVE mode, 6 V ≤ SSx/SSxy ≤ 35 V, SSx/SSxy - SFx < V_{DEP}, unless otherwise noted.

Table 596. Deployment drivers electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
I_{DEP_L}	Low deployment current value	-	1.33	1.4	1.55	A	SFx, SRx
I_{DEP_H}	High deployment current value	-	1.94	1.99	2.25	A	SFx, SRx
V_{DEP}	Voltage across HS driver during deployment	-	-	-	19.56	V	SSx, SSxy, SFx
$E_{DEP\_SQ\_1.75A/500us}$	Single deployment event energy, standard profile, squib load	V_{DEP} = 19.56 V, I_{DEP_H}, t_{DEP_EFF} = 500 µs	-	-	34.2	mJ	SSx, SSxy, SFx
$E_{DEP\_SQ\_1.75A/700us}$	Single deployment event energy, standard profile, squib load	V_{DEP} = 19.56 V, I_{DEP_H}, t_{DEP_EFF} = 700 µs	-	-	34.2	mJ	SSx, SSxy, SFx
$E_{DEP\_SQ\_1.2A/2ms}$	Single deployment event energy, standard profile, squib load	V_{DEP} = 19.56 V, I_{DEP_L}, t_{DEP_EFF} = 2 ms	-	-	63.7	mJ	SSx, SSxy, SFx
$E_{DEP\_SQ\_AUTOMATIC}$	Single deployment event energy, automatic dynamic profile, squib load	V_{DEP} = 19.56V, I_{DEP_H}, t_{DEP_EFF} = 500 µs (primary profile)	-	-	72.7	mJ	SSx, SSxy, SFx
E_{DEP_LEA}	Single deployment event energy, LEA load	V_{DEP} = 19.56 V, I_{DEP_L}, t_{DEP_EFF} = 3 ms	-	-	94.6	mJ	SSx, SSxy, SFx
N_{DEP_CYC}	Number of deployment cycles that can be withstanded	-	300	-	-	-	SSx, SSxy, SFx
$N_{DEP\_CH\_PARALLEL}$	Number of channels that can be deployed in parallel	-	-	-	16	-	SSx, SSxy, SFx
t_{DEP_CYC}	Successive deployment cycle repetition rate	-	10	-	-	s	SSx, SSxy, SFx
$I_{DEP\_MON\_TH}$	Deployment current monitor threshold	-	90%*I_{DEP_x}	-	-	A	SFx, SRx
V_{CLAMP_SG}	SGxy pin clamping voltage	I_{DEP_H}	-	-	3	V	SGxy
$V_{SG\_LOSS\_TH}$	SGxy ground loss threshold	SUBGNDx as ground reference	300	450	600	mV	SGxy
$I_{OC\_LS\_TH}$	LS driver overcurrent detection threshold	-	2.3	3.1	4.1	A	SRx
I_{LIM_LS}	LS driver current limit	-	2.3	3.1	4.1	A	SRx
$\Delta I_{LIM\_OC\_LS\_TH}$	I_{LIM_LS}-$I_{OC\_LS\_TH}$ value	Design info	0.1	-	-	mA	SRx
$R_{DSON\_LS\_HS}$	Combined LS+HS MOS on resistance	-	-	-	2.5	Ω	SSx, SSxy, SFx, SRx, SGxy

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
E_{UNPOW}	Energy transferred to load in case of unpowered short to battery/ground	R_{LOAD} = 2 Ω, L_{LOAD} = 0 µH, C_{SFx} = C_{SRx} = 22 nF, C_{SSx} = 10 nF	-	-	170	µJ	SSx, SSxy, SFx, SRx
I_{REV_SF}	SFx reverse current without malfunction	DC conditions	-	-	100	mA	SFx
$I_{LKG\_SS\_OFF\_1CH}$	SSx leakage current with device off	SSx ≤ 35 V, SFx = 0 V	-5	-	5	µA	SSx
$I_{LKG\_SS\_OFF}$	SSxy leakage current with device off	SSxy ≤ 35 V, SFx = SFy = 0 V	-10	-	10	µA	SSxy
$I_{LKG\_SS\_ON\_1CH}$	SSx/SSxy leakage current with device on, single channel	SSx ≤ 35 V, SFx = 0 V	70	100	135	µA	SSx, SSxy
$I_{LKG\_SS\_ON}$	SSxy leakage current with device on, dual channel	SSxy ≤ 35 V, SFx = SFy = 0 V	140	200	270	µA	SSxy
$I_{LKG\_SS\_1CH\_EN}$	SSx/SSxy leakage current with single channel enabled	SSx ≤ 35 V, SFx = 0 V	450	620	850	µA	SSx, SSxy
$I_{LKG\_SS\_2CH\_EN}$	SSxy leakage current with dual channel enabled	SSxy ≤ 35 V, SFx = SFy = 0 V	884	1040	1440	µA	SSxy
$I_{LKG\_SF\_OFF\_0V}$	SFx leakage current with device off, SFx = 0V	SSx/SSxy shorted together and open, SYSBST open	-5	-	5	µA	SFx
$I_{LKG\_SF\_OFF\_35V}$	SFx leakage current with device off, SFx = 35V	SSx/SSxy shorted together and open, SYSBST open	-5	-	50	µA	SFx
$I_{LKG\_SF\_ON\_0V}$	SFx leakage current with device on, SFx = 0V	SSx/SSxy = SYSBST = 35 V	-5	-	5	µA	SFx
$I_{LKG\_SF\_ON\_35V}$	SFx leakage current with device on, SFx = 35V	SSx/SSxy = SYSBST = 35 V	-5	-	50	µA	SFx
$I_{LKG\_SR\_OFF\_0V\_20V}$	SRx leakage current with device off, SRx = 0V-20V	SSx/SSxy shorted together and open, SYSBST open	-	-	50	µA	SRx
$I_{LKG\_SR\_OFF\_35V}$	SRx leakage current with device off, SRx = 35V	SSx/SSxy shorted together and open, SYSBST open	-	-	30	mA	SRx
$I_{LKG\_SR\_ON}$	SRx leakage current with device on	SRx pulldown disabled, SRx = 0 V - 35 V, SSx/SSxy = SYSBST = 35 V	-	-	50	µA	SRx
V_{CLAMP_SR}	SRx pin clamping voltage	-	35	-	40	V	SRx
I_{PD_SR}	SRx pulldown current	-	0.7	1	1.3	mA	SRx
I_{PD_SF}	SFx pulldown current	-	0.7	1	1.3	mA	SFx
$V_{SS\_OV\_TH}$	SSx/SSxy overvoltage detection threshold	-	19.66	20.69	21.72	V	SSx, SSxy
t_{DEP_RISE}	Deployment current rise time 10%-90%	R_{LOAD} = 2.2 Ω, L_{LOAD} = 44 µH, C_{SFx} = C_{SRx} = 22 nF,	-	-	32	µs	SFx, SRx

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
		SSx/SSxy = 18 V					
t_{DEP_DEL}	Deployment current delay time, from SPI CS to 90%	R_{LOAD} = 2.2 Ω, L_{LOAD} = 44 µH, C_{SFx} = C_{SRx} = 22 nF, SSx/SSxy = 18 V	-	-	50	µs	SFx, SRx
t_{DEP_FALL}	Deployment current fall time 90%-10%	R_{LOAD} = 2.2 Ω, L_{LOAD} = 44 µH, C_{SFx} = C_{SRx} = 22 nF, SSx/SSxy = 18 V	-	-	32	µs	SFx, SRx
N_{DEP_DWELL}	Deployment dwell time, number of configuration bits	-	-	8	-	bit	SFx, SRx
$t_{RES\_DEP\_DWELL}$	Deployment dwell time, resolution	(1)	15.84	16	16.16	µs	SFx, SRx
$t_{RES\_DEP\_CMT}$	Deployment current monitor timer, resolution	(1)	-	16	-	µs	SFx, SRx
$t_{DEP\_AUTO\_FLT}$	Automatic dynamic deployment profile switching filter time	(1)	16	-	24	µs	SFx, SRx
$t_{DEP\_AUTO\_START}$	Automatic dynamic deployment profile start counter time	(1)	64	72	80	µs	SFx, SRx
$t_{DEP\_AUTO\_SAFE}$	Automatic dynamic deployment profile safe dwell time	(1)	2.1	-	-	ms	SFx, SRx
$t_{FLT\_SG\_LOSS}$	SGxy ground loss detection filter time	(1)	46	50	54	µs	SGxy
$t_{DEL\_OFF\_LS}$	LS turn off delay time vs. HS turn off	(1)	50	-	-	µs	SRx
$t_{DEL\_OFF\_LS\_LEA}$	LS turn off delay time vs. HS turn off with LEA load selected	(1)	7.2	-	-	ms	SRx
$t_{FLT\_OC\_LS}$	LS overcurrent detection filter time	(1)	80	100	120	µs	SRx
$t_{FLT\_SS\_OV\_RISE}$	SSx/SSxy overvoltage detection filter time rise	(1)	80	100	120	µs	SSx, SSxy
$t_{FLT\_SS\_OV\_FALL}$	SSx/SSxy overvoltage detection filter time fall	(1)	1.5	2	2.5	µs	SSx, SSxy

1. *Guaranteed only in case CLKIN is provided with 1% accuracy and FLL is enabled.*

17.5.2 Deployment drivers diagnostics

40 °C < T_J < 175 °C, ACTIVE or PASSIVE mode, V_{SYSBST} > V_{UV_SYSBST}, unless otherwise noted.

Table 597. Deployment drivers diagnostics electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
I_{SRCx_L}	Source current generator output value, low selection	-	7.6	8	8.4	mA	SFx, SRx

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
I_{SRCx_H}	Source current generator output value, high selection	-	38	40	42	mA	SFx, SRx
$I_{SRCx\_DIFF\_H\_L}$	Source current generator output value, high-to-low difference	-	30.4	32	33.6	mA	SFx, SRx
SR_{ISRCx_SLOW}	Source current generator slow slew-rate	-	150	200	250	µA/µs	SFx, SRx
SR_{ISRCx_FAST}	Source current generator fast slew-rate	-	300	400	500	µA/µs	SFx, SRx
I_{SRCx_TEST}	Source current value for integrity check	-	0.85	1	1.15	mA	TEST
$I_{SINK\_SRx\_L}$	SRx sink current generator output value, low selection	-	10	17.5	25	mA	SRx
$I_{SINK\_SRx\_H}$	SRx sink current generator output value, high selection	-	50	75	100	mA	SRx
$I_{SINK\_SFx\_L}$	SFx sink current generator output value, low selection (channels 3, 5, 6, 7 only)	-	10	17.5	25	mA	SFx
$I_{SINK\_SFx\_H}$	SFx sink current generator output value, high selection (channels 3, 5, 6, 7 only)	-	50	75	100	mA	SFx
$I_{LIM\_DEP\_DIAG\_SW}$	Diagnostic supply switch limitation current	-	50	-	90	mA	SYSBST, VSYS
G_{LRM}	Load resistance amplifier voltage gain	-	5.096	5.2	5.304	-	SFx, SRx
$V_{B\_OUT\_LRM}$	Load resistance amplifier base output voltage with null differential input	-	200	300	400	mV	SFx, SRx
$V_{B\_IN\_LRM}$	Load resistance amplifier base voltage at negative input pin during measurement	-	0.4	0.7	1.2	V	SFx, SRx
$V_{B\_IN\_LRM\_CSR}$	Load resistance amplifier base voltage at negative input pin during measurement in common SRx configuration	DEP_MUX_LRM_SEL = 10	0.5	-	1.75	V	SFx, SRx
$ERR_{TOT\_LRM\_LR}$	Load resistance measurement total error, 0-1Ω range	-	-80	-	80	mΩ	SFx, SRx
$ERR_{TOT\_LRM\_MR}$	Load resistance measurement total error, 1-10Ω range	-	-8	-	8	%	SFx, SRx
$ERR_{TOT\_LRM\_HR}$	Load resistance measurement total error, 10-50Ω range	-	-8	-	8	%	SFx, SRx
$V_{O\_VRCM\_L}$	VRCM regulated output voltage, low selection	I_{O_VRCM} = 0 mA	1.35	1.5	1.65	V	SFx, SRx
$V_{O\_VRCM\_H}$	VRCM regulated output voltage, high selection	I_{O_VRCM} = 0 mA	2.25	2.5	2.75	V	SFx, SRx

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
$I_{LIM\_SRC\_VRCM}$	VRCM sourcing limitation current	-	-20	-	-10	mA	SFx, SRx
$I_{LIM\_SINK\_VRCM}$	VRCM sinking limitation current	-	10	-	20	mA	SFx, SRx
$I_{STB\_VRCM\_TH}$	VRCM short to battery detection threshold current	$V_{O\_VRCM\_H}$, V_{SHORT} = 6 to 18 V, R_{LEAK} = 1 - 10 kΩ (leakage detected if R_{LEAK} ≤ 1 kΩ and not detected if R_{LEAK} ≥ 10 kΩ)	1.53	1.8	2.07	mA	SFx, SRx
$I_{STG\_VRCM\_TH}$	VRCM short to ground detection threshold current	$V_{O\_VRCM\_H}$, V_{SHORT} = -1 to 1 V, R_{LEAK} = 1 - 10 kΩ (leakage detected if R_{LEAK} ≤ 1 kΩ and not detected if R_{LEAK} ≥ 10 kΩ)	382.5	450	517.5	µA	SFx, SRx
$I_{R\_LOW\_VRCM\_TH}$	VRCM low resistance detection threshold current	$V_{O\_VRCM\_H}$, R_{LOW} = 200 Ω - 500 Ω	5.1	6	6.9	mA	SFx, SRx
$I_{R\_HIGH\_VRCM\_TH}$	VRCM high resistance detection threshold current	$V_{O\_VRCM\_H}$, R_{HIGH} = 2 kΩ - 5 kΩ	595	700	805	µA	SFx, SRx
$I_{STB\_LS\_FET\_TEST\_TH}$	VRCM short to battery detection threshold current during LS FET test	$V_{O\_VRCM\_H}$, SSx/SSxy ≥ 5 V	1.87	2.2	2.53	mA	SFx, SRx
$I_{STG\_HS\_FET\_TEST\_TH}$	VRCM short to ground detection threshold current during HS FET test	$V_{O\_VRCM\_H}$, SSx/SSxy ≥ 5 V, (SSx – SFx) ≥ 2 V	497	585	673	µA	SFx, SRx
$G_{ADC\_VRCM\_HR}$	VRCM current A/D input scaling factor, high range	I_{O_VRCM} = 0.5 mA - 6.5 mA Design info	-	70	-	-	SFx, SRx
$G_{ADC\_VRCM\_LR}$	VRCM current A/D input scaling factor, low range	I_{O_VRCM} = 0.1 mA - 0.9 mA Design info	-	10	-	-	SFx, SRx
$I_{ADC\_VRCM\_FS}$	VRCM current A/D full scale range, after input scaling	Design info	-	100	-	µA	SFx, SRx
$CONV_{OFFSET}$	VRCM current A/D conversion at zero current	Low range ($V_{O\_VRCM\_H}$) Design info	-	17	-	LSB	SFx, SRx
$CONV_{OFFSET}$	VRCM current A/D conversion at zero current	Low range ($V_{O\_VRCM\_L}$) Design info	-	0	-	LSB	SFx, SRx
$CONV_{OFFSET}$	VRCM current A/D conversion at zero current	High range ($V_{O\_VRCM\_H}$, $V_{O\_VRCM\_L}$) Design info	-	0	-	LSB	SFx, SRx
$CONV_{OFFSET}$	VRCM current A/D conversion error at zero current	High range ($V_{O\_VRCM\_H}$, $V_{O\_VRCM\_L}$); Low range ($V_{O\_VRCM\_H}$, $V_{O\_VRCM\_L}$)	-30	-	30	LSB	SFx, SRx
N_{ADC_VRCM}	VRCM current A/D conversion number of bits	-	-	10	-	bit	SFx, SRx

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
$ERR_{TOT\_ADC\_VRCM}$	VRCM current A/D total conversion error	All contributions included (input scaling factor accuracy, multiplexer channels, references)	-100	-	100	LSB	SFx, SRx
$V_{LEA\_TH\_L}$	LEA presence detection threshold, low selection	Static measurement	0.28	-	1.75	V	SFx, SRx
$V_{LEA\_TH\_H}$	LEA presence detection threshold, high selection	Static measurement	0.56	-	2.5	V	SFx, SRx
E_{FET_TEST}	Energy transferred to load during LS/HS FET test	Design info	-	-	170	µJ	SFx, SRx
f_{LP_LRM}	Load resistance amplifier low-pass filter pole frequency	Design info	50	-	100	kHz	-
$t_{FLT\_STB\_VRCM}$	VRCM short to battery detection filter time	(1)	17	20	23	µs	SFx, SRx
$t_{FLT\_STG\_VRCM}$	VRCM short to ground detection filter time	(1)	17	20	23	µs	SFx, SRx
$t_{FLT\_R\_LOW\_VRCM}$	VRCM low resistance detection filter time	(1)	12	15	18	µs	SFx, SRx
$t_{FLT\_R\_HIGH\_VRCM}$	VRCM high resistance detection filter time	(1)	12	15	18	µs	SFx, SRx
$t_{FLT\_FET\_TEST}$	VRCM short to battery/ ground detection filter time during LS/HS FET test	(1)	0.8	1	1.2	µs	SFx, SRx
$t_{ON\_VRCM\_MUX\_PARALLEL}$	VRCM mux simultaneous activation on SRx and SFx	(1)	-	56	-	µs	SFx, SRx
$t_{TO\_FET\_TEST}$	LS/HS FET test timeout	(1)	190	200	210	µs	SFx, SRx
$t_{CONV\_ADC\_VRCM}$	VRCM current ADC single conversion time	-	-	80	-	µs	SFx, SRx
$t_{DEL\_LEA\_COMP}$	LEA comparator delay	Design info	-	-	2	µs	SFx, SRx
$t_{FLT\_LEA\_DIAG\_0}$	LEA diagnostic filter time selection 0	(1)	0.85	1.05	1. 25	µs	SFx, SRx
$t_{FLT\_LEA\_DIAG\_1}$	LEA diagnostic filter time selection 1	(1)	1.85	2.05	2. 25	µs	SFx, SRx
$t_{FLT\_LEA\_DIAG\_2}$	LEA diagnostic filter time selection 2	(1)	3.85	4.05	4. 25	µs	SFx, SRx
$t_{FLT\_LEA\_DIAG\_3}$	LEA diagnostic filter time selection 3	(1)	7.775	8.05	8.325	µs	SFx, SRx
$t_{TO\_LEA\_DIAG}$	LEA diagnostic test timeout	(1)	-	-	120	µs	SFx, SRx
$t_{DEP\_ADC\_PRE\_SETTL}$	Deployment ADC preconversion settling time	-	-	15.3	-	µs	-
$t_{DEP\_ADC\_POST\_SETTL}$	Deployment ADC post-conversion settling time	-	-	3.72	-	µs	-
$t_{DEP\_ADC\_CONV}$	Deployment ADC single conversion time	-	-	2.25	-	µs	-

1. *Guaranteed only in case CLKIN is provided with 1% accuracy and FLL is enabled.*

17.6 Remote sensor interface

-40 °C < T_J < 175 °C, ACTIVE or PASSIVE mode, 6 V < $V_{RSU\_SUP\_FLT}$ < 8.32 V, V_{VSYNC_UV} < V_{VSYNC} unless otherwise noticed.

Table 598. Remote sensor interface electrical characteristics

Symbol	Parameter	Condition/ Comments	Min	Typ	Max	Unit	Pin
I_{RSU}	Interface quiescent current	-	-35	-	-4	mA	RSUx
ΔI_{S_CM}	Sensor sink current common mode	Delta between min and max current sensor in common mode	22	-	30	mA	RSUx
ΔI_{S_LPM}	Sensor sink current low power mode	Delta between min and max current sensor in low power mode	11	-	15	mA	RSUx
V_{RSU_MAX}	Max. output voltage excluding sync. pulse	Internal regulation with I_{RSU} < - 4 mA	-	-	11	V	RSUx
$V_{RSU\_SYNC\_MAX}$	Max. output voltage including sync. pulse	(internal regulation, SYSBST = VIN) SYSBST = 10 V and 35 V	-	-	16.5	V	RSUx
R_{RSU}	RSU output resistance	From I_{RSU} = -4 mA to -65 mA	1.7	-	6.2	Ω	RSU_SUP_FLT, RSUx
$I_{STB\_RSU\_SUP\_FLT\_TH}$	Static reverse current into RSU_SUP_FLT	V_{RSUx} > $V_{RSU\_SUP\_FLT}$ + $V_{RSU\_STB\_OS}$	0.0	-	100	µA	RSU_SUP_FLT
$I_{STB\_VSYNC\_TH}$	Static reverse current into VSYNC or RSU_SUP_FLT	V_{RSUx} > V_{VSYNC} + $V_{RSU\_STB\_OS}$ (1)	0.0	-	100	µA	VSYNC, RSU_SUP_FLT
I_{STB_RSUx}	Static current into RSUx pin during STB condition	V_{RSUx} = 18V	-	-	1	mA	RSUx
$V_{RSU\_STB\_OS}$	Output short to battery offset threshold	-	10.0	-	100	mV	RSUx
I_{LIM_RSU}	Output current limit	I_{RSUx}	-130	-	-80	mA	RSUx
$\Delta_{ILIM\_OC\_PSI5}$	Difference between current limitation and short to ground threshold	ABS(I_{LIM_RSU}) - ABS(I_{STG})	5	-	-	mA	RSUx
I_{B_CM}	Quiescent current (normal mode sensor)	Default value used for algorithm initialization	-17.25	-15	-12.75	mA	RSUx
I_{B_LPM}	Quiescent current (low power mode sensor)	Default value used for algorithm initialization	-5.75	-5	-4.25	mA	RSUx

Symbol	Parameter	Condition/ Comments	Min	Typ	Max	Unit	Pin
I_{TH_CM}	Threshold (normal mode sensor)	Default value used for algorithm initialization	-31.05	-27	-22.95	mA	RSUx
I_{TH_LPM}	Threshold (low power mode sensor)	Default value used for algorithm initialization	-14.95	-13	-11.05	mA	RSUx
I_{LKGG}	Trigger point for fault leakage to ground detection	To ground, referred to base current I_B calculated value	-51.75	-45	-38.25	mA	RSUx
I_{STG}	Trigger point for fault short to ground detection	To ground, referred to total current measured at ADC output	-84	-73	-65	mA	RSUx
DAC_{RES}	DAC resolution	Design info	-	10	-	Bit	RSUx
I_{LSB}	LSB Current	Design info	-	93.75	-	µA	RSUx
V_{t2_CM}	Sync pulse amplitude common mode (trapezoidal and sinusoidal)	I_{RSU} = 4 - 35 mA Referred to RSUx voltage before sync pulse	3.8	4.2	-	V	RSUx
V_{t2_LPM}	Sync pulse amplitude trapezoidal low power mode	I_{RSU} = 4 - 35 mA Referred to V_{RSUx} voltage before sync pulse	2.8	3.2	-	V	RSUx
$V_{SYNCDROP}$	Sync drop-out voltage	V_{SYNC} - V_{RSUx} minimum delta voltage between VSYNC and RSUx pins to grant correct sync pulse	1	-	-	V	VSYNC, RSUx
$I_{LIM\_SYNC\_LS}$	Sync pulse current limit (LS driver)	-	50	-	80	mA	RSUx
I_{LIM_SYNC}	Static current limitation for each transceiver output RSUx	During sync pulse generator V_{RSUx} = GND	-130	-	-80	mA	RSUx
$N_{SENSORS}$	Total number of sensors connected to bus	Design info	1	-	4	-	RSUx
t_{Bit_125k}	Bit time (125kbps mode)	At the sensor connector	7.6	8	8.4	µs	RSUx
t_{Bit_189k}	Bit time (189kbps mode)	At the sensor connector	5	5.3	5.6	µs	RSUx
$t_{FLT\_OCTH\_RSU\_LONG}$	Over current detection deglitch filter time	Long filter time configuration during normal operation(2)	500	-	600	µs	RSUx
$t_{FLT\_OCTH\_RSU\_SHORT}$	Over current detection deglitch filter time	Short filter time configuration during normal operation(2)	50	-	60	µs	RSUx

Symbol	Parameter	Condition/ Comments	Min	Typ	Max	Unit	Pin
$t_{FLT\_SYNC\_INH\_RSU}$	Over current detection deglitch filter time for sync pulse inhibition	Filter time configuration during normal operation(2)	50	-	60	µs	RSUx
$t_{BLK\_OCTH\_RSU0}$	Over current detection blanking time 0	At interface power-on (BLKTxSEL = 0) (2)	4.6	-	5.4	ms	RSUx
$t_{BLK\_OCTH\_RSU1}$	Over current detection blanking time 1	At interface power-on (BLKTxSEL = 1) (2)	9.4	-	10.8	ms	RSUx
t_{STBTH}	Reverse battery blocking enable time	-	12	-	16	µs	RSUx
$t_{delay\_trap\_cm}$	DAC output to analog signal delay (trapezoidal common mode)	From DAC code commutation to analog signal at 2.1 V	186	-	2340	ns	RSUx
$t_{delay\_trap\_lpm}$	DAC output to analog signal delay (trapezoidal low power mode)	From DAC code commutation to analog signal at 2.1 V	197	-	2100	ns	RSUx
t_{delay_sin}	DAC output to analog signal delay (sinusoidal)	From DAC code commutation to analog signal at 2.1 V	221	-	2320	ns	RSUx
$t_{delay\_sync\_pulse}$	Sync pulse start delay time	From sync pulse start (without stagger time) to SPI_CS_RS rising edge(2)	-800	-	-600	ns	RSUx
$t_{SYNC\_DLY\_LONG}$	Sync pulse start long delay	Related to start of sync pulse on ch. N-1(2)	-11	-10	-9	µs	RSUx
$t_{SYNC\_DLY\_SHORT}$	Sync pulse start short delay	Related to start of sync pulse on ch. N-1(2)	-6	-7	-8	µs	RSUx
$t_{1\_TRAP\_CM}$	Sync signal earliest start trapezoidal common mode	From t_0 to sync pulse start(2)	-3	-2.10	-1.85	µs	RSUx
$t_{1\_TRAP\_LPM}$	Sync signal earliest start trapezoidal low power mode	From t_0 to sync pulse start(2)	-3.35	-2.34	-2	µs	RSUx
t_{1_SIN}	Sync signal earliest start sinusoidal	From t_0 to sync pulse start(2)	-7.05	-5	-4.4	µs	RSUx
t_0	Reference time	at 0.5 V on top of V(RSUx)	-	0	-	-	RSUx
t_2	Sync signal sustains start	at V_{t2_X} relative to t_0 rising edge(2)	-	-	7	µs	RSUx

Symbol	Parameter	Condition/ Comments	Min	Typ	Max	Unit	Pin
t_3	Sync signal sustains time pulse	at V_{t2_X} relative to t_0 falling edge(2)	16	-	22.5	µs	RSUx
t_4	Discharge time limit pulse	at 0.5 V on top of V(RSUx) falling edge(2)	-	-	35	µs	RSUx
$dV_{SR\_RISE\_RSU\_TRAP}$	Sync slope rising slew rate	Voltage signal from 20% to 80% of total pulse amplitude	0.43	-	1.5	V/µs	RSUx
$dV_{SR\_FALL\_RSU\_TRAP}$	Sync slope falling slew rate	Voltage signal from 80% to 20% of total pulse amplitude	-1.5	-	-0.25	V/µs	RSUx
$t_{FLT\_PSI5\_HF\_0}$	PSI5 deglitch filter time high frequency	F = 189 baud Configurable by SPI FLT = 0(2)(3)	0.99	1	1.1	µs	RSUx
$t_{FLT\_PSI5\_HF\_15}$	PSI5 deglitch filter time high frequency	F = 189 baud Configurable by SPI FLT = 15(2)(3)	1.9	1.93	2.02	µs	RSUx
$t_{FLT\_PSI5\_LF\_0}$	PSI5 deglitch filter time low frequency	F = 125 baud Configurable by SPI FLT = 0(2)(3)	1.48	1.5	1.58	µs	RSUx
$t_{FLT\_PSI5\_LF\_15}$	PSI5 deglitch filter time low frequency	F = 125 baud Configurable by SPI FLT = 15(2)(3)	2.41	2.44	2.53	µs	RSUx
$t_{FLT\_DIG\_LPF}$	Delay in A/D current conversion	Design info(2)fn(4)	1	1.5	2	µs	RSUx
$t_{FLT\_LKG\_RSU}$	Leakage deglitch filter time	(2)	10	-	15	µs	RSUx
$t_{WRITE\_EN\_DELAY\_LF}$	Data register write delay	Design info F = 125 baud Calculated from transition of last sensor bit to when data is available in SPI register(2)	-	-	19	µs	RSUx
$t_{WRITE\_EN\_DELAY\_HF}$	Data register write delay	Design info F = 189 baud Calculated from transition of last sensor bit to when data is available in SPI register(2)	-	-	14	µs	RSUx

Symbol	Parameter	Condition/ Comments	Min	Typ	Max	Unit	Pin
V_{VSYNC_UV}	Undervoltage on VSYNC pin	Delta between RSU_SUP_FLT and VSYNC	4.55	4.8	5	V	VSYNC
[DOS_UR7S_0602046]$T_{FLT\_VSYNC\_UV}$	Filter time of V_{VSYNC_UV}	(2)	8	10	12	µs	VSYNC
I_{VSYNC}	Current on VSYNC pin	For each channel, Sync pulse period 250 µs, C = 22 nF on RSUx pin	-	-	6	mA	VSYNC
$I_{RSU\_SUP\_FLT}$	Current on RSU_SUP_FLT pin	For each channel enabled, RSUx open	-	-	1	mA	RSU_SUP_FLT
$T_{OT\_RSU\_H}$	Over-temperature shut down threshold	-	185	-	215	deg	RSUx
$T_{OT\_RSU\_HYST}$	Over-temperature shut down threshold hysteresis	-	15	-	25	deg	RSUx
$t_{OT\_RSU\_FLT}$	Over-temperature shut down filter time	(2)	8	-	10	µs	RSUx

1. *The difference between $I_{STB\_RSU\_SUP\_FLT\_TH}$ and $I_{STB\_VSYNC\_TH}$ is that in the first case VRSU > VRSU_SUP_FLT but VRSU < VSYNC, while in the second case VRSU is greater than VRSU_SUP_FLT and VSYNC.*
2. *Guaranteed only in case CLKIN is provided with 1% accuracy and FLL is enabled.*
3. *The values have been verified by design.*
4. *Delay includes both A/D conversion and LPF.*

17.7 DC sensor interface

-40 °C < T_J < 175 °C, ACTIVE or PASSIVE mode, V_{SYSBST} > V_{UV_SYSBST}, unless otherwise noted.

Table 599. DC sensor interface electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
$V_{OUT\_DCS\_HIGH}$	DCS high output voltage regulation mode	DCS regulator enabled not in current limitation and R_{SENSOR} < $R_{DCS\_RANGE\_MAX}$	6	6.67	7.35	V	DCSx
$V_{OUT\_DCS\_LOW}$	DCS low output voltage regulation mode	DCS regulator enabled not in current limitation and R_{SENSOR} < $R_{DCS\_RANGE\_MAX}$	1.8	2	2.2	V	DCSx
$V_{OUT\_DCS\_SYSBST}$	DCS SYS output voltage	DCS regulator enabled	SYSBST-1.5V	SYSBST-0.6	SYSBST	V	SYSBST, DCSx
$I_{LIM\_DCS\_HIGH}$	DCS high current limitation regulation mode	DCS regulator enabled	-44	-40	-36	mA	DCSx
$I_{LIM\_DCS\_LOW}$	DCS low current limitation regulation mode	DCS regulator enabled	-22	-20	-18	mA	DCSx

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
$I_{LIM\_VOUT\_SYSBST}$	DCS SYS current limit	DCS V_{OUT_SYS} enabled	-20	-	-10	mA	DCSx
I_{DCS_RANGE1}	DCS current range 1	Design info	0	-	24	mA	DCSx
I_{DCS_RANGE2}	DCS current range 2	Design info	0	-	48	mA	DCSx
V_{DCS_RANGE1}	DCS voltage range 1	Design info	0	-	8	V	DCSx
V_{DCS_RANGE2}	DCS voltage range 2	Design info	-1.5	-	20.5	V	DCSx
R_{DCS_RANGE}	DCS resistance measurement range	Design info	50	-	5000	Ω	DCSx
$I_{PD\_STR\_DCS}$	DCSx disable current pulldown	Upon channel deactivation pull-down, $V_{DCS} \geq 1.5$ V	8.4	12	15.6	mA	DCSx
I_{PD_DCS}	DCSx weak current pull-down	$V_{DCS} \geq 1.5$ V	84	120	156	µA	DCSx
R_{PD_DCS}	DCSx resistive pull-down	-	300	500	700	kΩ	DCSx
$RATIO_{CURR\_LOW}$	Mirror ratio for current low range	With $I_{LIM\_DCS\_LOW}$ Design info	-	50	-	A/A	DCSx
$RATIO_{CURR\_HIGH}$	Mirror ratio for current high range	With $I_{LIM\_DCS\_HIGH}$ Design info	-	100	-	A/A	DCSx
dV_{SR_VOUT}	Output voltage slew rate	DCS regulator enabled	104	130	156	V/ms	DCSx
dI_{SR_IOUT}	Pull-down current slew rate	DCS regulator enabled	1	2.4	3.5	mA/µs	DCSx
$t_{PD\_STR\_DCS}$	Strong pull-down activation time	(1)	40	50	60	µs	DCSx
$t_{CROSS\_CONN\_0}$	Time required for cross-connection test	Settling time included, DCS_MEAS = 00(1)	296	303	310	µs	DCSx
$t_{CROSS\_CONN\_1}$	Time required for cross-connection test	Settling time included, DCS_MEAS = 01 (1)	485	495	505	µs	DCSx
$t_{CROSS\_CONN\_2}$	Time required for cross-connection test	Settling time included, DCS_MEAS = 10 (1)	862	880	898	µs	DCSx
$t_{CROSS\_CONN\_3}$	Time required for cross-connection test	Settling time included, DCS_MEAS = 11 (1)	1614	1647	1680	µs	DCSx
I_{CURR_MON}	Internal current conversion	Expected conversion code	-	41	-	LSB	-

1. *Guaranteed only in case CLKIN is provided with 1% accuracy and FLL is enabled.*

17.8 LIN interface and decoder

-40 °C < T_J < 175 °C, ACTIVE or PASSIVE mode, 6 V < VIN < 18 V, unless otherwise noted.

Refer to Figure 97 for external component configuration to be used for LIN interface testing.

Table 600. LIN interface and decoder electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
$V_{TX\_OH\_LIN}$	LIN high level (recessive state)	R_{PU_LIN} = 500 Ω, LIN_TX = VCCBCK	0.8VIN	-	VIN	V	LIN
$V_{TX\_OL\_LIN}$	LIN low level (dominant state)	R_{PU_LIN} = 500 Ω, LIN_TX = 0 V	-	-	1.2	V	LIN
$I_{LKG\_LIN\_DOM}$	LIN pin leakage current with transmitter in recessive state and LIN = 0V	LIN_TX = VCCBCK, VIN = 12 V	-1	-	-	mA	LIN
$I_{LKG\_LIN\_REC}$	LIN pin leakage current with transmitter in recessive state and LIN≥VIN	LIN_TX = VCCBCK, VIN = 8 - 18 V, LIN = 8 - 18 V, LIN ≥ VIN	-	-	20	µA	LIN
$I_{LKG\_LIN\_OFF}$	LIN pin leakage current with disabled interface and LIN≥VIN	VIN = 8 - 18 V, LIN = 8 - 18 V, LIN ≥ VIN	-	-	20	µA	LIN
I_{LIM_LIN}	Current limitation	LIN_TX = 0 V, LIN = 18 V	-180	-	-40	mA	LIN
$I_{LKG\_LIN\_GND\_LOSS}$	LIN pin leakage current in case of GND loss	Transmitter not dominant, VIN = 12 V, LIN = 0 - 18 V	-1	-	1	mA	LIN
$I_{LKG\_LIN\_VIN\_LOSS}$	LIN pin leakage current in case of VIN loss	Transmitter not dominant, LIN = 0 - 18 V	-	-	100	µA	LIN
$V_{TH\_RX\_DOM}$	Receiver recessive to dominant threshold	-	0.4VIN	0.45VIN	0.5VIN	V	LIN
$V_{TH\_RX\_REC}$	Receiver dominant to recessive threshold	-	0.5VIN	0.55VIN	0.6VIN	V	LIN
$V_{TH\_RX\_HYST}$	Receiver threshold hysteresis, $V_{TH\_RX\_REC}$- $V_{TH\_RX\_DOM}$	-	0.07VIN	0.1VIN	0.175VIN	V	LIN
$V_{TH\_RX\_CNT}$	Receiver center value, ($V_{TH\_RX\_REC}$+ $V_{TH\_RX\_DOM}$)/2	-	0.475VIN	0.5VIN	0.525VIN	V	LIN
$R_{PU\_INT\_LIN}$	LIN pin internal pull up resistance	LIN = 0 V	20	40	60	kΩ	LIN
$V_{D\_PU\_INT\_LIN}$	LIN pin internal pull up diode drop	I_{LIN} = -10 µA	0.4	0.7	1	V	LIN

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
C_{IN_LIN}	LIN internal input capacitance	Design info	-	-	30	pF	LIN
$T_{OT\_LIN\_H}$	Overtemperature shutdown threshold	-	185	-	215	deg	LIN
$T_{OT\_LIN\_L}$	Overtemperature shutdown recover threshold	-	165	-	195	deg	LIN
$T_{OT\_LIN\_HYST}$	Overtemperature shutdown threshold hysteresis	-	15	-	25	deg	LIN
t_{RX_PDEL}	Receiver propagation delay	t_{RX_PDEL} = max($t_{RX\_PDEL\_R}$,$t_{RX\_PDEL\_F}$), $t_{RX\_PDEL\_F}$ = t(0.5*V_{LIN_RX}) - t(0.45*V_{LIN}), $t_{RX\_PDEL\_R}$ = t(0.5*V_{LIN_RX}) - t(0.55*V_{LIN}); VIN = 12 V, C_{LIN_RX} = 20 pF; R_{PU_LIN} = 1 kΩ, C_{LIN} = 1 nF or R_{PU_LIN} = 660 Ω, C_{LIN} = 6.8 nF or R_{PU_LIN} = 500 Ω, C_{LIN} = 10 nF	-	-	6	µs	LIN_RX
$t_{RX\_PDEL\_SYM}$	Receiver propagation delay symmetry	$t_{RX\_PDEL\_SYM}$ = $t_{RX\_PDEL\_R}$ - $t_{RX\_PDEL\_F}$); VIN = 12 V, C_{LIN_RX} = 20 pF; R_{PU_LIN} = 1 kΩ, C_{LIN} = 1 nF	-2	-	2	µs	LIN_RX
D1	Duty cycle 1	$V_{TH\_RX\_REC\_MAX}$ = 0.744*VIN, $V_{TH\_RX\_DOM\_MAX}$ = 0.581*VIN; VIN = 7 - 18 V, t_{BIT} = 50 µs; D1 = $t_{LIN\_REC\_MIN}$/(2*t_{BIT}); R_{PU_LIN} = 1 kΩ, C_{LIN} = 1 nF or R_{PU_LIN} = 660 Ω, C_{LIN} = 6.8 nF or R_{PU_LIN} = 500 Ω, C_{LIN} = 10 nF; see Figure 96	0.396	-	-	-	LIN_RX
D2	Duty cycle 2	$V_{TH\_RX\_REC\_MIN}$ = 0.422*VIN, $V_{TH\_RX\_DOM\_MIN}$ = 0.284*VIN;	-	-	0.581	-	LIN_RX

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
		VIN = 7.6 - 18 V, t_{BIT} = 50 µs; D2 = $t_{LIN\_REC\_MAX}$/(2*t_{BIT}); R_{PU_LIN} = 1 kΩ, C_{LIN} = 1 nF or R_{PU_LIN} = 660 Ω, C_{LIN} = 6.8 nF or R_{PU_LIN} = 500 Ω, C_{LIN} = 10 nF; see Figure 96					
D3	Duty cycle 3	$V_{TH\_RX\_REC\_MAX}$ = 0.778*VIN, $V_{TH\_RX\_DOM\_MAX}$ = 0.616*VIN; VIN = 7 - 18 V, t_{BIT} = 96 µs; D3 = $t_{LIN\_REC\_MIN}$/(2*t_{BIT}); R_{PU_LIN} = 1 kΩ, C_{LIN} = 1 nF or R_{PU_LIN} = 660 Ω, C_{LIN} = 6.8 nF or R_{PU_LIN} = 500 Ω, C_{LIN} = 10 nF; see Figure 96	0.417	-	-	-	LIN_RX
D4	Duty cycle 4	$V_{TH\_RX\_REC\_MIN}$ = 0.389*VIN, $V_{TH\_RX\_DOM\_MIN}$ = 0.251*VIN; VIN = 7.6 - 18 V, t_{BIT} = 96- µs; D4 = $t_{LIN\_REC\_MAX}$/(2*t_{BIT}); R_{PU_LIN} = 1 kΩ, C_{LIN} = 1 nF or R_{PU_LIN} = 660 Ω, C_{LIN} = 6.8 nF or R_{PU_LIN} = 500 Ω, C_{LIN} = 10 nF; see Figure 96	-	-	0.590	-	LIN_RX
$t_{OT\_LIN\_FLT}$	Overtemperature shutdown filter time	(1)	6	8	10	µs	LIN
$t_{LIN\_TX\_DOM\_TO}$	LIN_TX dominant timeout	(1)	9	12	15	ms	LIN_TX
$t_{LIN\_PERM\_REC\_TO}$	Permanent recessive timeout	(1)	30	40	50	us	LIN_TX, LIN_RX
$t_{LIN\_PROT\_TO}$	Protocol timeout	(1)	4	5	6	s	LIN

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
$t_{LIN\_PERM\_DOM\_TO}$	Permanent dominant timeout	(1)	9	12	15	ms	LIN_RX
$t_{LIN\_MSG\_TO}$	Valid message timeout	MSG_TO = 00(1)	0.45	0.5	0.6	s	LIN_RX
$t_{LIN\_MSG\_TO}$	Valid message timeout	MSG_TO = 01(1)	0.94	1	1.05	s	LIN_RX
$t_{LIN\_MSG\_TO}$	Valid message timeout	MSG_TO = 10(1)	1.85	2	2.15	s	LIN_RX
$t_{LIN\_MSG\_TO}$	Valid message timeout	MSG_TO = 11(1)	3.75	4	4.25	s	LIN_RX
$V_{PGND\_LOSS\_TH}$	PGND ground loss detection threshold	$V_{SUBGNDx}$ = 0V	100	200	300	mV	PGND
$t_{PGND\_LOSS\_FLT}$	PGND ground loss detection filter time	(1)	8	10	12	µs	PGND

1. *Guaranteed only in case CLKIN is provided with 1% accuracy and FLL is enabled.*

Figure 96. LIN timing description

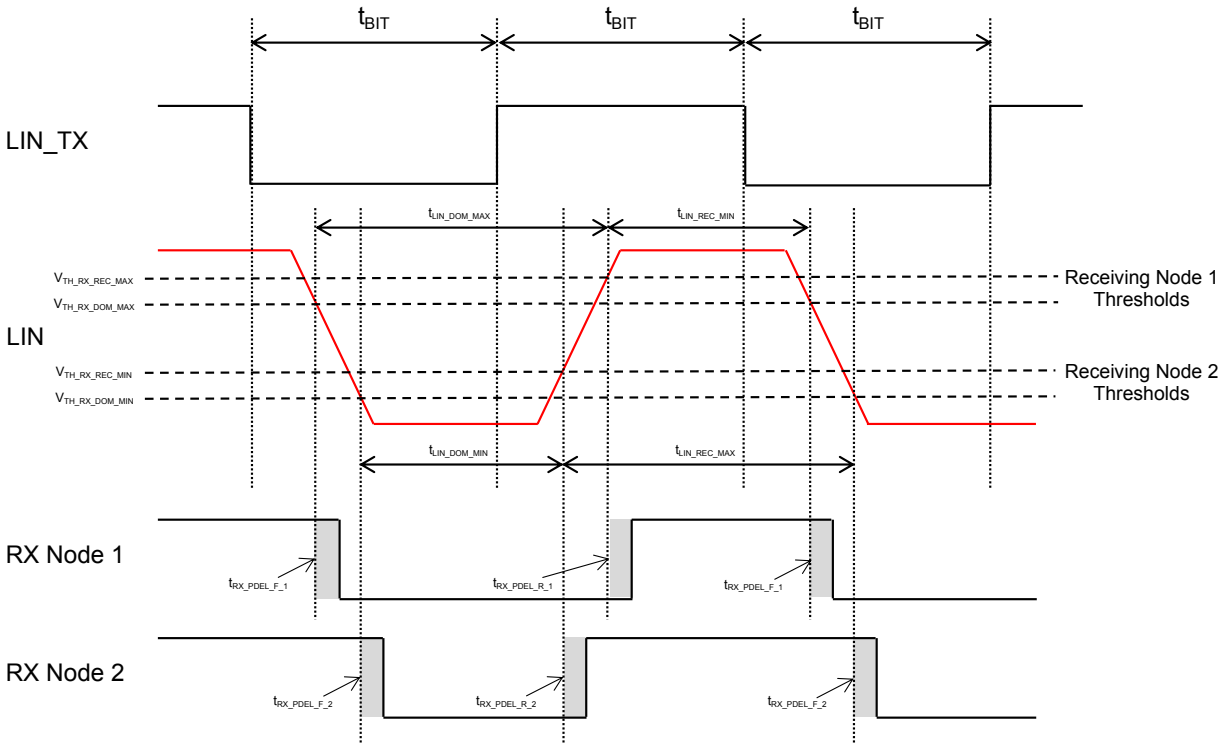
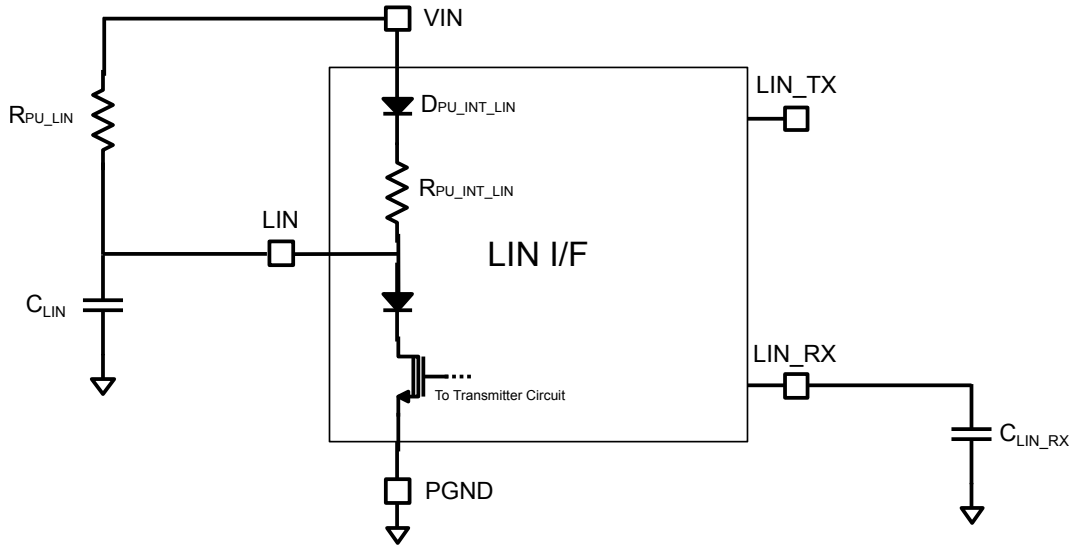


Figure 97. **LIN test circuit for duty cycles**



17.9 Arming/passenger inhibit logic

-40 °C < T_J < 175 °C, ACTIVE or PASSIVE mode, unless otherwise noted.

Table 601. **Arming/passenger inhibit logic electrical characteristics**

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
$V_{TH\_H\_ACL}$	ACL input voltage thresholds	-	1.92	1.99	2.06	V	-
$V_{TH\_L\_ACL}$	ACL input voltage thresholds	-	1.5	1.56	1.62	V	-
V_{HYS_ACL}	ACL hysteresis	-	0.39	0.475	0.56	V	-
R_{PD_ACL}	ACL pull-down resistance	V_{ACL} = 3.3 V	140	210	280	kΩ	-
t_{ACL_HI}	ACL period time thresholds	-	213	-	237	ms	-
t_{ACL_LO}	ACL period time thresholds	-	168	-	187	ms	-
$t_{ON\_ACL\_HI}$	ACL on-time thresholds	-	154	-	171	ms	-
$t_{ON\_ACL\_LO}$	ACL on-time thresholds	-	114	-	126	ms	-
t_{VALID_ACL}	Scrap validation T_{ACL} and T_{ON_ACL} valid	-	3	-	-	cycles	-
$t_{INVALID\_ACL}$	Scrap invalid T_{ACL} invalid	-	2	-	-	cycles	-
$t_{SCRAP\_TIMEOUT}$	Scrap timeout timer	-	520	550	580	µs	-
f_{SCRAP_SEED}	Scrap seed counter frequency	Design info	-	1	-	MHz	-
t_{PULSE_STRECH}	Arming enable pulse stretch time	-	28	32	35	-	-
t_{PULSE_STRECH}	Arming enable pulse stretch time	-	120	130	140	-	-

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
t_{PULSE_STRECH}	Arming enable pulse stretch time	-	245	261	280	-	-
t_{PULSE_STRECH}	Arming enable pulse stretch time	-	490	523	560	-	-
t_{PULSE_STRECH}	Arming enable pulse stretch time	-	1975	2096	2230	-	-
t_{PULSE_STRECH}	Arming enable pulse stretch time	-	3950	4193	4460	-	-
t_{CHPF}	HPF time constant	T = sample period N = HPF shift factor	-	$-T/ln(1-1/2^N)$	-	-	-
$t_{safing\_elaboration}$	SR calculation delay	-	-	2	-	µs	-
$t_{ARM\_UPDATED}$	ARMx update speed	From rising edge of CS (new sensor data) to ARM_INT register update	-	2	-	µs	-
$t_{E2E\_UPDATE\_TX}$	E2E update rates TX	Time between E2E REQ and RD E2E (from SPI rising edge of E2E TX REQ access to E2E_TX updated)	-	5	-	µs	-
$t_{E2E\_UPDATE\_RX}$	E2E update rates RX	Time to elaborate RX E2E UPDATE request (from SPI rising edge of E2E RX UPDATED REQ access to update the ARM RESULT)	-	5	-	µs	-
$t_{SNOOPING\_TIMEOUT}$	Snooping timeout timer	-	1.8	2	2.2	ms	-
$t_{DCS\_TIMEOUT\_PSINH}$	DC sensor timeout timer	DCS_TIMEOUT_PSINH_x = 00	0.45	0.5	0.6	s	-
$t_{DCS\_TIMEOUT\_PSINH}$	DC sensor timeout timer	DCS_TIMEOUT_PSINH_x = 01	0.94	1	1.05	s	-
$t_{DCS\_TIMEOUT\_PSINH}$	DC sensor timeout timer	DCS_TIMEOUT_PSINH_x = 10	1.85	2	2.15	s	-
$t_{DCS\_TIMEOUT\_PSINH}$	DC sensor timeout timer	DCS_TIMEOUT_PSINH_x = 11	3.75	4	4.25	s	-

17.10 General purpose low-side outputs

-40 °C < T_J < 175 °C, ACTIVE or PASSIVE mode, V_{VIN_GOOD} < V_{VIN} < V_{VIN_OV}, unless otherwise noted.

Table 602. GPO interface electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
$V_{SAT\_GPO\_H}$	Output saturation voltage	V_{GPODx}, I_{LOAD} = 75 mA	-	-	0.7	V	GPODx
$V_{SAT\_GPO\_H}$	Output saturation voltage	V_{GPODx}, I_{LOAD} = 50 mA	-	-	0.5	V	GPODx
I_{LIM_GPO}	Driver current limit	-	75	-	135	mA	GPODx
$I_{LIM\_TH\_GPO}$	Current limit detection threshold	GPO_LIM flag set	75	-	135	mA	GPODx
$I_{LIM\_TH\_GPO}$	I_{LIM_GPO} -$I_{LIM\_TH\_GPO}$	VGPODx = VIN (design info)	0	-	-	mA	GPOD
$V_{GPO\_TH\_HIGH\_1}$	Comparator high threshold voltage 1	HIGH_THRESHOLD_CONF = 00	56% VIN	60% VIN	64% VIN	V	GPODx

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
$V_{GPO\_TH\_HIGH\_2}$	Comparator high threshold voltage 2	HIGH_THRESHOLD_CONF = 01	61% VIN	66% VIN	71% VIN	V	GPODx
$V_{GPO\_TH\_HIGH\_3}$	Comparator high threshold voltage 3	HIGH_THRESHOLD_CONF = 10	70% VIN	75% VIN	80% VIN	V	GPODx
$V_{GPO\_TH\_HIGH\_4}$	Comparator high threshold voltage 4	HIGH_THRESHOLD_CONF = 11	74% VIN	80% VIN	86% VIN	V	GPODx
$V_{GPO\_TH\_LOW\_1}$	Comparator low threshold voltage 1	LOW_THRESHOLD_CONF = 00	18% VIN	20% VIN	22% VIN	V	GPODx
$V_{GPO\_TH\_LOW\_2}$	Comparator low threshold voltage 2	LOW_THRESHOLD_CONF = 01	22% VIN	25% VIN	28% VIN	V	GPODx
$V_{GPO\_TH\_LOW\_3}$	Comparator low threshold voltage 3	LOW_THRESHOLD_CONF = 10	30% VIN	33% VIN	36% VIN	V	GPODx
$V_{GPO\_TH\_LOW\_4}$	Comparator low threshold voltage 4	LOW_THRESHOLD_CONF = 11	36% VIN	40% VIN	44% VIN	V	GPODx
$V_{DYNAMIC\_PULLUP}$	GPO voltage threshold to disable output pull-up voltage	-	45% VIN	50% VIN	55% VIN	V	GPODx
$I_{GPO\_ON\_TH\_1}$	Current threshold ON 1	THRESHOLD_ON_CURR = 00	1	2	3	mA	GPODx
$I_{GPO\_ON\_TH\_2}$	Current threshold ON 2	THRESHOLD_ON_CURR = 01	2.4	4	5.6	mA	GPODx
$I_{GPO\_ON\_TH\_3}$	Current threshold ON 3	THRESHOLD_ON_CURR = 10	3.6	6	8.4	mA	GPODx
$I_{GPO\_ON\_TH\_4}$	Current threshold ON 4	THRESHOLD_ON_CURR = 11	4.8	8	11.2	mA	GPODx
$I_{GPO\_DYNAMIC\_PULLUP}$	GPO disable output pull-up current	V_{GPODx} = 0 V	-22	-16	-10	mA	GPODx
V_{GPO_PULLUP}	GPO output bias voltage	-	45% VIN	50% VIN	55% VIN	V	GPODx
I_{GPO_PULLUP}	GPO output bias current high side	V_{GPODx} = 0 V	-70	-53	-35	µA	GPODx
$I_{GPO\_PULLDOWN}$	GPO output bias current low side	V_{GPODx} = VIN = 18 V	10	-	80	µA	GPODx
$I_{LKG\_GPO\_OFF}$	GPOD output leakage Current OFF	VGPO = VIN power-off or sleep mode	-	-	5	µA	GPODx
$T_{JSD\_GPO\_H}$	Overtemperature shut down threshold		185	-	215	deg	GPODx
$T_{JSD\_GPO\_L}$	Overtemperature shutdown recover threshold	-	165	-	195	deg	GPODx
$T_{HYS\_TSD\_GPO}$	Overtemperature shut down hysteresis	-	15	-	25	deg	GPODx
$t_{GPO\_FLT\_TSD}$	Overtemperature shut down filter time	-	6	8	10	µs	GPODx
C_{GPO}	Load capacitor	Design info	6	-	-	nF	GPODx
$Ibias_{VIN}$	Bias current from VIN pin needed by each GPOx	V(GPO) = VIN = 13 V,driver in OFF condition. Design info	-	140	-	µA	GPODx
dV_{SRL_GPOx}	GPODx output voltage slew rate	30% - 70%; RLOAD = 250 Ω, C_{ECU} = 22 nF, VIN = 6 - 20 V	0.1	0.25	0.4	V/µs	GPODx

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
dV_{SRH_GPOx}	GPODx output voltage slew rate	30% - 70%; RLOAD = 250 Ω, C_{ECU} = 22 nF, VIN = 6 - 20 V	0.3	0.75	1.2	V/µs	GPODx
t_{FLT_OC}	Over current detection filter time	GPO driver ON(1)	10	12	14	µs	GPODx
$t_{GPO\_FLT\_MASK1}$	Fault mask time 1	BLANKING_DIAG = 00(1)	60	72	84	µs	GPODx
$t_{GPO\_FLT\_MASK2}$	Fault mask time 2	BLANKING_DIAG = 01(1)	100	120	140	µs	GPODx
$t_{GPO\_FLT\_MASK3}$	Fault mask time 3	BLANKING_DIAG = 10(1)	150	168	186	µs	GPODx
$t_{GPO\_FLT\_MASK4}$	Fault mask time 4	BLANKING_DIAG = 11(1)	200	224	248	µs	GPODx
$t_{GPO\_\_DYNAMIC\_PULLUP}$	GPO disable output pull-up current maximum time	(1)	45	50	55	µs	GPODx
$t_{GPO\_FLT\_CURR}$	Filter time current threshold ON	(1)	1.5	4	6	µs	GPODx
$t_{GPO\_FLT\_VHI}$	Filter time high voltage threshold	(1)	1.5	4	6	µs	GPODx
$t_{GPO\_FLT\_VLO}$	Filter time low voltage threshold	(1)	1.5	4	6	µs	GPODx
f_{PWM_LOW}	GPO PWM frequency low	Design info	-	100	-	Hz	GPODx
f_{PWM_HIGH}	GPO PWM frequency high	Design info	-	400	-	Hz	GPODx
f_{PWM_ACC}	GPO PWM frequency accuracy	(1)	-2	-	+2	%	GPODx
DC_{PWM}	GPO PWM duty cycle	Increment step = 0.4%(1)	0	-	100	%	GPODx
$t_{GPO\_FLT\_VHALF\_RISING}$	Filter time for $V_{DYNAMIC\_PULLUP}$ threshold rising edge	(1)	300	500	700	ns	GPODx
$t_{GPO\_FLT\_VHALF\_FALLING}$	Filter time for $V_{DYNAMIC\_PULLUP}$ threshold falling edge	(1)	1.5	4	4.5	us	GPODx

1. *Guaranteed only in case CLKIN is provided with 1% accuracy and FLL is enabled.*

17.11 Analog to digital converters (ADCs)

17.11.1 Power supply ADC queue

-40 °C < T_J < 175 °C, unless otherwise noted.

Table 603. Power supply ADC queue electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
$V_{RANGE\_ADC\_PWR}$	ADC input voltage range		0.1	-	2.5	V	-
$V_{REF\_ADC\_PWR}$	ADC reference voltage	-	2.46	2.5	2.54	V	-
N_{ADC_PWR}	ADC resolution	Design info	-	10	-	bit	-

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
DNL_{ADC_PWR}	Differential nonlinearity error (DNL)	Separation between adjacent levels, measured bit to bit of actual and an ideal output step. No missing codes. Design info	-1	-	+1	LSB	-
INL_{ADC_PWR}	Integral nonlinearity error (INL)	Maximum difference between the actual analog value at the transition between 2 adjacent steps and its ideal value. Design info	-3	-	+3	LSB	-
$ERR_{TOT\_ADC\_PWR}$	Total error	Includes INL, DNL, ADC reference voltage tolerance and quantization error	-15	-	+15	LSB	-
REP_{LSB_4}	Reproducibility, conversion result variation for constant input signal	4x sampling measurements. Guaranteed by design	-3	-	3	LSB	-
$t_{PWR\_ADC\_PRE\_SETTL}$	Pre-ADC settling time	-	-	15.3	-	µs	-
$t_{PWR\_ADC\_CONV}$	Single conversion time	-	-	2.25	-	µs	-
$t_{PWR\_ADC\_INT\_SETTL}$	Intra-queue settling time	-	-	14.1	-	µs	-
$t_{PWR\_ADC\_POST\_SETTL}$	Post- ADC settling time	-	-	3.72	-	µs	-
$RATIO_{DIV\_1}$	Divider ratio 1	$V_{IN\_RANGE\_1}$ = 0.1 V … 2.5 V	-	1	-	V/V	-
$RATIO_{DIV\_4}$	Divider ratio 4	$V_{INPUT\_RANGE\_4}$ = 1 V … 10 V	3.88	4	4.12	V/V	-
$RATIO_{DIV\_7}$	Divider ratio 7	$V_{INPUT\_RANGE\_7}$ = 1.5V … 17.5V	6.79	7	7.21	V/V	-
$RATIO_{DIV\_10}$	Divider ratio 10	$V_{INPUT\_RANGE\_10}$ = 2 V … 25 V	9.7	10	10.3	V/V	-
$RATIO_{DIV\_15}$	Divider ratio 15	$V_{INPUT\_RANGE\_15}$ = 3 V … 35 V	14.55	15	15.45	V/V	-
$I_{LEAK\_MUX\_ON}$	Total leakage on pin selected	-	0	-	240	µA	-

17.11.2 Sensor ADC queue

-40 °C < T_J < 175 °C, ACTIVE or PASSIVE mode, V_{SYSBST} > V_{UV_SYSBST}, unless otherwise noted.

Table 604. Sensor ADC queue electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
$V_{DCS\_ACC\_REL1}$	DCS voltage measurement accuracy active	V_{DCS} > 0.5 V Included ADC error without offset DCS_MEAS = 10	-5	-	+5	%	DCSx
V_{DCS_OS1}	DCS voltage measurement offset active	V_{DCS} > 0.5 V Offset DCS_MEAS = 10	-50	-	+50	mV	DCSx
$V_{DCS\_ACC\_REL2}$	DCS voltage measurement accuracy full scale	Included ADC error without offset from V_{DCS} -1 V to 20 V DCS_MEAS = 10	-3	-	+3	%	DCSx
V_{DCS_OS2}	DCS voltage measurement offset full scale	From V_{DCS} -1 V to 20 V DCS_MEAS = 10	-250	-	+250	mV	DCSx
$I_{DCS\_ACC\_REL1}$	DCS current measurement accuracy	With $I_{LIM\_DCS\_LOW}$ from 1mA to 15mA Included ADC error without offset DCS_MEAS = 10	-7	-	+7	%	DCSx

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
I_{DCS_OS1}	DCS current measurement offset	With $I_{LIM\_DCS\_LOW}$ from 1 mA to 24 mA Offset DCS_MEAS = 10	-150	-	+150	µA	DCSx
$I_{DCS\_ACC\_REL2}$	DCS current measurement accuracy	With $I_{LIM\_DCS\_LOW}$ from 15 mA to 24 mA Included ADC error without offset DCS_MEAS = 10	-4	-	+4	%	DCSx
I_{DCS_OS2}	DCS current measurement offset	With $I_{LIM\_DCS\_HIGH}$ from 1 mA to 48 mA Offset DCS_MEAS = 10	-300	-	+300	µA	DCSx
$I_{DCS\_ACC\_REL3}$	DCS current measurement accuracy	With $I_{LIM\_DCS\_HIGH}$ from 1 mA to 20 mA Included ADC error DCS_MEAS = 10	-7	-	+7	%	DCSx
$I_{DCS\_ACC\_REL4}$	DCS current measurement accuracy	With $I_{LIM\_DCS\_HIGH}$ from 20 mA to 48 mA Included ADC error DCS_MEAS = 10	-4	-	+4	%	DCSx
N_{DCS_ADC}	Resolution of DC sensor ADCs	Design info	-	10	-	bit	DCSx
V_{REF_ADC}	Voltage reference for voltage ADC	Design info	-	1.2	-	V	DCSx
I_{REF_ADC}	Current reference for Current ADC	Design info	-	480	-	µA	DCSx
$RATIO_{ACT}$	Divider ratio for DCSx voltage measurement active	Design info	-	6.67	-	V/V	DCSx
$RATIO_{EXT}$	Divider ratio for DCSx voltage measurement extended	Design info	-	18.33	-	V/V	DCSx
$RATIO_{VER}$	Divider ratio for VER measure	Design info	-	33.33	-	V/V	VER
$RATIO_{RSU}$	Divider ratio for RSUx measure	Design info	-	8	-	V/V	RSUx
$V_{DCS\_ACC\_VER}$	VER measurement accuracy	Total error with DCS_MEAS = 10	-50	-	50	LSB	DCSx
$V_{DCS\_ACC\_RSUx}$	RSUx measurement accuracy	Total error with DCS_MEAS = 10	-50	-	50	LSB	DCSx
$t_{S\_DCS\_0}$	Sampling time ADC	Settling time included, DCS_MEAS = 00(1)	24	25	26	µs	DCSx
$t_{S\_DCS\_1}$	Sampling time ADC	Settling time included, DCS_MEAS = 01(1)	40	41	42	µs	DCSx
$t_{S\_DCS\_2}$	Sampling time ADC	Settling time included, DCS_MEAS = 10(1)	71	73	75	µs	DCSx
$t_{S\_DCS\_3}$	Sampling time ADC	Settling time included, DCS_MEAS = 11(1)	134	137	140	µs	DCSx

1. *Guaranteed only in case CLKIN is provided with 1% accuracy and FLL is enabled.*

17.11.3 Deployment ADC queue

-40 °C < T_J < 175 °C, ACTIVE or PASSIVE mode, V_{SYSBST} > V_{UV_SYSBST}, unless otherwise noted.

Table 605. Deployment ADC queue electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
$RATIO_{DEP\_ADC\_MUX\_15}$	Deployment A/D multiplexer divider, division by 15	Voltage input range = 3 V - 37.5 V	14.55	15	15.45	-	SFx, SRx, SSx, SSxy
$RATIO_{DEP\_ADC\_MUX\_4}$	Deployment A/D multiplexer divider, division by 4	Voltage input range = 1 V - 10 V	3.88	4	4.12	-	TEST
$I_{LEAK\_DEP\_ADC\_MUX\_ON}$	Deployment A/D multiplexer, total leakage on selected pin	-	-	-	240	µA	-

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
$V_{DEP\_ADC\_REF}$	Deployment A/D reference voltage	-	2.4625	2.5	2.5375	V	-
N_{DEP_ADC}	Deployment A/D conversion number of bits	-	-	10	-	bit	-
$V_{DEP\_ADC\_RANGE}$	Deployment A/D input voltage conversion range	-	0.1	-	2.5	V	-
$ERR_{TOT\_DEP\_ADC}$	Deployment A/D total conversion error (divider factor accuracy excluded)	-	-15	-	15	LSB	-
$V_{LEA\_TH\_L}$	LEA presence detection threshold, low selection	Static measurement	0.28	-	1.75	V	SFx, SRx
$V_{LEA\_TH\_H}$	LEA presence detection threshold, high selection	Static measurement	0.56	-	2.5	V	SFx, SRx
E_{FET_TEST}	Energy transferred to load during LS/HS FET test	Design info	-	-	170	µJ	SFx, SRx
f_{LP_LRM}	Load resistance amplifier low-pass filter pole frequency	Design info	50	-	100	kHz	-
$t_{FLT\_STB\_VRCM}$	VRCM short to battery detection filter time	(1)	17	20	23	µs	SFx, SRx
$t_{FLT\_STG\_VRCM}$	VRCM short to ground detection filter time	(1)	17	20	23	µs	SFx, SRx
$t_{FLT\_R\_LOW\_VRCM}$	VRCM low resistance detection filter time	(1)	12	15	18	µs	SFx, SRx
$t_{FLT\_R\_HIGH\_VRCM}$	VRCM high resistance detection filter time	(1)	12	15	18	µs	SFx, SRx
$t_{FLT\_FET\_TEST}$	VRCM short to battery/ground detection filter time during LS/HS FET test	(1)	0.8	1	1.2	µs	SFx, SRx
$t_{ON\_VRCM\_MUX\_PARALLEL}$	VRCM mux simultaneous activation on SRx and SFx	(1)	-	56	-	µs	SFx, SRx
$t_{TO\_FET\_TEST}$	LS/HS FET test timeout	(1)	190	200	210	µs	SFx, SRx
$t_{CONV\_ADC\_VRCM}$	VRCM current ADC single conversion time	-	-	80	-	µs	SFx, SRx
$t_{DEL\_LEA\_COMP}$	LEA comparator delay	Design info	-	-	2	µs	SFx, SRx
$t_{FLT\_LEA\_DIAG\_0}$	LEA diagnostic filter time selection 0	(1)	0.85	1.05	1. 25	µs	SFx, SRx
$t_{FLT\_LEA\_DIAG\_1}$	LEA diagnostic filter time selection 1	(1)	1.85	2.05	2. 25	µs	SFx, SRx
$t_{FLT\_LEA\_DIAG\_2}$	LEA diagnostic filter time selection 2	(1)	3.85	4.05	4. 25	µs	SFx, SRx
$t_{FLT\_LEA\_DIAG\_3}$	LEA diagnostic filter time selection 3	(1)	7.775	8.05	8.325	µs	SFx, SRx
$t_{TO\_LEA\_DIAG}$	LEA diagnostic test timeout	(1)	-	-	120	µs	SFx, SRx
$t_{DEP\_ADC\_PRE\_SETTL}$	Deployment ADC preconversion settling time	-	-	15.3	-	µs	-
$t_{DEP\_ADC\_POST\_SETTL}$	Deployment ADC post-conversion settling time	-	-	3.72	-	µs	-
$t_{DEP\_ADC\_CONV}$	Deployment ADC single conversion time	-	-	2.25	-	µs	-

1. *Guaranteed only in case CLKIN is provided with 1% accuracy and FLL is enabled.*

18 Application circuit

Figure 98. **Application circuit**

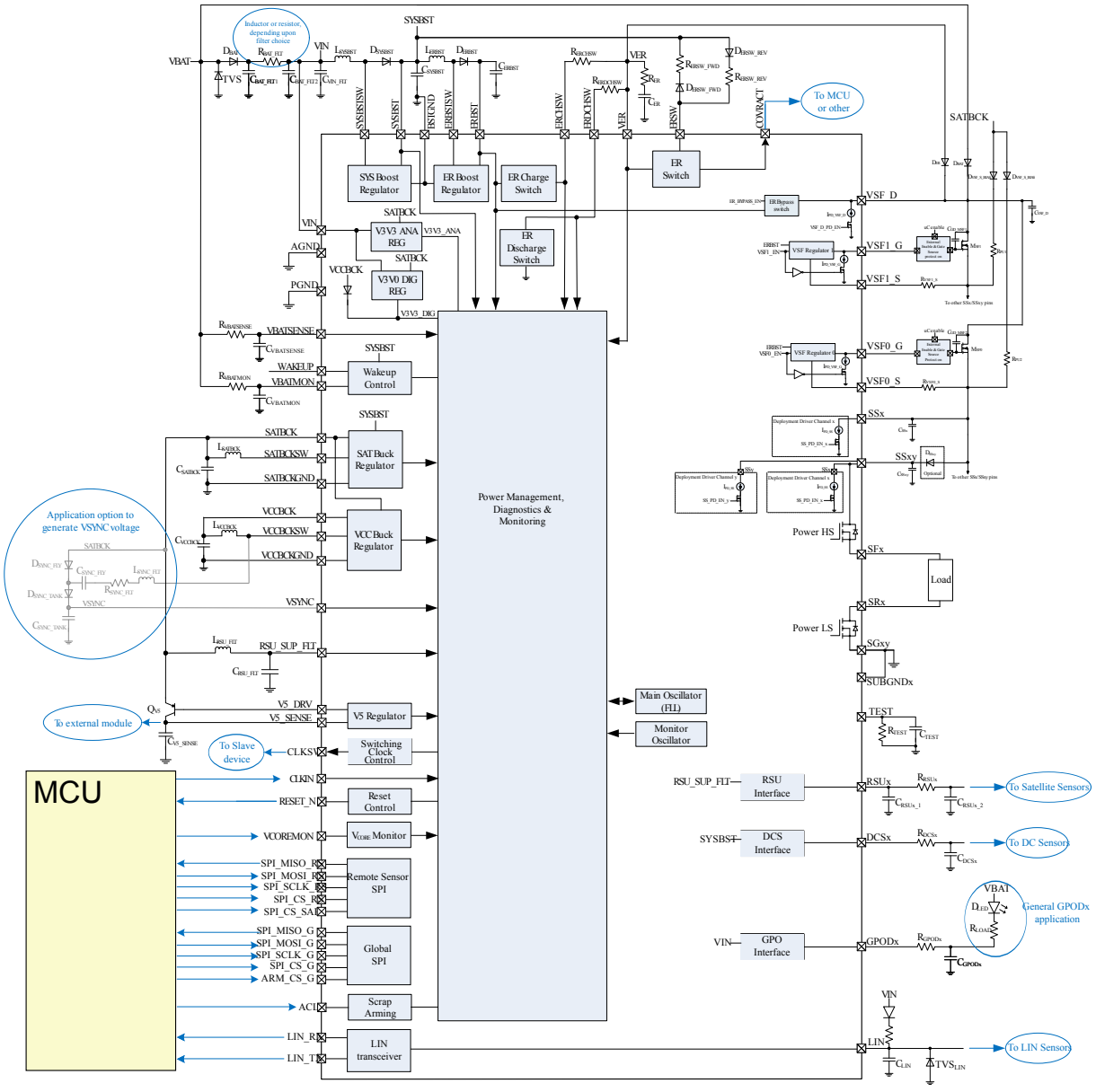


Table 606. **Bill of materials (BOM)**

Name	Component	Block/Usage	Min	Typ	Max	Unit
TVS	TVS	Battery transient protection	-	-	-	-
D_{BAT}	Diode	Battery protection	-	-	-	-
$R_{VBATMON}$	Resistor	Decoupling	-	1	-	kΩ
$C_{VBATMON}$	Capacitor	ESD protection	22	-	-	nF
$R_{VBATSENSE}$	Resistor	Decoupling	-	1	-	kΩ
$C_{VBATSENSE}$	Capacitor	ESD protection	22	-	-	nF

Name	Component	Block/Usage	Min	Typ	Max	Unit
C_{BAT_FLT1}	Capacitor	Battery filtering	-	4.7	-	µF
R_{BAT_FLT}	Resistor	Battery filtering	-	200	-	mΩ
C_{BAT_FLT2}	Capacitor	Battery filtering	-	4.7	-	µF
C_{VIN_FLT}	Capacitor	VIN filter	1.2	2.2	-	µF
D_{SYSBST}	Diode	SYS boost regulator	-	-	-	-
L_{SYSBST}	Inductor	SYS boost regulator	3.3	4.7	6.1	µH
R_{L_SYSBST}	Resistor	SYS boost inductor ESR	-	-	70	mΩ
C_{SYSBST}	Capacitor	SYS boost regulator	2.6	4.7	10	µF
R_{C_SYSBST}	Resistor	SYS boost capacitor ESR	-	20	-	mΩ
D_{ERBST}	Diode	ER boost regulator	-	-	-	-
L_{ERBST}	Inductor	ER boost regulator	23.1	33	130	µH
R_{L_ERBST}	Resistor	ER boost inductor ESR	-	-	650	mΩ
C_{ERBST}	Capacitor	ER boost regulator	1.2	2.2	-	µF
R_{C_ERBST}	Resistor	ER boost capacitor ESR	-	20	-	mΩ
C_{ER}	Capacitor	Energy reserve	2.2	-	52	mF
R_{ER}	Resistor	Energy reserve ESR	200	-	600	mΩ
R_{ERCHSW}	Resistor	Charge current sense	-	10	-	Ω
$R_{ERDCHSW}$	Resistor	Discharge current sense and limitation, ERBST_V_SEL bit = 0	33	47	68	Ω
		Discharge current sense and limitation, ERBST_V_SEL bit = 1	24	33	47	Ω
R_{ERSW_FWD}	Resistor	Current sense, ERSW to SYSBST path(1)	-	1	-	Ω
D_{ERSW_FWD}	Diode	ERSW to SYSBST path	-	-	-	-
R_{ERSW_REV}	Resistor	Current limitation, SYSBST to ERSW path	-	47	-	Ω
D_{ERSW_REV}	Diode	SYSBST to ERSW path	-	-	-	-
L_{SATBCK}	Inductor	SAT buck regulator	3.3	4.7	6.1	µH
R_{L_SATBCK}	Resistor	SAT buck inductor ESR	-	-	120	mΩ
C_{SATBCK}	Capacitor	SAT buck regulator	1.2	2.2	-	µF
R_{C_SATBCK}	Resistor	SAT buck capacitor ESR	-	10	-	mΩ
L_{VCCBCK}	Inductor	VCC buck regulator	3.3	4.7	6.1	µH
R_{L_VCCBCK}	Resistor	VCC buck inductor ESR	-	-	120	mΩ
C_{VCCBCK}	Capacitor	VCC buck regulator	1.2	2.2	-	µF
R_{C_VCCBCK}	Resistor	VCC buck capacitor ESR	-	10	-	mΩ
Q_{V5}	PNP BJT	V5 external power device	-	-	-	-
C_{V5_SENSE}	Capacitor	V5 voltage stabilization Given by 2 caps of 2.2 µF each, with 50% tolerance	1.1	-	6.6	µF
$R_{C\_V5\_SENSE}$	Resistor	V5 voltage stabilization capacitor ESR	0	-	20	mΩ
L_{RSU_FLT}	Inductor	RSU supply filter; optional	-	2.2	-	µH
C_{RSU_FLT}	Capacitor	RSU supply filter	2.2	-	22	µF
-	-	-	-	-	-	-

Name	Component	Block/Usage	Min	Typ	Max	Unit
C_{ER}	Capacitor	Energy reserve	2.2	-	30	mF
R_{ER}	Resistor	Energy reserve ESR	200	-	600	mΩ
D_{ER}	Diode	ER to VSF_D diode	-	-	-	-
D_{BAT}	Diode	Battery to VSF_D diode	-	-	-	-
$D_{VSF\_S\_BIAS}$	Diode	VSFx_S bias diode	-	-	-	-
C_{VSF_D}	Capacitor	Load capacitance on VSF_D	0	-	10	µF
M_{SFx}	Nch MOS	Safing FET	-	-	-	-
R_{PUx}	Resistor	VSF_S external bias resistor	210	221	232	Ω
R_{VSFx_S}	Resistor	Series resistance on VSFx_S	100	-	300	Ω
D_{SSxy}	Diode	SSxy decoupling diode	-	-	-	-
C_{SSx}	Capacitor	SSx pin loading capacitor	2.1	4.7	5.58	nF
C_{SSxy}	Capacitor	SSxy pin loading capacitor	2.1	4.7	5.58	nF
C_{GD_MSFx}	Capacitor	Gate to drain capacitance on safing FET	-	-	1.2	nF
R_{TEST}	Resistor	TEST pin pulldown resistor	-	2	3.3	kΩ
C_{TEST}	Capacitor	TEST pin capacitor	0	-	25	nF
C_{RSUx_1}	Capacitor	RSU damping capacitor, device side	17.6	22	26.4	nF
R_{RSUx}	Resistor	RSU damping resistance	-	3.3	-	Ω
C_{RSUx_2}	Capacitor	RSU damping capacitor, ECU side	1	2.2	6	nF
C_{DCSx}	Capacitor	DCS damping capacitor	-	47	-	nF
R_{DCSx}	Resistor	DCS damping resistance	-	10	-	Ω
R_{GPODx}	Resistor	GPODx ESD protection	10	-	-	Ω
C_{GPODx}	Capacitor	GPODx ESD protection	47	-	-	nF
R_{LOAD}	Resistor	Typical GPODx load	-	250	-	Ω
D_{LED}	LED	Typical GPODx load	-	-	-	-
TVS_{LIN}	TVS	STM ESDLIN03-1BWY	-	-	-	-
C_{LIN}	Capacitor	EMC protection on LIN	150	-	250	pF
R_{LIN_MASTER}	Resistor	pull up resistor for master operation only	900	1000	1100	Ω
D_{LIN_MASTER}	Diode	Serial diode mandatory for master operation	-	-	-	-

1. *Not necessary if C_{SYSBST} < 10 mF*

Chosen Q_{V5} transistor model PNP, 1.0, BCX53-10, 80.0 V, 1.0 A, SMD, SOT89.

Chosen M_{SFx} transistor model is dependent on:

- The number of deployment channels connected at MOS source node in the ECU
- The maximum number of parallel deployment events occurring on a single safing FET

18.1 Squib load model

Figure 99. **Squib load model**

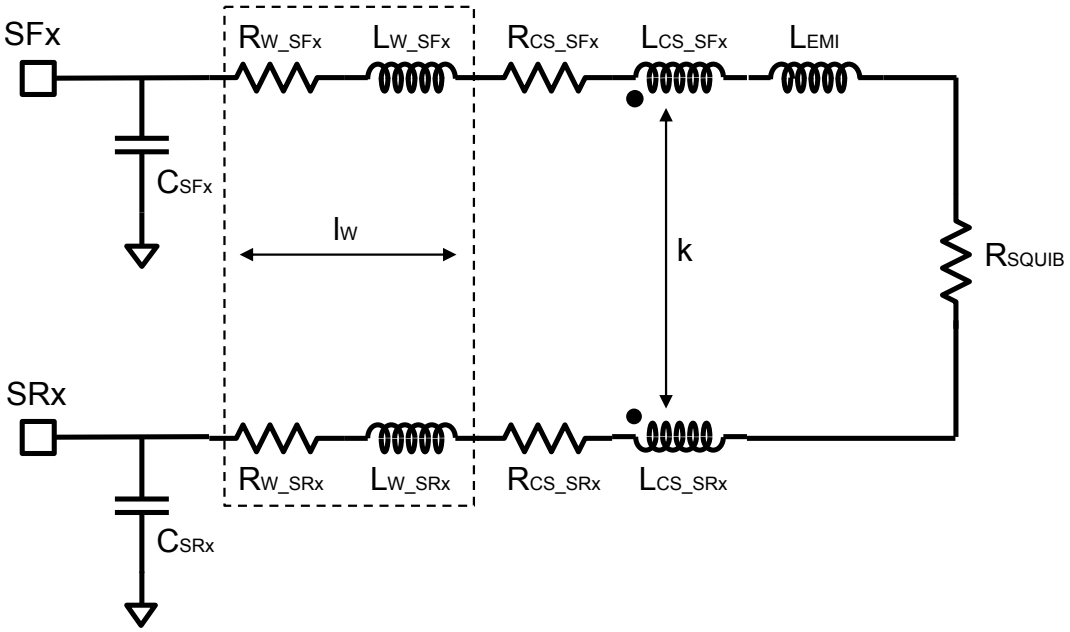


Table 607. **Squib load model parameters**

Name	Component	Block/Usage	Min	Typ	Max	Unit
C_{SFx}	Capacitor	ESD protection on SFx	13	22	138	nF
C_{SRx}	Capacitor	ESD protection on SRx	13	22	138	nF
l_W	Length	Wire length	1	-	10	m
R_{W_SFx}	Resistor	Wire contribution on SFx for l_W = 1 m	16.8	-	63.4	mΩ
R_{W_SRx}	Resistor	Wire contribution on SRx for l_W = 1 m	16.8	-	63.4	mΩ
L_{W_SFx}	Inductor	Wire contribution on SFx for l_W = 1 m	0.6	-	1.8	µH
L_{W_SRx}	Inductor	Wire contribution on SRx for l_W = 1 m	0.6	-	1.8	µH
R_{CS_SFx}	Resistor	Clock spring contribution on SFx (3 springs MAX)	0	-	0.7	Ω
R_{CS_SRx}	Resistor	Clock spring contribution on SRx (3 springs MAX)	0	-	0.7	Ω
L_{CS_SFx}	Inductor	Clock spring contribution on SFx	0	-	42.9	µH
L_{CS_SRx}	Inductor	Clock spring contribution on SRx	0	-	42.9	µH
k	Inductor coupling	Clock spring coupling	0.739	-	0.903	-
L_{EMI}	Inductor	EMI protection	0	-	7.7	µH
R_{SQUIB}	Resistor	Squib	1.7	2	2.5	Ω

18.2 LEA Load Model

Figure 100. **LEA load model**

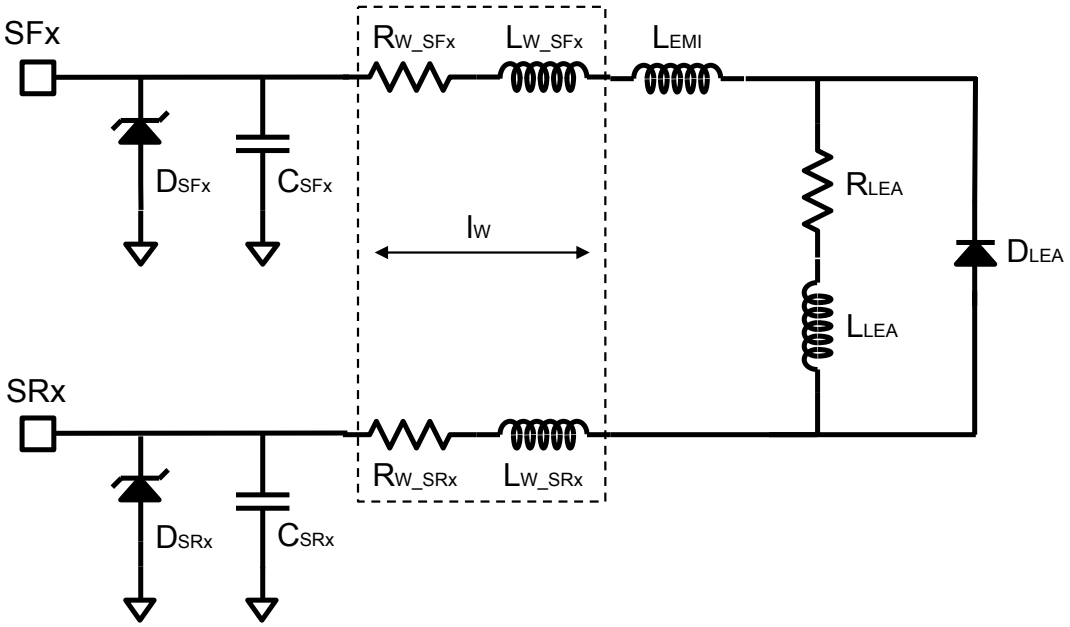


Table 608. **LEA load model parameters**

Name	Component	Block/Usage	Min	Typ	Max	Unit
D_{SFx}	Diode	SFx clamping	-	-	-	-
D_{SRx}	Diode	SRx clamping	-	-	-	-
C_{SFx}	Capacitor	ESD protection on SFx	13	22	138	nF
C_{SRx}	Capacitor	ESD protection on SRx	13	22	138	nF
l_W	Length	Wire length	1	-	10	m
R_{W_SFx}	Resistor	Wire contribution on SFx for l_W = 1 m	16.8	-	63.4	mΩ
R_{W_SRx}	Resistor	Wire contribution on SRx for l_W = 1 m	16.8	-	63.4	mΩ
L_{W_SFx}	Inductor	Wire contribution on SFx for l_W = 1 m	0.6	-	1.8	µH
L_{W_SRx}	Inductor	Wire contribution on SRx for l_W = 1 m	0.6	-	1.8	µH
L_{EMI}	Inductor	EMI protection	0	-	7.7	µH
L_{LEA}	Inductor	LEA	1.2	2.4	3.1	mH
R_{LEA}	Resistor	LEA ESR	1.67	2.34	3.13	Ω
D_{LEA}	Diode	LEA reverse protection	-	-	-	-

19 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

19.1 TQFP128 (14X14X1.0 mm, 8.0x8.0 mm exp. pad down) package information

Figure 101. TQFP128 (14X14X1.0 mm, 8.0x8.0 mm exp. pad down) package outline

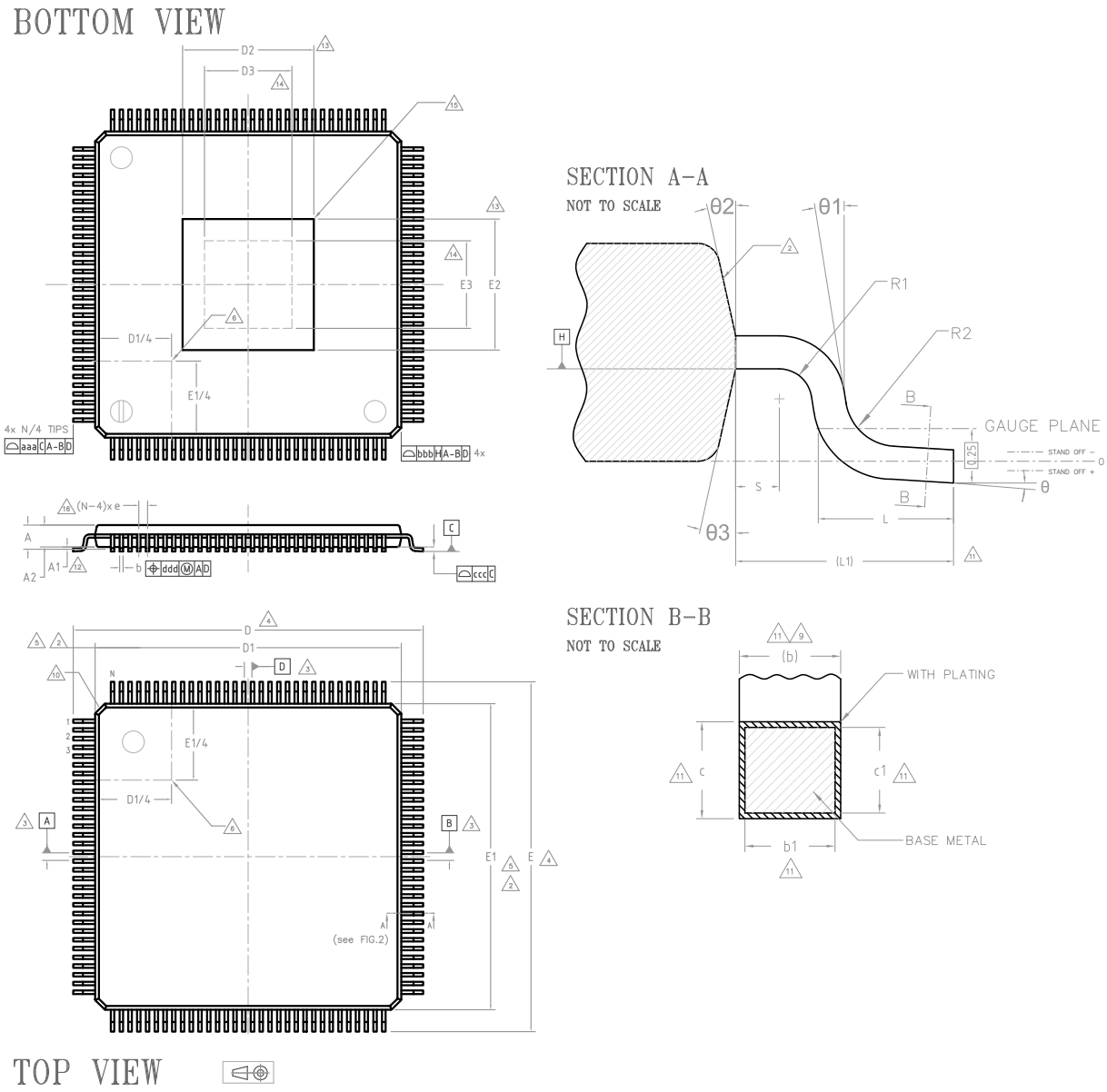
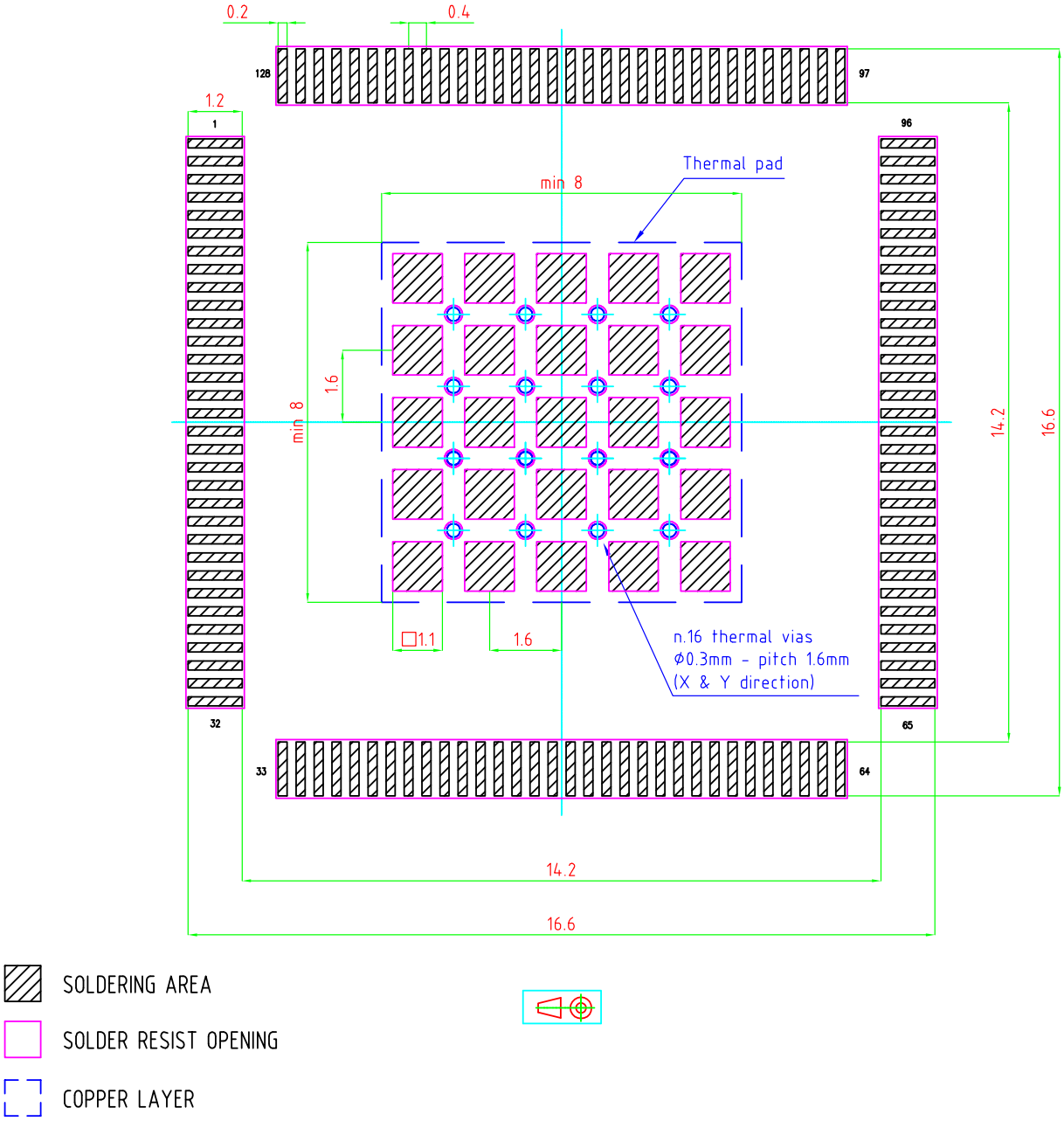


Table 609. TQFP128 (14X14X1.0 mm, 8.0x8.0 mm exp. pad down) package mechanical data

Symbol	Dimensions in mm		
	Min.	Typ.	Max.
Θ	0°	3.5°	7°
Θ1	0°	-	-
Θ2	11°	12°	13°
Θ3	11°	12°	13°
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
b	0.13	0.18	0.23
b1	0.13	0.16	0.19
c	0.09	-	0.20
c1	0.09	-	0.16
D	16.00 BSC		
D1	14.00 BSC		
D2(1)	-	-	8.18
D3(2)	6.80	-	-
e	0.40 BSC		
E	16.00 BSC		
E1	14.00 BSC		
E2(1)	-	-	8.18
E3(2)	6.80	-	-
L	0.45	0.60	0.75
L1	1.00 REF		
N	128		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
Tolerance of form and position			
aaa	0.20		
bbb	0.20		
ccc	0.08		
ddd	0.07		

1. *Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself. End user should verify D2 and E2 dimensions according to specific device application.*
2. *Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.*

Figure 102. **TQFP128 (14X14X1.0 mm, 8.0x8.0 mm exp. pad down) PCB footprint**



NOTE:
This is a draft proposal only and it might be not in line with customer or pcb supplier design rules.

Revision history

Table 610. **Document revision history**

Date	Version	Changes
24-Oct-2022	1	Initial release.

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